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Design of Analogue CMOS VLSI MEMS Sensor

*A dissertation presented in partial fulfillment
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by

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Abstract

There is an increasing demand of a highly sensitive and reliable pressure micro-sensor system, for implantable and non-implantable medical applications. The prerequisite of a miniaturized device for minimally invasive procedures, posed greater challenges in the complex integrated design of micro-system. Micro-sensor system designs in the recent advanced CMOS technologies are explored in this work for effective system miniaturization and improved performance. The material choices and geometry designs, which significantly influence the sensitivity and dynamic range of the micro-scale sensor devices, are well addressed. Co-integrations of MEMS devices with signal conditioning circuits that effectively reduce the parasitic effect are also performed for enhancing the overall system performance. In addition, system reliability is also improved with on-chip metal interconnections. The employed process technologies to a greater extent contributed to the high yield for these low cost micro-sensor systems.

This research focuses on the design of integrated CMOS MEMS capacitive pressure sensors for diverse bio-medical applications. Two monolithically integrated capacitive pressure micro-sensor systems are designed, fabricated and experimentally verified. A novel micro-electro-mechanical capacitive pressure sensor in SiGeMEMS process, vertically integrated on top of a 0.18 μm TSMC CMOS processed die is proposed. The perforated elliptic diaphragm, which is edge clamped at the semi-major axis is developed using poly-SiGe material. High performance on-chip CMOS conditioning circuits are also designed to achieve better overall sensitivity. Experimental results indicate a high sensitivity of around 0.12 mV/hPa along with a non-linearity of around 1% for the full scale range of applied pressure load. The L-clamp spring anchored diaphragm provided a wide dynamic range of around 900 hPa. Another integrated capacitive pressure micro-system, developed using the advanced standard IBM CMOS process in two geometrical designs is also proposed. A step-sided elliptic diaphragm that overcomes the CMOS process limitations is fabricated to achieve regulated membrane deflections and improved sensitivity. A foundry compatible post-process technique, for a lateral release length of 125 μm is also performed successfully on the 130 nm CMOS platform. A current cross mirroring technique is utilized to enhance the transconductance of an on-chip operational amplifier to achieve a high single stage gain. Sensitivities of the fluorosilicate sealed absolute pressure sensors were measured to be 0.07 mV/Pa and 0.05 mV/Pa for the elliptic and rectangular element, respectively. In addition, the linear capacitive transduction dynamic range was found to be 0.32 pF and 0.23 pF, respectively, for the elliptic and rectangular element.

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List of Acronyms and Abbreviations

| | |
|------------------------|--|
| AFM | Atomic Force Microscope |
| APM | Ammonia hydroxide-hydrogen Peroxide |
| ADC | Analog to Digital Converter |
| BEOL | Back End Of Line |
| BSIM | Berkeley Short-channel IGFET Model |
| CAD | Computer Aided Design |
| CHS | Chopper Stabilization |
| CMFB | Common Mode Feed Back |
| CMRR | Common Mode Rejection Ratio |
| CMOS | Complementary Metal Oxide Semiconductor |
| DRC | Design Rule Check |
| DRIE | Deep Reactive Ion Etching |
| DIP | Dual line in package |
| DUT | Device Under Test |
| DWW | Direct on wafer writing |
| EDA | Electronic Design Automation |
| ESD | Electrostatic Discharge |
| FC opamp | Folded Cascode Operational Amplifier |
| FC out+ | Positive going output voltage of folded cascode opamp |
| FC out- | Negative going output voltage of folded cascode opamp |
| FC_out _{diff} | Differential output voltage of folded cascode opamp |
| FEA | Finite Element Analysis |
| FEOL | Front End Of Line |
| GBW | Gain Bandwidth Product |
| GUI | Graphical User Interface |
| HPM | Hydrochloric acid-hydrogen peroxide |
| IC | Integrated Circuit |
| ICMR | Input Common Mode Range |
| ICP | Inductively Coupled Plasma |
| IEEE | Institute of Electrical and Electronics Engineers Inc. |
| LPF | Low Pass Filter |
| LPCVD | Low Pressure Chemical Vapor Deposition |

| | |
|------------------------|---|
| Lp_OUT+ | Positive going output voltage of LPF |
| Lp_OUT- | Negative going output voltage of LPF |
| M-Chopper | Modified Chopper Stabilization |
| MEMS | Micro Electromechanical System |
| MOSFET | Metal Oxide Semiconductor Field Effect Transistor |
| MST | Minimum Settling Time |
| MUMPS | Multi-User MEMS Processes |
| OTA | Operational Transconductance Amplifier |
| PMMA | Poly methyl methacrylate |
| PDMS | Polydimethylsiloxane |
| PGA | Pin Grid Array |
| PSRR | Power Supply Rejection Ratio |
| RF | Radio Frequency |
| RFC | Recycled Folded Cascode opamp |
| RIE | Reactive Ion Etching |
| Sensor _{out+} | Positive going output voltage of the sensor |
| Sensor _{out-} | Negative going output voltage of the sensor |
| SNR | Signal to Noise ratio |
| SDL | Schematic Driven Layout |
| SIP | System in package |
| THD | Total Harmonic Distortion |
| UGB | Unity Gain Bandwidth |
| VL_OUT _{diff} | Differential Output voltage of OTA |
| VM | Virtual Metrology |
| ZIF | Zero Insertion Force |

List of Symbols

| | | |
|-----------------|--------------------------------------|----------------------------|
| C | Capacitance | Farad |
| ϵ_r | Relative Permittivity | Farad per meter |
| ϵ_o | Permittivity of free space | Farad per meter |
| A | Area of the capacitor plate | Meter Square |
| λ | Channel length modulation | Micrometer |
| μ_n | Electron mobility | Meter square/Volts seconds |
| μm | Micrometer | |
| ϵ_{xx} | Normal strain in x direction | |
| ϵ_{yy} | Normal strain in y direction | |
| ϵ_{xy} | Shear strain | |
| w | Deflection of the plate | Micrometer |
| σ_{xx} | Normal stress in x direction | Newton/meter square |
| σ_{yy} | Normal stress in y direction | Newton/meter square |
| τ_{xy} | Shear stress | Pascal |
| E | Young's Modulus | Newton/meter square |
| ν | Poisson's ratio | |
| P_o | Applied Pressure | Hecto-Pascal |
| D | Flexural rigidity | Newton meter square |
| M_x | Bending moments in x direction | Newton Meters |
| M_y | Bending moments in y direction | Newton Meters |
| M_{xy} | Shear moments in x direction | Newton Meters |
| Pa | Pascal | Newton/meter square |
| g_m | Transconductance | Ampere/microvolt |
| k | Boltzmann's constant | Joules/Kelvin |
| T | Absolute temperature | Kelvin |
| R | Resistance | Ohms |
| B | Noise bandwidth | Hertz |
| W | Channel width of the MOSFET | Micrometer |
| L | Channel length of the MOSFET | Micrometer |
| I_D | DC Drain current of MOSFET | Amperes |
| i_d | Small signal drain current of MOSFET | Amperes |
| C_{ox} | Gate oxide capacitance | Farad |
| V_{cm} | Common mode voltage | Volts |
| A_{FC} | Open loop gain | Decibels |
| Q | Quality factor | |

Chapter 1

Introduction

1.1 Introduction to MEMS

Advancement in sensing scheme has led to the diagnosis and early treatment of killer diseases in the medical field. Reduced time in sensing biological quantities has saved human lives during critical illness. Sensors which are portable and implantable are in great demand for continuous monitoring of a patient's health. The implementation of miniaturized pressure sensors, micro needle, medicine dispenser and implantable pressure sensors has led to many non invasive diagnosis and treatment of diseases in the medical field [1]. This is due to the invention of a technology termed as MEMS, expanded as Micro-Electro-Mechanical system. Micro-Electro-Mechanical Systems are a technology that can be defined as miniaturized mechanical and electro-mechanical elements (i.e., devices and structures) that are made using the techniques of micro-fabrication. MEMS being a multidisciplinary technology are fabricated by exploiting the basic IC technology. There are different types of MEMS devices, which vary from relatively simple structures to extremely complex electromechanical systems with multiple moving elements. These devices are recently developed to include integrated electronics readout and control circuitry on the same substrate [2]. The main criteria for a structure to be a MEMS device is that there must be at least some element having some sort of mechanical functionality, whether or not these elements can move [2]-[9].

The functional elements of MEMS are miniaturized structures, sensors, actuators, and microelectronics. The important building blocks of the MEMS devices are micro-sensors and micro-actuators. Micro-sensors and micro-actuators are categorized as micro-transducers, which are defined as devices having dimensions of few micrometers that convert energy from one form to another. In the case of micro-sensors, the device typically converts a measured mechanical signal (non-electrical signal acquired from physical or chemical quantities) into an electrical signal. This electrical signal must be processed before it can be used for performing certain desired functions. The signal conditioning circuit (sensor readout) plays a very important role in making the measured quantity a beneficial signal. Generally, the processed signal will be either used to display the measured parameters or to drive an actuator for certain control functionality (converted back to mechanical energy).

The various MEMS market study reports that there is a significant increase in demand for pressure sensor manufacturing with numerous applications. Dixon et al., in the 2011 MEMS

device market study reported that pressure sensors has reached second place in terms of revenue among MEMS devices in the year 2010. Its growth increased to 26 percent from 2009 to hit \$1.22 billion. Growth at the end of 2011 was more modest at 6 percent, with revenue of \$1.30 billion, but double-digit expansion is predicted for 2012. As a result of steady market expansion, pressure sensors were expected to become the top MEMS device in terms of revenue in three years time. The 2013 MEMS market study revealed that pressure sensors soon found expanding use in the host of automotive, medical and industrial applications. This led the device to top the revenue list in 2014 as predicted; further, it is expected to reach \$1.9 billion in 2015 [6]. Medical electronics grabs the second place in exploiting some of the advantages of this integrated MEMS pressure device such as minimal size, low cost per device and low power requirement.

1.2 Motivation

Among the mechanical sensors, pressure sensor is found implemented extensively in bio-medical application. Integrated micro-pressure sensor has found tremendous use in implantable applications such as intraocular pressure measurement, intracranial pressure measurement, uterine activity monitoring, pediatric postoperative monitoring, and pulmonary artery pressure measurement. Further, non-implantable applications such as blood pressure measurement, sleep apnea monitoring, invasive and non-invasive treatments have also in recent years opted for this micro-device. In many applications, micro-devices are preferred over the macro-counterpart due to its high sensitivity and miniaturized size. Piezoresistive and Capacitive are the two generally preferred pressure sensing principles. Piezoresistive method due to its ease of batch production that does not require tedious post-processing (release etching) found employed tremendously in various applications; however, low dynamic range, moderate sensitivity and poor repeatability have significantly reduced the wide spread use of the piezoresistive sensing technique especially in medical field. Moreover, its poor thermal co-efficient requires additional temperature compensation circuit, as a result not only the system becomes bulky but the additional circuit component increases the power dissipation. Thus the device size and requirement of large battery, makes the piezoresistive device a poor choice for portable medical equipments.

The capacitive pressure sensing principle gained more importance due to its high sensitivity and wider dynamic range. Conventional sensors do not have an on-chip signal processing unit, hence the parasitic effects reduces the performance of this device [10]. Hybrid and monolithic integration of sensor device and readout circuit were later reported to improve the performance; however, efforts in the hybrid integration of sensor devices and associated conditioning circuitry in a single hermetic package have mostly resulted in poor performance of the sensing system. In addition, significant issues such as nonlinearity, reliability and environmental degradation made

hybrid integration technique a poor choice. Eventhough monolithic integration usually has a longer time to market compared to hybrid method; it offers lower overall production and packaging cost [7]. The unique monolithic integration of CMOS + MEMS devices using an industry standard CMOS process has immensely increased the performance and effectively reduced the size of the micro-sensor system. In addition, by proper choice of a thick BEOL metal layer as sensing element, the sensing capability can be comprehensively increased. Reliability, repeatability and longevity of the device can also be considerably improved with cautious post-processing technique. Eventhough CMOS technology allows designers to achieve a low power compact sensor; it poses challenges for adapting biocompatible material as the sensor element. A customized biocompatible thin film deposition in the order of few nanometers, on top of CMOS processed membrane overcomes this issue. This work is focused on the integrated design of the sensor micro-system using the deep nano-metric advanced CMOS process technologies. The novel structural design of the pressure sensors with three different geometries are designed with two different process technologies for performance improvement. Analysis of these devices were also performed and compared. To further enhance the linearity, sensitivity and reliability of the micro-sensor system, a CMOS sensing circuit that provides high gain, low noise floor and better linearity are also designed, analyzed and tested. The weak output signal of the sensor is processed by the extensively employed complex on-chip CMOS chopper stabilized operational amplifier. Continuous type low pass filter with better roll off removes the chopping frequency of the opamp. The final differential buffer stage will provide better driving capability for the readout circuit.

The targeted research inclination is towards the novel structural and electronic design of the pressure micro-sensor sensor system with a larger dynamic range, for a variety of uses in bio-medical applications. Different structures of the sensor to improve the above mentioned performance criteria of the pressure sensor is designed and analyzed using MEMS CAD tools. To explore and overcome the limitations imposed by the material properties on device performance, three pressure micro-sensors are designed with two different materials and their performances are analyzed using FEM (Finite Element Method) for accurate approximation. Three different geometries are fabricated using two process technologies; foundry compatible post-processing is also proposed for the successful release of the MEMS devices. The sensing circuitry that recovers and appropriately improves the signal quality of the poor sensor output is designed, simulated and analyzed using Mentor graphics CAD tool. Layout designs of the two micro-systems were carried out using L-Edit and Pyxis layout designer. The core sensing circuit for both these sensors remains the same; however, as the sensor dimensions vary so do, their responses; hence different amplifiers are designed for these micro-systems to achieve better performances. The amplifiers and the associated filtering and buffer circuits are designed using

mentor graphics tool to achieve better overall performance of the sensing system. The pressure micro-sensor systems are experimentally tested and their performances are compared.

1.3 Overview of the proposed research

The design objective of this work is to develop pressure sensors using poly-SiGe and aluminum as the structural material. Design of novel diaphragm geometries with on-chip readout sensing electronics that provides better process yield, considerable accuracy and improved reliability for diverse bio-medical applications is one of the key motives of this research. The design focuses on improvement in terms of the structural geometry, sensitivity, linearity and dynamic range of the sensor. Importance in improving the performance characteristics of the readout circuit such as high gain, low power dissipation, reduced die area and low noise floor are also equally considered. Two types of pressure sensor micro-systems are designed, fabricated and experimentally tested. SiGeMEMS micro-sensor monolithically integrated on top of the complex CMOS readout circuit is proposed. Two other micro-sensors integrated with high performance CMOS readout circuit stages in industry standard CMOS technology, are designed and fabricated overcoming the structural limitations imposed by the modern 130 nm CMOS IBM process. The cross sections of the micro-schemes are demonstrated in fig. 1.1 below.

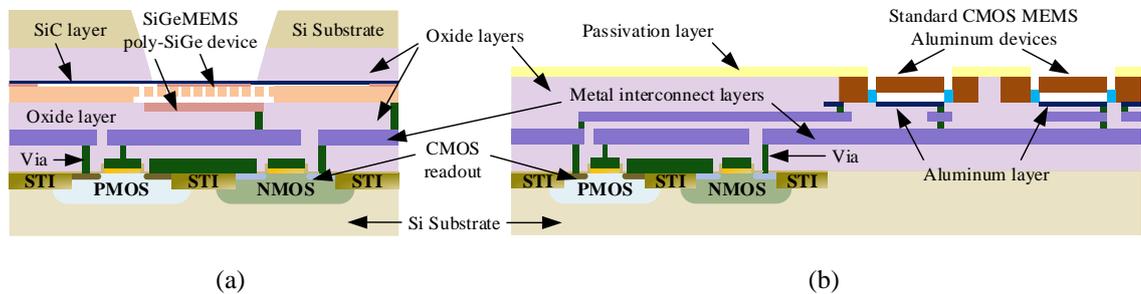


Fig.1.1: Cross section of, (a) CMOS + SiGeMEMS integrated pressure micro-sensor system, (b) Standard CMOS MEMS integrated pressure micro-sensor system

The issues that these designs have addressed to improve the performances compared to the previous designs are as follows:

- This novel design for the first time utilizes the modern technologies such as CMOS + SiGeMEMS and standard CMOS IBM 8RF-DM 130 nm technology with MEMS release post-processing to improve the performance of the pressure micro-sensor system, whereas the previous publications were designed in older technologies such as 2P4M and 1P6M process with low aspect ratio. Certain publications presented

designs that targeted 0.35 μm as the minimum feature size with a larger area and poor performance. Comparatively, this design has reduced the cost and die area.

- A novel CMOS integrated Micro-Electro-Mechanical capacitive pressure sensor in SiGeMEMS (Silicon Germanium Micro-Electro-Mechanical System) process is designed, analyzed and fabricated. Excellent mechanical stress–strain behavior of Polycrystalline Silicon Germanium (Poly-SiGe) is utilized effectively in this MEMS design to characterize the structure of the pressure sensor element. Perforated elliptic geometry diaphragm, anchored at the semi-major axis using L-clamp spring is designed and fabricated on top of the CMOS signal conditioning circuit (TSMC 180 nm technology). The custom clamped elliptic diaphragm yielded high sensitivity, wide dynamic range and good linearity compared to the other edge clamped diaphragms.
- High gain amplifier is proposed for signal conditioning the SiGeMEMS micro-sensor's output. Chopper Stabilized folded cascode opamp designed in 180 nm TSMC technology is gain boosted to get very high gain without introducing slow settling component, thus the speed of the overall SiGeMEMS sensor micro-system is not compromised. Furthermore, the second stage CS amplifier provides the desired voltage swing with low distortion and output impedance, providing better driving capability.
- Gm-C continuous filter that removes chopper amplifier residuals eliminates the use of power consuming stages such as oscillators and clock generators. Elliptic type filter design provides better roll-off even in the lower order; hence the transistor numbers and area are reduced. The reduced line width of the process drastically reduces the size of this complex circuit that incorporates at least five transconductance stages, thereby further reducing the area consumption.
- Low output impedance buffer stage is designed as a self biased circuit to provide driving capability for the sensor readout. Self biasing of this stage has further reduced the overall power dissipation by avoiding the requirement of bias circuitry. Current feedback in the design eliminates the need for increasing the g_m of the transistor; hence linearity is improved tremendously without increasing the aspect ratio of the transistors.
- Rectangular and nano-metric step-sided elliptic geometry micro-sensors, integrated with the CMOS readout in a standard 130 nm IBM CMOS process are also

designed and fabricated. An on-chip active switch provides the choice of parallel connection of these two devices, for significant improvement of dynamic range.

- Foundry based mass production compatible post-processing technique, that overcomes the issues of multi-layer standard CMOS MEMS process is addressed. A mix of wet and inductive plasma dry release etch, experimentally performed on a modern 8 metal BEOL 130 nm CMOS process is proposed. This process (also known by the acronym 8RFDM) contains 3 thin lowest metal layers (M1, M2 and M3), 2 thick middle metal layers (MQ and MG) and 3 thick top (upper) RF metal layers (LY (Al), E1 (Cu) and MA (Al)). The release process is done in the 3 upper metal layers MA, E1 and LY, as the sensors are constructed in this region.
- A g_m enhanced recycled folded cascode (RFC) opamp is designed and fabricated in IBM 130 nm CMOS technology for excellent amplification of the standard CMOS micro-sensors output. Current cross mirroring is employed for the significant improvement of the gain. The filter circuit and output buffer stage proposed for SiGeMEMS micro-system are redesigned to adapt for the 130 nm CMOS low supply voltage design.
- The integrated design of both the pressure micro-sensors with the sensing circuit reduces response time and the associated parasitic capacitance hence the sensitivity of the sensor is significantly improved. The reliability of the sensors was also promising, as the sensor and the circuit are not interconnected by external wires.

1.4 Thesis organization

The thesis is organized into eight Chapters. Chapter 2 outlines the overview of pressure micro-sensor system. The requirements of a highly sensitive micro-sensors and the associated on-chip readout circuit are discussed. It also includes the types of pick off techniques generally used in various reported micro-sensors. Concluding remarks on the reason for choosing absolute pressure sensor measurements and the pick-off techniques are provided.

In Chapter 3, introduction to CMOS MEMS integration and review of various integration methods are briefly discussed. Further, design process flow, model characterization and analysis of post-CMOS processed SiGeMEMS capacitive pressure micro-sensor element are detailed elaborately. The limitations and design strategies of the device layout are also outlined. The Chapter also includes modal analysis and post sealing process of the device. The Chapter concludes with the performance discussion of the designed SiGeMEMS micro-sensor.

Chapter 4 discusses the design aspects and performance improvement of SiGeMEMS sensor front end and interfacing circuit. CMOS design of M-chopper stabilized folded cascode opamp to achieve high gain with reduced noise is provided. Pole-zero locations are analyzed for the dual g_m -boosted stages and also the adapted stability methods are discussed. Further, it includes a detailed illustration of sensor interfacing circuit which performs single ended to differential conversion. Design of pre-amplification stage prior to FC opamp is briefly described. The Chapter continues with the discussion of bias circuit and sensor start-up circuit design. The layout design and simulation results are provided at the end.

Chapter 5 illustrates the output stages of the SiGeMEMS readout. Design and analysis of 4th order Gm-C low pass filter design in 180 nm CMOS TSMC technology is provided. Details of the 4th order elliptic topology that achieves better roll-off with less ripple are furnished. A self biased buffer stage with current feedback to achieve low gain error is described in detail. Layout and simulation result analysis are also discussed and concluded.

The standard CMOS design of integrated micro-sensor is described in Chapter 6. Design strategies of the two MEMS capacitive sensor design in the top three BEOL metal layers of IBM 130 nm CMOS technology are discussed. The CMOS process compatible technique to develop nano-metric edged elliptic geometry is provided in detail. COMSOL analysis to study the membrane deflection is also furnished. Low voltage on-chip CMOS sensor readout amplifier that employs current cross mirroring for transconductance enhancement is illustrated with the small signal analysis. Layout design of the integrated micro-sensor system is detailed. The Chapter concludes with the merits aspects of the CMOS MEMS design.

The etch processes which are feasible for industrial mass production is discussed in Chapter 7. The process to form a release etch window by opening the IBM CMOS fabricated triple layered passivation is also explored. Further, a mixture of wet and plasma dry etch process performed for the release of two different geometry pressure sensors is furnished. The Chapter continues with the discussion of an RIE etch performed for the lateral distance of 125 μm , in order to achieve stiction free release. Mechanical and electrical characterization done to confirm the full release and for the study of device surfaces are discussed. Details of post-release sealing are given and the concluding remarks for the successful device release are also provided at the end.

Chapter 8, furnishes the comprehensive experimental test setup and result discussions for both the pressure micro-sensor systems. Performance comparisons between the two fabricated systems and with other reported micro-sensors are done. The conclusion of the research work with the scope of expansion and future work are finally discussed in Chapter 9.

Chapter 2

System overview and literature review

2.1 Introduction to micro-sensor system

Micro-sensors are extremely small devices that detect information about a specific variable or physical quantities such as pressure, acceleration, angular motion or temperature. These sensors generally have a characteristic length of less than 1 mm. Integration of mechanical structures with sensing circuit that forms a single chip micro-sensor system has many advantages including high sensitivity and better linearity. Further, certain applications requiring controlling operations include actuators with the micro-sensor system on a single substrate for improved performances. Micro-structures (micro-sensor element) can be fabricated from single crystal silicon, polysilicon and metals. These materials are well known for their use in macro-scale structures, when employed in micro-scale fabrication their fundamental properties do not change, further, very few micro-defects are noted when compared to the macro-scale fabrication.

Over the past few decades the field of MEMS has created a path for researchers and developers to demonstrate an extremely large volume of micro-sensors for sensing different physical quantities including temperature, pressure, inertial forces, chemical species, magnetic fields, radiation, etc. Remarkably, these micro-machined sensors have demonstrated performances far exceeding than those of their macro-scale counterparts with better reliability. Thus, it is apparent that the high reliability demanding application such as bio-medical pressure measurement to adapt this miniaturized high performance pressure micro-sensor for the purpose of implantable continuous monitoring of health in critically ill-patients. The performance of the micro pressure sensor has outperformed the pressure sensor made using the most precise macro scale level machining techniques, in many ways. Not only is the performance of MEMS pressure devices, exceptional, but their method of production has led to the batch fabrication techniques, which is likely exploiting the fabrication method employed in the integrated circuit industry. Thus, production cost per device becomes low; as well the time to market is reduced. In general, the reasons for the popularity of the micro-sensor devices are:

- Low manufacturing cost due to the possibility of batch fabrication.
- Advanced IC manufacturing technology can be used, leading to the ability of comprehensive monolithic integration with high performance CMOS complex readout and control electronic circuit.

- Feasibility of designing the micro-sensors as an array with lower interconnection parasitic effects.
- Reduced die area.
- Miniaturized size, resulting in portability can be incorporated into wireless implantable medical devices.
- High Sensitivity.
- Low hysteresis.
- Reliability and Repeatability.
- Micro-components will yield low power consumption, can be massively employed and well maintained, and furthermore makes the system cheaper.

2.2. Sensing elements

Macro-scale pressure measurement systems are usually called pressure gauges or vacuum gauges. Some of the macro-scale versatile sensing elements are Bourdon tubes, diaphragms, capsules, and bellows. The Bourdon tube is a sealed tube that deflects in response to applied pressure [11], as the device size is large and susceptible to measurement drift with minute displacement; alternative pressure measurement techniques were developed. Capsules and bellows, suffered from slow response and less precision. In macro-scale all except diaphragms provided a fairly good performance. On the other hand, in micro-scale devices, the diaphragm sensing element has proven to be highly sensitive and linear. Further, they provide flexibility in customized device design for a specific application [3].

Sensing element can be broadly classified based on the sensing techniques as mechanical and electromechanical sensing elements. In mechanical gauges, the motion created by the sensing element is read directly by a dial or pointer [2]. The drawbacks in these elements are repeatability errors and limited frequency response; moreover, due to slow response they are suited only for slow changing measurements. On the other hand, electromechanical pressure sensors have faster reaction time, comparatively low hysteresis and repeatability errors. Moreover the associated readout circuit converts the applied pressure to an electrical signal with less delay that overcomes the drawbacks of mechanical sensors. Broad classifications of structural materials and engineering technologies have been employed in these devices, resulting in performance vs. cost tradeoffs and suitability for applications. The electrical output signal also provides a variety of choices for various applications [5].

The micro-scale pressure sensing element has found application even in harsh environments as they are less susceptible to vibration, temperature and dust. Portability aspect of these devices found immense use in wireless and handheld equipments. The micro-scale sensor elements

generally have a diaphragm element. Pressure sensing is achieved by picking the amount of displacement of this diaphragm by way of various pick-off techniques [11].

2.3. Pressure micro-sensor pick-off techniques

Pressure micro-sensors elements are typically designed as a diaphragm with different dimensions and geometries. This sensor is designed to measure characteristics of diaphragm deformation upon the applied pressure. There are three basic methods to pick-off (that is sensing of mechanical motion) the diaphragm deflection (mechanical motion) with the applied physical quantity as listed below:

- Capacitive (Electrostatic) detection
- Resistive (Conductive) detection
- Inductive (Amperometric) detection

The two most widely adapted detection techniques in micro-sensors are capacitive and resistive. These two techniques yielded better performances than the inductive pick-off with smaller device sizes. Furthermore, these two methods are more feasible and highly compatible to be developed using the modern process technologies.

2.3.1 Capacitive detection

In capacitive sensing pick-off, two membranes (or plates) usually of different materials separated by dielectric medium are employed. These two membranes are the electrodes of the capacitor. The dimensions of the top membrane (diaphragm) and the distance of these two membranes are designed according to the dynamic range requirement and the level of sensitivity. The top plate due to material's elasticity deforms under the influence of the external physical quantity (such as pressure). Bottom plate generally is a fixed membrane. When the distance between these two plates changes under the influence of measuring quantity, the capacitance between the plates varies. This variation in capacitance, which is relative to the measuring quantity, is then treated by an electronic signal conditioning circuit. The conditioned signal then can eventually be applied as an input to the actuator for control functions. Alternatively, the signal output can be simply used to display the sensed parameters for monitoring purpose. The capacitance of the parallel plate sensor can be found by [1]:

$$C = \frac{Q}{V} = \frac{\epsilon \cdot A}{d} \quad (1.1)$$

where Q is the charge on the plate, V the applied voltage, ϵ is the permittivity, A the Area of plate and d the distance between the plates.

2.3.2 Resistive detection

All material used for fabrication of structures or micro-sensors have resistance to the flow of electrons. When these structures or micro-sensors are stressed by a mechanical load or force its resistivity changes. The changing resistivity of a semiconductor due to applied mechanical stress is called piezoresistivity. The change of resistance in metal devices due to an applied mechanical load was first discovered in 1856 by Lord Kelvin. Since single-crystal silicon became the material of choice for the design of analog and digital circuits, many researches were conducted to study its property. The large piezoresistive effect in silicon and germanium was first discovered in 1954 by Smith. In semiconductors, applied stress changes inter-atomic spacing that affects the band gaps. This makes it easier or harder for electrons to be raised into the conduction band [2], resulting in the change of resistivity of the semiconductor. Piezoresistivity is defined by [1]:

$$\rho_{\sigma} = \frac{\left(\frac{\partial \rho}{\rho} \right)}{\epsilon} \quad (1.2)$$

where $\partial \rho$ is the change in resistivity, ρ the original resistivity and ϵ is the strain. The change in resistance due to piezoresistivity is much greater than a simple change in geometry and so a semiconductor can be used to create a much more sensitive sensor. The resistance of silicon changes not only due to the stress dependent change of geometry, but also due to the stress dependent resistivity of the material. This results in larger gauge factors than those observed in metals. The effect of resistance change due to stress can be employed in sensors for measuring physical and chemical quantities. Generally, the sensed signal will be weak; hence a signal processor is needed in order to beneficially apply this sensed information for the purpose of actuation.

2.4 Pressure micro-sensor system requirements and types

The recent achievements in realization of micro-scale structures with different geometries and materials using today's advanced CMOS technologies have broadened the spectrum of pressure sensor implementation in the medical field. Pressure micro-sensor system in its basic form can be defined as a transducer that converts physical quantities occurring in the human body into measuring currents and voltages in the range of a few micro-amps and micro-volts respectively. The important features that a micro-level bio-medical pressure sensor is expected to have are:

- Good Sensitivity
- Large dynamic range
- High precision of sensing
- Excellent resolution
- High accuracy
- Better offset
- Highly linear with respect to change in temperature
- Low hysteresis
- Fast response time
- High dynamic linearity
- Repeatability

Pressure sensors are immensely employed in critical medical care and general health care, some of them can be listed as below [11]-[18]:

- Noninvasive and invasive blood pressure monitors
- Fetal heart rate monitors
- Inhalers and ventilators
- Wound management
- Patient monitoring systems
- Spirometer and respiratory therapy devices
- Sleep apnea (CPAP machines)
- Dialysis systems
- Drug delivery systems
- Hospital beds

Thus, it can be stated that the sensor has become an integral part of human life. It is the most researched and fabricated sensor in MEMS industry and is expected to further increase in production and shipping till 2015. Over the past two decades, many techniques were developed to measure pressure, a vital physical quantity. Pressure, P , is defined as force per unit area, can be mathematically given as [19]:

$$P = \frac{F}{A} \quad (1.3)$$

where F is the force acting on the measurand and A , the area of the measurand. Pressure measurement can be generally referred with fluids, such as liquids and gases.

2.4.1 Types of pressure measurements

The pressure sensor device measures the pressure of a given physical quantity relative to a known pressure level. Based on the reference pressure they can be categorized into three types as shown in fig. 2.1:

- *Absolute pressure measurement* – pressure sensors that have vacuum as their referents are termed as an absolute pressure sensor. It provides pressure measurements relative to either perfect vacuum (free space) or moderate vacuum (around 0.6 Pa pressure). The measured values are generally independent of the environment, weather or altitude.
- *Differential pressure measurement* - the difference between two process pressures is usually provided by the differential pressure sensor. Two types of pressure measurement are possible by designing two pressure ports. The bidirectional differential pressure sensor provides the possibility of measuring both positive and negative pressures, whereas, the unidirectional differential pressure sensor provides only positive pressure measurement.
- *Gauge pressure measurement* – sensors that measure the physical quantity relative to the ambient or atmospheric pressure (usually 1013.25 hPa) are referred to as gauge pressure sensor. Their measured outputs are either positive or negative depending on the sensed pressure. If the measurand is above the atmospheric pressure then the measured value is positive else a negative pressure value is obtained.

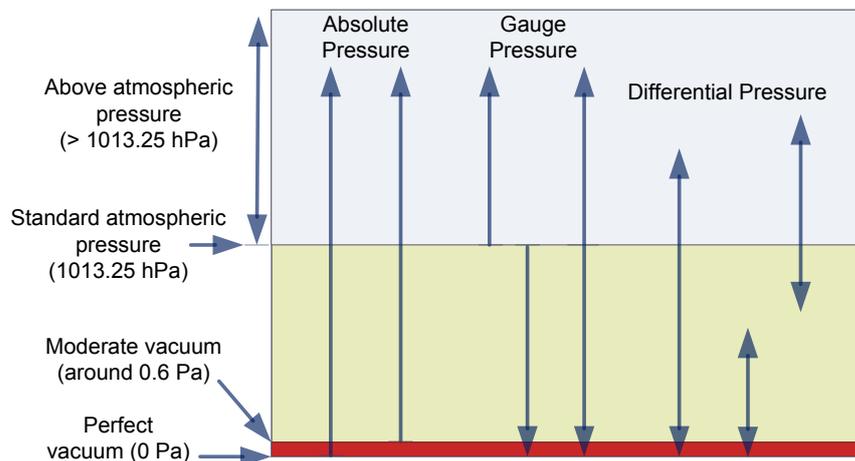


Fig. 2.1: Types of Pressure measurement [11]

As evident from the above discussion that absolute pressure sensor requires no special process for developing pressure port inlet, their fabrication becomes simpler and cheaper. Furthermore, it is not susceptible to any environmental changes, weather conditions or altitude levels, as their

reference cavity is sealed under vacuum; hence their reliability is higher. If the geometries and dimensions are designed precisely their dynamic range will be much larger than other measuring methods. Therefore, absolute pressure measurement technique is the best suited method for bio-medical pressure measurement application, where higher order of precision, larger dynamic range and sound reliability is in immense demand. Most of the biomedical pressure sensor uses non-SI nano-metric unit of pressure (mm Hg); yet, this work uses Pascal (Pa) being an SI unit of force per unit area measurement. In most sections of this thesis hecto-Pascal (hPa) unit is applied, as pressure conversion between mm Hg and hPa is almost 1 [12].

2.4.2 Readout circuit requirement

As stated earlier, the outputs of the sensor or transducer are generally low and weak, hence must be processed before it is made beneficial for desired application. An electronic signal conditioning circuit or simply a sensor readout circuit having high gain, better accuracy and low noise is necessary to do so. One of the fundamental factors that influence the performance of the MEMS micro-sensor system is the signal processing capability of the readout circuit [12]-[18]. There is a trade-off between sensitivity and electronic noise floor, hence designing a low noise sensing circuit with very low noise floor is critical. Even though the sensor will be designed with on-chip readout circuit to reduce the associated noise, the readout circuit will still provide noise in the range of few hundred nano-volts causing the total noise floor to increase [19]. Signal readout front end offers amplification and filtering of transducer signal and consequently, provides compensation and calibration. Compensation technique reduces the temperature effects, supply voltage variations, offset. Calibration significantly improves the sensor's parameters such as offset, sensitivity and linearity [20].

Sensing a minuscule change in the pressure imposes a greater responsibility on the electronic part for proper readout. Piezoresistive type sensor does not provide greater design complexity in terms of the precision readout of the transducer signal, however, suffers a greater deal of thermal noise and offset, hence the readout circuit with inherent temperature compensation capability is needed. In Capacitive type pressure sensors; the main advantage of the post-CMOS surface micro machining is the low interconnect capacitance and resistance between the MEMS part and the electronic circuit [21]. However, it leads to low proof mass and low sense capacitance. The sense capacitance (C_{sense}) and the capacitance variation (ΔC) are really small, normally in the range of few hundred femto-farads and 1-100 auto-farads, respectively [22]. Detecting such small capacitance variation relative to the sensor capacitance imposes several design challenges for the readout circuit. First the weak signal in the order of a few micro-volts needs an amplifier circuit with a gain of above 90 dB with good linearity.

Next, in both types of transduction principle, low frequency noise is found to be predominant; hence noise immunity technique that significantly improves the signal recovery must be incorporated in the electronic front end. Further the high gain amplifier itself will provide a greater amount of $1/f$ noise; hence amplifier with noise reduction technique is important. Chopper stabilization (CHS) technique that uses high frequency modulation is preferred due to its excellent $1/f$ and thermal noise reduction capability [20]. However, the output signal of the sensor readout front end is greatly affected by the chopper residuals; hence the low power filtering technique that has a steep roll-off is necessary to remove the modulation signal [21]. Thirdly, to improve the driving capability design of low impedance output stage is imperative.

2.5 A brief literature review

Detailed literature reviews of various journals with a primary focus on MEMS pressure sensor were conducted. General review of published research work in journals such as Journal of Micro-electro-mechanical Systems (JMEMS), Journal of Micromechanics and Micro-engineering, Journal of Microelectronics Engineering, revealed that nearly 2000 articles were published on this multidisciplinary & compelling device. Capacitive transduction techniques were preferred due to its improved performances over the piezoresistive technique in bio-medical applications. Furthermore, journals specifically on micro-system technologies such as Sensors, Actuators, Systems Integration, Journal of Smart Materials and Structures, Sensors and Actuators A (Physical), Sensors and Actuators B (Chemical), Sensors and Actuators C (Material) were also reviewed and found that most of the research interest were focused on performance improvement of diaphragm type capacitive pressure sensors for bio-medical related application. Few works on piezoresistive techniques were also reported for applications where performances such as temperature drift, low reliability and moderate sensitivity are not a concern. Further, research progress for on-chip sensor readout to achieve fast response and high sensitivity of the micro-sensor system was also explored. Design methodologies of the CMOS amplifiers, filters and buffers for improved signal conditioning capability were investigated. Despite these journals, an exploration on conference publications and white papers also proves the demand and a desperate need for research in improving the performance of the biomedical pressure measurement sensor micro-system.

The MEMS pressure sensor can be grouped into four basic types according to their sensing element as piezoresistive, capacitive, optical, and resonant. As stated earlier, the two major sensing techniques that are widely implemented in recent years are capacitive and piezoresistive pressure sensors. Former is preferred in biomedical applications for its higher order of stability. There are several advantages that make this transduction principle more attractive for health

care applications; a detailed discussion is given in the next Chapter. As this pressure micro-sensor design focuses on biomedical pressure measurement applications, the literature review is confined to only capacitive pick-off technique. The most capacitive sensing element is modeled as a diaphragm based sensor, pressure is determined by the deflection of diaphragms due to the applied force per unit area. Fig. 2.2 illustrates a schematic cross section of a typical pressure sensor diaphragm. The reference pressure can be a sealed vacuum chamber, so that absolute type pressure measurement can be performed [14].

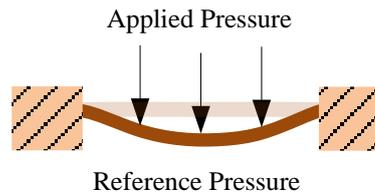


Fig. 2.2: Diaphragm Pressure Sensor

2.5.1 MEMS capacitive pressure sensor

In 1977, first capacitive pressure sensor was developed and demonstrated by Stanford, since then over the past 30 years, capacitive pressure sensors have been designed for a wide range of applications. In 1980, the micro capacitive pressure sensor was first fabricated by using the basic and versatile bulk micro machining technology [22]. The length of 3 millimeter, a height of 425 μm , and a construction of a chamber was the pattern of the sensor. Pressure deforming the thin upper stratum of the chamber changes the capacitance. The measuring range of the sensor was 0-300 mm Hg and was designed mainly for biomedical applications. Although a careful review on micro capacitive pressure sensors shows that many works was in progress from 1980 to 1992, Habibi et al., in 1995 [23], proposed a completely novel design in which capacitive type pressure sensor was developed on a glass substrate. Surface micromachining technology was first employed in fabricating the device. Array of micro pressure sensors was arranged on the glass substrate and the dynamic range was found to be 0-800 kPa. Babbitt et al., proposed another surface micro-machined capacitive sensor in 1997, for measuring pressures in the embryonic chicken heart; however, failed to achieve the required performance [24]. Nine years later in 2004, Casey et al. [25], proposed a minimally intrusive capacitive pressure sensor for biomedical application with a measuring range of 0-300 mm Hg. Eventhough the aspect ratio of the structure was high with five layers, sensitivity was satisfactory. Although, the performances of all these devices were optimum for biomedical applications, parasitic effects due to off-chip readout circuitry significantly affected the overall performances. Furthermore, as these devices are bulky it found only less implementation in biomedical applications.

Implementations of the capacitive transduction principle in applications other than medical field were also reviewed. The performance improvement techniques employed in other applications were explored for effective adaptation for biomedical pressure measurement applications. Capacitive measurement of pressure is mainly preferred for measuring absolute and differential pressures because of their capability of high pressure sensitivity, low temperature sensitivity, good DC response, low power consumption and simple structure [26]; hence the reason it has been used in many applications for sensing the pressure. However, capacitance change due to pressure is quite non-linear [26]. A bossed diaphragm is used later to overcome the non linearity [19], [21]-[23]. Sometimes the non linearity is reduced by using a contact mode (touching electrodes) [23]. Stray capacitance [24] and complex signal processing circuitry are still imposing a great deal of challenges in the design of capacitive sensors [25]. Also capacitors are easily affected by harsh environment which can vary the capacitance substantially, hence protection against this environment is critical [24]-[27].

Various commercial capacitive MEMS pressure sensors are available in the market with different performance specifications, designed using varied mechanical structures, materials, packages and fabrication technologies. Because of these varieties, the proper choice of MEMS capacitive pressure sensor for bio-medical sensing requirement is necessary. Once a type of MEMS pressure sensor is chosen, characterization is usually carried out, so that the functionality of this chosen device can be evaluated.

2.5.1.1 Dynamic range improvement

In 2002 Albert et al., proposed a capacitive device which is novel in terms of the structure geometry. A flexible method to deform the membrane under pressure was also suggested. Sensor was developed with the requisite performance for rigorous pressure sensing and flow sensing applications. As a consequence, this design enabled the development of a finished pressure transducer, with a wide dynamic range and accuracy that is roughly constant over the full operating range of the device. This sensor was primarily designed for the measurement of differential pressure with P_{ref} as the reference pressure; however, the sensor does not provide acceptable linearity over the wide dynamic range.

A novel liquid-crystal polymer (LCP) based capacitive pressure sensors fabricated using printed-circuit-processing techniques, was developed in 2006 by Jithendra, et al. LCP is a thermoplastic material with unique structural and physical properties. The advantages of LCP include low cost, versatility of fabrication (such as low temperature thermal bonding, and mechanical flexibility) and less moisture absorption, compared to other polymer films used in MEMS processes. The analysis of this sensor design showed a 0.15 V voltage change for an applied pressure of 0-100 kPa. For an applied pressure of 0-100 kPa the relative capacitance

change of the sensor was found to be 0.277 pF. The observed sensitivity was around 1.39 mV/kPa, which is promisingly better than the sensitivity of Kapton polyimide film based pressure sensor reported in [28]. However, this work proves to be complex in terms of fabrication and can be significantly affected by process variations. The sensitivity was also low at low pressure ranges; hence it is unsuitable for low pressure range applications.

2.5.1.2 Contact and touch mode capacitive pressure sensor

A capacitive sensor is sometimes designed to work in contact mode to increase linearity. In contact mode, the capacitance is nearly proportional to the contact area, which in turn exhibits good linearity with respect to applied pressure [31], [32]. The change of capacitance is mainly determined by the touched area, and is proportional to the applied pressure. This holds true over a range of pressures. However, this linearity comes at the cost of decreased sensitivity. The principal advantages of capacitive pressure sensors over piezoresistive pressure sensors are the increased pressure sensitivity and decreased temperature sensitivity [22], [30]-[32]. However, excessive signal loss from parasitic capacitance is a serious disadvantage. This has hindered the wide-spread use of these miniaturized capacitive sensors for various applications, but the disadvantage was later compensated by integrating an on-chip sensing circuit [26]. Shuwen et al., presented a prototype of a touch mode capacitive pressure sensor integrated with CMOS interface circuits to detect such small capacitance and to avoid parasitic effect. The proposed sensor structure was circular membrane made of polysilicon material. The outcomes of the research were good and from then on circular diaphragm where the preferred structure for fabricating capacitive pressure sensing element. The frequency and voltage output sensitivities are between 5.0-25.0 Hz/psi, and 10-50 MV/psi respectively in the linear pressure range of 8–60 pounds per square inch [32]. The integrated chip has a total noise of 39 mV in the frequency range of 0.03 Hz–10 kHz. The long-term stability was found to be 0.06% F.S. per week. The power consumption of the total system is less than 5 mW; however the design suffers from high hysteresis.

2.5.1.3 Enhancement of sensitivity and linearity

Very recently, Hezarjaribi et al., proposed a capacitive pressure sensor using silicon carbide as the material of choice for the diaphragm. Silicon Carbide is well suited for harsh environments, owing excellent electrical stability, mechanical robustness and chemical inertness properties [3]. In addition to the above excellent properties, the other key properties that made it attractive towards the use in sensors are low turn-on temperature drift, high sensitivity, and minimum dependence on side stress. The model has the advantage of good linearity which has

the potential to use in wireless handheld equipments. Further, it has also shown exact contact deformation; however, sensitivity is compromised and has higher order of hysteresis.

Parasitic capacitance is an inherent problem in the miniaturized capacitive devices. Pedersen et al., in his work suggested an on-chip CMOS ASIC for signal conditioning; thereby avoiding wire bonds that otherwise will induce parasitic capacitances [21], [33]. Another solution is to create a larger capacitive signal by fabricating an array of parallel coupled sensing elements, such that the total capacitance is the sum of all the individual elements, thus making the parasitic capacitance negligible compared to the signal capacitance. The research proposed combination of these two means; this led to a new design of a capacitive pressure sensor. The fabrication relies on fusion bonding two Si wafers together to create a vacuum cavity. Due to the membrane structure it offers a high capacitance signal and a low parasitic capacitance, which is important for achieving a high sensitivity. At a pressure above 2 bar, the sensor operates in touch mode and has an average sensitivity of 76 pF/bar (for the pressure variation from 2 to 6 bar). Furthermore, an AC bridge electronics circuit is also developed in the research that could be implemented for signal conditioning. The circuit has literally enhanced the overall sensitivity and the achieved peak sensitivity was found to be 8 mV/mbar. The stiffness, i.e. the flexural rigidity module, of the membrane was evaluated by fitting an analytic model to the measured response. The calculated stiffness and the behavior of the sensor in normal mode operation are in excellent agreement with theoretical values. The design failed to minimize the hysteresis but still suggested means to minimize the effect. It is proven that a DC bias of 4 V significantly reduces the hysteresis and a bias of 9 V nearly eliminates it, which is not preferable for low power applications. One advantage of this design is, as the exposed surface of the sensor is completely flat corrosion resistant thin films can be deposited for direct exposure to aggressive media. Thus a flat surface pressure sensor with the choice of bio-compatible thin-film coating could be adapted for biomedical applications.

In order to enhance the sensitivity and linearity of the pressure sensor, Zhou et al., proposed a structure which combines the area and distance change of the electrodes [19]. Diaphragms with high aspect ratio of area to thickness have been used to achieve ultrasensitive absolute capacitive pressure sensors [26]. Besides the principles based on electrode deformations of the sensor, a solid-state capacitor incorporating an elastic dielectric between the conductors have been in introduction for pressure, stress, strain and tactile sensing [22]. In this work, a novel pressure sensor employing a sandwich structure as dielectric layer between the two electrodes was realized, in order to overcome the post-processing difficulties. Two to three times' larger sensitivity enhancement was achieved with this structure; the explanation for this high sensitivity was due to the electrostriction effect of the elastic dielectrics. Hysteresis and the

parasitic effect of the capacitive sensor are not satisfactory for adapting in biomedical applications.

Capacitive sensors are an inevitable choice for biomedical application due to the availability of bio-compatible materials [24], [34]-[36]. Author Chiang et al., suggested a structure of capacitive pressure sensor consisting of two parallel electrical sensing plates, one dielectric layer sandwiched between the two sensing plates, and two outer insulating layers. This structure was mainly concentrated for biomedical applications in terms of the material used, but may suffer some disadvantages like fabrication complexity, dynamic range and linearity issues. Polyimide (PI, Durimide 7320) was chosen as the material of the insulating layers because of its bio-compatibility and insulating capability. The polydimethylsiloxane (PDMS, Sylgard 184) serves as the material of the dielectric layer. The Young's modulus of PI and PDMS is 2.5 GPa and 750 kPa, respectively [24]. The dielectric constant of 2.65 in PDMS is greater than the dielectric constant of air; hence a larger initial capacitance and higher capacitance change could be obtained according to the capacitance equation between two parallel plates.

The intrinsic stress levels in materials are generally very difficult to control and in most cases require compensation in the design or even sometime a compromise in terms of sensitivity is also done [3]. The stress problem has been addressed in [27], by using a sandwich structure for diaphragms. The diaphragm had layers that combine compressive and tensile stress. If the diaphragm is has more than one material, it may induce a stress gradient by mismatch of thermal expansion among different materials. Any intrinsic stress gradient in the diaphragm material will cause the diaphragm to bend, leading to a change of the air gap in the device, and thereof the sensitivity and cutoff frequency. Ganji et al., presented a technique to overcome the disadvantages of the earlier work. For the MEMS capacitive microphone realization, aluminum was the choice of material for the diaphragm with complex fabrication process steps to form array of perforations. This perforated aluminum diaphragm provided comparatively less intrinsic stress to some extent than the other design [37]. Aluminum material as the diaphragm or perforated diaphragm design could be easily adapted for biomedical applications to achieve increased sensitivity and better linearity [38], [39].

2.5.2 Readout circuit review

The CMOS circuit must amplify a very low-level signal from the pressure sensor using a high gain operational amplifier; the amplified signal will be proportional to the sensor output signal [34]. The sensor voltage usually lies within the range from 1 μV to 100 μV , proper design of opamp with a gain of around 100 dB is necessary to increase it to milli-volt range. A subsequent low pass filter will perform removal of high frequency noise due to transducer [40] and amplifier stages. The readout signal is generally an input to the Analog to Digital converter;

hence the readout circuit's output impedance must be low to drive the output stage. As a last stage, a buffer with low output impedance that has the capability to drive an output load of at least 4 μf must be designed. A detailed exploration of the literatures, carried out from the past work and study in the area of operational amplifier, low pass filter and buffers are reported below.

Operational amplifiers was originally designed and developed to perform certain mathematical operations in the early 1940 [20]. They were widely employed in addition, subtraction, multiplication, etc. Nowadays opamps are among the most widely used electronic devices, being used in a vast array of consumer, industrial, and scientific devices [41]. They have become a very commonly used electronic circuit since their availability on Integrated Circuits (ICs) from 1960s. Owing to their features such as very high gain, high input impedance, low output impedance, wider bandwidth, high CMRR and low noise, gave them the credibility of being the building blocks for a wide range of electronic circuits and applications [20].

Operational amplifiers have become the critical part of analog and mixed signal systems. Depending upon the specific requirements of applications, the circuit complexity of opamps varies, they are designed to realize functions ranging from DC bias generation to high speed amplification or filtering. The challenge in designing opamp continues to elevate as the incorporating system gets miniaturized. For the past decade, they are extensively employed in sensor readout applications due to their high gain and low power dissipation [42]-[44]. Furthermore, the possibilities of low supply voltage design provided by the advanced CMOS technology has significantly increased the battery life in handheld and implantable biomedical pressure measurement equipments. This demand could be met by scaling down the transistor channel lengths in the recent IC technologies. The key parameters that are to be considered for designing the opamp are [20]:

- Open loop and closed loop gain
- Small signal bandwidth
- Output Swing
- Linearity
- Power dissipation
- Noise and Offset
- Supply Rejection
- CM range

To accomplish all these characteristics in any design of opamp is extremely hard, thus based on the required parameters the topology design is usually performed. At least two cascaded stages

are essential to closely achieve good performance of opamp. Lu et al., proposed a single stage opamp in the late 1998, the design had a novel regulated-cascode transistors. These regulated transistors have a lower output compliance voltage, making it possible to further reduce the supply voltage and to design single-stage opamps. The opamp consisted of a complementary input differential amplifier and a trans-impedance building block as an active load. Parallel connection of one n-channel differential pair and a p-channel differential pair enabled full rail-to-rail operation. One advantage of a single-stage opamp is that it normally requires no frequency compensation to ensure good stability, thereby preserving its frequency performance [41], however the gain of this design was very low, the slew rate was poor and the power dissipation was also high. Moreover, speed and output swing is very low, hence these performances of a single stage amplifier made it unsuitable for critical sensing applications. Furthermore, mirror pole in the single ended circuit creates stability issues.

2.5.2.1 Opamp basic topologies

The analysis of a simple two stage opamp design [20] with all the transistors in the output stage placed in the saturation regime, shows that it has a large differential output swing; however, it offers drawback such as high power consumption and poor negative power-supply rejection. Its non-dominant pole, arising from its output node is determined by an explicit load capacitance, it typically occurs at a relatively low frequency. As a result, this amplifier has a compromised frequency response [45]. Hence it is evident that this topology is not adequate for sensor readout application.

A telescopic topology design of the opamp proposed by Gulati et al., consumes less power than other topologies; however, has a major disadvantage of severely limited output swing. The reason for this is that the tail transistor directly cuts into the output swing from both sides of the output. Hence in most cases it is clear that the output swing reduces by 45% [46]. At large supply voltages, the telescopic architecture becomes the excellent choice for applications requiring moderate gain. The output swing could be increased by 600 mV in by removing the tail current source [46], but the common-mode rejection and power-supply rejection of such a circuit is greatly compromised. Moreover, the circuit performance such as unity-gain bandwidth and settling time are significantly affected by the input common-mode and supply voltage variation, which is not a desirable characteristic of any opamp in sensor readout applications. To overcome these issues Gulati et al., presented a design that combines the low power and high speed advantage of the telescopic architecture with the high swing capability of the folded cascode. Eventhough the design provided a large swing and good slew rate, the power dissipation was higher than the conventional folded cascode amplifier. The design also had a less linear range of operation therefore provides only a moderate bandwidth.

2.5.2.2 Folded cascode topology

In folded cascode operational amplifier (FC opamp) to achieve high DC gain cascode configurations are employed. Many analog circuit designs use folded cascode, because of its large output swing [47]-[51]. The reason for the good output swing is due to the fact that the cascode configuration is not used in the input stage unlike telescopic design. The cascode configurations could be used in any other stage for improved gain of the CMOS transistor amplifier. In folded cascode amplifier the stage gain can also be increased so as to increase the overall gain. Moreover, the choice of the input common mode level is easier, hence only the bias voltage of PMOS and NMOS must alone be designed properly, which is more advantageous than telescopic. A conventional single ended output folded cascode opamp is usually designed with PMOS input transistors, in contrast NMOS also can also be a choice of the input stage but the former allows shorting the input and output terminal with negligible swing limitations. The major drawbacks that pose design challenges of this incredible topology is its low settling time and noise, therefore certain applications which requires high gain, large swing and high speed, faces tremendous hindrance in employing this topology. There are various design methodologies proposed by many researchers to improve the speed and noise of folded cascode opamp. It was also noticed from the literature survey that continuous studies were in progress since late 1980 for performance improvement of FC opamp.

Ribner et al., first analyzed the conventional folded cascode opamp in 1984. The purpose of this work was to establish the high PSRR and wide common mode input range. The clear depiction of the PMOS input stage over NMOS input stage was given in the literature. Yang et al., made a second order analysis of a new version one-stage folded cascode opamp. The objective of the study was to overcome the settling time issue which is dominant in folded cascode opamp. The obtained settling time response of this two-pole system for a step input was found to be under-damped, so that the first peak just touches the upper error bound [47]. The two pole model was accurate up to the unity-gain frequency. Although, the phase responses of the model and the opamp disagree slightly at the unity-gain frequency due to the inexact pole-zero cancellation, they are still in fairly good agreement and can be used to design the MST response for the opamp. Also by providing a well-defined pole separation, the MST response is improved in this design. Folded cascode opamp was designed with a load capacitance of 5 pF and $D = 0.01$ (desired error bound). A wider bandwidth is realized when the load capacitance was 4.5 pF, furthermore, an over-damped yet narrower bandwidth response at 5.5 pF was observed. Interestingly, longer settling time was observed when load capacitance is either larger or smaller than 5 pF, eventhough the unity-gain bandwidth increases for smaller load capacitance values. Despite the above improved performance, obtained poor gain and lack of stability criterion makes this design unsuitable for sensor readout application.

Another important aspect that needs to be considered in improving the performance of folded cascode opamp is the noise and input referred DC offset. The two noise sources in CMOS operational amplifier are flicker noise and thermal noise components. A key requirement of a sensor readout circuit is the low noise and low power consumption amplifier. Although the CMOS technology offers such tremendous advantage, $1/f$ noise pose hindrances for its full fledged use as it limits the minimum detectable signal in amplifier at low frequency. In folded cascode topology the noise factor is usually high compared to telescopic topology. Generally, for the designed bias conditions and device geometries in folded cascode opamp, flicker noise component is higher than the thermal noise component, especially, for frequencies below 1–10 kHz [48].

Chan et al., proposed a mathematical analysis for achieving minimum input referred noise. In his literature, he proved through HSPICE simulation that the minimum noise point occurs when the input folded transistor pair length were $3.1\ \mu\text{m}$ and $20\ \mu\text{m}$, with bias current ratios of the folded pairs being 1.6 and 0.6 respectively [49]. However, the gain and noise minimization technique of this design is inadequate for sensor readout application, where a very low signal has to be detected; hence an optimum solution must be found.

Chopping technique is the only possible option for input referred noise reduction in low signal detection CMOS operational amplifiers [52]. It is a modulation technique that can be employed to reduce the effects of opamp imperfections including noise and input referred DC offset voltage [53], [54]. The input signal is first modulated by the chopping signals $m(t)$ and $m'(t)$ (both signals are in the same frequency with phase shifted and are rectangular pulse) with f_{chopper} as the chopping frequency. The output of the modulator is shifted to odd harmonics by these high frequency chopping signals. Amplification is performed to this harmonic shifted sensor signal by the opamp, the modulated input signal is then demodulated by the same chopping signals (phase shifted f_{chopper} frequency) and shifted back to the even harmonics. Whereas, the noise and DC offset originated from the amplifier is just modulated once and shifted to the odd harmonics at the output, thus isolating the $1/f$ noise.

The conventional chopper amplifier needs a higher cut-off frequency than f_{chopper} , hence has a disadvantage of large power consumption. Measures to reduce the power consumption and simplify the circuit of chopper amplifiers are essential. Yang et al., proposed a chopper amplifier very recently. It is a two stage amplifier in which the first stage is a folded cascode opamp and the second is a common source amplifier with miller compensation. The CS stage was designed to provide large output voltage swing [52]. Simulated results showed that the amplifier consumes $117\ \mu\text{W}$ of power at a supply voltage 1.8 V, and the equivalent input noise

was 39 nV/Hz @100Hz; however, the reduced output swing of 500 mV is less convincing for sensor readout conditioning.

Musa et al., in 2006 included gain boosting stages in the conventional folded cascode to achieve increased gain. The design included both N-boosting and P-boosting stages. It has the advantage of increased output resistance and gain due to the gain boosting devices without the need of additional cascaded devices. However, transient response from such an opamp was degraded by the presence of pole-zero doublet [50], hence compensation for this non dominant pole-zero is necessary. This doublet appears as a slow exponential term in the step response of the opamp, thus degrading the total settling time drastically [20]. The current of this gain boosting stage must be kept in such a way that the poles must split along the imaginary axis forming a complex conjugate pair, thus the effect of the slow settling component due to pole-zero doublet will be eliminated and the transient response will behave like a single pole response [55]. However, further increase in current will cause a sharp reduction in phase margin, making the system unstable. In addition, increase in current causes increase in power dissipation apart from added gain stages; hence an optimum value of current for the gain boosted stages will solve this tradeoff. The efficient way to solve this issue is by properly choosing the length of the gain booster transistors.

2.5.2.3 Low pass filter stage

The necessity to filter out the chopping frequency arises from the fact that the presence of this signal will affect the sensitivity. Chopping frequency is used to modulate the input signal of the folded cascode opamp to remove input referred noise and hence must be filtered out so that the signal will be beneficial for further processing. Filters with better roll-off and high Q-factor are critical in this application. Filters are generally classified under network synthesis design methodology as Butterworth, Chebyshev, Elliptic (Cauer), Bessel, Gaussian, Optimum "L" (Legendre) filter and Linkwitz-Riley filter [56], these filters are also exists as low pass filter. Each filter is classified by a transfer function that defines the gain of the circuit for all input frequencies. While each of these filters may be used under different circumstances, the elliptical filter is a filter with widespread application due to its sharp frequency cutoff and equiband ripples. In addition, it also exemplifies several characteristics seen in other types of filters, which makes it excellent for CMOS technology design.

Elliptic filters can also be used to realize monolithic filters such as AO-RC, MOSFET-C, switched-C, Gm-C and digital [56], [55]. Out of these filters the two most popular filters widely used in integrated circuits are Switched-C and Gm-C. Switched-C has a couple of disadvantages which makes it unsuitable for readout circuits. Firstly, it requires extra high frequency signals for the clock; also the supplied frequency gets in to the signal and can be detected in the output

causing sensitivity issues. It requires an additional filter to remove this disturbance. Secondly, the clock frequency can cause aliasing if the information signal is close to its frequency. Finally, it offers a limited dynamic range. Most of the applications, over the past decades prefer Gm-C filters because of its dynamic range and low power consumptions than Switched-C filters. Moreover, the simplicity in the design implementation of Gm-C elliptic filter makes it more attractive for higher order filter design [57].

Certain filter implementations consist of passive components to replace their active counterparts. Pandey et al., used a class AB CMFB to improve stability of the filter at high frequencies. The analysis result showed a power consumption of CMFB circuitry less than 50% of OTA's power. The filter was fabricated in the 0.35 μm Taiwan Semiconductor Manufacturing Company (TSMC) CMOS process technology through the MOSIS educational service. Cut-off frequency of 550 MHz was achieved along with a group delay variation of ± 1 ns in the entire bandwidth [57]. The filter's roll-off was poor and had more ripples in both stop and pass bands; hence improvement to increase roll-off and techniques to reduce ripples in the pass band must be deduced.

2.5.2.4 Buffer stage

As discussed earlier, the output of the sensor readout circuit has to drive ADC for the proper actuating purpose or for displaying the sensed information about the physical quantity. Let us take the case of displaying this sensed information to a LCD display. Firstly, to drive the LCD display driver circuit it is necessary that the output stage of the sensor circuit must provide very low impedance. Secondly, output buffers must be built using operational amplifiers to drive the highly capacitive column lines. Finally, it must have better overall performance that determines the speed, resolution, voltage swing and power dissipation of signal drivers [58]. The important characteristics that a buffer must possess other than low impedance is wide signal range, wide bandwidth, low power dissipation, and no DC level shift between input and output terminals [59]. Basic source followers are the best example for a simple buffer but are limited by nonzero offset and nonlinearity. In most designs the output buffer of the sensor readout circuit is usually implemented by a differential amplifier, which is connected as a unity-gain buffer.

A simple one stage buffer circuit has no level shift; moreover, negative feedback could be employed to reduce nonlinearity [58]. There are also other possible buffer circuits with one or two stage opamps, which are generally designed as a voltage follower. Furthermore, some designs employ cascading of differential pair and voltage follower for better performance [59]. Class AB and class B types of buffers are also designed and implemented in various applications, but the number of transistors used to realize the circuit was more hence the power consumption. In order to design a low power buffer with better performance and characteristics,

fully differential buffer preferably with self bias could be the best option for a sensor readout circuit [60].

Table 2.1: Target specifications of the design

| Parameters | Target Value |
|---|------------------------------|
| Gain of the opamp | > 95 dB |
| Unity gain bandwidth of opamp | > 100 MHz |
| Phase margin of the opamp | 70 ° |
| Input referred noise of the opamp | < 300 nV/ $\sqrt{\text{Hz}}$ |
| Required supply voltage | < 1.8 V |
| Signal swing of the readout circuit | > 500 mV |
| Low pass filter order | < 5 th order |
| Cut off Frequency of the Filter | 10 kHz |
| Buffer driving capability | < 20 pF |
| Total harmonic distortion (THD) | < 2 % |
| Sensitivity of pressure micro-sensor system | > 0. 007 mV/hPa |
| Non-Linearity | < 3 % |
| Dynamic range | 50 hPa to 1000 hPa |
| Minimum Detectable Pressure | < 10 hPa |

2.6 Conclusion

The literature review revealed that the sensor device parameters that needs improvement are sensitivity, dynamic range, linearity, hysteresis and repeatability. The parameters of the sensor readout circuit that have to be enhanced include gain, bandwidth, stability, linearity and output swing. Further, reduction in the overall noise floor will considerably improve the overall micro-sensor system performance. The sensitivity depends on the thickness and shape of the diaphragm; hence an appropriate geometrical design is necessary to achieve high sensitivity. Generally, the fabricated sensor will exhibit some amount of sensitivity deviation than the one built and analyzed in the CAD environment; however the CAD tool will help in arriving at a proper design of structure and the choice of material for achieving better sensitivity. The other key requirement of a biomedical micro-sensor system is its minimum detectable input parameter that can cause an output voltage change. Therefore analysis in CAD environment must be done to develop and optimize a suitable device structure to lower the minimum detectable pressure.

The targeted design specifications for the pressure micro-sensor system is provided in the Table 2.1. Based on the literature review and other reported findings, two capacitive type pressure micro-sensor systems are designed and analyzed for a range of bio-medical applications. Absolute pressure measurement that provides better flexibility of measuring low pressures as well as high reliability is preferred in this work. Separate comprehensive high performance sensor readout circuit stages for each micro-sensor, which are integrated on-chip are also designed. Following Chapters discuss the techniques and design aspects involved in designing the high performance integrated micro-sensor systems.

Chapter 3

SiGeMEMS Capacitive Pressure Sensor

3.1 Introduction

Integration of micro-structured sensing and actuating devices with signal conditioning circuit has been of significant research interest for the past few years. Improvement in the performance of the transducer system has greatly influenced the growth in the development of on-chip prototype sensors and actuators. However, their production and utilization is still in the budding stage. MEMS pressure sensor's market expansion due to its demand in assorted application has made it to be the second leading MEMS device in terms of revenue [6]. Micro-pressure sensors have been employed extensively in numerous fields such as biomedicine, automotives, industrial safety, aeronautics etc. for the past few decades. Capacitive and piezoresistive transduction are the two well known techniques of commercialized pressure sensor implementation [38]. Piezoresistive type pressure sensor has the advantage of requiring very small signal amplitude change with induced stress, for effective sensing capability. Moreover, due to its robustness, it is much preferred in harsh environmental applications such as automobiles and industries; however the resistive element being highly sensitive to temperature change, makes it unsuitable for many other applications.

Ease of fabrication steps and insensitivity to temperature variation as well as environmental effects have made the capacitive sensing principle preferable over the piezoresistive implementation. However, parasitic effects result in significant degradation of the capacitive sensing technique. This disadvantage of capacitive element can be substantially reduced with an on-chip readout and conditioning circuitry [61]. In this work, efforts have been taken to design a high performance on-chip sensor readout that overcomes such limitation for a variety of biomedical applications. Efforts taken previously for hybrid integration of sensor devices and associated conditioning circuitry in a single hermetic package were found to have less attraction from among the MEMS sensor market, as most of them yielded low overall sensing system performance due to the significant issues of nonlinearity, reliability and environmental degradation. Eventhough monolithic integration usually has a longer time to market compared to hybrid sensor systems; it offers lower overall production and packaging costs [7]. The surface micromachining technique of monolithic integration is preferred due to its immunity towards on-chip CMOS circuit process variation unlike substrate etching in bulk micromachining [62]. Monolithic modular integration, allows separate design and development of both MEMS and CMOS electronic process on a single chip. The three main

modular integration methods are pre-CMOS; interleaved CMOS-MEMS and post-CMOS approach [63]. In pre-CMOS, MEMS devices are processed first with complete release steps prior to the development of CMOS electronic; this technique can significantly alter the device element characteristic leading to poor sensor performance. Interleaved process involves the alternation of CMOS and MEMS process. The cost involved in this technique is high leading to poor yield. Moreover thermal budget is inadequate when alternating the CMOS and MEMS process. Post-CMOS process provides a decent approach to overcome the limitation posed by the other integration strategies. MEMS device, processed on top of the CMOS electronic circuit is a promising technique, which is very much desirable for applications requiring high performances. Figs. 3.1, 3.2, and 3.3 shows the three integration approaches, it can be noted that the thermal budget of CMOS process greatly affects the MEMS devices in pre-CMOS and interleaved process, thus a CMOS process that precedes the MEMS processing as in post-CMOS approach is preferable. The choice of material for the MEMS structures that has low process temperatures (such as aluminum and titanium) does not degrade the electronic circuits. This made post-CMOS process more attractive in recent years.

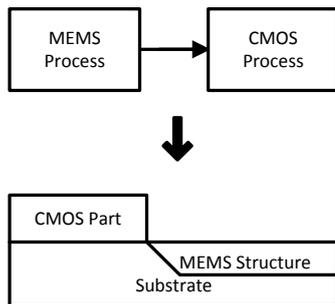


Fig. 3.1: pre-CMOS process

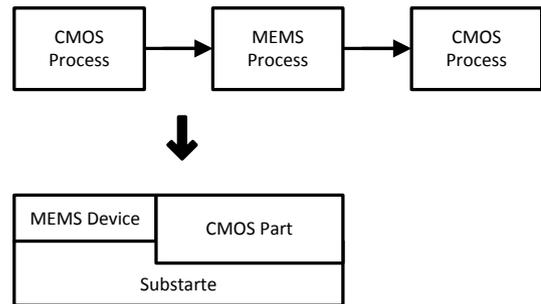


Fig. 3.2: Interleaved process

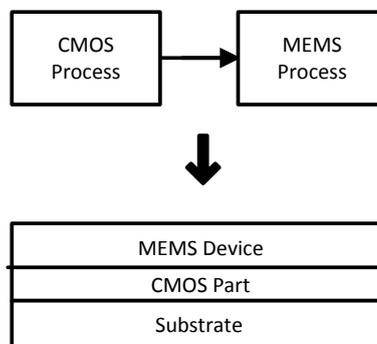


Fig. 3.3: post-CMOS process

3.2 Post-CMOS process

Many researches were under progress over the decade, to develop appropriate process technologies that can improve the performance of the planar integrated MEMS device with electronics in post-CMOS approach. IMEC's Silicon Germanium MEMS platform offers monolithic integration of CMOS and MEMS, where MEMS are processed on top of CMOS circuit. This includes complete deposition and patterning of the device using CMOS substrate as the starting wafer. Fixed baseline SiGeMEMS technology offered by IMEC through EUROPRACTICE allows both MEMS+CMOS process and MEMS only process. The latter supports SiGeMEMS process to be performed on the externally processed chip with choice of CMOS technologies; however, requires meeting the die size specification for the successful SiGeMEMS process outcome. Modular integration that combines both the high performance sub-micron CMOS technology and low process temperature polycrystalline Silicon Germanium (Poly-SiGe) MEMS technology provides high process reliability. Further, preservation of electronic readout circuit performance is a major concern in any post-CMOS process. The advantage of CMOS compatible low thermal budget processing makes this technology more dependable, as the risk of degradation of the CMOS circuit interconnects and vias are extremely low [64], [65], leading to excellent performance preservation. Cross section of the IMEC SiGeMEMS process is shown in the fig. 3.4. MEMS structures must conform to the absolute design limitation for withstanding the static load during processing. Some of the design limitations that need to be addressed are, size of free standing structures, maximum limit of releasing structure length from anchor to anchor, minimum number of anchors for the designed structure size and limitations of release hole at structure edges [66].

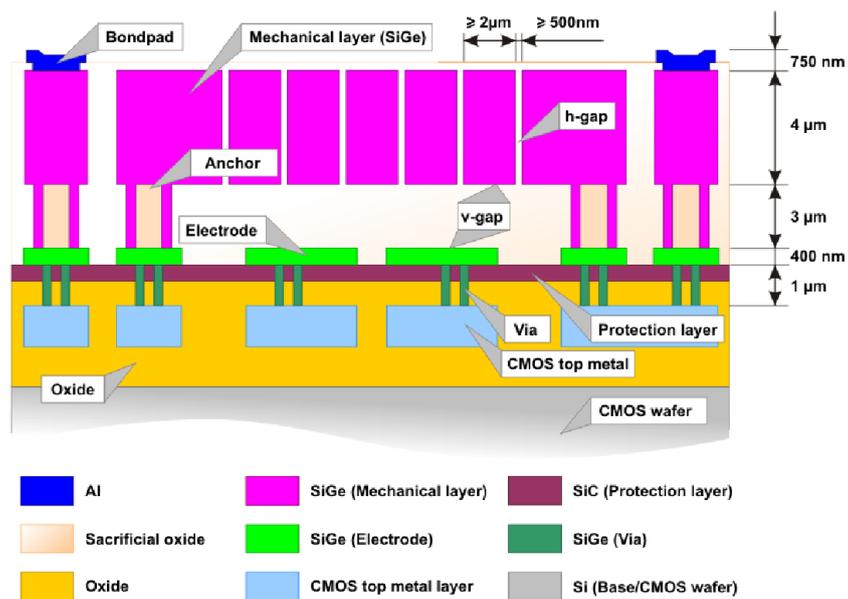


Fig. 3.4: Cross section of IMEC SiGeMEMS process [66]

Poly-SiGe being the structural material in this process makes it immensely suitable for sensor applications, as their density is an order of magnitude higher than the poly-silicon. The addition of 70% of germanium makes the intrinsic resistance of the MEMS structure low as the germanium's band gap is very small compared to poly-silicon [67], [68]. The low intrinsic resistivity structure when designed as a diaphragm for the capacitive type sensor can provide better sensitivity. Good electrical properties of poly-SiGe material offers low parasitic effects which are attractive for sensor applications, especially for capacitive sensor where parasitic effect is a major concern. Further, parasitic effects can also be substantially reduced as massive parallel interconnections are possible with this planar integration. Mechanical properties such as high strength, high Q factor, less creep and low fatigue of this material composition [66] are promising for obtaining increased linearity, stability and repeatability of the sensor. Moreover the increased etching rate at 90° C with the addition of germanium reduces processing time and increases yield [67].

3.3 Design process flow

The unique monolithic integration of SiGeMEMS sensor device on top of the CMOS (Complementary Metal Oxide Semiconductor) circuit (also forming the host substrate for the SiGeMEMS structure) in this CMOS integrated SiGeMEMS process has immensely miniaturized the proposed pressure sensor system. The low thermal variation of the material properties of polycrystalline-SiGe enables the post processing of the sensor devices on top of the CMOS circuit. Different diaphragm shapes and structures along with varied dimensions and thickness have been explored in the past decade for improving the overall system performance parameters such as sensitivity, linearity and dynamic range [7], [16], [38], [61]. Although reduced diaphragm thickness has yielded improved sensitivity, the trade-off has been poor linearity [61]. This proposed design has focused to overcome this sensitivity vs. linearity trade-off. The high performance CMOS readout electronic circuit which is designed and fabricated in TSMC 0.18 μm CMOS technology is left for discussion in Chapters 4 and 5. The design and analysis of the MEMS capacitive pressure sensor that is processed on top of the CMOS die is discussed in the following sections. The integration process flow is depicted in fig. 3.5.

The system block diagram of the proposed integrated sensor is shown in fig. 3.6. The weak and noisy sensor signal is amplified utilizing a modified low noise chopper-stabilized opamp (operational amplifier). The high frequency chopper residuals (artifacts) are filtered out by a steep roll-off Gm-C filter. The filter is followed by a self-biased buffer output stage, which can drive an off chip load of up to 15 pF. The design target of the proposed edge clamped perforated elliptic diaphragm structure is to achieve a wider dynamic range, without

compromising sensitivity and linearity. In order to achieve this performance, L-clamp type spring anchors that can provide better deflection (not reported before) is utilized.

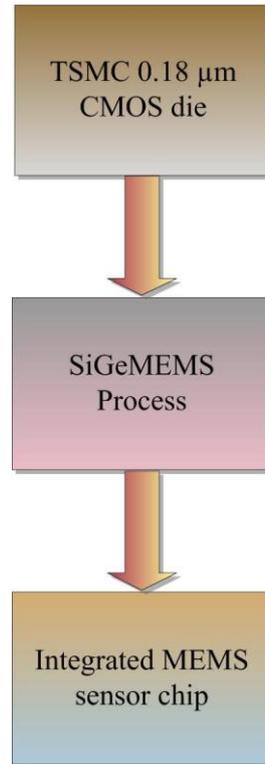


Fig. 3.5: Process flow of SiGeMEMS [66]

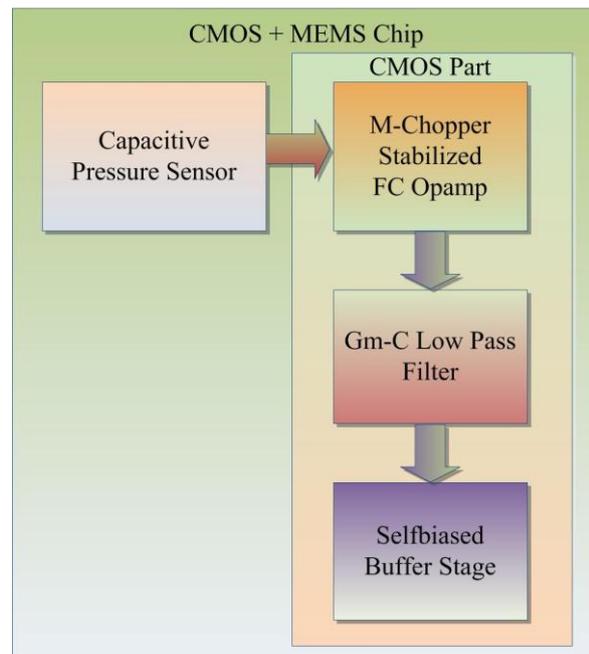


Fig. 3.6: System block diagram of the integrated MEMS capacitive pressure sensor with CMOS readout

The following sections are organized as follows: In section 3.4, characterization of the structural and fabrication aspects of the micro-sensor is described, in section 3.5, model analysis and the performance of integrated system characteristics are provided, while in Section 3.6, post process sealing technique for practical realization of the MEMS capacitive device is detailed. Finally, concluding remarks are presented in section 3.7.

3.4 Design and model characterization of sensor device

The capacitive sensing technique which is an inherently low noise transduction mechanism is also a relatively simple method. It uses either a variable displacement or a varying parallel-plate surface-area principle to pick up (sense) the desired physical quantity. Although this technique is less resilient to harsh environment compared to its piezoresistive counterpart; proper structural design can, in comparison, contribute to a relatively lower hysteresis and greater stability as the distinct advantages of this technique.

3.4.1 Theory

The principle of capacitive sensing technique is comparatively simpler and so do its physical structural arrangements. Initially, this technique was extensively employed only for precise measurement of object movement; however the high sensing capability together with inherent non-linearity and temperature cross-sensitivity has earned its reputation in other sensor application. The capacitive sensing technique constitutes of one fixed plate and one or more moving plates, distance between the plates varies when the physical quantity is in contact with the moving plate leading to variation in capacitance. The obtained variation in capacitance, is then processed by the readout circuit to measure the physical quantity. Integration of the readout circuit with these capacitance plates on a single die will cater for the development of a high sensitive sensing system [2]. MEMS+CMOS integration can reduce the hysteresis and improve repeatability and long term stability, further, production cost is substantially reduced.

Normal and touch mode are the two widely employed types of capacitive sensing methodology. The latter is employed to overcome the limitation of membrane risk failure; however it suffers from long processing issue as an additional depositing insulation layer on top of the bottom electrode is required. Moreover dynamic range is limited due to the limitations of diaphragm structural dimension and touch mode operation [28]. Analytical modeling of touch mode sensor is also difficult. On the other hand, the normal mode capacitive sensor can be easily described analytically and their parameters such as zero pressure capacitance and sensitivity can be precisely calculated. Deflection effects of the corresponding structural geometry can also be evaluated for the desired membrane dimensions using the

simple small deflection model; hence capacitive sensor with the normal mode of operation that has a wide dynamic range is preferred in this work. As the capacitive element usually has larger in-plane dimensions compared to its thickness, the appropriate plate theory that can be applied for further optimization of geometry and dimensions to achieve the desired performance is the thin plate theory. Thin plate analysis under a small deflection regime considers that the maximum deflection for the specific pressure range is half the thickness of the membrane. The three dimensional plate problem in this regime is greatly reduced to two dimensions by the Love-Kirchhoff's hypothesis. The assumptions can be given as [69]:

- Small deflection in the middle plane of the plate compared to its thickness.
- No significant strain occurs in the middle plane of the plate with the applied load.
- Shear forces can be considered as negligible.
- Negligible normal stress in the transverse direction of the plate compared to the other two stress components.

Hence normal and shear stresses in z direction (transverse) are assumed to be zero and only normal stresses σ_{xx} , σ_{yy} and shear stress τ_{xy} due to x and y directions are considered. Thus the plane stress condition for the analysis of the diaphragm deflection is applied in this work. Under the influence of the applied pressure normal to the diaphragm surface in y direction of the two plane Cartesian co-ordinate, the edge clamped plate experiences strain due to the induced stress. The induced stress can be measured in terms of bending moment that causes deflection of the diaphragm. Considering the material of the plate being linear elastic, strain the measure of deformation can be expressed in terms of deflection as [69]:

$$\varepsilon_{xx} = -z \left(\frac{\partial^2 w}{\partial x^2} \right) \quad (3.1)$$

$$\varepsilon_{yy} = -z \left(\frac{\partial^2 w}{\partial y^2} \right) \quad (3.2)$$

$$\varepsilon_{xy} = -2z \left(\frac{\partial^2 w}{\partial x \partial y} \right) \quad (3.3)$$

where ε_{xx} , ε_{yy} are normal strain, ε_{xy} is shear strain and w is the deflection of the plate in

respective directions (x or y). From the above equations it is evident that the variation of strain in x and y direction is uniform throughout the plates, the Hooke's law also holds for strain measurement and is zero in mid-plane of the plate's top and bottom surface. Normal stresses due to the applied pressure can be found from the normal strain as below [69]:

$$\sigma_{xx} = \frac{E}{(1-\nu^2)} (\varepsilon_{xx} + \nu\varepsilon_{yy}) = -\frac{Ez}{(1-\nu^2)} \left(\frac{\partial^2 w}{\partial x^2} + \nu \frac{\partial^2 w}{\partial y^2} \right) \quad (3.4)$$

$$\sigma_{yy} = \frac{E}{(1-\nu^2)} (\varepsilon_{yy} + \nu\varepsilon_{xx}) = -\frac{Ez}{(1-\nu^2)} \left(\frac{\partial^2 w}{\partial y^2} + \nu \frac{\partial^2 w}{\partial x^2} \right) \quad (3.5)$$

Shear stress can be given as:

$$\tau_{xy} = \frac{E}{2(1+\nu)} (\varepsilon_{xy}) = -\frac{Ez}{2(1+\nu)} \left(\frac{\partial^2 w}{\partial x \partial y} \right) \quad (3.6)$$

where ν is Poisson's ratio of the plate material, z the vertical distance from the center of the plate and E the young's modulus. The bending moments that expresses the resultant forces can be given in terms of stress; however stress and strain can be evaluated by first determining the equation that governs the deflection of the plate. The differential equation that is widely used for plate deflection calculation is [69]:

$$\frac{P}{D} = \left(\frac{\partial^4 w}{\partial x^4} + \frac{\partial^4 w}{\partial y^4} + 2 \frac{\partial^4 w}{\partial x^2 \partial y^2} \right) \quad (3.7)$$

where P is the applied pressure, D the flexural rigidity and w the deflection of the plate. The solution of the above equation gives the maximum deflection at the center of the plate. The bending and shear moments that causes deflection of the element, mainly depends on the properties (flexural rigidity) of the plate material. For this homogenous isotropic plate, the moments for the two dimensional analysis can be found by solving the basic elastic curvature equation of a thin plate; however the above equations (3.4), (3.5) and (3.6) expresses stresses in terms of deflection; hence it would be a straightforward method to derive the bending moments from stresses. The bending moments can be given as [69]:

$$M_x = -D \left(\frac{\partial^2 w}{\partial x^2} + \nu \frac{\partial^2 w}{\partial y^2} \right) \quad (3.8)$$

$$M_y = -D \left(\frac{\partial^2 w}{\partial y^2} + \nu \frac{\partial^2 w}{\partial x^2} \right) \quad (3.9)$$

The shear moment can be given as:

$$M_{xy} = -D(1-\nu) \left(\frac{\partial^2 w}{\partial x \partial y} \right) \quad (3.10)$$

where D is the flexural rigidity of the plate. It can be evident from the above equations that the bending moments of the plate depends on its flexural rigidity by way of stress and strain relationship, apart from the influence of its material properties. For the all-side clamped diaphragm, the shear moment is negligible at the edges, thus the transverse force is equal to the reaction force (no Ersatz's force) [69] it can be expressed as:

$$\frac{\partial w}{\partial x} = 0 \quad (3.11)$$

$$\frac{\partial^2 w}{\partial x \partial y} = 0 \quad (3.12)$$

It is evident from equation (3.8), (3.9) and (3.10) that greater the thickness of the plate, lesser the flexural rigidity and in turn the bending moment is reduced. Thus the increased pressure load for comparatively thicker diaphragm deforms less. Increasing thickness of the diaphragm can still satisfy the thin plate assumption if the diaphragms dimensions are larger than its thickness. These diaphragms will deflect to half of its thickness under increased pressure load as compared to the usual diaphragm design, thus complying with the Love-Kirchhoff's hypothesis. The dynamic range is also increased by extending the deflection limit, with significant increase in the linearity of the device.

Mostly, the sensor element or the moving plate of the capacitive sensor is designed as square or rectangular geometries. This is due to the fact that the mask design and preparation is straightforward as both have sharp edges. Moreover these geometries will comply with the foundry design rule check and also the risk of the unsuccessful release of the membrane is less.

The displacement or deflection analysis of the structure geometry is extremely complicated with mere manual mathematical workout; hence software tools that perform numerical analysis such as finite element method or finite differential method are generally preferred. More accurate results can be achieved using the high end technique for optimization of geometry that will provide the desired performance for a particular application. The analysis reported in [70] shows, larger induced stress that can lead to better sensitivities is possible with the square and rectangular geometries by keeping the side lengths smaller. However their dynamic ranges become limited as they begin to deflect for higher pressure ranges. Moreover larger stress at the centers of edges makes them unreliable, as the failure rate of the sensor is higher at lower pressures. This makes them unsuitable for wider dynamic range pressure sensor applications. The normal stresses at the center of edges for a square geometry, with the side length of a and thickness of h can be given as [69]:

$$\sigma_{sxx} = 1.23p \frac{a^2}{h^2} \quad (3.13)$$

$$\sigma_{syy} = \nu \left(1.23p \frac{a^2}{h^2} \right) \quad (3.14)$$

The normal stresses at the centre of edges for rectangular geometry whose length and breadth are $2a$ and $2b$ respectively with thickness h is given as [69]:

$$\sigma_{rxx} = 2p \frac{a^2}{h^2} \frac{b^4}{a^4 + b^4} \quad (3.15)$$

$$\sigma_{ryy} = \nu \left(2p \frac{a^2}{h^2} \frac{b^4}{a^4 + b^4} \right) \quad (3.16)$$

Circular type diaphragm is the other alternative geometry that overcomes these limitations. The center deflection in this is more than the other geometries, this leads to improved sensitivity [71]. Moreover comparatively lesser edge stresses than the other two geometries for the same applied pressure makes it more reliable. The normal stresses at the edges of the circular plate of radius a can be given as:

$$\sigma_{Cxx} = 0.75p \frac{a^2}{h^2} \quad (3.17)$$

$$\sigma_{Cyy} = \nu \left(0.75p \frac{a^2}{h^2} \right) \quad (3.18)$$

Increased stiffness is also noticed in the circular element when compared to square and rectangular diaphragms for the same dimensions. In addition, it can also provide a better dynamic range. Even-though the above performances are promising for most sensor applications, critical parameters such as linearity, hysteresis and repeatability demanded by the large dynamic range pressure sensing application is less convincing. Hence proper choice and design of sensor geometry is necessary for achieving optimum performance. Elliptic geometry which can be formed by stretching a circular diaphragm, can grant the required high performance for precise pressure sensing application. It can be demonstrated that this structure can be arrived by removing the sharp edges of the rectangular diaphragms; hence could provide the combined performance of a rectangular diaphragm and a circular element. Such a type of an element, which can provide better sensitivities as well as improved linearity with low hysteresis, is designed in this work.

3.4.2 Design of perforated elliptic diaphragm

The elliptic structured diaphragm of the capacitive pressure sensor is designed with increased major axis (r_2) and decreased minor axis (r_1) for achieving the combined performance of circular and rectangular geometries as discussed earlier. Further, two techniques were employed for significant improvement of the device performances. Firstly, numerous square planar perforations throughout the membrane in order to achieve higher linearity are employed. The residual stress in the usual diaphragm element significantly affects the sensitivity and linearity of the device after release. Increased residual stress due to the diaphragm material in certain cases renders bending of the membrane or even breakage leading to an unsuccessful process outcome. Multiple perforations in the element can significantly reduce the risk of failure and improve the performances. Secondly, clamping only near the semi-major axis edges using clamp springs enables better low pressure sensitivity compared to an all-side edge clamped sensor structure. This caters to increased deflection as the clamp spring provides more diaphragm flexibility even under very low applied pressure. A very low minimum detectable pressure (MAP) is also achievable with this L-camped element. The designed diaphragm element is shown in fig. 3.7. As vertical pressure is applied to the diaphragm the separation between the diaphragm and the bottom electrode varies yielding a

fluctuation in the capacitance. Ignoring the fringe electrostatic field flux lines, the capacitance variation is governed by [16]:

$$C = \frac{\epsilon_r \epsilon_o A}{d} \quad (3.19)$$

where ϵ_r is the relative permittivity of the dielectric material, ϵ_o the permittivity of free space, A the cross-sectional area of the diaphragm and d the separation between the electrodes/plates.

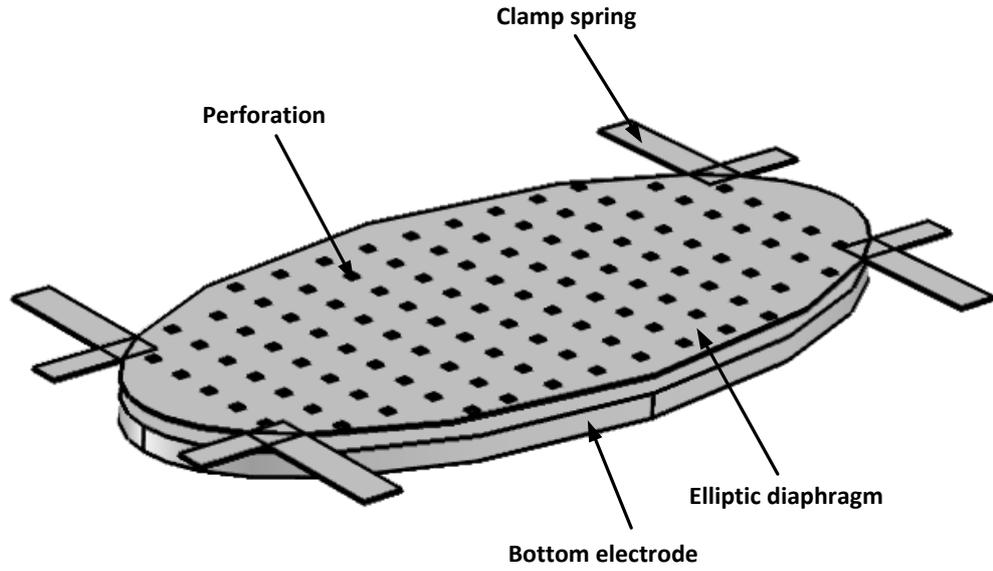


Fig. 3.7: Perforated elliptic diaphragm, clamped at the semi-major axis using clamp springs

Under the influence of applied pressure, the diaphragm deforms due to the distributed stress and strain. The edge clamping using the clamp spring causes the diaphragm to deflect in a non-uniform manner. As a result the change in distance between the diaphragm and the bottom electrode is not uniform throughout the cross-section, and hence (3.19) must be obtained by surface integration over the 2D (spatial) distance between the electrodes, which can be written as [16]:

$$C = \iint \left[\frac{\epsilon_r \epsilon_o}{d_o - D(x, y)} \right] dx dy \quad (3.20)$$

where d_o is the distance between the plates at zero pressure and $D(x, y)$ is the incremental change in the distance after a deflection at a spatial location (x, y) . The effective plate

deflection (w) for an elliptic diaphragm can be expressed as:

$$w = \left(\frac{1}{\pi r_1 r_2} \right) \iint D(x, y) dx dy \quad (3.21)$$

where r_1 and r_2 are respectively the radii of the semi-minor and semi-major axis, while the effective deflection, w in the z direction is determined by averaging the spatially integrated deflection over the entire surface area of the elliptic diaphragm. The diaphragm thickness is very small compared to the other dimensions, and, hence assumption of Love-Kirchhoff's hypothesis [69] is considered in the stress analysis of its deflection, as mentioned earlier. Furthermore, the maximum diaphragm displacement is considered to be around half its thickness in the desired dynamic range, so that 2D plane stress analysis of thin plates is satisfied with this design. Three independent in-plane strain tensor components only exist in this assumption and can be arranged in a matrix form as given below:

$$\varepsilon(x, y) = \begin{bmatrix} \varepsilon_{xx}(x, y) \\ \varepsilon_{yy}(x, y) \\ 2\varepsilon_{xy}(x, y) \end{bmatrix} \quad (3.22)$$

The stress tensor components σ_z , σ_{xz} and σ_{yz} become null in such an analysis and the stress tensors conventionally arranged in a 3×3 matrix reduces to a singular column matrix consisting of only three stress tensor component, given as [69]:

$$\sigma(x, y) = \begin{bmatrix} \sigma_{xx}(x, y) \\ \sigma_{yy}(x, y) \\ \sigma_{xy}(x, y) \end{bmatrix} \quad (3.23)$$

Assuming a uniform stress distribution throughout the diaphragm, the internal forces that cause the bending of the element can be found by integrating the stresses through the thickness. Further, assuming the diaphragm material to be isotropic and homogenous; its stress-strain behavior can be considered to be linear within the range of its elastic limit. The diaphragm performance will not degrade when the applied pressure load does not exceed so as to deflect it beyond its elasticity; hence the dynamic range of the device will also fall within this region. The linear elastic region is shown in the fig. 3.8. This stress-strain linearity assumption up to the elastic limit is based on the Hook's law and can be given by [69]:

$$\begin{bmatrix} \sigma_{xx}(x, y) \\ \sigma_{yy}(x, y) \\ \sigma_{xy}(x, y) \end{bmatrix} = E \begin{bmatrix} \varepsilon_{xx}(x, y) \\ \varepsilon_{yy}(x, y) \\ 2\varepsilon_{xy}(x, y) \end{bmatrix} \quad (3.24)$$

An elliptical structure, as mentioned earlier can be considered as a circle pulled along the opposite sides in order to be stretched, and hence, the radius in that direction increases (becomes the semi- major axis), while the area remains unchanged. The stress and strain analysis of the elliptical structure is assumed to follow an edge clamped circular structure. The deflection analysis of this geometry is discussed in the next section.

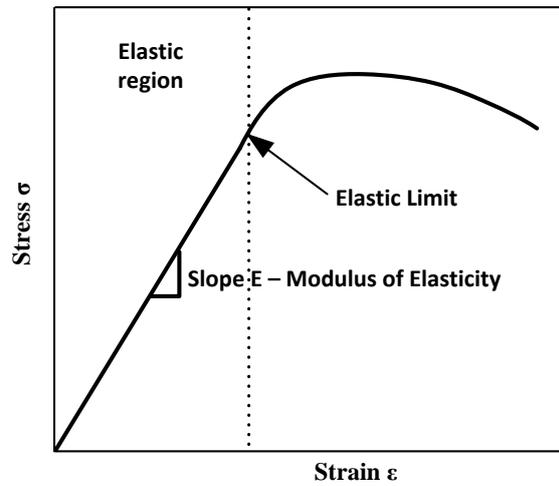


Fig. 3.8: Stress-Strain relationship curve [69]

3.4.3 Structural description and layout design

Fig. 9 shows the cross-section of the target CMOS integrated MEMS perforated elliptical structured capacitive pressure sensor in SiGe-MEMS process technology. This CMOS+MEMS process has $0.6 \mu\text{m}$ as the minimum feature size for the design of MEMS devices. An elliptical structured micro diaphragm using Poly-SiGe material of spatial axis $(r_1 \times r_2)$ with dimensions of $100 \mu\text{m}$ and $4 \mu\text{m}$ thickness is clamped at the semi-major axis for the curvilinear deformation of the entire diaphragm at low pressure loads. Comparatively, the deflection of any all edge clamped diaphragm at very low applied pressure, is almost negligible yielding poor sensitivity and low dynamic range [7].

The proposed microstructure is fabricated by stacking on top of the CMOS conditioning circuit designed in 180 nm TSMC CMOS technology as shown in fig. 3.9. The on-chip readout circuit is used for improving the strength (clarity) of the sensed weak signal. The low thermal

variation of the poly-SiGe material used for the MEMS sensor structure offers minimal thermal drift in the performance of the underlying conditioning circuit MOS devices. The interconnection of the microstructure and the CMOS circuit is through low resistivity poly-SiGe vias as indicated in the fig. 3.9. Redundant vias are designed for improved connection and to avoid degradation of interconnections due to via failure during etching. The top aluminum metal layer of the CMOS process is used to connect the electrodes of the capacitive MEMS sensor to bonding pads for test access. Longer metal interconnects are designed with redundant holes for substantial reduction in stress as larger features yield increased stress leading to low process yield. Increased mask layers can also lead to poor yield; hence few mask layers are merged to form single mask. Eventhough this merging of the mask layouts poses challenges in the layout design; it significantly reduces the production cost.

The electrical isolation between the MEMS structure and the CMOS circuitry is generally achieved by the oxide layer; however as a method to substantially reduce the parasitic issues due to CMOS top metal interconnections, an additional isolation layer that also substantially reduces the threshold voltage variation of underlying MOS devices is included in this process. Moreover this 400 nm thick silicon carbide (SiC) passivation layer defends the underlying CMOS circuits from the strong HF based release etchant done during the MEMS device process. Poly-SiGe anchors of height 3 μm and width 0.8 μm firmly fixes the clamp spring at the edges of the elliptic diaphragm along the semi-major axis. Multiple anchors are employed so that the membrane will be held intact during release process catering to successful release. Anchor arrays are designed to ensure that the MEMS structure will stand the robotic handling during processing. Moreover the residual stress in the diaphragm can cause the membrane failure during etching; hence the proper design of anchor is necessary to achieve a successful process outcome. Further, these arrays of anchors are explored for obtaining specific bending moments at the edges of the diaphragm that can withstand the specified pressure range. Anchors are semi-conductive; hence precautions are taken while designing the bottom electrode to avoid possible leakage and/or short circuit.

The clamp springs are designed using the MEMS structure layer so that a single mask is required for deposition and release etch. As a beneficiary process outcome, the planar perforations in the diaphragm override the necessity for reducing the structure thickness to avoid post release sliding, thus overcoming the sensitivity vs. linearity trade-off. The sacrificial oxide layer (replaced by air-gap dielectric) is etched out through the top-side linearity enhancement perforations of the diaphragm, using them as the structure release holes/vias as well. The dimensions of the release holes/perforations is 10 $\mu\text{m} \times 10 \mu\text{m}$ and are spaced at a spatial pitch of 10 μm throughout the diaphragm plane, which as a consequence, results in relatively less deflection in the high pressure range

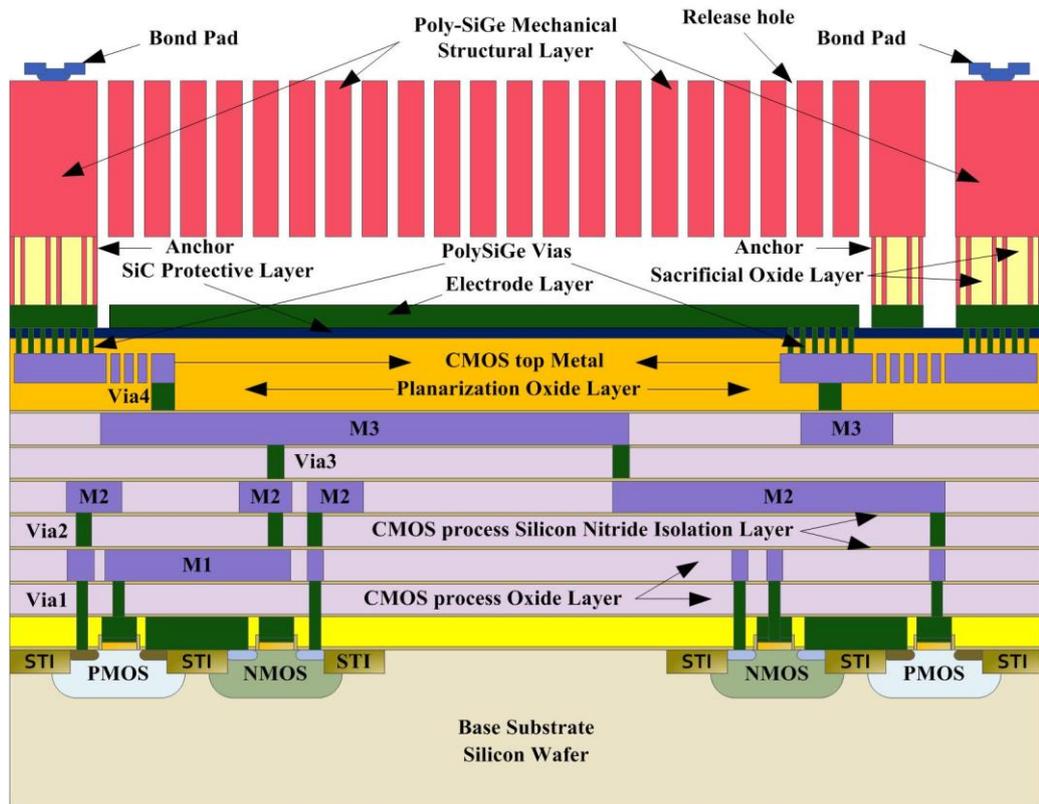


Fig. 3.9: Cross-section of the target CMOS integrated SiGeMEMS process for integrated MEMS pressure sensor

The displacement of the diaphragm is $2\ \mu\text{m}$ for an applied pressure of $1000\ \text{hPa}$, which is half the thickness of the diaphragm ($4\ \mu\text{m}$). The narrow $3\ \mu\text{m}$ separation between the two plates (determined by the process constrained thickness of the sacrificial oxide layer) limits the dynamic range of the sensor, and as a consequence further thin plate analysis assumption also does not permit larger deflections (beyond the $2\ \mu\text{m}$ range in this case). Generally, deflection beyond half the diaphragm thickness can lead to short circuit/ leakage due to electrostatic pull-in, [72] especially for this diaphragm design whose lateral dimensions are far greater than its thickness; however, the perforated elliptic design reduces the electrostatic pull-in substantially due to lower surface-area of the capacitance, thus providing further improvements in the linearity and dynamic range of the proposed MEMS sensor. Moreover, the $4\ \mu\text{m}$ thick Poly-SiGe mechanical layer processed around $300\ ^\circ\text{C}$, provides increased stiffness; hence pull-in occurs at comparatively higher voltage. Thus the collapse of the mechanical layer with the bottom electrode due to electrostatic effect is almost negligible. Finite element analysis revealed that a deflection of up to $2.2\ \mu\text{m}$ does not significantly deteriorate the sensor performance.

The deflection (w) of the edge clamped elliptic diaphragm in thin plate regime can be easily developed by modifying the deflection equation of a circular diaphragm. The circular membrane's deflection equation given in [69] can be modified for elliptic membrane as below:

$$w = \left[\frac{P_o}{64Dr_2^2} \right] (r_2^4 - r^2 r_2^2) \quad (3.25)$$

where P_o is the applied pressure, r_2 is the length of the semi-major axis, r is the polar coordinate and D is the flexural rigidity. It is evident from equation (3.25) that the diaphragm deflection increases fractionally with an increase in the length of the semi-major axis r_2 of the elliptic diaphragm. The large value of r_2 can seriously alter the elliptic geometry, rendering poor deformation and nonlinearity; hence the proper ratio of r_1 and r_2 must be maintained. It was found that by keeping the axis ratios of r_1 and r_2 less than 1:3, an optimal performance of the device could be achieved. The maximum deflection occurs at the center of the diaphragm ($r = 0$) and is determined as follows [73]:

$$w = \frac{P_o r_2^2}{64D} \quad (3.26)$$

Also, the flexural rigidity that specifies the amount of stiffness of the elliptic diaphragm membrane is given by [74]:

$$D = \frac{Eh^3}{12(1-\nu^2)} \quad (3.27)$$

where h and ν are respectively the thickness of the diaphragm and the Poisson's ratio. A proper choice of material that has a moderate modulus of elasticity (E) is critical to achieve optimum deflection as it influences the stiffness in greater extent. Higher the modulus of elasticity, higher will be the flexural rigidity, leading to higher membrane stiffness thus resulting in poor deflection. Moreover, referring to equation (3.27), diaphragm thickness h can be reduced to compensate for the increased stiffness in materials that has high modulus of elasticity; however, the risk of device failure will also be high. On the other hand, keeping the thickness high will not provide a significant increase in stiffness, for diaphragms with material having low modulus of elasticity. The 4 μm thick poly-SiGe diaphragm (with 70% of germanium) provided an optimum flexural rigidity for the desired dynamic range. Substituting (3.27) into (3.26), the deflection of the plate can be given by:

$$w = \left(\frac{r_2^2}{h^3} \right) \left[\frac{3P_o(1-\nu^2)}{16E} \right] \quad (3.28)$$

From (3.28) it is more evident that the ratio between the length of the semi-major axis and the elliptic diaphragm thickness directly influences the deflection at the center of the diaphragm. Thin diaphragms can deflect more yielding good sensitivity, however linearity is penalized, hence more importance was given to the characterization of the radial dimensions of the diaphragm, r_1 and r_2 . The poly-SiGe diaphragm with its low modulus of elasticity of around 130 GPa [75] gives increased deflection even at a very low applied pressure of 100 Pa. This offers the advantage of low minimum detectable pressure, thus increasing the dynamic range of the sensor. Also, for the same surface area, the elliptic diaphragm deflects more under a very low applied pressure compared to a circular diaphragm structure.

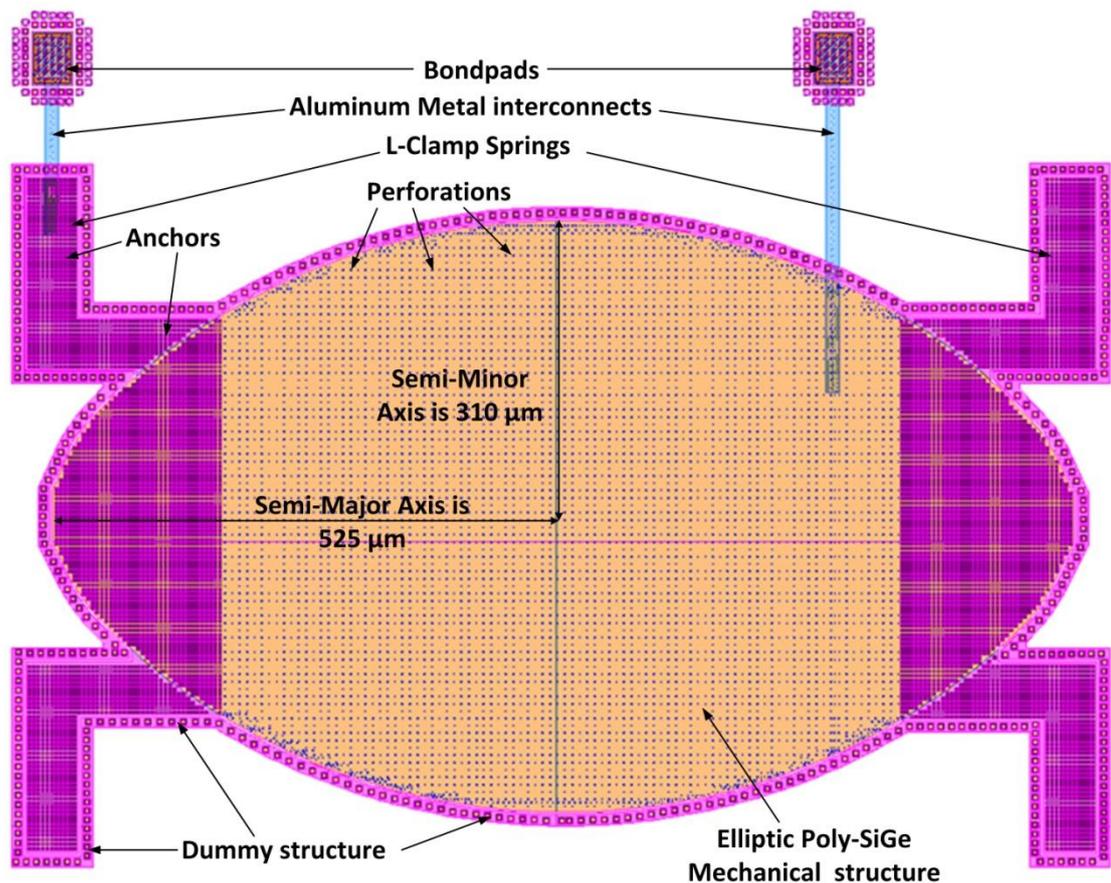


Fig. 3.10: Layout design of the elliptic diaphragm

Layout design of the MEMS elliptic capacitive pressure sensor designed using the SiGeMEMS design kit is shown in fig. 3.10. An all angle polygon drawing tool of L-Edit MEMS software offered by Tanner v15.1[®] is used to overcome the challenges in designing the smooth edged elliptic structure. For successful process outcome from design to fabrication and packaging to ship-out, several design precautions such as polygon angles, anchoring of the device, length of the free standing structure and spacing of perforations were taken. Even though caliber being the leading DRC tool (design rule check) was used to conform to the process design rule, an additional secondary check with the foundry process engineer after every design progress of the device helped to overcome several design constraints.

A closer look at the device design will reveal some of the design methodologies employed for achieving the successful structure release and prototyping. The curved edges in elliptic structure are realized by drawing and connecting many slanted angled polygon structures as shown in fig. 3.11. The minimum allowed polygon angle is not violated while doing so. Anchors placement and spacing are done to withstand the pressure loads of robotic handling while processing and packaging. Modeling of arrays of anchors as discussed earlier were employed so that the released diaphragm can withstand the static pressure load difference 1.0 bar that occurs between the top and bottom side. Moreover, simulation of the designed structure revealed that acceleration even above 3000 g did not cause structural failure, thus concluding the satisfactory layout design. Several dummy structures that surround the device layout are designed to avoid any accidental filling of foundry fill dummies on the device area. Perforations are placed well away from the anchors to ensure proper anchoring without any lift-off during release etch, in addition, minimum spacing of these layers from the free standing structure edges was also maintained to preserve the integrity of the sensor geometry during the release process.

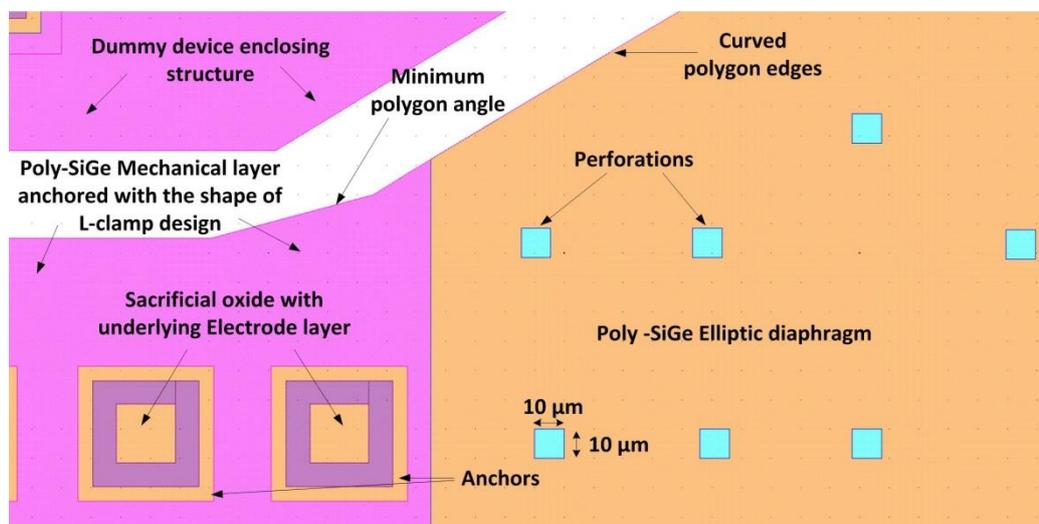


Fig. 3.11: A portion of the elliptic diaphragm showing the layout design methodology

Dual in line package with an ESD taped lid for option to open for device exposure to physical quantities was preferred, as fewer numbers of pin for both CMOS and MEMS device are sufficient. Fig. 3.12 shows the package layout design of the multiuser wafer project (MPW) with 28 pins. It can be noted that there are various other devices present in the layout which is irrelevant to this work. Underlying on-chip CMOS readout circuit is not visible as the additional filling is done to meet the foundry density requirement. Bond pins 25 and 24 provide options for external connection of MEMS device to off chip readout circuit. Bond pins 26 and 27 are for the readout purpose. The design rules for standard ASIC bonding for cavity size $900\ \mu\text{m} \times 900\ \mu\text{m}$ are met; some important package layout design strategies are [76]:

- The bondpins are distributed along the 4 sides of the cavity on which the chip will be mounted. Bondpads are also distributed equally along the four sides of the chip.
- A $100\ \mu\text{m}$ of pitch distance between two adjacent bondpads are maintained for auto wire bonding.
- A minimum distance of $120\ \mu\text{m}$ between a corner bondpad is kept.
- The bond wires from middle bondpad to middle bondpin on each side are kept as small as possible.
- Crossing of bonding wires that can short circuit the devices and CMOS circuits is avoided.
- The angle between the edge of the die and the bondwire is kept at an angle greater than 45° .
- Maximum length of the bondwire is kept less than 3 mm to achieve better accuracy.

3.5 Model analysis

Model structural analysis is much simplified by numerical method using finite element analysis (FEA). The traditional analysis method that provides the most appropriate solution for any solid in solid mechanics is now commonly used for MEMS multi-physics discipline where mechanical and electrical analysis is required. To analyze the displacement for the pressure load, an elliptical element with known mechanical properties and defined boundary (surface enclosing the geometry) conditions is divided in to N number of partition (dividing the interval of integration). Then the appropriate simple function for formulating displacement is applied to each partition and solved to obtain products. Summing all these products resulted in a solution to the integration of the displacement function over the entire region [77]. Thus an appropriate solution with very low error is obtained using the numerical integration. CAD software was utilized to speed up the analysis as the diaphragm dimensions are typically large. Further software tools provide self-adaptive analysis where the number of sections called mesh can be varied during analysis for more appropriate solution to reduce error.

A versatile CAD tool, COMSOL multi-physics v4.2a[®] that provides electro-mechanics interface to combine solid mechanics module and electrostatics is utilized to optimize the performance and dimensions of the elliptical geometry diaphragm. Perforated elliptical geometries are not predefined in CAD tools, further no option for creating such model directly in the 3D work plane of the geometry model tool is available; hence the elliptic geometry is drawn in the 2D work plane with desired dimensions, then multiple tiny 2D square blocks were drawn and difference Boolean operation was invoked to create perforations on the elliptic 2D structure. 3D model of this geometry is then extruded and material properties were assigned for the diaphragm. Further boundary conditions were applied and tetrahedral mesh size was optimized for sector FEA analysis. The steps involved in this study are described as a block diagram below in fig. 3.13.

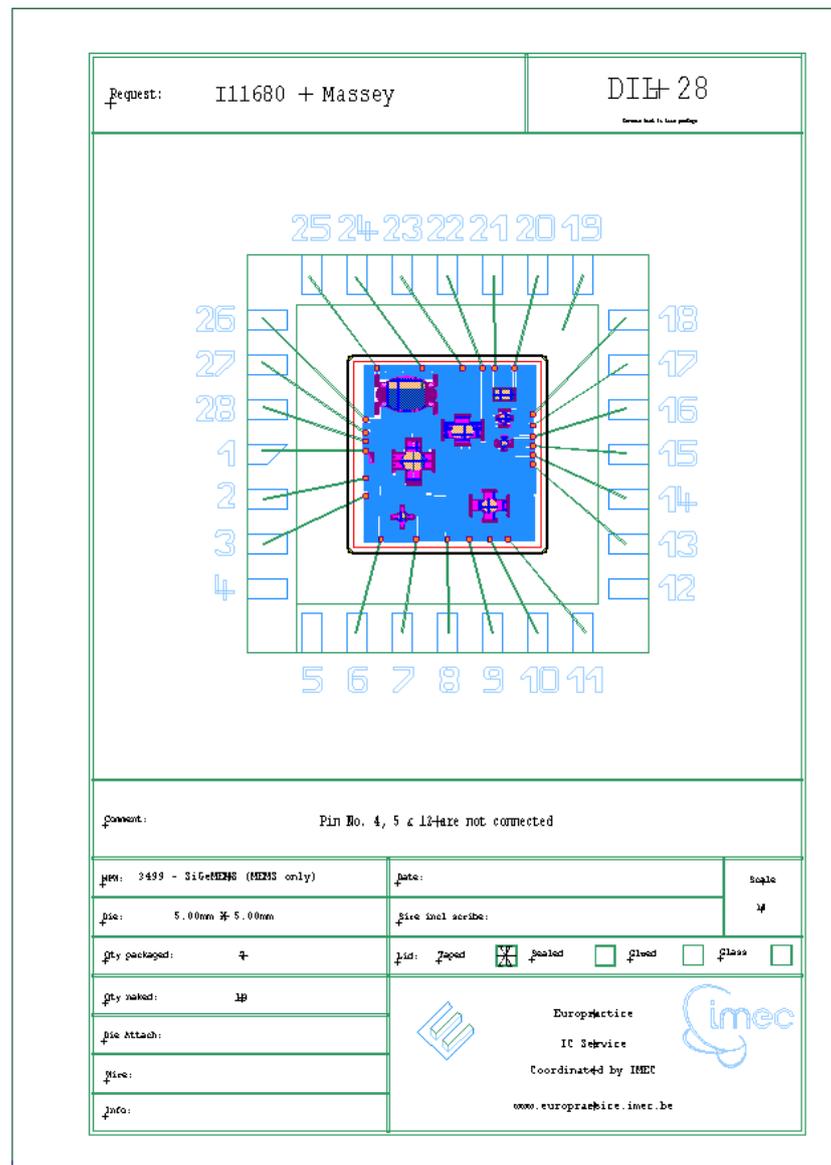


Fig. 3.12: Package layout of CMOS+MEMS design

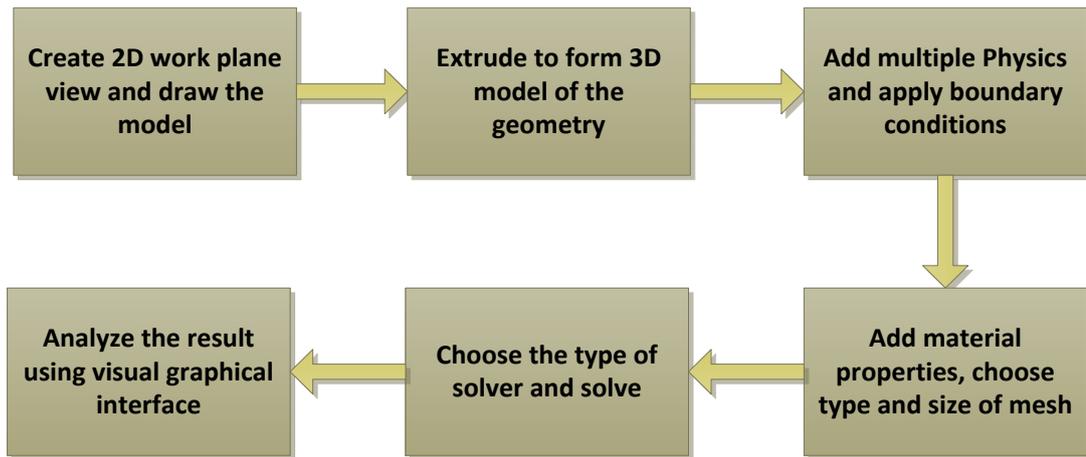


Fig. 3.13: COMSOL model analysis procedure

Two important characteristics were targeted in this analysis. Firstly, to determine the capacitance variation with applied axial (normal to the surface) pressure and secondly, to observe the corresponding vertical displacement that causes the change in capacitance for the entire load sweep. These are critical in studying the linearity of the device as assumption of a linearly elastic material model was used to characterize the sensor. Solid mechanics analysis was utilized to study the displacement of the membrane for the applied load pressure. For the parametric pressure sweep analysis, axial load from 10 to 1000 hPa in steps of 10 hPa were provided. The observed displacements were between 0.09234 μm and 2.05 μm . Deformed geometry interface that uses Arbitrary Lagrangian Eulerian (ALE) method to deform the mesh was invoked to visualize the nature of model deflection. A separate rectangular structure to represent the air dielectric medium between the capacitive electrodes is designed. This helped in forming a moving mesh physical model to extract the varying capacitance under the applied pressure. Electrostatic physical analysis was then carried out to acquire the diaphragm surface capacitance and the instantaneous capacitance variation. With the applied bias voltage of 1.4 Volts, the incremental capacitance variation (DC) was found to be between 0.0463 and 0.8213 pF (an increase over the no-load idling diaphragm capacitance of 2.57 pF). This wide linear response of the device is due to the deflection of the membrane under the pressure load from 50 to 1000 hPa. The sensitivity of the sensor is thus calculated to be approximately 0.775 fF/hPa (with around 1% non-linearity). Fig. 3.14 shows the deflection analysis simulated results of the perforated diaphragm, obtained from the visual graphical interface of COMSOL. Analysis showed that the sensor characteristics in terms of capacitance variation (DC), linearity and displacement performance with applied pressure load (in the range of 50–850 hPa) were satisfactory. The results indicate improved performances in terms of dynamic range, minimum detectable pressure and diaphragm elastic limit. Experimental results and comparisons are left for discussion in the final Chapter.

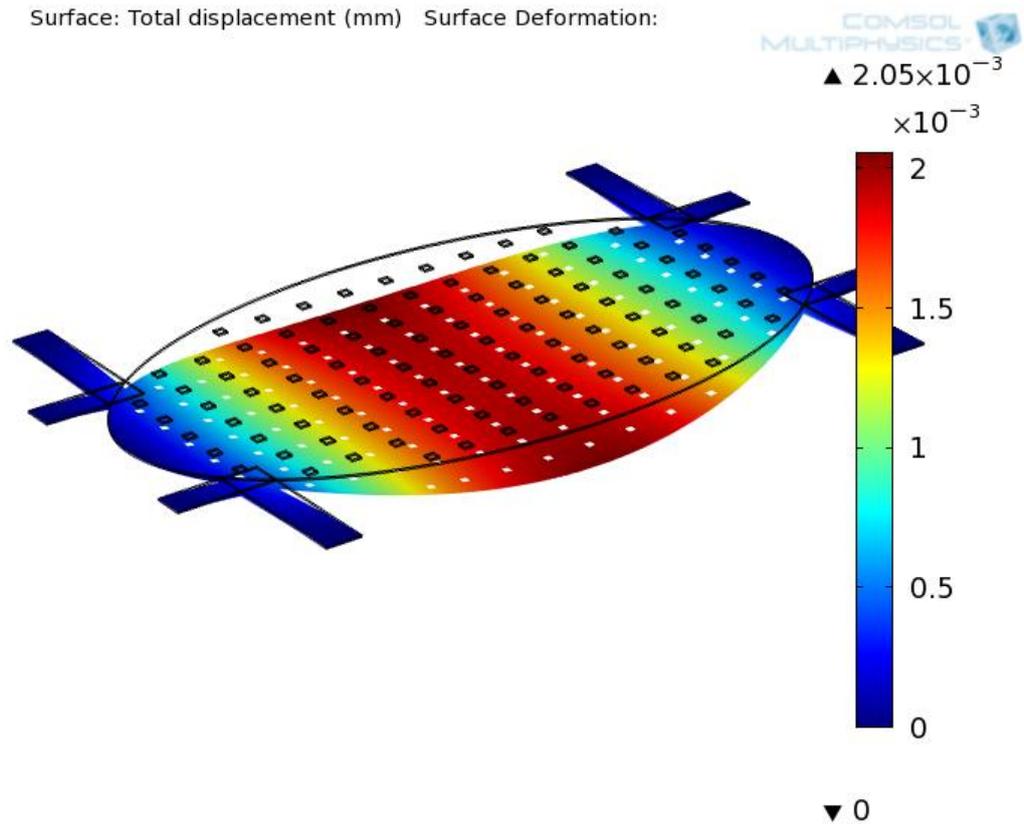


Fig. 3.14: Displacement analysis of the elliptic diaphragm

3.6 Post-process sealing

The fabricated poly-SiGe capacitive membrane integrated with readout CMOS part must undergo a post process to seal the device, forming a MEMS capacitive pressure sensor device. To achieve a wider dynamic range sensing device, proper choice of sealing method is critical. The three major types of pressure devices that can be formed based on the choice of sealing are absolute, gauge and differential pressure sensor [2]. For most biomedical and chemical pressure sensing application, sub-Torr pressure sensing device is necessary; hence absolute pressure sealing mode is adapted to obtain a sub-atmospheric pressure sensing device with wider dynamic range. Device sealing was performed with a specific process flow that is compatible for SiGe CMOS+MEMS processed chip. A standalone SiGeMEMS process (which has to be the top wafer of the sealed pressure sensor) is carried out on a separate $\langle 100 \rangle$ Si substrate, the process is stopped with the patterning of Electrode layer as the top layer for this wafer as shown in fig. 3.15. Further deposition and patterning steps of SiGeMEMS process is neglected for this die, in order to allow the Electrode layer to be later sealed on top of the structural layer of SiGe CMOS+MEMS wafer. As structural layer is of the same material except with higher thickness, sealing of the similar material layers will not be cumbersome.

Patterning of the Electrode layer of the top wafer must be done cautiously for allowing free diaphragm movement of the bottom wafer under applied pressure after sealing. Two critical design aspects were considered; firstly, the patterned electrode layer of the top wafer should not limit the deflection of the bottom diaphragm after bonding. Secondly, maximum bonding regions of the Electrode layer with the bottom wafer must be achieved for better bonding strength and longevity. The Electrode layer is patterned in such a way that it will have contact only at the center of the structural layer for maximum stress transfer. This will avoid any contact of the Electrode layer with rest of the structural region, thus permitting the free movement of the diaphragm. However for better wafer bonding, the Electrode layer was also patterned to ensure good contact with the dummy layers and anchor regions of the bottom die. Bonding failure that can occur under repeated application of load is thus avoided. Next, a silicon substrate backside etch is performed on this wafer (which is to be the top wafer). Once this wafer is bonded on to the SiGe CMOS+MEMS wafer, this back side opening will act as a pressure inlet channel. DRIE oxide-etch is performed for this deep etch as the passage is needed to be opened till the Silicon Carbide (SiC) layer as shown in fig. 3.16. As the Electrode layer is patterned to a central stem like diminutive structure, risk of structural breakage with applied pressure is high; hence an additional SiC layer support to keep the stem structure intact is necessary. Moreover this SiC passivation provides increased membrane strength for other layers and hence holds the wafer together. As the backside opening is very much confined to the size of the stem structure (forming a square window), wafer damage due to backside etch is negligible.

A direct bonding between the SiGe CMOS+MEMS wafer and the back etched standalone SiGeMEMS wafer is then carried out under high vacuum to form the absolute capacitive pressure sensor. The top layer of both the wafer is of poly-SiGe (with germanium 70%) material; hence the bonding temperature that exceeds poly-SiGe deposition temperature may cause changes in material properties of the device layer. This can seriously degrade the device performance. Further CMOS circuit interconnects and vias can withstand up to 500° C, any process temperature above this value can cause degradation in interconnections. Considering the above limitations, a low temperature plasma activated direct bonding is done after initial pre-processing of chemical mechanical polishing (CMP). Annealing is performed at a very low temperature of 400° C to enhance the strength of bonding. Fig. 3.17 shows the cross section of SiGe CMOS+MEMS with an array of anchors; bondpads are not included in this figure for better clarity of the anchor regions. Moreover as the diagram is not to scale, avoiding the bondpads (which are placed at the edges of the wafer) makes the bonding region more visible in the subsequent diagrams. The cross section of the bonded wafer is shown in fig. 3.18. The central stem electrode layer of top standalone SiGeMEMS wafer is intended to transfer stress on the diaphragm (mechanical layer) of the bottom wafer, under the influence of the external

applied pressure through the inlet. As discussed earlier, the center deflection of the diaphragm greatly influences the sensitivity of the device; hence the reason, the top electrode layer of the standalone SiGeMEMS wafer (top wafer shown in fig. 3.18) is designed to transfer the induced stress (resulted by the applied pressure) only on to the center of the sensor diaphragm (bottom wafer shown in fig. 3.18). This has resulted in increased deflection and sensitivity of the integrated SiGeMEMS sensor micro-system.

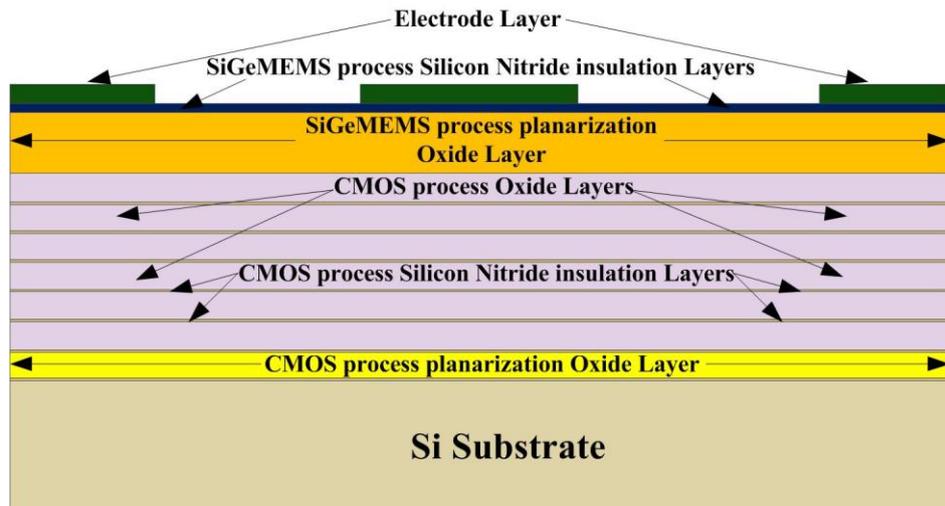


Fig. 3.15: Standalone SiGeMEMS processed top wafer

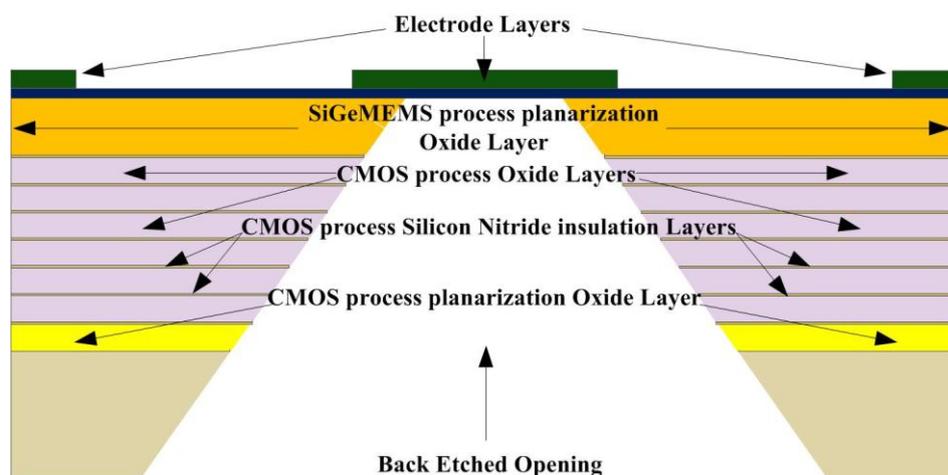


Fig. 3.16: Backside etched top wafer

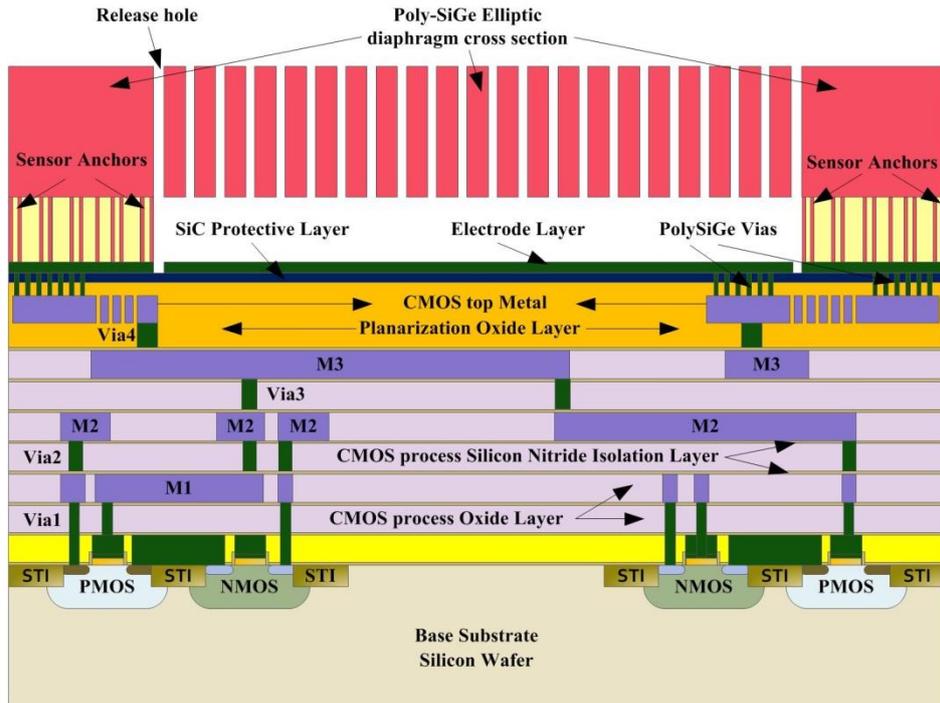


Fig. 3.17: Cross-section of integrated SiGe CMOS+MEMS sensor (bottom wafer)

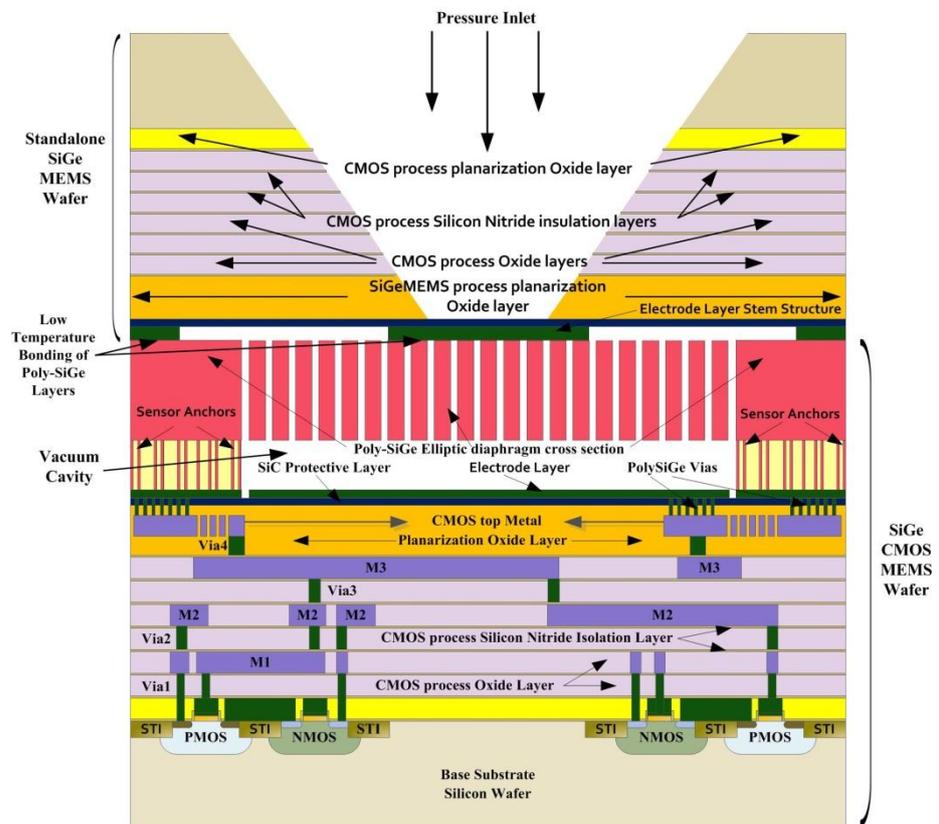


Fig. 3.18: Cross section of MEMS integrated sealed absolute pressure sensor

3.7 Conclusion

A highly sensitive integrated capacitive pressure sensor is designed and analyzed using a 0.6 μm feature size SiGe CMOS+MEMS process. The on-chip signal conditioning circuitry was designed in 0.18 μm TSMC CMOS technology vertically integrated (in 3D) with the MEMS process. The capacitive pressure sensor was analyzed under a range of pressure loads. The novel perforated elliptic diaphragm, clamped at the semi-major axis yielded a wide dynamic range. Clamp springs designed to edge clamp the diaphragm increased the sensitivity significantly without degrading the linearity performance. Plasma activated bonding significantly reduced the bonding temperature, thus negligible change in diaphragm material properties was observed. The MEMS device which was sealed as an absolute pressure sensor, exhibited a very low minimum detectable pressure (MDP) of around 2 hPa when simulated. A wide dynamic range of around 950 hPa was also noticed. Device non-linearity was found to be under 1 % for the full scale range of applied pressure. A high gain precision conditioning circuit that is designed to cater for both low supply voltage functionality and weak sensor signal amplification is discussed in the next two Chapters. The sensor readout circuitry is discussed in two parts for the purpose of clarity. Sensor readout frontend that constitutes pre-conditioning and amplifier stages are discussed in Chapter 4, whereas the readout output stages that includes filtering and low output impedance buffer are discussed in Chapter 5. Simulations analysis that was carried out by sinusoidal excitation at different stages is shown appropriately at the end of each discussion. The experimental results with test setup are also discussed in Chapter 8. This integrated pressure sensor, based on the observed performance characteristics with appropriate packaging, can be used for biomedical applications such as single/multi-point catheter pressure monitoring, intraocular pressure measurement, pacemaker pressure device and other coronary pressure measurements.

Chapter 4

SiGeMEMS Sensor Readout Frontend

4.1 Introduction

The need for a high gain, low noise amplifier has recently increased steadily as the intricate design of the MEMS sensors are employing industry standard CMOS processed chip as the base layer. Eventhough CMOS MEMS sensors have been in the market for a decade, research on integration of sensors with on-chip signal conditioning circuit has recently increased due to the development of high gain sub-micron CMOS signal conditioning circuits. Sensor's output signal being very weak needs to be substantially increased for the further beneficial process. This weak signal further imposes a greater challenge in designing a competent conditioning circuit. A pre-conditioning circuit is therefore compulsory before the actual signal amplification, for exceptional pick-off of the sensed physical quantity. The block diagram that shows the essential components of the sensor readout frontend is shown below in fig. 4.1.

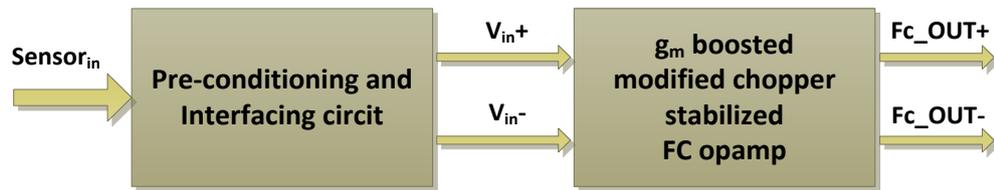


Fig. 4.1: Block diagram of sensor readout frontend

Although there are few pre-processing circuitry involved in conditioning the weak sensor output, the main component that needs more design attention is the amplifier circuit. The inherent noise and nonlinearity in an amplifier can significantly reduce the possibility of recovering the weak sensor output. Thus, design of low noise and highly linear amplifier is necessary. An operational transconductance amplifier (OTA) is the preferred signal amplification circuit due to its high output impedance that results in high gain [78]. The output current of the OTA is proportionate to the differences of both the input voltages; hence, the reason it is referred to as a transconductance (g_m) amplifier. Conventional single stage OTA has disadvantages such as limited linear input voltage range, low bandwidth and low output impedance; therefore it does not meet today's demand for the sensor's signal amplification. This then leads to the requirement of an advanced OTA such as telescopic or folded cascode amplifier. The choice of the advanced OTA depends on the performance demand posed by the sensor system. The desired performances for a capacitive type pressure sensor whose output will

be in the order of a few micro-volts are high gain, low noise, good linearity, low offset, high slew rate and high power supply rejection ratio. Although telescopic amplifier can meet some of the requirements, they still fail to provide high output voltage swing, which is critical in modern low supply voltage circuit design. Moreover, high output voltage swing is the primary requirement for any sensor readout circuit design. A folded cascode amplifier is a special variation of telescopic amplifier. In this cascode connected transistor pairs which are of different type from the input differential pairs are used to achieve high output voltage swing [79]. It also exhibits good a frequency response and provides moderately low noise. The single stage conventional folded cascode operational amplifier yields only up to 40 dB, which is not promising for the sensor readout application. Hence a novel design that can yield a gain of at least 90 to 100 dB and an output voltage swing of 0.6 V to 0.8 V for a 1.4 V supply is the primary target. Once the desired amplifier design is achieved, further, design of output stages that enable interfacing and driving of the external circuit is essential.

4.2 Design aspect

The on-chip sensor interface circuit is a crucial component that converts the low level transduced sensor output to a useful electronic signal with a low noise factor [41]. The weak sensor signal is degraded due to the RC transmission line effect of the electrical interconnect metal wires from the microstructure to the CMOS circuit. Thus, sensor signal conditioning poses a significant challenge in designing a comprehensive frontend readout circuit and the overall performance of the sensor module largely depends on the readout circuit implementation. The circuit performance parameters that are targeted for enhancement are high gain, low noise, low power, reduced area and high linearity. The three main circuit components involved are the modified chopper stabilized opamp, Gm-C low-pass filter and the self biased buffer stage. Frontend design using the modern CMOS deep submicron technology enables higher speed of the analog circuitry but makes the high gain amplifier design more challenging. Accuracy and linearity are constrained by the low voltage requirement of deep submicron processes. Furthermore, the low supply voltage constraint also results in performance degradation due to the limited input common mode range [79].

4.2.1 CMOS folded cascode operational amplifier imperfection

The two major drawbacks that significantly degrade the performance of CMOS folded cascode operational amplifier (Shown in fig. 4.2) are noise and offset. The types of noise that occurs in any CMOS circuitry can be [20] are shot noise, thermal noise, flicker noise, burst noise and avalanche noise. The two major prominent noise sources that directly influence the performance degradation in CMOS folded cascode operational amplifier are thermal and flicker

The error in the difference of both input voltages commonly referred to as differential input causes overall sensing system accuracy issues, especially for sensor readout applications, since the signal voltage will be of a few micro-volts. A few hundred micro-volts of input offset voltage that occurs in CMOS folded cascode opamp will substantially affect the overall sensitivity of the sensor system. This high input offset voltage must be compensated. The single stage folded cascode operational amplifiers that were reported till now to reduce these imperfections, yields low gain and poor output voltage swing. On the other hand, simple two stage design reported to improve the gain and output voltage swing, provided a poor frequency response and low settling time. Thus a competent design that yields a very low noise floor as well as overcoming the above tradeoff is needed.

4.2.2 Noise reduction technique in folded cascode operational amplifier

Folded cascode operational amplifier (FC opamp) being a better choice for sensor readout, has a significantly high noise floor compared to the telescopic counterpart; hence noise reduction technique is required for the accurate conditioning of micro-volt sensor signal. Fully differential configuration will be the immediate choice of noise suppressing technique as it has inherent immunity towards input offset voltage and provides better common mode rejection ratio (CMRR). The advantage of high CMRR in this configuration substantially rejects common mode noise thus eliminating external noise. Further, since the output voltage is differential; it swings over the common mode voltage, hence the output voltage swing, which is critical for sensor signal conditioning, increases by a factor of 2. Moreover, due to the differential output, while examining the transfer function as a power series, it is found that the even order harmonic gets cancelled, thus providing less harmonic distortion.

The other approaches to reduce noise involve proficient design of the amplifier input and output stage transistors. The possible design aspects are:

- g_m of the input transistors must be appropriately increased to reduce thermal and flicker noise.
- Chopper stabilization technique to push the input signal to odd harmonics will significantly lower input offset issues, thermal and flicker noise. By employing fully differential chopper stabilization technique the thermal and flicker noises are shifted to the higher chopping frequency.
- g_m of the current sources must be lowered to reduce noise keeping in mind not to minimize I_D much. Reduction in I_D lowers the gain, hence a competent design is necessary to overcome tradeoff.

The above noise reduction technique can substantially provide less possibility for gain enhancement. The relationships between transconductance, drain current and output resistance of a MOSFET transistor are given by [20]:

$$g_m = \frac{2I_D}{(V_{GS} - V_{TH})} \quad (4.3)$$

$$g_m = \sqrt{2\mu_n C_{ox} \frac{W}{L} I_D} \quad (4.4)$$

$$r_o = \frac{1}{\lambda I_D} \quad (4.5)$$

where g_m is the transconductance, I_D the drain current, V_{GS} is the gate to source voltage, V_{TH} is the threshold voltage, μ_n is the electron mobility, C_{ox} is the gate oxide capacitance, W the width of the channel, L the length of the channel and λ the channel length modulation. The g_m of the transistors is proportionate to the DC current I_D . Increasing the transconductance of transistors for the purpose of lowering thermal and flicker noises will cause an increase in I_D ; however, the output resistance of the transistors lowers, eventually lowering the gain. On the other hand, if the output resistance of the transistor is increased for the purpose of gain enhancement, I_D reduces causing g_m to decrease and thus increasing the noise at the input stage. To overcome this tradeoff an alternative design is required to enhance the gain without compromising noise suppression.

4.2.3 Design of folded cascode operational amplifier

The proposed high gain two stage opamp schematic design for the readout circuit which utilizes a gain enhanced folded cascode as the first stage is shown in fig. 4.3. Conventional chopper stabilization circuit shown in fig. 4.4 is used initially to reduce noise and offset. Differential transconductance boosting is done to overcome the limitations of conventional folded cascode operational amplifier and the associated tradeoff. The composite gain enhancement is achieved by controlling the g_m -boosting gain A_c of the doubly g_m -boosted cascode. If g_{mFC} is the overall transconductance of the folded cascode (FC) amplifier, and g_m the input stage transconductance, then, $g_{mFC} = g_m (1 + A_c)$ [80]. The negative feedback utilized in the doubly g_m -boosting cascode stage elevates the output impedance, leading to gain enhancement without compromising noise suppression.

The proposed FC opamp yields a higher gain-bandwidth (GBW) product than the conventional folded cascode structure without increasing the power budget. Stacked PMOS devices are utilized as the input stage of the FC opamp to further enhance the transconductance.

The noise injected by these PMOS devices is an order of magnitude lower than NMOS devices, and hence a relatively low input referred noise is achieved [79]. The proposed two stage fully differential FC opamp that utilizes two separate common source amplifiers for each FC output as shown in fig. 4.5, provides large output voltage swing. The differential output design is less susceptible to output common mode noise compared to a single-ended version. The total noise power that includes both thermal and input referred noise of the FC opamp can be approximately derived as:

$$\overline{V^2}_{in_{tot}} = 8KT \left(\frac{2}{3g_{m1,2}} + \frac{2}{3} \cdot \frac{g_{m5,6}}{g_{m1,2}^2} + \frac{2}{3} \cdot \frac{g_{m9,10}}{g_{m1,2}^2} \right) + \left[\frac{2.K_P}{(WL)_{1,2}.C_{ox}.f} + \frac{2.K_N}{(WL)_{5,6}.C_{ox}.f} \cdot \frac{g_{m5,6}^2}{g_{m1,2}^2} + \frac{2.K_P}{(WL)_{9,10}.C_{ox}.f} \cdot \frac{g_{m9,10}^2}{g_{m1,2}^2} \right] \quad (4.6)$$

where K_P and K_N are respectively the PMOS and NMOS flicker noise coefficients. The first and the second term represent thermal and flicker noise respectively. It is evident from (4.6) that thermal and flicker noises are the dominant factors that increase the noise floor of the FC opamp. Therefore, two methods were employed to reduce the overall noise; firstly, the transconductance of the input transistors (that is $g_{m1,2}$ in equation 4.6) is appropriately increased to reduce the thermal and flicker noise components. Secondly, the effective g_m of the current source devices which is $g_{m5,6}$ in (4.6), is kept somewhat low so as to reduce noise while not minimizing I_D (in order to maintain reasonable slew rate). Reduction in the g_m of the current sources reduces the output impedances resulting in reduction of the overall voltage gain, and hence, a careful overall gain vs. noise design trade-off is necessary. In addition, to further reduce the flicker noise the transconductance of current sinks ($g_{m9,10}$) is also substantially lowered.

The composite design of the fully differential chopper stabilization within the FC opamp structure (with a modified chopping technique), enables improved output signal precision and significant noise reduction thereby increasing the sensitivity of the front-end. Comparatively, the conventional chopper introduces random spikes at the output causing a residual offset of up to 500 nV/ $\sqrt{\text{Hz}}$, which is significantly high for precision sensor application. Thus conventional chopper modulator (shown in fig. 4.4) which distorts the output signal, needs proper modification. The modified chopper modulator is designed with a transmission gate block to modulate the input signal, thus introducing negligible spikes when demodulated. Fig. 4.7 shows the differential transmission gate chopping network operating with in-phase and out-of-phase chopping frequencies. The employment of two different chopping frequencies along with

complementary PMOS choppers makes possible the reduction of the residual offset falling in the range of $100 \text{ nV}/\sqrt{\text{Hz}}$. The theoretically achievable improvement in residual offset is given by the ratio of $f_{\text{chophigh}} (\Phi_2)$ and $f_{\text{choplow}} (\Phi_1)$ [79]. Furthermore, gain accuracy of the modified chopper is also found to be quite high.

The stability and frequency compensation of the signal conditioning circuit was analyzed by determining the location of the poles and zeros introduced by the parasitic capacitance at different stages. The location of the poles and zeros for the first stage are shown in fig. 4.6. The pole-zero doublet introduced by the gm-boosting stage degrades the transient response of the opamp. This doublet appears as a slow exponential term in the step response increasing the settling time of the opamp. In order to make the transient response behavior similar to that of a single pole system, the zero, ω_z was pushed to a higher frequency by increasing the drain current (bias current) of the gm boosting stage. The g_m of this stage was also appropriately adjusted (by varying the device aspect ratios) to transform the pole into a complex conjugate pair [81], thus eliminating the slow response introduced by this stage. In addition, pole splitting achieved by miller compensation provides stability to the two stage opamp [48], however it introduces a RHP zero. Increasing the impedance in the feed-forward path pushes the RHP zero to a higher frequency, thereby increasing the stability [50].

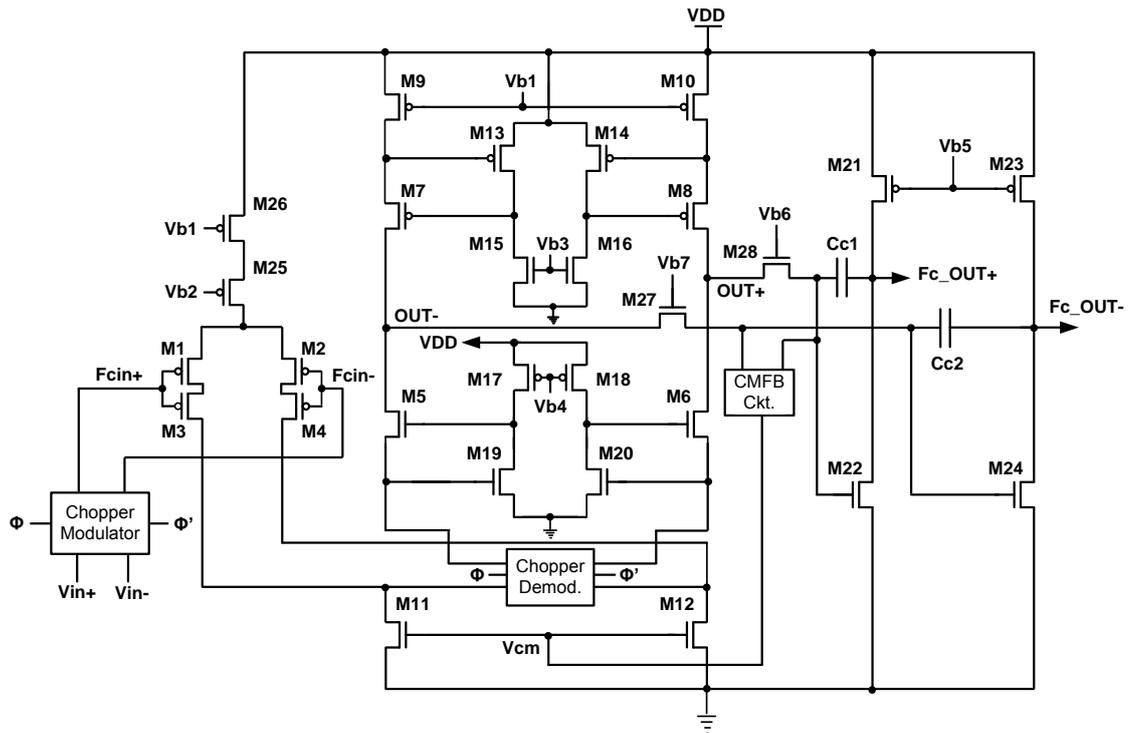


Fig. 4.3: Proposed FC opamp with conventional chopper stabilization

Hence an NMOS transistor biased in the triode regime, in series with the compensation capacitor is used to yield an improvement in stability over the conventional miller compensation technique. Proper choice of the coupling capacitor, CC (CC1 and CC2 in Fig. 4.5) enables the under damping of the settling behavior by setting the phase margin above 45°. However, the increased phase margin causes bandwidth limitations, and hence, a careful bandwidth vs. stability trade-off was implemented. The frequency response analysis revealed that the CS second stage of the FC opamp introduces additional two poles and one zeros. The simplified and combined poles and zeros of the proposed one half of the two stage g_m boosted fully differential folded cascode opamp can be given as:

$$\omega_{p1} = \frac{1}{C_{GD7} + C_{GD5} + C_{DB7} + C_{GD22}} \quad (4.7)$$

$$\omega_{p2} = \frac{1}{C_{DB19} + \left(1 + \frac{g_{m5}}{g_{m1m2}g_{ds7}}\right)C_{GD5} + C_{GS22} + C_{GS5}} \quad (4.8)$$

$$\omega_z = \frac{g_{m21}}{C_{GD22}} \quad (4.9)$$

$$\omega_{p3} = \frac{1}{C_{DB22} + C_{chop} + \left(1 + \frac{g_{m22}}{g_{ds19}g_{m5}}\right)C_{GD22} + \left(1 + \frac{g_{m5}}{g_{ds7}g_{m1m2}}\right)C_{GS5}} \quad (4.10)$$

where ω_{p1} is the dominant pole, ω_{p3} is a non dominant pole, and ω_{p2} and ω_z are the pole zero doublet. ω_{p4} is a high frequency pole and is less significant as it falls beyond unity gain bandwidth of the FC opamp.

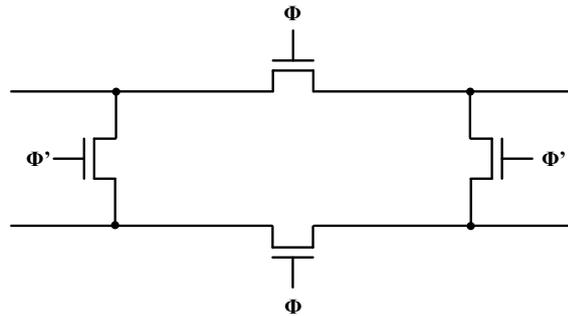


Fig. 4.4: Conventional chopper stabilization circuit [52]

The zero ω_z of the pole zero doublet is pushed to higher frequency beyond unity gain frequency for improving settling time. Thus both ω_{p4} and ω_z become close enough to be as good as cancelled; hence are insignificant. The dominant pole ω_{p1} is brought closer to the origin, whereas the inter-stage pole ω_{p3} is taken to the higher frequency by pole splitting as shown in fig. 4.6 (b). C_{GD} in the above equation indicates the gate to drain parasitic capacitance of the corresponding transistors, whereas C_{DB} is drain to bulk parasitic effect and C_{GS} is gate to source parasitic capacitance. The chopper transistor's parasitic effect C_{chop} is also considered in this analysis. It can be noted that dominant pole ω_{p1} is influenced much by the output node of the first stage. Transistor M22 of the second CS stage is also connected to the first stage output node through the triode connected transistor M27 and therefore contributes to the dominant pole. Miller compensation is employed to split the poles ω_{p1} and ω_{p3} [20]. As each node gives rise to a pole in the transfer function of the FC opamp that can affect settling time and hence the speed, introducing additional node in the design for the purpose of frequency compensation is extensively reduced. Thus most of the frequency compensation is taken care by proper choice of the associated transistor's g_m and I_D values.

A Differential difference amplifier (DDA) common mode feedback shown in fig. 4.8 is employed in the design to set the common mode output of the opamp. A differential CMFB is employed in order to achieve large output swing [50]. DDA is an extension of a basic differential input opamp circuit. An opamp generally has one differential input, whereas in DDA two differential input are employed. The difference in these two differential voltages is converted into current by the transistors M49 to M55, the current sinks M55 and M56 gives a proportionate corresponding voltage for the converted current. The output voltage of a DDA shown in fig. 4.8 can be given as:

$$V_{cm} = A_{FC} [((Out +) + V_{ref}) - (V_{ref} - (Out -))] \quad (4.11)$$

where A_{FC} is the open loop gain of the FC opamp first stage. DDA having a large transconductance and low non linearity efficiently stabilizes the output common mode voltage. Simple CMFB on the other hand has higher non linearity yielding poor stabilization, moreover if compensated by degenerative resistors will load the output stage resulting in poor performance of the FC opamp. To further improve the output voltage swing, common source (CS) second stage is used. As a complementary beneficial outcome CS stage provided an additional gain of 15 to 20 dB thus the overall gain of the opamp is further enhanced. The proposed g_m boosted FC operational amplifier with frequency compensation is shown in fig. 4.5. The complete circuit interface using the circuit symbols of the sensor biasing and startup circuit and its associated pre-conditioning interface circuit, which is hereby referred as the sensor frontend is shown in fig. 4.5.

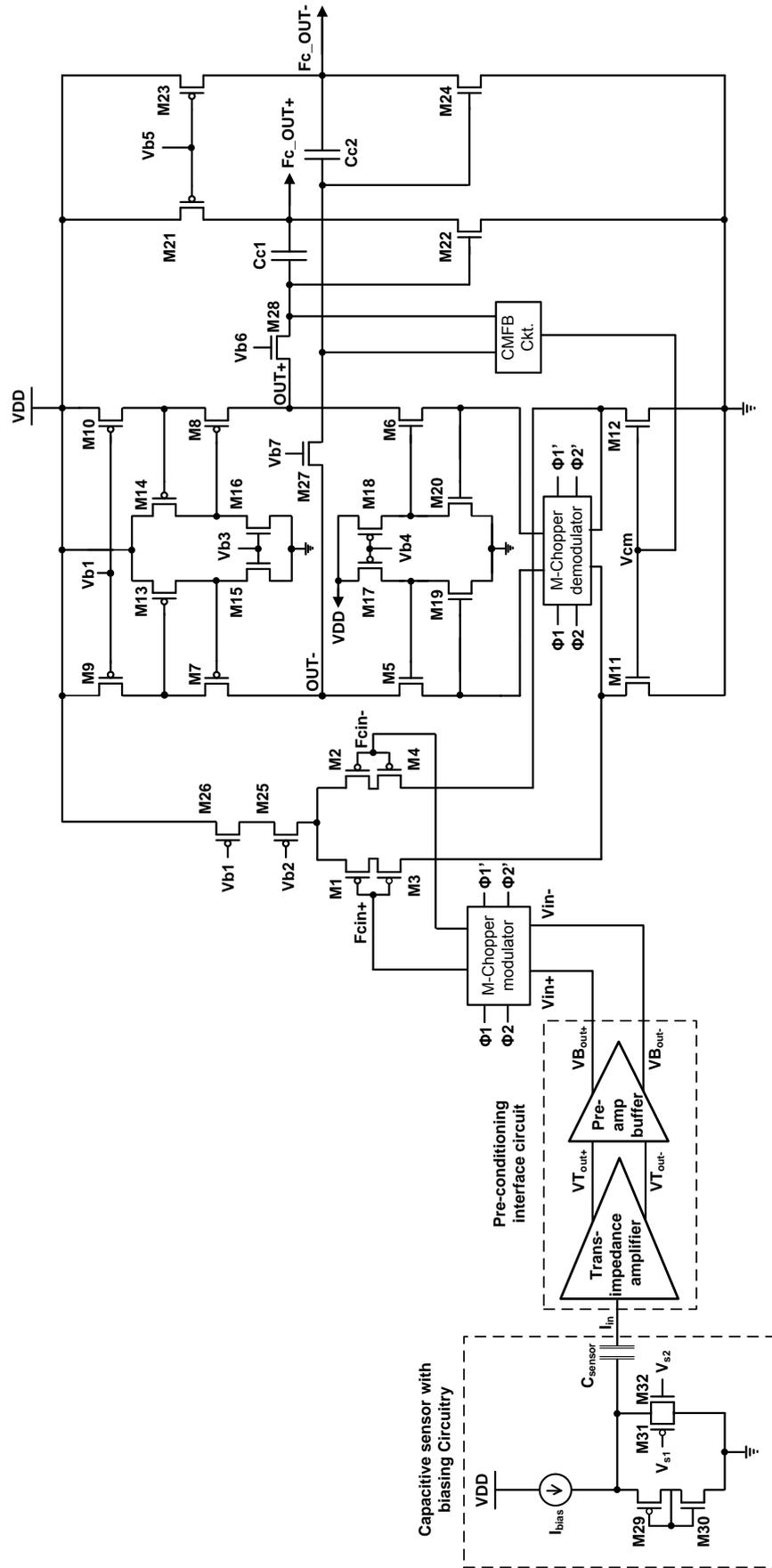
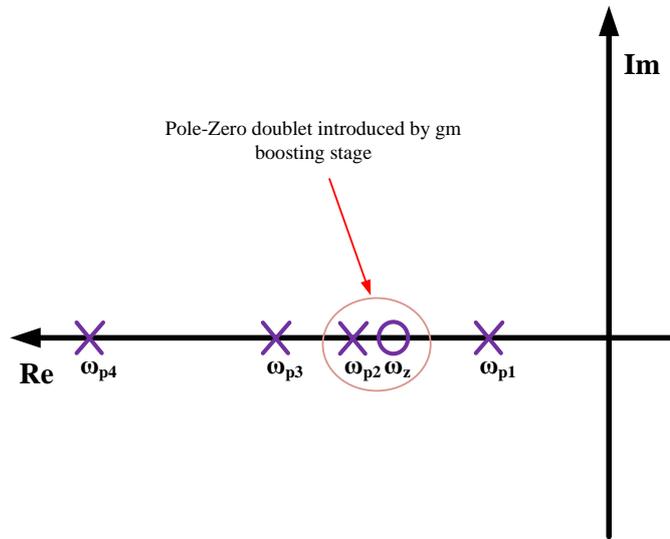
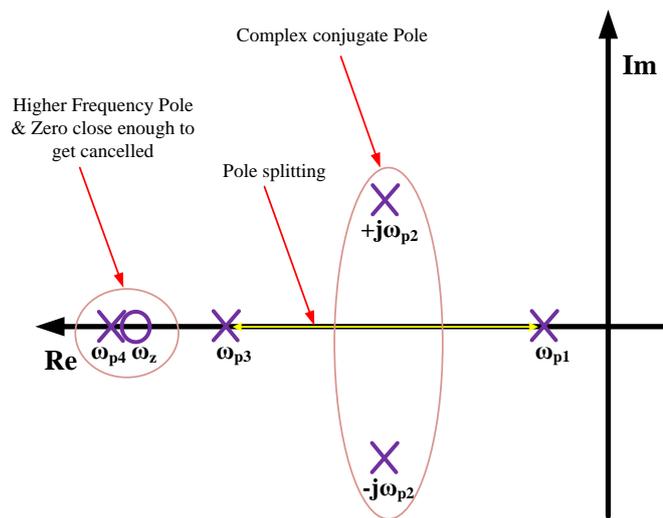


Fig. 4.5: Modified chopper stabilized g_m boosted FC opamp with pre-conditioning circuit



a) Pole - Zero Locations in Proposed gm boosted FC opamp



b) Pole - Zero Locations after compensation

Fig. 4.6: Pole - Zero Plots

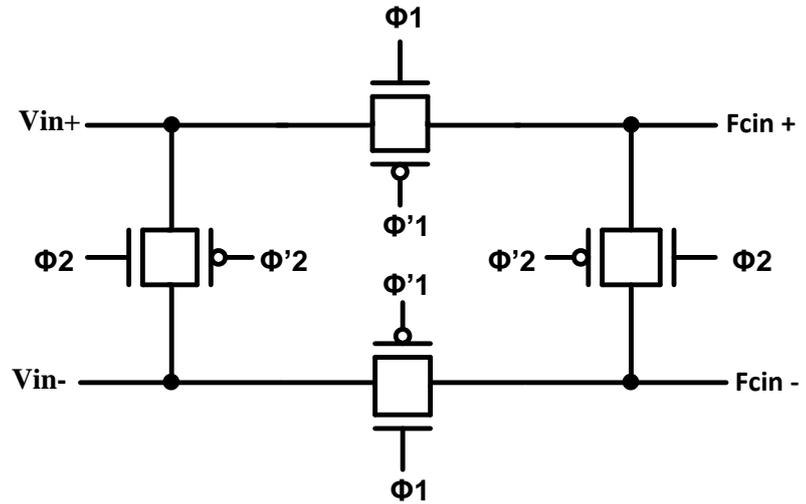


Fig. 4.7: Transmission gate chopper

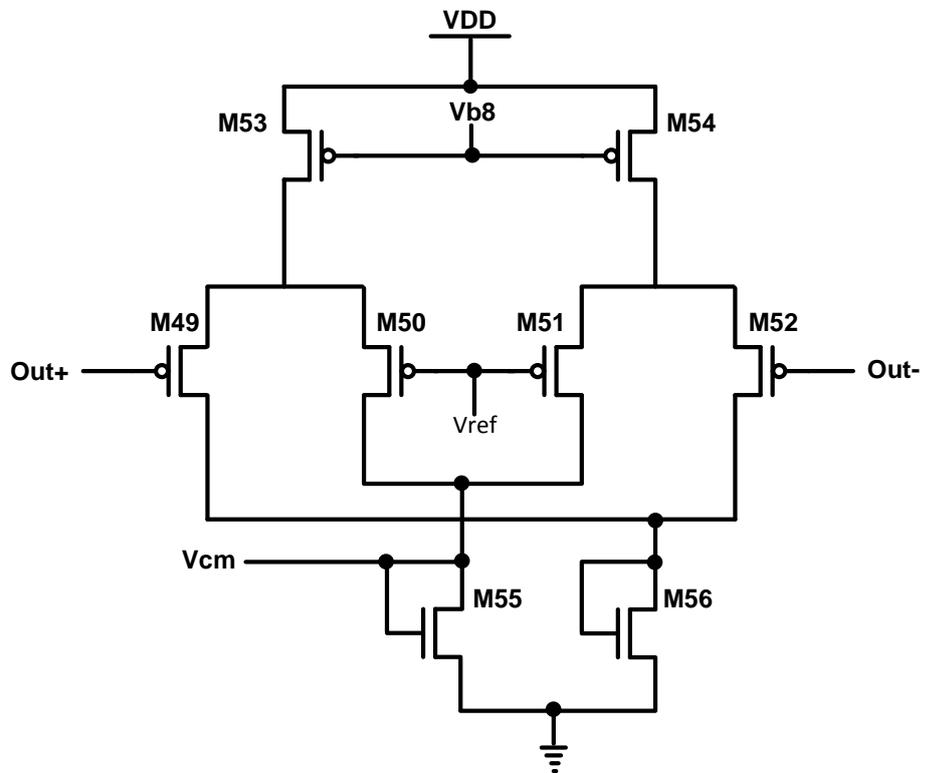


Fig. 4.8: Differential difference amplifier used as CMFB Circuit

4.2.4 Pre-conditioning interface circuit

Interfacing the high sensitive sensor output with the high performance two stage gm-boosted fully differential FC opamp is critical. The input impedance of the amplifier is moderately high and hence a proper impedance matching with the weak sensor output signal is mandatory. Interfacing techniques need two critical aspects to be addressed, firstly, the fully differential amplifier requires differential inputs, but the sensor's output is single ended; hence conversion is necessary. Secondly, a preparatory circuit that precedes the high gain FC opamp amplification is inevitable for initial signal strengthening. Moreover, impedance matching between the amplifier and the frontend interfacing circuitry must be achieved. The symbol block diagram shown in fig. 4.9 below depicts the components involved in sensor interface.

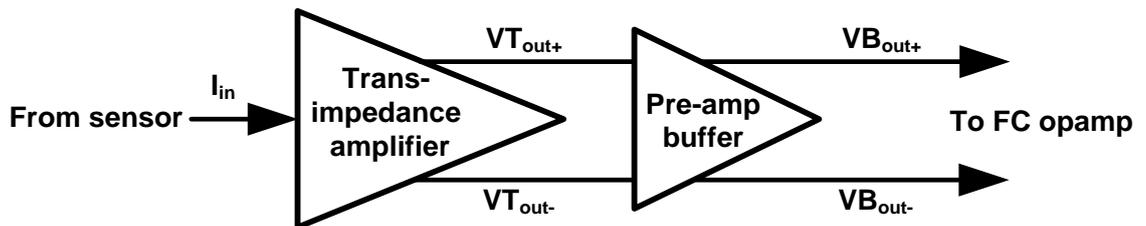


Fig. 4.9: Pre-conditioning interface circuit

A trans-impedance amplifier shown in fig. 4.10 that can provide differential output voltage in proportionate with the input current (from the sensor), is utilized as the startup circuit in this front end design. Differential common source amplifier is used due to its wider bandwidth and moderate gain, thus this initial pick-up signal enhancement makes further processing sophisticated. The advantage of using common source as the trans-impedance amplifier is its comparatively low noise floor. Further, the noise introduced by the preceding stage experiences a transitional impedance path; hence get attenuated by the high trans-impedance gain. Thus provides better performances than the common gate and source follower amplifiers. The feedback loop in the conventional circuit provides excellent attenuation to the input referred noise ($1/f$ noise); however there is a possibility of a slight increase in the noise floor due to the thermal noise provided by the feedback resistors. An imbalance in the differential output swing may occur due to a mismatch of the feedback currents in either half of the differential circuit. Larger resistance is generally required for feedback to balance the output, but will yield poor bandwidth and high power dissipation. The effect of feedback resistor on the noise and bandwidth can be given by the input referred noise equation [20]:

$$\overline{i_{rin}} = \frac{4.k.T.BW}{R_f} \quad (4.12)$$

where k is Boltzmann constant, T temperature, BW bandwidth and R_f the feedback resistor. The active feedback transistors M39 and M40 biased in the triode region provides a better balance of the differential output even with smaller aspect ratios. Eventhough the active feedback contributes to some amount of noise, the overall noise level of the circuit is within the acceptable limit. The input referred noise caused by the transistors of one half of the circuit is given as:

$$\overline{i_{in}} = \frac{\overline{i_{trans}} Z_L}{Z_f} \quad (4.13)$$

where i_{trans} is the noise current due to the transistors, Z_L impedance due to M35 and M36 and, Z_f the impedance due to the feedback transistors M39 and M40 operated in sub-threshold region. The diode connected load M33 and M34 do not require additional bias circuitry hence reduces some amount of power dissipation. The major drawback of these diode connected transistors is the reduced headroom hence can significantly affect the output voltage swing. However, since high gain is not the expected outcome at this part of the readout circuitry, g_m of the input transistors (which generally contributes to gain enhancement) and the current sinks are varied

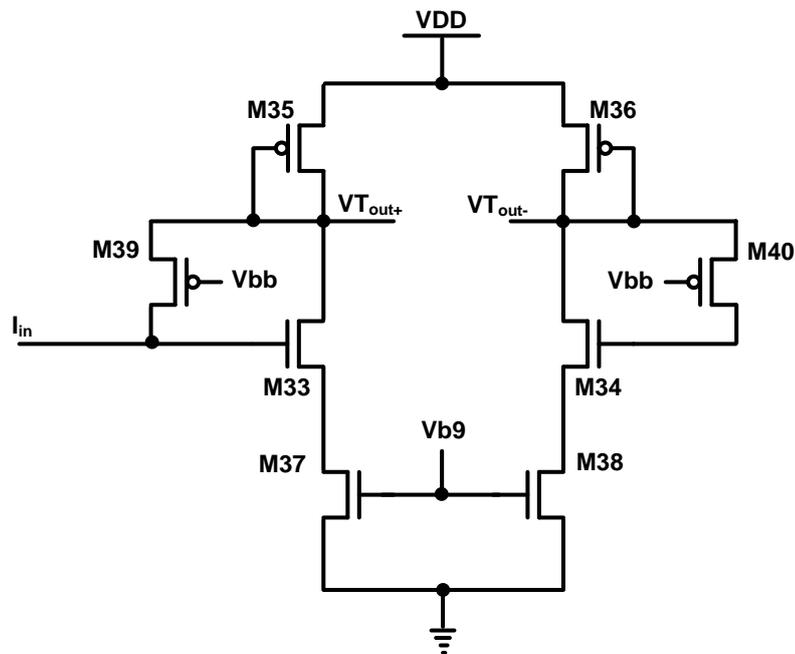


Fig. 4.10: Trans-impedance amplifier

accordingly to the desired output voltage swing. Precise designs of the aspect ratios of the transistors are done to achieve a good output voltage swing and to meet noise and bandwidth requirements.

The topology of the differential source follower pre-amplifier (pre-amp) buffer is shown in fig. 4.11. The main purpose of this pre-amp buffer is to do a preliminary frequency shaping and to amplify tiny signals without degrading it with inherent distortion and noise. There is an impedance mismatch between the trans-impedance and FC opamp, as the trans-impedance amplifier has moderate output impedance, whereas FC opamp has high input impedance. This pre-amp buffer of the frontend optimizes the impedance match between the trans-impedance amplifier and the g_m boosted folded cascode opamp.

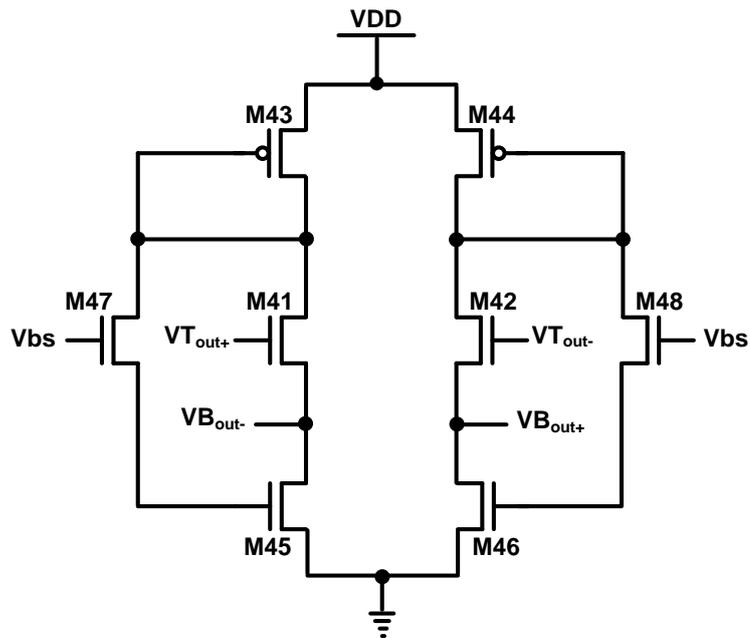


Fig. 4.11: Pre-amp buffer

The moderate output impedance makes trans-impedance amplifiers a poor driving circuit and hence may not drive the high gain FC opamp. Moreover, to avoid loading these initial startup circuits by the gain enhancing FC opamp, isolation is necessary. The modern sub-micron CMOS technology makes the pre-amp buffer design more challenging. The low supply voltage for the voltage follower provides more non-linearity yielding poor performance to the overall sensor readout frontend. Basic unity gain voltage follower due to their unity feedback yields poor output voltage swing. Flipped voltage follower (FLVF) on the other hand is unsuitable for implementation as pre-amp because it provides high gain errors (gain is a lot less than unity). The significant negative gain can substantially degrade the overall gain enhancement; hence a buffer circuit with low gain error and good linearity must be designed. Differential source

follower, which uses local feedback technique, is mostly implemented with a self bias design; however constant current biasing is provided to transistors M47 and M48 in order to get better swing. The diode connected load eventhough reduces the voltage headroom; the g_m of the transistors M41 to M46 and the feedback current is designed appropriately to obtain a desirable output voltage swing. The feedback transistors avoid the unity feedback thus further improving output voltage swing. The circuit is also designed with a fewer number of transistors as inherent noise and distortion is a primary concern that can damage the weak sensor output at this stage of signal conditioning. The DC levels at the output of a trans-impedance stage is shifted to low levels due to the balanced design for the differential output, hence there is risk of clipping the lower part of the sensed signal with further amplification. Thus the transistors in the pre-amp buffer are designed with proper W/L ratios to obtain the required DC level shift.

4.2.5 Biasing circuit for the proposed FC opamp

A constant current mirror biasing is essential for a differential amplifier stage in sub-micron technology as the mismatch in MOSFET parameters between the transistor pairs can severely affect the circuit performance. The current mirror has the capability of matching device characteristics closely, even with process variations. The current mirror bias circuit designed for the folded cascode operational amplifier's process variation immunity is shown in fig. 4.12. The resistor R1 provides the reference current for this designed high precision biasing circuitry. An active reference current generator can be used alternatively, however to minimize the possibility of deviation in reference current due to process variation, resistive current source is preferred. This reference current is scaled by the W/L ratio of the NMOS transistor M57. Mirroring of this current is possible by additional connection of NMOS transistors to the gate of the transistor M57. Transistor M57 operating in active region yields stable gate to source voltage and can be used to cater for multiple current sources. Each mirroring pair can yield different bias currents scaled by the factor of their respective aspect ratios. The drain current ratios between transistor M58 and M57, if their scaling factor is equal, that is if $V_{DS58} = V_{DS57}$, the equation can be given as [20];

$$\frac{I_{D58}}{I_{D57}} = \frac{L_{57}W_{58}}{L_{58}W_{57}} \quad (4.14)$$

This then indicates that the current ratios can be set to any desired value by scaling the transistors. PMOS transistors are used as diode connected active loads to obtain bias voltages Vb1, Vb3 and Vb4, the active loads M66, M68 and M59 can be easily scaled to obtain respective bias voltages at the drain of M65, M67 and M58 respectively.

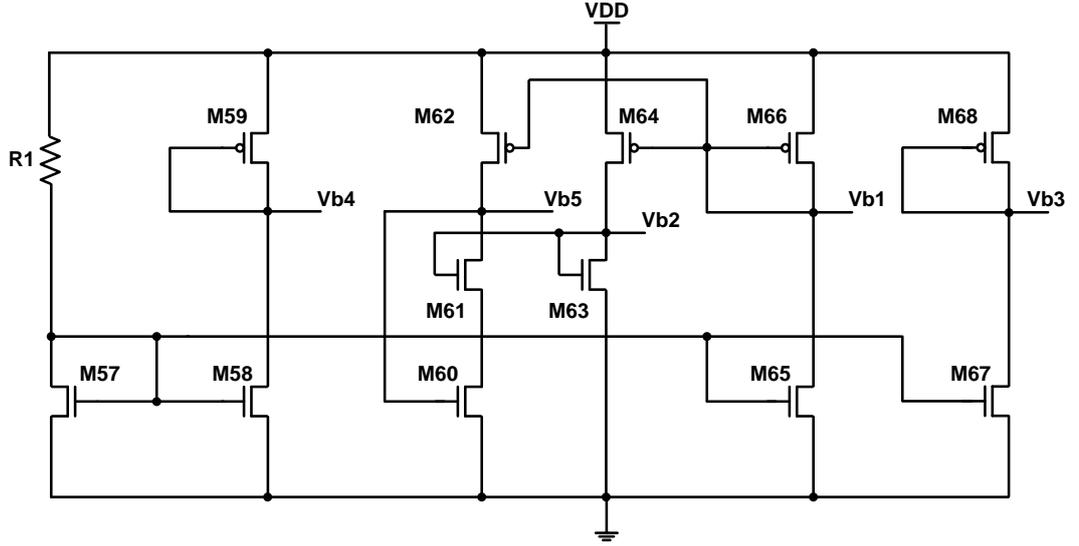


Fig. 4.12: Current mirror biasing circuitry

Cascode current mirrors are employed for bias voltages Vb2 and Vb5. As these voltages bias the input stage and output stage transistors respectively, their design is critical. All transistors M60 to M64 operating in saturation yield high accuracy, thus can significantly improve the amplifier's performance. The gate to source voltage of these transistors is increased considerably to reduce the mismatch due to threshold voltage variation, thus a high precision is obtained. Cascode current mirrors provide high input impedances hence isolate the reference current sources, therefore catering to improve the impedances at both the stages. The improvement in the output impedance provided by M61 can be given as:

$$r_{out} = (g_{m62}r_{o62})g_{m61}r_{o61}r_{o60}r_{o62} \quad (4.15)$$

The total output impedance r_{out} (looking at the drain of M61), thus increases the output impedance of Vb5 associated mirroring circuit. This leads to performance improvement of the FC opamp's second stage. The output impedance due to this cascode type current mirror eliminates any current offset. Further, increased output impedance renders less output current variation with varying input voltage, making the circuit more stable and immune to loading effect. However, increased output impedance can reduce the headroom limiting the maximum required voltage drop for reliable operation of the current source. The transconductance of g_{m62} and g_{m61} are designed appropriately for tradeoff minimization, which contributes to the precision enhancement of the amplifier performance. Moreover, their wide swing nature has a wider operating range. The uncomplicated design of this multi-current mirror biasing circuit met all required specifications to provide stable biasing voltages. Sophisticated current mirror biasing network is not preferred at this stage, as increased transistor numbers will elevate the overall noise floor of the sensor readout frontend.

4.2.6 Sensor bias and start-up circuitry

MEMS capacitive sensors need to be excited with a DC source to pick up the change in the sensed physical quantity. Generally, a direct DC voltage source can be used if the sensors are connected in a bridge circuit; however, bridge circuit provides better sensitivity with only resistive type sensors. Balancing error in the bridge due to supply voltage variation can greatly affect signal recovery in capacitive bridges. The error will be further enhanced by the succeeding conditioning circuitry providing poor performances. Moreover, as the capacitance variation in the MEMS sensor falls in the range of a few femto-farads, designing a highly precision bridge is tedious. Small variation in the physical quantity will yield smaller variation in capacitance, thus measuring the minuscule quantity requires high voltage and high frequency excitation for convincing signal pick-off if a capacitance bridge network is used. This can pose a serious drawback of increased power dissipation, which is not acceptable for integrated sub-micron technology CMOS MEMS sensor design.

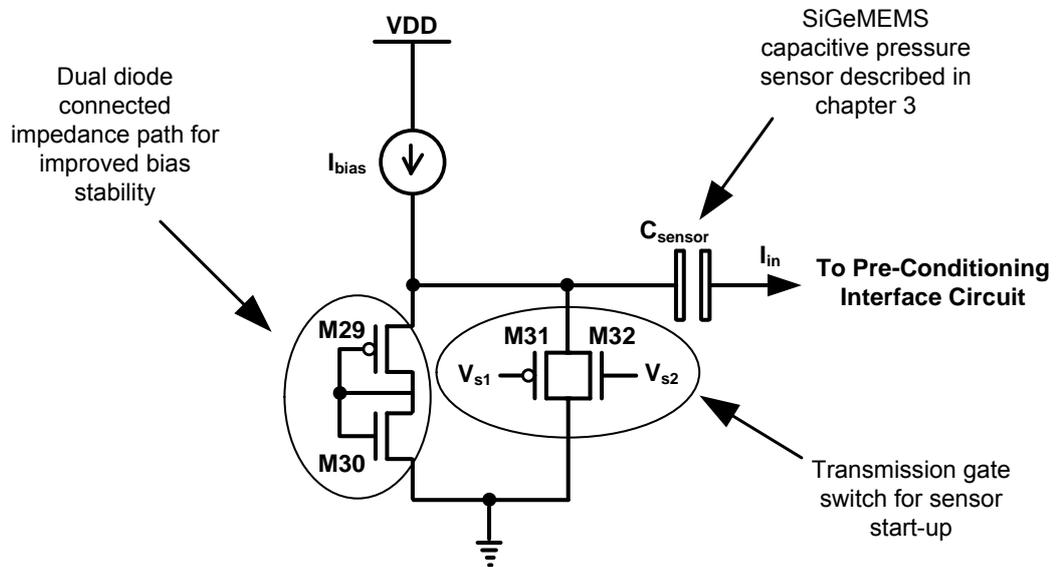


Fig. 4.13: Sensor bias and start-up circuitry

The simplest yet competent sensor excitation network with extremely low power dissipation is designed in this work. Design aspect for enhancing current mirror parameters such as dynamic range, increased output impedance and DC balance were considered for improving the sensing accuracy of the MEMS integrated sensor. Fig. 4.13 shows the circuit interconnections of constant current biasing with pre-determined I_{bias} and the associated initial start-up circuit for the MEMS capacitive sensor. Cascode current mirror source that provides high precision pick off is shown in fig. 4.14.

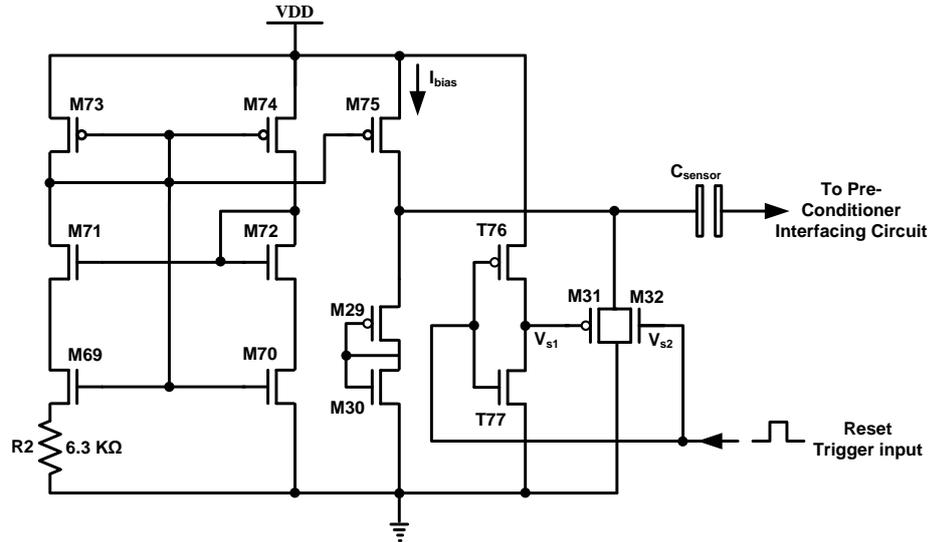


Fig. 4.14: Cascode current mirror for sensor biasing and start up

Reference current for the bias circuitry is designed with the resistor R2. Transistors M69 to M75 form the cascode current mirror circuit, whereas transistor M29 and M30 serves as an active impedance path. Almost seven transistors are employed for proper shielding from the output bias voltage variation that can occur at the drain of transistor M75. Four NMOS transistors M69, M70, M71 and M72 are used as the initial cascode current copying network for better immunity to channel length modulation. PMOS transistor pair M73 and M74 provides first level shielding for the four NMOS cascode pairs against output voltage variation. Another second stage level of shielding is designed using transistor M75 to intensify the shielding, thus almost negligible variation in the bias current occurs due to output bias voltage variation. The diode connected devices M29 and M30 are always in saturation providing a stable low impedance path that contribute to low power dissipation. All transistors operated in saturation, when V_{ds} of M75 being the output bias voltage of cascode current mirror increases, the V_{gs} of M73 and M74 remains constant and hence their drain currents are also constant. However, the current through the diode connected active resistive path M29 and M30 increases and the drop across them also increases; hence V_{ds} of M75 falls making I_{bias} constant. Thus the second shielding level protects the first level of the cascode current mirror stage against an increase in output bias voltage. On the other hand, when I_{bias} decreases, V_{ds} of M75 decreases; however as current through M73 and M74 increases, their V_{ds} increase forcing V_{gs} of M75 to increase. Increase in V_{gs} of M75 will cause increase in its V_{ds} causing I_{bias} to increase, thus I_{bias} is kept constant against decrease in output bias voltage. Therefore a highly stable constant current bias provides better compliance range that contributes in modeling high accuracy and superior precision capacitive pressure sensor system. The need of a start-up circuit for the capacitive sensing device arises from its electrical charge storage ability. Generally, each constructed capacitor has a discharging time that corresponds to its capacitance, area of the plate and the

dielectric gap. To discharge its stored electrical charge from its plate when the potential across both the plates drops down from the highest value, the capacitor generally needs a closed low impedance path. The discharging path also influences the discharging time of the stored charge as it is related to the time constant τ , given as:

$$\tau = Z_d C \quad (4.16)$$

where Z_d is the impedance of the closed loop discharging path. Greater the value of the impedance, greater will be the discharging time. The capacitive pressure sensor element if excited without a proper low impedance closed loop path can lead to stored stray charges that would distort the sensor system performance during succeeding operation. Thus precision and accuracy of the sensor device could be significantly affected; hence the capacitive sensor must be discharged initially with every start-up. Transistors M31, M32, T76 and T77 (shown in fig. 4.14) form the start-up circuit. An active transmission gate switch with transistors M31 and M32 are constructed to provide very low impedance path for a faster discharging time. Transistors of this switch are designed with minimum aspect ratios for the technology used; hence their parasitic effect together with the resistance of the channel will provide very low impedances. Due to the extremely low threshold voltage attenuation feature of transmission gates, a better switching is achieved thus catering to the faster discharging time of the stored charge. Gate voltages V_{s1} and V_{s2} excite the transistors M31 and M32 of the transmission gate switch respectively. A low voltage level at V_{s1} and a high voltage level at V_{s2} turn on the transmission gate thereby forming a low impedance discharge path for the capacitive device. A CMOS inverter is designed using transistors T76 and T77 to provide this excitation voltage. An off-chip generated external triggering circuit drives the inverter through a reset pin. The trigger pulse of a predesigned pulse-width forces the inverter output to change thereby the transmission gate is controlled at the initial startup. The input trigger pulse directly controls the NMOS device (M32) of the transmission gate, whereas output voltage of the inverter controls the PMOS device (M31). The output voltage settling time of the CMOS inverter could possibly lead to a jitter that may cause a delay in turning ON the PMOS device. This can limit the discharging time of the sensor; hence a proper pulse-width that keeps the transmission gate ON for the complete discharge of all the sensor's stray charges is necessary. When the supply voltage is turned ON with no trigger input, the inverter output starts to reach a high state. The transmission gate remains OFF during this transition time. When the trigger input pulse is given through the reset pin, NMOS device (M32) is turned ON immediately whereas the inverter output takes time to reach the low level. During this time the transmission gate is still OFF as the PMOS device still has a high input at its gate. Once the inverter's output reaches low, then the transmission gate is turned ON. This creates a very low impedance path for the capacitive sensor to discharge

the previously stored-in charges. Once the trigger pulse at the inverter's input goes low, its output goes back again to a high state. The transmission gate thus will remain OFF until the next reset.

4.3 Simulation results and discussion

The SiGeMEMS technology offers integration of MEMS device on top of a TSNC CMOS wafer. This yields a better performance of the sensor system by catering low signal to noise ratio through reduced interconnect parasitic effect, miniaturized sensor chip and very low power consumption. The layout design of the sensor readout frontend was designed in TSMC 0.18 μm CMOS technology using Tanner tool V15.1[®] as shown in figs. 4.15, 4.16 and 4.17. The minimum line width offered by this technology further lowers the parasitic effects and power dissipation. Moreover the offered options of medium and low threshold voltage transistors provide better flexibility for low voltage design. Simulation is performed using the BSIM4 model, which has a more effective MOSFET model that includes most of the physical effects that occurs in sub-100 nm regime. The other two important aspects for utilizing this model in the sensor system design are; firstly, it includes an improved model for thermal noise that occurs in the channel. Secondly, the unified flicker (1/f) noise model with bulk charge effect consideration is smooth over the entire bias regions. Analysis of the designed signal conditioning frontend circuit in 0.18 μm TSMC CMOS technology was carried out with 10 μV sinusoidal input signal of 500 Hz. The folded cascode opamp with the modified input stage and doubly gm-boosting stage provided an increased transconductance. The input differential pair transistors were designed as an interleaved multi-fingered input pairs to achieve better matching between the pairs as shown in fig. 4.18. Each input transistor (M1, M2, M3 and M4) was spitted into two parallel connected transistors for the purpose of interleaving. Transistors M1a, M1b and M3a, M3b forms one half of the stacked differential pair and transistors M2a, M2b and M4a, M4b forms the other stacked pair. An overlap multi-fingered structural design of this critical stage renders reduced process variation. Simulation results indicate that the modified chopper provided less spikes at the output of its modulator. The demodulated output was still found to have some amount of chopper residuals even-though the spikes are reduced. The waveform comparison of the conventional chopper and the modified chopper is shown in fig. 4.19. The modified transmission gate chopper that uses dual chopping frequencies (for the observed 1/f noise corner frequency of 1 kHz) offered low spikes compared to conventional chopping network. Result analysis of the designed FC opamp indicate that a single ended gain of around 97 dB along with 64° phase margin and 100 nV/ $\sqrt{\text{Hz}}$ input referred noise were achieved. The gain for the fully differential modified-chopper FC opamp was calculated to be around 105 dB. Thus the obtained magnitude response for the proposed FC opamp was found to have a high gain as well as wider bandwidth when compared to the conventional two stage FC

opamp. Also the achieved phase margin proves that the operational amplifier is stable in a closed loop configuration despite the significant open loop gain. Comparison of the gain and phase response is shown in fig. 4.20. A wide unity gain bandwidth of 200 MHz (achieved with a better roll-off), which is sufficient for the pressure sensor duty cycle, was thus achieved without compromising gain. The compensation capacitor effectively shorts the CS stage NMOS devices into diode-connected loads at the high frequency chopper residuals. This helps in minimizing the artifacts when compared to the sensed signal.

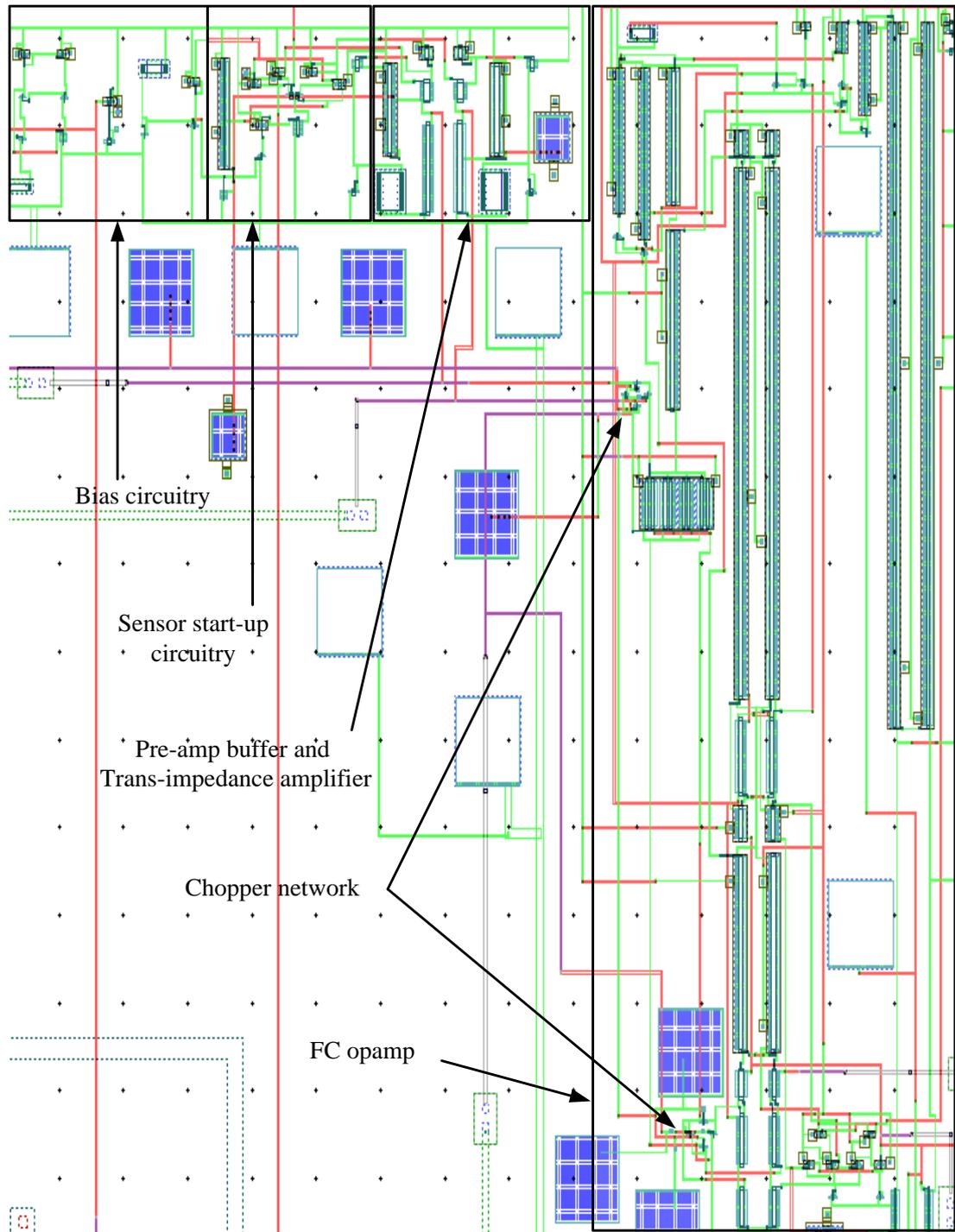


Fig. 4.15: Sensor readout frontend layout design

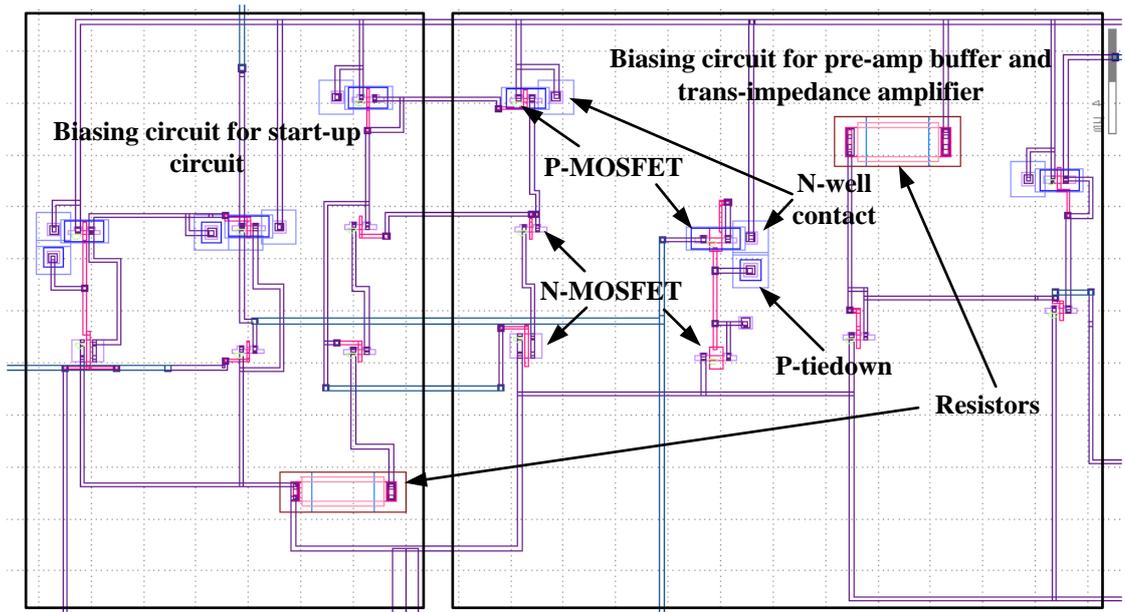


Fig. 4.16: Layout design of bias circuitry for start-up, pre-amp buffer and trans-impedance amplifier

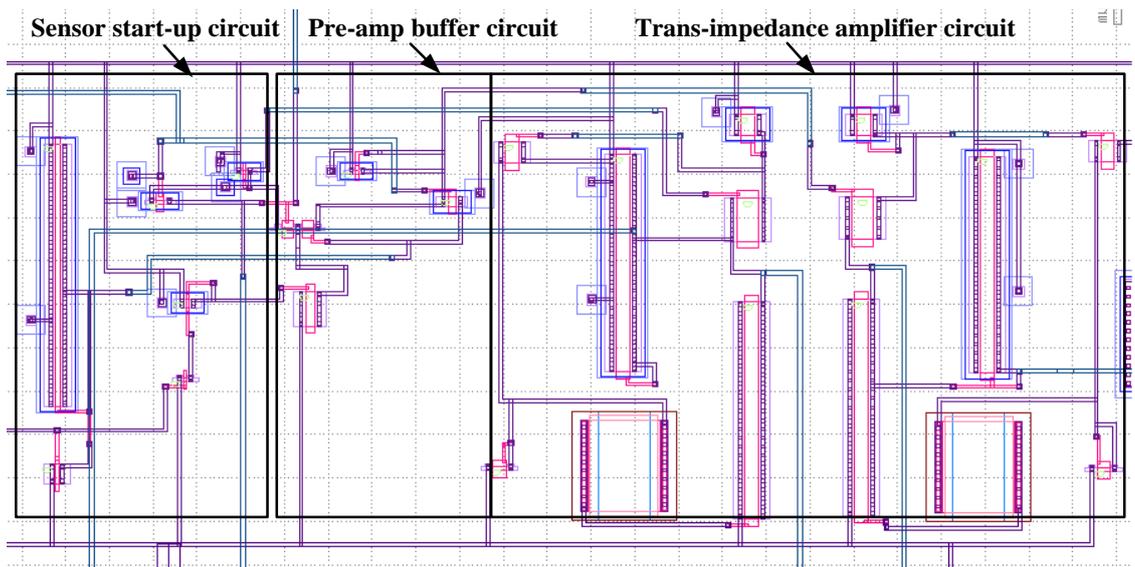


Fig. 4.17: Layout design of sensor start-up, pre-amp buffer and trans-impedance amplifier

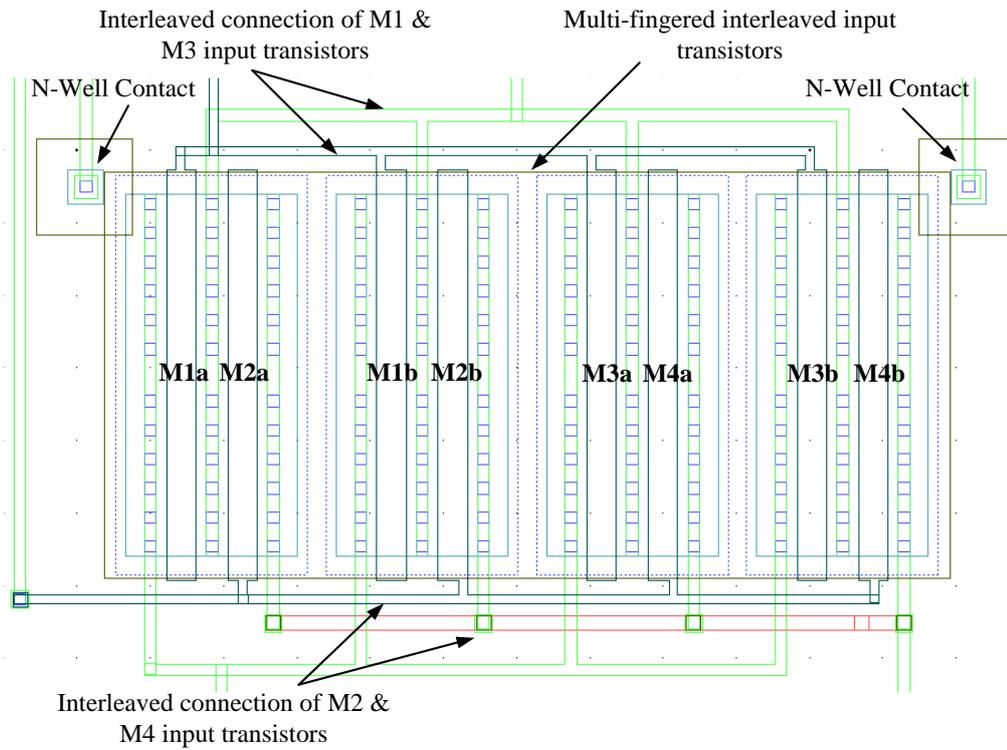


Fig. 4.18: Input transistors layout design

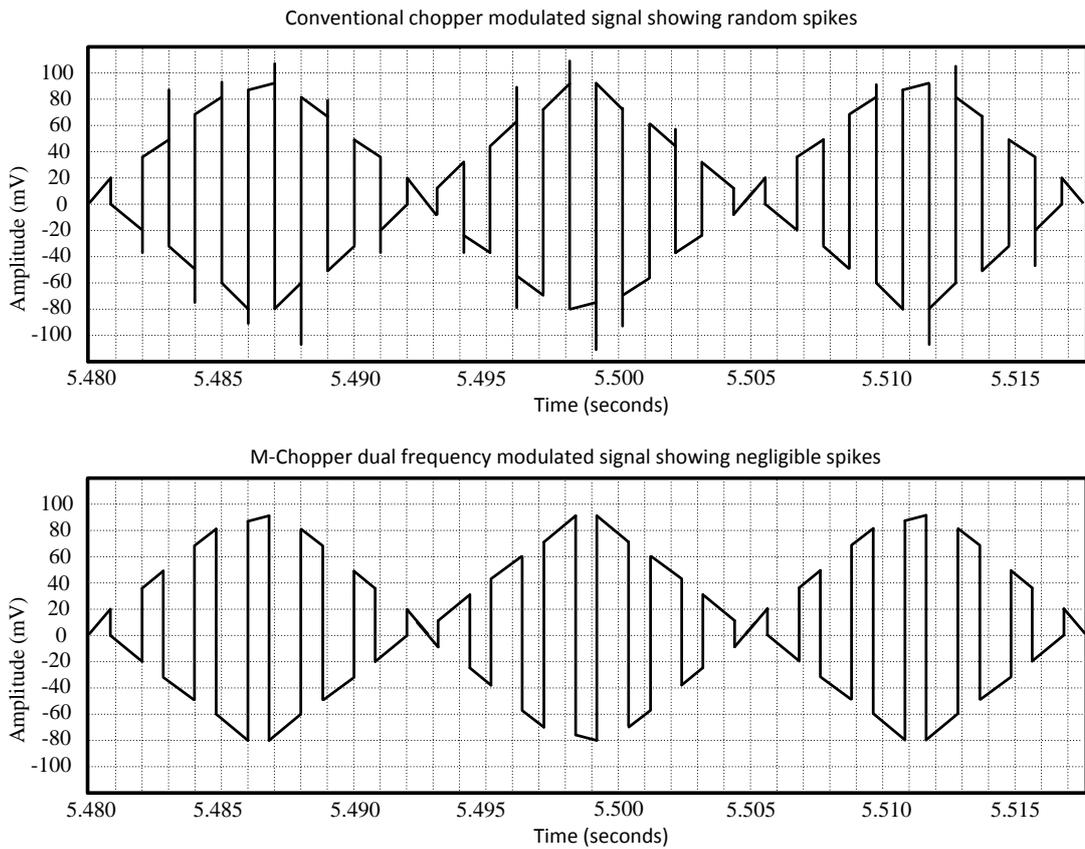


Fig. 4.19: Comparison of chopper outputs

Table 4.1:
Aspect ratios of M-chopper
FC opamp Stage

| Device | Size |
|-------------|--|
| M1,M2,M3,M4 | $\frac{10 \mu\text{m}}{0.2 \mu\text{m}}$ |
| M5,M6 | $\frac{3 \mu\text{m}}{0.6 \mu\text{m}}$ |
| M7,M8 | $\frac{3.5 \mu\text{m}}{0.6 \mu\text{m}}$ |
| M9,M10 | $\frac{2.5 \mu\text{m}}{0.6 \mu\text{m}}$ |
| M11,M12 | $\frac{4.1 \mu\text{m}}{0.6 \mu\text{m}}$ |
| M13,M14 | $\frac{60 \mu\text{m}}{0.6 \mu\text{m}}$ |
| M15,M16 | $\frac{0.2 \mu\text{m}}{0.6 \mu\text{m}}$ |
| M17,M18 | $\frac{22 \mu\text{m}}{0.6 \mu\text{m}}$ |
| M19,M20 | $\frac{5.55 \mu\text{m}}{0.2 \mu\text{m}}$ |
| M21,M23 | $\frac{80 \mu\text{m}}{0.6 \mu\text{m}}$ |
| M22,M24 | $\frac{4.6 \mu\text{m}}{0.2 \mu\text{m}}$ |
| M25 | $\frac{20 \mu\text{m}}{0.6 \mu\text{m}}$ |
| M26 | $\frac{15 \mu\text{m}}{0.6 \mu\text{m}}$ |
| M27,M28 | $\frac{11 \mu\text{m}}{0.18 \mu\text{m}}$ |
| Cc1,Cc2 | 0.25pF |

Table 4.2:
Aspect ratios of trans-impedance stage,
pre-amp & CMFB

| Device | Size |
|----------------------------|---|
| M29,M30 | $\frac{0.2 \mu\text{m}}{0.5 \mu\text{m}}$ |
| M31,M32 | $\frac{0.22 \mu\text{m}}{0.18 \mu\text{m}}$ |
| M33,M34 | $\frac{0.16 \mu\text{m}}{0.5 \mu\text{m}}$ |
| M35,M36 | $\frac{0.26 \mu\text{m}}{0.18 \mu\text{m}}$ |
| M37,M38 | $\frac{1.6 \mu\text{m}}{0.4 \mu\text{m}}$ |
| M39 | $\frac{0.17 \mu\text{m}}{0.5 \mu\text{m}}$ |
| M40 | $\frac{0.5 \mu\text{m}}{0.35 \mu\text{m}}$ |
| M41,M42 | $\frac{2 \mu\text{m}}{1 \mu\text{m}}$ |
| M43,M44 | $\frac{1 \mu\text{m}}{0.6 \mu\text{m}}$ |
| M45,M46, M47,M48 | $\frac{10 \mu\text{m}}{0.6 \mu\text{m}}$ |
| M49,M51,M53 M54,M55,M56 | $\frac{0.22 \mu\text{m}}{0.18 \mu\text{m}}$ |
| M50,M52 | $\frac{0.22 \mu\text{m}}{0.2 \mu\text{m}}$ |

The noise analysis for the proposed FC opamp revealed that a low harmonic distortion (THD) of -64.5dB was obtained with a 1 KHz sinusoidal input, as shown in fig. 4.21. This is an order of magnitude less when compared to the conventional FC opamp. Flicker and thermal noise which is a primary concern in this design was also found to be very low as shown in fig. 4.22. Table 4.1 shows the aspect ratios of the designed FC opamp stage, whereas table 4.2 lists the device sizes of the trans-impedance stage, Pre-amp and Common mode feedback (CMFB) circuits. Transistor design ratios for the sensor biasing and the start-up circuits are given in table 4.3. Biasing circuit that was critical to achieve the desired gain for the proposed FC opamp had the device sizes listed in table 4.4.

Table 4.3:
Aspect ratios of sensor
bias and start-up circuit

| Devices | Size |
|----------|---|
| M69 | $\frac{0.2 \mu\text{m}}{0.19 \mu\text{m}}$ |
| M70 | $\frac{1.35 \mu\text{m}}{0.18 \mu\text{m}}$ |
| M71 | $\frac{0.25 \mu\text{m}}{0.18 \mu\text{m}}$ |
| M72 | $\frac{0.25 \mu\text{m}}{0.18 \mu\text{m}}$ |
| M73, M74 | $\frac{0.26 \mu\text{m}}{0.18 \mu\text{m}}$ |
| M75, T76 | $\frac{0.28 \mu\text{m}}{0.18 \mu\text{m}}$ |
| T77 | $\frac{0.24 \mu\text{m}}{0.18 \mu\text{m}}$ |
| R2 | $\frac{32 \mu\text{m}}{40 \mu\text{m}}$ |

Table 4.4:
Aspect ratios of FC Opamp
biasing network

| Devices | Size |
|---------------------------------|---|
| M57, M58, M60, M63, M67, M62 | $\frac{0.2 \mu\text{m}}{0.19 \mu\text{m}}$ |
| M59 | $\frac{0.36 \mu\text{m}}{0.19 \mu\text{m}}$ |
| M61 | $\frac{0.18 \mu\text{m}}{0.19 \mu\text{m}}$ |
| M64 | $\frac{10 \mu\text{m}}{0.18 \mu\text{m}}$ |
| M65 | $\frac{0.17 \mu\text{m}}{0.2 \mu\text{m}}$ |
| M66 | $\frac{16 \mu\text{m}}{0.19 \mu\text{m}}$ |
| M68 | $\frac{19 \mu\text{m}}{0.19 \mu\text{m}}$ |
| R1 | $\frac{3.2 \mu\text{m}}{24.28 \mu\text{m}}$ |

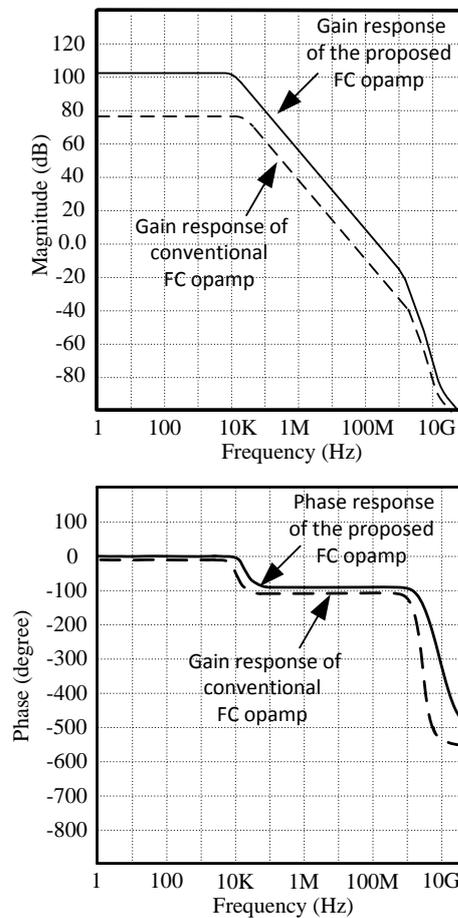


Fig. 4.20: AC Analysis of Modified chopper stabilized FC opamp & conventional two stage FC opamp

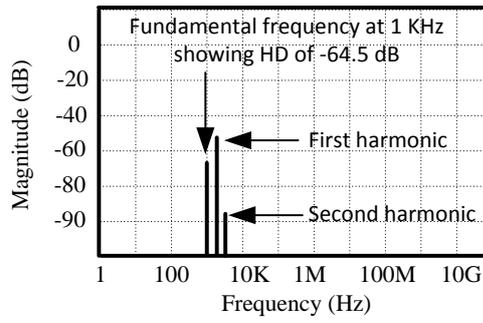


Fig. 4.21: Harmonic distortion of M-chopper stabilized FC opamp

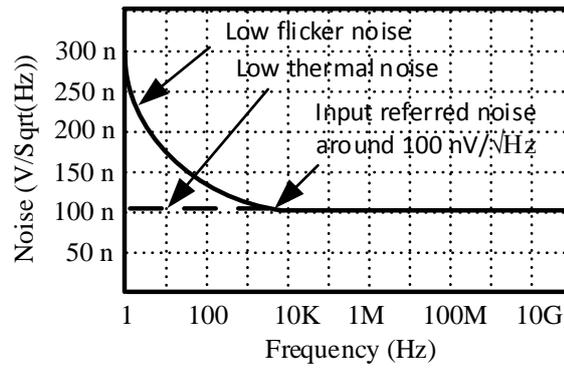


Fig. 4.22: Noise in the proposed FC opamp

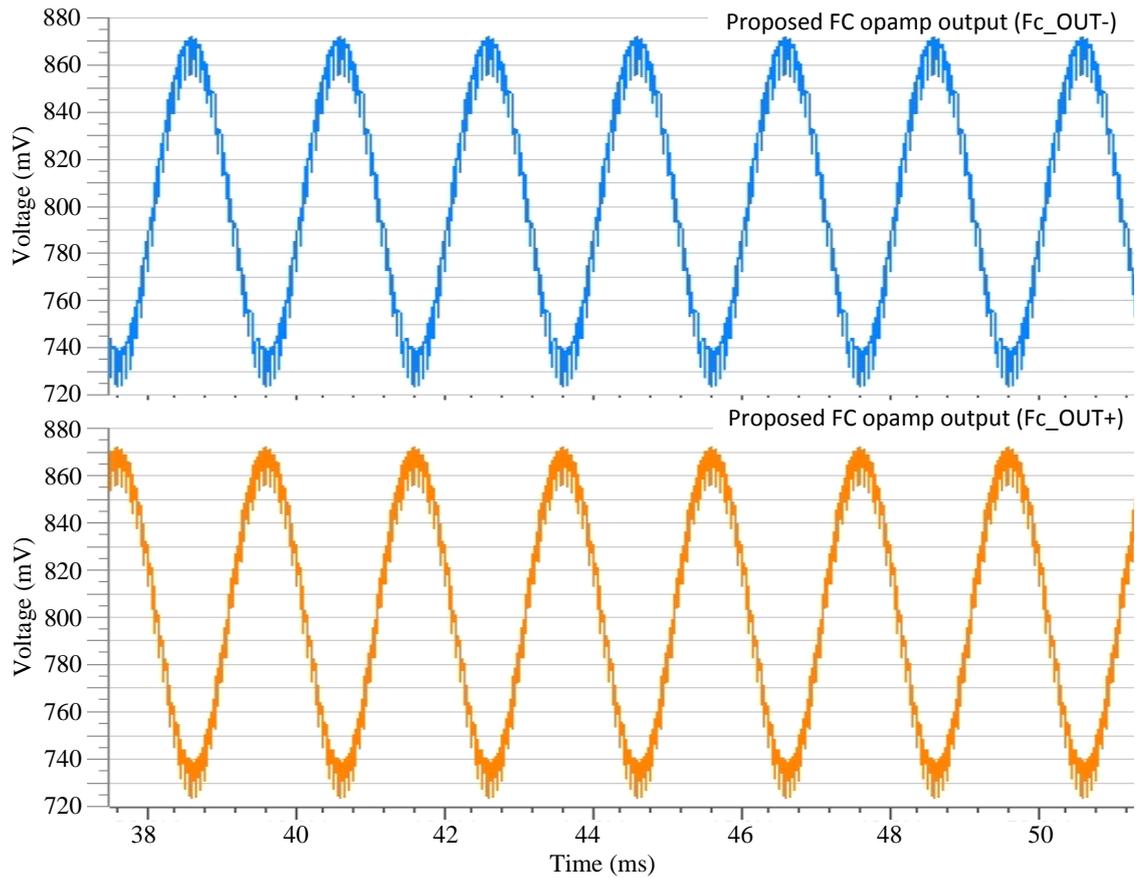


Fig. 4.23: Single ended transient responses of proposed FC opamp

Table 4.5: Features of proposed FC opamp

| Parameters | Achieved Value |
|----------------------|----------------------------|
| Technology | TSMC 180 nm CMOS |
| Closed loop Gain | 105 dB |
| Unity Gain Bandwidth | 200 MHz |
| Power Supply | 1.4 V |
| Settling Time | 4.6 ns |
| Input Referred Noise | 100 nV/ $\sqrt{\text{Hz}}$ |
| Power Consumption | 125 μW |
| THD | < 1% (-64.5 dB) |
| Output Voltage Swing | 0.6 V |
| Phase Margin | 64° |

4.4 Conclusion

A high gain sensor readout frontend is designed for viable pick-off of the weak sensor signal. The performance such as low noise and better stability of the designed amplifier ensures good repeatability and sensitivity of the sensor system. The trans-impedance stage provided a balanced single ended to differential conversion with an initial boosting of the weak sensor output. Pre-amp buffer on the other hand, yielded low gain error making further processing effective. Moreover, the low gain error of the pre-amp buffer made interfacing between pre-conditioning circuit and FC opamp feasible. The sensor start-up circuit eliminated the stray charges which otherwise would have degraded the system performance, thus contributing to the precision and accuracy of signal pick-up. The entire initial conditioning process made it feasible for the FC opamp to efficiently amplify with low noise floor. The achieved features of the proposed FC opamp are listed in table 4.5. Eventhough the opamp utilizes modified chopper stabilization for noise immunity; the chopping frequency residuals are found to be present at the output even after demodulation. This is evident from the single ended response at both output nodes of the opamp as shown in fig. 4.23. Removal of the chopper residuals is necessary for better sensitivity; therefore a low pass filter with the cutoff frequency lower than the chopper residual frequency must be designed.

Chapter 5

SiGeMEMS Sensor Readout Output Stage

5.1 Introduction to output stage

Typical sensor readout must have the capability to drive a peripheral component like an actuator or a display. The low impedance external circuit can heavily load the amplifier stages (if it was designed to be the final stage) and could seriously pull down the gain level causing degradation to sensor CMOS circuit performance. Hence most output stages of the signal conditioning circuit will consist of high input impedance and low output impedance buffer for better isolation. The proposed FC opamp is found to have moderate output impedance as it is designed to yield a very high differential gain of 105 dB. This moderate increase in the output impedance of the amplifier makes it vital to include a low output impedance stage, for improving the driving capability. Highly linear low output impedance CMOS circuit that has better impedance matching with the FC opamp is required to be as the sensor readout output stage. Prior to this output buffer stage, a filter circuit that can efficiently remove the entire chopper residuals of the FC opamp output is crucial. On the other hand, increased gain attenuation in the pass band of the filter stage may lead to the degradation of the overall efficiency of the sensor system. Therefore much consideration must be given in the filter design to reduce the gain attenuation.

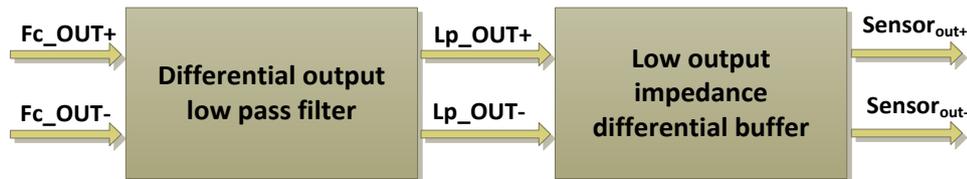


Fig. 5.1: Block diagram of sensor readout output stage

The block diagram of the SiGeMEMS sensor readout output stage is shown in fig. 5.1 above. It is preferable to implement a fully differential type of low pass filter and output buffer stage to exploit the inherent noise immune ability throughout the signal conditioning circuit. Moreover the common mode error in the differential CMOS circuits will be completely eliminated by means of differential signal cancellation. Thus at the final output of the sensor readout ($Sensor_{out}$), the overall common mode error is significantly reduced. As a result the sensor signal conditioner will have high overall common mode rejection ratio (CMRR) and better power supply rejection ratio (PSRR). In addition, the low supply fully differential design will increase the overall signal to noise ratio, as the composite signal swing doubles with the

same amount of power consumption as that of single ended. Further, increased headroom with the same amount of supply voltage lowers distortion; this in turn contributes to lowering the overall noise floor.

5.2 Introduction to low pass filter

Two methods of filtering technique are widely used in most of the applications, switched capacitor filter (SC) and continuous time filter (CT). The former has the advantage of accurate corner frequency; however, it has issues such as aliasing, trade-off in choosing sample rate, effects of sample and hold circuit and noise [82]. These issues have led to the design complexity of SC filters. Moreover, the requirement of large sized devices for efficient filtering has led to an increase in the die area, making it bulky for a sub-micron CMOS technology. Further increased aspect ratios yielded increased power consumption causing it to be unsuitable for low power sensor readout application. The CT filters, even though suffers from inaccurate corner frequency they can be designed for a wider dynamic range with no aliasing issues. In addition, it has the advantage of unnecessary anti-aliasing circuits that can increase the power dissipation. The possibility of achieving a better roll off in CT filters is much simpler, even with a low order design. Thus CT filters become a promising choice as a residual remover by meeting the above mentioned critical requirements.

Gm-C filter is one of the popular continuous time filters widely used in both high frequency (that ranges up to 2GHz) and low frequency applications (starting from sub-Hertz range of 0.1 Hz). This analogue transconductance-capacitance (Gm-C) filter does not have any local feedback and hence provides very good frequency response catering to stable filtering. The flexibility of frequency tuning of this filter by means of constant current DC biasing, makes it appropriate for sensor readout application. As the transconductance (g_m) cell in this Gm-C filter, greatly influences its performance, a suitable design to increase the cell linearity will yield a considerable improvement in the overall linear range. Owing to its many advantages, applications such as WiMax, hand held devices, sensor readout circuit, bio-medical signal conditioning, seismic and other wireless communications employ this filter design [83]-[86]. One of the major challenges in designing the Gm-C filter in deep submicron CMOS technology is the short channel effects [83], [84]. This second order effect can cause serious non-linearity; therefore methods need to be put in place to achieve better linearity. Moreover, supply voltage variation due to loading effect and thermal drift causes a shift in cut-off frequency. Even though Gm-C filters are preferred for their ease of full integration and effective on-chip filtering capability; their power dissipation is high when compared to other CT filters. Previously reported works have suggested techniques such as lowering of supply voltage and minimally sized transistors to reduce power dissipation; however, they are inadequate for high sensitive

sensor readout application. Moreover, for the utilized technology, the performance of the sensor system will be degraded if these techniques are employed. Further, most of the reported filter designs that use operational transconductance amplifier provided only a maximum of 400 mV output voltage swing due to the increase in overdrive voltage of the transistors; hence supply voltage reduction is unsuitable. The output voltage of the designed high gain FC opamp will also be clipped at the filter output stage with the reduction in supply voltage, leading to poor sensitivity of the sensor system. Considering the above issues, a lower order filter configuration with an improved transconductance cell that overcomes the trade-off is proposed. A 4th order low voltage filter that overcomes the on-chip design limitations with low noise is designed and analyzed.

5.3 Design of transconductance (OTA) cell

In most of the Gm-C filter design gain attenuation is a critical aspect. The transconductance of the operational transconductance amplifier (OTA) must be designed accordingly such that the gain yielded by the preceding stage must not be lowered [85]. Hence to preserve the gain enhancement achieved by the FC opamp, transconductance cell of the filter must have low or negligible gain error. To accomplish such precise gain preservation in the filter stage, it is important to maintain a proper biasing current for the OTA; therefore much importance is given to design a stable constant current biasing network. The biasing current will largely contribute to the g_m improvement of the transconductance cell. Generally, for the purpose of a better roll-off, the filter's order is largely increased. The large increase in the order count leads to an invariable increase in the number of OTA cells. This makes the design of a proper biasing network stage for each cell more tedious, but of extreme importance, as all the transistors must be kept in saturation to avoid distortion due to non-linear region of operation. This can contribute to minimizing the large amounts of gain error. There is a trade-off between biasing current and the output voltage swing; as the biasing current for the current sources is chosen appropriately to achieve better I_D for the purpose of g_m enhancement, overdrive voltage also increases. This is evident in the following equations [20]:

$$I_D = \frac{1}{2} k \frac{W}{L} (V_{GS} - V_{TH})^2 = \frac{1}{2} k \frac{W}{L} V_{OD}^2 \quad (5.1)$$

$$g_m = \frac{2I_D}{V_{OD}} \quad (5.2)$$

$$g_m = \sqrt{2k \frac{W}{L} I_D} \quad (5.3)$$

where $k = \mu_n C_{ox}$. In equation (5.1), it can be noted that increasing I_D causes an increase in the overdrive voltage by the square of some fraction. This fractional increase in the overdrive voltage will lead to a significant decrease in transconductance as apparent in equation (5.2); as a result the effective increase in transconductance is lessened. Considering the square law relation of the transconductance and the drain current in equation (5.3), a greater amount of increase in I_D is necessary to achieve better transconductance despite the trade off. Moreover, the output voltage swing substantially reduces due to an increase in the overdrive voltage. A two stage fully differential OTA is designed in this work to achieve a better g_m and a large output voltage swing of around 600 mV. Furthermore, in this deep submicron technology, to lower the second order effects, the aspect ratio of the transistors is designed appropriately. The design of OTA with common mode feedback circuit is shown in fig. 5.2 [83].

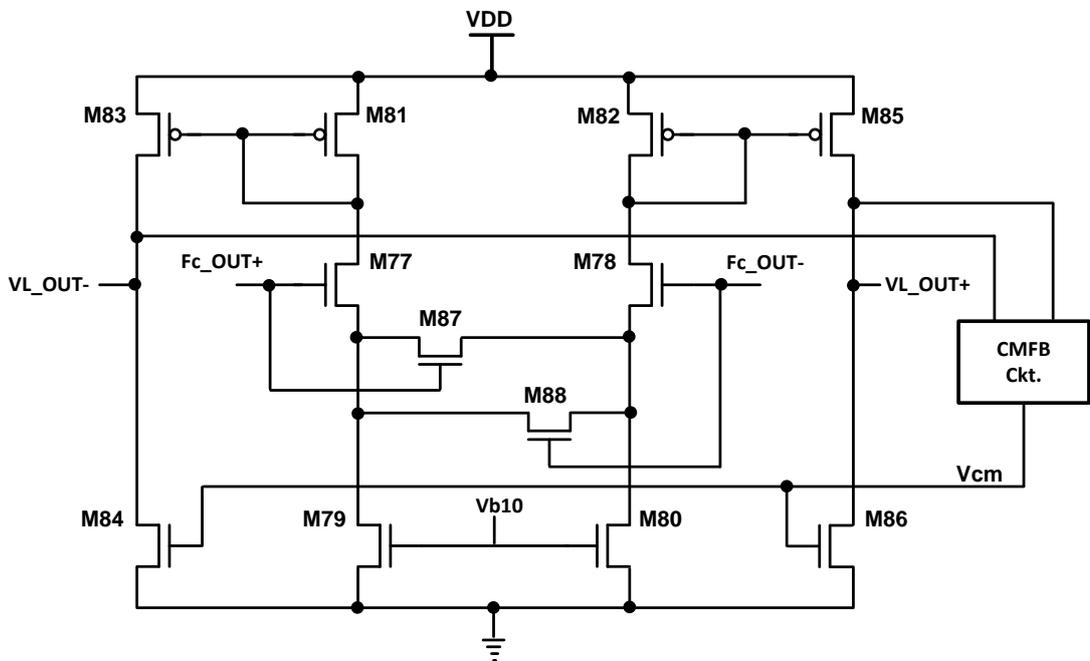


Fig. 5.2: Transconductance cell schematic [83]

Transistors M77 to M82 form the fully differential first stage of the OTA, M77 and M78 are the input transistors that have diode connected loads M81 and M82. The two critical aspects of the output stage of the sensor readout are addressed at this stage of the design. Firstly, the alternative use of cascode load can increase the small signal resistance of the current mirror yielding high output impedance. Eventhough this technique can lead to reduced gain error, stacking of transistors at this stage will occupy more headroom. The reduced headroom in this first stage causes distortion, further, increased overdrive due to cascode connection will contribute to low output voltage swing. Thus diode connected load is employed to minimize the

transistor numbers in the first stage, thereby reducing distortion. Secondly, in addition to the reduced number of load transistors their aspect ratios were also lowered, which resulted in significant reduction of noise floor and power dissipation. Transistors M87 and M88 are operated in the triode region to provide active degeneration for linearity improvement. The linear range of the OTA depends on the input ranges for which these transistors remain in the triode region; hence proper W/L ratio (aspect relation) between these transistors and the input pairs should be maintained. This active degeneration with better biasing has catered for bandwidth improvement of the filter. Transistors M79 and M80 are the differential current sink that stabilize the tail currents of this stage. These devices set the minimum level of voltage (V_{min}) above which the current will be constant. The larger value of W/L ratios for M79 and M80 greatly improved the levels of V_{min} . A precise constant current bias circuit was also designed for biasing these transistors to achieve the desired V_{min} . The output impedance of the output swing compensated single stage amplifier is found to be low; hence the gain will also be low, causing attenuation. This eventually leads to the gain error in the filter network.

In order to overcome the negative gain caused by the first stage, a second stage consisting of simple common source amplifier is included in this design. Transistors M83 to M86 form the high output swing stage that can grant proper gain error compensation. Transistors M87 and M88 operate in the sub threshold region to form source degeneration for the input stage. The active degenerated pairs provide linearity for the desired cut-off frequencies. The aspect ratios of these transistors are also kept low for effective area minimization; moreover, biasing these transistors in triode region renders low power consumption. The employed degenerative pairs can possibly reduce the loop gain; hence the tail transistors W/L ratios have to be made larger to maintain the same loop gain. To provide further compensation for the gain error, output impedance of the OTA cell must be increased without lowering the output swing. A suitable method that can significantly increase the output impedance without introducing dominant poles is to equip the transconductance cell with a negative resistance load. Thus the design consisting of a transconductance with the negative feedback resistor will resemble an integrator [86]. The equivalent circuit for a single stage OTA cell with a negative resistance is shown in fig. 5.3 below. The transfer function analysis proved that the output impedance improved significantly and this is evident from the equation below:

$$\frac{VL_OUT_{diff}}{Fc_OUT_{diff}} = \frac{g_m r_{out} R_{Load}}{r_{out} R_{Load} s C_{out} + R_{Load} - r_{out}} \quad (5.4)$$

where VL_OUT_{diff} is the differential output of the OTA and Fc_OUT_{diff} is the differential output of the FC opamp.

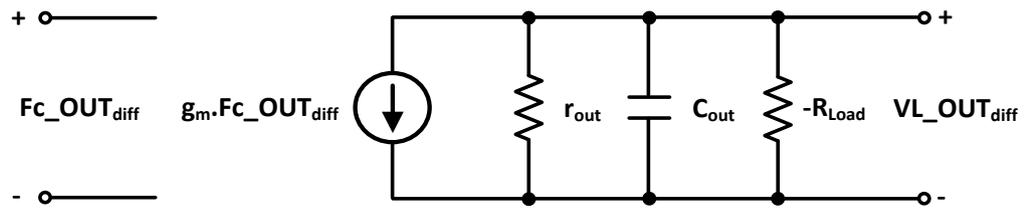


Fig. 5.3: Small signal model of single stage OTA with negative resistive load [86]

5.3.1 Common mode feedback

The fully differential amplifier's common mode voltage has to be stabilized by adjusting the common mode output current. For this reason the differential difference common mode feedback circuit designed for FC opamp is utilized here. Differential difference CMFB circuitry is preferred due to its continuous time mode feedback, as it caters for the accurate common mode level control [87]. Although DDA is linear only for a limited input range, the aspect ratio of the two interlaced differential pairs that sense the common mode difference are chosen appropriately to operate for larger voltage swing. The large gate source voltage of the current source keeps the CMFB loop linear for a larger differential signal, this can lead to better gain bandwidth product. All the transistors in the DDA CMFB circuit are operated in saturation to attain better DC loop gain for accomplishing a wide dynamic range. The DDA uses four identical PMOS transistors to average and compare the common mode voltage. A common mode voltage reference of 0.6 V is given to the gates of two of the PMOS transistors. The gates of the other two PMOS transistors receive the error voltage from the OTA output nodes, these four common mode sense transistors determine the amount of shift level required for correction. If there is a shift in the common mode level, the common mode voltage V_{cm} (this is the correction signal which is indicated in fig. 5.4, at the output of CMFB circuit) obtained from the source of the transistors indicates the correction level.

The tail currents for these four PMOS transistors are provided by the diode connected loads. These diode connected loads cut down the common mode gain reducing the control voltage drift, thus the non-linearity in this circuit is reduced significantly as compared to current mirror load employed CMFB. The common mode output voltage is feedback to the load transistors gates of OTA second stage. By controlling the level of V_{min} in the output stage, the output common mode level of the fully differential OTA cell is well controlled. DDA is found to have effectively cancelled the common mode signal in this design. Moreover suppression of the even order harmonics was also promising. The block diagram shown below describes the CMFB function in the OTA cell. The detail circuit diagram of DDA is shown earlier in Chapter 4.

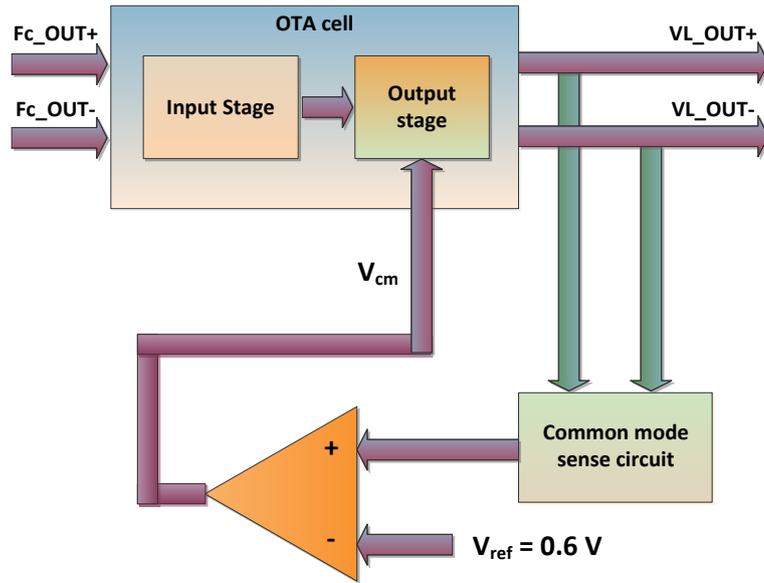


Fig. 5.4: Block diagram of common mode control

5.3.2 Supply independent bias circuit

The biasing circuit in fig. 5.5 is designed to bias the OTA cell and the CMFB circuits. The input double cascode structure design with large W/L ratios provides a stable reference current. This helps in effective scaling of other transistors in the bias network to obtain different bias options for the entire low pass filter circuitry. Reference current provided by the resistor R3 appears as a stable gate source voltage between gate and source of the diode connected transistor M89. The cascode connected PMOS transistors M89 and M91 further stabilizes this current. This is then copied to the drain of transistor M94 by means of NMOS cascode mirror copy circuits M93 to M96. The cautious design of W/L ratios results in copied current becoming a scaled factor of the reference current. As V_{bcm} biases the load transistors of CMFB circuit, proper shielding of the biasing current against output voltage variation and supply voltage fluctuation that can provide better linearity for the CMFB circuit is considered. Transistor pairs M90 and M92 actively shield transistors M94 and M96 from the output bias current drift due to output voltage variation. Any deviation in the designed drain current of M94 is suitably compensated by transistors M90 and M92, through inherent adjustments of their V_{DS} . Thus a stable constant bias current is provided to the CMFB that caters to lowering distortion. The obtained stable bias voltage V_{bcm} can then be given as:

$$V_{bcm} = V_{DS94} + V_{DS96} \quad (5.5)$$

The above equation can further be given in terms of the scaling factor of NMOS cascode pairs,

multiplied by the sum of the drain source voltage of parallel cascode pairs ($V_{DS93} + V_{DS95}$). The same cascode pair that sources the V_{bcm} bias circuit is also used for generating V_{ref} bias voltage, which is the common mode reference voltage for the CMFB Circuit. A stable 0.6 Volts of V_{ref} for the CMFB circuit that influences the rejection of OTA cell's common mode noise is achieved by proper scaling of transistors M97 to M100. Self biased cascode loads M97 and M98 are designed for achieving better headroom in order to attain large swing. Stacking of transistors is limited for V_{b10} bias voltage design as their limited swing can affect the output bias voltage leading to degraded performance of the OTA cell. One PMOS device M101 is utilized as the current source in this stage; however cascode NMOS pairs M102 and M'102 are still included in the design for achieving larger output resistance. Increased output impedance of this bias stage has substantially reduced the output bias current variation. This increase of output resistance at the drain of M102 is evident from the analysis of the output current given as:

$$I_{b10} = \frac{V_{b10}}{(g_{m102} \cdot r_{ds102}) r_{ds'102} // r_{ds101}} \quad (5.6)$$

where g_{m102} and r_{ds102} are the transconductance and output resistance of the M102, $r_{ds'102}$ and r_{ds101} are the output resistance of M'102 and M101 respectively. The supply independent network design of M91 to M94 provides better shielding for the bias voltage V_{b10} against power supply variation. The current at the cascode node of M91 and M93 and, the current at the node of M92 and M94 have a fixed relationship. This makes them proof against supply, process and to some extent temperature variation. The established positive feedback in this loop provides better loop gain that avoids the use of an increased number of transistors and/or high aspect ratio transistor, to achieve the desired bias voltage. Eventhough the possibility of over-damping in this feedback has a high probability of introducing instability; proper design of negative resistance can significantly improve the stability. The stability criterion for the proposed bias circuit can be given from [88] as:

$$n \left(\frac{g'_{m94}}{g_{m91}} \right) < 1 \quad (5.7)$$

$$\text{where } g'_{m94} = \frac{g_{m94}}{1 + g_{m94} \cdot r_{ds91}} \quad (5.8)$$

g_{m94} and r_{ds91} are the transconductance of transistor M94 and the output resistance of transistor M91 respectively. This bias current will therefore keeps the tail current sink of the OTA cell at

saturation always and hence will maintain a stable constant pre-determined current value. A suitable V_{\min} is thus achieved, above which the distortion is almost negligible. The designed stable bias circuit will significantly improve the filter's robustness towards corner frequency drift caused due to temperature and power supply variations.

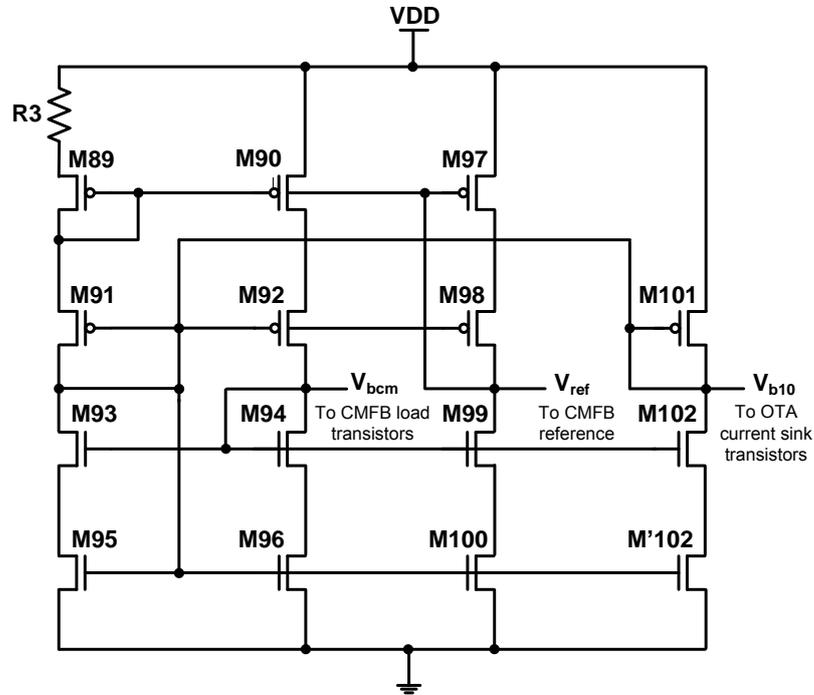


Fig. 5.5: Biasing circuit for OTA and CMFB circuits

5.4 Filter design

Initially, as in any standard filter design procedure; the transfer function and the order of the filter are first selected. This is a pertinent initial step for sensor's signal filtering design. Selectivity requirement such as pass band flatness and phase response characteristics will also play a major role in choosing the appropriate analogue filter. Increase in the order of filter can pose issues such as increased noise and power dissipation. Moreover, opting for a more feasible filter that can be realized with fewer components will significantly enhance the performance of the sensor system with low complexity. Generally analogue integrated filters can be synthesized either by cascade of active biquad structures or by passive prototype based LC ladder connections. For this sub-micron technology, as area and power dissipation is a major concern, integration of the serially connected LC ladder would be a poor choice. Inductors even with the smaller value will invariably increase the die area. Further to this, the passive components structure can substantially increase the power dissipation. In addition, LC ladder requires extra OTA for grounding the floating capacitor contributing to further increase in area and power.

Eventhough the biquad cascaded structure can introduce complex pole pair with the addition of another biquad structure [88], a lesser number of stages would be sufficient enough to achieve the desired selectivity requirement with low complexity. Furthermore, a convenient choice of transfer function for the filter approximation such as Butterworth, Chebyshev Elliptic (Cauer) and Bessel filter make biquad structures a better choice for filter synthesis. The transfer function of an ideal filter can be given as [86]:

$$H(s) = \frac{N(s)}{D(s)} = \frac{a_M s^M + a_{M-1} s^{M-1} + \dots + a_0}{b_N s^N + b_{N-1} s^{N-1} + \dots + b_0} = \frac{a_M (s - z_1)(s - z_2) \dots (s - z_M)}{b_N (s - p_1)(s - p_2) \dots (s - p_N)} \quad (5.9)$$

where a_{M-0} and b_{N-0} are the element values of the filter. These coefficients are of the type real numbers. The suffix of coefficient b shows the order count. The stability criteria for the filter states that N must be greater than M and all poles must lie in the left half plane of the S domain [89]. Considering the above transfer function and the criteria for an ideal filter, a suitable low pass filter structure that can effectively filter the chopper residuals with a flat pass-band and better roll-off is designed in this work. Elliptic (Cauer) filters are important in applications requiring a sharp magnitude response. They are widely employed in wireless communication due to their flat pass-band. The advantage of using this filter for sensor readout circuit arises from the fact that their ripples get divided equally in both pass-band and stop-band. A minimal error is introduced due to the equi-band ripples; this leads to low distortion and improved linearity unlike Chebyshev filters. The primary reason for the choice of elliptic filter is their minimal attenuation in pass-band unlike many other filters. The stop-band attenuation is always specified by a minimum value based on filter structure, thus guaranteeing that during the stop band the AC response will never increase past this value. For this application, the increased attenuation in stop band of the elliptic filter provides better removal of high frequency residuals that appears at the output of FC opamp when designed as a low pass filter. The steeper transition further improved the reliability of the filter.

5.4.1 Biquad structure

Biquad structures provide design flexibility when cascaded stages are employed; hence biquad structures with different Gm-C integrator topology are cascaded in this design [86], [87]. The custom designed OTA cell (discussed in section 5.3) which uses less die area and offers better linearity, is employed in this biquad structure for the Gm realization of the Gm-C integrator. An active Gm-C integrator cell consists of a transconductance circuitry and a capacitor. The transconductance circuitry converts the input voltage in to a current. DC gain enhancement is not necessary in this circuit; hence it is preferable not to include cascode current

mirror loads, which can substantially decrease both the input linear range and output voltage swing. Addition of a second stage can however boost the gain significantly to compensate for any gain error in the first stage. The output current of the transconductance stage appears as a voltage with a capacitor connected at its output. A proper design of the transconductance can significantly increase the performances of the Gm-C integrator such as transfer function, noise and linearity. A balanced differential Gm-C integrator is employed to further improve the performance of the biquad structures. The capacitors are kept floating in this Gm-C structure for effective reduction in the capacitance value. Grounded capacitors normally will have increased capacitance value leading to larger die area, especially when a MIM (metal-insulator-metal) capacitor type design is employed. To appropriately design the time constant of the circuit, the parasitic capacitance of this active transconductance circuit must also be considered. This parasitic capacitance C_p appears parallel to the capacitance C_x as shown in fig. 5.6; hence the capacitance value decreases for the desired time constant, thus as a complimentary benefit reduces the effective area of the sensor chip.

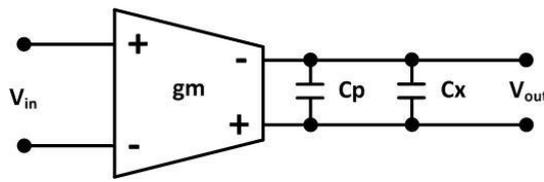


Fig. 5.6: Floating capacitor balanced differential integrator

The non-dominant pole of the lossless integrator shown in fig. 5.7 can significantly affect the roll-off of the filter, degrading the frequency response. A lossy integrator, with its transconductance designed suitably to keep the non-dominant pole at higher frequency beyond unity gain bandwidth is therefore preferred. The lossy integrator can be constructed by connecting an additional transconductance cell to the output of a lossless integrator; which means that the overall transconductance network can be built with negligible intermediate poles.

5.4.2 Filter topology

The topology of the 4th order elliptic Gm-C filter is shown in fig. 5.7. This higher order filter is constructed by cascading one second order biquad structure with two first order Gm-C integrator. The proposed biquad consisting of three transconductance cells G_{m1} , G_{m2} and G_{m3} with two capacitors $C1$ and $C2$, will yield a bi-quadratic transfer function that introduces one dominant pole and one non dominant pole. The dominant pole is set exactly at the desired 3db frequency, whereas the non dominant pole is pushed to the stop band. A transmission zero is introduced by feeding additional current generated by the G_{m3} transconductance cell. Thus a steeper roll-off is achieved even with the low order count [87], [88]. This biquad structure

consisting of three transconductance cells is preferred for its low power consumption, unlike the biquad in [84]. Two first order structures are cascaded in the later stages instead of an additional second order biquad stage, which further reduces the possibility of introducing intermediate poles. Moreover, area and power are also significantly reduced. Transconductance G_{m4} and G_{m5} form the second stage first order structure with a negative resistance load that improves the output impedance. The third stage is a lossless fully differential integrator, which will introduce a further 20dB/decade roll-off. The poles offered by these later stages are set to fall beyond their unity gain bandwidth by proper design of the transconductance. This avoids any inter-stage poles, which can degrade the frequency response of the filter. The Transfer function of the second order biquad Structure is given by:

$$H_2(s) = \frac{K\omega_o^2}{s^2 + \omega_o/Qs + \omega_o^2} \quad (5.10)$$

$$\text{Where, } K = \frac{G_{m1}}{G_{m3}} \quad (5.11)$$

$$\omega_o = \frac{\sqrt{G_{m3}G_{m2}}}{C_1C_2} \quad (5.12)$$

The quality factor of the biquad structure is given by:

$$Q = \sqrt{\frac{C_1}{C_2} G_{m3} G_{m2}} \quad (5.13)$$

The transfer function of the first order section with negative resistance is given by:

$$H_1(s) = \frac{G_{m4}r_{05}}{1 + sC_3r_{05}} \quad (5.14)$$

The transfer function of lossless Integrator is given by:

$$H_o(s) = \frac{G_{m6}}{sC_4} \quad (5.15)$$

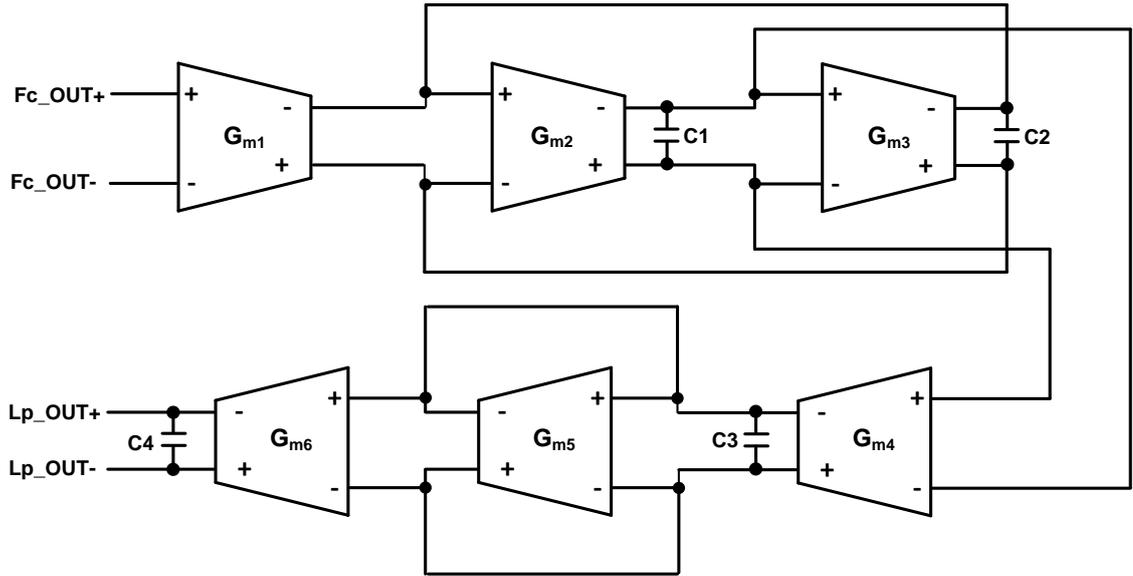


Fig. 5.7: Fourth order elliptic Filter topology

The general form of transfer function for the realized 4th order low pass elliptic filter is given as [89]:

$$H_4(s) = H_o \prod_{i=1}^2 \frac{s^2 + A_{oi}}{s^2 + B_{li}s + B_{oi}} \quad (5.16)$$

where the uppercase A and B represent the coefficients of normalized transfer function. Transconductance G_{m6} is varied to compensate for the attenuation caused by the previous stages, thus the cascaded stages have reduced the gain error drastically. Gm-C filter has excellent gain-bandwidth properties, therefore cascading these structures is quite simple and easy. Moreover, their advantages such as high speed and wide bandwidth are greatly exploited for the signal conditioning circuit [88]. In this design the passive elements are replaced by their active counterpart, which will give comparatively lower sensitivity to process and temperature variations [90].

5.4.3 Simulation result of low pass filter

Tanner tool V15.1[®] was used to design the filter in 180 nm CMOS technology. S-edit tool was used to design the schematic of the LPF. T-spice and W-edit were used for simulation and waveform analysis respectively. First the low pass filter is analysed with a sinusoidal input of 150 mV prior to interfacing with FC opamp. Making use of the advantage of fully differential

amplifier, the short channel effects and the common mode noise are substantially reduced. Furthermore, fully differential amplifier design has also suppressed the even order harmonics [90]-[92], thus lowering distortion which is critical for the 4th order filter design. The reduced parasitic effect offered by the sub-micron technology supported the elimination of undesired intermediate pole. In addition, due to the minimum line width of 180 nm CMOS technology, unaltered pole and zero locations are achieved. The minimum number of transconductance stage contributed to less number of integrator loop, this catered to better stability by reducing the effect of excess phase. All transistors were designed to remain in saturation except the degenerative ones in order to obtain a better linear range. The magnitude response in fig. 5.8 shows that the filter has a steeper roll-off of 80 dB/decade with negligible gain error for the utilized Gm-C topology. A cut-off frequency of around 11 KHz with the high linear phase response is obtained by appropriately designing the cascaded OTA. This is satisfactory for removal of chopper residuals present at the output of FC opamp. Even if the cut-off frequency is increased by altering the value of the capacitance, it was found that the filter's response is still linear up to GHz range. This is due to the high precision of the employed metal-insulator-metal capacitors offered by the CMOS technology. The power consumption for the 1.4 V supply is found to be as low as 1.4 mW. The complete filter design with the bias circuitry is analysed to have a total harmonic distortion (THD) of -60 dB for an input voltage of 150 mV. The two stage transconductance cell of the OTA with simple current loads yielded better differential output voltage swing of 600 mV peak to peak for the low supply voltage used.

Table 5.1: LPF simulation results

| Technology | 180 nm CMOS |
|----------------------------------|--------------------------------|
| Supply Voltage | 1.4 Volts |
| Filter type | 4 th Order Elliptic |
| Power Consumption | 1.4 mW |
| THD (@150mV) | -60 dB |
| Output voltage swing | 600 mV (P-P) |
| Current Consumption (static) | 0.7 mA |
| No. of Gm unit | 6 |
| Total On-chip Capacitance | 2.5 nF |
| Cut-off Frequency of the Filter | 11 KHz |
| Total no. of Transistors per OTA | 20 |

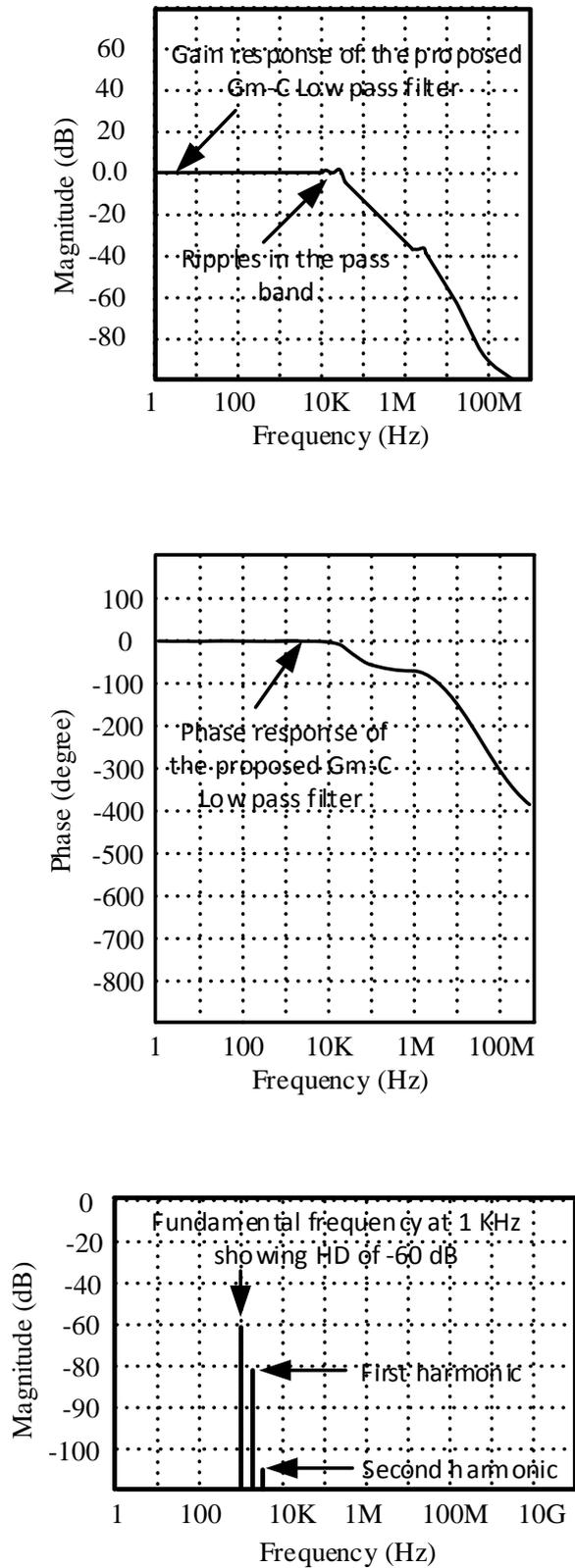


Fig. 5.8: AC response & harmonic distortion of LPF with separate excitation

Table 5.2: Aspect ratios of the Gm-C filter and component values

| Device | Size |
|-------------------|---|
| M77,M78 | $\frac{0.26\ \mu\text{m}}{0.2\ \mu\text{m}}$ |
| M79,M80 | $\frac{0.55\ \mu\text{m}}{0.2\ \mu\text{m}}$ |
| M81,M82 | $\frac{0.2\ \mu\text{m}}{0.25\ \mu\text{m}}$ |
| M83,M85 | $\frac{0.5\ \mu\text{m}}{0.2\ \mu\text{m}}$ |
| M84,M86 | $\frac{0.2\ \mu\text{m}}{0.25\ \mu\text{m}}$ |
| M87,M88 | $\frac{0.22\ \mu\text{m}}{0.18\ \mu\text{m}}$ |
| M89,M92 | $\frac{5\ \mu\text{m}}{0.7\ \mu\text{m}}$ |
| M90,M93 | $\frac{1\ \mu\text{m}}{0.6\ \mu\text{m}}$ |
| M91,M94, M'102 | $\frac{20\ \mu\text{m}}{0.6\ \mu\text{m}}$ |
| M95,M97 | $\frac{1\ \mu\text{m}}{0.6\ \mu\text{m}}$ |
| M98,M100 | $\frac{0.22\ \mu\text{m}}{0.6\ \mu\text{m}}$ |
| M99,M101, M102 | $\frac{10\ \mu\text{m}}{0.6\ \mu\text{m}}$ |
| R3 | 2.5K Ω |
| C1 | 1 nF |
| C2,C3,C4 | 0.5 nF |

The complete simulation results are listed in table 5.1 and the device aspect ratios designed for the first OTA cell with its bias circuitry are listed in table 5.2. The filter parameters for various reported filter designs are compared with the proposed design in table 5.3. It is evident from the table that this work has contributed a competent filter design with improved performances such as better roll off, large output voltage swing and minimum power consumption. For the low 1.4 V supply voltage, it was found that the designed OTA cell devices that have W/L ratios listed in table 5.2 can remain in saturation for a wider input range, resulting in a larger linear range of operation. Fig. 5.9 depicts the layout of the LPF designed using Tanner L-Edit tool.

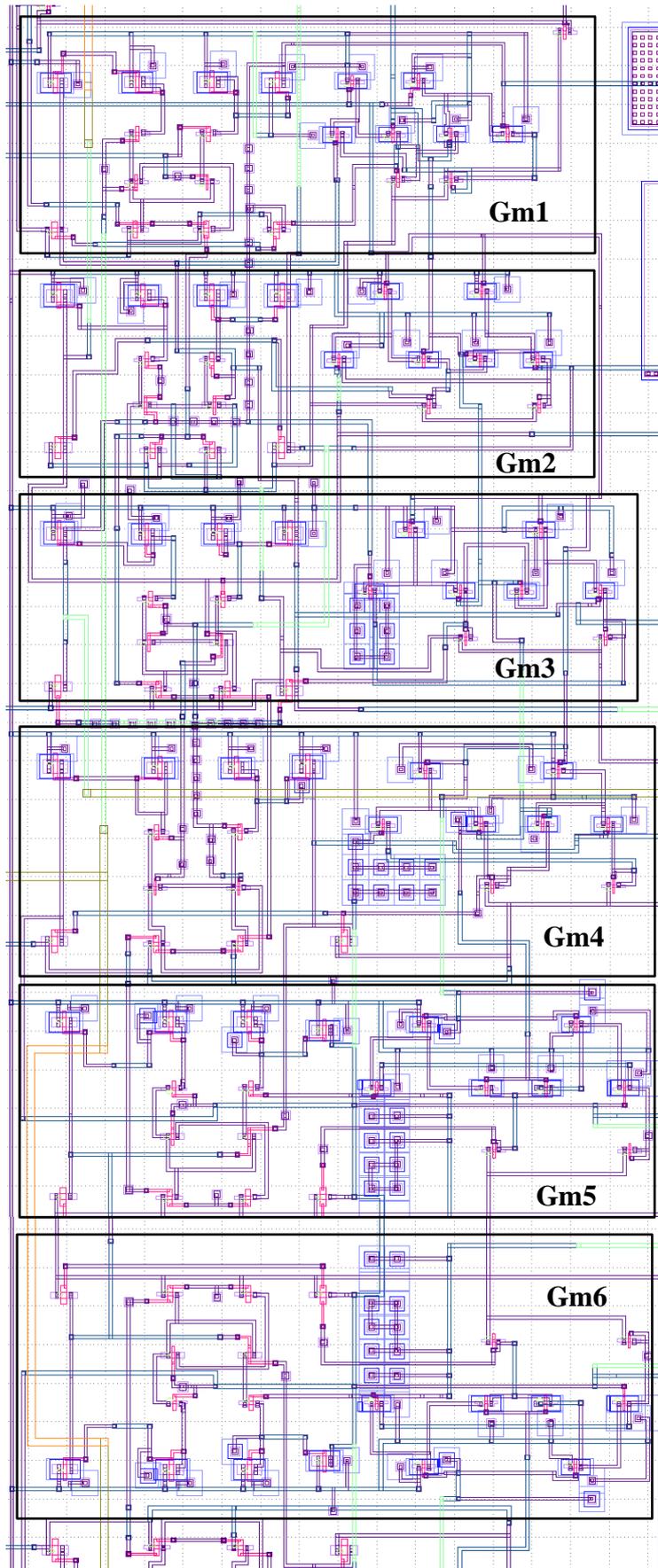


Fig. 5.9: Layout design of LPF Gm stages

Table 5.3: Comparison of different filter designs

| Ref. | Filter Parameters | | | | | |
|-----------|-------------------|----------------|--------------------------------|-------------------|------------------|----------------------|
| | Technology | Supply Voltage | Filter Type | Power Consumption | THD @150mV input | Output Voltage Swing |
| [84] | 180 nm TSMC CMOS | 1.8 V | 5 th Order FLF | 67 mW | -40 dB | 400 mV |
| [83] | 65 nm CMOS | 1.8 V | 5 th Order Bessel | 21.6 mW | -40 dB | 400 mV |
| [85] | 120 nm CMOS | 1.5 mV | 3 rd Order | 14.25 mW | -49 dB | 400 mV |
| [90] | 90 nm CMOS | 0.9 V | 5 th Order Elliptic | 1.5 mW | -66 dB | 300 mV |
| [91] | 180 nm CMOS | 1.8 V | 2 nd Order | 8.1 mW | -40 dB | 450 mV |
| [92] | 0.35 μ m CMOS | 1.0 V | 1 st Order | 005 nW | -40.3 dB | - |
| This Work | 180 nm TSMC CMOS | 1.4 V | 4 th Order Elliptic | 1.4 mW | -60 dB | 600 mV |

5.5 Self biased differential buffer

Generally, the sensor readout circuit is required to drive an off-chip analog-to-digital converter (ADC) for display or actuation purpose. The high output impedance of the transconductance stages within the low-pass filter (after the FC chopper amplifier) is not suited to drive these off-chip devices; hence the reason why a low output impedance buffer driver circuit that would not degrade the overall linearity would be required. In most applications buffered opamps are designed to improve both the linearity as well as the driving ability; however, high gain error makes it unsuitable for sensor system applications. Moreover, in this application where a filter intermediate stage is essential between the FC opamp and the external interface for high frequency removal, designing a FC opamp based buffer is irrelevant. Thus an output stage buffer that can drive a low output resistance and/or a large output capacitance is necessary. As depicted in the block diagram description in fig. 5.10, the output stage of the sensor readout must be able to drive an output resistance that is typically in the range of 10 Ω to 1000 Ω . Moreover the circuit must have a good ability to sink and source sufficient current.

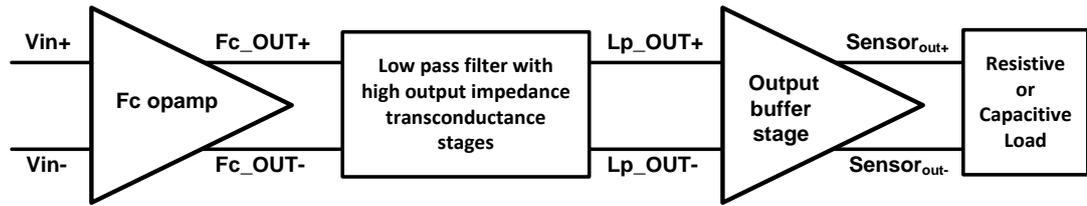


Fig. 5.10: Block diagram description of signal flow in sensor readout

Using a single ended operational amplifier, two types of buffer can be designed to achieve high linearity and low gain error. The first type which has an open loop configuration suffers from low efficiency, negative gain and limited output swing. Furthermore, there is a larger level shift between the input and the output. The other type uses negative shunt feedback forming a closed loop network and this is much preferred due to its reduced output resistance, which has increased ability to drive larger loads. The negative feedback can to some extent suppress the offset and noise, moreover increased stability is also achieved. A single ended closed loop buffered op-amp with negative feedback is shown in fig. 5.11 [93], [94], care must be taken in designing the op-amp to achieve gain closer to unity even with low resistive loads. The limited bandwidth provided by this type of filter is unsatisfactory for sensor readout applications. The output resistance is given by [94]:

$$R_{out} = \frac{R_o}{1 + A_{cv}} \quad (5.17)$$

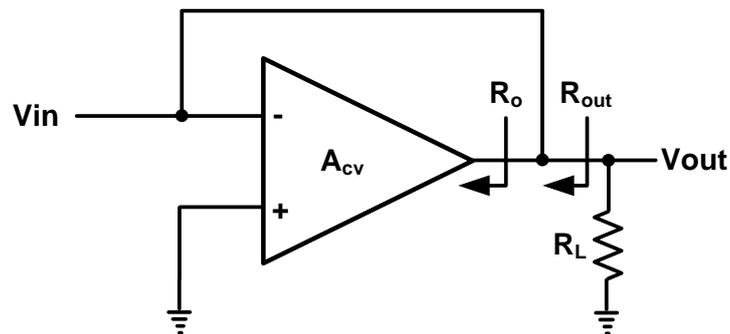


Fig. 5.11: Negative feedback in buffered opamp

where R_o is the output resistance of the open loop op-amp, R_{out} the output resistance of the closed loop op-amp and A_{cv} the closed loop gain. It can be noted from the equation in (5.17)

that increased load resistance will increase the total output resistance leading to decrease in the closed loop gain. Many closed loop operational amplifier based buffers that overcomes the above trade-off have been reported in recent years. Designs involving push-pull amplifiers and several cascaded stages pose more challenges in keeping the output resistance low. Even though these sophisticated buffers can drive even larger LED and LCD panels without much gain error, they have poor linearity and increased power dissipation. Moreover increased number of stages and nodes in these designs contribute too many poles and zeros making compensation more complicated. Thus complex buffers become unsuitable for sensor readout output stage implementation. Simple unity-gain buffers can be realized using source followers. Although the circuit implementation is straightforward, they are limited by non-zero offset and non-linearity. As discussed earlier, employing negative feedback can reduce the offset and non-linearity; however gate-to-source voltage drop of the source follower will still introduces offset [95]. Moreover the single stage circuit introduces high gain error. Two stage circuits with current feedback can be employed to significantly reduce the gain error and output impedance without the need for increased device aspect ratios. Further reduction in the overall area and power consumption can also be achieved.

5.5.1 Design of self biased buffer

Conventional differential source follower buffer with simple current load and sink requires input transistors with larger aspect ratios to minimize the voltage gain loss. It was found from the previous work that the transistors size must be doubled to achieve the desired transconductance. This leads to larger parasitic capacitance, thus the overall capacitance almost doubles causing the bandwidth to reduce by half than usual. Lowering of bandwidth at the output stage of the sensor readout is undesirable. Moreover an increased W/L ratio of transistors renders poor area utilization and larger power dissipation. Alternatively, certain differential flipped voltage follower design reported in [96] can provide better performance with low aspect ratios; however requirement of larger bias current still increases the power consumption. Current feedback loop through active devices was proposed in [97] to significantly increase the transconductance without the need for larger aspect ratios. This closed loop design is promising for an on-chip buffer implementation, but constant current bias network is needed for six transistors to achieve the desired transconductance. Increased power dissipation and the area are still a major concern. A self biased differential buffer is designed in this work to achieve the desired parameters such as minimum area, low power dissipation, increased transconductance, minimal gain loss and increased bandwidth. Considering the left half of the circuit, the enhancement of output transconductance can be explained. By enhancing the transconductance of M105 through the cascode current mirror feedback loop M107, M109, M110 and M105, the effective transconductance is increased. The cautious

design of the aspect ratios for the cascode current mirror will keep the desired effective output resistance low. Diode connected device M113 shares the current sink device M105 with the input transistor M103. The parallel connection of M103 and M113 helps to maintain an increased DC drain current through M105. Thus an effective reduction in the size of M105 which yields high transconductance is possible. Moreover, linearity of the buffer circuit is also effectively improved.

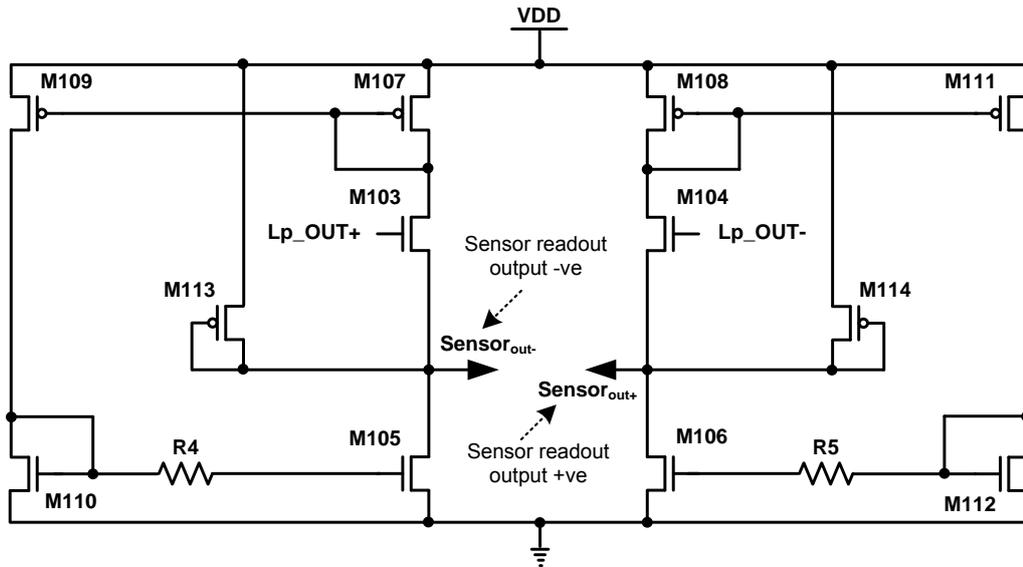


Fig. 5.12: Self biased differential buffer

5.5.2 Simulation results for self biased buffer

An on-chip buffer is designed using 180 nm TSMC CMOS technology to exploit the miniaturization feature similar to the sensor frontend and low pass filter designs. The schematic of fully self-biased differential source follower designed using S-Edit is shown in fig. 5.12. Larger voltage swing of 0.6 V for the 1.4 V supply was achieved. The response was linear for a wider bandwidth of up to 20 MHz with a 150 mV sinusoidal excitation. The simulation analysis showed that the circuit has the capability to drive the capacitive load up to 15 pF. The results of the simulation output are listed in table 5.4. Total current consumption with only DC biasing was found to be as low as 120 μ A. The static and dynamic power consumptions were also obtained as desired. The total harmonic distortion was less than 1%, which is critical for sensor readout output stage. The results obtained were satisfactory and hence the layout design is next carried out in L-Edit as shown in fig. 5.13. Area minimization being a primary concern was also very well achieved by utilizing the modern CMOS technology. The designed device sizes are listed in table 5.5.

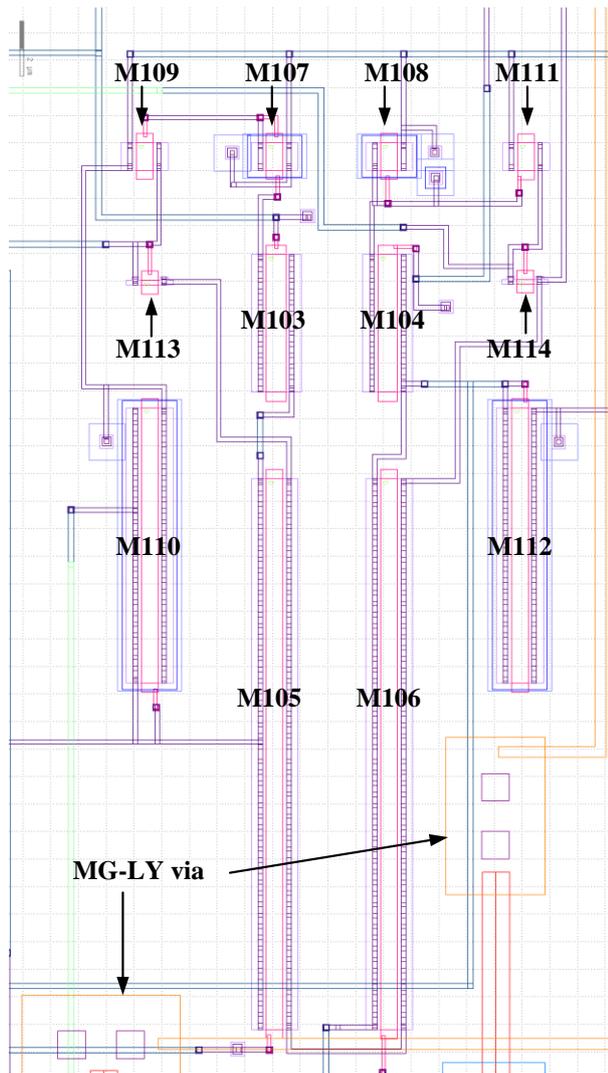


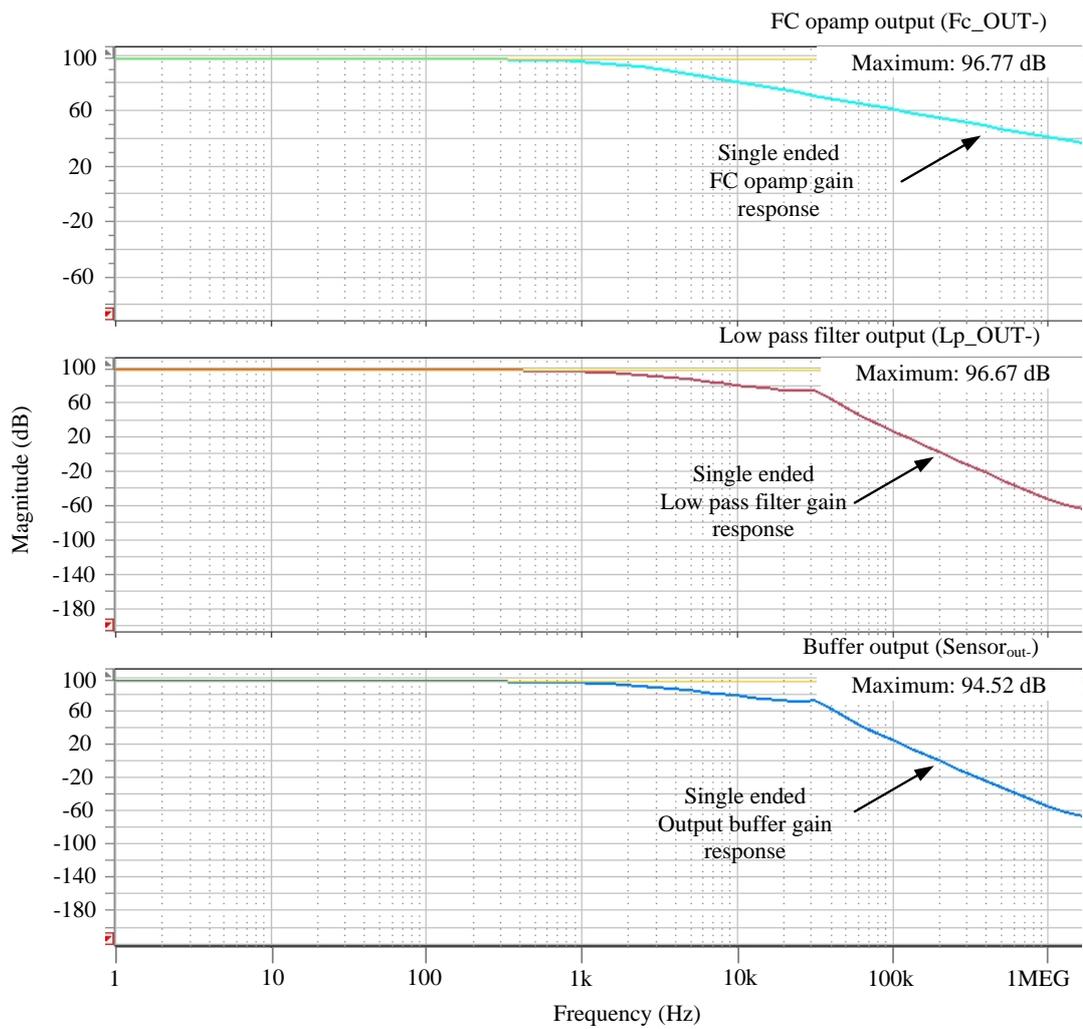
Fig. 5.13: Layout design of self biased differential buffer

Table 5.4: Simulation output of the buffer

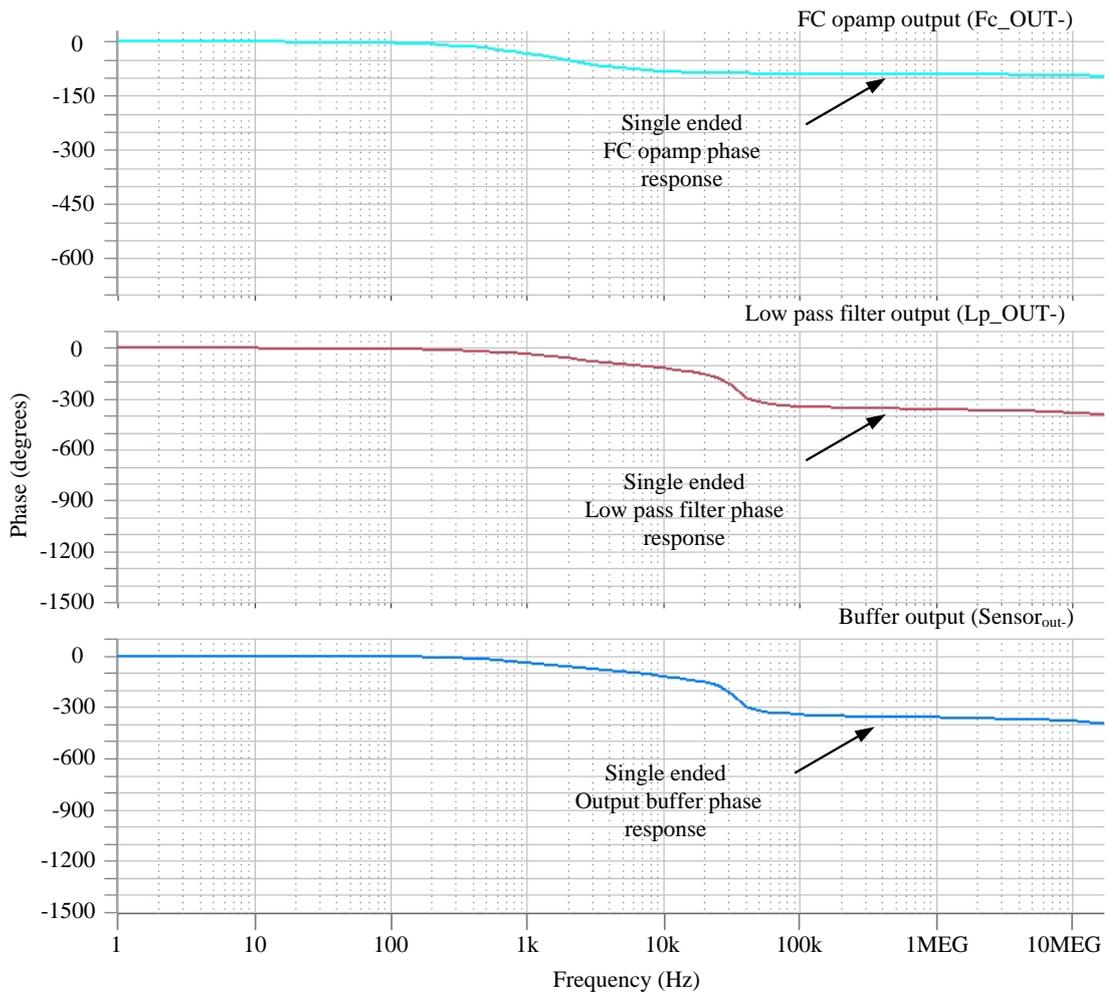
| Parameters | Value |
|---------------------------|--------------------|
| Process | 180 nm TSMC CMOS |
| Power Supply | 1.4 V |
| Total Current Consumption | 120 μ A |
| Static Power Consumption | 168 μ W |
| Dynamic Power Consumption | 180 μ W |
| Output Voltage Swing | 0.6 V |
| THD @500Hz input | < 1% (-60dB) |
| Output Noise@ 1KHz | 140 nV/ \sqrt Hz |
| Load (Capacitive) | Up to 15 pF |

Table 5.5: Aspect ratio of the buffer circuit and component values

| Devices | Size |
|---------------------------|---|
| M103, M104 | $\frac{5 \mu\text{m}}{0.7 \mu\text{m}}$ |
| M105, M106 | $\frac{20 \mu\text{m}}{0.6 \mu\text{m}}$ |
| M107, M108, M109, M111 | $\frac{1 \mu\text{m}}{0.6 \mu\text{m}}$ |
| M110, M12 | $\frac{0.2 \mu\text{m}}{0.6 \mu\text{m}}$ |
| M113, M114 | $\frac{10 \mu\text{m}}{0.6 \mu\text{m}}$ |
| R4, R5 | 1.5 K Ω |



(a)



(b)

Fig. 5.14: (a) Gain response of the sensor readout, (b) Phase response of the sensor readout

5.6 Result analysis for the integrated sensor readout

After the satisfactory result analysis of individual module, all the modules of sensor readout were interfaced together for overall analysis. A top level cell was created in the S-Edit tool of the Tanner tool v15.1[®] and the instance of each module was invoked and interfaced stage by stage according to the design. At this analysis stage, sensor bias and start-up circuitry were not invoked, as it was not feasible to properly analyse the signal swing with the random capacitive sensor signal. Since the FC opamp has a very high gain, sinusoidal excitation of around 10 μ V was provided to analyse the full output waveform. This avoids the possibility of waveform clipping in the intermediate stages due to the high gain of FC opamp. Four pulse waveform sources were used to modulate the input signal for chopper stabilization. Two of the square pulses were kept at a low frequency of 1 KHz with 90° out of phase. The other two were kept at higher frequencies of 10 KHz with 90° out of phase between them. This modified chopper stabilization has effectively reduced the spikes, which otherwise would have been larger at

the output of the transmission gate chopper demodulator. Exact same frequencies and phase were maintained for the demodulator chopper, for effective removal of chopper signals at the output of FC opamp. Outputs from the FC opamp, low pass filter and buffer were probed for transient and AC analysis. FC opamp provided the large output swing; however chopper residuals were still present as expected. The single ended AC analysis in fig. 5.14 (a) shows that there is a marginal decline in the gain of FC opamp and this may be due to the slight deviation in the output impedance with the interfacing of succeeding low pass filter stage. The magnitude response of the low pass filter shows some amount of ripples in the pass band; however, it exhibited better roll-off. Also no significant attenuation was noted. The buffer AC analysis plot also resembles the same magnitude response as that of the low pass filter except a -2 dB gain error was noticed. Linear phase responses were achieved at all stages of the sensor readout as shown in fig 5.14 (b). In fig. 5.15, it was noticed that the low pass filter had completely removed the chopper residuals and the low output impedance buffer performed the level shifting very well. The integrated sensor readout layout design carried out in L-Edit tool using 180 nm TSMC CMOS technology is shown in fig. 5.16.

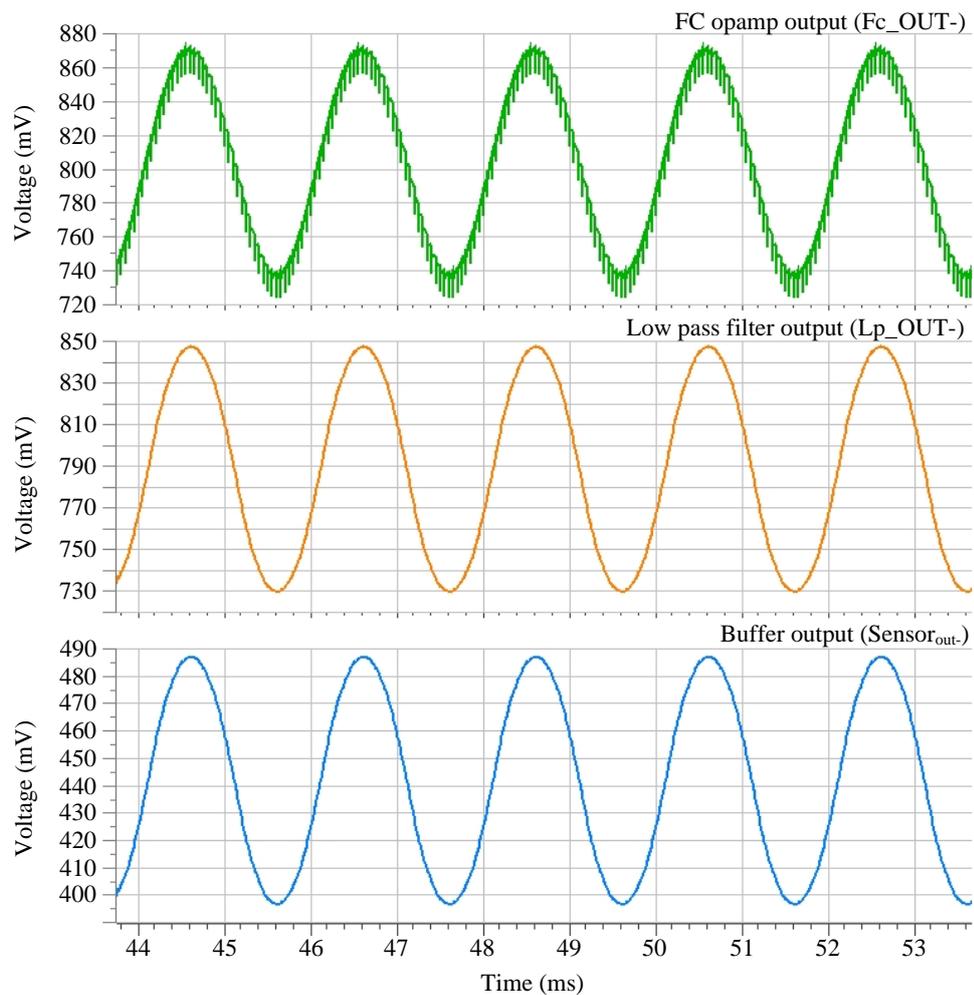


Fig. 5.15: Transient analysis of the sensor readout

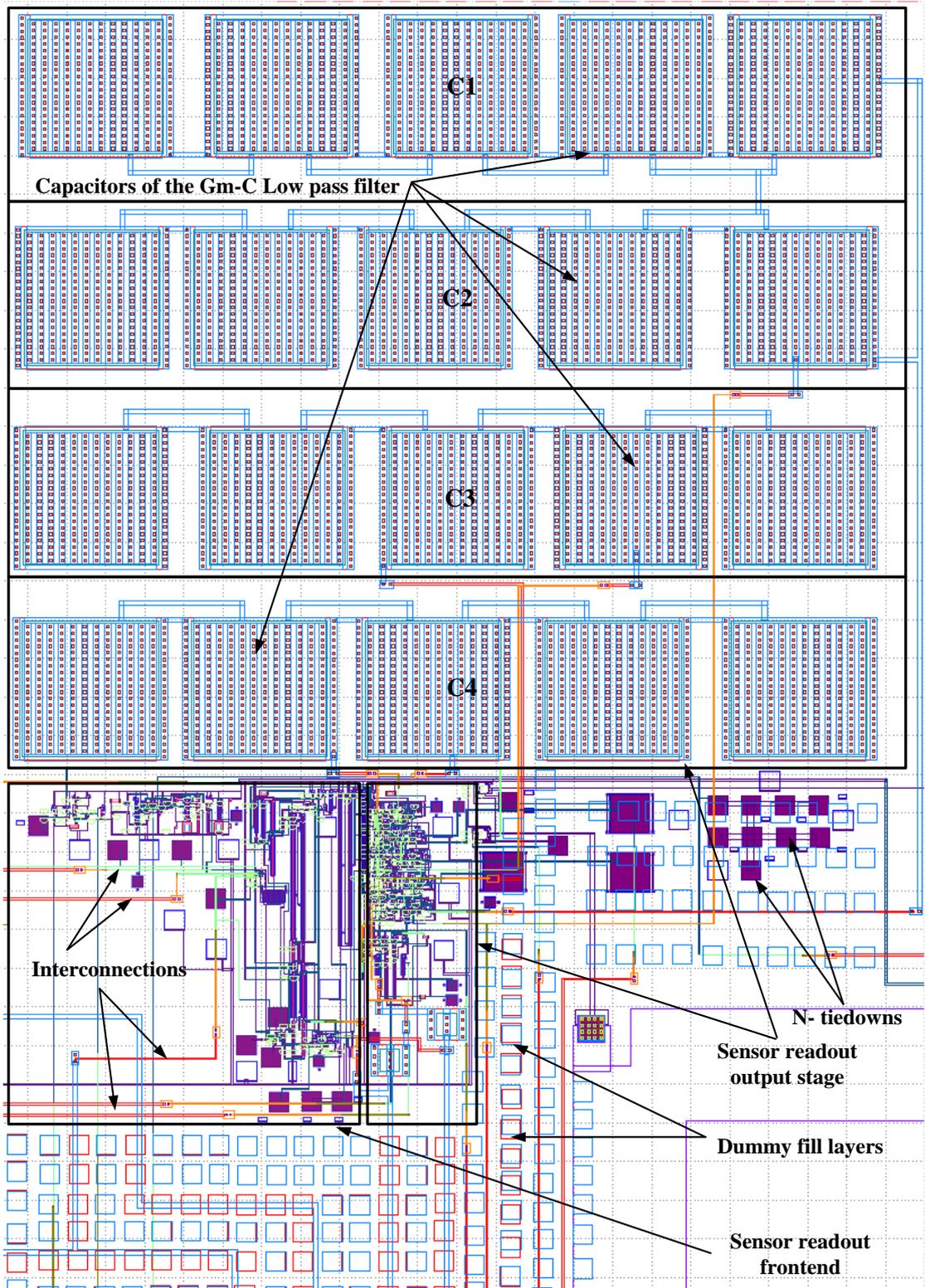


Fig. 5.16: Layout design of the entire sensor readout showing frontend and output stages

5.7 Conclusion

The low power 4th order gm-C filter has been designed to overcome limitations such as high power consumption, non linearity, and low output voltage swing. The fully differential OTA in 180 nm TSMC CMOS technology has also been designed in 1.4 V supply voltage with CMFB. The simulation result showed a roll-off of 80 dB/decade. Phase response proved that the filter is highly linear for a wider cut-off frequency of 11 KHz. The total harmonic distortion (THD) observed for a differential input voltage of 150 mV peak to peak was -60 dB, which was found to be less than 1%. The self biased buffer design had the capability to drive a capacitive load as high as 15 pF. Its output impedance and the dynamic power dissipation were also significantly low leading to the satisfactory design of sensor readout output stage. A competent on-chip sensor readout frontend and output stage designed in 0.18 μm CMOS technology that was discussed both in Chapters 4 & 5 respectively, was found to have a satisfactory performance. The physical layouts for this integrated signal conditioning circuits were also carried out using L-Edit with the same CMOS technology. The marginal decrease in the overall area of the signal readout circuit was mainly due to the use of metal-insulator-metal capacitors in the Gm-C filter stage otherwise the effective area could have been larger. This TSMC CMOS processed chip became the starting base for the SiGeMEMS process discussed in Chapter 3. Design, analysis and fabrication of an elliptic structured MEMS capacitive pressure sensor were actually the succeeding step of this work; however for the purpose of clarity and flow of discussion, it was described in Chapter 3. The CMOS last-metal opening for establishing interconnections between CMOS circuitry and MEMS sensor is cautiously placed during CMOS layout design for achieving minimal interconnection length for the overall parasitic effect reduction. This contributed to increased sensor sensitivity. The experimental analysis of the micro-sensor system is discussed in Chapter 8.

Chapter 6

Integrated MEMS Pressure Sensor with CMOS Readout in standard CMOS process

6.1 Introduction

Most post-CMOS integration techniques use optimized processes for developing MEMS devices on top of CMOS circuit in addition to the standard CMOS process [98]. Even though the integration process is simple and straightforward; it significantly increases the commercialization cost and time to market. A survey published by InvenSense on September 2012 showed that the present CMOS-MEMS technique requires increased process steps, thus the MEMS device development technique using the modern standard CMOS technology that substantially reduces the number of masks and process steps is required. In mid 90's CMOS-MEMS with a structural element of front-end-of-line (FEOL) was built in standard CMOS and thought to be the future of MEMS design, however, post-processing was unsuccessful in many applications. Post-processing in FEOL has a high risk of damaging either interconnects or the gate oxide, which will result in poor CMOS circuit performance. Later, the proposed separate CMOS-MEMS SIP (System in Package) approach was found to have increased drawbacks such as high cost, high number of wire-bonds and high parasitic effects. Subsequently, BiCMOS-MEMS approach became popular in recent years. A survey of few most recent designs in this BiCMOS-MEMS embedded integration indicates that only of up to 0.25 μm technology were adapted in the process. Moreover, less metal layers that do not allow better process integration were used. Complex integration of CMOS circuit yielded poor performances with this older technology; moreover, the high noise factor in BiCMOS circuit is unsuitable to be adapted for sensor readout applications [99]. Further, the post processing performed in the above integrated devices uses backside etching that led to increased post process variation. The backside substrate etching will drastically vary the threshold voltage of CMOS transistors driving them out of saturation and thus yielding a very low gain with high noise.

Recently 3 and 4 metal standard CMOS-MEMS integration became popular [99]-[102]. The integration of high precision complex CMOS circuitry is a challenge as less number of metal interconnects restrict the high gain high speed circuit layout design. This compelled the incorporation of simple amplification circuit. Moreover, increased interconnect line width causes significant time delay leading to poor performance of the on-chip conditioning circuit. In a 4 metal layered CMOS technology, due to larger line width and device size, signal conditioning circuit may yield poor performances. Further, the die area becomes larger as they

employ noise cancellation technique and on-chip buffer stage. In addition, etching cannot be performed over a long period of time as there is no isolation layer present to prevent the etching solvent from damaging the CMOS circuitry. The required etch time is thus limited by the high probability of CMOS circuit degradation, leading to low feature sized design. The proximity of the device layer is also very close to the underlying CMOS circuit, thus post processing becomes even more tedious. Considering all the above drawbacks and limitations, an industry standard CMOS-MEMS integration technique in the modern 8 metal layered 130 nm CMOS technology is proposed. A foundry compatible post processing technique for device release is also proposed in this work. A monolithic planar integration of high performance complex CMOS readout circuit with sensor devices, in the standard IBM 130 nm CMOS process (CMRF8SF DM) is performed. The cross-section shown in fig. 6.1 depicts the FEOL and BEOL layers of IBM CMOS8RF process with MA top metal option. As compared to the previously reported 4 metal CMOS-MEMS integration, the effective sizes of the sensor micro-systems are drastically reduced in this design. The minimum line width in the recent advanced mixed signal CMOS technology offers less parasitic effect to the sensor devices; hence the overall parasitic effect including anchors is very low in these 8 metal interconnections.

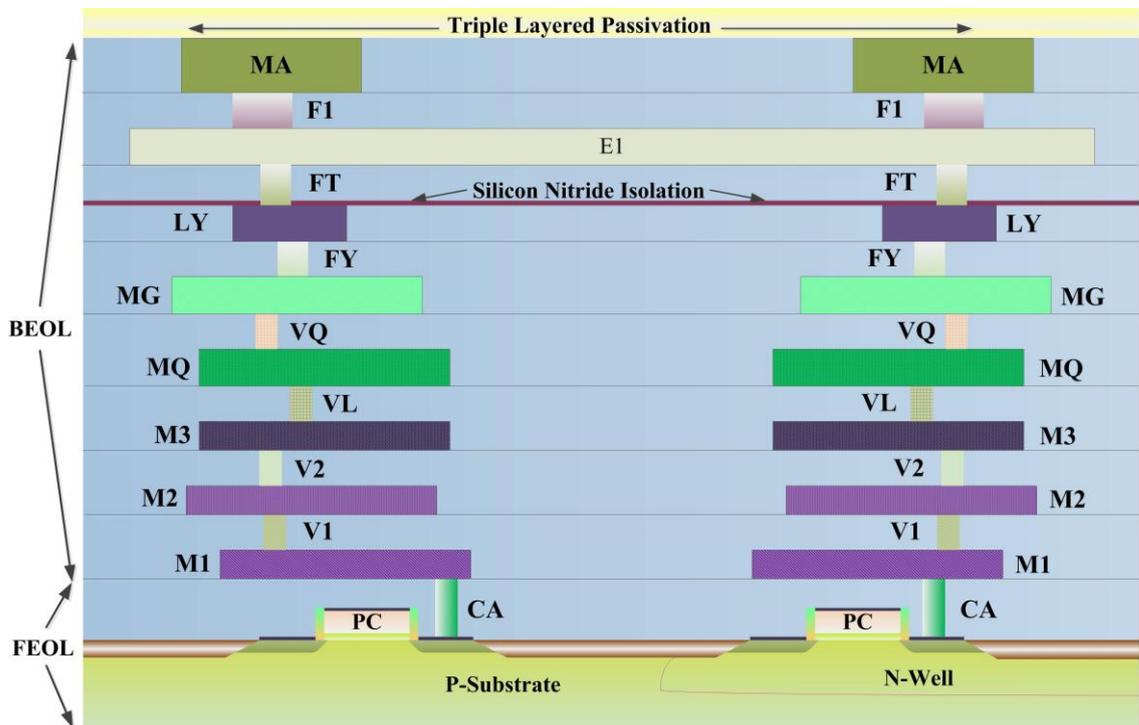


Fig. 6.1: Cross section of IBM CMRF8SF DM process [103]

This work has also exploited the advantages of CMRF8SF DM process, by utilizing the low voltage supply options provided with the thin oxide MOSFET of this multilayer standard CMOS process. The overall power dissipation is thus found to be very low for this sensor micro-machined micro-system. In an 8 metal layer process, an isolation layer serves as an etch stop layer that avoids additional post-processing. Furthermore, the major advantage of 8 metal stacking is that the underlying transistors are nearly 20 μm away from the top MEMS element. This gives much freedom to go in for a long duration lateral etch, further, in an event of over etch the CMOS circuit remain unaffected. The released devices and the associated readout CMOS circuit were experimentally tested. The enhanced performances such as sensitivities, hysteresis and repeatability validate the novelty of the fabricated and post processed sensor chip. The optimized process recipe and successful release steps for a lateral length of 125 μm (die level 130 nm standard CMOS process), are the contributions of this work.

6.2 Features of IBM CMOS8RF technology

The advanced industrial standard CMOS technology offers many advantages that make it attractive for CMOS-MEMS integration. The features of 130 nm IBM CMOS technology that is appealing for sensor integration are [103]:

- Low threshold voltage MOS transistors that yield high performance with a low voltage supply of 1.2 V, provides low overheads catering to high gain amplifier design with cascode stacking.
- Low substrate resistivity of 1-2 ohm-cm enables the substrate to be a proper ground for this low frequency sensor micro-system.
- Shallow trench isolation (STI) provides box type (3D) isolation between the transistors from leakage currents.
- A 0.12 μm lithographic image makes the process simpler and improves the yield.
- The high-k dual nitride metal-insulator-metal capacitor (MIM) uses three metal stacks to minimize the effective area of the sensor micro-system.
- Low resistance Co salicided N+ and P+ polysilicon and diffusion areas offer low signal distortion.
- 8 levels of global metal with common wiring levels with different last metal options provide flexibility of interconnection for complex signal conditioning stages.
- Tungsten stud contact for connecting polysilicon or diffusion to first metal levels

offers low sheet resistance, thereby ensuring a good current flow and negligible voltage drop.

- MA last metal option with a thickness of 4 μm would cater for the better sensor diaphragm design and successful post processing.
- Three layered planarized passivation ensures proper shielding of CMOS interconnects and devices against strong solvent during post processing.
- Bondpads with DV cut options offer flexibility for post-release wire-bonding to PCB.

6.3 CMOS-MEMS design process flow

CMOS circuit design and analysis is performed using the Pyxis schematic tool of Mentor Graphics® CAD software. The entire conditioning circuitry follows the block diagram of the readout circuit discussed in Chapters 4 and 5. The aspect ratios of the transistors were designed accordingly for 1.2 V power supply. In order to enhance the amplifier performance and to further reduce the circuit complexity (that was discussed in Chapter 4), a transconductance enhanced recycled folded cascode (RFC) amplifier is designed. A detail discussion on the design and analysis of this transconductance doubling RFC stage is provided in the subsequent section of this Chapter. Two MEMS capacitive pressure sensor devices with an option of programmable dynamic range are designed and analyzed alongside in the COMSOL CAD software. Once the CMOS circuit and MEMS devices were optimized, complete integrated layout design is then carried out in the Pyxis layout editor. After the satisfactory DRC check, the GDSII file is exported and sent to the IBM foundry for processing. The fabricated die is then post-processed for MEMS device release. Finally, wire bonding is done for this integrated membrane released die, for the purpose of experimental analysis. The complex CMOS-MEMS process that is involved in this design is depicted as a flowchart in fig. 6.2. Some of the design guidelines that were strictly followed for successful process outcome of the CMOS readout circuitry are [103]:

- Nodes sensitive to leakage current are kept at 3X minimum spacing from the transistors.
- Polysilicon and diffusion lines that are highly susceptible to defect or damage are kept greater than 0.25 μm thick. This ensures the integrity of the layers for successful outcome of the design. Moreover to achieve a proper DC voltage drop, polysilicon wires are kept greater than 0.3 μm thick wherever necessary. The lengths of these lines are however kept at minimum for complying with the foundry design rule.

- Chaining of gates was avoided to reduce the local sheet resistance. Contacts for gates are kept with minimum design rule distance.
- To improve the process reliability and yield, most of the metal layers interconnect design and their spacing is relaxed. Precaution was also taken not to compromise with the layout designs that involves the exact width and length. Certain layouts that necessarily require foundry recommended rules are strictly followed for maximum process yield. Despite these layout design methods, additional design strategies to minimize the area of the chip were followed.

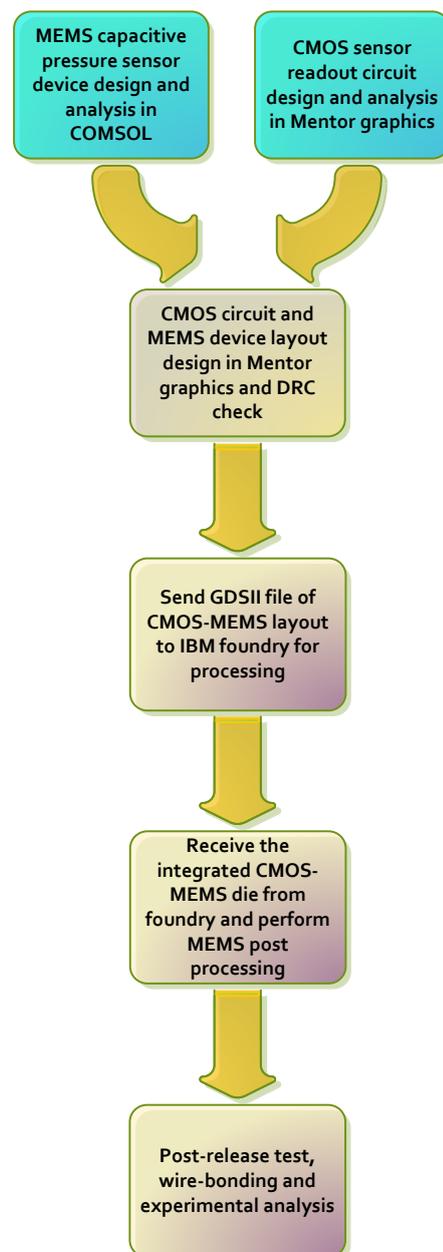


Fig. 6.2: Standard CMOS-MEMS process flowchart

- Redundant contact and vias were used to avoid contact open circuit due to process failure.
- Minimum intersection area of metal interconnects and vias for all layers are done to improve electro-migration reliability.
- Foundry specified global and local pattern density for MA, E1 and LY layers are met in the design.

The analysis and optimization of the MEMS sensor's geometry and dimensions are also discussed in the consecutive sections. The CMOS nano-metric design limitations restrict the geometry design of the sensor structure; however, certain design methodologies are used to overcome these challenges. Two capacitive pressure sensors with rectangular and nano-metric step-edged elliptic diaphragms are designed using the top three thick BEOL metals of CMRF8SF IBM Process. A detailed description of the design is given in section 6.5. Foundry based MPW run compatible post-processing, for the standard CMOS technology developed MEMS sensor devices are detailed in Chapter 7.

6.4 CMOS amplifier design

The block diagrams of the sensor signal conditioning circuit are similar to the one used in the CMOS + SiGeMEMS design (shown in fig. 4.1 and fig. 5.1 of Chapters 4 and 5 respectively). The performance improvement of the amplifier circuit is given much importance in this design as low voltage supply is used. Stacking of transistors is avoided to increase the output voltage swing as the overheads are comparatively high for the 1.2 V supply voltage. The total number of transistors used is also substantially reduced, leading to low noise and low power dissipation. Thus a much simpler single stage amplifying technique with high gain is achieved. A detailed discussion on design and analysis of the transconductance enhanced recycled folded cascode (RFC) is given in this section. Redundant discussion on the preceding and succeeding signal conditioning stages are avoided in this Chapter as they are already discussed in Chapters 4 & 5. The requirement for a high gain and low noise sensor readout amplifier are addressed. A novel current cross mirroring technique is employed to enhance the small signal current. The small signal current is increased by a factor that depends on the input stage current mirroring ratios F and H of the proposed Recycled Folded Cascode (RFC) operational amplifier. The increased small signal current doubles the transconductance (g_m) thus yielding very high single stage gain. Four fractionally split input differential pair transistors are used for achieving further increase in gain without compromising the unity gain bandwidth. Bias current splitting yielded a better slew rate and faster settling time at reduced DC power dissipation. Simulation results using the 130 nm IBM CMOS technology demonstrated a gain of 86.4 dB

for the single stage fully differential mode of the proposed amplifier. A significantly wider open loop bandwidth of 210 MHz was also achieved for an 82.5° phase margin. In addition, an input referred noise level as low as 48.3 μV_{rms} was also achieved.

6.4.1 Transconductance enhanced RFC

An operational transconductance amplifier (OTA) dominates the micro-sensing system circuit design due to its high transconductance ($i_{\text{out}}/v_{\text{in}}$) gain and negligible harmonic distortion. Telescopic and Folded cascode (FC) OTA topologies are the major building block for various CMOS amplifier stages, with FC being the preferred topology due to better gain and signal swing. The inherent advantages such as low flicker noise, low common mode level and high frequency non-dominant poles make PMOS transistors more appropriate as FC input stage [104]. A number of techniques were reported for improving the performance of the FC opamp [104]-[107]; however, power budget was significantly high. Unity gain bandwidth was also compromised by scaling down the size of the input transistors, example shown in [104]. On the other hand, using multistage amplifiers for achieving higher amplification introduces additional noise and pole-zero pairs, thus degrading the performance of a sensor readout circuit. Switched Capacitor (SC) OTAs are another alternative, but their aliasing issue makes them unsuitable for low frequency transducers such as in a pressure sensor application. Moreover, SC amplifier in a sensing system application needs an output filter stage for eliminating the unwanted spikes. The proposed design overcomes the above discussed limitations. Transconductance of the input stage is doubled by a novel current cross mirroring technique, thus significantly increasing the gain of a single stage Recycled Folded Cascode (RFC) amplifier. Transmission gate chopper stabilization circuit that ensures negligible high frequency spikes is employed to reduce the input referred noise. The aspect ratios of the input and the output driving transistor are chosen appropriately for low power consumption without compromising bandwidth.

6.4.2 Circuit design and analysis

It was demonstrated in [104] that the g_m of an RFC is improved by splitting the input transistors and recycling the current. However, since the current flows through only half the aspect ratio (or *fractional aspect ratio*) compared to the conventional FC input transistors, it experiences a high resistance path ($r_o=1/\lambda I_D$), which limits the small signal current and hence the overall g_m . Alternatively, a similar technique, but with multiple cross mirroring is employed in this proposed design which compensates the trade-off between output resistance and g_m of the input stage, allowing the unconstrained enhancement of g_m . Three transistors with appropriate aspect ratios from each half of the differential input pairs with the

combination of the additional transistor from either sides does not provide a high overall resistive path, thus bias current is not compromised yielding higher transconductance. The input stage of the proposed g_m doubling RFC is shown in fig. 6.3. The conventional FC input pair are split into four fractional pairs; hence no compromise is made in terms of silicon area and power. The aspect ratios of the four split input transistors are in the ratio P: Q: Q: P, where Q is kept very small in order to achieve negligible change in the output resistance of the splitted input stage when compared to [104]; hence, I_D is not affected. The bias current $2I_b$ that flows through the cascode current source T14 and T13 is divided by the aspect ratios of the input transistors by a factor of 3 on either branch of the input transistors. Considering one half of the differential circuit i.e. T1a, T1b, T1c and T1d, the device aspect ratios are chosen such that $I_b/3$ flows through T1a and T1d and $I_b/6$ flows through T1b and T1c. When all the input transistors are in saturation, considering the small signal current for differential operation, current through T1c is mirrored with a ratio of H by transistors T3c and T4d. This increased current is again summed with the currents of transistors T2c and T1d and cross mirrored with a ratio of F by transistors T3a and T3b. Finally, the small signal currents through T3a and T1a combine and flow into the output stage. The small signal output current of the proposed RFC (after differential to single-ended conversion by the output stage) is then given by, $i_{out_diff} = g_{mT1a} \cdot v_{in_diff} [(FH)/2+F/2+F+1]$ that flows through the output current summing network in fig. 6.3. The transconductance given by the RFC in [104] for the input stage is:

$$G_m = (g_m / 2)[K - 1] \quad (6.1)$$

The transconductance of the RFC becomes equal to the conventional FC when K is 3 according to (6.1); hence to double the transconductance higher value of K is necessary. From [104] it is understood that when k is more than 3, the input stage transistors are driven to the triode region causing distortion and a reduction in the overall gain. Large signal analysis is carried out to find the DC bias currents that flow through both the input and the output stages. The DC current direction for one half of the g_m enhanced RFC is shown in fig. 6.4, bias current $I_b/6$ that flows through T1c is mirrored to T4d as $H(I_b/6)$. Using Kirchoff's current law (KCL) at node N1, current through T3b is given as:

$$I_x = \frac{I_b}{6}(3 - H) \quad (6.2)$$

where I_x is the drain current of T3b, I_b is the DC bias current and H the current mirroring ratio.

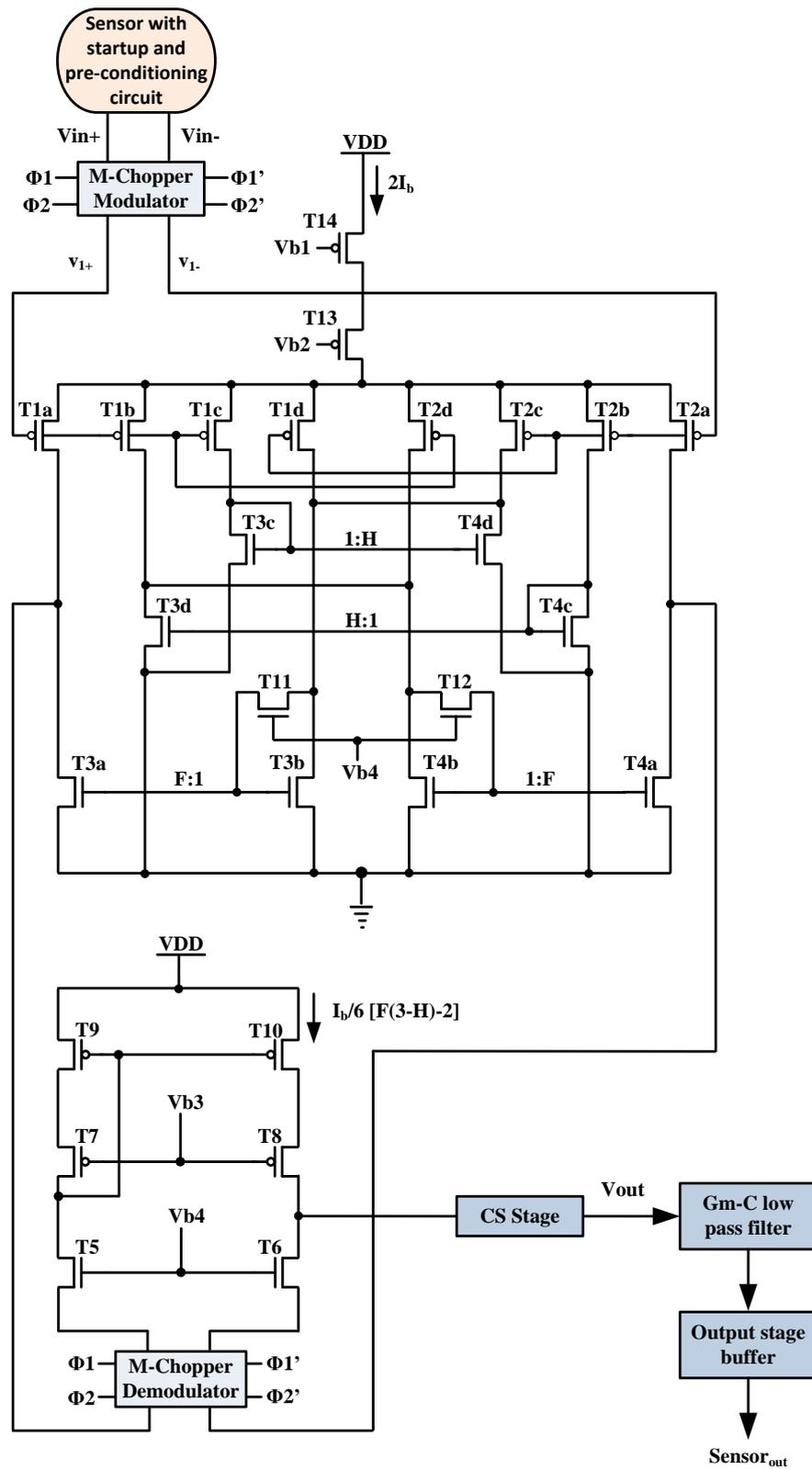


Fig. 6.3: Proposed transconductance doubling RFC

With the mirroring ratio of F, I_y can be given as F times I_x :

$$I_y = FI_x = F \left[\frac{I_b}{6} (3 - H) \right] \quad (6.3)$$

Using KCL at node N2, the bias current that flows through the output stage transistors can be given as:

$$I_z = I_y - \left(\frac{I_b}{3} \right) = F \left[\frac{I_b}{6} (3 - H) \right] - \left(\frac{I_b}{3} \right) \quad (6.4)$$

$$I_o = I_z = \frac{I_b}{6} [F(3 - H) - 2] \quad (6.5)$$

The transconductance for the proposed circuit is derived from the small signal analysis. The small signal equivalent circuits shown in figs. 6.6 (a) to 6.6 (d) are drawn based on the assumed current direction given in fig. 6.4 for better approximation. The small signal currents i_{1a} and i_{1c} flow towards the drain of the PMOS input transistors T1a and T1c, as the input voltage at their gates are assumed to be positive (V_{1+}), whereas, currents i_{1d} and i_{2c} flows away from the drain of transistors T1d and T2c, as they are assumed to have a negative going (V_{1-}) gate input voltages. Fig. 6.6 (a) shows the complete small signal model of one half of the g_m enhanced RFC. Combining the current sources and the impedances, the enhanced small signal current through T3a can be deduced. The simplifying steps of the equivalent circuit are shown in figs. 6.6 (b) to 6.6 (e). The transconductance from the small signal equivalent circuit in fig. 6.6 (e) can be given as:

$$G_m = (g_{mT1a}) \left[\frac{F(H + 1) + N(F + 1)}{N} \right] \quad (6.6)$$

Alternatively, the transconductance can be derived from fig. 6.4 using Kirchhoff's current law. The small signal currents i_{1a} and i_{1c} can be given as $g_{mT1a}V_{1+}$ and $(g_{mT1a}/N).V_{1+}$ respectively, whereas currents i_{1d} and i_{2c} can be given as $g_{mT1a}(-V_{1-})$ and $(g_{mT1a}/N)(-V_{1-})$ respectively. Currents i_{1d} and i_{2c} can be rewritten as $g_{mT1a}(V_{1+})$ and $(g_{mT1a}/N).(V_{1+})$ respectively as $(-V_{1-}) = V_{1+}$. Node N1 in fig. 6.4 can be redrawn for the purpose of clarity to find the small signal current as shown in fig. 6.5.

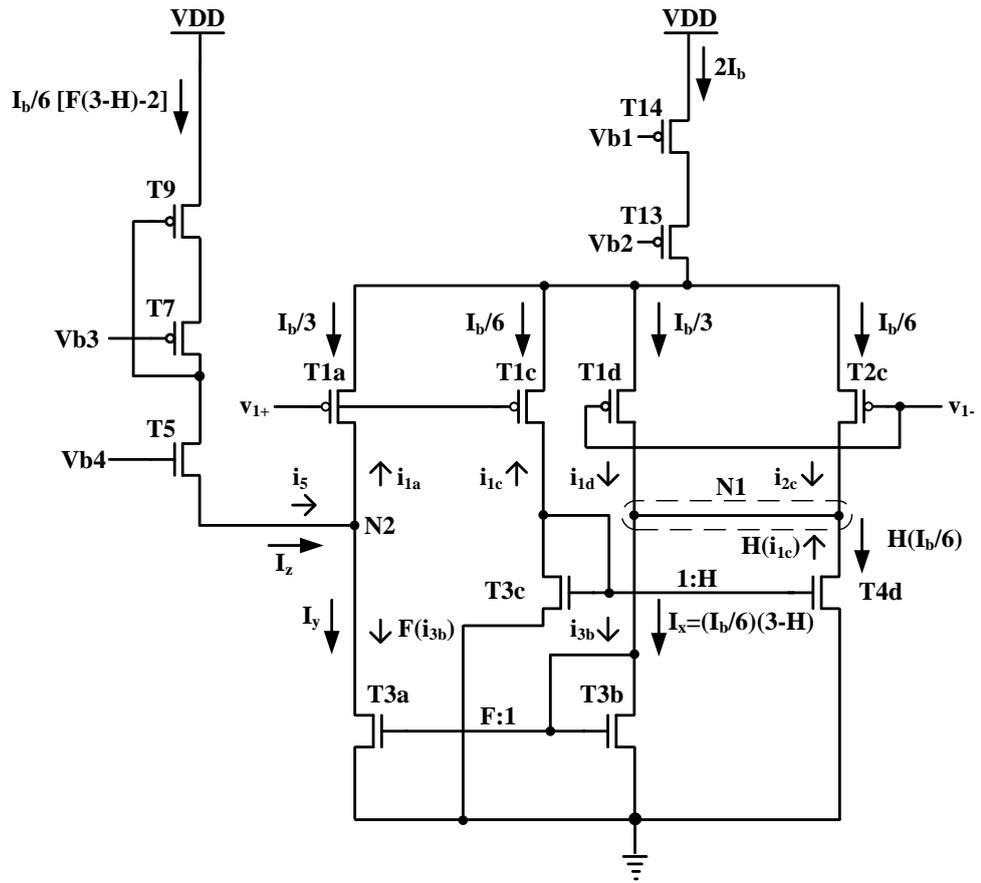


Fig. 6.4: One half of the proposed gm doubling RFC with large and small signal current directions

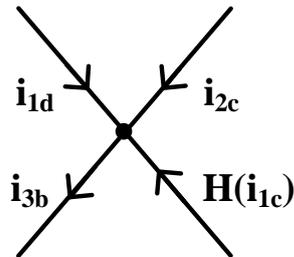


Fig. 6.5: Node currents at node N1

The small signal currents can be derived as follows:

$$i_{3b} = H(i_{1c}) + i_{1d} + i_{2c} \quad (6.7)$$

$$i_{3b} = H\left(\frac{g_{mT1a}}{N} v_{1+}\right) + g_{mT1a} v_{1+} + \frac{g_{mT1a}}{N} v_{1+} \quad (6.8)$$

$$i_{3b} = \left(\frac{H}{N} + 1 + \frac{1}{N} \right) g_{mT1a} v_{1+} \quad (6.9)$$

Applying Kirchhoff's current law at node N2, current i_{3a} can be given as:

$$i_{3a} = F(i_{3b}) = F \left[\left(\frac{H}{N} + 1 + \frac{1}{N} \right) g_{mT1a} v_{1+} \right] \quad (6.10)$$

$$i_5 = i_{3a} + i_{1a} = F(i_{3b}) + i_{1a} = F \left[\left(\frac{H}{N} + 1 + \frac{1}{N} \right) g_{mT1a} v_{1+} \right] + g_{mT1a} v_{1+} \quad (6.11)$$

$$i_5 = \left[F \left(\frac{H}{N} + 1 + \frac{1}{N} \right) + 1 \right] g_{mT1a} v_{1+} \quad (6.12)$$

$$i_5 = \left[\frac{F(H+1) + N(F+1)}{N} \right] g_{mT1a} v_{1+} \quad (6.13)$$

As $i_5 = i_o$, the above equation can be written as:

$$i_o = \left[\frac{F(H+1) + N(F+1)}{N} \right] g_{mT1a} v_{1+} \quad (6.14)$$

The above equation can be expressed in terms of transconductance as:

$$Gm = \frac{i_o}{v_{1+}} = g_{mT1a} \left[\frac{F(H+1) + N(F+1)}{N} \right] \quad (6.15)$$

this is similar to equation (6.6). To express the above equation in terms of conventional FC opamp transconductance, the popular square law equation can be simplified as follows:

$$g_m = \sqrt{2\mu_n c_{ox} \frac{W}{L} I_D} \quad (6.16)$$

For the circuit shown in fig. 6.4, $g_m = g_{mT1a}$, $I_D = I_b/3$ and $W/L = 1/3$, substituting in the above equation we get:

$$g_{mT1a} = \sqrt{2\mu_n \cdot c_{ox} \frac{1}{3} \frac{I_b}{3}} \quad (6.17)$$

Squaring both sides, we get:

$$g_{mT1a}^2 = 2\mu_n \cdot c_{ox} \frac{I_b}{9} \quad (6.18)$$

$$9 \cdot g_{mT1a}^2 = 2\mu_n \cdot c_{ox} I_b \quad (6.19)$$

Taking the square root on both sides of (6.19) will result as:

$$3 \cdot g_{mT1a} = \sqrt{2\mu_n \cdot c_{ox} I_b} \quad (6.20)$$

The above equation can be expressed in terms of conventional FC opamp with the W/L ratio being 1:

$$3 \cdot g_{mT1a} = g_m \quad (6.21)$$

Thus g_{m1a} can be given as:

$$g_{mT1a} = \frac{g_m}{3} \quad (6.22)$$

Substituting in equation (6.15) the overall transconductance can be given as:

$$G_m = (g_m/3) \left[\frac{F(H+1) + N(F+1)}{N} \right] \quad (6.23)$$

where g_m is the transconductance of the conventional FC and N is the transistor aspect ratio scaling factor (between each inner device with the outer device, being 2 in fig. 6.3). Equation (6.23) is the same as equation (6.6), thus the amplifier transconductance is verified with both simplified circuit and small signal equivalent. When the scaling factor N is set to 2 along with the mirror factors F and H being set close to 2, the transconductance actually doubles in accordance with (6.23) when compared to [104].

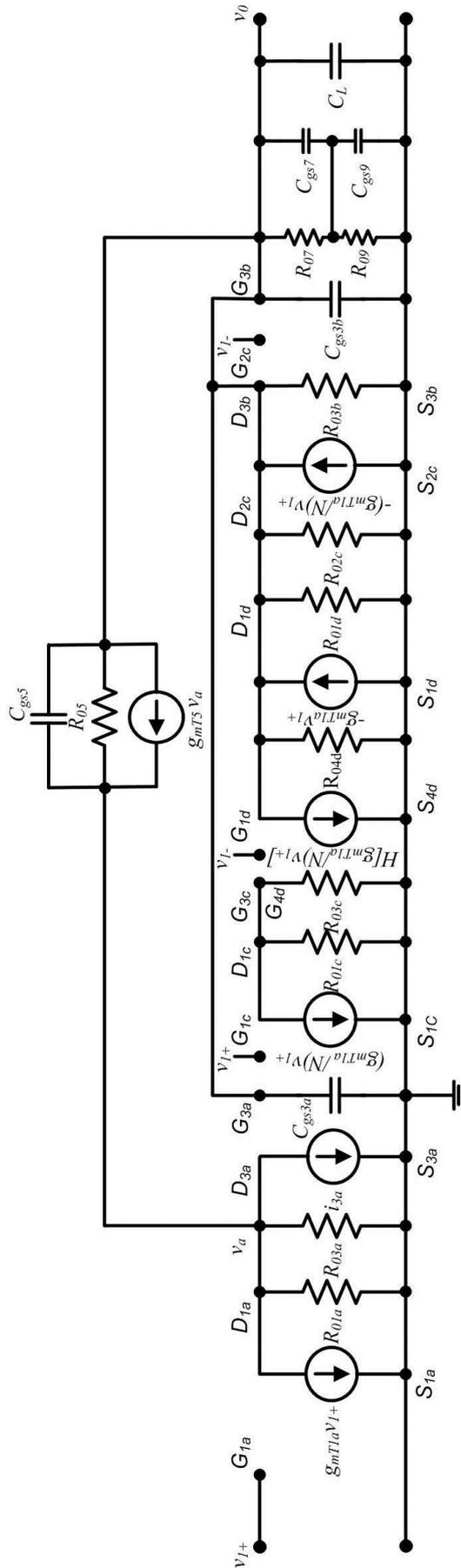


Fig. 6.6: (a) Small signal equivalent of one half of the proposed transconductance enhanced RFC

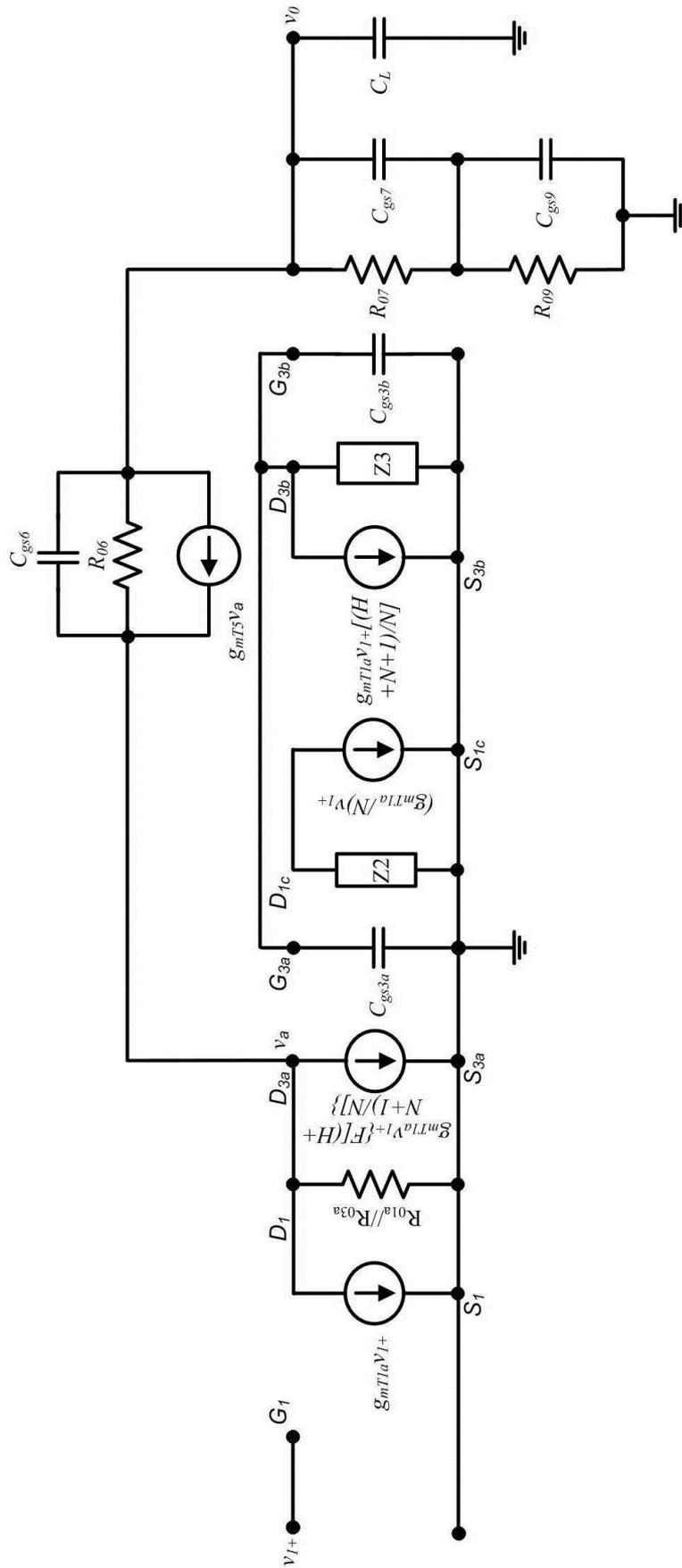


Fig. 6.6: (b) Current sources are merged for small signal analysis

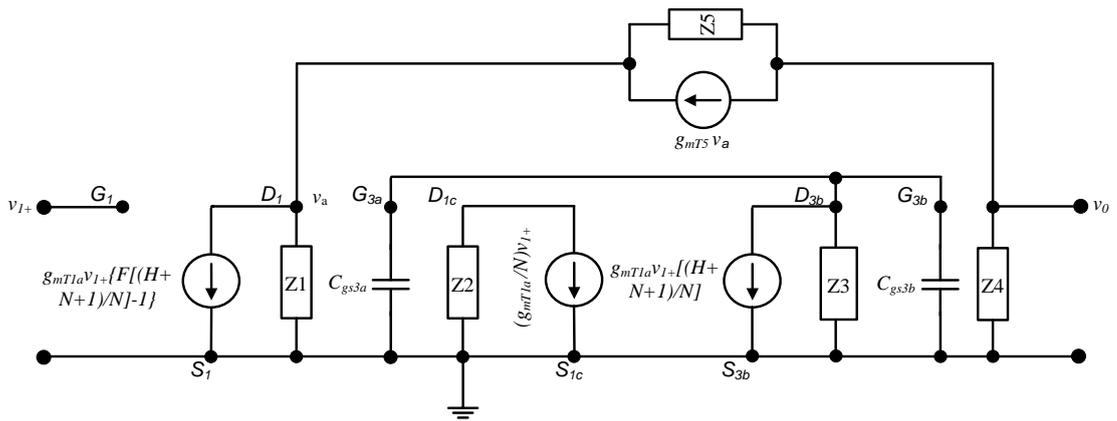


Fig. 6.6: (c) Output impedances are combined for further simplification for small signal analysis

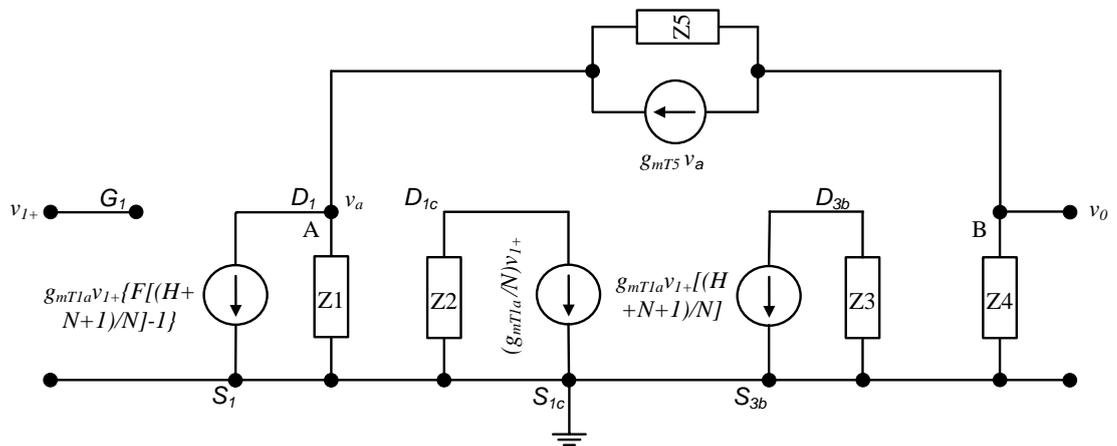


Fig. 6.6: (d) Simplified small signal equivalent of one half of the proposed transconductance enhanced RFC

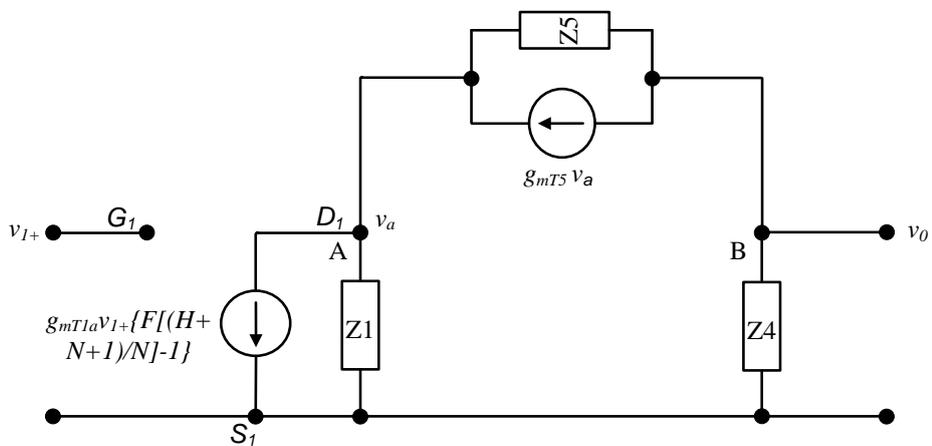


Fig. 6.6: (e) Simplified equivalent circuit for small signal gain analysis

The ratios F & H being 2 does not hold true in terms of the biasing aspect of output stage, as can be noted from (6.5) that I_o becomes zero. Hence ratio F is increased for achieving proper output bias current without driving the input transistors to triode region. Current mirror ratio H is kept constant at 2 to ensure proper values of V_{GS} and V_{DS} of the input stages, so that even with process variation the transistors are not driven out of saturation. It was found that with F been varied from 6 to 10, all the transistors were in saturation and the circuit is significantly stable with a high open loop gain of 88 dB. Moreover, it is evident that increasing the output impedances of T6 (T5), T8 (T7) and T10 (T9) in the cascoding differential-to-single-ended converter provides an additional increase in the overall gain. However, considering the power dissipation and the bias current limitations, the aspect ratios of these devices are kept reasonably low. Additionally, reduction in the size of T1a (T2a) and T3a (T4a) due to bias current splitting, further increases the output impedance of the input stage [104], [105]. Thus, an overall increase in gain of 14 to 16 dB is achieved for this single stage amplifier. Another advantage is that the increased resistance at the high impedance nodes pushes the non-dominant poles to higher frequency yielding a better phase margin and stability. Higher phase margin causes a better roll-off in the gain curve beyond the dominant pole. Thus a significant improvement in the unity gain bandwidth is also achieved. In addition, increase in the gain also results in better power-supply-rejection-ratio (PSRR).

The simplified small signal model for half of the differential circuit is shown in fig. 6.6 (e). The current sources and the impedances are combined to analyze the amplifier's transfer function. The simplified small signal model of the single stage amplifier circuit is associated with two nodes A and B. Using nodal analysis with arbitrary current directions, the transfer function can be given by:

$$A_d = \frac{V_o}{V_{i+}} = G_m \left[\frac{Z_4(1 - g_{mT5}Z_5) - Z_5 \left(2 + \frac{Z_5}{Z_1} \right)}{1 + \frac{Z_5}{Z_1} - g_{mT5}Z_5} \right] \quad (6.24)$$

where Z_1 , Z_4 & Z_5 are the small signal impedances given by:

$$Z_1 = R_{o1a} // R_{o3a} \quad (6.25)$$

$$Z_4 = (R_{07} // sC_{gs7}) // (R_{09} // sC_{gs9}) \quad (6.26)$$

$$Z_5 = R_{05} // sC_{gs5} \quad (6.27)$$

where R_{01a} , R_{03a} and R_{05} are the output impedances of the devices T1a, T3a and T5 respectively. C_{gs5} is the parasitic effect of T5. The impedances Z_2 and Z_3 in fig. 6.6 (d) can be given as:

$$Z_2 = R_{01c} // R_{03c} \quad (6.28)$$

$$Z_3 = R_{03b} // R_{02c} // R_{01d} \quad (6.29)$$

where R_{01c} , R_{01d} , R_{03b} , R_{03c} , & R_{02c} are the output impedances of the devices T1c, T1d, T3b, T3c & T2c respectively. G_m is the overall transconductance of the proposed folded cascode amplifier given as in equation (6.23). From equation (6.24) it is evident that increasing impedances Z_4 and lowering Z_5 can significantly increase the gain. However, considering the power dissipation, the current limitation and the location of poles and zeros, the aspect ratios of T5, T7 and T9 are appropriately designed. The low frequency output resistance that contributes to further enhancement of gain can be given as:

$$R_{out} = (g_{mT5} + g_{mbT5})r_{dsT5} \cdot Z_1 // (g_{mT7} + g_{mbT7})r_{dsT7}r_{dsT9} \quad (6.30)$$

Alternatively, the small signal dc gain, when the scaling factor of the input transistors equals to 2 ($N=2$), can be determined as:

$$A_o = \frac{v_{out_diff}}{v_{in_diff}} = \frac{i_{out_diff} \cdot R_o}{v_{in_diff}} = G_m \cdot R_o \quad (6.31)$$

$$G_m = g_{m1a} \left[\frac{FH}{2} + \frac{F}{2} + F + 1 \right] \quad (6.32)$$

$$G_m = g_{mT1a} \left[\frac{FH + 3F + 2}{2} \right] \quad (6.33)$$

$$G_m = \frac{g_m}{3} \left[\frac{FH + 3F + 2}{2} \right] \quad (6.34)$$

$$G_m = \frac{g_m}{6} [FH + 3F + 2] \quad (6.35)$$

Substituting the value of G_m and R_o in (6.31) the small signal DC gain is given as:

$$A_o = \frac{g_m}{6} [FH + 3F + 2] (g_{mT5} + g_{mbT5}) r_{dsT5} \cdot Z_1 // (g_{mT7} + g_{mbT7}) r_{dsT7} r_{dsT9} \quad (6.36)$$

Eventhough the size of the input devices are kept larger than the current summing devices, the overall output impedance is compensated at the output stage to achieve an increase in gain. From (6.36), it can be noted that gain increases more than twice with $F = 5$, and $H = 2$, when compared to [104], moreover, it increases four times when compared to the conventional FC op-amp. The chopper circuits being the interconnection of four crossed coupled switches are assumed to be closed for this AC analysis. Further, their chopping frequencies are neglected as these higher frequencies can be filtered out at the output.

The critical parameter that directly affects the settling time and linearity apart from thermal effects is the slew rate. In fig. 6.3, when v_{1+} increases so as to switch off the transistors T1a, T1b, T1c, and T2d, bias current $2I_b$ flows entirely through T2a, T2b, T2c and T1d, thus the slew rate can be given as:

$$SR = \frac{[F(3-H)-2]}{3C_L} I_b \quad (6.37)$$

Increase in bias current due to current cross mirroring ratios enhances the slew rate by two and a half times with $F = 10$ and $H = 2$ when compared to the conventional FC op-amp. Moreover, while comparing to conventional RFC, the symmetrical slew rate has increased by a factor of 1/2 when the signal input is within the transient limit. This is achieved by keeping the aspect ratios of the differential output load transistor pair equal, for the single ended output design shown in fig. 6.3. For the differential mode output to achieve a symmetric slew rate, CMFB circuit can be employed to balance the differential output charge/discharge rates, leading to significant increase in the overall speed of the proposed sensor readout with same area and power. The CMFB circuit must be carefully designed as mentioned earlier in Chapter 4, to obtain better loop gain and bandwidth in fully differential mode operation. Fig. 6.7 shows the slew rate response comparison between RFC and gm enhanced RFC with a pulse excited amplifier. It can be noted that the overshoots during the rise and fall of the pulse are significantly reduced in the proposed amplifier; further, the positive and negative slew rate has substantially increased.

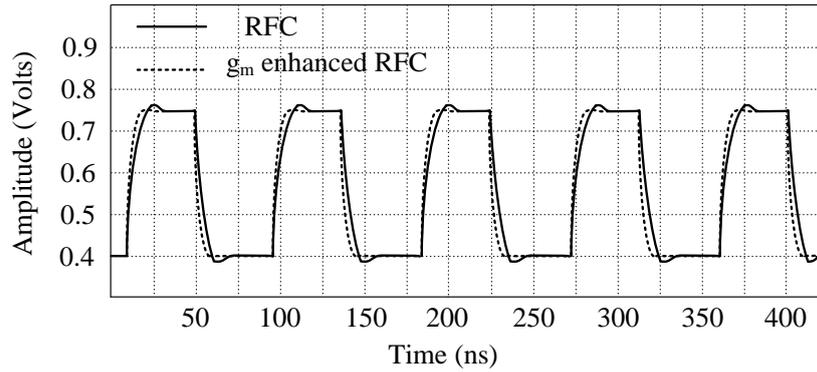


Fig. 6.7: Pulse response of the proposed amplifier

The poles and zeros of the amplifier transfer function, determine the phase margin that provides a better transient response. The output node (node B in fig. 6.6 (e)) of the amplifier contributed to the dominant pole. The proper design of the aspect ratios and current mirror ratios of the transistors in the folding node provided a higher frequency non dominant pole. The pole-zero doublet at node N2 is contributed by the transistors T3a and T5 of the one half differential circuit shown in fig. 6.4. As transistors T3a and T5 are designed using NMOS devices, the doublet is pushed to higher frequency beyond UGB. The proposed amplifier is therefore highly stable for the operating frequency ranges of the proposed sensor micro-system. The current mirroring transistors (T3b, T4b, T3c, T4c, T3d and T4d) that enhance the transconductance do not contribute to additional poles and zeros, thus contributing to better frequency response.

6.4.3 Implementation and results

Area and power are critical parameters in CMOS sensor readout circuit design. Considering the sensor readout requirement, CMOS technology not less than 130 nm (the 8RF-DM process available from IBM) is preferable, as further channel length scaling can result in low transconductance and hence low gain. The sizes of T1b, T1c, T2b and T2c whose currents are cross-mirrored from one half of the differential pair to the other are kept low in order to achieve the proper current mirroring ratio for the indirect transconductance enhancement. Aspect ratios of devices T1a, T1d, T2a and T2d are kept higher for the direct transconductance enhancement. The sizing of these devices was given critical consideration so that their small signal impedances do not lower the unity gain bandwidth. BSIM4 sub-100 μm regime model using Mentor Graphics platform was employed for the simulations. The diode connected devices T3b and T4b are implemented using the triode regime linear active switches T11 and T12 respectively. The devices T11 and T12 are sized so as to provide proper drain voltages for T3b and T4b respectively; which ensures that the devices will remain in saturation during small signal perturbations. This helps to avoid non-linearity and hence achieve the proper (desired) small signal current mirroring ratio. An overall gain of 86.4 dB and a

phase margin of 82.5 degree (@ 0 dB gain) were achieved for the single stage amplifier as depicted in fig. 6.8. A unity gain bandwidth of 210 MHz was also achieved without compromising gain or stability. The proposed g_m -doubling RFC stage, thus meets the critical performance requirements of a sensor readout amplification circuit. In addition, a high output voltage swing of 0.8 V for the 1.2 V supply voltage was obtained by using a common-source (CS) output stage as shown in fig. 6.9 (simulation done without chopper stabilization). AC response of the two stage amplifier shown in fig. 6.10 indicated a high single ended gain of 95.8 dB. The calculated differential gain was found to be as high as 105 dB with the advantage of less area and power. This is comparatively significant with that of the RFC op-amp designs in [104]-[106]; however a marginal reduction in the phase margin was observed when compared to the single stage amplifiers. The cascode biasing stage was designed to ensure good upper and lower bounds of the slew rate (i.e. $SR+$ and $SR-$) achieving a high slew rate of $27.2V/\mu s$. The input referred noise was lowered to $48.3 \mu V_{rms}$ by employing dual frequency transmission-gate choppers. The amplifier also achieved a very high THD (Total Harmonic Distortion) of -75 dB for a 1 kHz input as shown in fig. 6.11. The performance enhancement over conventional RFC design with the proposed amplifier is evident from table 6.1. The aspect ratios that were designed to achieve the desired performances of the g_m enhanced RFC amplifier is shown in table 6.2.

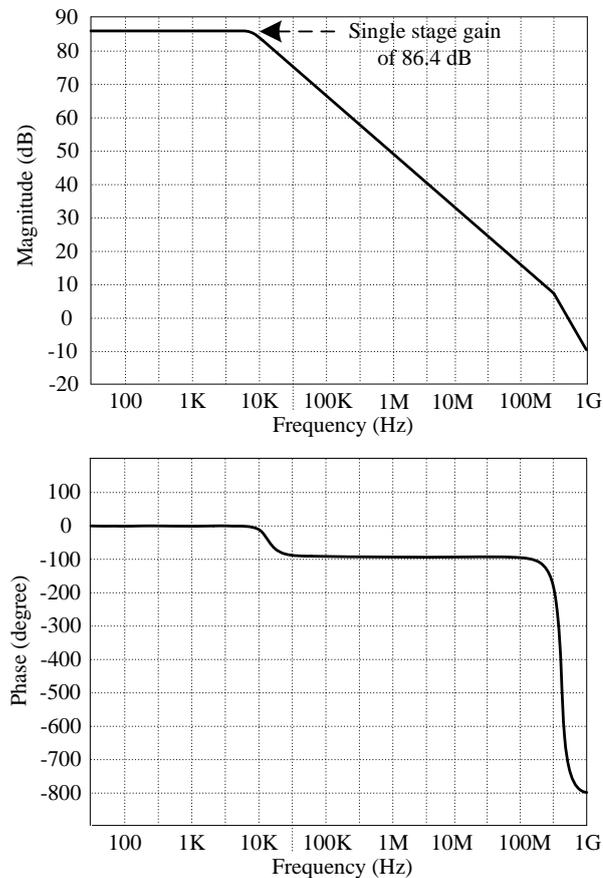


Fig. 6.8: AC response of single stage g_m enhanced RFC

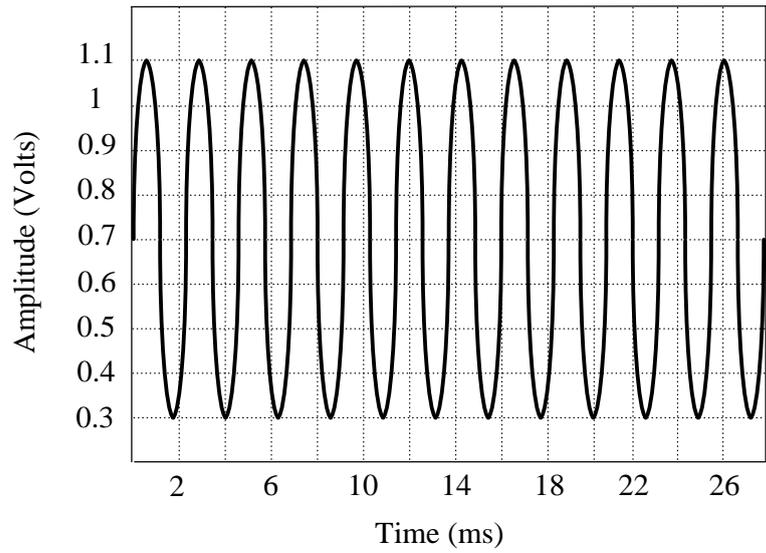


Fig. 6.9: Transient analysis of the proposed two stage g_m doubling RFC

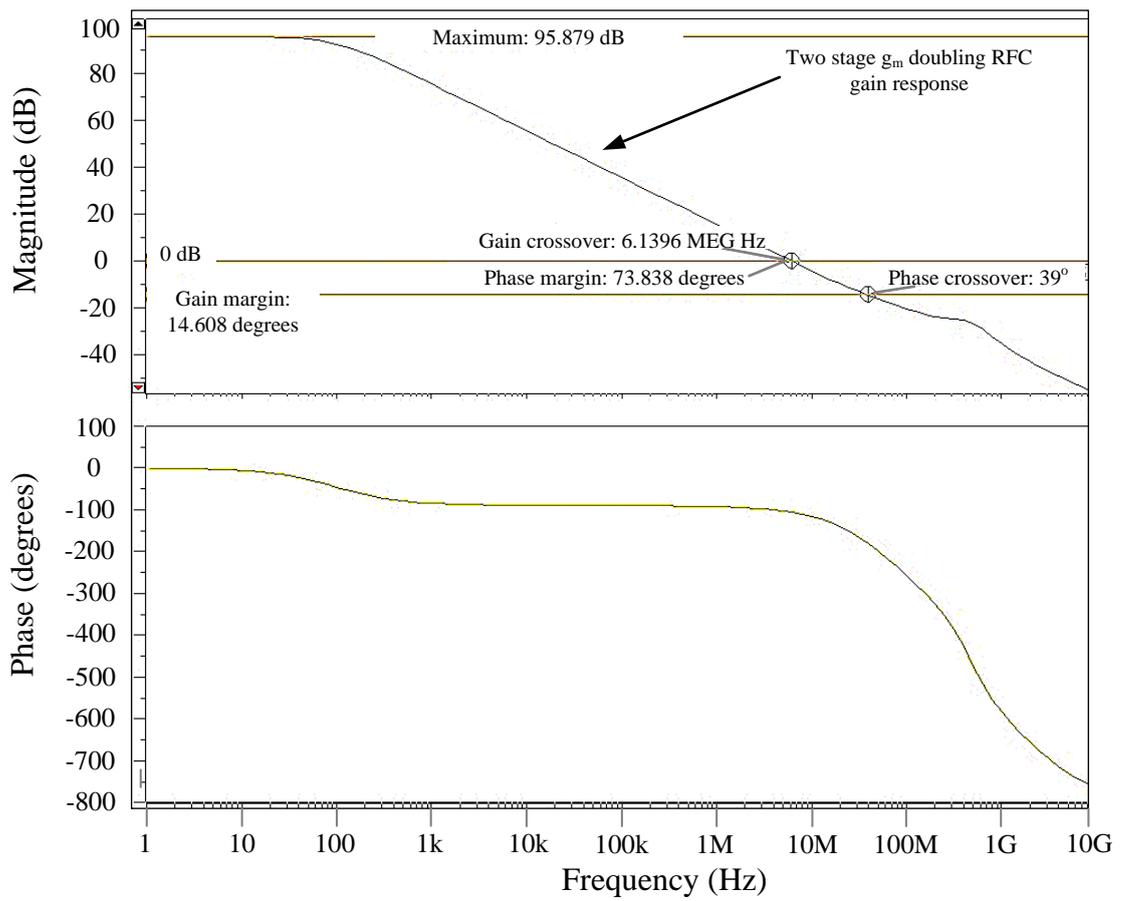


Fig. 6.10: AC analysis of the proposed two stage g_m doubling RFC

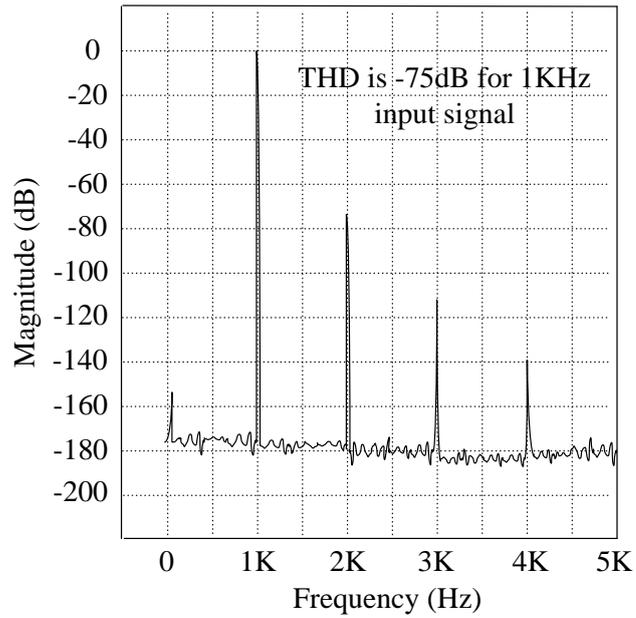


Fig. 6.11: THD analysis for the proposed enhanced g_m RFC

Table 6.1: Performance comparison of different RFC circuits

| Parameters | Folded Cascode [104] | Recycled Folded Cascode [104] | Improved RFC [105] | Enhanced g_m RFC - single stage [This Work] |
|------------------------------------|----------------------|-------------------------------|--------------------|---|
| Bias Current (μ A) | 260 | 260 | 260 | 185 |
| C_L (pF) | 7 | 7 | 7 | 7 |
| Gain (dB) | 41.1 | 60.9 | 70.2 | 86.4 |
| UGBW (MHz) | 70.7 | 134.2 | 83 | 210 |
| Slew Rate (V/ μ s) | 42.1 | 70.2 | 59.6 | 27.2 |
| 1% Settling Time (ns) | 20.7 | 11.2 | - | 11.3 |
| Input Referred Noise (μ Vrms) | 53.2 | 70.7 | - | 48.3 |
| Phase Margin (degree) | 83 | 77 | 70.2 | 82.5 |

Table 6.2: Aspect ratios for the proposed amplifier

| Devices | Size |
|-----------------------|--|
| T1a, T2a, T1d, T2d | $\frac{4 \mu\text{m}}{0.4 \mu\text{m}}$ |
| T1b, T2b, T1c, T2c | $\frac{2 \mu\text{m}}{0.4 \mu\text{m}}$ |
| T3a, T4a | $\frac{5 \mu\text{m}}{0.6 \mu\text{m}}$ |
| T3b, T4b | $\frac{1 \mu\text{m}}{0.6 \mu\text{m}}$ |
| T3c, T4c | $\frac{0.8 \mu\text{m}}{0.6 \mu\text{m}}$ |
| T3d, T4d | $\frac{2.2 \mu\text{m}}{0.6 \mu\text{m}}$ |
| T5, T6 | $\frac{2 \mu\text{m}}{0.6 \mu\text{m}}$ |
| T7, T8 | $\frac{3 \mu\text{m}}{0.6 \mu\text{m}}$ |
| T9, T10 | $\frac{2.5 \mu\text{m}}{0.6 \mu\text{m}}$ |
| T11, T12 | $\frac{0.2 \mu\text{m}}{0.12 \mu\text{m}}$ |
| T13 | $\frac{12 \mu\text{m}}{0.6 \mu\text{m}}$ |
| T14 | $\frac{5 \mu\text{m}}{0.6 \mu\text{m}}$ |

6.5 Design of sensor devices

The device elements designed using the top MA metal layer of the BEOL metal stack in a 130 nm IBM CMOS process are 4 μm thick; hence membrane deformation up to half the plate thickness (i.e. 2 μm) can yield a good linearity and wider dynamic range [69]. Moreover, to comply with the thin plate assumption, the dimensions of the devices are limited so as to get a maximum deformation limit of 2 μm for the desired dynamic range. Thin Plate analysis is carried out in designing the structure and dimensions of the diaphragms as described in Chapter 3. The dynamic range of the sensor devices is directly influenced by their dimensions, thickness and the distance between the plates. In standard CMOS planar integration, as there is no

freedom in designing the vertical structure of the layers such as, diaphragm thickness and distance of the plate, proper design of the device dimensions is the only possible avenue to limit the maximum allowable deflection. Maximum deflection limit in any micro-capacitive sensor devices determine the sensor reliability, as the probability of membrane collapse with bottom electrode is high due to electrostatic effect. At the center of a circular diaphragm, the maximum deflection can be given by [69]:

$$w_{\max} = \frac{p_o a^4}{64D} \quad (6.38)$$

where a is the radius of the diaphragm, D the flexural rigidity and p_o the applied transverse uniform load. The radius of the diaphragm is increased so as to achieve better dynamic range; however, from (6.38) it can be noted that the center deflection also increases leading to high risk of membrane collapse in a micro-level device. To overcome this trade-off the other possible solution is the appropriate choice of diaphragm material that can moderately increase the flexural rigidity; however, for an MA layer, the IBM 130 nm CMOS process uses a standard material with optimized process parameters; therefore there is no possibility to restrict the deflection through material choice. Hence, D remains constant throughout the diaphragm for this homogeneous plate. The device layer being an aluminum material has approximately 30 psim of flexural rigidity. This nominal value of flexural rigidity makes the aluminum diaphragm more brittle than diaphragms developed using polysilicon. This can to some extent limit the maximum deflection at the center without compromising dynamic range and sensitivity. Further, reducing the radius of the diaphragm can substantially limit the center deflection for a given applied load. Moreover, smaller radius circular diaphragm yields increased induced stress and better sensitivity; however, dynamic range and linearity are penalised [70]. Circular geometry eventhough has advantages such as low edge stress and increased center deflection, becomes a poor choice when a limited maximum center deflection is required. Considering the option of an alternative geometry for the same area, an elliptical structure can provide a wider dynamic range without the cost of low sensitivity and poor linearity. The maximum deflection of elliptic diaphragm can be given as [69]:

$$w_{\max} = \frac{p_o}{8D} \frac{a^4 b^4}{3a^4 + 3b^4 + 2a^2 b^2} \quad (6.39)$$

where a is the radius of semi-major axis and b the radius of semi-minor axis. Considering b to be half of a , the equation reduces to:

$$w_{\max} = \frac{p_o a^4}{472D} \quad (6.40)$$

From the above equation it is evident that for the same area the elliptic diaphragm provides a substantially lower maximum deflection, hence comparatively much higher pressure load can be applied to this geometry than circular plate. Thus an increased dynamic range is achieved with the elliptic geometry while not lowering sensitivity and linear response range. The standard CMOS process is generally limited by the minimum polygon angle and feature size; moreover, curved and acute angled structures cannot be realized as mask preparation is almost impossible. The curved edges of the elliptic geometry are therefore restructured with step sided edges. To comply with the restricted minimum polygon size of the MA layer in an 130 nm IBM CMOS process, each step edge was designed with a minimum size of 0.4 μm , the designed geometry is shown in fig. 6.12. Further, the curved edge geometry when subjected to FEM analysis, invariably increases evaluation time for the designed structure size, also the total number of mesh increases at the curved edges due to the angled polygons. Thus step edged elliptic geometry reduces the analysis and evaluation time. The benefits provided by the step sided edges during FEM analysis as a beneficiary CMOS-MEMS design process outcome, can be summarized as:

- Due to the sharp edged structure, the number of meshes at the edges reduces while performing a fine tetrahedral mesh analysis.
- As the structure at the edges are a definite 90° angle, any mesh type is suitable for analysis and therefore mesh optimization becomes much faster.
- Result evaluation is also faster as the number of sectors to be analyzed are comparatively less.

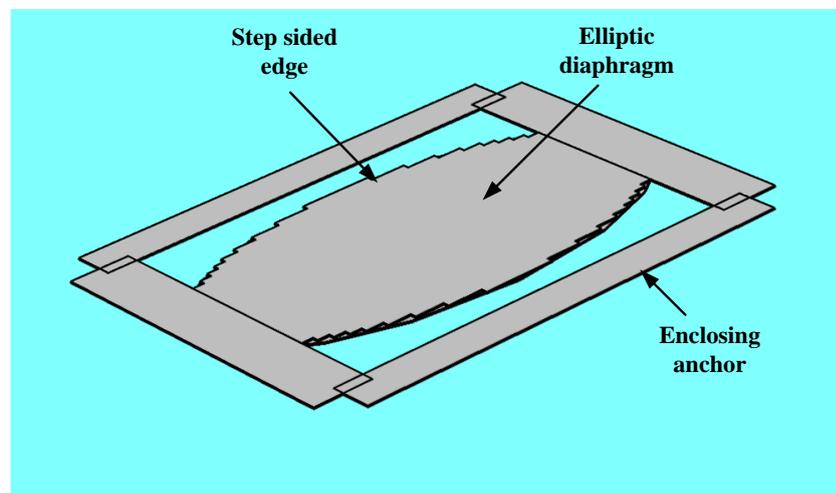


Fig. 6.12: Elliptic geometry with step edge

A different geometry with an option of parallel connection to the elliptic structure can provide flexibility to further increase the dynamic range of the sensing system. A rectangular diaphragm which is compatible for standard CMOS foundry fabrication is more appealing than other structures. Moreover, from the thin plate deflection equation, it is found that the rectangular element can provide a higher dynamic range than square and circular element. It can be noted from fig. 6.13 that closed type anchors are designed to ensure proper clamping. The enclosed anchor design of the sensor elements provides better stress and strain distribution for the pressure ranges above 100 hPa. Moreover, during post processing the vertices of the enclosed polygon became much beneficial in trench etch DWW mask patterning. The FEM analysis for surface deformation of both the sensor elements are shown in figs. 6.14 and 6.15. It can be noted from the figures that for a pressure load of 1000 Pa, the elliptic element deformed less than the rectangular counterpart. This indicates that elliptic diaphragm is much more suitable for a comparatively larger pressure sensing range. The IBM 130 nm CMOS process cross section shown in fig. 6.1 clearly depicts the BEOL metal stack and FEOL layers. The diaphragms are designed in the top MA aluminum layer and the bottom electrode of the capacitive sensor is formed using LY layer of the BEOL metal stack. The CMOS circuitry of the sensor readout is designed in the FEOL layers. The layout of the integrated sensor system is designed using the Pyxis layout editor of Mentor graphics CAD tool, fig. 6.16 (a) shows the layout snapshot of the amplifier circuit, whereas fig. 6.16 (b) shows the MEMS devices layout design with complete readout frontend including low pass filter and output buffer stages.

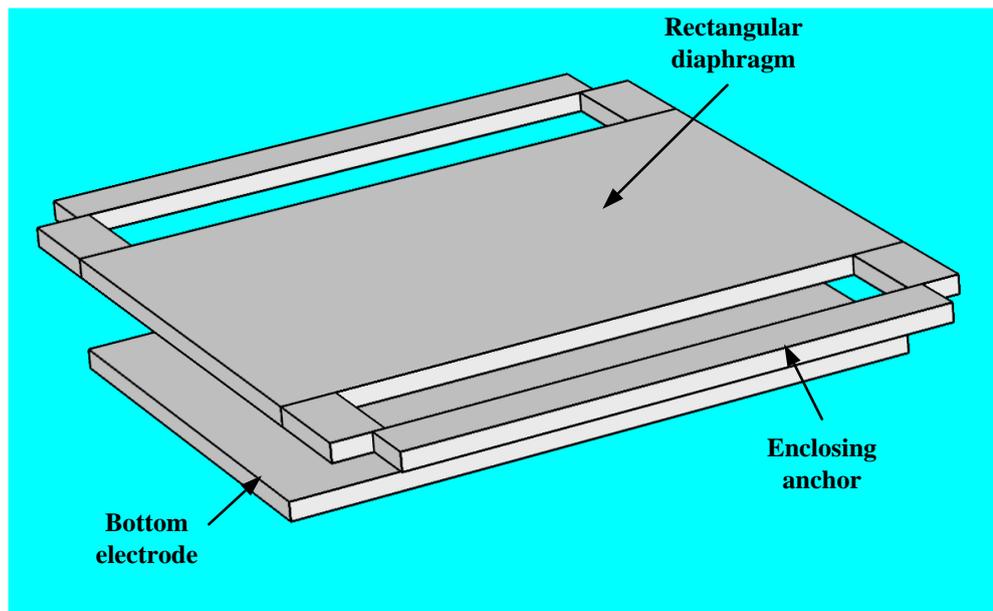


Fig. 6.13: Rectangular geometry with bottom electrode

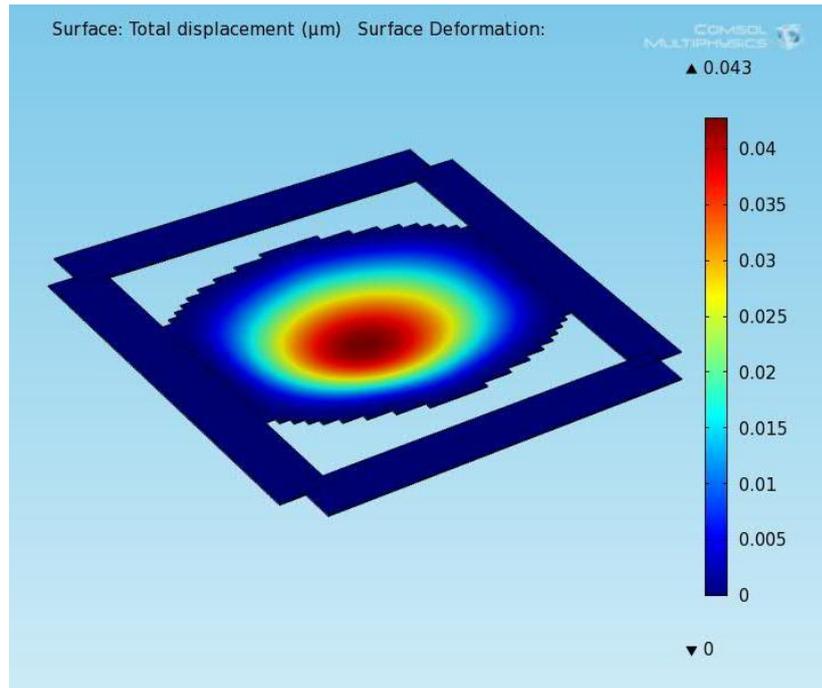


Fig. 6.14: Elliptic diaphragm defromation analysis

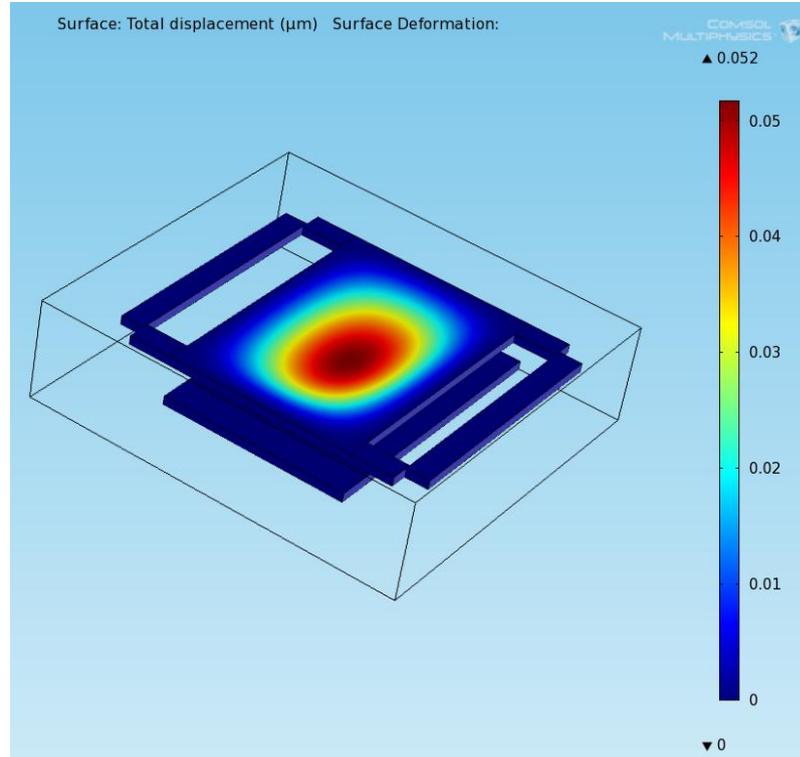
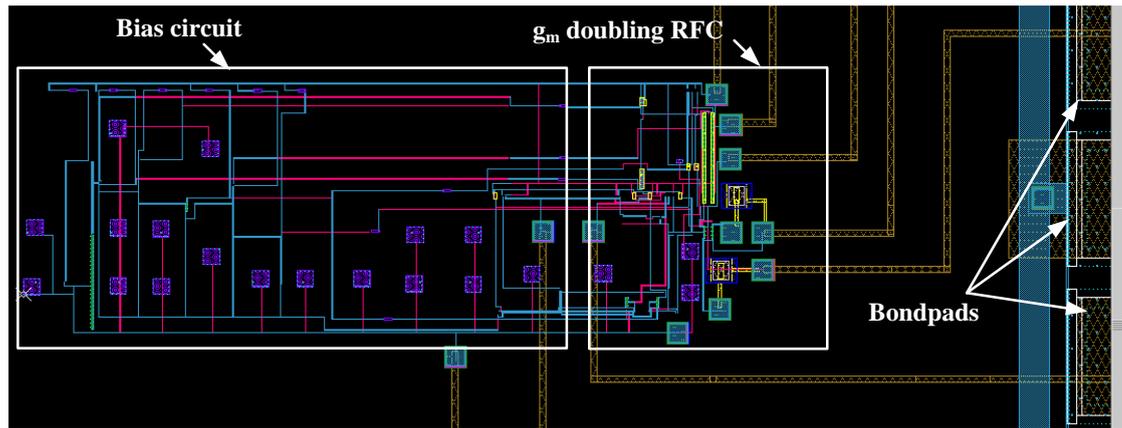
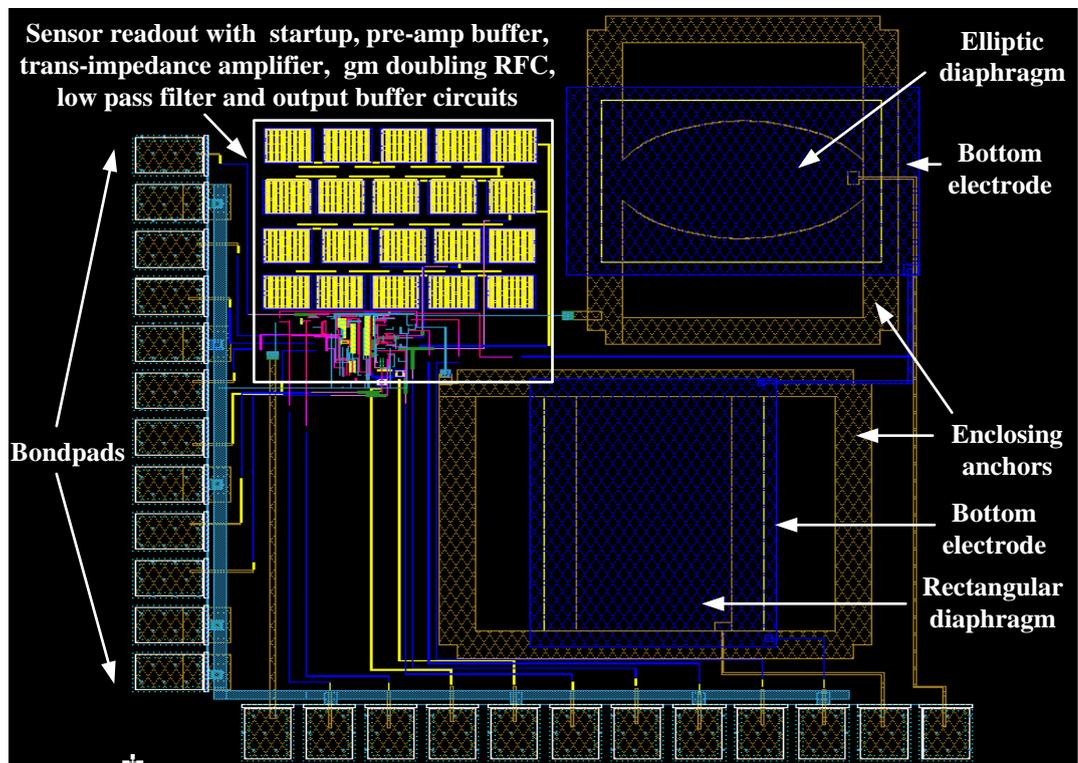


Fig. 6.15: Rectangular diaphragm defromation analysis



(a)



(b)

Fig. 6.16: Pyxis layout window (a) amplifier circuit layout (b) CMOS integrated design snapshot

6.6 Fabricated CMOS-MEMS device

The microscopic image of an IBM fabricated CMOS integrated MEMS sensor die is shown in fig. 6.17. Both the rectangular and elliptic diaphragms developed in MA layer of 130 nm standard CMOS process can be viewed, their dimensions can also be verified with the microscopic measurements. MIM (metal-insulator-metal) capacitors of the CMOS readout circuit designed for low pass filter section are apparently visible. These capacitors are designed using

the top RF metals E1, QY and LY; hence their visibility is good though the microscope. However, the other parts of the readout circuits that were designed using FEOL layers are not visible as they are buried inside. Moreover, the foundry fill layers cover up all the underlying layers; hence it renders poor microscopic visibility of the NMOS devices, PMOS devices and interconnects. A higher resolution microscope is used to verify the process outcome of the elliptic diaphragm edges, as it was a concern. Fig. 6.18 shows that the fabricated step edged elliptic diaphragm ultimately provided a curved shaped structure. Thus the physical realization of the elliptic MEMS device, complying with the standard CMOS process design rule is promising.

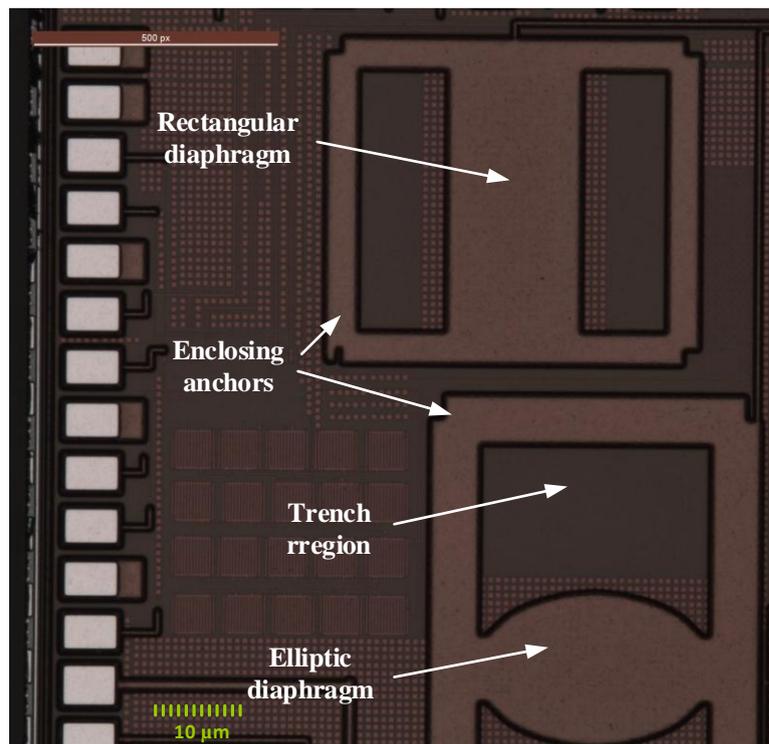


Fig. 6.17: Integrated CMOS-MEMS devices in 130 nm IBM CMOS process

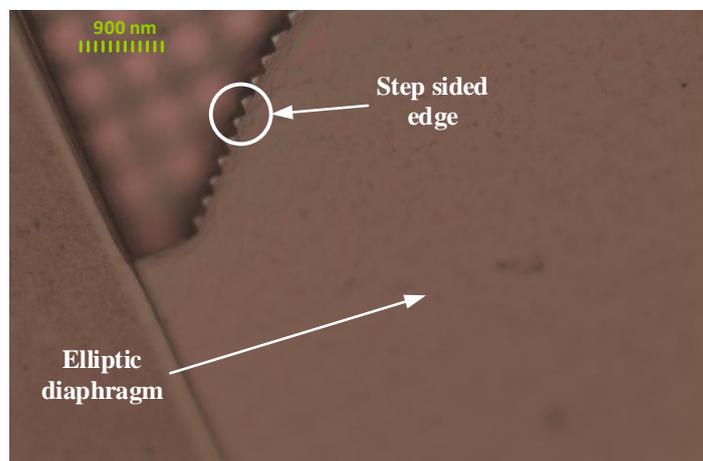


Fig. 6.18: Fabricated step edged elliptic diaphragm complying with the standard CMOS process

6.7 Conclusion

Monolithic integration of complex CMOS readout with MEMS capacitive sensor devices in industry standard 130 nm IBM CMOS process is successfully demonstrated. CMOS sensor signal readout circuit is designed as usual in the FEOL layers, whereas MEMS devices are developed in the top three metal layers of the BEOL metal stack. Three thin, two thick and three RF metals were employed in the BEOL metal options to achieve the desired performance of the sensor system. It has been demonstrated that by using the proposed current cross mirroring technique, a significant gain increment of 16.2 dB was achieved compared to [105] and this was without compromising the unity gain bandwidth. Using lower bias drain and area budget the proposed amplifier achieves an adequate slew rate and settling time, which is critical for the low frequency sensor readout application. The comparison between FC, RFC and the proposed g_m doubling RFC given in table 6.1 indicates the performance enhancement of the proposed design. The design parameters such as device sizes, bias voltages, and the values of F, H and N are carefully assigned to ensure that the proposed design is robust against process, supply voltage and temperature variations. Two different geometries with an optional on-chip active switch for parallel capacitive connections were designed to achieve a wider dynamic range. A CMOS foundry compatible elliptic diaphragm design with enclosed anchor is designed to improve stress-strain distribution at high pressure loads. FEM analysis was carried out to optimize the device dimension of both elliptic and rectangular diaphragms. Deformation analysis indicated that the designed elliptic device has a comparatively wider dynamic range than rectangular device; parallel connection of these two devices yielded an increased overall dynamic range and sensitivity. Post-processing of the fabricated MEMS devices is discussed in the next Chapter.

Chapter 7

Post-processing of IBM CMOS MEMS Device

7.1 Introduction

The development of mature sacrificial layer etching process in recent years has increased the popularity of surface micro-machined MEMS component design. Monolithic integration of MEMS sensor components and CMOS circuit provides reduced degree of complexity compared to other co-fabrication and hybrid integration techniques. The latter is known to suffer from thermal budget constraint in the post-deposition annealing process [98]. The compromised post-process in hybrid integration affects the performance of the MEMS device, as well as, the electronic sensor signal conditioning circuitry. Many experimental results for release etch process in CMOS MEMS have been reported with either wet etch or dry vapor phase etch (VPE) [98]-[102], [108]. However, an effort to release using only the wet etch poses a serious issue of stiction effect, consequently yielding only an unsuccessful release of the device membrane. Use of only the VPE dry etch, on the other hand, leaves a residue with rough surfaces, affecting the reliability of the released MEMS device. Monolithic post-processing and characterization of CMOS MEMS capacitive absolute pressure sensors integrated on an 8-metal BEOL (back-end-of-line) 130 nm CMOS device is explored for the first time in this work. An optimized foundry compatible etch process for an IBM CMOS fabricated top triple layered passivation is discussed. A mixture of wet and Plasma dry etch process is proposed for both an elliptic and a rectangular structured pressure sensor capacitor. Lateral 125 μm stiction free etch from opposite sides was performed successfully for the monolithically integrated diaphragms on the 130 nm CMOS platform. Low power inductive coupled plasma using CHF_3 gas along with high RF bias power is utilized to increase the lateral etch rate compared to vertical etch rate. Mechanical and electrical characterization results indicate a successful etch of the triple layer passivation and the sacrificial oxide. Comparatively higher orders of sensitivities for both elliptic and rectangular geometry fluorosilicate sealed absolute pressure sensors were observed. In addition, the linear capacitive transduction dynamic ranges were also promising for both geometries with 80 hPa pressure variation.

Most of the CMOS integrated MEMS post-processing work reported so far utilizes only at most a 4-metal layer CMOS process (*an early generation CMOS process*). The post processing proposed is performed with a mix of wet and inductive plasma dry release etch, experimentally performed on a modern 8 metal BEOL 130 nm CMOS process [103] overcoming the limitations posed by several reported work discussed above. This CMOS process (also known

by the acronym 8RFDM) contains 3 thin lowest metal layers (M1, M2 and M3), 2 middle thick metal layers (MQ and MG) and 3 thick top (upper) RF metal layers LY(Al), E1(Cu) and MA(Al)). The capacitive sensor is constructed in the region of the 3 upper metal layers. The co-integrated capacitive sensor is constructed in the region of the three upper metal layers. The top MA (Al) layer of the BEOL is the diaphragm (top electrode) and the third metal layer LY (Al) is the bottom electrode. The intermediate E1 (Cu) metal layer was designed as a mesh to act as a test structure during post-processing. Moreover, there are two fabricated sensor geometries (elliptical and rectangular diaphragms) which can be connected with an on-chip active switch to form a parallel variable capacitance, thereby, avoiding curling effects which occur in a multi-finger design based variable capacitive device [99]. Exploring the merger of intricate MEMS sensor fabrication processing on today's advanced deep nano-metric digital CMOS process technologies for single chip sensor-merged-microprocessor-microsystem design is the targeted contribution of this work. This can result in pre-determined post-processing mask layout layers (post-CMOS layers) for MEMS sensor release as a contiguous integrated CMOS foundry mass production process from design tape-out to foundry wafer/die ship-out of the complete sensor micro-system. The overview of the process steps involved in this sensor release etching is shown as a flowchart in fig. 7.1.

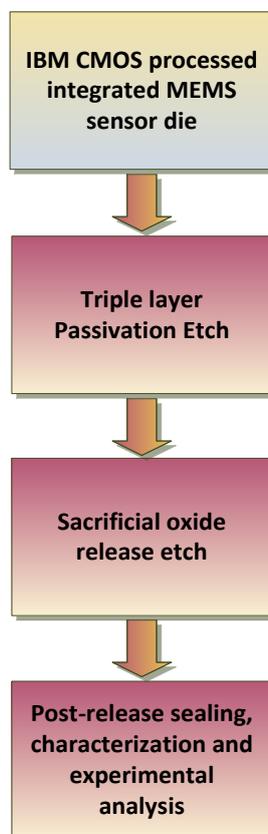


Fig. 7.1: Process steps for sensor release etch

The Chapter is organized as follows: In section 6.2, a brief overview of the photolithography process and resist coating technique is discussed. Section 6.3 describes the etching process for the triple layer passivation in creating the diaphragm devices. Next, section 6.4 depicts the 125 μm lateral release etch technique. In section 6.5, the mechanical and electrical characterizations of the diaphragms are discussed, finally in section 6.6 the concluding remarks are provided. The experimental results for the capacitive pressure sensors are discussed in the next Chapter.

7.2 Etching lithography

The three main processes involved in this advanced CMOS MEMS post processing technique are passivation etch, trench formation and lateral etch. Hence the etching lithography consisted of several stages: 1st stage for dry passivation etch, 2nd stage for dry trench etch, 3rd stage for sidewall protection and wet etch and the last stage for dry lateral release. The composite post-process cross-section diagrams in fig. 7.7 depict these lithography stages in the context of the entire CMOS MEMS post-processing details. Maskless patterning reported in [100] causes reduction in the thickness and sensitivity of diaphragms, hence at least two mask writing steps that uses Direct on Wafer Writing (DWW) are required to perform the complete etching process, as well as, protect the side walls (preserving the sensor anchors). The first mask defines the area of the passivation etch that exposes both the elliptic and rectangular diaphragms, while the second mask defines the trench and under etch (lateral etch) areas. The second mask is repeated several times, as the photo-resist tends to get stripped-off during long etching durations. The specimen being a 9 mm² naked die is taped on to a 1 cm² dummy <100> wafer using a special double-sided ultra-tape, for spin coating. Choice of the tape is quite critical; as it should be both particle free and residue free, otherwise, it will yield poor thermal transfer during dry etch. An ultra-clean tape containing minute leachable metals with Polyethylene backing and Acrylic adhesion is used. The dummy wafer with the attached die specimen is cleansed initially using Acetone [(CH₃)₂CO] to remove atmospheric dust. After initial aerated drying, it is then dried on the hot plate for 30 seconds at 75° C.

The total triple layer passivation thickness being 4.3 μm , requires a photo-resist thickness of at least 7 μm , so that considering even a 1:1 selectivity ratio, the resist will remain in place for the entire RIE (dry Plasma etching) passivation etch process. The resist is optimized for spin duration, spin speed and resist quantity by trial runs on a dummy wafer before actually trying on the specimen. The sample is spin coated at an angular velocity of 4000 rpm for 40 seconds using a thick AZ P4620 series photo-resist. For the first five seconds the spin coater runs @ 500 rpm for slow even coating throughout the surface of the wafer. This slow startup avoids resist lumps or bubble formation at the edges of the actual specimen. In addition, the coater is also slowed

down to 500 rpm for the last 5 seconds at the end of the 40 second duration. Prebake is carried out at 75° C for 10 seconds on a hot plate to dry the solvent (acetone moisture). The specimen is then subjected to DWW using a Micro-tech LW405A laser writer as shown in Fig. 7.2. Eventhough the DWW used in this work is at the die level, the same type of resist and methodology is also compatible with pre-determined design-rule driven wafer level foundry process. The etching mask layout was designed using the Clewin mask layout CAD tool. The device layout pattern on the specimen die is used as the reference pattern to get position accuracy of up to $\pm 0.1 \mu\text{m}$. The vector patterning mode requires three vertices points to align the specimen with the etch mask layout of the Laser-Draw 2D software. The masked specimen is then exposed and developed in diluted KOH (Potassium Hydroxide) solution. A mixture of KOH solution with DI (De-ionized) water using a concentration ratio of 2:3 yielded good resist development with the specimen being kept in the solution for a duration of 6 minutes. This development duration was necessary due to the thickness of the resist. The top polyimide layer of the die served as a protective layer for the underlying CMOS devices and circuits against the strong KOH developer. Microscopic observation showed that the regions where the passivation etching is necessary developed quite well (being away from the edges), as evident from the resist developed top-view images in fig. 7.3. The lithography for both the sensors appeared to be satisfactory. The specimen is then hard baked at 125°C for 4 minutes to enhance the resist adhesion to the surface of the chip. This avoids resist peel-off during passivation etch, which can affect the top Aluminum CMOS circuit interconnects as in another post-CMOS MEMS process reported in [101]. This proposed MEMS post-processing mostly uses plasma process (@ low chamber temperature) for sensor structure release; hence risk of degradation in the circuit interconnects and vias are not present as reported in [101], where the die is exposed to high thermal budget release (@ 535°C).

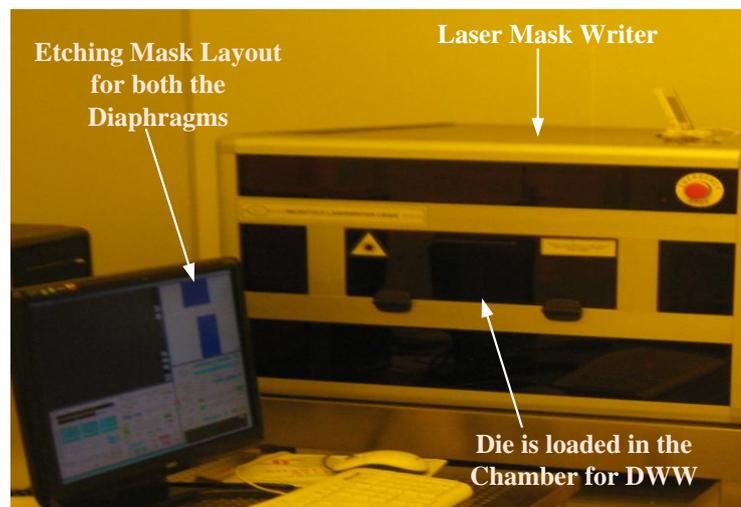
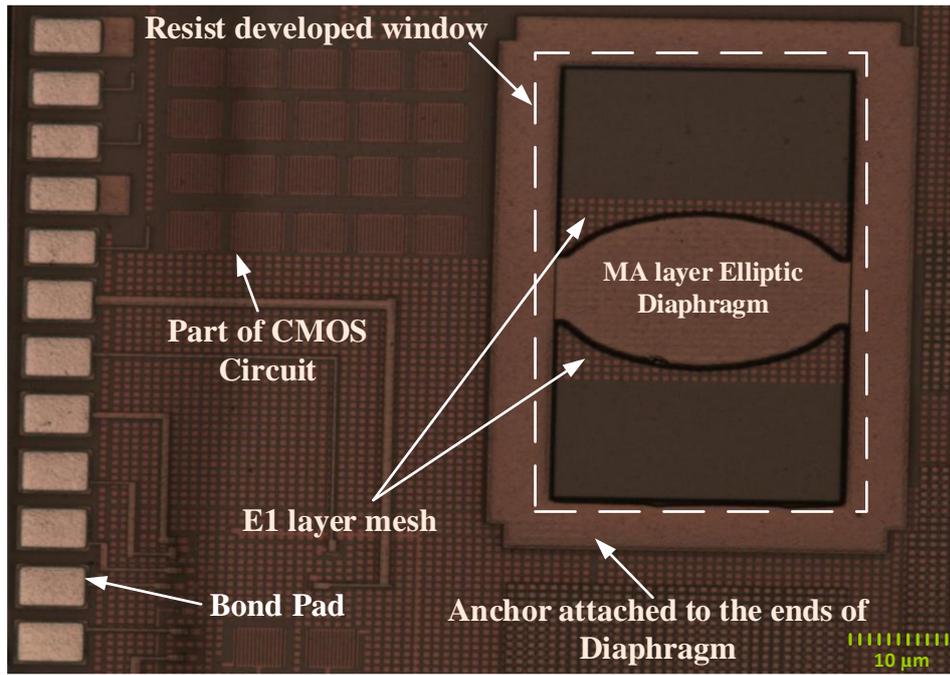
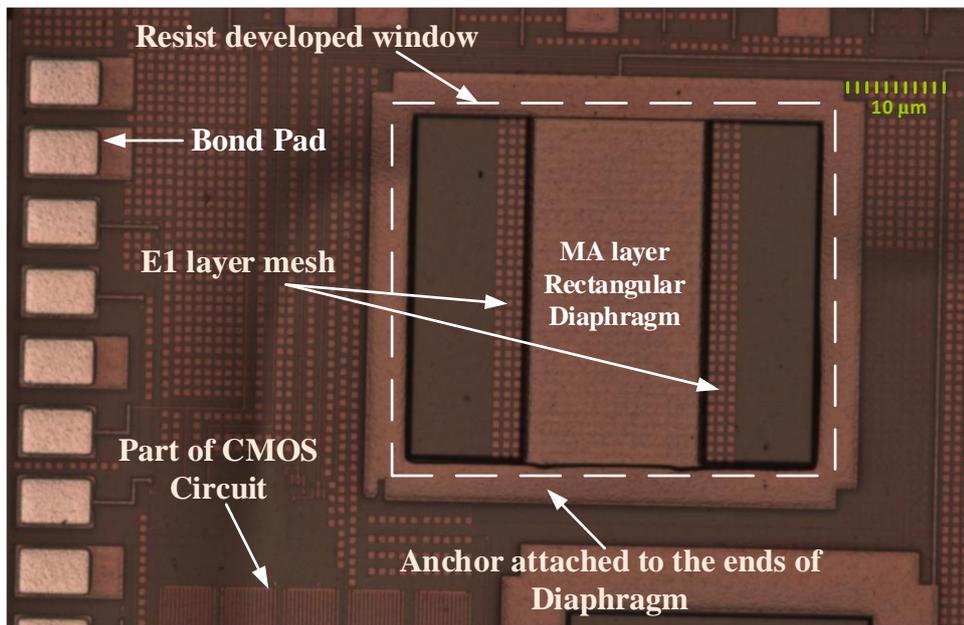


Fig. 7.2: DWW Mask writing system and setup



(a)



(b)

Fig. 7.3: Resist developed sensor capacitances, (a) Elliptic diaphragm, (b) Rectangular diaphragm

7.3 Passivation etch process

The triple layered passivation sandwich in the 130 nm IBM CMOS 8RFDM technology has the following constituent layers; the top Polyimide layer, the middle Nitride layer and the bottom Oxide layer. The dry Plasma based RIE method which provides an almost anisotropic etch is employed for the passivation cut.

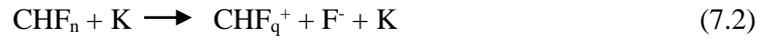
7.3.1 Polyimide etch

Oxygen (O_2) Plasma is used to perform the Polyimide cut. The complex virtual metrology (VM) optimization was avoided due to the time-constraint [109]. A simpler method of optimizing the process parameters is to first trial-run the cut on a dummy sample. To optimize the recipe, Polyimide of thickness $2.5\ \mu\text{m}$ is sputtering deposited on a sample wafer. The chamber pressure is maintained at 600 milliTorr. A low RF coil power of 100 W along with a high Inductively Coupled Plasma (ICP) power of 1000 W is applied while maintaining the chamber temperature at 0°C . The sample is etched for 5 minutes using Oxygen with 50 sccm (standard cubic centimeter per minute) flow rate. Step height analysis using an Atomic Force Microscope (AFM) revealed that the Polyimide is etched down to $0.7\ \mu\text{m}$. The process is repeated for 5 more minutes with an increased ICP power of 1200 W resulting in a cut depth of about $2.5\ \mu\text{m}$, thus concluding the successful trial etch. The etch is next performed on the actual specimen using this optimized trial recipe. To increase the etch rate and etch selectivity, C_4F_8 (Octo-fluoro-cyclo-butane) gas with 3 sccm flow rate is added. Step height analysis verified the depth of the actual polyimide etch. No significant residue was observed on the die that could effect the following Plasma etch. Resist remains on the die became hardened and was removed by the stripping process detailed in section 7.3.3.

7.3.2 Nitride and Oxide etch

Nitride, in the passivation is $0.45\ \mu\text{m}$ thick. RIE dry etch using SF_6 (sulfur hexafluoride) Plasma with 45 sccm flow rate is utilized to achieve good vertical side-walls that will make further processing feasible. Wet etch is not used at this stage in order to minimize side-wall under cuts. In addition, in a further effort to avoid undercuts at this critical step, CHF_3 (Fluoro-form) gas at 30 sccm flow rate is added to the SF_6 plasma for better anisotropy. Increased anisotropy will avoid the lift-off of the diaphragm anchors during subsequent isotropic wet etch. Using 40 milliTorr chamber pressure ($@\ 0^\circ\ \text{C}$), 20 W RF coil power and 250 W ICP power a good vertical Nitride etch rate was achieved. After an initial etching for 40 seconds, step height analysis revealed $0.38\ \mu\text{m}$ etch (cut) depth, hence an additional etch for 8 seconds was performed. The etch rate for the 48 second duration was thus 580 nm/minute. The final dry passivation oxide layer etch was performed using CHF_3 Plasma at 40 sccm flow-rate. Process

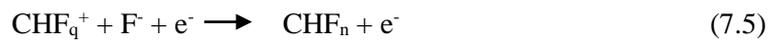
parameters of 1500 W ICP power, 50 W RF coil power and 5 milliTorr chamber pressure (@0°C), yielded the required etch depth of 1.35 μm . The specimen was etched for 6.3 minutes, for which the etch rate was 500 nm/minute. The CHF_3 Plasma was observed to have a bright milky white color as shown in fig. 7.4 inside the ICP-RIE (fluorine) chamber of the Oxford Instruments PLASMALAB100. The Plasma RIE reactions are next presented in brief to consider any residues in the etching process that may deteriorate the post-processed MEMS sensor. The molecular dissociation and ionization of CHF_3 during this etching process can be given by [110]:



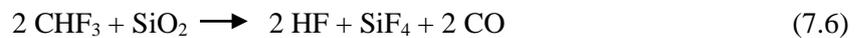
Reaction of $\text{F}_{(a)}$ atoms with Oxide, can be given by:



In the above reactions, $y \leq 3$, $n \leq 2$, $q \leq 1$, $\text{F}_{(a)}$ is atomic fluorine, and, K is an electron or a heavy particle. When the Plasma density is very low with few molecular ions, some of the F^- ions recombine with CHF_q^+ ions in the reverse reaction, and, further chemical reactions can be given by:



The reaction of the recombined CHF_3 on oxide is given by:



The dissociation and ionization of SF_6 can be given by:



Reaction of $\text{F}_{(a)}$ with Nitride, can be given by:

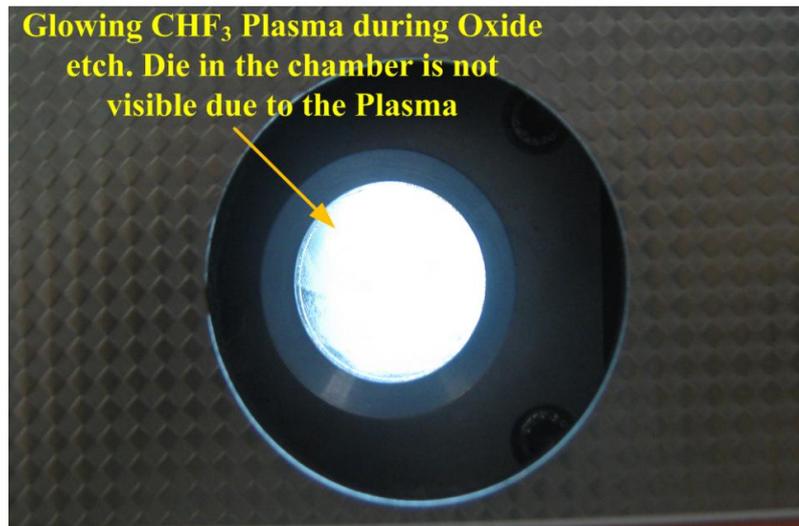


Fig. 7.4: Photo of RIE chamber during CHF₃ Plasma etch

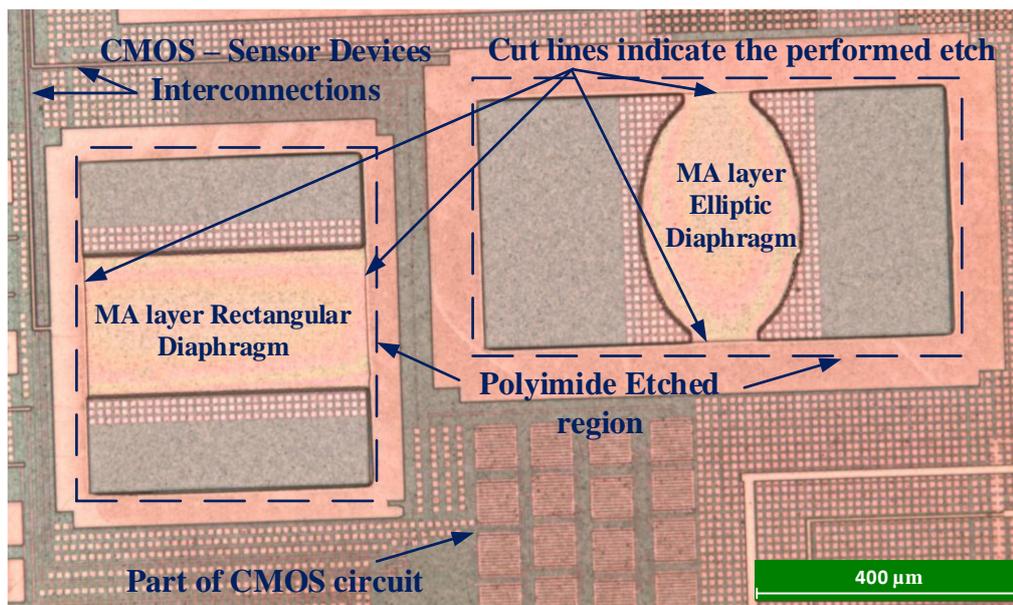
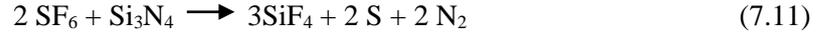


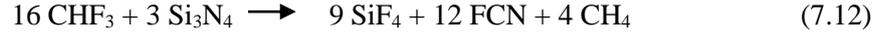
Fig. 7.5: Diaphragms after Polyimide etch



In the above reactions, $x \leq 6$, $m \leq 5$, and, $p \leq 4$. Some of the F^- and SF_p^+ will recombine and react with Nitride (similar to the CHF_3 Plasma), and these reactions can be given by:



The CHF_3 Plasma dissociations for Nitride etch follows (7.1), (7.2), (7.4) and (7.5). Also, any recombined F^- and CHF_q^+ in this case will react with Nitride and will be given by:



As can be seen from the above ionizations and reactions of the Plasma etch process, most of the products are gaseous and any residue will settle on the chamber wall, and hence, no post-cut cleaning is required to preserve the sensor integrity.

7.3.3 Photoresist stripping

The 7 μm thick photoresist, coated over the chip with direct mask writing survived the three steps of dry passivation etch. The resist remnants cannot be easily stripped-off using wet acetone cleaning alone, being hardened by exposure to ion bombardment. Even though, the top few micrometers of resist gets stripped off, prebake during the lithography process makes the underlying resist layers stick strongly to the surface of the chip. On the other hand, the exposed diaphragm metal could be damaged by the use of any strong solvents. Use of DHF (diluted HF acid), APM (RCA1[111]: Ammonia hydroxide-hydrogen Peroxide-DI water mixture in the ratio 5:1:1) and HPM (RCA2[111]: Hydrochloric acid-hydrogen peroxide-DI water mixture in the ratio 6:1:1), can cause surface micro contamination. PIRANHA treatment (H_2SO_4 and H_2O_2 mixture in the ratio 7:1) was the other alternative, however, more than two minutes treatment can considerably reduce the thickness of the diaphragm metal, thus affecting the linearity and sensitivity of the sensor device. EKC265 solvent, on the other hand, was not also considered suitable, as the copper metallization, interconnect and via in the CMOS circuit of the standard 130 nm IBM CMOS process may be degraded. Moreover this solvent, although used for many industrial resist stripping purposes, requires long duration of plasma ashing for effective stripping. Considering all possible avenues, combination of repeated Oxygen plasma ashing along with wet acetone sonicator cleaning was implemented to strip-off the photo-resist. Initially, plasma ashing with low chamber pressure was carried out for 2 minutes; however resist remains were still found to be present. Thus 6 more minutes of ashing, followed by 10 minutes of acetone sonicator cleaning completely stripped off the resist. Fig. 7.5 shows the image of the passivation etched resist stripped diaphragms. This optimized cleaning procedure is quite compatible with wafer level manufacturing.

7.4 Release etch process

Thin photoresist ($\approx 1\mu\text{m}$) of type AZ ECI 3012, which is suitable for both wet and dry etch is used for the second DWW lithography (Mask 2) for trench and lateral etches (release etch). The use of thin photoresist ensures that tedious resist removal procedures are not needed. The extension of mask 2 over passivation ensures its step coverage. It is suitably designed to achieve proper sidewall resist film thickness through the spin coating and development process as shown in fig 7.7 (f) and verified by AFM analysis. Owing to undercut issues in wet etch, DWW mask layout is designed such that mask window is well away from the side-wall anchor region. This prevents the chemicals from seeping towards areas under the anchor during limited time etch. A combination of dry Plasma and wet etch was adapted for the diaphragm release. The wet pre-lateral etch was carried out for a longer duration than usual to secure a lateral micro-vent (orifice) for subsequent $125\mu\text{m}$ dry lateral release. This wet etch can possibly attack the underlying SiO_2 layers towards the anchors and hence requires a considered/cautious approach.

7.4.1 Trench formation

Dry RIE etch using CHF_3 plasma with 50 sccm flow-rate is used in this first phase of release etch. Oxide layers on either side of the diaphragms are etched vertically to a depth of $5\mu\text{m}$ to form trenches. Dry etch with high ICP power and low RF bias power yields a higher vertical etch rate than lateral etch rate [112] thus forming rectangular box like trenches of dimensions $100\mu\text{m} \times 80\mu\text{m}$. The applied high inductive power of 2000 W increases the ion bombardment and hence the etch rate, whereas the low RF power of 50 W avoids the formation of residual films on the die surface [112]. In order to perform a $5\mu\text{m}$ vertical etch, the process pressure was kept at 5 milliTorr (@ 5°C). The specimen is etched for 9.5 minutes yielding a 530 nm/minute dry etch rate. Some amount of over etch is performed further to confirm the depth of the trench cut. The created shallow trenches allows the subsequent wet etch to further deepen the trench vertically, thus avoiding random directional etch that can damage the diaphragms and the anchors. Diluted KOH (KOH with DI water) rinsing is carried out to remove any piles of oxide after the dry RIE [113]. The thin resist over the surface of the specimen gets stripped-off during this etch; hence a repeat lithography is necessary for further under-etch process.

7.4.2 Wet under etch

Buffered HF (BHF) solution which has a faster oxide etch rate and good selectivity between photo-resist and oxide is used as the under-etching (pre-lateral etch) solution. The mixture contains 100 grams of NH_4F (Ammonium Fluoride) diluted in 150 ml of HF and DI water mixture (in 1:2 ratio). The expected etch rate is 300 nm/minute. There is no intrinsic stopper structure available for the wet etch in the standard 130 nm CMOS process, and hence, timed

etch-stop technique was utilized. BHF etch being isotropic causes few micrometers of lateral oxide etch below the diaphragm thus providing an easy start-up for subsequent lateral dry etch. The 4 μm thick diaphragm (the top MA aluminum) can withstand the aqueous HF chemistry of vertical oxide etch of up to 7 μm . To avoid damages at the sides of the diaphragm, wet etch time is thus limited to an etching depth of 7 μm ; hence the specimen is kept in the solution for approximately 20.4 minutes. Since the oxide etch rate of 300 nm/minute using this BHF mixture can strip-off the resist in 10 minutes, the litho process is repeated after the first 10 minutes of the BHF etch. Eventhough this process involves two steps of lithography, it is less expensive compared to the Vapor phase HF (VP HF) etch method. The yield, if mass production is conducted will be comparable to that using VP HF. The Oxide reaction with HF is given by [114]:



The H_2SiF_6 soluble residue is removed by DI water spray and air-gun drier. The aluminum diaphragm surface is protected by the stable photoresist during the wet etch. However, as a precaution, 5% nonionic surfactant (alkylphenol polyglycidol) is added so that any hydrogen bubble formation can be removed through DI water rinsing. The added surfactant reduces the particulate contamination and lowers the surface micro roughness. Thus no significant remains of hydrogen bubble and surfactant were noticed on the diaphragm surface after the BHF etch and cleaning. This preferred surfactant also has a faster desorption time from the aluminum surface. The surface roughness of the aluminum diaphragm, when analyzed for a $1.0 \mu\text{m} \times 1.0 \mu\text{m}$ area using AFM was found to be as low as 1.54 \AA .

7.4.3 Dry lateral etch

Dry release etch is preferred to avoid stiction issues. CHF_3 Plasma is employed to perform an under etch of 125 μm on either side of the diaphragm through the trenches for a full device release. DWW mask features are designed to allow the ion bombardment on the sacrificial oxide through the trenches and lateral micro-vent, thereby enabling lateral etch under the diaphragms. Faster lateral etch can be achieved with high RF power and low ICP power [112]. Process parameters are optimized by first performing a trial run on a dummy wafer deposited with oxide by LPCVD (low pressure chemical vapor deposition) process. The run showed a 50 nm/minute lateral etch rate for a chamber pressure of 10 milli Torr (@5°C). On the actual specimen, to perform a lateral etch of 125 μm , it was found that 40.8 hours of CHF_3 Plasma etch is necessary. The chamber temperature was maintained at 5°C while RF bias power was increased to 400 W with ICP power lowered to 20 W. This applied high RF power can increase the possibility of residual film formation on the die surface; hence, the chamber pressure was lowered to 7

milliTorr to minimize any residual film. The lithographic patterning was repeated every 2 hours to make sure the diaphragm is not exposed, however, some amount of etch at the sides of the diaphragm could not be avoided. Using thick photoresist the number of lithography steps can be reduced. The nano-metric stepped (slotted) edge features of the elliptic diaphragm (due to pre-fabrication L-Edit MEMS layout constraint) were rounded off (smoothed out) during this long etch time as a beneficial complementary process outcome. Except for this edge smoothing, no other undesired etch is noticed that can substantially reduce the sensitivity of the sensor device. On the other hand, some etch at the sides of the Rectangular diaphragm was noticed. The Si_3N_4 layer above the bottom electrode plate (LY metal, the 3rd metal layer from the top) served as the etch stop layer, hence with the lateral etch of 125 μm , vertical etch was reduced considerably. This etch-stop layer eliminated the need to add a dummy layer of etch-stop metal deposition for protecting the LY (bottom capacitor plate) layer and hence avoiding a long process flow as in [115]. The CHF_3 Plasma with 25 sccm flow rate also provided good selectivity between SiO_2 and Si_3N_4 , and hence, the bottom electrode was well protected. The intermediate E1(Cu) mesh layer which was designed and fabricated as an array of 10 $\mu\text{m} \times 10 \mu\text{m}$ square structures spanning the diaphragm were held intact by the interleaving oxide layer. With the oxide removal in the 125 μm lateral etch the copper mesh array of square layers falls off thus confirming the full release of the diaphragm. Microscopic images of elliptic and rectangular diaphragms during and after release etch is shown in fig. 7.6. The partially released elliptic diaphragm in fig. 7.6 (a) shows some remnant of the E1 copper mesh and residues. The surface texture of the fully released image indicate that the aluminum diaphragm were not affected by the exposure to various plasma during the etch process. Table 7.1 lists the complete dry etch process details.

7.4.4 Post-release Etch

Post release etch process for removal of Nitride isolation layer is necessary to avoid composite dielectric medium in the capacitive sensor devices. The purpose of the Nitride layer above the LY metal in the 8RFDM CMOS BEOL stack is to provide better electrical isolation between the thick RF metals. However, as an inherent advantage, it defends the bottom electrode from surface fluorocarbon residue formation due to the carbon rich CHF_3 Plasma. Furthermore, the isolation layer has protected the capacitive device against pull-in or breakdown. The Nitride etch recipe mentioned in section 7.3.2 is repeated in this etch but with low ICP power and high RF power. Table 7.2 shows the feature comparison of various reported CMOS MEMS devices with this work. The comparative advantage of the proposed post-processing technique is quite evident from the table, with the achievement of a two-sided anchored 250 μm laterally etched diaphragm.

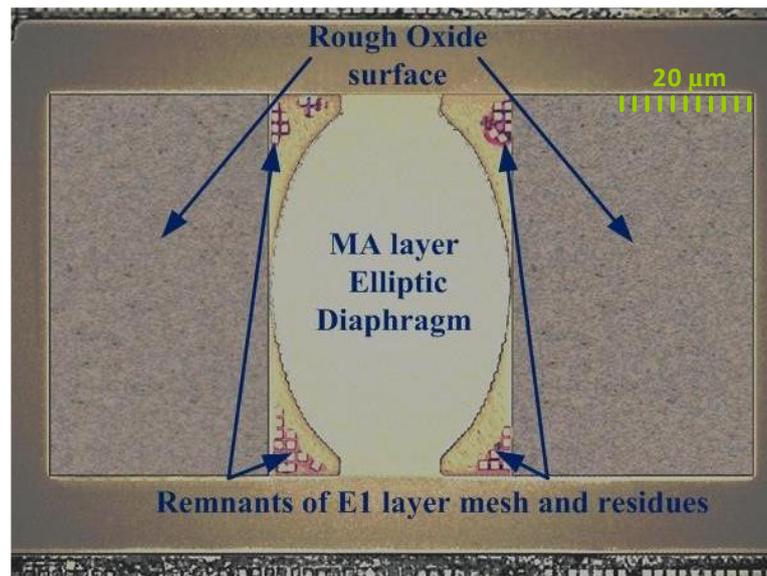
Table 7.1
Process Details for Dry Etch

| Etching Layer | Gas | Flow Rate (sccm) | Process Pressure (mTorr) | ICP Power (W) | RF Power (W) | Etching Time & Rate (minutes) |
|--------------------------|-------------------------------------|------------------|--------------------------|---------------|--------------|-------------------------------|
| <i>Polyimide</i> | <i>Oxygen</i> C4F8 | 50 3 | 60 | 1200 | 100 | 10 & 250 nm/ |
| <i>Nitride</i> | SF ₆ CHF ₃ | 45 30 | 40 | 2500 | 20 | 0.48 & 580 nm/ |
| <i>Passivation Oxide</i> | CHF ₃ | 40 | 5 | 1500 | 50 | 6.3 & 500 nm/ |
| <i>Trench Oxide</i> | CHF ₃ | 50 | 5 | 2000 | 50 | 9.5 & 530 nm/ |
| <i>Sacrificial Oxide</i> | CHF ₃ | 25 | 10 | 400 | 20 | 2448 & 50 nm/ |

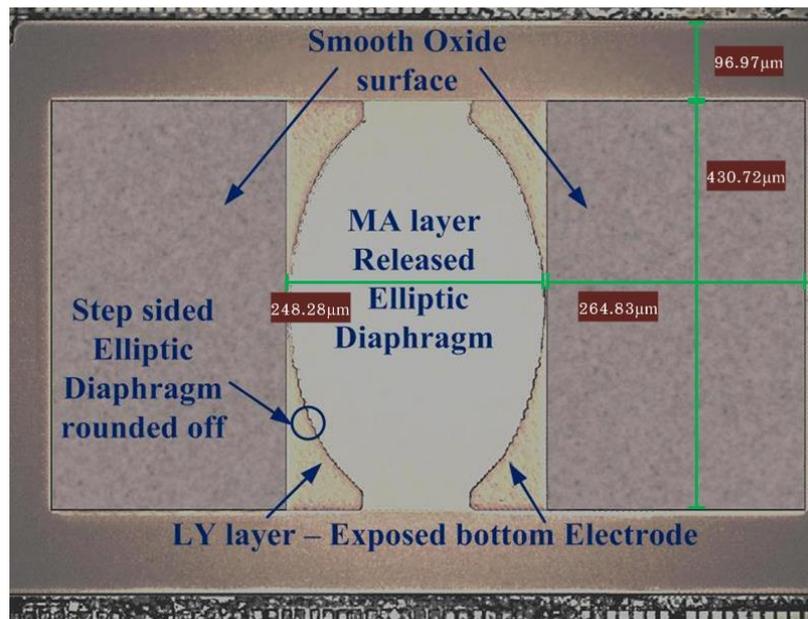
The cross-section of the stages in the MEMS release process as shown in fig. 7.7 can be mapped into the sequence shown by the flowchart in fig. 7.8 for the complete post processing. Since yield in general, have inverse exponential relationship with die area and power complexity, the use of only a small die area ($< 3 \text{ mm} \times 3 \text{ mm}$) and only 2 masks, ensures high post processing yield. As damage and/or lift-off of the diaphragm or the bottom electrode during wet etch and/or dry etch could be a cause of failure, these critical aspects were addressed during the post-process as discussed above. Hence defect-free sensor release was ensured. Due to the complexity of the co-integrated CMOS read-out circuit, some of the CMOS interconnections are routed through the LY and E1 layers for compactness. As the bottom electrode of the capacitive sensor is also on the LY layer, the CMOS circuit is located with some horizontal displacement beneath the diaphragm (as indicated in figs. 7.3, 7.5 and 7.7) for accommodating the LY-to-LY horizontal spacing design rule for the 130 nm IBM CMOS process. Moreover the risk of damaging the LY layer CMOS interconnects during post processing is minimized through appropriate horizontal spacing from the diaphragm above in excess of the design rule. In addition, the MA layer CMOS interconnects that route signals to the bonding pads (also using the MA metal) must always stay well away from the etching regions, in order to avoid any circuit degradation while performing the post-processing. Hence it was not desirable to layout the CMOS circuit just beneath the MEMS diaphragm.

Table 7.2:
Feature Comparison of Various Reported CMOS-MEMS Devices

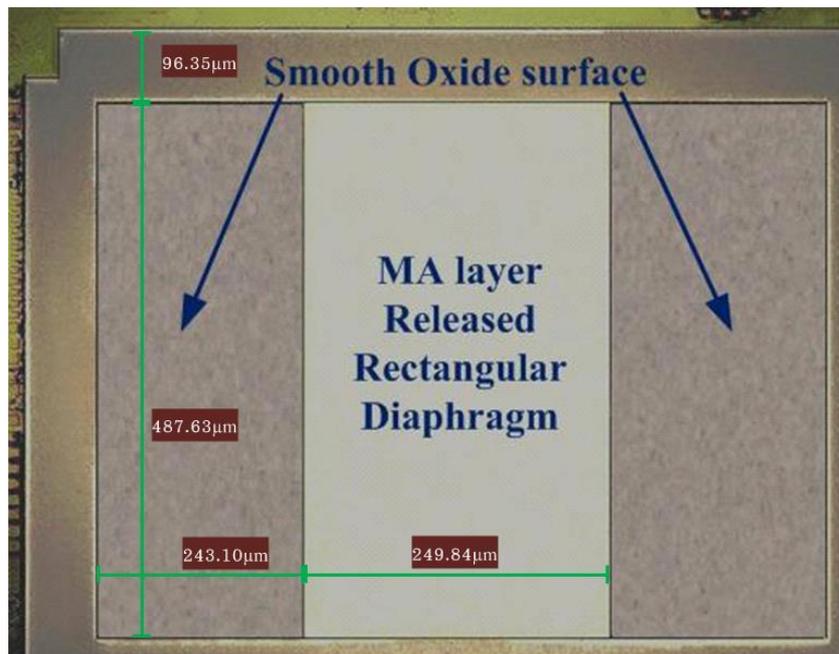
| Device Reported | Number of Metals | CMOS Technology | Type of Sacrificial Release Etch | Risk of Stiction Effect | Lateral Release length | Device Anchored | Post Process Thermal Budget Used |
|-----------------|------------------|---------------------------------|----------------------------------|-------------------------|------------------------|-----------------|----------------------------------|
| This Work | 8 | 0.13 μ m IBM CMOS | Wet and Plasma RIE Etch | No | 250 μ m | Two Sided | 125 $^{\circ}$ C |
| [98] | 4 | 0.35 & 0.18 μ m TSMC | Wet Etch | Yes | Up to 178 μ m | One Sided | < 350 $^{\circ}$ C |
| [99] | 4 | 0.35 μ m BiCMOS | Wet Etch | Yes | 95 μ m | One Sided | 180 $^{\circ}$ C |
| [100] | 4 | - | RIE Plasma Etch | No | 80 μ m | One Sided | 120 $^{\circ}$ C |
| [101] | 5 | 0.25 μ m SiGe BiCMOS | Wet Etch | Yes | 30 μ m | Two Sided | 450 $^{\circ}$ C |
| [102] | 3 | 0.6 μ m Austria Microsystem | DRIE Plasma Etch | No | 250 μ m | One Sided | 225 $^{\circ}$ C |
| [108] | 1 Poly 6 Metal | 0.18 μ m TSMC | Wet Etch | Yes | 6.05 μ m | One Sided | 125 $^{\circ}$ C |
| [114] | 2 Poly 4 Metal | 0.35 μ m TSMC | Wet Etch | Yes | 158 μ m | One Sided | 125 $^{\circ}$ C |
| [118] | 2 Poly 4 Metal | 0.35 μ m TSMC | DRIE | Yes | 1.5 μ m | Two Sided | - |
| [127] | 2 Poly 4 Metal | 0.35 μ m TSMC | Wet Etch | Yes | 1.5 μ m | One Sided | - |



(a)

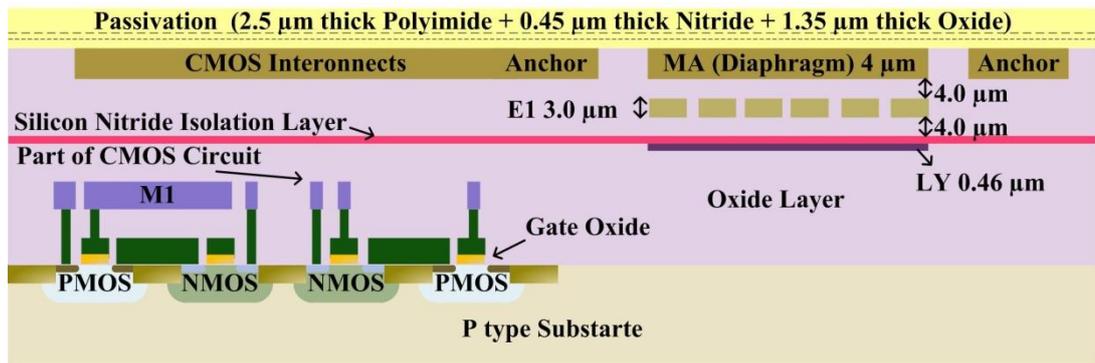


(b)

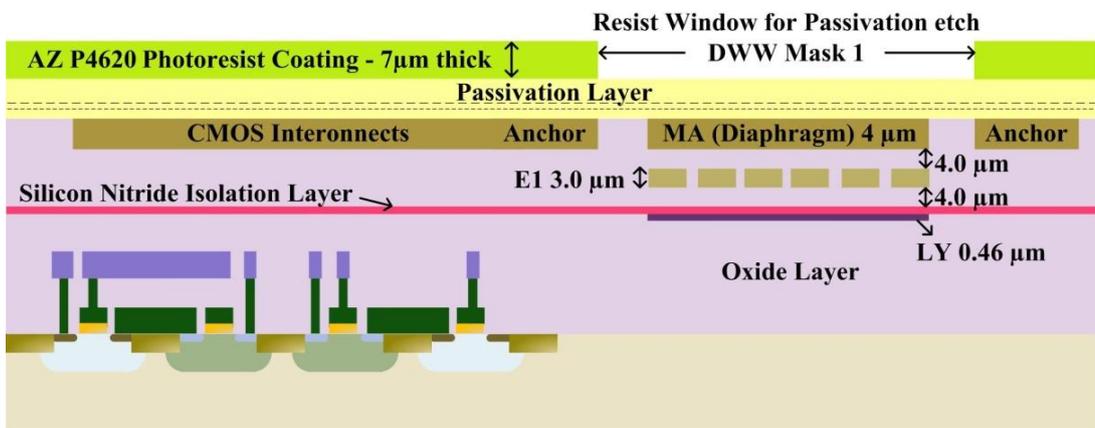


(c)

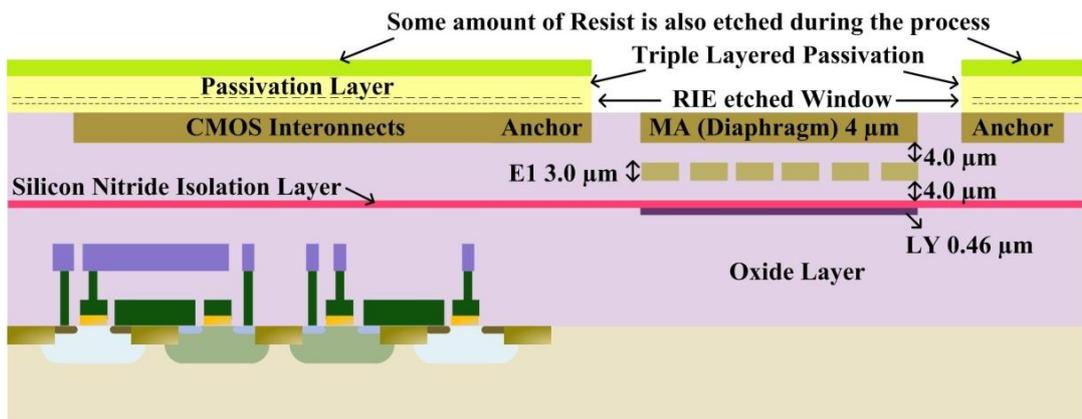
Fig. 7.6: Release etch, (a) partial release of Elliptic Diaphragm, (b) complete sacrificial Oxide and Nitride etch and release of Elliptic Diaphragm, and, (c) fully released Rectangular Diaphragm



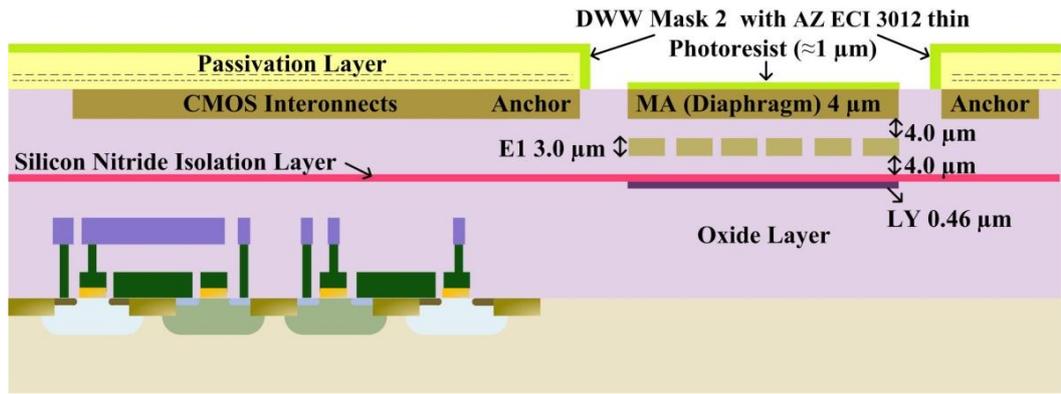
(a)



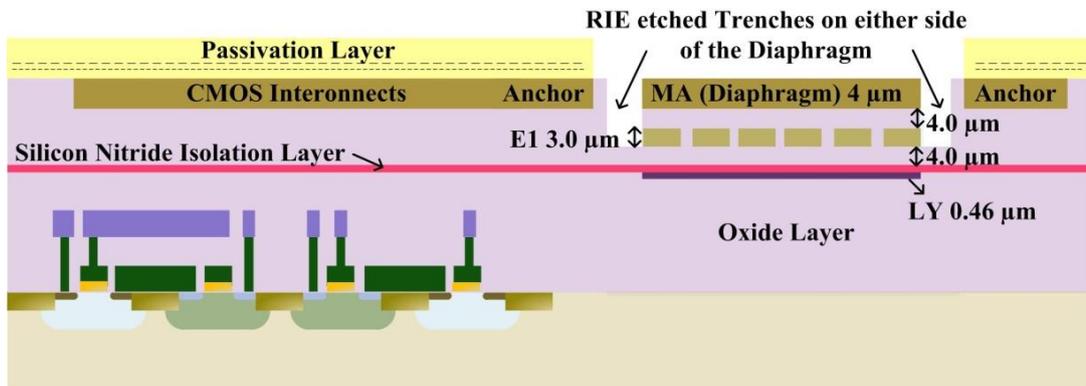
(b)



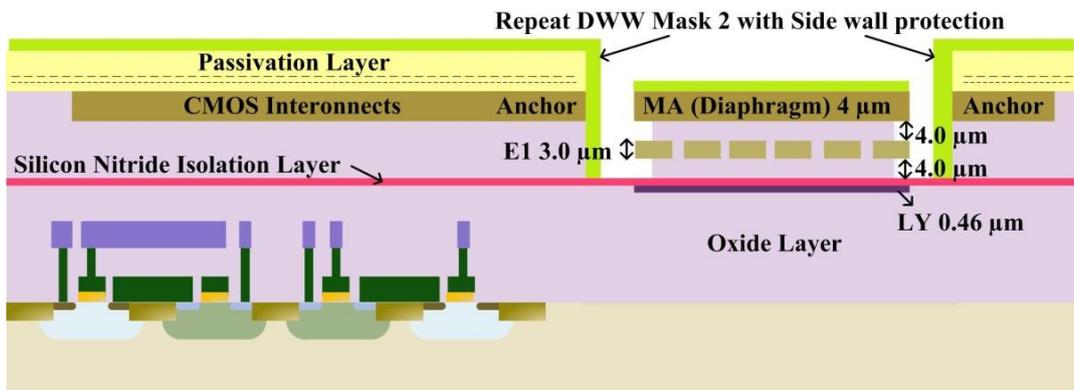
(c)



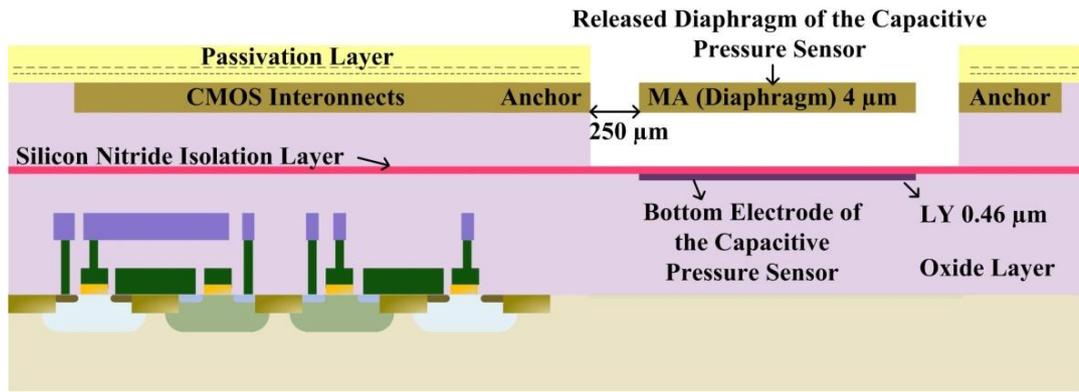
(d)



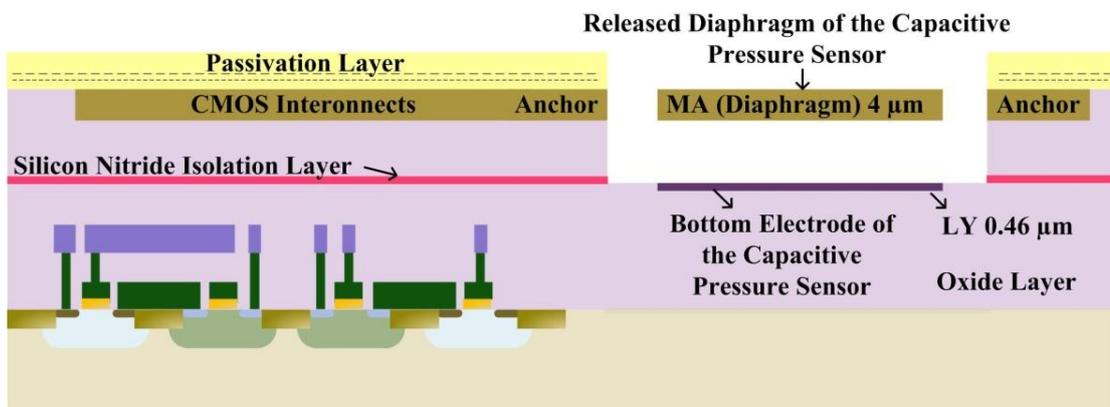
(e)



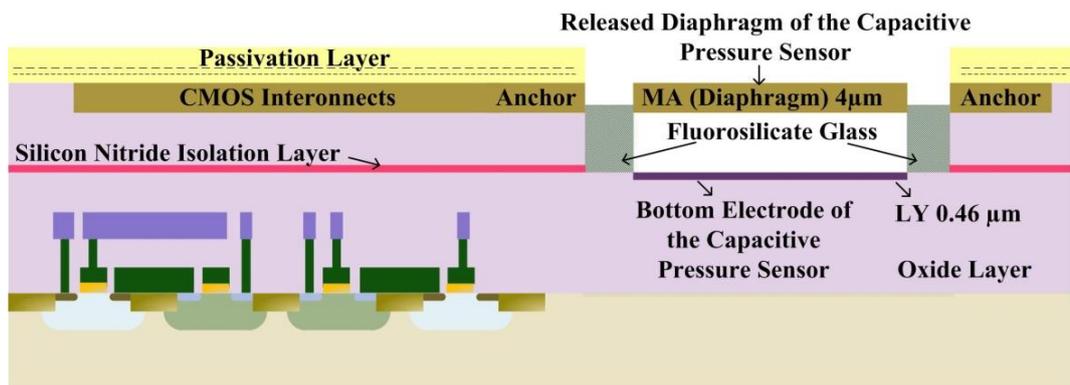
(f)



(g)



(h)



(i)

Fig. 7.7: Cross-section diagrams of the step-by-step MEMS release process, (a) initial CMOS chip with circuitry and unreleased MEMS capacitors, (b) lithography with thick resist (DWW patterning mask 1), (c) after passivation etch, (d) lithography with thin resist (DWW patterning mask 2), (e) after dry trench etch, (f) lithography with thin resist (DWW patterning mask 2 repeat with sidewall protection), (g) after wet etch and following dry etch (composite etch), (h) after post release etch. (i) after post release fluorosilicate sealing

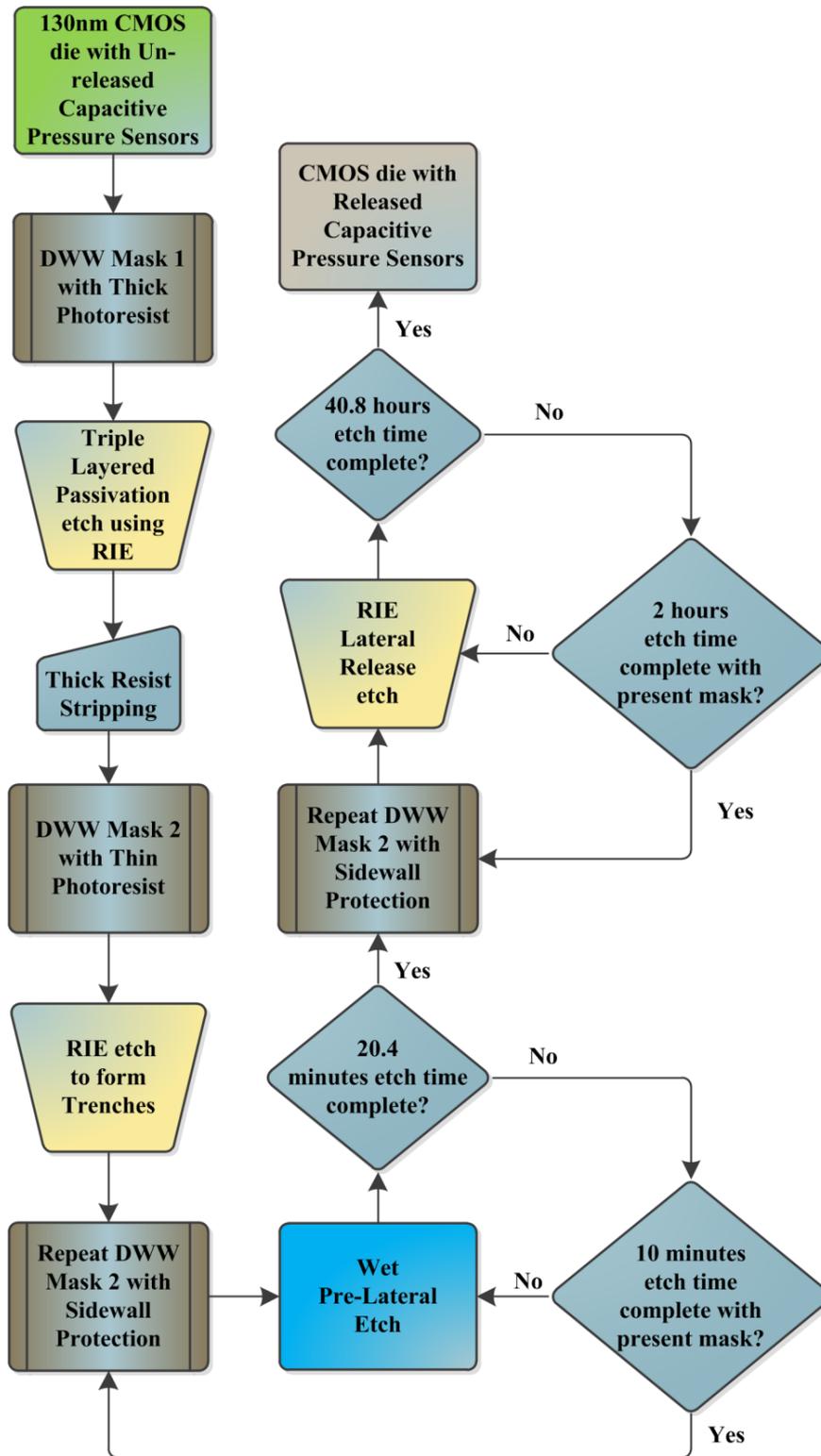


Fig. 7.8: Flowchart of the sensor release process sequence

7.4.5 Post-release sealing

The released devices are next sealed as absolute pressure sensors. The trench areas must be sealed under a certain pressure condition so that the areas under the diaphragm are sealed from external physical quantity. Thus sealing in general, customizes the pressure devices for a desired sensing mode and application as discussed in Chapter 2. Sealing process in this work includes deposition and patterning of Fluorosilicate glass (FSG). First, 12 μm deposition of Fluorosilicate [116] is carried out by PECVD (Plasma Enhanced Chemical Vapor deposition) in moderate Vacuum (@ 0.5 Torr) inside a reactor. The operating temperature of 225°C (*for sealing*) during PECVD deposition process does not degrade the CMOS interconnects and vias. CF_4 (Tetrafluoromethane), oxygen and argon gases with optimized flow-rates of 30, 40 and 10 sccm respectively are fed into the top electrode of the reactor via a shower head. Addition of Oxygen and Argon enhances the deposition rate for this high aspect ratio sealing. Liquid TEOS (Tetraethoxysilane) is introduced as a precursor in to the plasma by bubbling helium through it into the reactor. TEOS being highly volatile at normal room temperature vaporizes readily at the operating temperature so that the risk of stiction effect is negligible. The fluorine source, CF_4 may dissociate yielding higher fluorine ion concentration that would sputter the surface resulting in etching and slow deposition rate. Hence, Hydrogen is also fed into the reactor as it would reduce the free fluorine and minimize the surface contamination of the silicate glass. During this 12 μm deposition process, the FSG will reach just above the bottom edge of the diaphragms inside the trenches yielding a vacuum sealed cavity under the diaphragms as shown in fig. 7.7(i). Next the deposited Fluorosilicate glass is patterned by a separate DWW masking and sputtering using Ar^+ and O^{2-} ions. Mask 2 used for the lateral etch process cannot be repeated here as patterning FSG needs to be accurate so that only the trenches are sealed, otherwise would affect the deformation and the sensitivities of the diaphragms. Thus the FSG sealing is achieved only in the trench areas just above the bottom of the diaphragm and removed from rest of the surface areas. Plasma cleaning is carried out at the completion of the deposition process. The Fluorosilicate sealed rectangular device is shown in fig. 7.9.

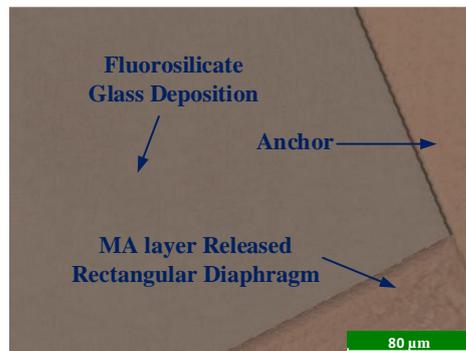


Fig. 7.9: Fluorosilicate glass sealed rectangular diaphragm

7.5 Brief summary of the post-process

The post-processing steps involved in the release and sealing of the sensor devices is briefly listed below for the purpose of clarity:

- Photolithography using Mask 1 (thick photoresist) is done for etching passivation, to expose the diaphragms and trench forming regions as shown in fig. 7.7 (b).
- Triple layer Passivation is etched as shown in fig. 7.7 (c).
- Photolithography using Mask 2 (thin photoresist) is done for etching oxide layer to form trenches on either side of the diaphragms as depicted in fig. 7.7 (d).
- Dry oxide etch using RIE is performed forming trench on either side of the diaphragm membrane.
- Mask 2 lithography is repeated and wet Buffered Hydroxide etch is performed to etch oxide, resulting in micro-vent formation, fig. 7.7 (e) shows the cross section diagram of micro-vent formed and PR stripped chip.
- Repeat lithography using Mask 2 for dry lateral etch of sacrificial oxide is shown in fig. 7.7 (f).
- Dry lateral release etch is performed with repeat lithography for every 2 hours using Mask 2. The fully released diaphragm is shown in fig. 7.7 (g).
- Post release etch is performed to remove the Silicon Nitride etch stop layer as shown in fig. 7.7 (h).
- Trench areas are sealed using the Fluorosilicate glass deposition, to form an absolute MEMS pressure device as shown in fig. 7.7 (i).

7.6 Characterization

Two types of characterization were done to ensure the successful release and the integrity of the MEMS devices. As discussed earlier, at the end of each process step, an AFM study was carried out to validate the expected success of the etch profile. However, further mechanical characterization is necessary to study the final post-process outcome. In addition, to examine critical device parameters such as membrane stiction, electrostatic effect and pull in voltage an electrical characterization study was performed.

7.6.1 Discussion of mechanical characterization

Prior to the start of each etch process; it is necessary to confirm the proper removal of layers by the preceding process. As per earlier discussion, this is achieved by finding the etch (cut) depth at the completion of each process through AFM step height analysis at the junction of etched-unetched region. For this purpose a surface topography, that is, $Z = f(X, Y)$ study is

carried out using the Bruker AFM Dimension Icon instrument. Peak Force Tapping (PFT) mode in the Dimensional Icon equipment makes the analysis easy and provides better resolution compared to conventional AFM. AFM determines the difference in the layer height at the junctions through the traveling time delay of a laser beam, thus providing a more accurate step height than 3D optical profilometer. The equipment setup for the AFM analysis is also shown in figs. 7.10 and 7.11. Fixed frequency of 2 kHz used in this mode avoids probe tuning, unlike conventional Tapping mode. Minimal force is applied on the cantilever tip for controlling purposes, resulting in very low lateral forces, thus yielding less noise when quantizing the data. PFT operates under the ScanAsyst feedback technology that uses special algorithms and feedback systems. Image quality is constantly monitored during scanning. Parameters such as setpoint, gain, scan rate, range, and noise threshold are adjusted to maintain a low force on the cantilever tip. The system setup is provided in table 7.3. The maximum scan size is set to 90 μm of which the midpoint is set at the junction of the etched window to get minimal artifacts in the images. The probe XY position is set to scan 45 μm distances from the etched window junction towards the unetched region on the surface of the die and further 45 μm from the etched window towards the etched region. ScanAsyst converts the tapped data into the “quantitative nanomechanical mapping” (QNM) [117]. Analysis is repeated several times to obtain better results. Fig. 7.12 shows different AFM images obtained during analysis. Fig. 7.12 (a) shows the scan size region with cantilever probe tip, fig. 7.12 (b) shows the 3D step height analysis result after partial polyimide etch, whereas, figs. 7.12 (c) and (d) shows the results of the step height analysis performed after two different process steps. Table 7.4 summarizes the step height measured at various process steps.

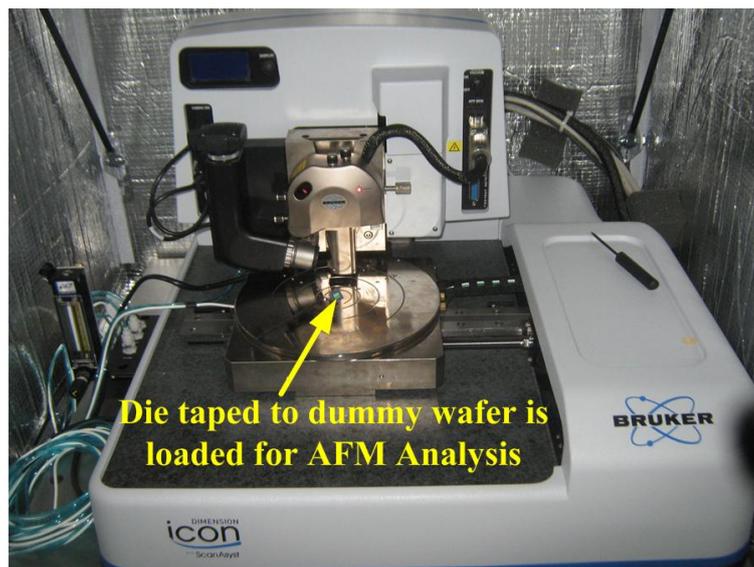


Fig. 7.10: Bruker-Dimension Icon AFM system loaded with the specimen

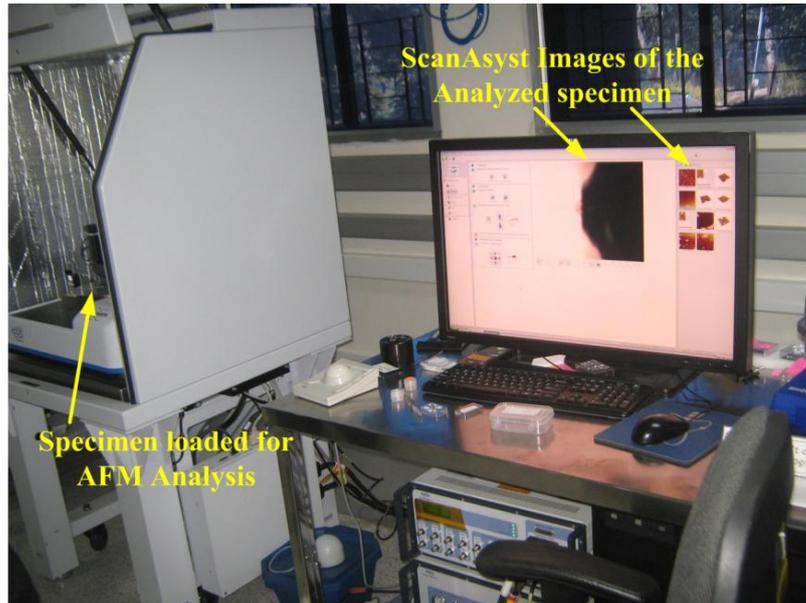
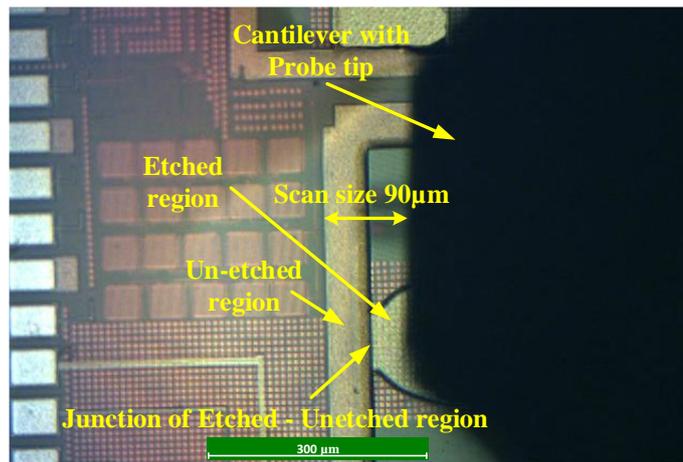
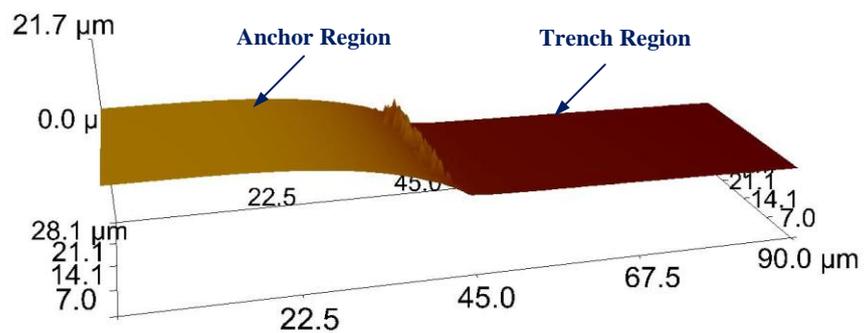


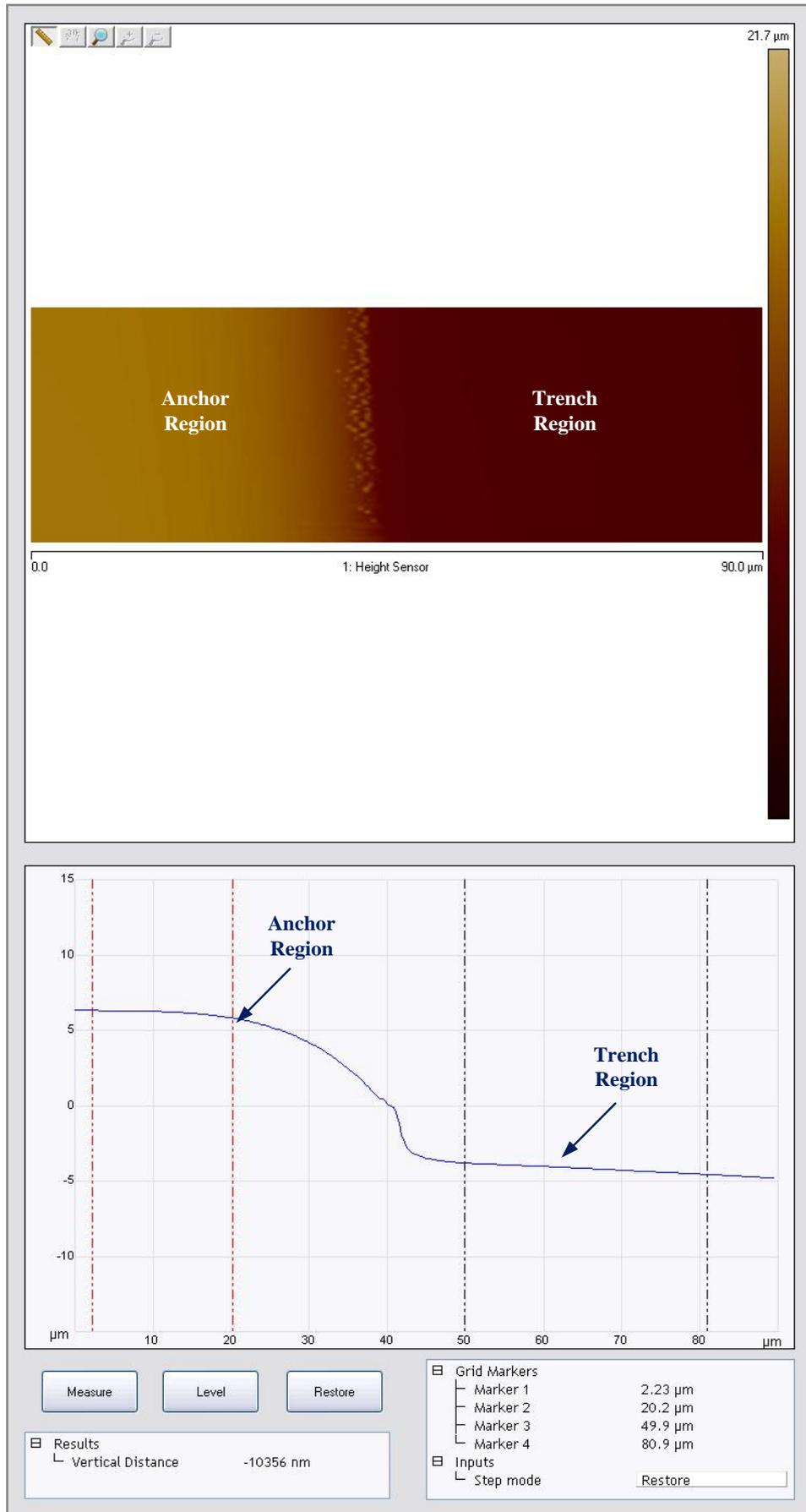
Fig. 7.11: The complete AFM analysis system



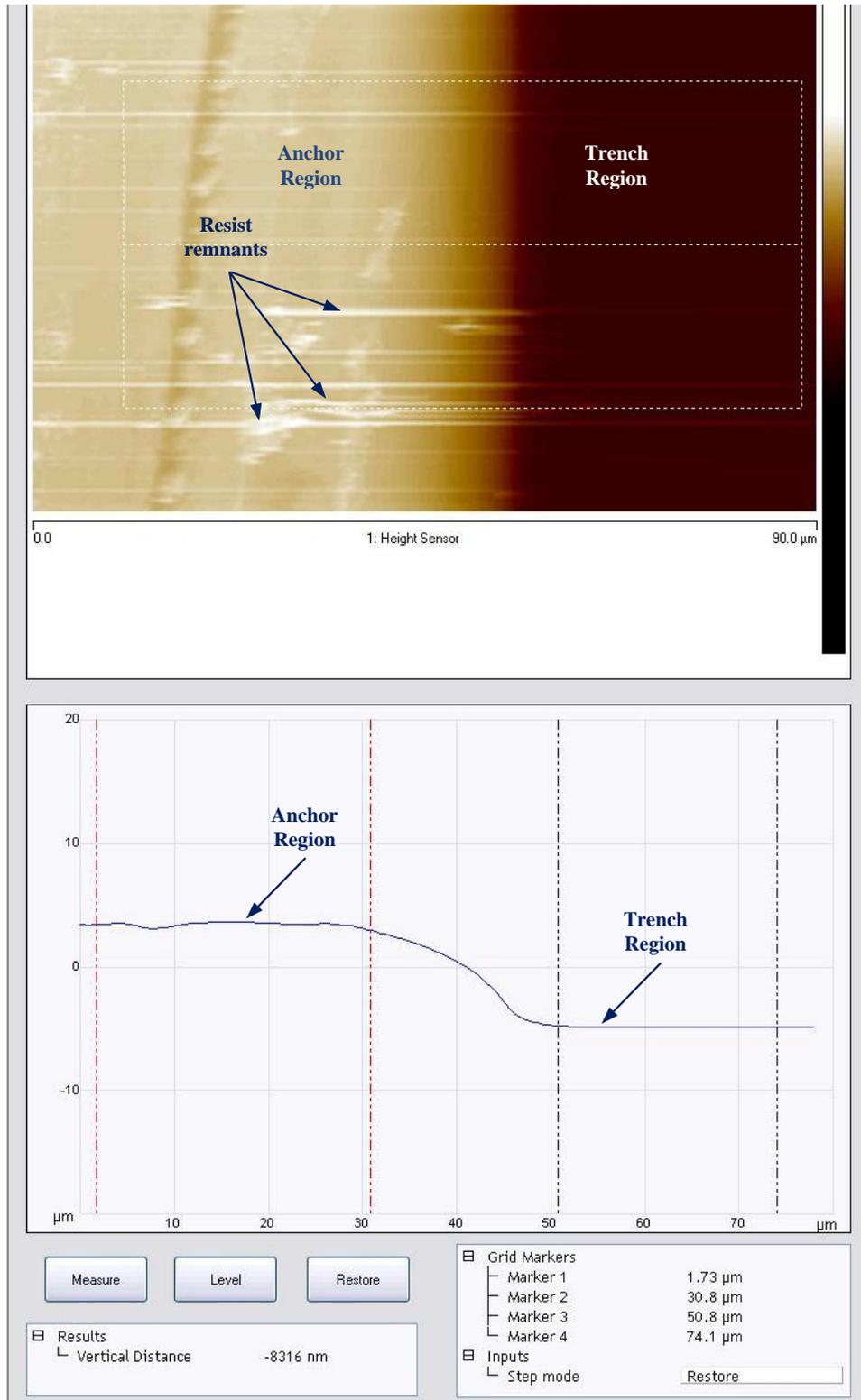
(a)



(b)



(c)



(d)

Fig. 7.12: Atomic Force Microscope step-height analysis, (a) Chip image from AFM microscope after partial Polyimide etch, (b) Step height in 3D after partial Polyimide etch, (c) Top-view of Polyimide etch and step height analysis plot after partial Polyimide etch, and, (d) Top view (white patches indicating resist remnants after resist strip-off) and step height analysis plot after complete passivation etch

Table 7.3: Dimension Icon System Setup – DIM 4000

| Scanning Parameters | Optimized Value |
|--|--|
| Engage X Y & Z Position | -19783.4 μm , 42151.3 μm & -55 μm |
| X,Y & Zsensitivity | 141.3, 134.6 & 41.6793 nm/V |
| X,Y & Z range | 90,90 & 10 μm |
| Scan Size | 90000 nm |
| Full Range Sensor Gain | 0.6 |
| Aspect Ratio | 1:1 |
| Step XY period | 0.005 |
| Step XY Size | 300 |
| Scan Rate | 1.0016 Hz |
| Engage Setpoint & Force Data Points | 0.95 & 64 |
| Calculation Period & Unload Fit Region | 60 & 0.7 |
| Peak Force Engage Setpoint, Peak Force Amplitude & Lift Height | 0.15 nN, 100 nm & 300 nm |
| Peak Force Max Amplitude & PFT Frequency | 15nm & 2 KHz |
| Scan Max Optimizing Time ScanAsyst Noise Threshold | 30 minutes & 0.5 nm |

Table 7.4: AFM Analysis Results

| S.No. | Specimen Analyzed State | Step Height |
|-------|------------------------------------|---|
| 1 | First Resist Coated Specimen | 7 μm |
| 2 | Polyimide Etched Specimen | 8.6 μm (resist is attacked) |
| 3 | Nitride Etched Specimen | 7.8 μm (resist is further stripped) |
| 4 | Passivation Oxide Etched Specimen | 6.3 μm (resist continued to strip off) |
| 5 | Resist Stripped Specimen | 4.3 μm |
| 6 | Trenched Specimen (Resist removed) | 8.3 μm |

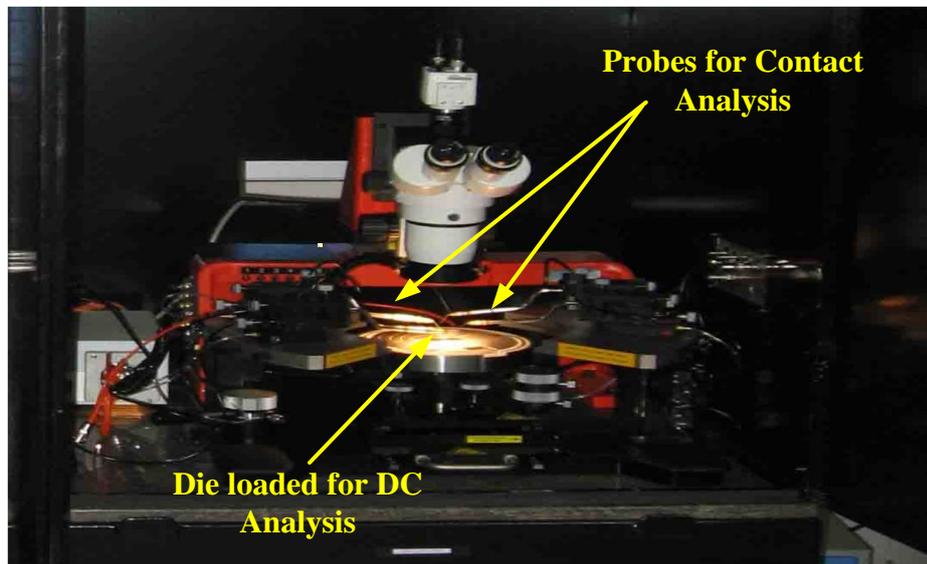


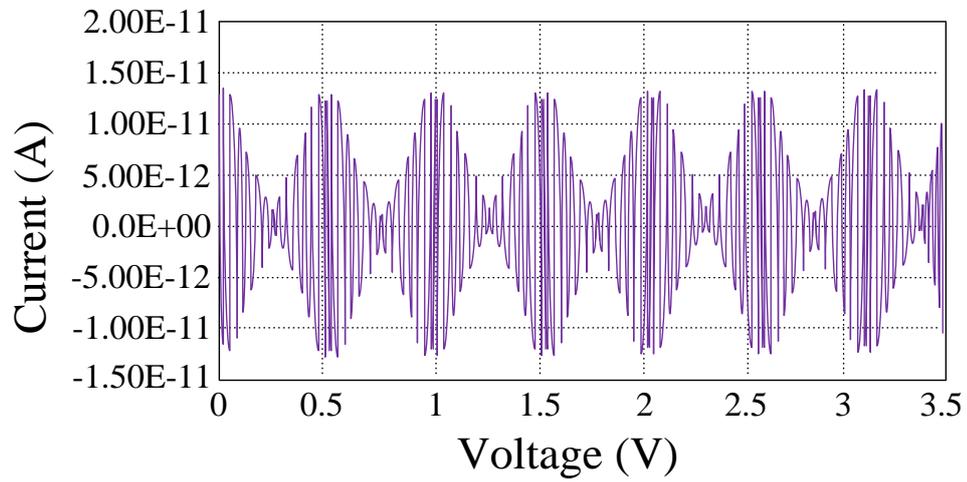
Fig. 7.13: DC Probe Station: Agilent Device Analyzer B1500A with 5 MHz pulsed source

7.6.2 Discussion of electrical characterization

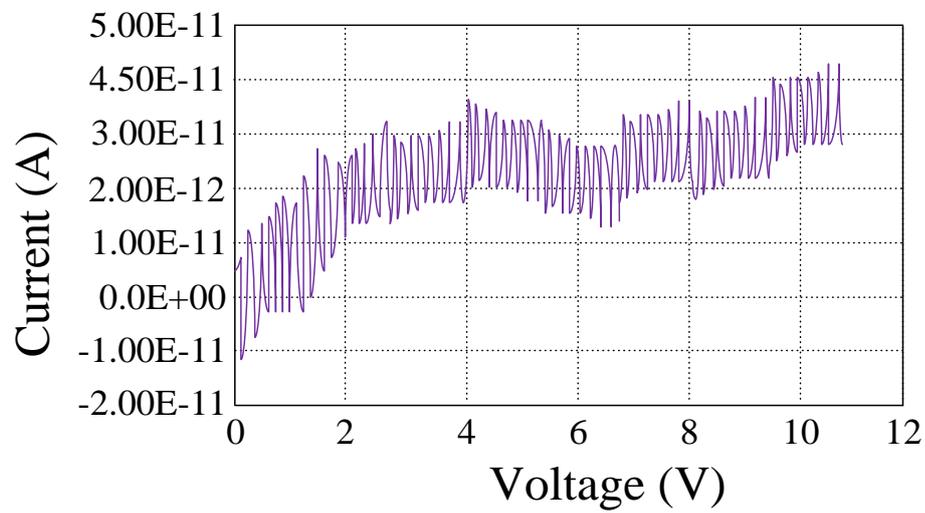
The critical phase in passivation etch is to determine the successful complete exposure of MA metal of both the diaphragms (top electrodes of the capacitive sensor). Even though variations in the color and the surface texture of the layers can to some extent reveal the cut opening, characterization is necessary. The full exposure of the diaphragm can be verified through electrical conductivity analysis. The electrical characterization was carried out using the Agilent device analyzer B 1500A with 5 MHz pulsed source as shown in fig. 7.13. Probing two opposite ends of the diaphragm, with a varying DC voltage, revealed whether the device top metal is exposed or not. Current and resistance measurements at several process steps are shown in figs. 7.14, 7.15 and 7.16. Fig. 7.14 (a) shows the contact analysis before the Polyimide etch (corresponding to Fig. 7.7 (b)) while fig. 7.14 (b) shows the analysis after the Nitride etch. In fig. 7.14 (a) even with 10 V DC there was a negligible current flow, whereas in fig. 7.14 (b) there was a slight deviation in the current graph (slightly larger current flow only) indicating that oxide layer is still present above the metal diaphragms. The ripples in fig. 7.14 can possibly be contributed by the measurement uncertainty in the pico-ampere range due to probe traces at the two end positions on the diaphragm surface. Figs. 7.15 (a) and (b) provides the measurements of the resistance and the current respectively, after the oxide etch (corresponding to Fig. 7.7 (c)). It can be seen that even for a potential as low as 1 V across the diaphragm surface a current of 0.1 A flows, indicating the complete exposure of the MA layer of the diaphragm. The noise flow (leakage current) for the experimental setup measured using a 1 V step input with probes held in the air was around 100 fA. The resistance is calculated using the applied voltage and the measured current. The calculated resistance was thus found to be very low in the order of a few ohms after the oxide etch (as shown in fig. 7.15 (a)). The small ramp (linear rise) in the measured resistance with voltage is mostly caused by the heating of the diaphragm due to high current flowing through it, further the instrument and measurement system tolerance also contributes to the ramp.

The diaphragm release was confirmed by the collapse of the interleaving copper mesh (E1 layer of the BEOL stack), however, further verification was also carried out by a two-point cross-probing of the diaphragm and LY layer contacts. Negligible measured current along with high resistance indicates the full release of the diaphragm as shown in fig. 7.16 (corresponding to fig. 7.7 (h)). The presence of any intervening oxide layer would have resulted in a current in the order of μA at a high applied voltage of 12 V. Also, the measured resistance in the order of Giga Ohms confirmed that no stiction occurred between the MA and LY layers. The measured pull-in voltages were 38.8 V and 39.2 V for the elliptic and rectangular devices respectively. Also the resistance (between the MA and LY plates) at pull-in (just before *touch-down*) was

13.57 Mega Ohms and 16.74 Mega Ohms respectively, for the elliptic and rectangular diaphragms (including the diaphragm anchors).

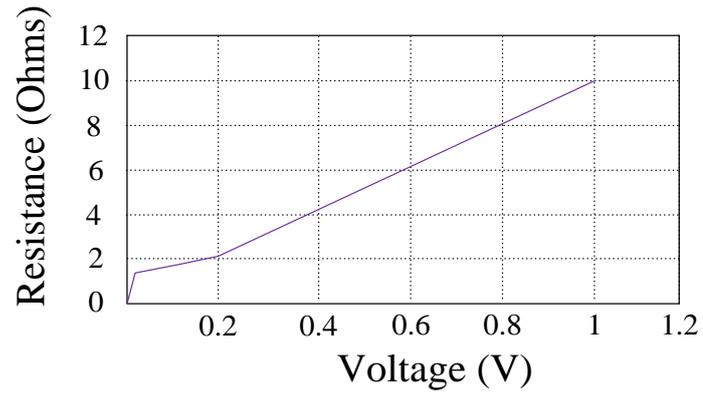


(a)

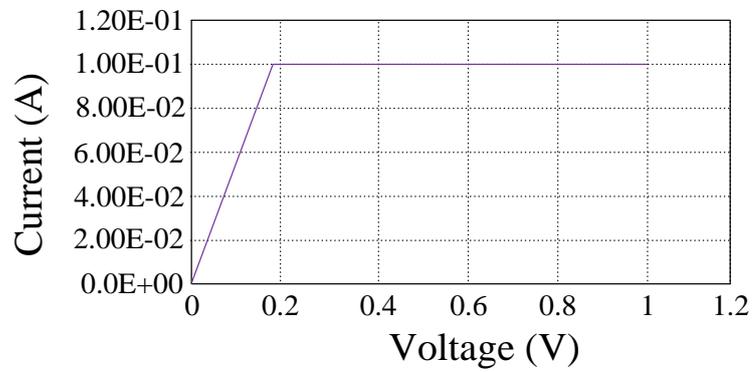


(b)

Fig. 7.14: Electrical contact analysis, (a) before Polyimide etch (with full passivation intact), (b) after Nitride etch (with Oxide layer still present)



(a)



(b)

Fig. 7.15: Electrical contact analysis of exposed diaphragm after etching the oxide layer of passivation,

(a) Resistance variation, (b) Current variation

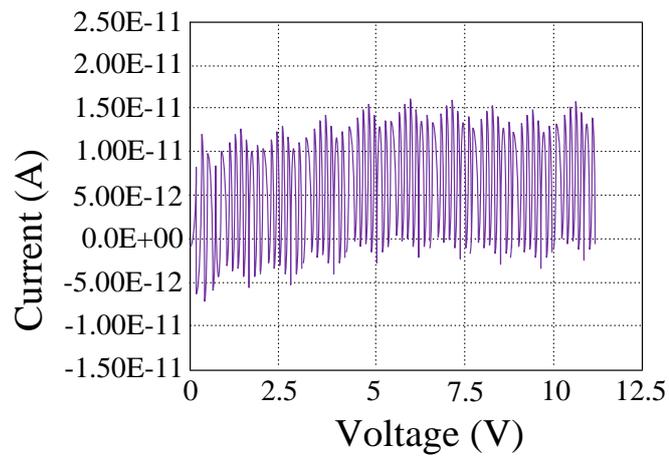


Fig. 7.16: Electrical contact analysis between MA (top electrode) and LY (bottom electrode)

7.7 Conclusion

The successful MEMS capacitive sensor release etch employing a mixture of wet and Plasma dry etch on a 8-metal BEOL 130 nm standard IBM CMOS process has been demonstrated. Lateral etch (under etch) of 125 μm from opposite sides between the diaphragm (*top MA electrode*) and the bottom plate (*LY electrode*) was achieved without damaging the anchors and the underlying CMOS signal conditioning circuitry. The highly compact 8 metal layer CMOS MEMS allows smaller line-width and hence offers lower parasitic effects compared to those reported in [118]-[127] for micro-systems design. An optimized technique of resist stripping without damaging the exposed Aluminum diaphragms was also verified. The comparatively low cost CHF_3 plasma etch yielded a smooth surface with no residues, hence avoiding the need for strong wet cleaning chemicals that attacks Aluminum diaphragms and are associated with stiction effects. The fabricated intermediate copper mesh test structure (*E1 layer* of the BEOL stack) falls off during the release etch, thus confirming the full release of the diaphragm. As the diaphragm is partially transparent while viewing through the microscope, the absence of copper mesh layer is easily ascertained. There was no requirement for an expensive scanning electron microscope analysis. Thermal budget for the 0.13 μm CMOS circuitry is taken into consideration and any process that required more than 225°C temperature is eliminated from the post-process flow in order to protect the on chip CMOS circuits. The released sensor capacitors were mechanically and electrically characterized using step height and electric contact analysis respectively. Experimental measurements of the transduction behavior as an absolute capacitive pressure sensor were also carried out in terms of sensitivity, dynamic range, hysteresis and repeatability. The obtained test results indicate that the elliptic structured device has a better overall performance in terms of sensitivity and dynamic range compared to the rectangular device. Detailed descriptions of the results are given in the next Chapter.

Chapter 8

Experimental Analysis and Comparison

8.1 Introduction

The two CMOS integrated sensor devices developed from different process technologies are experimentally tested to validate their performances. These two dies are wire-bonded on to two different general purpose PCB boards. The required test environment and equipment setup for both the devices are almost similar; however as their structural design and dimensions were unique, different setup systems with different test pressure ranges are preferred. The exclusive setup arrangements and test methodologies for these two sensor micro-systems are illustrated elaborately in the following sections; nevertheless, for the purpose of clarity, an overview of the experimental test setup is shown in fig. 8.1. Nitrogen gas was used in both cases to induce pressure loads on the diaphragms. A pressure calibrator with an option of temperature controller can be calibrated for the desired test pressure and temperature ranges. All measured values are interfaced to the PC for faster data acquisition; the test results are displayed in the PC by means of a graphical user interface (GUI) for better understanding of the output signal variation with applied pressure. A high precision LCR meter, interfaced between the electrical circuitry of the device under test (DUT) and a PC helps in the speedy experimental analysis. Detailed descriptions of the obtained test results were given in section 8.2 and 8.3. Comparisons of the measured test results between both the fabricated diaphragms, as well as, with the previously reported works were also done in section 8.4. The observed performances were promising for both the designs.

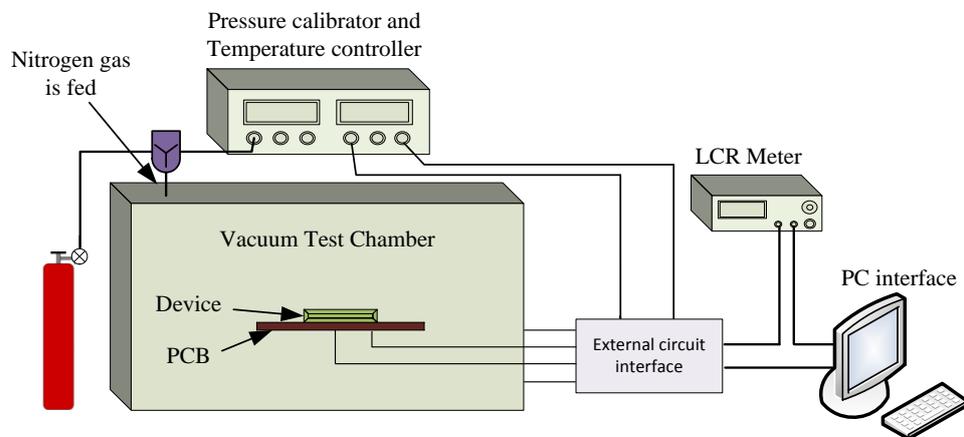


Fig. 8.1: Overview of the experimental setup

8.2 SiGeMEMS capacitive sensor experimental analysis

The microscopic photograph of the integrated sensor die is shown in the fig. 8.2. The underlying CMOS readout circuit and interconnects were not apparently seen in the microscopic observation due to the presence of top layers such as the sensor element, anchors and foundry fill dummies. As the release process has been done already during the MEMS process at IMEC, no post-processing is necessary. Experimental tests were straightaway conducted after custom-sealing the device, to study the performance of the sensor micro-system. According to the thin plate theory, the pressure sensitivity is expected to be linear for half the membrane thickness; hence, the 4 μm thick diaphragm can yield linear pressure sensitivity up to a displacement of 2 μm . The vacuum cavity below the diaphragm is 3 μm thick and so do the distance between the plates, therefore electrostatic pull-in will have negligible effect on the performance of the devices. The microscopic measurements of semi-minor and semi-major axis of the elliptic diaphragm were found to be 280 μm and 485 μm respectively. The entire area of integrated sensor die measures 4 mm \times 4 mm. The diced chip is packaged using the versatile DIP plastic packaging technique, with an option of ESD taped plastic lid as shown in fig. 8.3, the plastic lid can be pulled open for exposing the sensor to the physical quantity. The packaged micro-system is then soldered to the PCB for establishing proper connections with external testing equipments. Custom PCB design that suits the DIP packaging is done in Altium designer CAD tool. The integrated chip with the PCB is kept in a vacuum chamber for experimental analysis to determine device performance such as sensitivity, linearity, hysteresis and repeatability. The capacitive measurement under different pressure ranges are made possible by lead transfer from the chip to outside LCR meter through an electrical interface of the vacuum chamber. A constant 1.4 V regulated power supply is also designed to power the on-chip signal conditioning circuit and also to excite the capacitive pressure sensor. A vacuum pump was utilized to form the initial vacuum inside the vacuum chamber; further, nitrogen source was used to increase the pressure inside the testing chamber from the initial vacuum condition. Pressure test calibration equipment, shown in fig. 8.4 controls the vacuum pump and nitrogen gas source.

The observed sensor capacitance and the output voltage of the sensing circuit under various pressure ranges are depicted in figs. 8.5 and 8.6. The linear sensing range of the device during pressure-up was from 4 to 900 hPa, with the device sensitivity of 0.65 fF/hPa. During the down pressure, linear response was observed between 900 hPa and 7 hPa, a marginally high sensitivity of 0.69 fF/hPa was also noticed. The observed device hysteresis, repeatability and nonlinearity were 0.038%, 0.024% and 1% respectively. Measuring the output voltage of the amplifier with varying pressure loads, the overall sensitivity of the sensor system was calculated to be 0.12 mV/hPa. A wider dynamic range of around 900 hPa was also noticed. The test results closely follow the simulation results, the slight deviation in the linear sensing range and overall

sensitivity may be due to the diaphragm residual stress. Further, variation in surface capacitance due to the sealing process, wire bonding and packaging stresses may also have contributed to the deviation in practical test results. Experimental test results revealed that the sensor's cavity has some amount of residual pressure, even though the sealing is done under nominal vacuum conditions. This is due to the possibility of the process gas being trapped inside the cavity during the sealing process. Residual pressure test (pressure scanning test) conducted by lowering the pressure below 4 hPa indicated a residual pressure of around 2 hPa. This is due to the outward deformation of the diaphragm [128] with the pressure inside the cavity becoming higher than the applied pressure after becoming just equal to it. Thus the reliable minimum detectable pressure (MDP) is limited to around 4 hPa. At a very low applied driving voltage of 33.2 V, the perforated diaphragm touches the bottom electrode due to electrostatic force. This is found to be 64% less than the other similar geometry non-perforated diaphragm (51 V pull-in voltage). The low pull-in voltage proves that the perforated diaphragm has low internal stress and stiffness, which is a vital parameter for sensor's performance. The measured linear sensing range, sensitivity and pull in voltage of the device demonstrate that a vacuum sealed perforated elliptic diaphragm fabricated using poly-SiGe material and anchored at semi-major axis yielded increased performance with minimal residual cavity pressure.

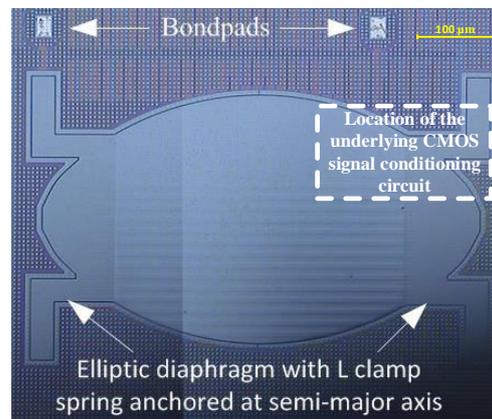


Fig. 8.2: Microscopic photograph of the integrated SiGeMEMS sensor die

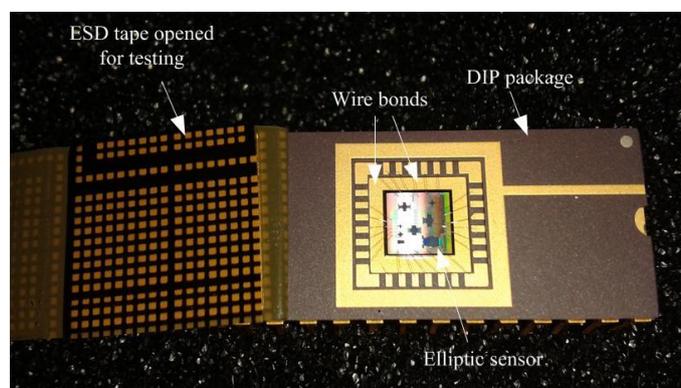


Fig. 8.3: Packaged SiGeMEMS micro-system with option of ESD taped lid

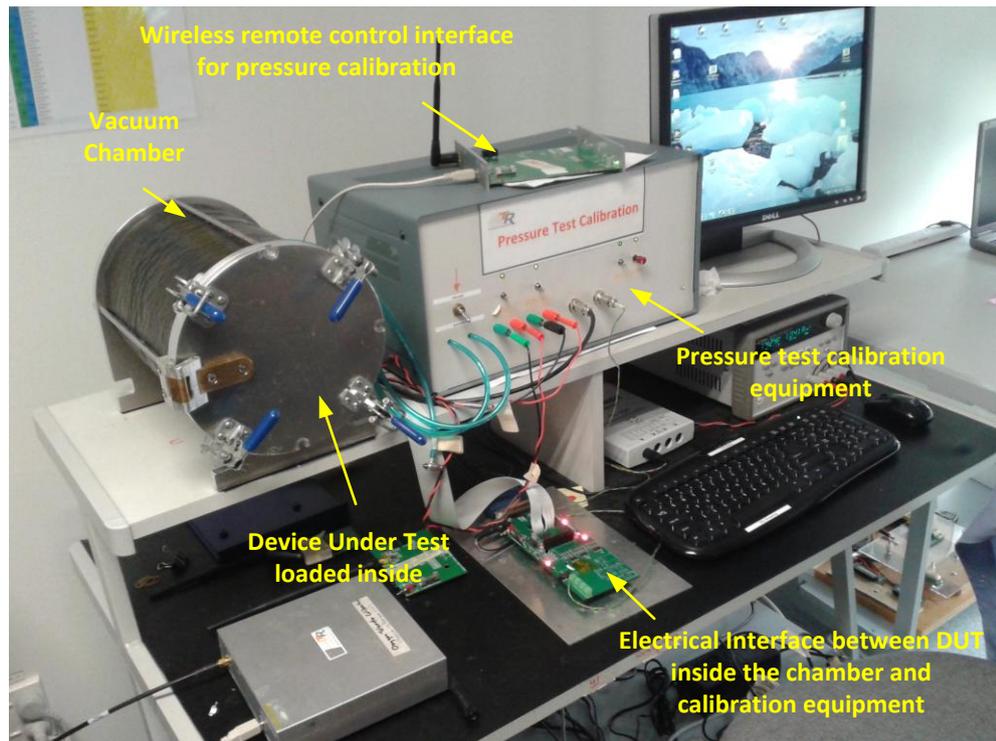


Fig. 8.4: SiGeMEMS chip experimental test setup

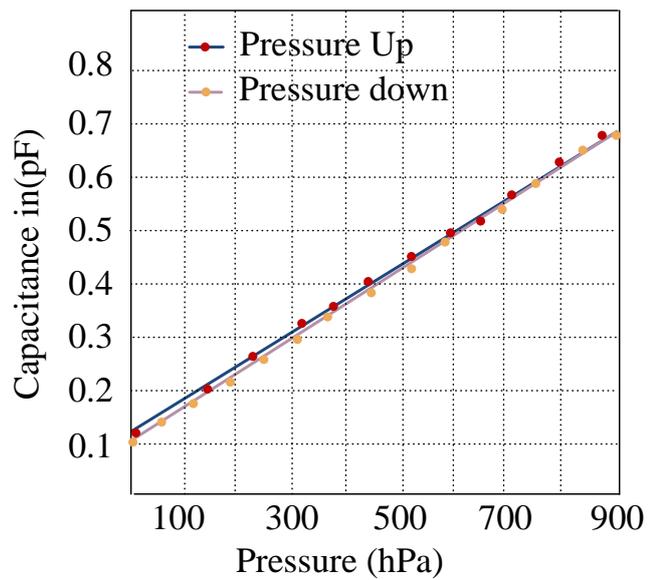


Fig. 8.5: Capacitance variation with applied pressure load

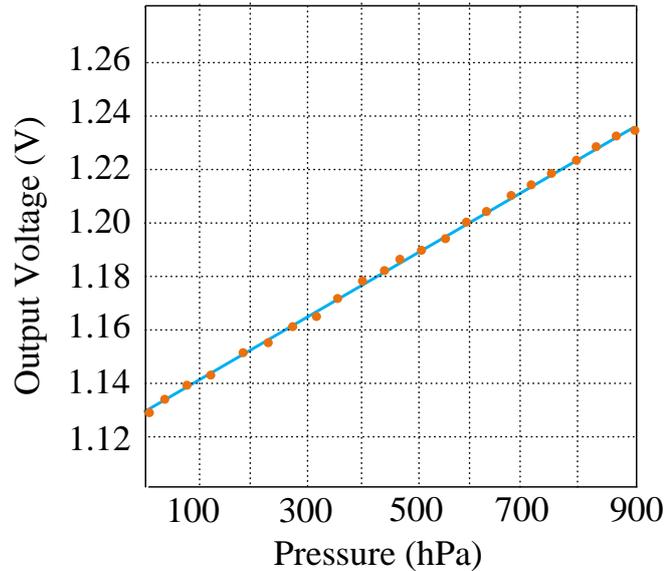


Fig. 8.6: Voltage output of the sensor micro-system with applied pressure

8.3 Experimental test on standard IBM CMOS integrated MEMS devices

The performances of CMOS integrated MEMS capacitive pressure sensors, processed in standard IBM 130 nm CMOS MPW (multi project wafer) run were validated with two stages of experimental tests. Out of 40 chips ordered from the foundry, 20 were packaged and 20 were naked dies. The dies with the passivation have to undergo post processing for release of the device membranes, as no exclusive MEMS process was performed by the foundry. In the first stage, preliminary test to study the sensor readout performances were conducted with the packaged IC. The foundry packaged chip MOSIS V25F-BF has designated pin access to the sensor readout inputs and outputs. As MEMS sensor device membranes have not yet been released and are fully enclosed within the plastic package, it will not provide any signal input to the CMOS circuitry; therefore an external sinusoidal excitation is needed for this preliminary test. This is achieved by means of a simple function generator (FG). A naked die could also have been wire bonded onto the PCB for this initial test setup; however, as the devices are not released at this stage, PCB design would be of no advantage. Moreover, as the die is fully covered with passivation, it will still not function as expected; hence using the packaged chip at this stage for analysis is better. Next, a complete study of the micro-sensor system was conducted as the second stage of experimental analysis immediately after the release of MEMS devices (described in Chapter 7). The post-processed die was wire bonded onto the PCB and then subjected to pressure load analysis. Performance measurements such as sensitivity, linearity and dynamic range of the micro-sensor system were then conducted.

8.3.1 Preliminary test on sensor readout

The designed and fabricated IC consists of two capacitive MEMS pressure sensor integrated with CMOS sensor readout. Different stages of sensor readout include sensor startup circuitry, chopper stabilized transconductance enhanced RFC opamp, 4th order Gm-C Low pass filter and a low impedance self biased buffer. Pin connections were assigned to all the intermediate stages of the sensing circuit for the purpose of troubleshooting. Moreover, the die was also designed with dedicated pins for both the sensors to allow external access, for the purpose of measuring the varying capacitance under applied pressure ranges. Further, the designated pins allow the external signal conditioning circuit to be connected for calibration purposes; however, device measurement is left for the second stage of analysis. The expected outcomes of the first stage of testing are high voltage gain and low noise output signal with better load driving capability of up to 4 pf.

8.3.1.1 Chopping signal generator circuitry

The chopper stabilized g_m enhanced RFC opamp, requires four signals for driving the transmission chopper network. Two high frequency signals that are out-of phase will have to drive the horizontally connected two PMOS and two NMOS transistors of the chopper network, while the other two out-of phase low frequency signals will drive the vertically connected PMOS and NMOS transistor pairs. An external chopping frequency generator is built with HEF4060B [129] (Oscillator & counter IC) to generate these four chopping signals, as the conventional function generators are limited to two output channels. A 2 MHz crystal clock (IQD FREQUENCY PRODUCTS - LF SPXO000118 - CRYSTAL OSCILLATOR) is utilized for the stable square wave generation. The 14 stage counters of the HEF4060B IC will divide the high frequency crystal oscillator signal to achieve the required frequency pulses of 10 KHz and 100 KHz. These signals will drive the modified chopper circuit leading to modulation of signal at the input of g_m doubling RFC opamp. The pin details of the IC are shown in fig. 8.7. The internal circuitry of the counter IC is shown in the fig. 8.8. The external circuit connections between the IC and the crystal oscillator are done as shown in fig. 8.9. The output pulses of HEF4060B being 5 V are dropped down to 1V by means of a series resistive network. R_{bias} in fig. 8.9 is varied from 100 K Ω to 1 M Ω to obtain the desired output frequencies. The 100 KHz pulse is obtained from pin no. 13 and 10 KHz from pin no. 3 of HEF4060B. These pulses are inverted using the 7404 inverter IC to obtain the out-of phase pulses. These four chopping pulses modulated the amplifier's low frequency input signal with negligible spikes. Thus low input referred noise is achieved and the overall distortion is reduced. The same circuitry was employed to drive the chopper demodulator at the output stage of the RFC opamp for efficient recovery of the input sinusoidal signal.

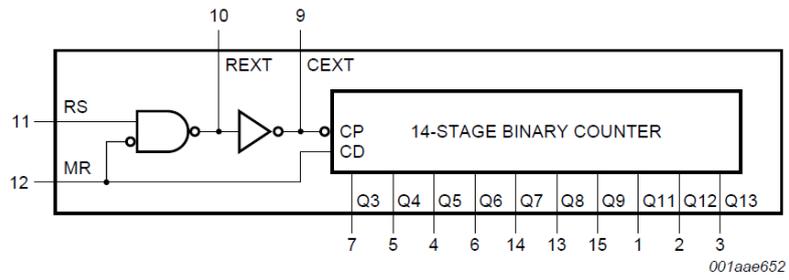


Fig. 8.7: Oscillator diagram of HEF4060B [129]

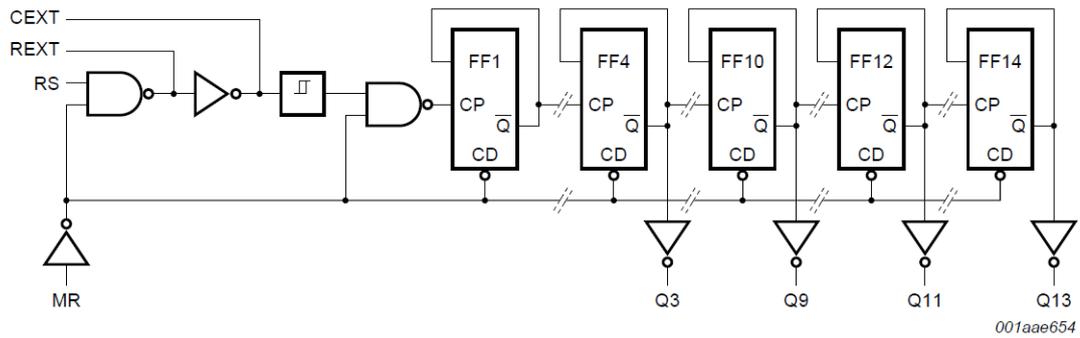


Fig. 8.8: Logic diagram of HEF4060B [129]

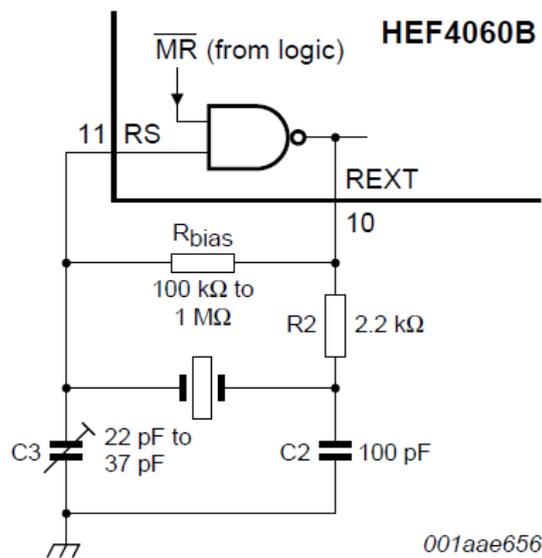


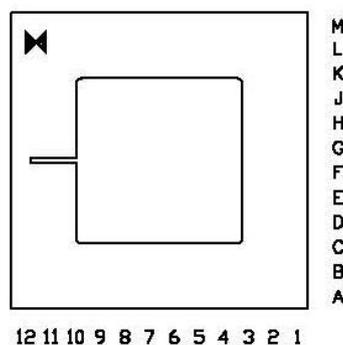
Fig. 8.9: Crystal oscillator circuit diagram using HEF4060B [129]

8.3.1.2 System test circuitry

The IC is packaged using the MOSIS offered standard 108 pin grid array package (PGA 108M) with a cavity size of 0.350 square inches. This ceramic package is manufactured by Kyocera with the drawing equivalent KD-P89113, as shown in figs. 8.10 and 8.11. The IC includes multiple projects for efficient academic cost reduction purpose; hence package having more number of pins was opted. This work however uses only 32 pins with an option of analyzing the readout circuit stage by stage. Few additional bondpads were intentionally designed to form two sets of probe-pads (12 bondpads) that suit die probing for intense analyzing. The bondpads to bondpins connections are shown in fig. 8.12, highlighted areas shows the total number of bondpins used in this work. The location of the devices interconnected with the underlying readout CMOS circuit, in the chip area of 3 mm × 3 mm is also highlighted. The size of the entire micro-system including the bondpads is around 1 mm × 1 mm, which is significantly less. The packaged IC is mounted on a ZIF socket (figs. 8.13 and 8.14) for external circuit interconnection feasibility. The external circuitry shown in fig. 8.15 and fig. 8.16, which is built on the breadboard is then connected with the integrated readout circuit along with necessary test equipments.

| | | | | | | | | | | | | |
|---|----|----|----|----|----|----|----|-----|-----|-----|-----|----|
| M | 82 | 84 | 86 | 89 | 92 | 95 | 98 | 101 | 104 | 107 | 108 | 1 |
| L | 81 | 83 | 85 | 88 | 91 | 94 | 97 | 100 | 103 | 106 | 2 | 3 |
| K | 80 | 79 | 78 | 87 | 90 | 93 | 96 | 99 | 102 | 105 | 4 | 5 |
| J | 77 | 76 | 75 | | | | | | | 6 | 7 | 8 |
| H | 74 | 73 | 72 | | | | | | | 9 | 10 | 11 |
| G | 71 | 70 | 69 | | | | | | | 12 | 13 | 14 |
| F | 68 | 67 | 66 | | | | | | | 15 | 16 | 17 |
| E | 65 | 64 | 63 | | | | | | | 18 | 19 | 20 |
| D | 62 | 61 | 60 | | | | | | | 21 | 22 | 23 |
| C | 59 | 58 | 51 | 48 | 45 | 42 | 39 | 36 | 33 | 24 | 25 | 26 |
| B | 57 | 56 | 52 | 49 | 46 | 43 | 40 | 37 | 34 | 31 | 29 | 27 |
| A | 55 | 54 | 53 | 50 | 47 | 44 | 41 | 38 | 35 | 32 | 30 | 28 |

(a)



(b)

Fig. 8.10: (a) Bottom view of PGA 108M package (b) Top view of the packaged IC [130]

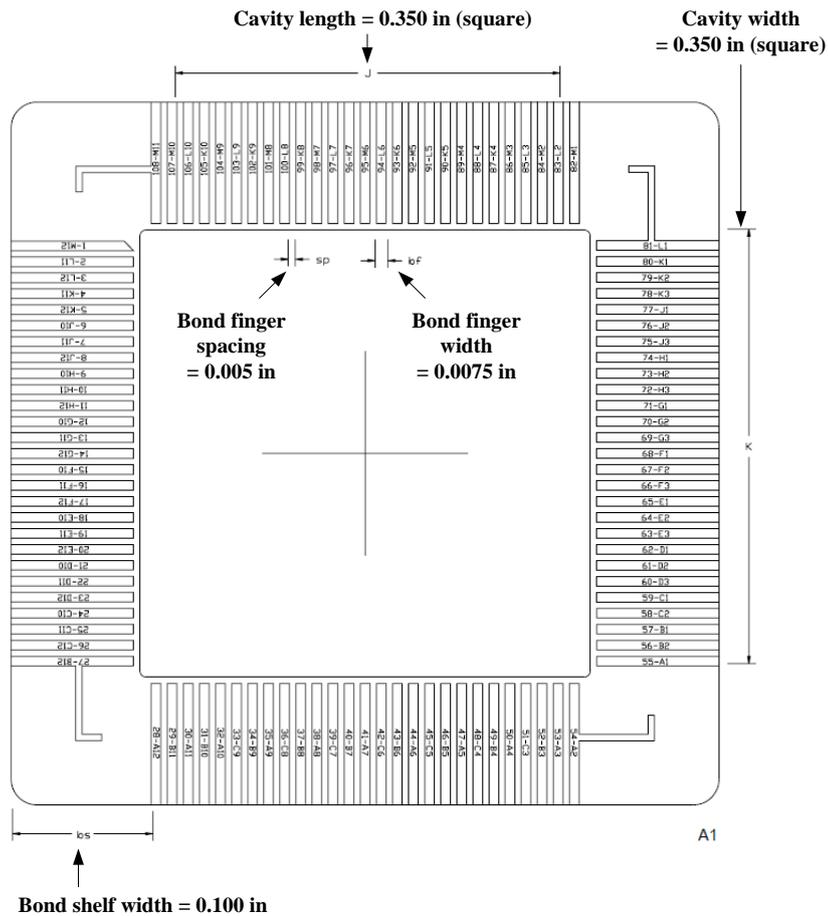
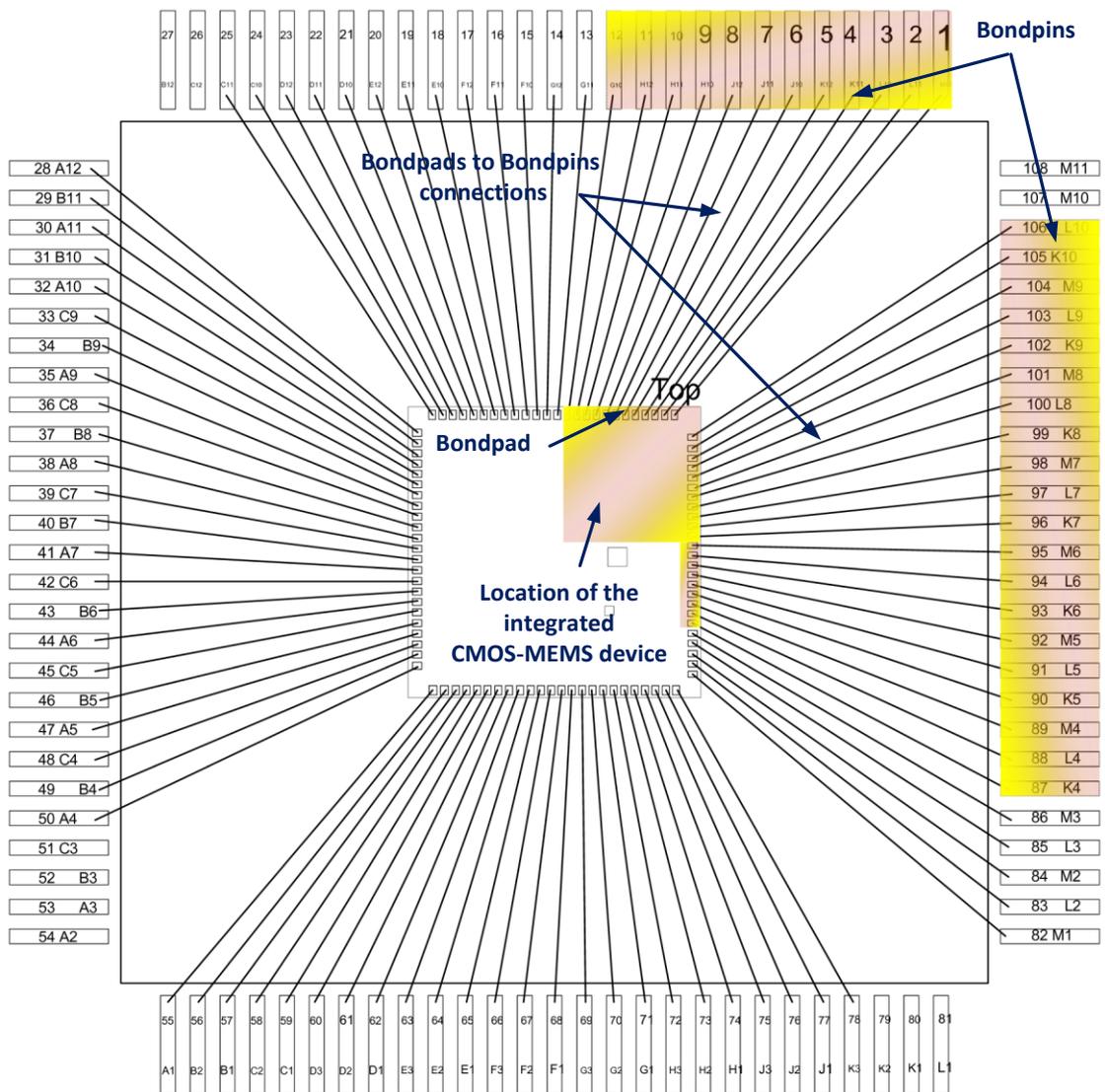


Fig. 8.11: Drawing equivalent of PGA 108M package [130]

In this first phase of the preliminary test, chopper stabilized g_m doubling RFC opamp is tested with the setup shown in fig. 8.15. RFC opamp is the main functional stage in the signal conditioning circuitry; hence, intense testing is performed to verify whether intended gain and linearity is achieved. A single supply V_{DD} of 1.2 V from a regulated precision power supply drives the signal conditioning circuit. The external chopping frequency generator circuitry and the inverter circuit, requiring a driving voltage of 5 V is powered by an independent highly stable Regulated Power Supply (RPS). A precision sine wave signal generator drives the differential inputs of the signal conditioning circuit at pins 9 & 10. The output of the signal conditioning circuit is analyzed using a Tektronics TDS2012 Digital storage oscilloscope (DSO) featuring 100 MHz 1 GS/s. An ESCORT EDM-89S Digital multimeter (DMM) is utilized to calibrate the signal generator circuitry that drives the chopper network. The V_{pp} (peak to peak voltage) of the output signal is also measured using DMM. The signal conditioning circuit is expected to amplify the micro-volt range output of the sinusoidal input signal to milli-volt range. The amount of output differential voltage variation with respect to the differential input voltage is measured at pins 3 and 4 of the designed IC; the corresponding differential gain is calculated to be around 105 dB.



| | |
|--|---------|
| Qty: 20 req'd | PGA108M |
| Customer Providing Diagram | |
| Minimum pad size: 95 x 62; minimum pad pitch: 100 um | |
| | |

Fig. 8.12: Bonding diagram showing bondpads to bondpins connections

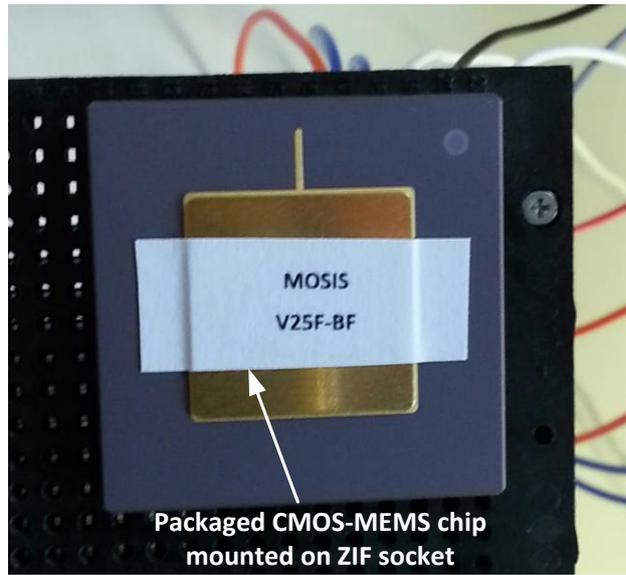


Fig. 8.13: IC in ZIF socket

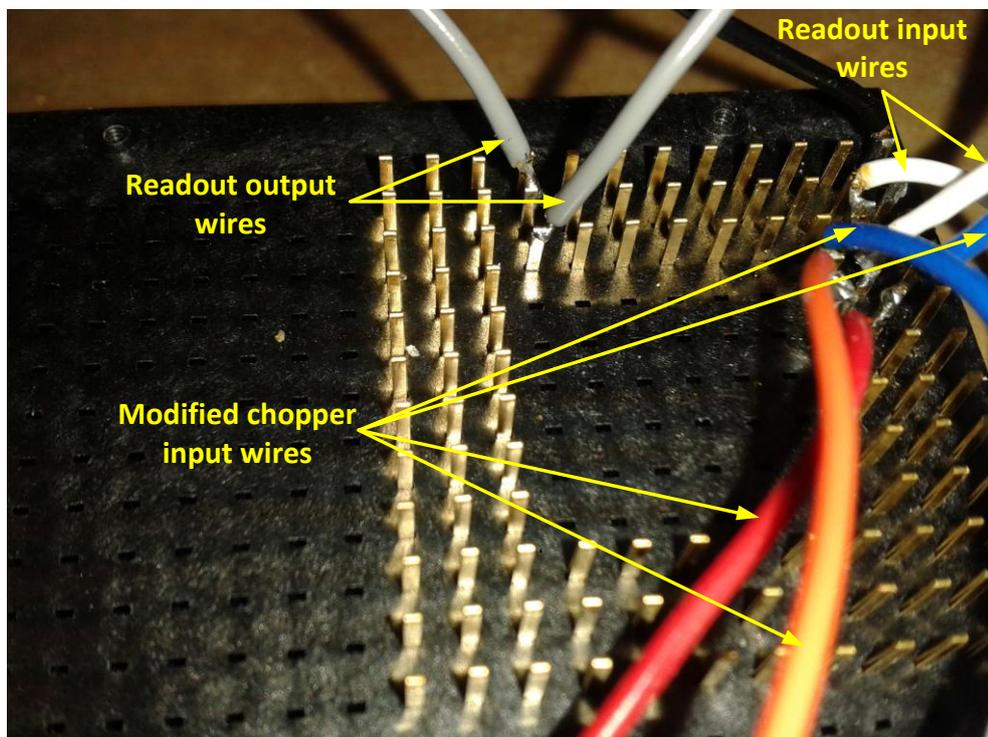


Fig. 8.14: Bottom view of ZIF socket showing the soldered pins

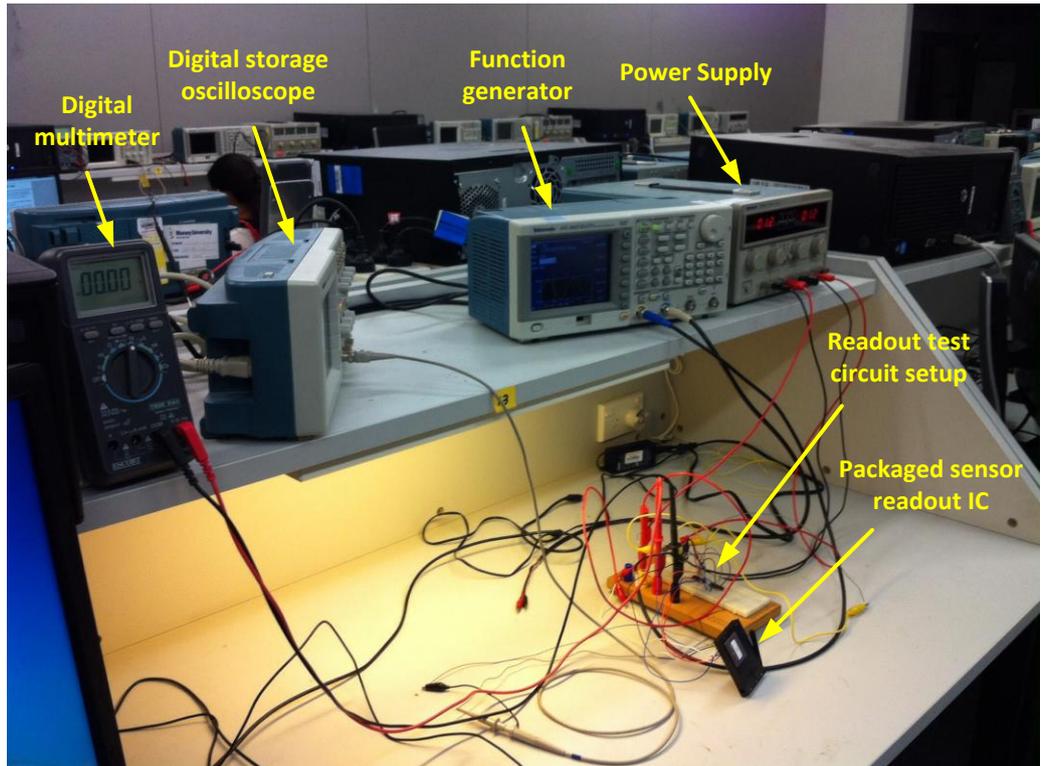


Fig. 8.15: System testing Setup

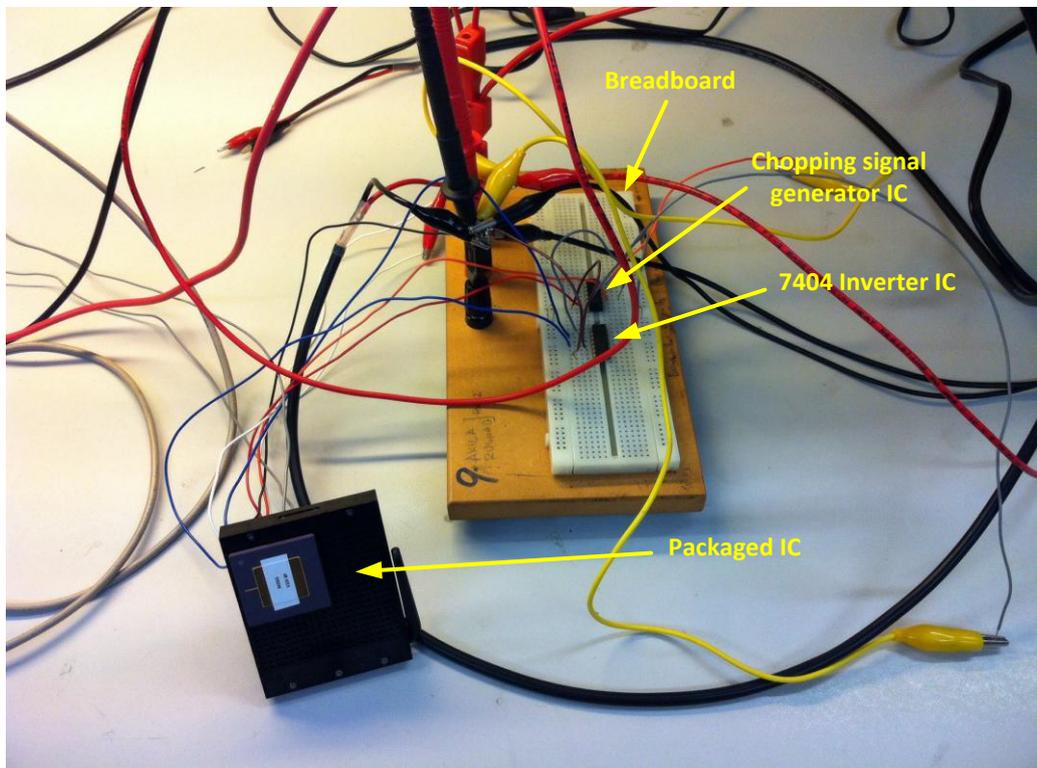


Fig. 8.16: Part of the test circuit connections

8.3.1.3 Preliminary test results

Initial testing was performed to confirm the expected output. The modulation of the input signal with the chopping frequency was as intended. Due to the process variation, the voltage gain of the M-Chopper RFC opamp was marginally low when compared with the simulated value. The input signal and the modulated opamp output are shown in figs. 8.17 and 8.18 respectively. The 10 μV sinusoidal input signal shown in fig. 8.17 looks noisy due to the resolution of the DSO. The clipped RFC opamp output signal in fig. 8.18 indicates that it has a high gain of around 105 dB. The only unexpected behavior noticed was the low output voltage swing. Approximately a 0.7 V of swing was observed, which was nearly 0.1 V less than the simulated output swing. The minor variation in the output swing could possibly be the result of

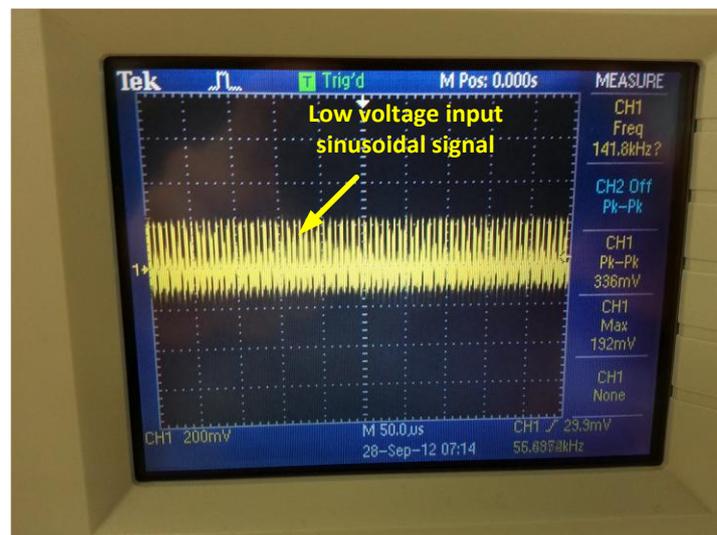


Fig. 8.17: Input signal to the opamp

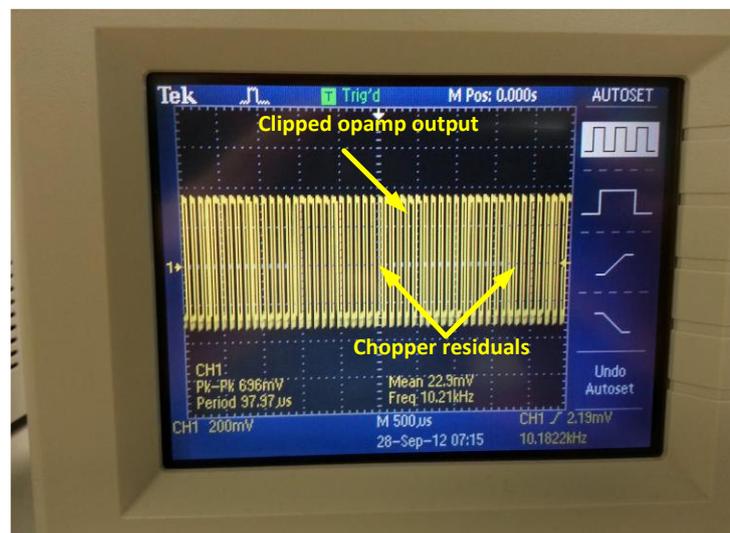


Fig. 8.18: Modulated signal at the output of opamp

increased overhead at the second stage CS amplifier; this could have been caused by the process induced variation of transistor's threshold voltages. Further, chopper residuals were still found to be present at the opamp output even after demodulation; however, it was completely removed by the succeeding Gm-C low pass filter stage. No gain error was observed at the output of the low pass filter. The output stage buffer can able to drive a significant capacitive load of up to 4 pf, without limiting the load current; however a gain error of -2 dB could not be avoided.

8.3.2 Comprehensive experimental analysis

The naked die of the integrated CMOS MEMS sensor developed using the standard IBM process, is then post-processed and sealed to form a comprehensive sensor micro-system as described in Chapter 7. A complete experimental analysis to validate the performance of the micro-system including the sensor's functionality, as well as readout circuit's signal pick-off capability was carried out. The hermetically sealed MEMS capacitive pressure sensors do not require tedious vacuum electrical lead transfer techniques as this is taken care of during the BEOL interconnect metallization process. The sensor interconnections with an on-chip CMOS readout circuit are routed through the bottom BEOL metal stack (M1/M2/M3), and hence these metallization are not in proximity to the region of release etch and vacuum sealing. The experimental test system has an inherent advantage of a low noise setup, as no interconnections with external readout circuitry that can pick up noise and render stray capacitances is required. An on-chip high gain g_m -boosted OTA (Operational Trans-conductance Amplifier) provides sufficient amplification for this low frequency sensor output. Two stage chopper-stabilized CMOS sensor signal conditioning readout circuit uses a cascade of an RFC (recycled folded cascode) input OTA along with a common-source output stage, yielding an overall gain of around 105 dB. The current mirror factors H and F contribute to the enhancement of the amplifier transconductance. Using switching pins the readout circuit can connect to each sensor individually or to a parallel connection of both the diaphragms. A pressure chamber, mass flow controller, Nitrogen gas pump, LCR meter, power supply and a DMM (Digital Multi Meter) are some of the equipments used in the test setup as shown in fig. 8.19. The integrated sensors are bonded on to the general purpose FR-4 PCB board using a wire-bonder as shown in Fig. 8.20. The measured physical dimensions of the elliptic and rectangular sensing diaphragms were $431 \mu\text{m} \times 248 \mu\text{m}$ and $488 \mu\text{m} \times 250 \mu\text{m}$ respectively. The diaphragm's anchor width being around $95 \mu\text{m}$ contributes some parasitic capacitance, which can be cancelled using reference capacitance techniques [26]. In addition to the integrated readout circuit pins, the capacitive sensors can also be accessed directly via bottom and top plates interconnect pins (*for external signal conditioning option*). The stable capacitances measured using an Agilent 4284A Precision LCR meter (with 0.05% basic impedance accuracy) at zero applied pressure were 1.16

pF and 1.23 pF for the elliptic and the rectangular sensing elements respectively. In addition, the capacitive transduction dynamic range was found to be 0.32 pF and 0.23 pF respectively, for the elliptic and rectangular element (for 80 hPa pressure variation) as shown in fig. 8.21. Over the measured pressure range, the elliptic element provided better sensitivity of 4 fF/hPa compared to the rectangular element for which the sensitivity was 2.9 fF/hPa. The elliptic diaphragm exhibited slightly higher linearity compared to the rectangular diaphragm within its dynamic range. Device sensitivity was observed to be marginally higher in the high range of applied pressure (40 hPa – 80 hPa).

The test system used a low 1.2 V supply, so that the power dissipation with both capacitive devices employed along with the CMOS sensing circuit was found to be as low as 425 μ W. The maximum sensitivity at the output pins of the readout circuit for a pressure range of up to 100 hPa is found to be 0.07 mV/Pa for the elliptic element and 0.05 mV/Pa for the rectangular device as shown in fig. 8.22. In comparison, the sensitivity achieved by a pressure sensor reported in [118] was an order of magnitude lower at only 0.00787 mV/Pa. Thermal coefficient of the capacitive sensor is critical for the linearity aspect of the device. Although capacitive sensors are mostly independent of temperature variations compared to piezo-resistive sensors, marginal decreases (*nonlinear behavior*) in the capacitance (@ the higher pressure range) were observed when the chamber temperature was increased above room temperature (27°C). The sensor capacitances were measured for three different temperatures (15°C, room temperature and 55°C) as shown in fig. 8.23 (a) and (b). The average capacitance drift was around 10 fF over a range of 20°C temperature variation. In general, decrease in the capacitance in the order of femto-farads was observed in the higher pressure range from 60 hPa to 100 hPa for the elliptic device and 75 hPa to 100 hPa for the rectangular device. This is possibly due to the non-uniform diaphragm stress distribution over higher pressure ranges (@ higher temperatures). The vent valve was released (*relieved*) frequently during the test for linear increase of pressure inside the chamber. The observed hysteresis and repeatability (*test-retest reliability*) for the elliptic element were 0.045% (3.6 hPa /80 hPa) and 0.02% (1.6 hPa/80 hPa) point of reading respectively. On the other hand, the hysteresis was lower in the rectangular element with 0.024% (1.9 hPa/80 hPa) but a moderate repeatability of 0.05% (4 hPa/80 hPa) was noted in this case. Referred to the 80 hPa input range; the hysteresis was 3.6 hPa and 1.9 hPa, while, the repeatability was 1.6 hPa and 4 hPa respectively for the elliptic and the rectangular sensors. The residual stress in the diaphragm was low at approximately 11 MPa, which is lower than that in anchored polysilicon structures fabricated in multi-user MEMS (MUMPS) processes. Liner buckling analysis carried out prior to plasma etching indicated that the aluminum membrane can withstand a comparatively higher stress of around 500 MPa compared to a similar geometry polysilicon membrane which could break at around 300 MPa.

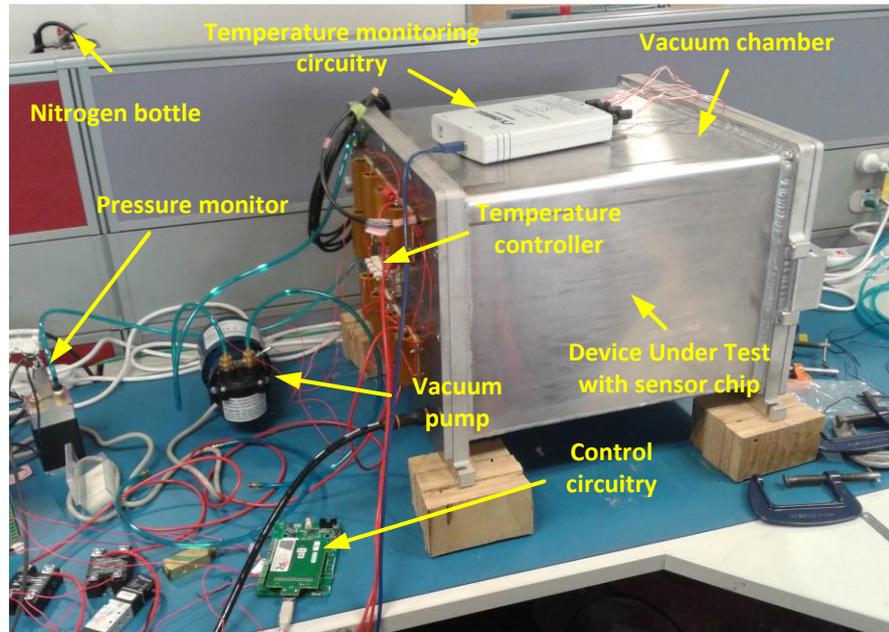


Fig. 8.19: Experimental test setup for sensor transduction performance measurement

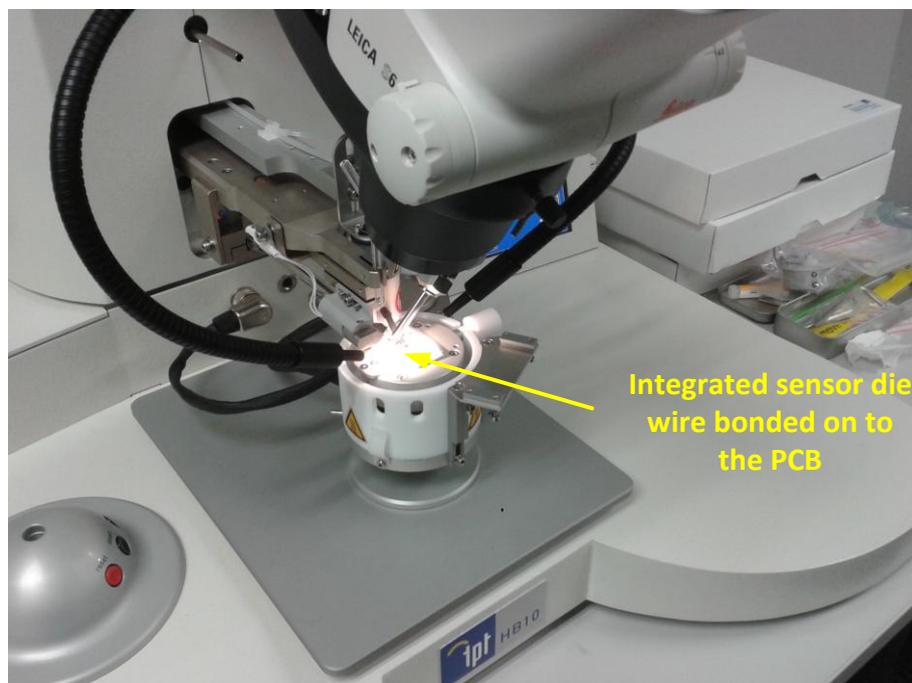


Fig. 8.20: Post-processed CMOS MEMS naked die being wire-bonded on to the PCB

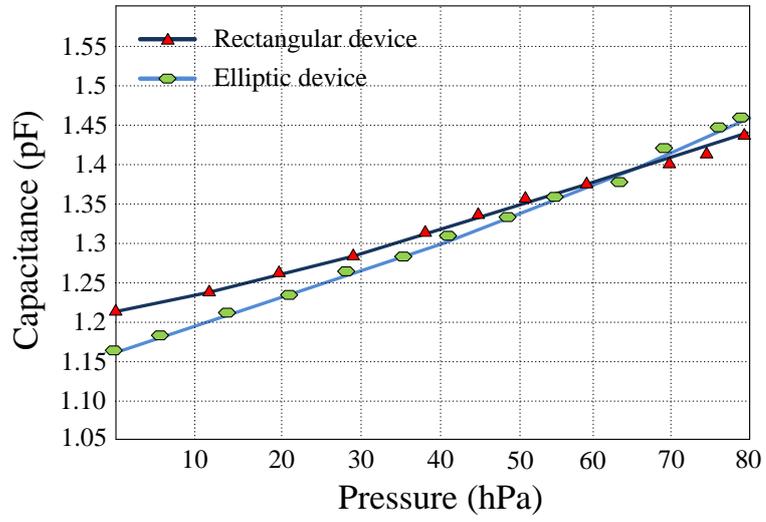


Fig. 8.21: Performance of the elliptic and rectangular devices

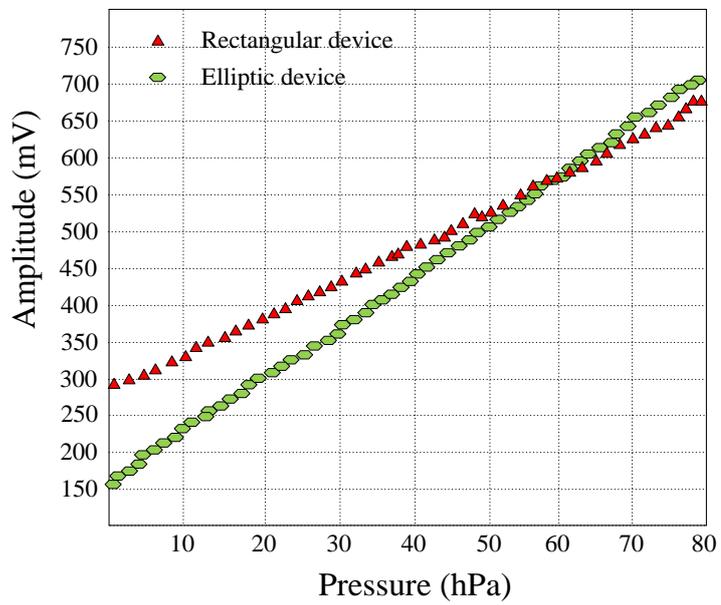
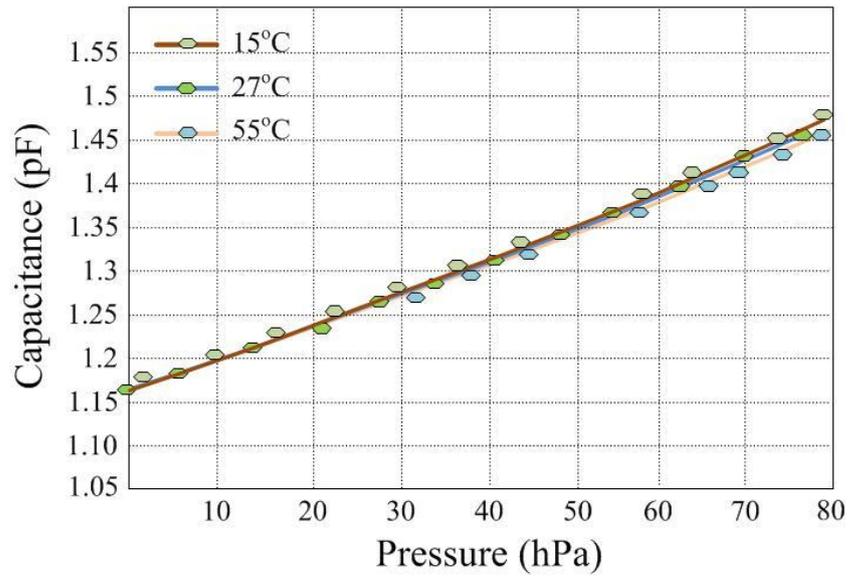
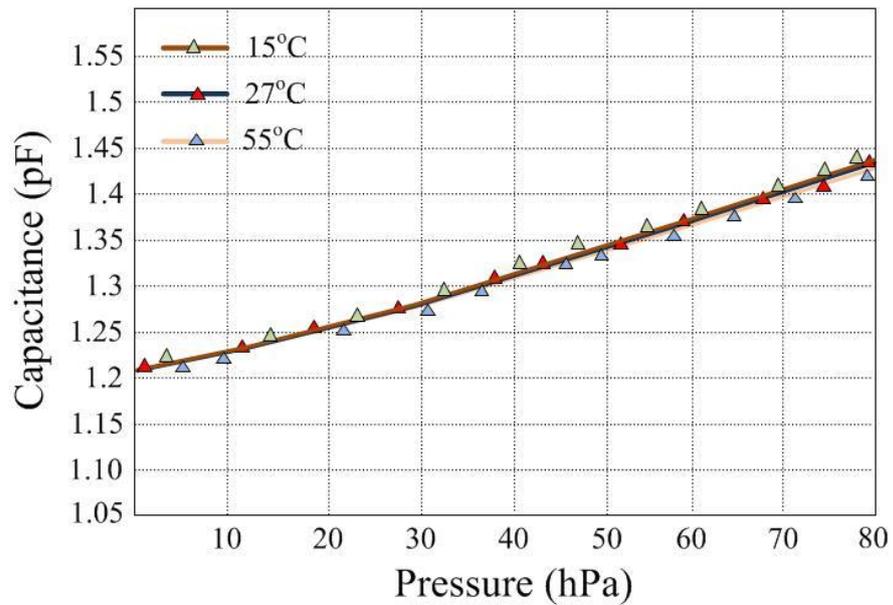


Fig. 8.22: Sensing circuit response with applied pressure



(a)



(b)

Fig. 8.23: Temperature dependencies of, (a) Elliptic element, (b) Rectangular element

8.4 Comparison of CMOS MEMS sensor micro-systems

Two types of integrated sensor micro-system for the purpose of pressure sensing in bio-medical related applications such as, catheter pressure monitoring and intraocular pressure measurement were designed and experimentally tested. The experimental results of these three micro-sensors, designed and fabricated using two different process technologies are compared with each other to study the process compatibility of monolithic integration of CMOS circuits

with high performance MEMS devices. Further, comparison study among the various reported CMOS MEMS micro-system was also conducted to ascertain the advantages of the designed devices.

8.4.1 Comparison of SiGeMEMS and standard CMOS MEMS sensor micro-systems

The dimension of the SiGeMEMS micro-sensor device is comparatively larger than the standard CMOS MEMS devices; this is possible due to the increased release length rendered by the perforations in the structure. The free standing structure in a SiGeMEMS process can extend up to 700 μm (anchor to anchor distance) as the perforations provide proper seepage of release chemicals. Further, proper design of perforations helps in reach of chemicals to the underlying sacrificial oxide at the edges of the diaphragms, thus ensuring full structure release. Increased deflection is achieved with the design of clamp spring anchoring in SiGeMEMS diaphragm; however its sensitivity is an order of magnitude less than the CMOS MEMS devices. This is possibly due to the increased thickness of 0.8 μm at the center of the diaphragm as an additional stem sealing structure is used. On the other hand, the all sided anchored standard CMOS MEMS sensor micro-system yielded a better dynamic range and sensitivity; moreover both rectangular and elliptic aluminum elements of CMOS MEMS process exhibited lower hysteresis than elliptic element fabricated using poly-SiGeMEMS material. Rectangular diaphragm had the lowest hysteresis than both the elliptic geometries however its repeatability was poor. Higher linearity is observed in the SiGeMEMS device due to the excellent stress-strain behavior of poly-SiGe material. Perforations in this diaphragm also significantly increased the linearity; however marginal decrease in the surface capacitance contributed to lower output capacitive sensing values than the standard CMOS MEMS devices. Eventhough both micro-systems include two stage high gain amplifiers, SiGeMEMS micro-system provided lower overall sensitivity than standard CMOS MEMS micro-system due to its comparatively low sensor output signal. It was also noted that the comprehensive scientific values of the former is lower than the latter. The industry standard CMOS processed MEMS diaphragm have lower young's modulus of 69 GPa. This contributed to low membrane stiffness, which yielded better deflection even with a comparatively smaller dimension at low pressure ranges. Comparatively higher young's modulus of 130 GPa in poly-SiGe membrane has invariably increased its flexural rigidity; however faster deformation recoverability provided better repeatability and linearity. Further their stiffness is considerably reduced with arrays of perforations and moreover the clamp spring anchoring at semi-major axis of the diaphragm led to membrane deformation even at a very low applied pressure. Comparatively higher membrane stiffness of poly-SiGe material provided a lesser transverse deformation of the diaphragm at higher pressure ranges contributing

to increased dynamic range than CMOS MEMS devices. Lower poisson's ratio of 0.22 in this membrane yielded less lateral deformation providing low material creep at higher applied pressure loads than aluminum membranes.

All the three devices (elliptic SiGe device, elliptic and rectangular standard CMOS MEMS device) were found to have better reproducibility, as the micro-mechanical structures were comparatively thick (4 μm). In addition, their yield losses were extremely low. The die sizes of both the micro-sensor systems were approximately 1 mm \times 1 mm which is more appealing for invasive bio-medical pressure monitoring applications. The MEMS process temperature was substantially lower in both the processes (SiGeMEMS and standard CMOS MEMS processes) hence degradation of CMOS devices and interconnects were negligible. Excellent mechanical properties of poly-SiGe material [67], allowed for low temperature MEMS post-processing on top of the CMOS wafer, on the other hand, the proposed foundry compatible low temperature mixed wet and dry plasma enhanced etch processes in standard CMOS MEMS contributed to the low temperature post process. Moreover these miniaturized micro-systems effectively contributed to multiplication of cost reduction compared to other reported micro-systems [118], [127]. The above feature comparisons proves that both the SiGeMEMS and standard CMOS MEMS processed micro-sensor systems are very much compatible for MEMS multi-sensor micro-system, moreover the obtained sensitivities and dynamic range indicate that if the devices and CMOS circuits are further scaled for the purpose of miniaturization, they can still provide comparatively better performance for effective sensing.

8.4.2 Comparison of various reported CMOS MEMS sensor micro-systems

The designed three micro-devices were found to have low power dissipation with better dynamic range than the pressure sensor reported in [130]. The dimensions of the devices were comparatively 10 times less than the integrated MEMS devices reported in [130] with higher sensitivities. Eventhough the sensor response was ideally linear in the reported micro-sensor system [131] for gait analysis, the performances of the signal conditioning circuit were poor with higher noise factor and significantly large CMOS die area. This work has demonstrated two miniaturized integrated MEMS sensor devices that exhibited better overall responses and are compatible for multiple bio-medical applications including foot plantar pressure monitoring. The reported CMOS MEMS micro-pressure sensor for TPMS application (tire pressure monitoring system) in [132] is found to have low sensitivity of 0.27 mV/hPa when compared to the CMOS MEMS devices designed in this work. SiGeMEMS device is found to have a linear dynamic range of 7 to 90 kPa, which is an order of magnitude higher than in [132]. Moreover, the size of the reported device in [132] is nearly 1.5 times larger than this work with higher power dissipation, additionally the sensor readout performances is found to be poor with high

non-linearity of 4.58%. The mechanical sensitivity of all the devices in this work is significantly higher as the volume compliance is nominal with 4 μm than the reported CMUT-in-CMOS approach in [132]. The resulting capacitance change for a given applied pressure in this work is larger than the ultrasonic image capacitive sensor, moreover, the sensor devices operates with considerably low applied bias voltage prior to pull-in or collapse. The devices developed by both SiGeMEMS and standard CMOS MEMS process with 3 μm and 11 μm plate gap respectively, had higher pull-in voltages (>30 V); hence the chances of snapping of the devices at the operating pressure ranges are negligible unlike the variable gap designed device in [133]. Further, the scientific values of the proposed devices are significantly higher than the linear varying gap devices and would render better overall performances for bio-sensor applications. The eight and four multilayer fabrication process employed in this work contributed to the integration of complex signal conditioning circuit and overall miniaturization of the sensor micro-system. Alternatively, the 2P4M process in [133] had a high pull-in voltage than the proposed devices; also poor plate gap spacing limits the dynamic range of the sensor. Further, as the MEMS devices have to be built in the top two layers above the CMOS circuitry, integration of high performance CMOS circuitry is extremely difficult. The insufficient metal interconnection layers in this 2P4M thus limit the overall system performance. Moreover, the MEMS above CMOS integration as in the proposed SiGeMEMS process is impossible in [133]; hence CMOS circuit must be integrated with too much lateral displacement from the MEMS devices for avoiding parasitic issues and threshold voltage variation of MOS transistors. Thus a poor overall sensitivity than the proposed sensor systems is noticed. Further, as the device and circuit implementation was in the older TSMC 0.35 μm technology, higher power dissipation is also observed. This is due to the limitations in the minimum bias and supply voltages.

As compared to W. Fang's 2P4M CMOS MEMS publication [127], this work has employed a mix of wet and dry etch for device release. Maskless approach and metal wet etch performed in the publication titled "Design and application of a metal wet-etching post-process for the improvement of CMOS-MEMS capacitive sensors," will increase the risk of degradation to device performance and serious stiction effect. Alternatively, dry etch that provides good sidewalls, as well as avoids lift-off of device anchors was performed in this work for trench and lateral release etch. AFM analysis was carried out to characterize the sidewall after the stripping the resist. The sidewall revealed a satisfactory anisotropic etch profile. As the anchors were found to be intact with the AFM step height and profile analysis, SEM imaging by further dicing the chip for etch profile study, as used in the above 2P4M is not necessary. In the other W. Fang's paper titled "Monolithic integration of capacitive sensors using a double-side CMOS MEMS post process" [118], a deep backside wet etch was performed for device release. Backside etch performed on a 0.35 μm CMOS technology wafer can drastically alter the

threshold voltage of the MOS transistors and can drive them to non linear regions. This can seriously affect the CMOS circuit performance leading to poor gain, in addition it can vary the pre-known parasitic effects of the circuitry and can cause higher noise levels rendering post-process variations. Moreover, double sided etch involves increased process steps and longer post-process time, causing overall delay in the foundry level mass production from design to ship-out. This work has overcome these issues by developing a pre-determined release process sequence for the single sided etch, which provides negligible post-process variations to the CMOS circuits. Detailed descriptions of these release process steps were provided in Chapter 6. The experimental results discussed in the previous section validate the claim. The size of the proposed standard CMOS MEMS sensor micro-systems are an order of magnitude less than the previously reported 4 metal CMOS MEMS integration [99]-[102]. The minimum line width in the recent advanced CMOS technology offers less parasitic effect to the sensor devices; therefore the overall parasitic effect including anchors is comparatively less in this work. In 4 metal standard CMOS integration long etch duration cannot be performed as it can easily degrade the CMOS circuitry due to lack of isolation layer, further, the device proximity with the underlying CMOS circuit is also a lot less ($< 5 \mu\text{m}$) which leads to high risk of CMOS device damage. On the other hand, the advanced 8 metal layer integration includes an isolation layer that provides an inherent etch stop technique to avoid CMOS circuit degradation. Moreover, the vertical layer distance between the device and CMOS circuits is nearly $20 \mu\text{m}$; hence there is more freedom to go in for a larger lateral etch length without any circuit impairment. The entire post-process is performed on a $3 \text{ mm} \times 3 \text{ mm}$ IBM foundry fabricated die. Several die level challenges like die handling, resist spin coating, die level etching and post etch cleaning were also addressed. High power supply in older CMOS technologies yields high power dissipation for the sensor signal conditioning that incorporates noise cancellation technique and an on chip buffer. This work utilizes the advanced 8 metal layer technology that uses low voltage supply, therefore the overall power dissipation is remarkably lowered.

8.5 Conclusion

A highly sensitive integrated capacitive pressure sensor is designed, fabricated and characterized through measurements using a $0.6 \mu\text{m}$ feature-size SiGeMEMS process. The on-chip co-hosted signal conditioning circuitry was fabricated in $0.18 \mu\text{m}$ TSMC CMOS process vertically integrated (in 3D) with the MEMS process. Further, successful release of two other MEMS capacitive sensors, which were developed on a 8-metal BEOL 130 nm standard IBM CMOS process was demonstrated by employing a mixture of wet and plasma dry etch. The experimental analysis validates the successful integration of the MEMS pressure micro-sensor systems.

Chapter 9

Conclusion and Future Work

9.1 Conclusion

Two capacitive micro-sensor systems to sense pressure ranges for various biomedical applications were designed and developed in two different process technologies. Micro-mechanical devices on top of the CMOS signal conditioning circuit with elliptic geometry using 0.18 μm TSMC CMOS technology + SiGeMEMS process was designed and tested. Comparatively large dynamic range with better linearity and moderate sensitivity was achieved by employing clamp spring anchoring at semi-major axis of the elliptic diaphragm. This ultra-wide dynamic range perforated micro-sensor scheme, can be utilized with appropriate packaging for medical applications requiring pressure measurement ranging from few hPa (or mm Hg) such as intraocular pressure measurement, to few hundred hPa (or mm Hg) such as intravenous blood pressure measurement.

Two other MEMS sensor devices with rectangular and nano-metric step-edged elliptic diaphragms in the top three BEOL metal stack of standard 130 nm IBM CMOS process were also proposed. A complex CMOS readout circuit in 130 nm CMOS technology was monolithically integrated with these two devices. Comparatively high sensitivities with low hysteresis and better linearity were achieved in both the standard CMOS designs; however, low dynamic range was observed. Due to immense sensitivity, this standard CMOS MEMS micro-system can be utilized in low range implantable medical applications that demand high sensitivity like pulmonary artery pressure measurement and other continuous real-time monitoring of hemodynamic parameters [134]-136]. A vertical planar integration of MEMS devices on top of the previously processed CMOS circuit was demonstrated in CMOS+MEMS SiGeMEMS process. This technology is based on the MEMS-last approach [66], where MEMS devices were processed on top of the modern complex circuit developed using industry standard CMOS technology like IBM or TSMC. This type of monolithic integration led to improved performance compared to other integrations. It was found that the overall signal to noise ratio was better due to reduced interconnect parasitic resistance and capacitance. Low power dissipation was achieved as it enables the integration of low voltage modern CMOS technology circuit. Further, the 3D vertical monolithic integration, effectively reduced the die size leading to miniaturized packaged micro-sensor system. Foundry based low temperature MEMS process (post-process) preserved the CMOS interconnects and circuits. The deposition temperature of poly-SiGe structural material was very much compatible for the CMOS part, thus performance

degradation of the sensor readout circuit was avoided. Moreover, the excellent properties of poly-SiGe material such as higher strength, high Q factor, less creep and low fatigue [66], led to the design of wide dynamic range MEMS device. The L-clamp spring anchoring and perforations offered excellent compensation for the reduced membrane deflection due to the high flexural rigidity, thus a very low minimum detectable pressure (MDP) was achieved.

Design and post processing of integrated standard CMOS MEMS devices with readout on an 8 Metal layered process, which was not reported before were proposed. Post-processing of both elliptic and rectangular devices was successfully carried out. The optimized process recipe and successful release steps for a lateral length of 125 μm (die level 130 nm standard CMOS process) were the contributions of this work. During this long duration lateral dry etch, better side-wall protection for the region towards the anchor was achieved by thin PR coating with mask 2. The only region exposed to this RIE etch are the sides of device diaphragms; hence the possibility of random etch elsewhere was avoided. Microscopic observation revealed that there was no damage to the anchors; however the nano-metric step sides of the elliptic diaphragm were rounded off as it was completely exposed during the long etching duration. It was found that CHF_3 etch provided high selectivity between Aluminum and oxide, hence serious damages to the sides of the diaphragm (Al) that can cause degradation to device performance were not noticed. The E1 (copper) interleaving mesh layer was a test structure and was helpful in identifying the full release of the element. Hampering of these layers during wet etch was noted as expected, furthermore, it helped with judging the formation of micro-vent. It was also observed that the mesh layers below the edges of the diaphragm were removed during this wet pre-lateral etch; hence the lateral length of the micro-vent was easily ascertained through microscopic observation.

Mechanical and electrical characterizations of the released pressure sensors were done; their experimental results and the performance of the sensor devices (discussed in Chapter 8) validate the successful release process. Analysis performed to study the chip damage and degradation after post-process, revealed that the sensor anchors were intact and the device dimensions and structure were retained without any serious damages to the diaphragm sides. Device characterization in a vacuum chamber is carried out under various applied pressures. The sensor readout circuit performances were satisfactory. The g_m enhanced RFC opamp was found to have a high single stage gain with good stability and low noise. The diaphragms having high mechanical sensitivities are designed using non-biocompatible materials, therefore as a future work biocompatible thin film deposition such as titanium oxide or alumina [137] of few nanometers must be coated for implantable applications. Further, with a thin film detector molecule deposition [138], the application can be extended for biochemical sensing.

The key findings and the contributions of this work to enhance the performance of the MEMS pressure micro-sensor system were:

- Micro-Electro-Mechanical capacitive pressure sensor in SiGeMEMS (Silicon Germanium Micro-Electro-Mechanical System) process was designed, fabricated and characterized. Excellent mechanical stress–strain behavior of Polycrystalline Silicon Germanium (Poly-SiGe) was utilized effectively to design the structure of the pressure sensor element. Perforated elliptic geometry diaphragm, anchored at the semi-major axis using L-clamp spring was designed and fabricated on top of the CMOS signal conditioning circuit (TSMC 180 nm technology). The custom clamped elliptic diaphragm yielded high sensitivity, wide dynamic range and good linearity compared to the other edge clamped diaphragms.
- An on-chip signal conditioning circuit comprising an amplifier, a low pass filter and a buffer output stage was designed. A high gain CMOS operational amplifier is proposed for signal conditioning the SiGeMEMS micro-sensor's output. Chopper Stabilized folded cascode opamp designed in 180 nm TSMC technology was gain boosted to get very high gain without introducing slow settling component, thus the speed of the overall SiGeMEMS sensor micro-system was not compromised. Furthermore, the second stage CS amplifier provides the desired voltage swing with low distortion and output impedance, providing better driving capability. Gm-C continuous filter that removes chopper amplifier residuals eliminates the use of power consuming stages such as oscillators and clock generators. Elliptic type filter design provides better roll-off even in the lower order; hence the transistor numbers and area are reduced. The reduced line width of the process drastically reduces the size of this complex circuit that incorporates at least five transconductance stages, thereby further reducing the area consumption. Low output impedance buffer stage is designed as a self-biased circuit to provide driving capability for the sensor readout. Self-biasing of this stage has further reduced the overall power dissipation by avoiding the requirement of bias circuitry. Current feedback in the design eliminates the need for increasing the g_m of the transistor; hence linearity was improved tremendously without increasing the aspect ratio of the transistors.
- Rectangular and nano-metric step-sided elliptic geometry micro-sensors, integrated with the CMOS readout in a standard 130 nm IBM CMOS process were also designed and fabricated. An on-chip active switch provides the choice of parallel connection of these two devices, for significant improvement of dynamic range.

- Foundry based mass production compatible post-processing technique, that overcomes the issues of multi-layer standard CMOS MEMS process was addressed. A mix of wet and inductive plasma dry release etch, experimentally performed on a modern 8 metal BEOL 130 nm CMOS process was proposed. This process (also known by the acronym 8RFDM) contains 3 thin lowest metal layers (M1, M2 and M3), 2 thick middle metal layers (MQ and MG) and 3 thick top (upper) RF metal layers (LY (Al), E1 (Cu) and MA (Al)). The release process was done in the 3 upper metal layers MA, E1 and LY, as the sensors were constructed in this region.
- A g_m enhanced recycled folded cascode (RFC) opamp was designed and fabricated in IBM 130 nm CMOS technology for excellent amplification of the standard CMOS micro-sensors output. Current cross mirroring was employed for the significant improvement of the gain. The filter circuit and output buffer stage proposed for SiGeMEMS micro-system were redesigned to adapt for the 130 nm CMOS low supply voltage design.

9.2 Future work

This research work in future will be further developed using the recently advanced industry standard CMOS technologies such as 90 nm and 65 nm. However, the design and the optimized recipe for the post-processing must be employed with minor variations according to the structural materials and mask layout limitations. The etch time must also be adapted according to the dimensions of the diaphragm and the amount of lateral release length, in order to achieve the required etch depth. A similar intermediate mesh layer however, can be effectively utilized to ascertain the complete membrane release. The advanced technology will yield comparatively low performance due to the reduced channel length of the MOS devices. Thus to achieve high performance redesigning of signal conditioning circuit is necessary. The use of low supply voltage in the recently advanced CMOS technologies will permit the reduction of power dissipation. Further, the overall size of the sensor micro-system can be minimized.

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Appendix I

List of Publications and Copyright permission from the Publishers

1. List of Publications

Journal publications

- Paper titled "CMOS integrated elliptic diaphragm capacitive pressure sensor in SiGe MEMS," is published in *Microsystem Technologies* journal, vol. 20, no. 1, pp. 145-155, on 29th May 2013. URL. <http://link.springer.com/article/10.1007/s00542-013-1818-8/fulltext.html>
- Paper titled "Post-processing and Performance Analysis of BEOL Integrated MEMS Pressure Sensor Capacitors in 8-Metal 130 nm CMOS" is published in *Microelectronic engineering* journal, vol. 119, pp. 89-94, on 1st May 2014. URL. <http://www.sciencedirect.com/science/article/pii/S0167931714000719>
- Paper titled "Release Etching and Characterization of MEMS Capacitive Pressure Sensors Integrated on a standard 8-metal 130 nm CMOS process," is published in *Sensors and Actuators A: Physical Journal*, vol. 212, pp. 68-79, on 1st June 2014. URL. <http://www.sciencedirect.com/science/article/pii/S0924424714001253>
- Paper titled "Elliptic Diaphragm Capacitive Pressure Sensor and Signal Conditioning Circuit Fabricated in SiGe CMOS Integrated MEMS," is published in *IEEE Sensors Journal*, vol. 15, No. 3, pp. 1825 – 1937, on 4th November 2014. URL. <http://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=6945787>

Papers under review

- Paper titled "A Transconductance Doubling CMOS Regulated Folded Cascode (TD-RFC) for Micro-Sensor Readout," was submitted for publication in *IEEE Electronic Letters* is presently under review.
- Paper titled "High sensitive Absolute MEMS Capacitive Pressure Sensor in SiGeMEMS Process for biomedical applications," was submitted for publication in *IEEE Sensor Letters* is presently under review.

Conference publications

- Paper titled "A Low Power 4th Order Low Pass Gm-C Filter in 130nm CMOS," was presented in ENZCON conference held at Massey University, PN, New Zealand during November 2011.
- Paper titled "A CMOS Integrated MEMS capacitive pressure sensor design in a 3D SiGeMEMS process," was presented in M2VI conference held at AUT, Auckland, New Zealand during 28th-30th November 2012.

- Paper titled “Multi-Recycled Folded Cascode Amplifier for Sensor Readout,” was presented in ENZCON conference held at Massey University, Albany, Auckland, New Zealand during 3rd -5th September 2013.

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Appendix II

Application forms for the Statement of Contribution to Doctoral Thesis containing Publications

Appendix III

Papers Published in Journals and Conferences

CMOS integrated elliptic diaphragm capacitive pressure sensor in SiGe MEMS

Ananiah Durai Sundararajan · S. M. Rezaul Hasan

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Abstract A novel CMOS integrated Micro-Electro-Mechanical capacitive pressure sensor in SiGe MEMS (Silicon Germanium Micro-Electro-Mechanical System) process is designed and analyzed. Excellent mechanical stress–strain behavior of Polycrystalline Silicon Germanium (Poly-SiGe) is utilized effectively in this MEMS design to characterize the structure of the pressure sensor diaphragm element. The edge clamped elliptic structured diaphragm uses semi-major axis clamp springs to yield high sensitivity, wide dynamic range and good linearity. Integrated on-chip signal conditioning circuit in 0.18 μm TSMC CMOS process (forming the host substrate base for the SiGe MEMS) is also implemented to achieve a high overall gain of 102 dB for the MEMS sensor. A high sensitivity of 0.17 mV/hPa (@1.4 V supply), with a non linearity of around 1 % is achieved for the full scale range of applied pressure load. The diaphragm with a wide dynamic range of 100–1,000 hPa stacked on top of the CMOS circuitry, effectively reduces the combined sensor and conditioning implementation area of the intelligent sensor chip.

1 Introduction

Integration of micro-structured sensing and actuating devices with signal conditioning circuit has been of significant research interest for the past few years. Improvement in the

performance of the transducer system has greatly influenced the growth in the development of on-chip prototype sensors and actuators. However, their production and utilization is still in the budding stage. Micro-pressure sensors have been in great demand in numerous fields such as Bio-medicine, Automotives, Industrial safety, Aeronautics etc. for the past few decades. Capacitive and Piezoresistive transduction are the two well known techniques of commercialized pressure sensor implementation (Clark and Wise 1979). Ease of fabrication steps and insensitivity to temperature variation as well as environmental effects have made the capacitive sensing principle preferable over the piezoresistive implementation. However, parasitic effects result in significant degradation of the capacitive sensing technique, hence it requires on-chip readout and conditioning circuitry for performance enhancement (Doody et al. 2011).

Efforts in the hybrid integration of sensor devices and associated conditioning circuitry in a single hermetic package has mostly resulted in poor performance of the sensing system due to the significant issues of nonlinearity, reliability and environmental degradation. Even though monolithic integration usually has a longer time to market compared to hybrid sensor systems; it offers lower overall production and packaging cost (Witvrouw 2006). The unique monolithic integration of SiGe MEMS sensor device on top of the CMOS (Complementary Metal Oxide Semiconductor) circuit (also forming the host substrate for the SiGe MEMS structure) in this CMOS integrated SiGe MEMS process has immensely miniaturized the proposed pressure sensor system. The low thermal variation of the material properties of polycrystalline SiGe enables the post processing of the sensor devices on top of the CMOS circuit. Different diaphragm shapes and structures along with varied dimensions and thickness have been explored in the past decade for improving the overall system performance

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parameters such as sensitivity, linearity and dynamic range (Clark and Wise 1979; Doody et al. 2011; Witvrouw 2006; Chau and Wise 1987). Although reduced diaphragm thickness has yielded improved sensitivity, the trade-off has been poor linearity (Doody et al. 2011). This proposed design has focused to overcome this sensitivity vs. linearity trade-off. The system block diagram of the proposed integrated sensor is shown in Fig. 1. The weak noisy sensor signal is amplified utilizing a modified significantly low-noise chopper-stabilized op-amp (operational amplifier). The high frequency chopper residuals (artifacts) are filtered out by a steep roll-off Gm-C filter. The filter is followed by a self-biased buffer output stage which can drive an off chip load of up to 15 pF. The design target for the proposed edge clamped perforated elliptic diaphragm structure is to achieve wider dynamic range, without compromising sensitivity and linearity. In order to achieve this performance, clamp type spring is utilized as shown in Fig. 2 which has not been reported before. This paper is organized as follows: In Sect. 2, characterization of the structural and fabrication aspects of the micro-sensor is described, in Sect. 3, the detailed description of the requirements and design analysis of the on-chip signal conditioning circuit is explained, while in Sect. 4, the model analysis and

performance of the integrated system characteristics is provided. Finally, concluding remarks are presented in Sect. 5.

2 Design and characterization of sensor device

The capacitive sensing technique which is an inherently low noise transduction mechanism is also a relatively simple method that uses either a varying displacement or a varying parallel-plate surface-area principle to pick up (sense) the desired physical quantity. Although this technique is less resilient to harsh environment compared to its piezoresistive counterpart; proper structural design can, in comparison, contribute to a relatively lower hysteresis and greater stability as the distinct advantages of this technique.

2.1 Theory

The elliptic structured diaphragm of the capacitive pressure sensor is designed with numerous planar perforations in order to achieve higher linearity. Also, clamping near the semi-major axis edges only using clamp springs enables better low pressure sensitivity compared to an all edge clamped sensor structure. As vertical pressure is applied on the diaphragm the separation between the diaphragm and the bottom electrode varies yielding a fluctuation in the capacitance. Ignoring the fringe electrostatic field flux lines, the capacitance variation is governed by (Chau and Wise 1987),

$$C = \frac{\epsilon_r \epsilon_0 A}{d} \tag{1}$$

where, ϵ_r is the relative permittivity of the dielectric material, ϵ_0 is the permittivity of free space, A is the cross-sectional area of the diaphragm and d is the separation between the electrodes/plates. Under the influence of applied pressure, the diaphragm deforms due to the distributed stress and strain. The edge clamping using the clamp spring causes the diaphragm to deflect in a non-uniform manner. As a result the change in distance between the diaphragm and the bottom electrode is not uniform throughout the cross-section, and hence (1) must be obtained by surface integration over the 2D (spatial) distance between the electrodes, which can be written as (Chau and Wise 1987),

$$C = \iint [\epsilon_r \epsilon_0 / \{ d_0 - D(x,y) \}] dx dy \tag{2}$$

where d_0 is the distance between the plates at zero pressure and $D(x,y)$ is the incremental change in the distance after deflection at a spatial location (x,y) . The effective plate deflection (w) for an elliptic diaphragm can be expressed as,

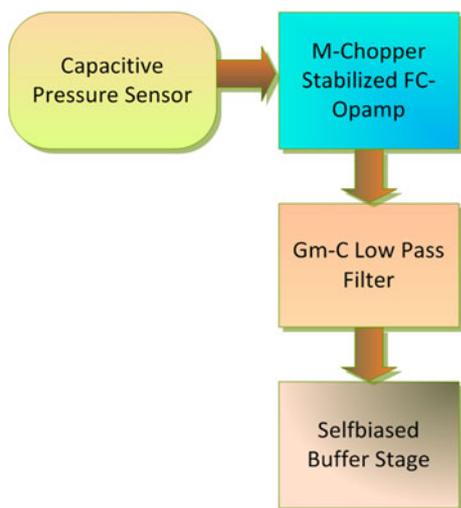


Fig. 1 System block diagram of the proposed signal conditioning integrated MEMS capacitive pressure sensor

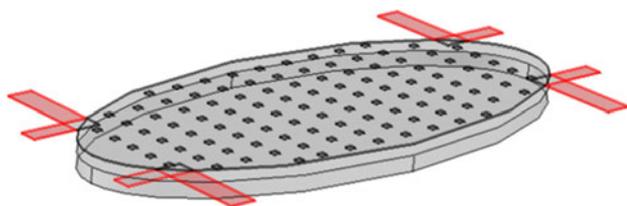


Fig. 2 Perforated elliptic diaphragm, clamped at the semi-major axis using clamp springs

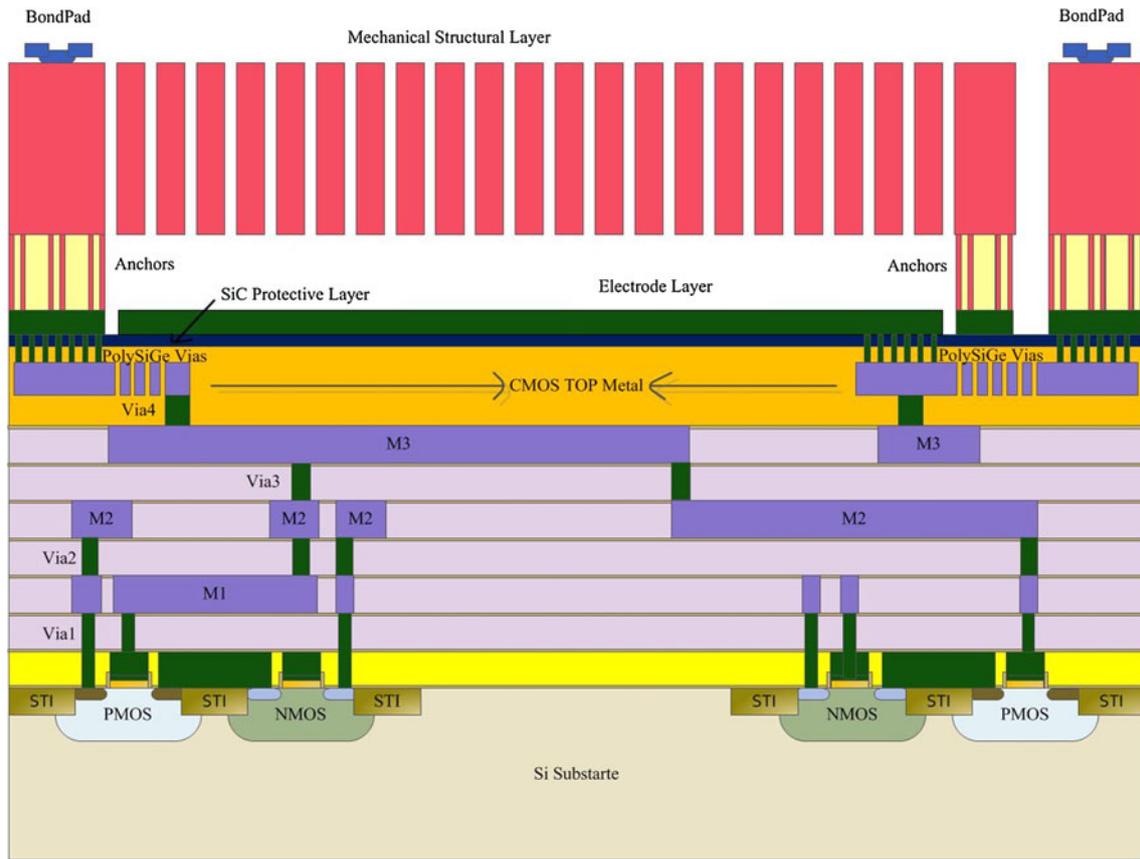


Fig. 3 Cross-section of the target CMOS integrated SiGe-MEMS process for integrated MEMS pressure sensor

$$w = [1/(\pi \cdot r1 \cdot r2)] \iint D(x, y) dx dy \tag{3}$$

where, $r1$ and $r2$ are respectively the radii of the semi-minor and semi-major axis, while the effective deflection, w in the z direction is determined by averaging the spatially integrated deflection over the entire surface area of the elliptic diaphragm. The diaphragm thickness is very small compared to the other dimensions, and, hence assumption of Kirchoff's hypothesis (Ventsel et al. 2001) is considered in the stress analysis of its deflection. Furthermore, the diaphragm displacement will usually be around half its thickness, so that, 2D plane stress analysis of thin plates is best suited in this design. The stress tensor components σ_z , σ_{xz} and σ_{yz} becomes null in such an analysis and the stress tensor matrix reduces (Ventsel et al. 2001) to:

$$\sigma = \begin{bmatrix} \sigma_x \\ \sigma_y \\ \sigma_{xy} \end{bmatrix} \tag{4}$$

Assuming the diaphragm material is isotropic, its stress-strain behavior can be considered to be linear within the range of its elastic limit. This stress-strain linearity assumption up to the elastic limit is based on the Hook's law and can be given by (Ventsel et al. 2001),

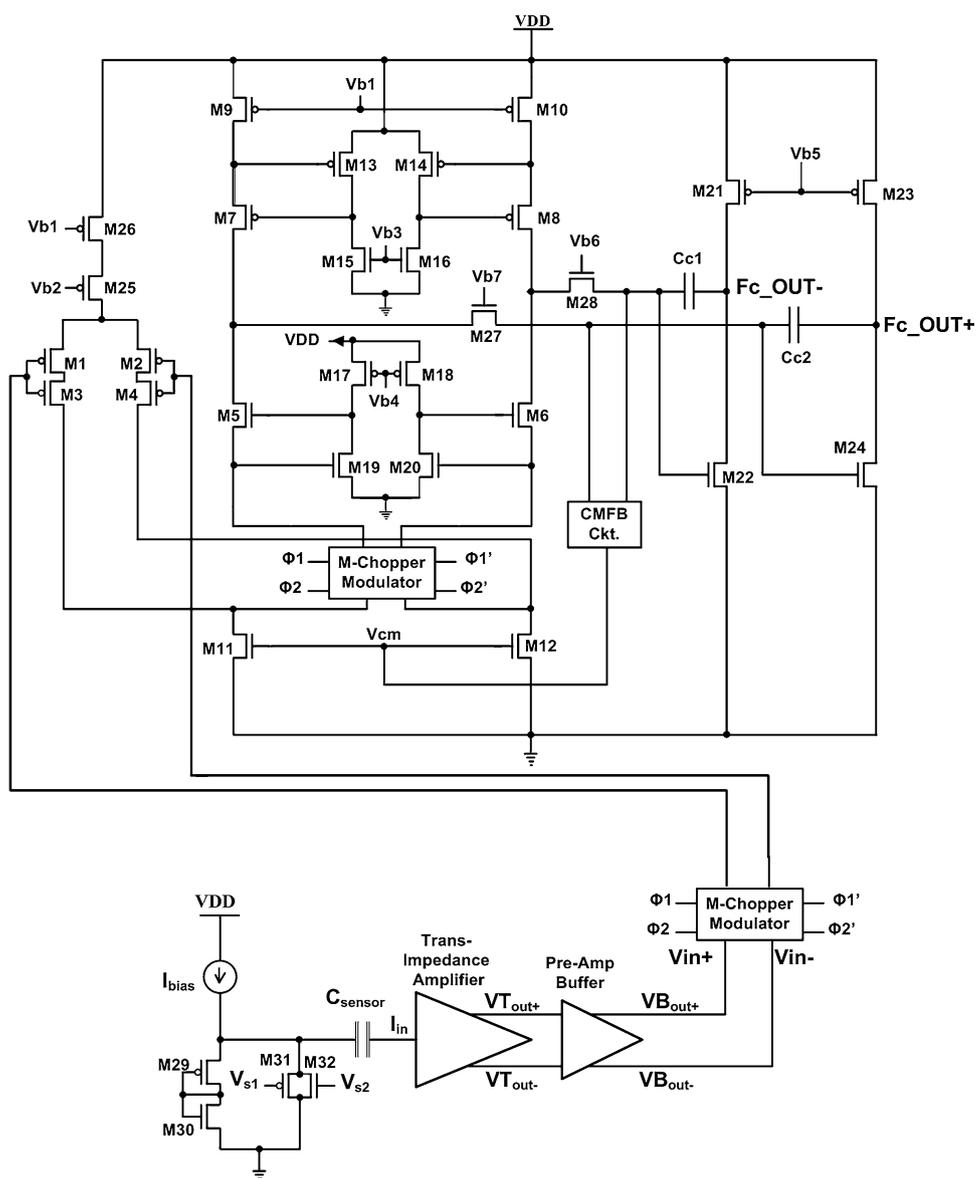
$$\sigma = E\varepsilon \tag{5}$$

where, σ is the stress due to the applied pressure, ε the resulting strain, and E is the modulus of elasticity. An elliptical structure can be considered as a circle pulled along the opposite sides in order to be stretched, and hence, the radius in that direction increases (becomes the semi-major axis), while the area remains unchanged. The deflection, stress and strain analysis of the elliptical structure is thus assumed to be similar to that of an edge clamped circular structure.

2.2 Structural description and fabrication

Figure 3 shows a cross-section of the target CMOS integrated SiGe-MEMS process technology for the pressure sensor (available through Europractice). This SiGe process has a $0.6 \mu\text{m}$ minimum feature size. An elliptical structured micro diaphragm using Poly-SiGe material of spatial axis ($r_1 \times r_2$) dimensions of $100 \mu\text{m} \times 250 \mu\text{m}$ and $4 \mu\text{m}$ thickness, is clamped at the semi-major axis for the curvilinear deformation of the entire diaphragm at low pressure loads. Comparatively, the deflection of any all-edge clamped diaphragm at very low applied pressure, is almost negligible yielding poor sensitivity and low dynamic range

Fig. 4 Modified chopper folded cascode op-amp along with sensor front-end



(Witvrouw 2006). The proposed microstructure is fabricated by stacking on top of the CMOS conditioning circuit used for improving the strength (clarity) of the sensed signal. The low thermal variation of the poly-SiGe material used for the MEMS sensor structure offers minimal thermal drift in the performance of the underlying conditioning circuit MOS devices. The interconnection of the microstructure and the CMOS circuit is through low resistivity poly-SiGe vias. The top aluminum metal layer of the CMOS process is used to connect the electrodes of the capacitive MEMS sensor to bonding pads for test access. The electrical isolation between the MEMS structure and the CMOS circuitry is achieved through a 400 nm thick silicon carbide (SiC) passivation layer. Poly-SiGe anchors of height 3 μm and width 0.8 μm firmly fixes the clamp spring at the edges of the elliptic diaphragm along the

semi-major axis. The clamp spring (along with the planar perforations) overrides the necessity for reducing the thickness of the structure, thus overcoming the sensitivity vs. linearity trade-off. Various arrays of anchors are explored for obtaining specific bending moments at the edges of the diaphragm that can withstand a specified pressure range. As the anchors are semi-conductive, precaution is taken in designing the bottom electrode in order to avoid possible leakage and/or short circuit.

The sacrificial oxide layer (replaced by air-gap dielectric) is etched out through the top-side linearity enhancement perforations of the diaphragm, using them as the structure release holes/vias as well. The dimension of the release holes/perforations is 10 $\mu\text{m} \times 10 \mu\text{m}$ and are spaced at a spatial pitch of 10 μm throughout the diaphragm plane, which as a consequence, results in relatively

less deflection in the high pressure range. The displacement of the diaphragm is 2 μm for an applied pressure of 1,000 hPa, which is half the thickness of the diaphragm. The narrow 3 μm separation between the two plates (determined by the process constrained thickness of the sacrificial oxide layer) limits the dynamic range of the sensor, and as a consequence further thin plate analysis assumption also does not permit larger deflections (beyond the 2 μm range in this case). Generally, deflection beyond half the diaphragm thickness can lead to short circuit/leakage due to pull-in voltage (Nie et al. 2010), however, the perforated elliptic design reduces the pull-in voltage substantially due to lower surface-area of the capacitance, thus providing further improvement in the linearity and dynamic range of the proposed MEMS sensor. Finite element analysis revealed that a deflection of up to 2.2 μm does not significantly deteriorate the sensor performance. The deflection (*w*) of the elliptic diaphragm in thin plate analysis can be easily developed by modifying the analysis for a circular diaphragm in (Ventsel et al. 2001) as follows,

$$w = [So/64Dr_2^2](r_2^4 - r^2r_2^2) \tag{6}$$

where, *S_o* is the applied pressure, *r₂* is the length of the semi-major axis, *r* is the polar coordinate and *D* is the flexural rigidity. As per (6) the diaphragm deflection increases with an increase in the length of the semi-major axis (*r₂*) of the elliptic diaphragm. The maximum deflection is at the center of the diaphragm (*r* = 0) and is determined as follows (Tabarestani et al. 2012):

$$w = Sor_2^2/64D \tag{7}$$

Also, the flexural rigidity, *D* is given by (Hosseini et al. 2007),

$$D = Et^3/12(1 - \nu^2) \tag{8}$$

where, *t* and *ν* are respectively the thickness of the diaphragm and the Poisson’s ratio. Substituting (8) into (7), the deflection of the plate can be given by,

$$w = (r_2^2/t^3)[\{3So(1 - \nu^2)\}/16E] \tag{9}$$

From (9) it is evident that the ratio between the length of the semi-major axis and the elliptic diaphragm thickness directly influences the deflection at the center of the diaphragm. Thin diaphragms can deflect more yielding good sensitivity, however linearity is penalized, hence more importance was given to the characterization of the radial dimensions of the diaphragm, *r₁* and *r₂*. The Poly-SiGe material with its low modulus of elasticity of around 130 GPa (Gonzalez et al. 2012) gives increased deflection even at a very low applied pressure of 100 Pa. This offers the advantage of low minimum detectable pressure, thus increasing the dynamic range of the sensor. Also, for the same surface area, the elliptic diaphragm deflects more under a very low applied pressure compared to a circular diaphragm structure.

3 Read out circuit design

The on-chip sensor interface circuit is a crucial component that converts the low-level transduced sensor output to an useful electronic signal with a low noise factor (Lu and Sou 1998). The weak sensor signal is degraded due to the RC transmission line effect of the electrical interconnect metal wires from the microstructure to the CMOS circuit. Thus sensor signal conditioning poses a significant challenge in designing a comprehensive front-end read-out circuit and the overall performance of the sensor module largely depends on the readout circuit implementation. The circuit performance parameters that are targeted for enhancement are high gain, low noise, low power, reduced area and high linearity. The three main circuit components involved are the modified chopper stabilized op-amp, Gm-C low-pass filter and the self biased buffer stage. Front-end design using the 0.18 μm CMOS deep submicron technology enables higher speed of the analog circuitry but makes high gain amplifier design more challenging. Accuracy and linearity are constrained by the low voltage requirement of deep submicron processes. Furthermore, the low supply voltage constraint also results in performance degradation due to the limited input common mode range (Lipka et al. 2009). The proposed high gain two stage op-amp design for the readout circuit utilizes a gain enhanced folded cascode as the first stage. The composite gain enhancement is achieved by controlling the *g_m*-boosting gain, *A_c* of the doubly *g_m*-boosted cascode. If *g_{mFC}* is the overall transconductance of the folded cascode (FC) amplifier, and *g_m* the input stage transconductance, then, *g_{mFC}* = *g_m*(1 + *A_c*)

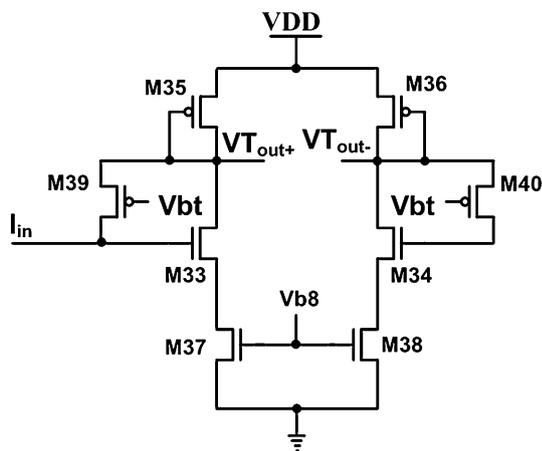


Fig. 5 Transimpedance amplifier and single-ended-to-differential converter of the sensor front-end

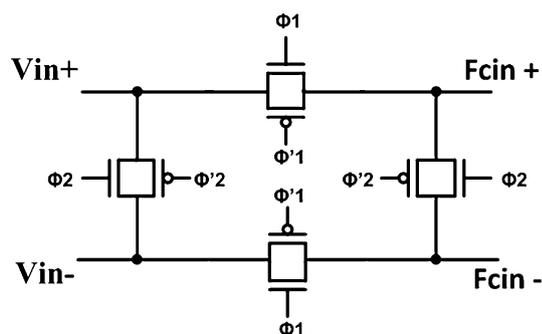


Fig. 6 Modified chopper network using differential transmission gate chopping

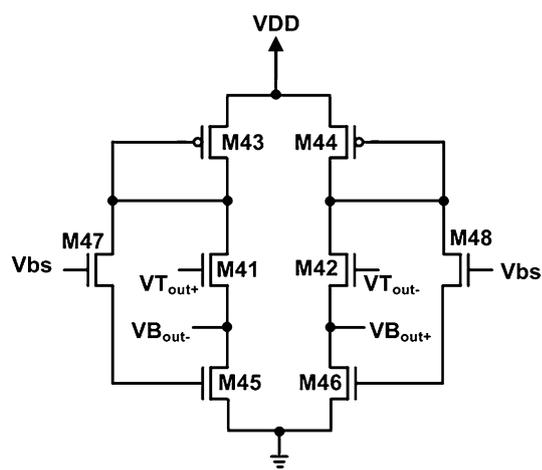


Fig. 7 Differential source-follower pre-amplifier buffer

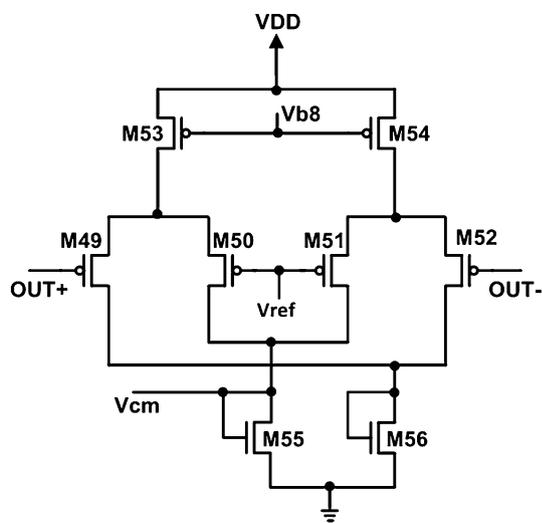


Fig. 8 Differential difference amplifier common-mode feedback circuit

(Berntsen et al. 2005). The negative feedback utilized in the doubly g_m -boosting cascode stage elevates the output impedance leading to gain enhancement. The proposed FC

op-amp yields a higher gain-bandwidth (GBW) product than the conventional folded cascode structure, without increasing the power budget. Stacked PMOS devices are utilized as the input stage of the FC op-amp to further enhance the transconductance. The noise injected by these PMOS devices is an order of magnitude lower than NMOS devices, and hence a relatively low input referred noise is achieved (Lipka et al. 2009). The proposed two stage fully differential FC op-amp shown in Fig. 4 provides large output voltage swing and is less susceptible to common-mode noise compared to a single-ended version. Fig. 5 shows the transimpedance amplifier and single-ended-to-differential converter of the sensor front-end. The total input referred noise power of the FC op-amp can be approximately derived as,

$$\begin{aligned} \overline{V^2 in_noise_{tot}} &= 8KT \left(\frac{2}{3g_{m1,2}} + \frac{2}{3} \cdot \frac{g_{m5,6}}{g_{m1,2}^2} + \frac{2}{3} \cdot \frac{g_{m9,10}}{g_{m1,2}^2} \right) \\ &+ \left[\frac{2K_p}{(WL)_{1,2} \cdot C_{ox} \cdot f} + \frac{2K_N}{(WL)_{5,6} \cdot C_{ox} \cdot f} \cdot \frac{g_{m5,6}^2}{g_{m1,2}^2} \right. \\ &\left. + \frac{2K_p}{(WL)_{9,10} \cdot C_{ox} \cdot f} \cdot \frac{g_{m9,10}^2}{g_{m1,2}^2} \right] \end{aligned} \quad (10)$$

where, K_p and K_N are respectively the PMOS and NMOS flicker noise coefficients. Thermal and flicker noise are the dominant factors that increase the noise floor of the FC op-amp. Two methods were employed to reduce the overall noise; g_m of the input transistors is appropriately increased to reduce the thermal and flicker noise components, and the effective g_m of the current source devices is kept somewhat low so as to reduce noise while not minimizing I_D (in order to maintain reasonable slew rate). Reduction in the g_m of the current sources reduces the output impedances resulting in reduction of the overall voltage gain, and hence, a careful overall gain vs. noise design trade-off is necessary. The composite design of the fully differential chopper stabilization within the FC op-amp structure (with a modified chopping technique) enables improved output signal precision and significant noise reduction, thereby increasing the sensitivity of the front-end. Comparatively, the conventional chopper introduces random spikes at the output causing a residual offset of up to 500 nv/\sqrt{Hz} , which is significantly high for precision sensor application. The modified chopper technique utilizes a transmission gate block to modulate the input signal, thus introducing negligible spikes when demodulated. Figure 6 shows the differential transmission gate chopping network operating with in-phase and out-of-phase chopping frequencies. The employment of two different chopping frequencies along with complementary PMOS choppers makes possible the

Fig. 9 A 4th order elliptic low-pass Gm-C filter for sensor readout (after the FC chopper amplifier)

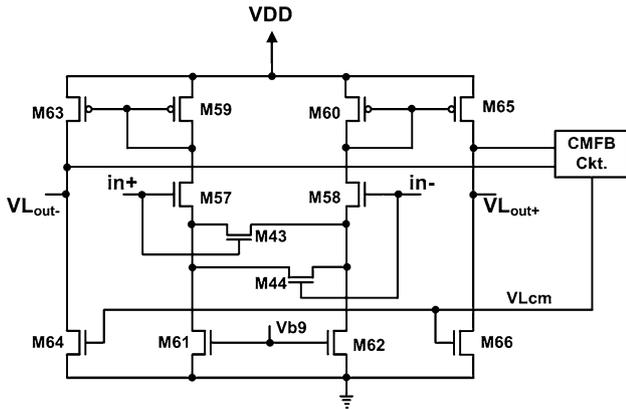
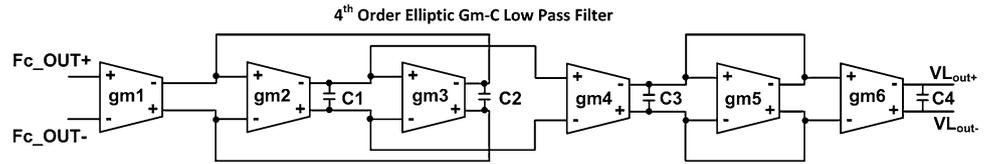


Fig. 10 Circuit diagram of the filter trans-conductance amplifier

reduction of the residual offset to the range of 100 nV/ $\sqrt{\text{Hz}}$. The theoretically achievable improvement in residual offset is given by the ratio of $f_{\text{chophigh}} (\Phi_2)$ and $f_{\text{choplow}} (\Phi_1)$ (Lipka et al. 2009). Furthermore, gain accuracy of the modified chopper is also found to be quite high. The topology of the differential source-follower pre-amplifier buffer is shown in Fig. 7, while the differential difference amplifier common-mode feedback (CMFB) circuit is shown in Fig. 8.

The stability and frequency compensation of the signal conditioning circuit was analyzed by determining the location of the poles and zeros introduced by the parasitic capacitance at different stages. The pole-zero doublet introduced by the g_m -boosting stage degrades the transient response of the op-amp. This doublet appears as a slow

exponential term in the step response increasing the settling time of the op-amp. In order to make the transient response behavior similar to that of a single pole system, the zero, ω_z was pushed to a higher frequency by increasing the drain current (bias current) of the g_m boosting stage. The g_m of this stage was also appropriately adjusted (by varying the device aspect ratios) to transform the pole into a complex conjugate pair (Rezaul Hasan 2005), thus eliminating the slow response introduced by this stage. In addition, pole splitting achieved by miller compensation provides stability to the two stage op-amp (Ribner and Copeland 1984), however it introduces a RHP zero. Increasing the impedance in the feed-forward path pushes the RHP zero to a higher frequency, thereby increasing the stability (Musa et al. 2006). Hence an NMOS transistor biased in the triode regime, in series with the compensation capacitor is used to yield an improvement in stability over the conventional miller compensation technique. Proper choice of the coupling capacitor, C_C (C_{C1} and C_{C2} in Fig. 4) enables the under damping of the settling behavior by setting the phase margin above 45° . However, the increased phase margin causes bandwidth limitations, and hence, a careful bandwidth vs. stability trade-off was implemented. Differential difference amplifier (DDA) common mode feedback is employed in the design to set the common mode output of the op-amp in order to achieve large output swing (Musa et al. 2006). The required output voltage swing is achieved by using the common source (CS) second stage which provides additional gain to improve the overall gain of the op-amp. Simulation results indicate that a gain of 105 dB

Fig. 11 Self-biased output buffer

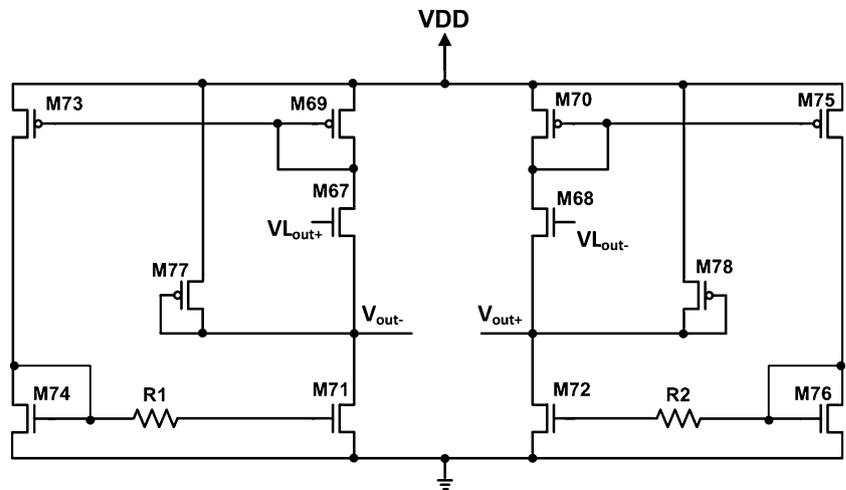


Table 1 Modified chopper FC op-amp stage

| Device | Size |
|----------------|------------------------|
| M1, M2, M3, M4 | 10/0.2 μm |
| M5, M6 | 3/0.6 μm |
| M7, M8 | 3.5/0.6 μm |
| M9, M10 | 2.5/0.6 μm |
| M11, M12 | 4.1/0.6 μm |
| M13, M14 | 60/0.6 μm |
| M15, M16 | 0.2/0.6 μm |
| M17, M18 | 22/0.6 μm |
| M19, M20 | 5.55/0.2 μm |
| M21, M23 | 80/0.6 μm |
| M22, M24 | 4.6/0.2 μm |
| M25 | 20/0.6 μm |
| M26 | 15/0.6 μm |
| M27, M28 | 11/0.18 μm |
| Cc1, Cc2 | 0.25 pF |

Table 2 Transimpedance stage pre-amp and CMFB

| Device | Size (μm) |
|------------------------------|------------------------|
| M29, M30 | 0.2/0.5 |
| M31, M32 | 0.22/0.18 |
| M33, M34 | 0.16/0.5 |
| M35, M36 | 0.26/0.18 |
| M37, M38 | 1.6/0.4 |
| M39 | 0.17/0.5 |
| M40 | 0.5/0.35 |
| M41, M42 | 2/1 |
| M43, M44 | 1/0.6 |
| M45, M46, M47, M48 | 10/0.6 |
| M49, M51, M53, M54, M55, M56 | 0.22/0.18 |
| M50, M52 | 0.22/0.2 |

along with 64° phase margin and $100 \text{ nv}/\sqrt{\text{Hz}}$ input referred noise is achieved by the designed op-amp. A wide unity gain bandwidth of 200 MHz which is sufficient for the pressure sensor duty cycle is also achieved in this design. The compensation capacitors effectively shorts the CS stage NMOS amplifying devices into diode-connected loads for high frequency chopper residuals, thus suppressing these artifacts compared to the sensed pressure signal. However, simulations indicated that a high roll-off low-pass filter was necessary to completely remove the chopping frequency from the output. Gm-C filters provide adequate roll-off behavior even with lower order structures, and is well-suited for sensor signal conditioning. A 4th order low-pass Gm-C filter was thus implemented at the output of the chopper stabilized op-amp. An active resistance is employed in the final trans-conductance stage of the filter in order to reduce attenuation, so that, a low

Table 3 Filter Gm-stage and output buffer

| Device | Size |
|------------|-------------------------|
| M57, M58 | 0.26/0.2 μm |
| M59, M60 | 0.55/0.2 μm |
| M61, M62 | 0.2/0.25 μm |
| M63, M65 | 0.5/0.2 μm |
| M64, M66 | 0.2/0.25 μm |
| M79, M80 | 0.22/0.18 μm |
| M67, M68 | 5/0.7 μm |
| M69, M70 | 1/0.6 μm |
| M71, M72 | 20/0.6 μm |
| M73, M75 | 1/0.6 μm |
| M74, M76 | 0.22/0.6 μm |
| M77, M78 | 10/0.6 μm |
| R1, R2 | 1.5 K Ω |
| C1 | 1 Nf |
| C2, C3, C4 | 0.5 Nf |

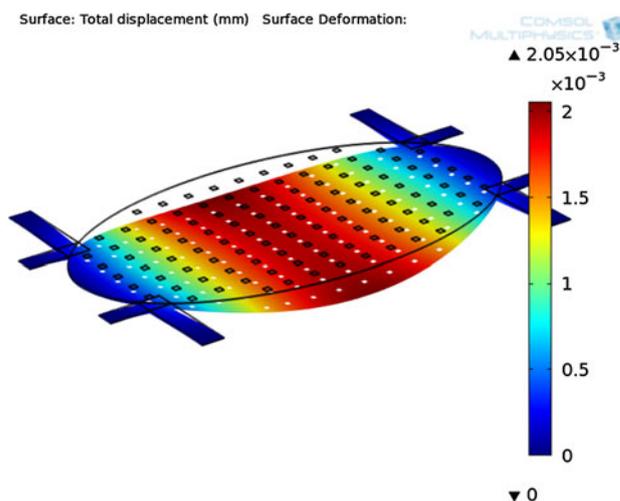


Fig. 12 COMSOL deflection analysis of the perforated diaphragm

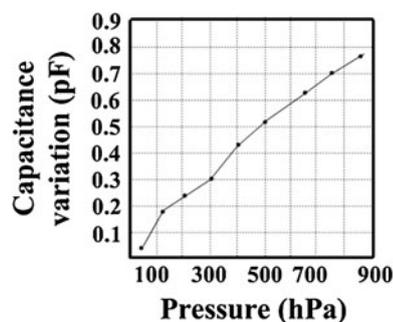


Fig. 13 Capacitance variation with applied pressure

attenuation of -3 dB is achieved for this filter design. Fig. 9 shows the block diagram of the Gm-C filter. The circuit diagram of the filter trans-conductor is shown in Fig. 10.

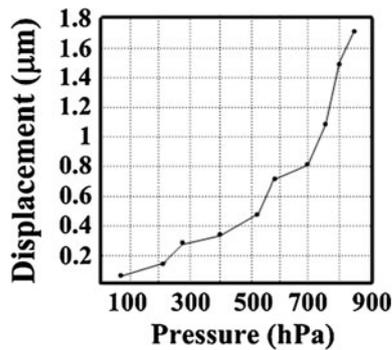


Fig. 14 Displacement variations with applied pressure

Generally, the sensor readout circuit is required to drive an off chip analog-to-digital converter (ADC) for display or for actuation purpose. The high output impedance of the trans-conductance stages within the low-pass filter (after the FC chopper amplifier) is not suited to drive these off-chip devices, and hence a low output impedance buffer driver circuit is required without degrading the overall linearity. Although simple unity-gain buffers can be realized using source followers, they are limited by non-zero offset and nonlinearity. Nonlinearity can be reduced by employing negative feedback but gate-to-source voltage drop of the source follower still introduces offset (Xing et al. 2009). Current feedback can be employed to significantly reduce the output impedance without the need for increased device aspect ratios, so that a reduction in the overall area and power consumption is realized. A self-biased differential source follower is designed using this technique as shown in Fig. 11, which can drive a load of up to 15 pF. The transistor device sizes and component values in the overall signal conditioning circuitry are provided in the Tables 1, 2 and 3.

4 Simulation results

Finite element analysis was carried out in COMSOL Multiphysics for optimizing the dimensions of the elliptic geometry diaphragm. Two important characteristics were targeted in this analysis. Firstly, to determine the capacitance variation with applied axial (perpendicular) pressure and secondly, to observe the corresponding vertical displacement causing the change in capacitance for the entire load sweep. This is critical in studying the linearity of the device as assumption of linearly elastic material model was used to characterize the sensor. Solid mechanics analysis was utilized to study the displacement of the membrane for the applied load pressure. For the parametric pressure sweep, axial load from 10 to 1,000 hPa in steps of 10 hPa, resulted in displacement variation from 0.09234–2.05 µm.

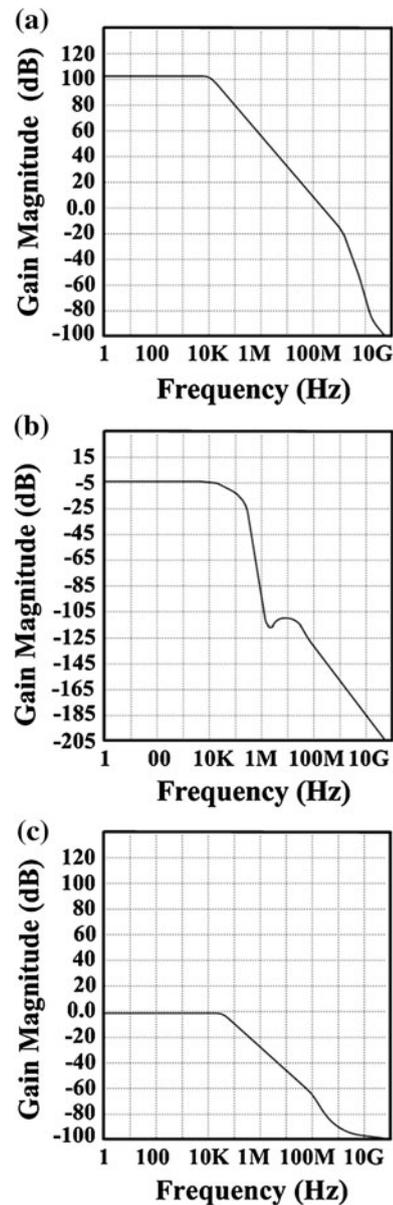


Fig. 15 AC analysis of a modified chopper FC op-amp, b Gm-C low-pass filter and c self-biased output driver/buffer

Moving mesh physical model was assigned for the dielectric layer between the top and bottom solid mechanics plate models in the simulation in order to extract the varying capacitance under the applied pressure. Electrostatic physical analysis was then carried out to acquire the diaphragm surface capacitance and the instantaneous capacitance variation. With the applied bias voltage of 1.4 V, the incremental capacitance variation (ΔC) was between 0.0463 and 0.8213 pF (an increase over the no-load idling diaphragm capacitance of 2.57 pF) due to the deflection of the membrane, under pressure load from 50 to 1,000 hPa. The sensitivity of the sensor is thus calculated to be approximately 0.775 fF/hPa (with around

1 % non-linearity). Figure 12 displays the COMSOL deflection analysis of the perforated diaphragm. Figures 13 and 14, respectively depicts the sensor characteristics in terms of capacitance variation (ΔC) linearity and displacement (Δz) performance with applied pressure load (in the range of 50–850 hPa). The results indicate improved performances in terms of dynamic range, minimum detectable pressure and diaphragm elastic limit.

Design and analysis of the CMOS signal conditioning circuit in 0.18 μm TSMC technology was carried out utilizing Tanner tools. The folded cascode op-amp with the modified input stage and doubly g_m -boosting stage provided an increased transconductance. The gain for the fully differential modified-chopper FC op-amp was found to be around 105 dB. Also, a phase margin of 64° was achieved which proves that the operational amplifier is stable in a closed loop configuration despite the significant open loop gain. Figure 15 shows the frequency behavior of the op-amp, the 4th order Gm-C low-pass filter (with ≈ -3 dB pass-band gain) and the self-biased output driver/buffer

(with ≈ 0 dB pass-band gain). The modified transmission-gate chopper using 10 and 100 kHz chopping frequencies (assuming $1/f$ noise corner frequency at 1 kHz) offered lower spikes compared to conventional chopping as shown in Fig. 16 (lower plot) when excited with a sinusoidal input signal. A high overall sensitivity of 0.17 mV/hPa (@ 1.4 V supply voltage) is achieved for the integrated sensor system. Figure 17 shows the overall pressure vs. output sensor voltage relationship.

5 Conclusion

A highly sensitive integrated capacitive pressure sensor is designed and characterized using a 0.6 μm feature size SiGe MEMS process. The on-chip signal conditioning circuitry is designed in 0.18 μm TSMC CMOS technology vertically integrated (in 3D) with the MEMS process. The capacitive pressure sensor is analyzed under a range of pressure loads. The novel perforated elliptic diaphragm, clamped at the semi-major axis yielded a wide dynamic range. Clamp springs designed to edge clamp the diaphragm increased the sensitivity significantly without degrading the linearity performance. A high gain precision conditioning circuit is designed to cater for the low supply-voltage and weak sensor signal. Simulation of the CMOS circuit is carried out by sinusoidal excitation at the input stage. Non-linearity under 1 % was achieved for the full scale range of applied pressure. This integrated pressure sensor, based on the observed performance characteristics (with overall sensitivity of 0.17 mV/hPa @ 1.4 V supply voltage), with appropriate packaging, can be used for biomedical applications such as catheter pressure monitoring and intraocular pressure measurement.

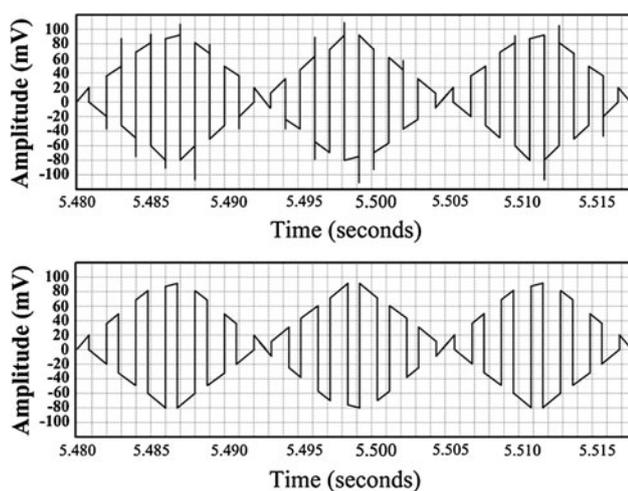


Fig. 16 Modulated input signal by Conventional chopper (*top plot*) with random spikes, and, modified chopper (*bottom plot*) showing negligible spikes

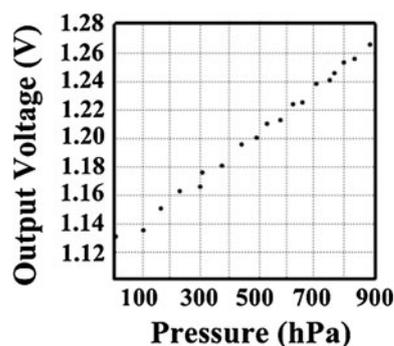
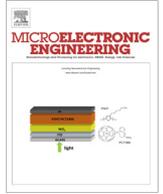


Fig. 17 Applied pressure vs. output sensor voltage using a 1.4 V supply

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Post-processing and performance analysis of BEOL integrated MEMS pressure sensor capacitors in 8-metal 130 nm CMOS



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ABSTRACT

Customized post-processing and characterization of MEMS capacitive pressure sensors in an 8-metal back-end-of-line (BEOL) standard 130 nm “non-MEMS” CMOS technology is reported in this paper. An optimized foundry compatible etch process customized for an IBM CMOS fabricated top triple layered passivation is discussed. A mixture of wet and plasma dry etch process is proposed for both an elliptic and a rectangular structured pressure sensor capacitor. Lateral 125 μm stiction free etch from opposite sides was performed successfully for the integrated diaphragms. Low power inductive coupled plasma using CHF_3 gas along with high RF bias power is utilized to increase lateral etch rate compared to vertical etch rate. Mechanical and electrical characterization indicate a successful etch of the triple layer passivation and the sacrificial silicon dioxide. Sensitivities of the sealed absolute pressure sensors were measured to be 0.07 mV/Pa and 0.05 mV/Pa for the elliptic and rectangular element respectively. In addition, the linear capacitive transduction dynamic range was found to be 32 fF and 23 fF respectively for the elliptic and rectangular element (for 80 hPa pressure variation).

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1. Introduction

Development of mature sacrificial layer etching process in recent years has increased the popularity of surface micro-machined MEMS sensor devices. Monolithic integration of MEMS sensor components and CMOS circuit provides reduced degree of complexity compared to other co-fabrication and hybrid integration techniques. The later is known to suffer from thermal budget constraint in the post-deposition annealing process [1]. The compromised post-process in hybrid integration affects the performance of the MEMS device, as well as, the electronic sensor signal conditioning circuitry.

Many experimental results for release etch process in CMOS MEMS have been reported with either wet etch or dry vapor phase etch (VPE) [2–7]. However, effort to release using only the wet etch poses a serious issue of stiction effect, consequently yielding only an unsuccessful release of the device membrane. Use of only the VPE dry etch, on the other hand, leaves a residue with rough surfaces, affecting the reliability of the released MEMS device. Most of the CMOS integrated MEMS post-processing work reported so far utilizes only at most a 4-metal layer CMOS process (an early

generation CMOS process). This paper has addressed these post-processing issues and has proposed a mix of wet and inductive plasma dry BEOL release etch, experimentally performed on a modern 8 metal 130 nm CMOS process [8] overcoming these limitations. This process contains 3 thin lowest metal layers (M1, M2 and M3), 2 middle thick metal layers (MQ and MG) and 3 thick top (upper) RF metal layers (LY(Al), E1(Cu) and MA(Al)). The capacitive sensor is constructed in the region of the 3 upper metal layers. The top MA (Al) layer of the BEOL is the diaphragm (top electrode) and the third metal layer, LY (Al) is the bottom electrode. The intermediate E1 (Cu) metal layer was designed as a mesh to act as a test structure during post-processing. Moreover, there are two fabricated sensor geometries (elliptical and rectangular diaphragms) which can be connected with an on-chip active switch to form a parallel variable capacitance. Exploring the merger of intricate customized MEMS sensor fabrication processing on today’s advanced deep nano-metric “non-MEMS” digital CMOS process technologies for single chip sensor-merged-microprocessor-microsystem design is the targeted contribution of this work. This can result in pre-determined mask layout layers (post-CMOS layers) for MEMS sensor release as a contiguous integrated CMOS foundry mass production process from design tape-out to foundry wafer/die ship-out of the complete sensor micro-system.

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2. Etching lithography

The three main processes in this post processing are passivation etch, trench formation and lateral etch. Two mask writing steps that uses direct on wafer writing (DWW) are used to perform the complete customized MEMS etching process, as well as, protect the side walls (preserving the sensor anchors) on the standard 130 nm IBM CMOS die. The first mask defines the area of the passivation etch that exposes the diaphragms, while the second mask defines the trench and under etch (lateral etch) areas. The 9 mm² die specimen is taped on a 1 cm² dummy (100) wafer for spin coating. After cleansing and initial aerated drying, it is then dried on a hot plate for 30 s at 75 °C. The total triple layer passivation thickness being 4.3 μm, requires a photo-resist thickness of at least 7 μm, so that considering even a 1:1 selectivity ratio, the resist will remain in place for the entire dry plasma passivation etch process. The resist is optimized for spin duration, spin speed and resist quantity by trial runs on a dummy wafer. The sample is spin coated at an angular velocity of around 4000 rpm for 40 s using a thick AZ4620 series photo-resist. Prebake is carried out at 75 °C for 10 s to dry the solvent remnants. The specimen is then subjected to DWW using a Micro-tech LW405A laser writer. Even though the DWW used in this work is at the die level, the same type of resist and methodology is also compatible with pre-determined design-rule driven wafer level foundry process. The masked specimen is developed in diluted KOH solution for 6 min. The top polyimide layer of the die served as a protective layer for the underlying CMOS circuits. The specimen is then hard baked at 125 °C for 4 min to enhance resist adhesion. This proposed MEMS post-processing mostly uses plasma process at low chamber temperature for sensor structure release; hence risk of degradation in the circuit interconnects and vias are not present as reported in [4], where the die is exposed to high thermal budget release (at 535 °C). Details of the lithographic process can be found in [Supplementary data Section 1](#).

3. Passivation etch process

The triple layered passivation sandwich in the 130 nm CMOS technology has a top polyimide layer, a middle silicon nitride (Si₃N₄) layer and a bottom silicon dioxide (SiO₂) layer. The dry plasma based reactive ion etching (RIE) method which provides an almost anisotropic etch is employed for the customized passivation cut.

3.1. Polyimide Etch

Oxygen plasma is used for the polyimide cut. The process parameters are optimized through trial-run on a dummy sample. To this end, polyimide of thickness 2.5 μm is first sputtering-deposited on a sample wafer for test etching. The chamber pressure is maintained at 600 mTorr. A low RF coil power of 100 W along with a high inductively coupled plasma (ICP) power of 1000 W is applied while maintaining the chamber temperature at 0 °C. The ICP power is applied from the top through inductive RF energy transfer, while, the RF coil (or, RF bias) power is applied at the substrate plate for better anisotropic etch. Both RF sources are at 13.56 MHz. The sample is etched for 5 min using oxygen with 50 standard cubic centimeter per minute (sccm) flow rate. Step height analysis using an atomic force microscope (AFM) revealed that the polyimide is etched down to 0.7 μm. The process is repeated for 5 more minutes with an increased ICP power of 1200 W resulting in a cut depth of about 2.5 μm, thus concluding the successful trial etch. The etch is next performed on the specimen using this optimized recipe. Step height analysis verified the depth of the actual etch.

3.2. Silicon nitride and silicon dioxide etch

Silicon nitride, in the passivation is 0.45 μm thick. RIE dry etch using sulfur hexafluoride (SF₆) plasma with 45 sccm flow rate is utilized to achieve good vertical side walls. Wet etch is not used at this stage in order to minimize side wall under cuts. In addition, fluoroform (CHF₃) at 30 sccm flow rate is added to the SF₆ plasma for better anisotropy. Increased anisotropy will avoid the lift-off of the diaphragm anchors during subsequent isotropic wet etch. Using 40 mTorr chamber pressure at 0 °C, 20 W RF coil power and 250 W ICP power a good vertical silicon nitride etch-rate was achieved. After an initial etching for 40 s, step height analysis revealed 0.38 μm etch-depth, hence an additional etch for 8 s was performed. The etch-rate for the 48 s duration was thus 580 nm/min. The final dry passivation silicon dioxide layer etch was performed using CHF₃ plasma at 40 sccm. Process parameters of 1500 W ICP power, 50 W RF coil power and 5 mTorr chamber pressure at 0 °C, yielded the required etch depth of 1.35 μm. The specimen was etched for 6.3 min, for which the etch rate was 500 nm/min.

3.3. Photoresist stripping

The 7 μm thick photoresist survived the three dry passivation etch steps. Although the top few micrometers of resist gets stripped off, prebake during the lithography process makes the underlying resist layers stick to the chip surface. On the other hand, the exposed diaphragm metal could be damaged by the use of any strong solvents. Considering all possible avenues, combination of repeated oxygen plasma ashing along with wet acetone sonicator cleaning was implemented to strip-off the photo-resist. Eight minutes of ashing, followed by 10 min of acetone sonicator cleaning completely stripped off the resist. This optimized cleaning procedure is quite compatible with wafer level manufacturing. The cleaning (removal) period is short enough to not lower the yield in a wafer level mass production setup.

Details of passivation etching and resist stripping can be found in [Supplementary data Section 2](#).

4. Release etch process

Thin photoresist (≈ 1 μm) is used for the second DWW lithography (mask 2) for trench and lateral etches (release etch) with KOH development time of less than 2 min. Mask 2 layout is designed such that the mask window is well away from the side-wall anchor region. A combination of dry plasma and wet etch was adapted for the diaphragm release in this customized MEMS on 130 nm IBM CMOS die. The wet pre-lateral etch was carried out for a longer duration than usual to secure a lateral micro-vent (orifice) for subsequent 125 μm dry lateral release. The intermediate copper mesh test structure (the E1 layer) was designed in the form of 10 μm × 10 μm squares spanning the size of the diaphragm, and, held together by the intervening silicon dioxide layer.

4.1. Trench formation

RIE using CHF₃ plasma with 50 sccm flow-rate is used in this first phase of dry release etch. Silicon dioxide layers on either side of the diaphragms are etched 5 μm vertically to form trenches. Dry etch with 2000 W ICP power and 50 W RF bias power yields a higher vertical etch rate than lateral etch rate [9] thus forming box like trenches of dimensions 100 μm × 80 μm × 5 μm. The process pressure was kept at 5 mTorr (at 5 °C). The specimen is etched for 9.5 min yielding a 530 nm/min dry etch rate. Diluted KOH rinsing is carried out to remove any piles of silicon dioxide after the RIE

[10]. The thin resist gets stripped-off during this etch, hence a repeat lithography is necessary for further under etch (lateral etch) process.

4.2. Wet under etch

Buffered HF (BHF) with 300 nm/min etch-rate was used for the wet under-etch (pre-lateral etch). BHF etch being isotropic causes few micrometers of lateral SiO₂ etch below the diaphragm thus providing an easy start-up for subsequent lateral dry etch. The 4 μm thick diaphragm (the top MA aluminum) can withstand the aqueous HF chemistry of vertical SiO₂ etch of up to 7 μm. To avoid damages at the sides of the diaphragm, wet etch time is thus limited to an etching depth of 7 μm; hence the specimen is kept in the solution for approximately 20.4 min. Since the SiO₂ etch-rate of 300 nm/min using BHF can strip-off the resist in 10 min, the lithographic process is repeated after the first 10 min. Even though this process involves two steps of lithography, it is less expensive compared to the vapor phase HF (VP HF) etch method. The yield, if mass production is conducted will be comparable to that using VP HF.

4.3. Dry lateral etch

Dry release etch is preferred to avoid stiction issues. CHF₃ plasma is employed to perform an under (lateral) etch of 125 μm on either side of the diaphragm through the trenches for a full device release. DWW mask features are designed to allow the ion bombardment on the sacrificial SiO₂ through the trenches and lateral micro-vent, thereby enabling lateral etch under the diaphragms. Faster lateral etch can be achieved with high RF bias power and low ICP power [9]. Process parameters were optimized by first performing a trial run on a dummy wafer. The run showed a 50 nm/min lateral etch rate for a chamber pressure of 10 mTorr at 5 °C. On the actual specimen 125 μm lateral-etch required 40.8 h of CHF₃ plasma etch. The chamber temperature was maintained at 5 °C while RF bias power was increased to 400 W with ICP power lowered to 20 W. The lithographic patterning was repeated every 2 h to make sure the diaphragm is not exposed. Using thick

photoresist the number of lithography steps can be reduced. The Si₃N₄ layer above the bottom electrode plate (the LY metal layer) served as the etch stop layer, hence with the lateral etch of 125 μm, vertical etch was reduced considerably. The CHF₃ plasma with 25 sccm flow rate also provided good selectivity between SiO₂ and Si₃N₄, and hence, the bottom electrode was well protected. Table 1 lists the complete dry etch process steps. The copper mesh test structure falls off during the lateral etch. After release, it was mostly removed through acetone sonicator cleaning.

4.4. Post-release etch

Post release etch process for removal of Si₃N₄ isolation layer is necessary to avoid composite dielectric medium in the capacitive sensor devices. However, as an inherent advantage, it defends the bottom electrode from residue formation due to the carbon rich CHF₃ plasma. Furthermore, the isolation layer has protected the capacitive device against pull-in or break-down. The Si₃N₄ etch recipe mentioned in Section 3.2 is repeated in this etch but with low ICP power and high RF bias power.

Table 2 shows the comparison of various reported CMOS MEMS devices with this work. The comparative advantage of the proposed technique is quite evident from the table, with the achievement of a two-sided anchored 250 μm laterally etched diaphragm. The detailed cross-section of the stages in this customized MEMS release process for the standard 130 nm IBM CMOS die is shown in Fig. 1.

4.5. Post release sealing

The released device is next sealed as an absolute pressure sensor. The trench areas are sealed by depositing and patterning fluorosilicate glass [11] by plasma enhanced chemical vapor deposition (PECVD) in moderate vacuum at 0.5 Torr inside a reactor. The operating temperature of 225 °C (for sealing) during PECVD deposition process does not degrade the CMOS interconnects and vias. Plasma cleaning is carried out at the completion of the deposition process.

More details of the release process is available in Supplementary data Section 3.

Table 1
Dry etch process details.

| Etching layer | Gas | Flow rate (sccm) | Process pressure (mTorr) | ICP power (W) | RF power (W) | Etching time & rate |
|-------------------|-------------------------------|------------------|--------------------------|---------------|--------------|-------------------------|
| Polyimide | Oxygen | 50 | 60 | 1200 | 100 | 10 min. & 250 nm/min. |
| | C ₄ F ₈ | 3 | | | | |
| Nitride | SF ₆ | 45 | 40 | 2500 | 20 | 0.48 min. & 580 nm/min. |
| | CHF ₃ | 30 | | | | |
| Passivation oxide | CHF ₃ | 40 | 5 | 1500 | 50 | 6.3 min. & 500 nm/min. |
| Trench oxide | CHF ₃ | 50 | 5 | 2000 | 50 | 9.5 min. & 530 nm/min. |
| Sacrificial oxide | CHF ₃ | 25 | 10 | 400 | 20 | 2448 min. & 50 nm/min. |

Table 2
Feature comparison of various reported CMOS–MEMS devices.

| Device reported | Number of metals | CMOS technology | Type of sacrificial release etch | Risk of stiction effect | Lateral release length (μm) | Device anchored | Post process thermal budget used (°C) |
|-----------------|------------------|----------------------------|----------------------------------|-------------------------|-----------------------------|-----------------|---------------------------------------|
| This Work | 8 | 0.13 μm IBM CMOS | Wet & plasma RIE etch | No | 250 | Two sided | 125 |
| [1] | 4 | 0.35 & 0.18 μm TSMC | Wet etch | Yes | Up to 178 | One sided | <350 |
| [2] | 4 | 0.35 μm BiCMOS | Wet etch | Yes | 95 | One sided | 180 |
| [3] | 4 | – | RIE plasma etch | No | 80 | One sided | 120 |
| [4] | 5 | 0.25 μm SiGe BiCMOS | Wet etch | Yes | 30 | Two sided | 450 |
| [5] | 3 | 0.6 μm Austria microsystem | DRIE plasma etch | No | 250 | One sided | 225 |
| [6] | 1 Poly 6 metal | 0.18 μm TSMC | Wet etch | Yes | 6.05 | One sided | 125 |
| [13] | 2 Poly 4 metal | 0.35 μm TSMC | Wet etch | Yes | 158 | One sided | 125 |

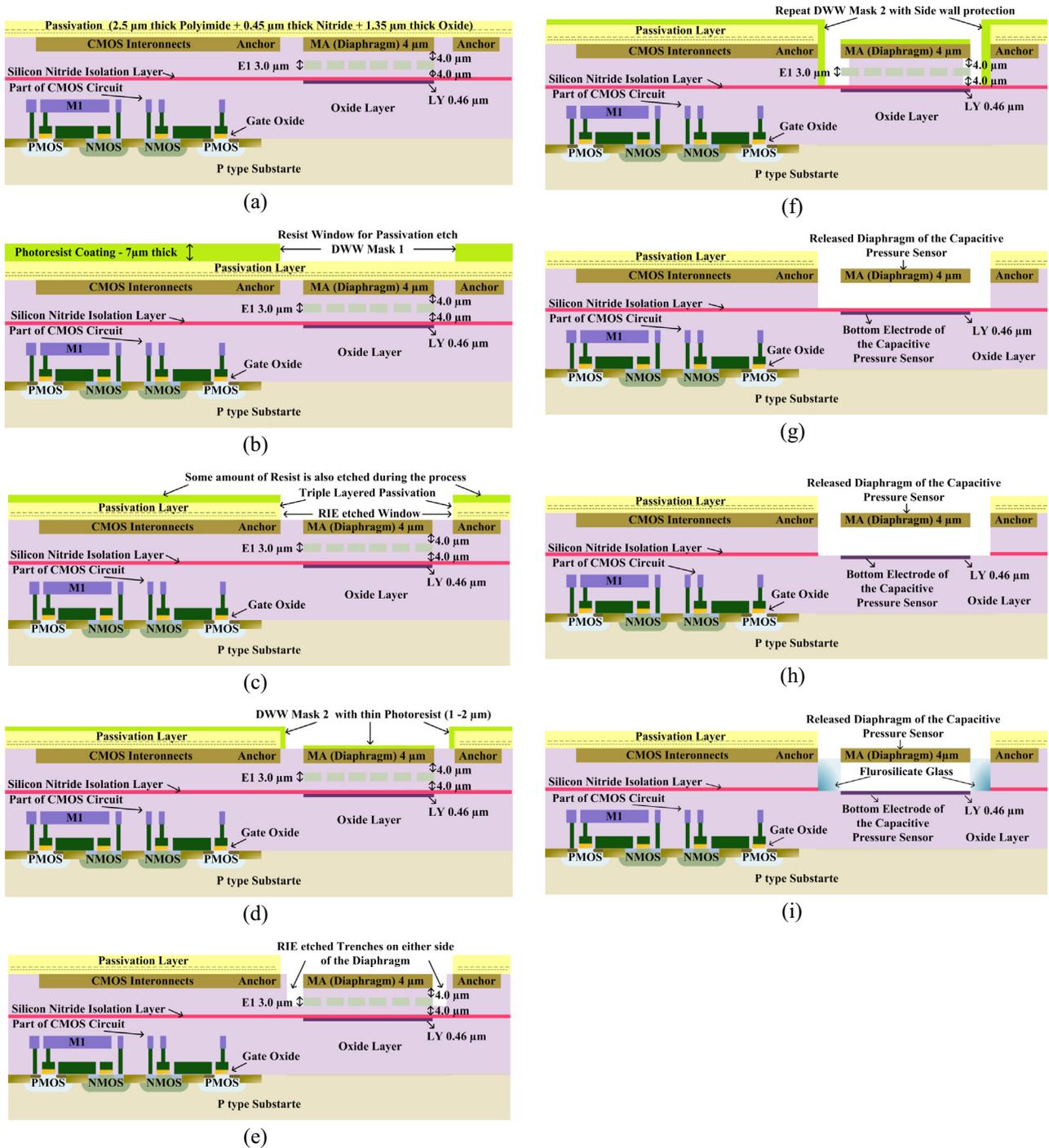


Fig. 1. Cross-sections of the step-by-step customized MEMS release process, (a) initial CMOS chip with circuitry and unreleased MEMS capacitors, (b) lithography with thick resist (DWW patterning mask 1), (c) after passivation etch, (d) lithography with thin resist (DWW patterning mask 2), (e) after dry trench etch, (f) lithography with thin resist (DWW patterning mask 2 repeat with sidewall protection), (g) after wet etch and following dry etch (composite etch) whereby the copper mesh falls off, (h) after post release etch, (i) after post release fluorosilicate sealing.

5. Characterization

5.1. Mechanical characterization

The etch (cut) depth at the completion of each process can be determined through AFM step height analysis. For this purpose a surface topography is carried out using the Bruker AFM Dimension Icon instrument. A fixed frequency of 2 kHz is used in the Peak Tapping Mode. Table 3 summarizes the step height measured at various process steps. The maximum scan size is set to 90 μm of

which the midpoint is set at the junction of the etched window to get minimal artifacts in the images. The analysis is repeated several times to obtain accurate results.

5.2. Electrical characterization

The full exposure of the diaphragm was verified through electrical conductivity analysis using the Agilent device analyzer B 1500A with 5 MHz pulsed source. The measured pull-in voltages were 38.8 V and 39.2 V for the elliptic and rectangular devices

Table 3
AFM step height analysis results.

| S. No | Specimen analysis state | Step height (μm) |
|-------|--|-------------------------------------|
| 1 | First resist coated (corresponding to Fig. 1(b)) | 7 |
| 2 | Polyimide etched | 8.3 (Resist is attacked) |
| 3 | Nitride etched | 7.8 (Resist is further stripped) |
| 4 | Passivation oxide etched (corresponding to Fig. 1(c)) | 6.3 (Resist continued to strip off) |
| 5 | Resist stripped | 4.3 |
| 6 | Trenched & resist removed (corresponding to Fig. 1(e)) | 8.3 |

respectively. Also the resistance between the MA and LY plates at pull-in (just before touch-down) were 13.57 M Ω and 16.74 M Ω respectively for the elliptic and rectangular diaphragms including the diaphragm-anchors.

Details of characterization is available in [Supplementary data Section 4](#).

6. Sensor measurements and experimental results

The hermetically sealed capacitive sensors does not require tedious vacuum electrical lead transfer techniques as this is taken care of during the interconnect metallization process. The sensor interconnections with on-chip CMOS readout circuit are routed through the bottom BEOL metal stack (M1/M2/M3), and hence these metalizations are not in proximity to the region of release etch and vacuum sealing. The experimental test system has an inherent advantage of low noise setup, as no interconnections with external readout circuitry that can pick up noise and render stray capacitances is required. An on-chip high gain g_m -boosted operational trans-conductance amplifier (OTA) provides sufficient amplification for this low frequency sensor output. Using switching pins the readout circuit can connect to each sensor individually or to a parallel connection of both the diaphragms. The measured physical dimensions of the elliptic and rectangular sensing diaphragms were 430 μm \times 289 μm and 262 μm \times 514 μm respectively. In addition to integrated read-out circuit pins, the capacitive sensors can also be accessed directly via bottom and top plate interconnect pins (for external signal conditioning option). The stable capacitances measured at zero applied pressure were 116 fF and 123 fF for the elliptic and the rectangular sensing elements respectively. In addition, the capacitive transduction dynamic range was found to be 32 fF and 23 fF respectively for the elliptic and rectangular element (for 80 hPa pressure variation)

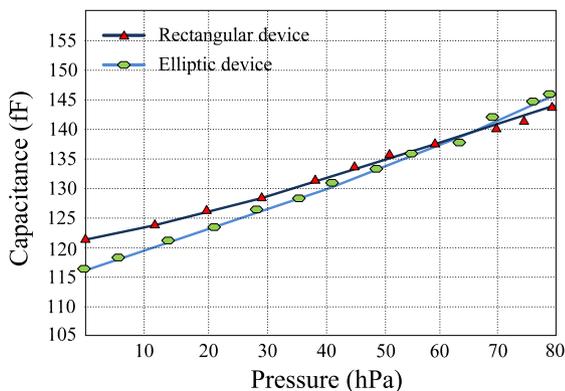


Fig. 2. Performance of the elliptic diaphragm and rectangular diaphragm capacitive sensor devices.

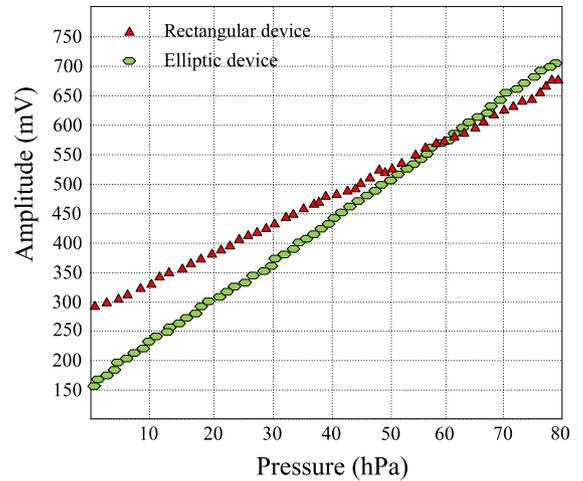


Fig. 3. Sensing circuit transduction response with applied pressure.

as shown in Fig. 2. Over the measured pressure range, the elliptic element provided better sensitivity of 0.4 fF/hPa compared to the rectangular element for which the sensitivity was 0.29 fF/hPa. The elliptic diaphragm exhibited slightly higher linearity compared to the rectangular diaphragm within its dynamic range. Device sensitivity was observed to be marginally higher in the higher range of applied pressure (40–80 hPa). The test system used a low 1.2 V supply, so that the power dissipation with both capacitive devices employed along with the sensing circuit was found to be as low as 425 μW . The maximum sensitivity at the output pins of the readout circuit for a pressure range of up to 100 hPa

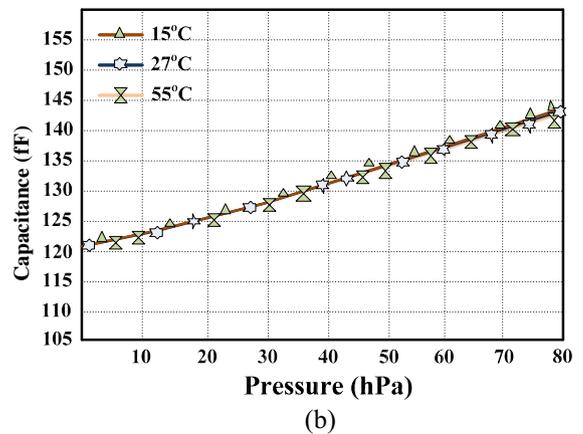
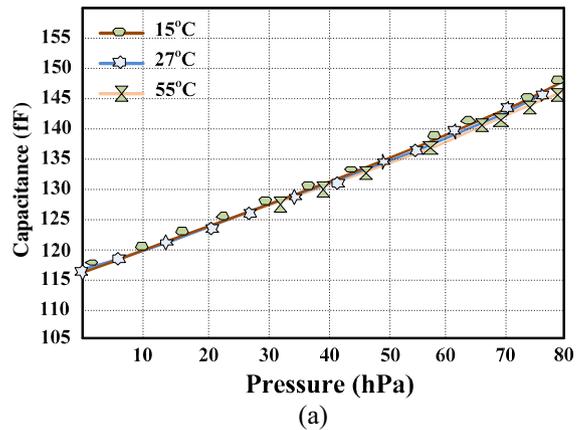


Fig. 4. Temperature dependency of (a) elliptic diaphragm element, and, (b) rectangular diaphragm element.

is found to be 0.07 mV/Pa for the elliptic element and 0.05 mV/Pa for the rectangular device as shown in Fig. 3. Thermal coefficient of the capacitive sensor is critical for the linearity aspect of the device. Although capacitive sensors are mostly independent of temperature variations compared to piezo-resistive sensors, marginal decreases (*nonlinear behavior*) in the capacitance (at the higher pressure range) were observed when the chamber temperature is increased above room temperature (27 °C). The sensor capacitances were measured for three different temperatures (15 °C, room temperature and 55 °C) as shown in Fig. 4(a) and (b). The average capacitance drift was around 2.5 fF over a range of 20 °C temperature variation. In general, decrease in the capacitance in the order of few fFs was observed in the higher pressure range from 60 hPa to 100 hPa for the elliptic device and 75 hPa to 100 hPa for the rectangular device. This is possibly due to the non-uniform diaphragm stress distribution over higher pressure ranges (at higher temperatures). The observed hysteresis and repeatability (*test–retest reliability*) for the elliptic element were 0.045% and 0.02% point of reading respectively. On the other hand, the hysteresis was lower in the rectangular element with 0.024% but a moderate repeatability of 0.05% was noted in this case. The residual tensile stress in the diaphragm was low at approximately 11 MPa, which is lower than that in anchored polysilicon structures fabricated in multi-user MEMS (MUMPS) processes. Linear buckling analysis indicated that the aluminum membrane can withstand a comparatively higher stress of around 500 MPa compared to a similar geometry polysilicon membrane which can break at around 300 MPa. Some of the details of the measurement setup is provided in the [Supplementary data Section 5](#).

7. Conclusion

Successful customized MEMS capacitive sensor release etch employing a mixture of wet and plasma dry etch on a “*non-MEMS*” 8-metal 130 nm standard CMOS process has been demonstrated. Lateral under etch of 125 μm from opposite sides between the diaphragm (*top MA electrode*) and the bottom plate (*LY electrode*) was achieved without damaging the anchors and the underlying CMOS circuitry. The highly compact 8 metal layer customized CMOS MEMS allows smaller line-width and hence offers lower parasitic effects compared to those reported in [12–16] for micro-systems design. An optimized technique of resist stripping without damaging the exposed aluminum diaphragms was also verified. The comparatively low cost CHF₃ plasma etch yielded a smooth surface with no residues, hence avoiding the need for strong wet chemicals that attacks aluminum diaphragms and are associated with stiction effects. The fabricated intermediate copper mesh test structure (*E1 layer* of the BEOL stack) falls off during the release etch, thus confirming the full release of the diaphragm through microscopic observation. Thermal budget for the 0.13 μm CMOS circuitry is

taken into consideration and any process that required more than 225 °C temperature is eliminated from the post-process flow for protecting the on chip CMOS circuits. The released sensor capacitors were mechanically and electrically characterized and experimental measurements of the transduction behavior was also carried out in terms of sensitivity, dynamic range, hysteresis and repeatability. The test results indicate that the elliptic structured device has better overall performance in terms of sensitivity and dynamic range compared to the rectangular device.

Acknowledgments

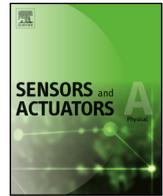
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Appendix A. Supplementary data

Supplementary data associated with this article can be found, in the online version, at <http://dx.doi.org/10.1016/j.mee.2014.02.035>.

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Release etching and characterization of MEMS capacitive pressure sensors integrated on a standard 8-metal 130 nm CMOS process



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ABSTRACT

Monolithic post-processing and characterization of CMOS MEMS capacitive absolute pressure sensors co-integrated on an 8-metal BEOL (back-end-of-line) 130 nm CMOS device is reported in this paper. An optimized foundry compatible etch process for an IBM CMOS fabricated top triple layered passivation is discussed. A mixture of wet and plasma dry etch process is proposed for both an elliptical and a rectangular structured pressure sensor capacitor. Lateral 125 μm stiction free etch from opposite sides was performed successfully for the monolithically integrated diaphragms on the 130 nm CMOS platform. Low power inductive coupled plasma using CHF_3 gas along with high RF bias power is utilized to increase lateral etch rate compared to vertical etch rate. Mechanical and electrical characterization results indicate a successful etch of the triple layer passivation and the sacrificial oxide. Sensitivities of the fluorosilicate sealed absolute pressure sensors were measured to be 0.07 mV/Pa and 0.05 mV/Pa for the elliptical and rectangular element, respectively. In addition, the linear capacitive transduction dynamic range was found to be 0.32 pF and 0.23 pF, respectively, for the elliptical and rectangular element (for 80 hPa pressure variation).

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1. Introduction

The development of mature sacrificial layer etching process in recent years has increased the popularity of surface micro-machined MEMS component design. Monolithic integration of MEMS sensor components and CMOS circuit provides reduced degree of complexity compared to other co-fabrication and hybrid integration techniques. The later is known to suffer from thermal budget constraint in the post-deposition annealing process [1]. The compromised post-process in hybrid integration affects the performance of the MEMS device, as well as, the electronic sensor signal conditioning circuitry. Many experimental results for release etch process in CMOS MEMS have been reported with either wet etch or dry VPE (vapor phase etch) [2–7]. However, effort to release using only the wet etch poses a serious issue of stiction effect, consequently yielding only an unsuccessful release of the device membrane. Use of only the VPE dry etch, on the other hand, leaves a residue with rough surfaces, affecting the reliability of the released MEMS device. Most of the CMOS integrated MEMS post-processing

work reported so far utilizes only at most a 4-metal layer CMOS process (an early generation CMOS process). This paper has addressed these post-processing issues and has proposed a mix of wet and inductive plasma dry release etch, experimentally performed on a modern 8 metal BEOL 130 nm CMOS process [8] overcoming these limitations. This process (also known by the acronym 8RFD) contains 3 thin lowest metal layers (M1, M2 and M3), 2 middle thick metal layers (MQ and MG) and 3 thick top (upper) RF metal layers (LY(Al), E1(Cu) and MA(Al)). The co-integrated capacitive sensor is constructed in the region of the 3 upper metal layers. The top MA (Al) layer of the BEOL is the diaphragm (top electrode) and the third metal layer, LY (Al) is the bottom electrode. The intermediate E1 (Cu) metal layer was designed as a mesh to act as a test structure during post-processing. Moreover, there are two fabricated sensor geometries (elliptical and rectangular diaphragms) which can be connected with an on-chip active switch to form a parallel variable capacitance, thereby, avoiding curling effects which occurs in a multi-finger design based variable capacitive device [2]. Exploring the merger of intricate MEMS sensor fabrication processing on today's advanced deep nano-metric digital CMOS process technologies for single chip sensor-merged-microprocessor-microsystem design is the targeted contribution of this work. This can result in pre-determined post processing mask layout layers (post-CMOS layers) for MEMS sensor release as a contiguous integrated CMOS

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foundry mass production process from design tape-out to foundry wafer/die ship-out of the complete sensor micro-system. The paper is organized as follows: In Section 2, a brief overview of the photolithographic process and resist coating technique is discussed. Section 3 describes the etching process for the triple layer passivation in creating the diaphragm devices. Next, Section 4 depicts the 125 μm lateral release etch technique. In Section 5, the mechanical and electrical characterization of the diaphragms, and, in Section 6 the experimental results for the capacitive pressure sensors are discussed. Finally, in Section 7 the concluding remarks are provided.

2. Etching lithography

The three main processes involved in this advanced CMOS MEMS post processing technique are passivation etch, trench formation and lateral etch. Hence, the etching lithography consisted of several stages; first stage for dry passivation etch, second stage for dry trench etch, third stage for side wall protection and wet etch, and, the last stage for dry lateral release. The composite post-process cross-section diagrams in Fig. 6 depicts these lithography stages in the context of the entire CMOS MEMS post-processing in details. Maskless patterning reported in [3] causes reduction in the thickness and sensitivity of diaphragms, hence at least two mask writing steps that uses DWW (direct on wafer writing) are required to perform the complete etching process, as well as, protect the side walls (preserving the sensor anchors). The first mask defines the area of the passivation etch that exposes both the elliptic and rectangular diaphragms, while the second mask defines the trench and under etch (lateral etch) areas. The second mask is repeated several times, as the photo-resist tends to get stripped-off during long etching durations. The specimen being a 9 mm² naked die is taped on to a 1 cm² dummy (100) wafer using a special double-sided ultra-tape, for spin coating. Choice of the tape is quite critical; as it should be both particle free and residue free, otherwise, it will yield poor thermal transfer during dry etch. An ultra-clean tape containing minute leachable metals with polyethylene backing and acrylic adhesion is used. The dummy wafer with the attached die specimen is cleaned initially using acetone [(CH₃)₂CO] to remove atmospheric dust. After initial aerated drying, it is then dried on the hot plate for 30 s at 75 °C. The total triple layer passivation thickness being 4.3 μm , requires a photo-resist thickness of at least 7 μm , so that considering even a 1:1 selectivity ratio, the resist will remain in place for the entire RIE (dry plasma etching) passivation etch process. The resist is optimized for spin duration, spin speed and resist quantity by trial runs on a dummy wafer before actually trying on the specimen. The sample is spin coated at an angular velocity of 4000 rpm for 40 s using a thick AZ P4620 series photo-resist. For the first five seconds the spin coater runs at 500 rpm for slow even coating throughout the surface of the wafer. This slow startup avoids resist lumps or bubble formation at the edges of the actual specimen. In addition, the coater is also slowed down to 500 rpm for the last 5 s at the end of the 40 s duration. Prebake is carried out at 75 °C for 10 s on a hot plate to dry the solvent (acetone moisture). The specimen is then subjected to DWW using a Micro-tech LW405A Laser Writer as shown in Fig. 1. Even though the DWW used in this work is at the die level, the same type of resist and methodology is also compatible with pre-determined design-rule driven wafer level foundry process. The etching mask layout was designed using the Clewin mask layout CAD tool. The device layout pattern on the specimen die is used as the reference pattern to get position accuracy of up to $\pm 0.1 \mu\text{m}$. The vector patterning mode requires three vertices points to align the specimen with the etch mask layout of the Laser-Draw 2D software. The masked specimen is then exposed and developed in diluted KOH (potassium hydroxide) solution. A mixture of KOH solution with DI (de-ionized) water

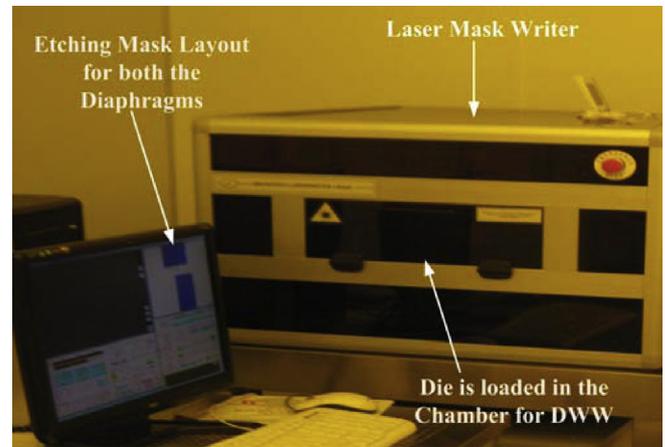


Fig. 1. DWW mask writing system and setup.

using a concentration ratio of 2:3 yielded good resist development with the specimen being kept in the solution for a duration of 6 min. This development duration was necessary due to the thickness of the resist. The top polyimide layer of the die served as a protective layer for the underlying CMOS devices and circuits against the strong KOH developer. Microscopic observation showed that the regions where the passivation etching is necessary developed quite well (being away from the edges), as evident from the resist developed top-view images in Fig. 2. The lithography for both the sensors appeared to be satisfactory. The specimen is then hard baked at 125 °C for 4 min to enhance the resist adhesion to the surface of the

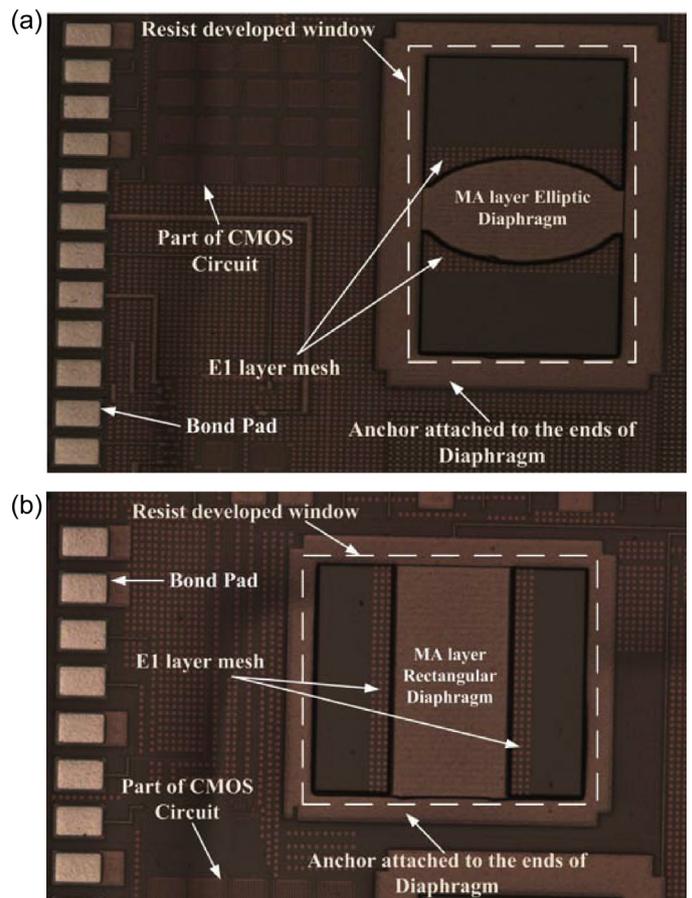


Fig. 2. Resist developed sensor capacitances: (a) elliptic diaphragm, (b) rectangular diaphragm.

chip. This avoids resist peel-off during passivation etch which can affect the top aluminum CMOS circuit interconnects as in another post-CMOS MEMS process reported in [4]. This proposed MEMS post-processing mostly uses plasma process (at low chamber temperature) for sensor structure release; hence risk of degradation in the circuit interconnects and vias are not present as reported in [4], where the die is exposed to high thermal budget release (at 535 °C).

3. Passivation etch process

The triple layered passivation sandwich in the 130 nm IBM CMOS 8RFDM technology has the following constituent layers; the top polyimide layer, the middle nitride layer and the bottom oxide layer. The dry plasma based RIE method which provides an almost anisotropic etch is employed for the passivation cut.

3.1. Polyimide etch

Oxygen (O₂) plasma is used to perform the polyimide cut. The complex VM (virtual metrology) optimization was avoided due to the time-constraint [9]. A simpler method of optimizing the process parameters is to first trial-run the cut on a dummy sample. To optimize the recipe, polyimide of thickness 2.5 μm is sputtering deposited on a sample wafer. The chamber pressure is maintained at 600 mTorr. A low RF coil power of 100 W along with a high ICP (inductively coupled plasma) power of 1000 W is applied while maintaining the chamber temperature at 0 °C. The sample is etched for 5 min using oxygen with 50 sccm (standard cubic centimeter per minute) flow rate. Step height analysis using an AFM (atomic force microscope) revealed that the polyimide is etched down to 0.7 μm. The process is repeated for 5 more minutes with an increased ICP power of 1200 W resulting in a cut depth of about 2.5 μm, thus concluding the successful trial etch. The etch is next performed on the actual specimen using this optimized trial recipe. To increase the etch rate and etch selectivity, C₄F₈ (octafluorocyclobutane) gas with 3 sccm flow rate is added. Step height analysis verified the depth of the actual polyimide etch. No significant residue was observed on the die that could effect the following plasma etch. Resist remains on the die became hardened and was removed by the stripping process detailed in Section 3.3.

3.2. Nitride and oxide etch

Nitride, in the passivation is 0.45 μm thick. RIE dry etch using SF₆ (sulfur hexafluoride) plasma with 45 sccm flow rate is utilized to achieve good vertical side walls that will make further processing feasible. Wet etch is not used at this stage in order to minimize side wall under cuts. In addition, in a further effort to avoid undercuts at this critical step, CHF₃ (fluoroform) gas at 30 sccm flow rate is added to the SF₆ plasma for better anisotropy. Increased anisotropy will avoid the lift-off of the diaphragm anchors during subsequent isotropic wet etch. Using 40 mTorr chamber pressure (at 0 °C), 20 W RF coil power and 250 W ICP power a good vertical nitride etch rate was achieved. After an initial etching for 40 s, step height analysis revealed 0.38 μm etch (cut) depth, hence an additional etch for 8 s was performed. The etch rate for the 48 s duration was thus 580 nm/min. The final dry passivation oxide layer etch was performed using CHF₃ plasma at 40 sccm flow-rate. Process parameters of 1500 W ICP power, 50 W RF coil power and 5 mTorr chamber pressure (at 0 °C), yielded the required etch depth of 1.35 μm. The specimen was etched for 6.3 min, for which the etch rate was 500 nm/min.

The CHF₃ plasma was observed to have a bright milky white color as shown in Fig. 3 inside the ICP-RIE (fluorine) chamber of the Oxford Instruments PLASMLAB100. The plasma RIE reactions are next presented in brief to consider any residues in the etching

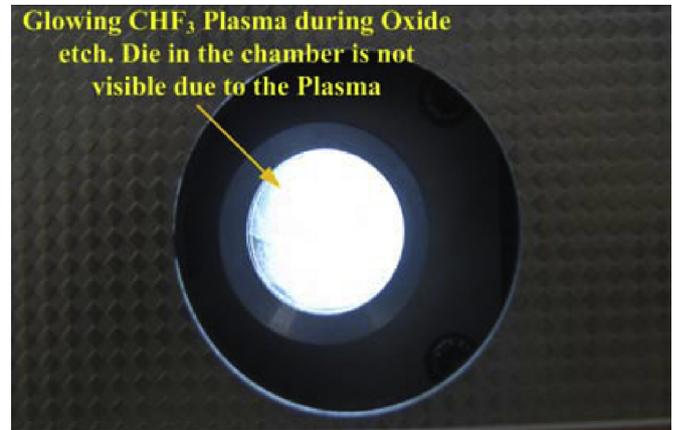


Fig. 3. Photo of the RIE chamber during CHF₃ plasma etch.

process that may deteriorate the post-processed MEMS sensor. The molecular dissociation and ionization of CHF₃ during this etching process can be given by [10],



Reaction of F_(a) atoms with oxide, can be given by,



In the above reactions, $y \leq 3$, $n \leq 2$, $q \leq 1$, F_(a) is atomic fluorine, and, K is an electron or a heavy particle. When the plasma density is very low with few molecular ions, some of the F⁻ ions recombine with CHF_q⁺ ions in the reverse reaction, and, further chemical reactions can be given by,



The reaction of the recombined CHF₃ on oxide is given by,



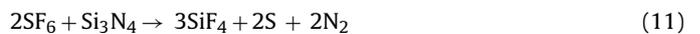
The dissociation and ionization of SF₆ can be given by,



Reaction of F_(a) with nitride, can be given by,



In the above reactions, $x \leq 6$, $m \leq 5$, and, $p \leq 4$. Some of the F⁻ and SF_p⁺ will recombine and react with nitride (similar to the CHF₃ plasma), and these reactions can be given by,



The CHF₃ plasma dissociations for nitride etch follows (1), (2), (4) and (5). Also, any recombined F⁻ and CHF_q⁺ in this case will react with nitride and will be given by,



As can be seen from the above ionizations and reactions of the plasma etch process, most of the products are gaseous and any residue will settle on the chamber wall, and hence, no post-cut cleaning is required to preserve the sensor integrity.

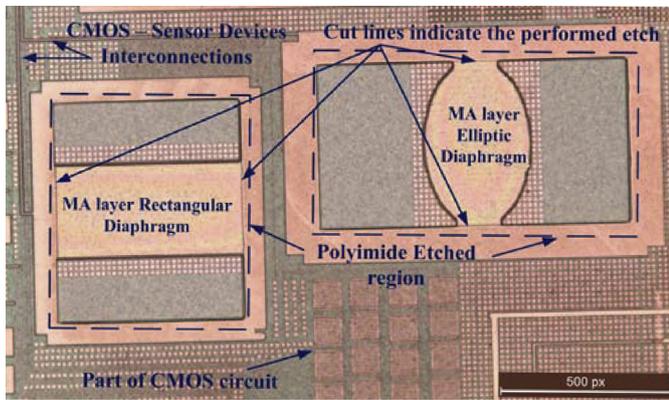


Fig. 4. Passivation etched and resist stripped diaphragms.

3.3. Photoresist stripping

The 7 μm thick photoresist, coated over the chip with direct mask writing survived the three steps of dry passivation etch. The resist remnants cannot be easily stripped-off using wet acetone cleaning alone, being hardened by exposure to ion bombardment. Even though, the top few micrometers of resist gets stripped off, prebake during the lithography process makes the underlying resist layers stick strongly to the surface of the chip. On the other hand, the exposed diaphragm metal could be damaged by the use of any strong solvents. Use of DHF (diluted HF acid), APM (RCA1 [11]: ammonia hydroxide–hydrogen peroxide–DI water mixture in the ratio 5:1:1) and HPM (RCA2 [11]: hydrochloric acid–hydrogen peroxide–DI water mixture in the ratio 6:1:1), can cause surface micro contamination. PIRANHA treatment (H_2SO_4 and H_2O_2 mixture in the ratio 7:1) was the other alternative, however, more than two minutes treatment can considerably reduce the thickness of the diaphragm metal, thus affecting the linearity and sensitivity of the sensor device. The EKC265 solvent, on the other hand, was also not considered suitable, as the copper metallization, interconnect and via in the CMOS circuit of the standard 130 nm IBM CMOS process may be degraded. Moreover, this solvent, although used for many industrial resist stripping purposes, requires long duration of plasma ashing for effective stripping. Considering all possible avenues, combination of repeated oxygen plasma ashing along with wet acetone sonicator cleaning was implemented to strip-off the photo-resist. Initially plasma ashing with low chamber pressure was carried out for 2 min; however resist remains were still found to be present. Thus 6 more minutes of ashing, followed by 10 min of acetone sonicator cleaning completely stripped off the resist. Fig. 4 shows the image of the passivation etched resist stripped diaphragms. This optimized cleaning procedure is quite compatible with wafer level manufacturing.

4. Release etch process

Thin photoresist ($\approx 1 \mu\text{m}$) of type AZ ECI 3012, which is suitable for both wet and dry etch is used for the second DWW lithography (Mask 2) for trench and lateral etches (release etch). The use of thin photoresist ensures that tedious resist removal procedures are not needed. The extension of mask 2 over passivation ensures its step coverage. It is suitably designed to achieve proper side wall resist film thickness through the spin coating and development process as shown in Fig. 6(f) and verified by AFM analysis. Owing to undercut issues in wet etch, DWW mask layout is designed such that mask window is well away from the side-wall anchor region. This prevents the chemicals from seeping toward areas under the anchor during limited time etch. A combination of dry plasma and wet etch

was adapted for the diaphragm release. The wet pre-lateral etch was carried out for a longer duration than usual to secure a lateral micro-vent (orifice) for subsequent 125 μm dry lateral release. This wet etch can possibly attack the underlying SiO_2 layers toward the anchors and hence requires a considered/cautious approach.

4.1. Trench formation

Dry RIE etch using CHF_3 plasma with 50 sccm flow-rate is used in this first phase of release etch. Oxide layers on either side of the diaphragms are etched vertically to a depth of 5 μm to form trenches. Dry etch with high ICP power and low RF bias power yields a higher vertical etch rate than lateral etch rate [12] thus forming rectangular box like trenches of dimensions 100 $\mu\text{m} \times 80 \mu\text{m}$. The applied high inductive power of 2000 W increases the ion bombardment and hence the etch rate, whereas the low RF bias power of 50 W avoids the formation of residual films on the die surface [12]. In order to perform a 5 μm vertical etch, the process pressure was kept at 5 mTorr (at 5 $^\circ\text{C}$). The specimen is etched for 9.5 min yielding a 530 nm/min dry etch rate. Some amount of over etch is performed further to confirm the depth of the trench cut. The created shallow trenches allows the subsequent wet etch to further deepen the trench vertically, thus avoiding random directional etch that can damage the diaphragms and the anchors. Diluted KOH (KOH with DI water) rinsing is carried out to remove any piles of oxide after the dry RIE [13]. The thin resist over the surface of the specimen gets stripped-off during this etch, hence a repeat lithography is necessary for further under-etch process.

4.2. Wet under etch

Buffered HF (BHF) solution which has a faster oxide etch rate and good selectivity between photo-resist and oxide is used as the under-etching (pre-lateral etch) solution. The mixture contains 100 g of NH_4F (ammonium fluoride) diluted in 150 ml of HF and DI water mixture (in 1:2 ratio). The expected etch rate is 300 nm/min. There was no intrinsic stopper structure available for the wet etch in the standard 130 nm CMOS process, and hence, timed etch-stop technique was utilized. BHF etch being isotropic causes few micrometers of lateral oxide etch below the diaphragm thus providing an easy start-up for subsequent lateral dry etch. The 4 μm thick diaphragm (the top MA aluminum) can withstand the aqueous HF chemistry of vertical oxide etch of up to 7 μm . To avoid damages at the sides of the diaphragm, wet etch time is thus limited to an etching depth of 7 μm ; hence the specimen is kept in the solution for approximately 20.4 min. Since the oxide etch rate of 300 nm/min using this BHF mixture can strip-off the resist in 10 min, the lithographic process is repeated after the first 10 min of the BHF etch. Even though this process involves two steps of lithography, it is less expensive compared to the vapor phase HF (VP HF) etch method. The yield, if mass production is conducted will be comparable to that using VP HF. Oxide reaction with HF is given by [14],



The H_2SiF_6 soluble residue is removed by DI water spray and air-gun drier. The aluminum diaphragm surface is protected by the stable photoresist during the wet etch. However, as a precaution, 5% nonionic surfactant (alkylphenol polyglycidol) is added so that any hydrogen bubble formation can be removed through DI water rinsing. The added surfactant reduces the particulate contamination and lowers the surface micro roughness. Thus no significant remains of hydrogen bubble and surfactant were noticed on the diaphragm surface after the BHF etch and cleaning. This preferred surfactant also has a faster desorption time from the aluminum surface. The surface roughness of the aluminum diaphragm, when

analyzed for a $1.0\ \mu\text{m} \times 1.0\ \mu\text{m}$ area using AFM was found to be as low as $1.54\ \text{\AA}$.

4.3. Dry lateral etch

Dry release etch is preferred to avoid stiction issues. CHF_3 plasma is employed to perform an under etch of $125\ \mu\text{m}$ on either side of the diaphragm through the trenches for a full device release. DWW mask features are designed to allow the ion bombardment on the sacrificial oxide through the trenches and lateral micro-vent, thereby enabling lateral etch under the diaphragms. Faster lateral etch can be achieved with high RF bias power and low ICP power [12]. Process parameters are optimized by first performing a trial run on a dummy wafer deposited with oxide by LPCVD (low pressure chemical vapor deposition) process. The run showed a $50\ \text{nm}/\text{min}$ lateral etch rate for a chamber pressure of $10\ \text{mTorr}$ (at 5°C). On the actual specimen, to perform a lateral etch of $125\ \mu\text{m}$, it was found that $40.8\ \text{h}$ of CHF_3 plasma etch is necessary. The chamber temperature was maintained at 5°C while RF bias power was increased to $400\ \text{W}$ with ICP power lowered to $20\ \text{W}$. This applied high RF bias power can increase the possibility of residual film formation on the die surface; hence, the chamber pressure was lowered to $7\ \text{mTorr}$ to minimize any residual film. The lithographic patterning was repeated every $2\ \text{h}$ to make sure the diaphragm is not exposed, however, some amount of etch at the sides of the diaphragm cannot be avoided. Using thick photoresist the number of lithography steps can be reduced. The nano-metric stepped (slotted) edge features of the elliptic diaphragm (due to pre-fabrication L-Edit MEMS layout constraint) were rounded off (smoothed out) during this long etch time as a beneficial complementary process outcome. Except for this edge smoothing, no other undesired etch is noticed that can substantially reduce the sensitivity of the sensor device. On the other hand, some etch at the sides of the rectangular diaphragm was noticed. The Si_3N_4 layer above the bottom electrode plate (LY metal layer) served as the etch stop layer, hence with the lateral etch of $125\ \mu\text{m}$, vertical etch was reduced considerably. This etch-stop layer eliminated the need to add a dummy layer of etch-stop metal deposition for protecting the LY (bottom capacitor plate) layer and hence avoiding a long process flow as in [15]. The CHF_3 plasma with $25\ \text{sccm}$ flow rate also provided good selectivity between SiO_2 and Si_3N_4 , and hence, the bottom electrode was well protected. The intermediate E1(Cu) mesh layer which was fabricated as $10\ \mu\text{m} \times 10\ \mu\text{m}$ squares spanning the diaphragm size was held intact by the interleaving oxide layer. With the oxide removal in the $125\ \mu\text{m}$ lateral etch the copper mesh test structure falls off thus confirming the full release of the diaphragm. Microscopic images of elliptic and rectangular diaphragms during and after release etch is shown in Fig. 5. The partially released elliptic diaphragm in Fig. 5(a) shows some remnants of the E1 copper mesh and residues. The surface texture of the fully released images indicate that the aluminum diaphragms were not affected by the exposure to various plasma during the etching process. Table 1 lists the complete dry etch process details.

4.4. Post-release etch

Post release etch process for removal of nitride isolation layer is necessary to avoid composite dielectric medium in the capacitive sensor devices. The purpose of the nitride layer above the LY metal in the 8RFDM CMOS BEOL stack is to provide better electrical isolation between the thick RF metals. However, as an inherent advantage, it defends the bottom electrode from surface fluorocarbon residue formation due to the carbon rich CHF_3 plasma. Furthermore, the isolation layer has protected the capacitive device against pull-in or break-down. The nitride etch recipe mentioned

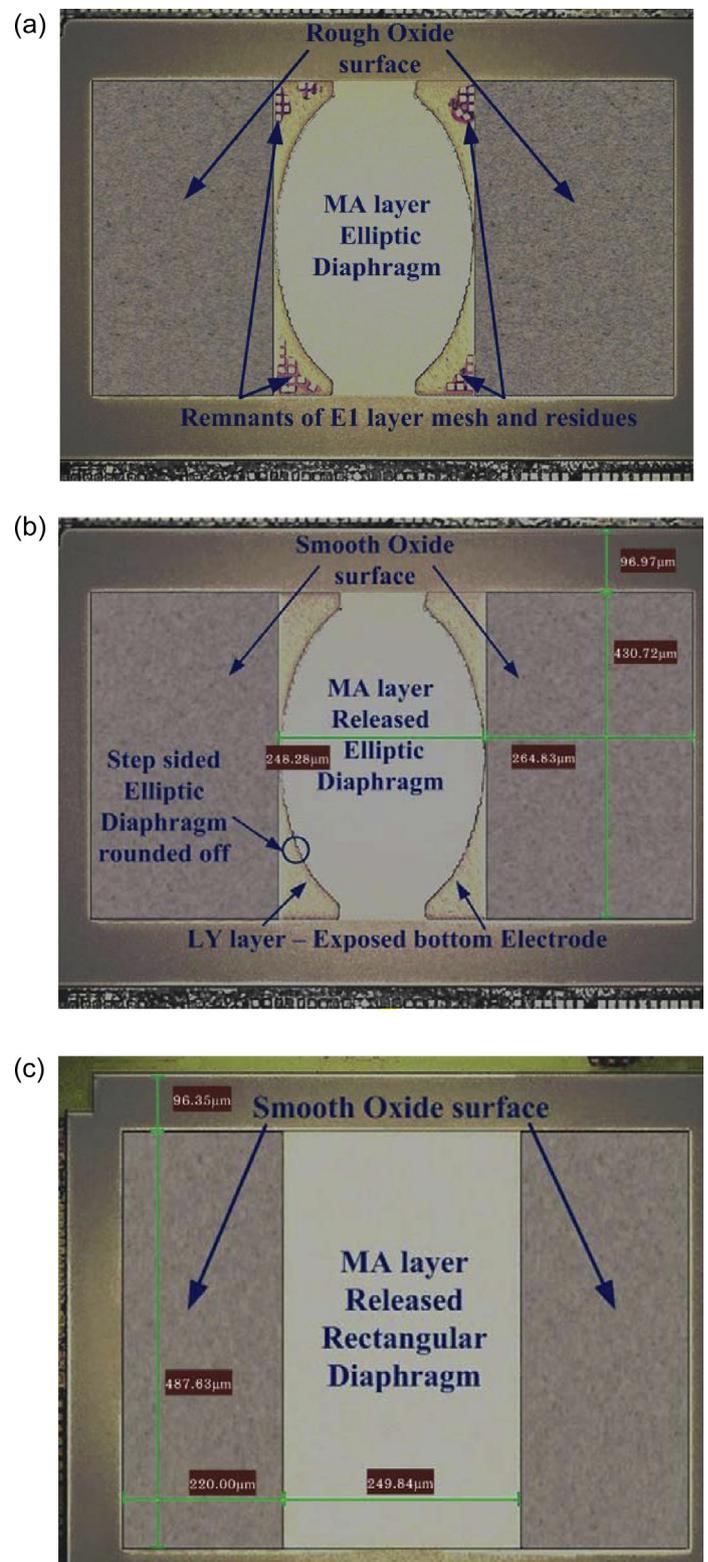


Fig. 5. Release etch: (a) partial release of elliptic diaphragm, (b) fully released elliptic diaphragm, and (c) fully released rectangular diaphragm.

in Section 3.2 is repeated in this etch but with low ICP power and high RF bias power.

Table 2 shows the feature comparison of various reported CMOS MEMS devices with this work. The comparative advantage of the proposed post-processing technique is quite evident from the table, with the achievement of a two-sided anchored $250\ \mu\text{m}$ laterally

Table 1
Process details for dry etch.

| Etching layer | Gas | Flow rate (sccm) | Process pressure (mTorr) | ICP power (W) | RF power (W) | Etching time and rate |
|-------------------|-------------------------------|------------------|--------------------------|---------------|--------------|-----------------------|
| Polyimide | Oxygen | 50 | 60 | 1200 | 100 | 10 min & 250 nm/min |
| | C ₄ F ₈ | 3 | | | | |
| Nitride | SF ₆ | 45 | 40 | 2500 | 20 | 0.8 min & 580 nm/min |
| | CHF ₃ | 30 | | | | |
| Passivation oxide | CHF ₃ | 40 | 5 | 1500 | 50 | 6.3 min & 500 nm/min |
| Trench oxide | CHF ₃ | 50 | 5 | 2000 | 50 | 9.5 min & 530 nm/min |
| Sacrificial oxide | CHF ₃ | 25 | 10 | 400 | 20 | 2448 min & 50 nm/min |

etched diaphragm. The cross-section of the stages in the MEMS release process as shown in Fig. 6 can be mapped into the sequence shown by the flow chart in Fig. 7 for the complete post processing. Since yield in general, have inverse exponential relationship with die area and process complexity, the use of only a small die area (<3 mm × 3 mm) and only 2 masks, ensures high post-processing yield. As damage and/or lift-off of the diaphragm or the bottom electrode during wet etch and/or dry etch could be a cause of failure, these critical aspects were addressed during the post-process as discussed above. Hence defect-free sensor release was ensured.

Due to the complexity of the co-integrated CMOS read-out circuit, some of the CMOS interconnections are routed through the LY and E1 layers for compactness. As the bottom electrode of the capacitive sensor is also on the LY layer, the CMOS circuit is located with some horizontal displacement beneath the diaphragm (as indicated in Figs. 2, 4 and 6) for accommodating the LY-to-LY horizontal spacing design rule for the 130 nm IBM CMOS process. Moreover, the risk of damaging the LY layer CMOS interconnects during post processing is minimized through appropriate horizontal spacing from the diaphragm above in excess of the design rule. In addition, the MA layer CMOS interconnects that route signals to the bonding pads (also using the MA metal) must also stay well away from the etching regions, in order to avoid any circuit degradation while performing the post-processing. Hence it was not desirable to layout the CMOS circuit just beneath the MEMS diaphragm.

4.5. Post release sealing

The released devices are next sealed as absolute pressure sensors. The trench areas are sealed by depositing and patterning fluorosilicate glass (FSG). First, 12 μm deposition of fluorosilicate [16] is carried out by PECVD (plasma enhanced chemical vapor deposition) in moderate vacuum (at 0.5 Torr) inside a reactor. The operating temperature of 225 °C (for sealing) during PECVD deposition process does not degrade the CMOS interconnects and vias.

CF₄ (tetrafluoromethane), oxygen and argon gases with optimized flow-rates of 30, 40 and 10 sccm, respectively, are fed into the top electrode of the reactor via a shower head. Addition of oxygen and argon enhances the deposition rate for this high aspect ratio sealing. Liquid TEOS (tetraethoxysilane) is introduced as a precursor into the plasma by bubbling helium through it into the reactor. TEOS being highly volatile at normal room temperature, vaporizes readily at the operating temperature so that the risk of stiction effect is negligible. The fluorine source, CF₄ may dissociate yielding higher fluorine ion concentration that would sputter the surface resulting in etching and slow deposition rate. Hence, hydrogen is also fed into the reactor as it would reduce the free fluorine and minimize the surface contamination of the silicate glass. During the 12 μm deposition process, the FSG will reach just above the bottom edges of the diaphragms inside the trenches yielding a vacuum sealed cavity under the diaphragms as shown in Fig. 6(i). Next the deposited FSG is patterned by a separate DWW masking and sputtering using Ar⁺ and O²⁻ ions. Thus the FSG sealing is achieved only in the trench areas just above the bottom of the diaphragm and removed from rest of the surface areas. Plasma cleaning is carried out at the completion of the deposition process. The fluorosilicate sealed rectangular device is shown in Fig. 8.

5. Characterization

5.1. Discussion on mechanical characterization

Prior to the start of each etch process, it is necessary to confirm the proper removal of layers by the preceding process. As per earlier discussion, this is achieved by finding the etch (cut) depth at the completion of each process through AFM step height analysis. For this purpose a surface topography, i.e. $Z=f(X, Y)$ study is carried out using the Bruker AFM Dimension Icon instrument. A fixed frequency of 2 kHz is used in the Peak Tapping Mode. Table 3 summarizes the step height measured at various process steps. The maximum scan size is set to 90 μm of which the midpoint is set at

Table 2
Feature comparison of Various reported CMOS–MEMS devices.

| Device reported | Number of metals | CMOS technology | Type of sacrificial release etch | Risk of stiction effect | Lateral release length | Device anchored | Post process thermal budget used |
|-----------------|------------------|---------------------|----------------------------------|-------------------------|------------------------|-----------------|----------------------------------|
| This work | 8 | 0.13 μm IBM CMOS | Wet and RIE plasma etch | No | 250 μm | Two sided | 125 °C |
| [1] | 4 | 0.35 & 0.18 μm TSMC | Wet etch | Yes | Up to 178 μm | One sided | <350 °C |
| [2] | 4 | 0.35 μm BiCMOS | Wet etch | Yes | 95 μm | One sided | 180 °C |
| [3] | 4 | – | RIE plasma etch | No | 80 μm | One sided | 120 °C |
| [4] | 5 | 0.25 μm SiGe BiCMOS | Wet etch | Yes | 30 μm | Two sided | 450 °C |
| [5] | 3 | 0.6 μm AMS | DRIE plasma etch | No | 250 μm | One sided | 225 °C |
| [6] | 1 Poly 6 Metal | 0.18 μm TSMC | Wet etch | Yes | 6.05 μm | One sided | 125 °C |
| [19] | 2 Poly 4 Metal | 0.35 μm TSMC | Wet etch | Yes | 158 μm | One sided | 125 °C |

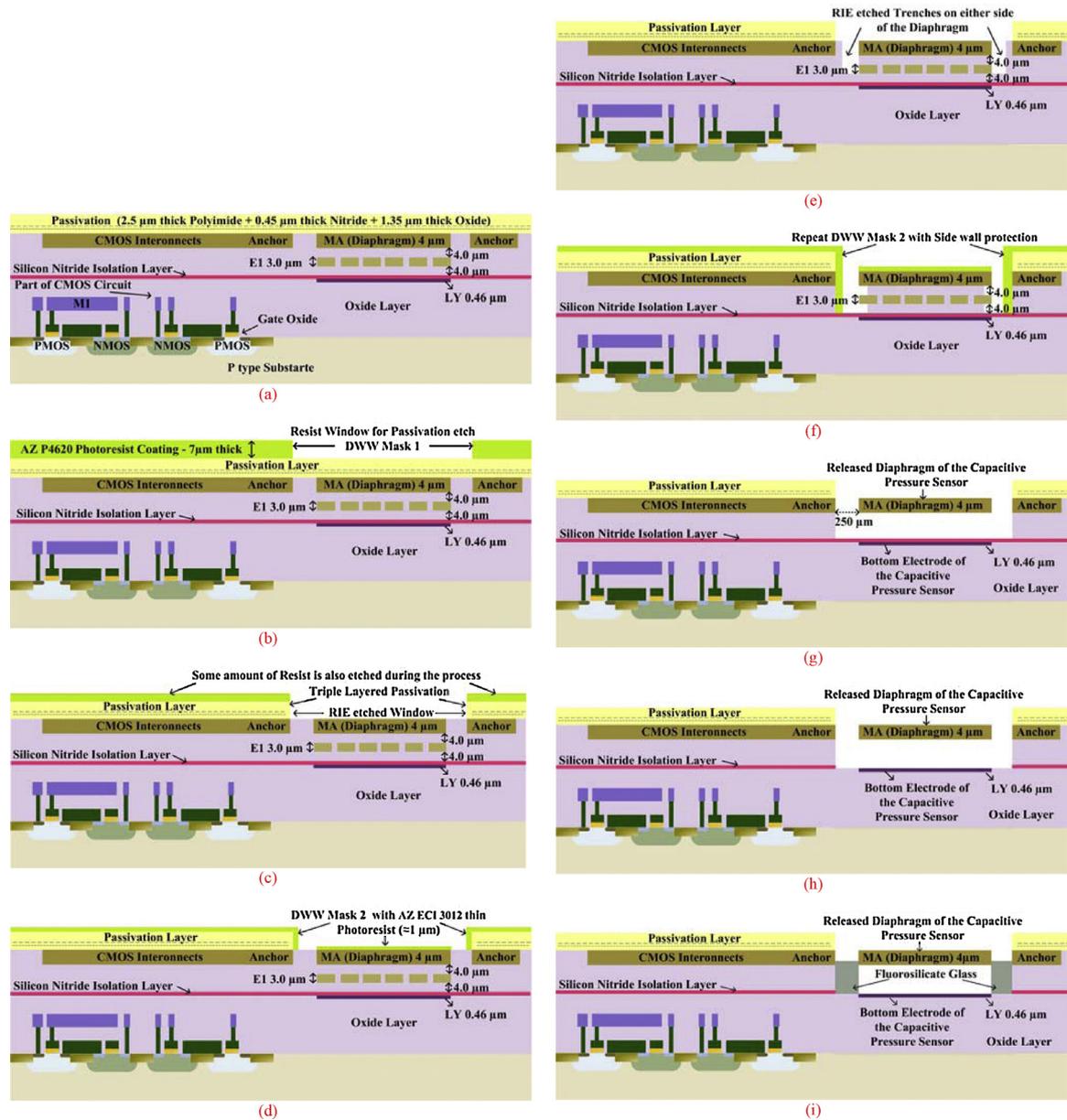


Fig. 6. Composite cross-section diagrams of the step-by-step MEMS release process: (a) initial CMOS chip with circuitry and unreleased MEMS capacitors, (b) lithography with thick resist (DWW patterning mask 1), (c) after passivation etch, (d) lithography with thin resist (DWW patterning mask 2), (e) after dry trench etch, (f) lithography with thin resist (DWW patterning mask 2 repeat with sidewall protection), (g) after wet etch and following dry etch (composite etch) whereby the copper mesh falls off, (h) after post release etch, and, (i) after post release fluorosilicate sealing. (note: x and y dimensions are not in exact scale due to column width constraint).

the junction of the etched window to get minimal artifacts in the images. The probe XY position is set to scan $45\ \mu\text{m}$ distance from the etched window junction toward the unetched region on the surface of the die and further $45\ \mu\text{m}$ from the etched window toward the etched region. Analysis is repeated several times to obtain accurate results. Fig. 9 shows the die image during ScanAsyst step height analysis.

5.2. Discussion on electrical characterization

The critical phase in passivation etch is to determine the successful complete exposure of MA metal of both the diaphragms (top electrode of the capacitive sensor). Even though variations in color and surface texture can to some extent reveal the cut opening, characterization is necessary. The full exposure of the diaphragm can

be verified through electrical conductivity analysis. The electrical characterization was carried out using the Agilent device analyzer B 1500A with 5 MHz pulsed source as shown in Fig. 10. Probing two opposite ends of the diaphragm, with a varying DC voltage, revealed whether the device top metal is exposed. Current and resistance measurements were carried out at several process steps. Contact analysis was conducted before the polyimide etch (corresponding to Fig. 6(b)) and also after the nitride etch. Even with 10 V DC there was negligible current flow in both cases, indicating that oxide layer is still present above the metal diaphragms. Fig. 11(a) and (b) provides the measurements of the resistance and the current, respectively, after the oxide etch (corresponding to Fig. 6(c)). It can be seen that even for a potential as low as 1 V across the diaphragm surface a current of 0.1 A flows, indicating the complete exposure of the MA layer of the diaphragm. The noise

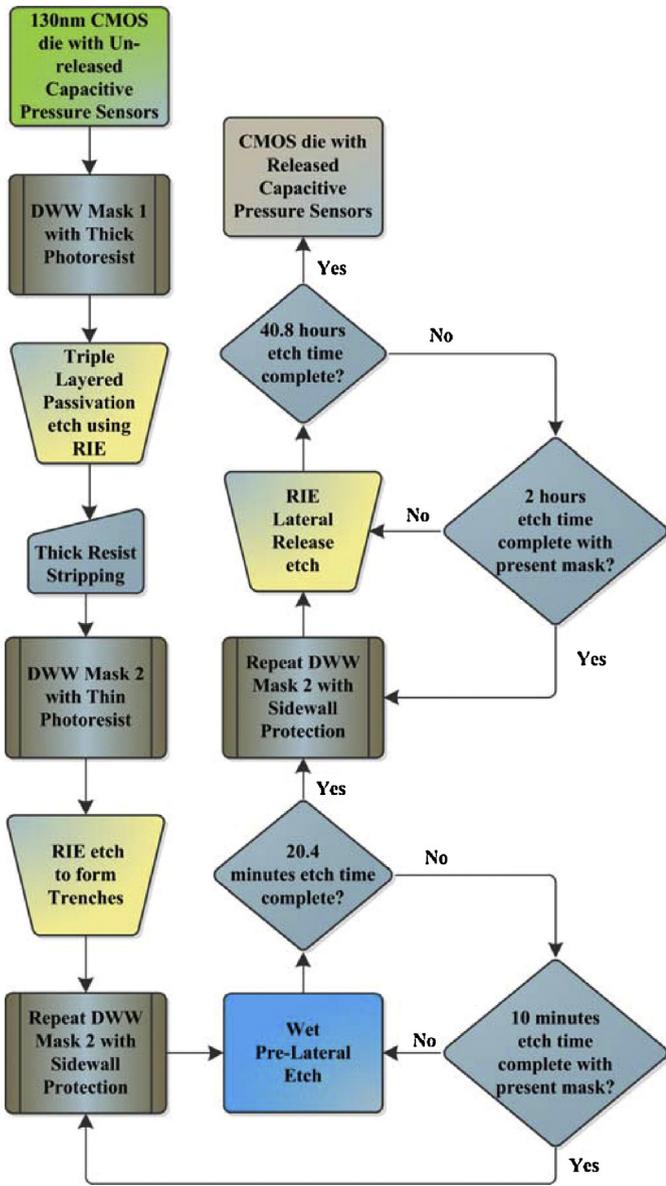


Fig. 7. Flow chart of the sensor release process sequence with an average number of photolithographic steps being 22.

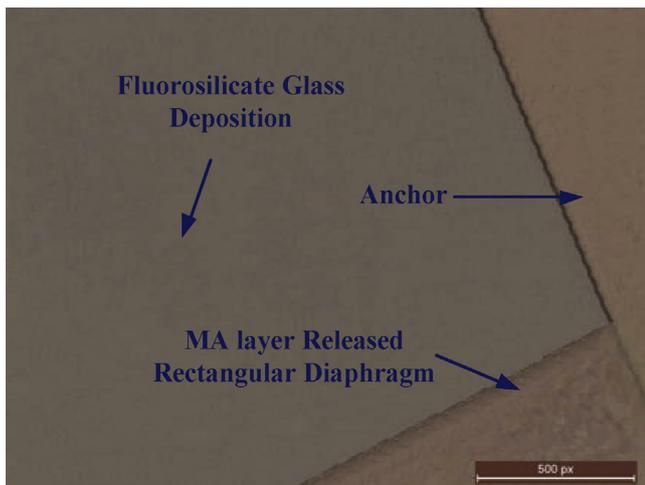


Fig. 8. Microscopic image of fluorosilicate glass sealed rectangular device.

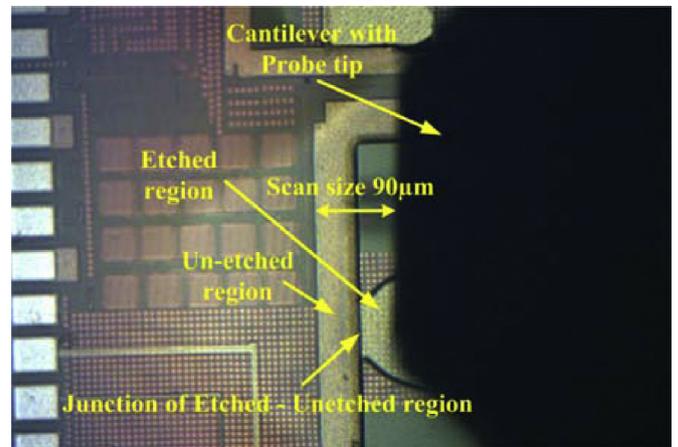


Fig. 9. Atomic force microscope—step height analysis, chip image from the AFM microscope after partial polyimide etch.

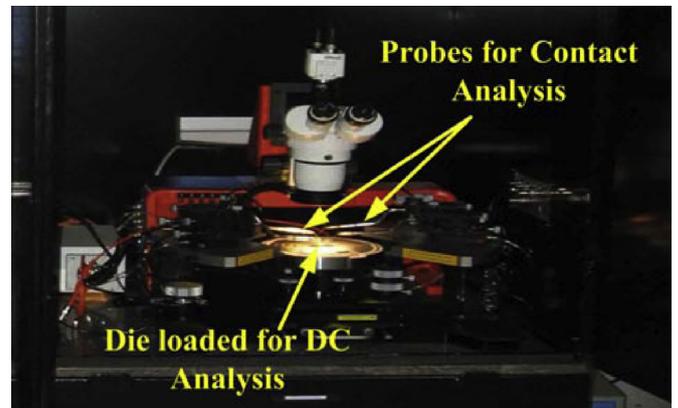


Fig. 10. DC probe station: Agilent device analyzer B1500A with 5 MHz pulsed source.

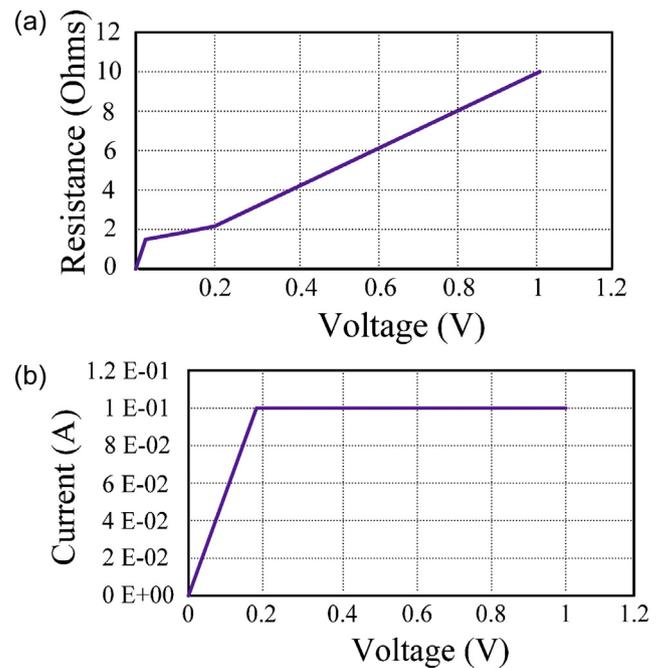


Fig. 11. Electrical contact analysis of exposed diaphragm after etching the oxide layer of passivation: (a) resistance variation, (b) current variation.

Table 3
AFM analysis results.

| S. No. | Specimen Analysis State | Step height |
|--------|--|---|
| 1 | First resist coated (corresponding to Fig. 6(b)) | 7 μm |
| 2 | Polyimide etched | 8.3 μm (resist is attacked) |
| 3 | Nitride etched | 7.8 μm (resist is further stripped) |
| 4 | Passivation Oxide etched (corresponding to Fig. 6(c)) | 6.3 μm (resist continued to strip off) |
| 5 | Resist stripped | 4.3 μm |
| 6 | Trenched & resist removed (corresponding to Fig. 6(e)) | 8.3 μm |

flow (leakage current) for the experimental setup measured using a 1 V step input with the probes held in air, was around 100 fA. The resistance is calculated using the applied voltage and the measured current. The calculated resistance was thus found to be very low in the order of a few ohms after the oxide etch (as shown in Fig. 11(a)). The small ramp (linear rise) in the measured resistance with voltage is mostly caused by the heating of the diaphragm due to the high current flowing through it. The diaphragm release was confirmed by the collapse of the interleaving copper mesh, however, further verification was also carried out by a two-point cross-probing of the diaphragm and LY layer contacts. Negligible measured current along with high resistance indicates full release of the diaphragm (corresponding to Fig. 6(h)). The presence of any intervening oxide layer would have resulted in a current in the order of μA at a high applied voltage of 12 V. Also, the measured resistance in the order of $\text{G}\Omega$ confirmed that no stiction occurred between the MA and LY layers. The measured pull-in voltages were 38.8 V and 39.2 V for the elliptic and rectangular devices, respectively. Also the resistance (between the MA and LY plates) at pull-in (just before *touch-down*) were 13.57 $\text{M}\Omega$ and 16.74 $\text{M}\Omega$, respectively, for the elliptic and rectangular diaphragms (including the diaphragm anchors).

6. Sensor measurements and experimental results

The hermetically sealed capacitive pressure sensors does not require tedious vacuum electrical lead transfer techniques as this is taken care of during the BEOL interconnect metallization process. The sensor interconnections with the on-chip CMOS readout circuit are routed through the bottom BEOL metal stack (M1/M2/M3), and hence these metallization are not in proximity to the region of release etch and vacuum sealing. The experimental test system has an inherent advantage of low noise setup, as no interconnections with external readout circuitry that can pick up noise and render stray capacitances is required. An on-chip high gain g_m -boosted OTA (operational trans-conductance amplifier) provides sufficient amplification for this low frequency sensor output. Fig. 12 shows the schematic diagram of the two stage chopper-stabilized CMOS sensor signal conditioning readout circuit. It uses a cascade of an RFC (recycled folded cascode) input OTA along with a common-source output stage yielding an overall gain of around 105 dB. In Fig. 12 the factors H and F constitute current mirror ratios for g_m -boosting. Using switching pins the readout circuit can connect to each sensor individually or to a parallel connection of both the diaphragms. Pressure chamber, mass flow controller, nitrogen gas pump, LCR meter, power supply and DMM (digital multi meter) are some of the equipments used in the test

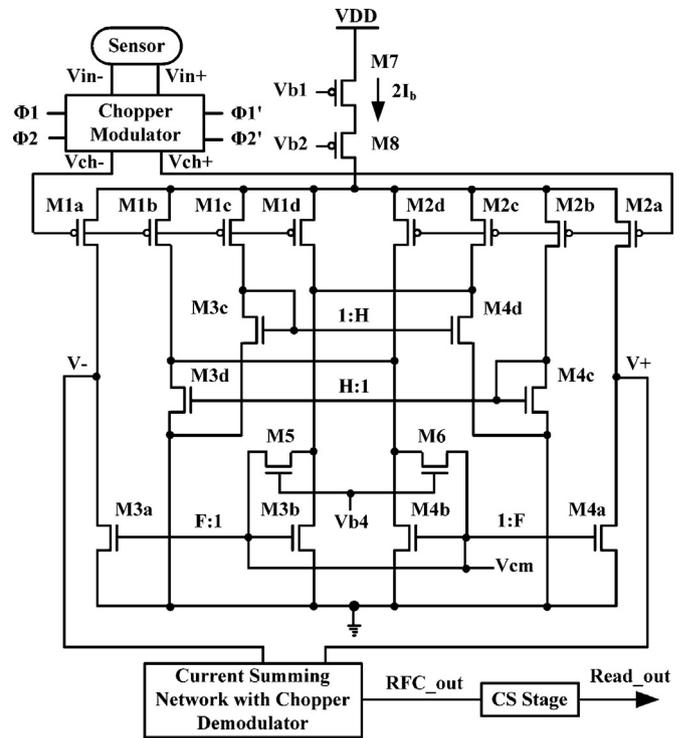


Fig. 12. Schematic diagram of the two stage high gain chopper-stabilized CMOS sensor signal conditioning readout circuit.

setup as shown in Fig. 13. The integrated sensors are bonded on to the general purpose FR-4 PCB board using a wire-bonder as shown in Fig. 14. The measured physical dimensions of the elliptic and rectangular sensing diaphragms were $431 \mu\text{m} \times 248 \mu\text{m}$ and $488 \mu\text{m} \times 250 \mu\text{m}$, respectively. The diaphragm's anchor width being around $95 \mu\text{m}$ contributes some parasitic capacitance, which can be cancelled using reference capacitance techniques [17]. In addition to integrated read-out circuit pins, the capacitive sensors can also be accessed directly via bottom and top plate interconnect pins (for external signal conditioning option). The stable capacitances measured using an Agilent 4284A precision LCR meter (with 0.05% basic impedance accuracy) at zero applied pressure were 1.16 pF and 1.23 pF for the elliptic and the rectangular sensing elements, respectively. In addition, the capacitive transduction dynamic range was found to be 0.32 pF and 0.23 pF, respectively,

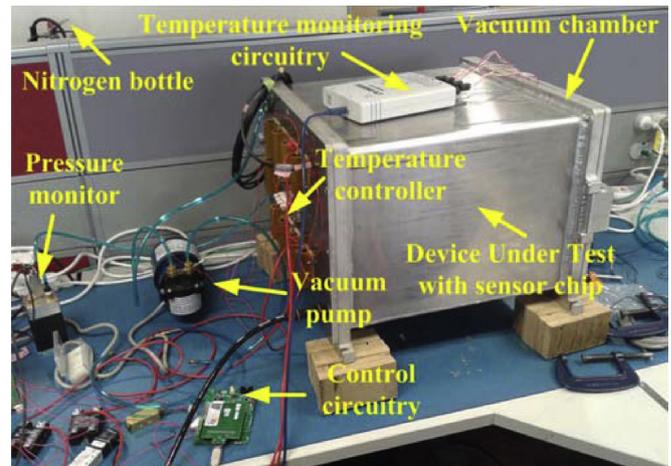


Fig. 13. Experimental test setup for sensor transduction performance measurement.



Fig. 14. Photo of the post-processed CMOS naked die containing the integrated MEMS capacitive pressure sensor being wire-bonded on to PCB.

for the elliptic and rectangular element (for 80 hPa pressure variation) as shown in Fig. 15. Over the measured pressure range, the elliptic element provided better sensitivity of 4 fF/hPa compared to the rectangular element for which the sensitivity was 2.9 fF/hPa. The elliptic diaphragm exhibited slightly higher linearity compared to the rectangular diaphragm within its dynamic range. Device sensitivity was observed to be marginally higher in the higher range of applied pressure (40–80 hPa). The test system used a low 1.2 V supply, so that the power dissipation with both capacitive devices employed along with the CMOS sensing circuit was found to be as low as 425 μ W. The maximum sensitivity at the output pins of the readout circuit for a pressure range of up to 100 hPa is found to be 0.07 mV/Pa for the elliptic element and 0.05 mV/Pa for the rectangular device as shown in Fig. 16. In comparison, the sensitivity achieved by a pressure sensor reported in [18] was an order of magnitude lower at only 0.00787 mV/Pa. Thermal coefficient of the capacitive sensor is critical for the linearity aspect of the device. Although capacitive sensors are mostly independent of temperature variations compared to piezo-resistive sensors, marginal decreases (*nonlinear behavior*) in the capacitance (at the higher pressure range) were observed when the chamber temperature is increased above room temperature (27 °C). The sensor capacitances were measured for three different temperatures (15 °C, room temperature and 55 °C) as shown in Fig. 17(a) and (b). The average capacitance drift was

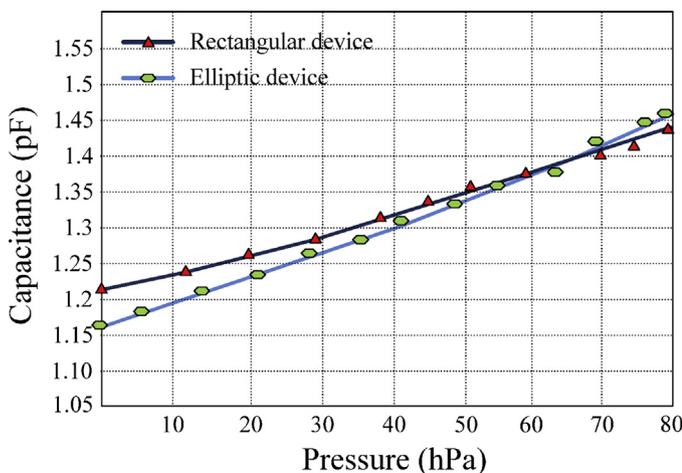


Fig. 15. Performance of the elliptic and rectangular devices.

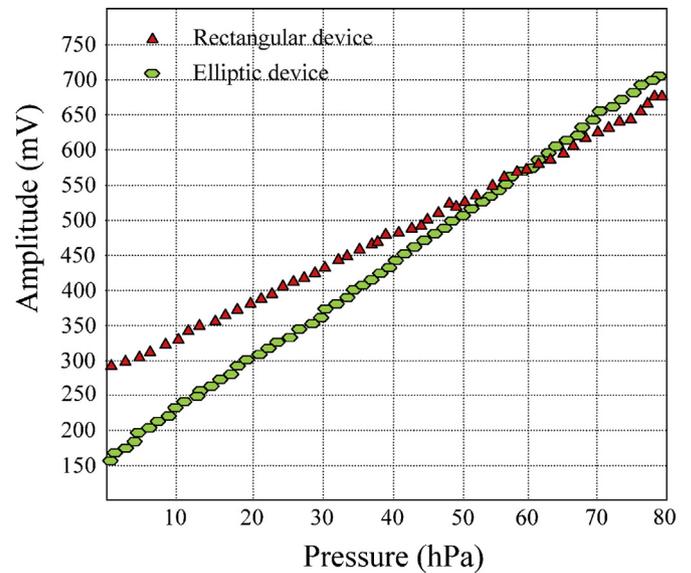


Fig. 16. Sensing circuit response with applied pressure.

around 10 fF over a range of 20 °C temperature variation. In general, decrease in the capacitance in the order of femto-farads was observed in the higher pressure range from 60 hPa to 100 hPa for the elliptic device and 75 hPa to 100 hPa for the rectangular device. This is possibly due to the non-uniform diaphragm stress distribution over higher pressure ranges (at higher temperatures).

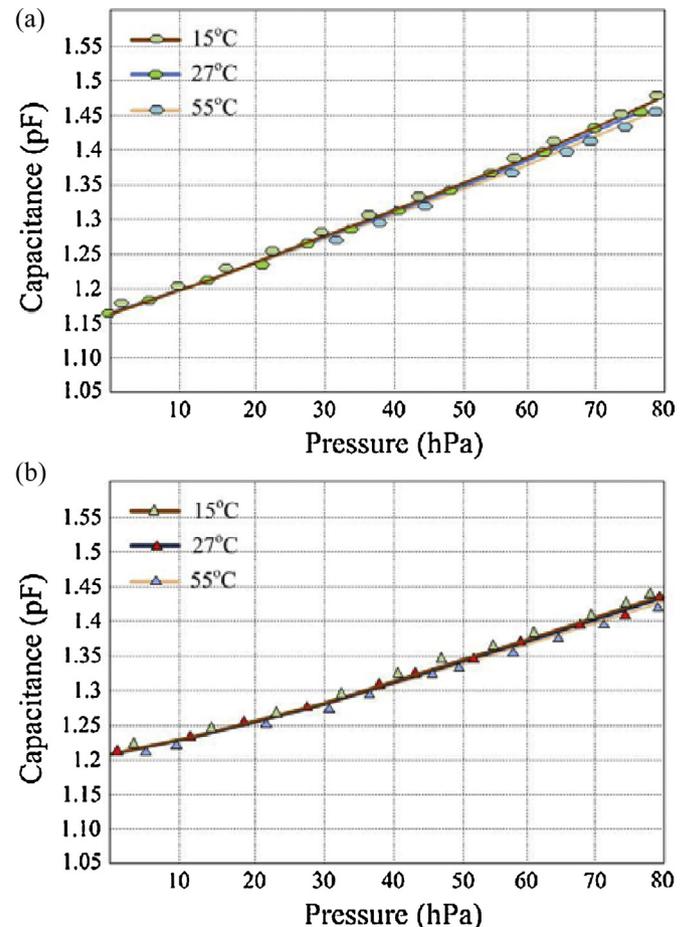


Fig. 17. Temperature dependency of (a) elliptic element, and (b) rectangular element.

The vent valve was released (*relieved*) frequently during the test for linear increase of pressure inside the chamber. The observed hysteresis and repeatability (*test-retest reliability*) for the elliptic element were 0.045% and 0.02% point of reading, respectively. On the other hand, the hysteresis was lower in the rectangular element with 0.024% but a moderate repeatability of 0.05% was noted in this case. Referred to the 80 hPa input range; the hysteresis was 3.6 hPa and 1.9 hPa, while, the repeatability was 1.6 hPa and 4 hPa, respectively, for the elliptic and the rectangular sensors. The residual tensile stress in the diaphragm was low at approximately 11 MPa, which is lower than that in anchored polysilicon structures fabricated in multi-user MEMS (MUMPS) processes. Linear buckling analysis carried out prior to plasma etching indicated that the aluminum membrane can withstand a comparatively higher stress of around 500 MPa compared to a similar geometry polysilicon membrane which could break at around 300 MPa.

7. Conclusion

Successful MEMS capacitive sensor release etch employing a mixture of wet and plasma dry etch on a 8-metal BEOL 130 nm standard IBM CMOS process has been demonstrated. Lateral etch (under etch) of 125 μm from opposite sides between the diaphragm (*top MA electrode*) and the bottom plate (*LY electrode*) was achieved without damaging the anchors and the underlying CMOS signal conditioning circuitry. The highly compact 8 metal layer CMOS MEMS allows smaller line-width and hence offers lower parasitic effects compared to those reported in [19–23] for micro-systems design. An optimized technique of resist stripping without damaging the exposed aluminum diaphragms was also verified. The comparatively low cost CHF_3 plasma etch yielded a smooth surface with no residues, hence avoiding the need for strong wet cleaning chemicals that attacks aluminum diaphragms and are associated with stiction effects. The fabricated intermediate copper mesh test structure (*E1 layer* of the BEOL stack) falls off during the release etch, thus confirming the full release of the diaphragm through microscopic observation. As the diaphragm is partially transparent while viewing through the microscope, the absence of copper mesh layer is easily ascertained. The necessity for expensive scanning electron microscope analysis is thus avoided. Thermal budget for the 0.13 μm CMOS circuitry is taken into consideration and any process that required more than 225 $^\circ\text{C}$ temperature is eliminated from the post-process flow for protecting the on chip CMOS circuits. The released sensor capacitors were mechanically and electrically characterized using step height and electric contact analysis, respectively. Experimental measurements of the transduction behavior as an absolute capacitive pressure sensor was also carried out in terms of sensitivity, dynamic range, hysteresis and repeatability. The test results indicate that the elliptic structured device has better overall performance in terms of sensitivity and dynamic range compared to the rectangular device.

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Elliptic Diaphragm Capacitive Pressure Sensor and Signal Conditioning Circuit Fabricated in SiGe CMOS Integrated MEMS

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Abstract—This paper presents a novel CMOS integrated capacitive pressure sensor, fabricated in silicon–germanium microelectromechanical systems (SiGeMEMS) process, with the sensor held and linked to the CMOS beneath. The CMOS process houses the on-chip signal conditioning circuit. The superior stress–strain behavior of polycrystalline silicon–germanium (poly-SiGe) is effectively utilized to develop and characterize the structure of the pressure sensor diaphragm element. The edge-clamped elliptic structured diaphragm employs semimajor axis L-shaped clamp springs to yield high sensitivity, wide dynamic range, and good linearity. To maximize the center deflection of the diaphragm, a stem structure is designed to transfer the entire stress on to the diaphragm center. The signal conditioning circuit is fabricated in a 0.18 μm TSMC CMOS process (forming the host substrate for the SiGe-MEMS sensor) and achieves a high overall gain of 100 dB for the sensor readout. Experimental results indicate a high sensitivity of ~ 0.12 mV/hPa (at 1.4 V supply), along with a nonlinearity of $\sim 1\%$ for the full-scale range of applied pressure load. The diaphragm with a wide dynamic range of 100–1000 hPa is stacked on top of the CMOS circuitry. The piggyback structure reduces the combined sensor and conditioning circuit implementation area of the intelligent sensor chip to $\sim 750 \mu\text{m} \times 750 \mu\text{m}$. The major and minor axis dimensions of the sensor were 485 μm and 280 μm , respectively. The device achieved wider low-pressure sensing range at lower supply voltage compared with commercial pressure sensors.

Index Terms—Poly-SiGe, MEMS sensor, microstructures, stress, strain, CMOS, perforation, chopper stabilization.

I. INTRODUCTION

MICRO-STRUCTURED sensors and actuators integrated with on-chip signal conditioning circuit has been of considerable research interest to the sensor design community for some time now. Improvement in the performance of the transducer system has greatly influenced the growth in the development of on-chip prototype sensors and actuators. However, their manufacturing and utilization is still in the early stage with prospects for rapid growth. Miniaturized pressure sensors have been in great demand in numerous

fields such as Bio-medicine, Automotives, Industrial control, Avionics etc. for many years now. Transduction using capacitance or piezoresistance are the two well known techniques of pressure sensor design and implementation [1]. The requirement of fewer fabrication mask steps along with insensitivity to thermal perturbations, as well as, environmental effects have made the capacitive sensing technique preferable compared to the piezoresistive implementation. However, parasitic effects (*due to curling boundary fields*) result in significant performance degradation of the capacitive sensing technique, and hence it requires on-chip readout and conditioning circuitry for performance enhancement [2]. Efforts in the hybrid integration of sensor devices and associated signal conditioning electronics in a single hermetic package has mostly resulted in unsatisfactory performance of the composite sensing system due to the significant issues of nonlinearity, reliability and environmental degradation. Even though the monolithic integration of sensor and signal conditioning usually has a longer time to market compared to hybrid sensor systems; it offers lower overall production and packaging cost [3]. The unique novel co-fabrication of SiGe-MEMS sensor device on top of a CMOS circuit (also forming the host substrate for the SiGe-MEMS structure in a “piggyback” formation) is discussed in this paper. This CMOS SiGe-MEMS technique has drastically shrunk the spatial dimensions of the pressure sensor system. The proposed device provides wider low pressure sensing range at lower supply voltage compared to commercially available pressure sensors such as KP236N6165 and PS-AN13.

Thermal variation of the material properties of polycrystalline SiGe is quite low, thus enabling the post processing of sensor devices directly above the bulk CMOS circuitry located in the native silicon substrate. Capacitive sensor diaphragms of various shapes and structures along with different dimensions and thickness have been explored in the past for enhancing the overall system performance parameters such as sensitivity, linearity and dynamic range [1]–[4]. Although reducing the thickness of the diaphragm (which forms the top plate of the capacitive sensor) has yielded improved sensitivity, the trade-off has been poor linearity [2]. This proposed design and fabrication has focused to overcome this sensitivity vs. linearity trade-off. The functional block diagram of the proposed CMOS integrated SiGe MEMS sensor is shown in Fig. 1. The weak noisy sensor signal in the form of an input current is initially converted into a voltage

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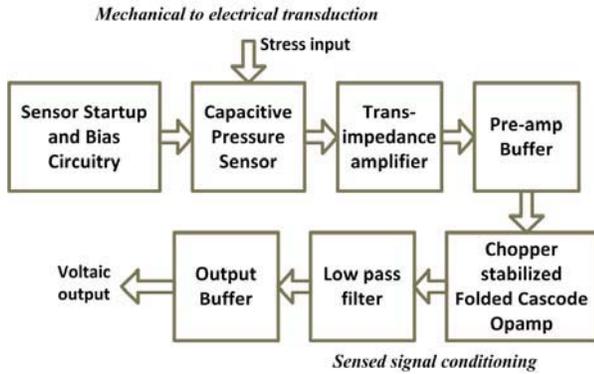


Fig. 1. Block diagram for the novel design and fabrication of capacitive pressure sensor and co-integrated signal conditioning circuit in CMOS integrated SiGe-MEMS.

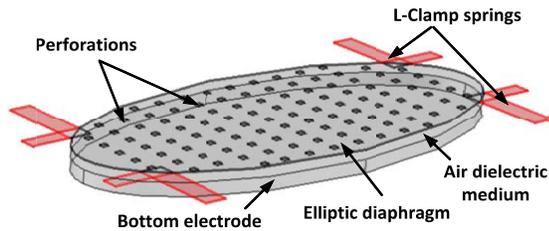


Fig. 2. Elliptic diaphragm with geometrically regular perforations, clamped at the semi-major axis using clamp springs.

signal using a trans-impedance amplifier. The trans-impedance amplifier requires very low input referred noise performance. After some pre-amplification, this voltage signal is then amplified using a low-noise high gain chopper-stabilized folded-cascade operational amplifier (opamp). The high frequency chopper residuals (artifacts) are filtered out by a higher-order steep roll-off Gm-C low-pass filter. The filter is followed by an output buffer which should be capable of driving a large off-chip load of up to 15 pF. The sensor diaphragm is also perforated to reduce electrostatic pull-in. The overall design target for the SiGe-MEMS fabricated edge clamped perforated elliptic diaphragm structure is to achieve wide dynamic range, without compromising sensitivity and linearity. In addition, deflection to measure very low pressure loads is also desired. In order to achieve this performance, edge-clamping is employed at the semi-major axis using clamp type springs as shown in Fig. 2. This paper is organized as follows: In section II, SiGe sensor element design and implementation is discussed, in section III, sensor signal transduction and design of the on-chip CMOS signal conditioning circuit is explained, while in section IV, the sensor and circuit simulation technique is discussed. The experimental results from sensor fabrication and measurement are provided in detail in section V, and, finally, concluding remarks are presented in section VI.

II. SiGe SENSOR ELEMENT DESIGN AND IMPLEMENTATION

The capacitive sensing technique which is an inherently low noise transduction mechanism is also a relatively simple method that usually utilizes a varying mechanical displacement (parallel plate separation) to sense the desired physical

quantity and extract a transduced voltaic signal. Although this technique is considered less resilient to harsh environment compared to a piezoresistive sensing; proper structural design can, in comparison, contribute to a relatively lower hysteresis and greater stability as distinct advantages for the capacitive sensing technique.

A. Diaphragm Fundamentals

The elliptic structured diaphragm which forms the top plate of the capacitive pressure sensor is implemented with numerous planar perforations in a regular geometric order. This technique enhances the sensor linearity which is a design target. In addition, clamping only near the semi-major axis edges of the fabricated structure using clamp springs enables better low pressure sensitivity compared to an all edge clamped sensor element. With vertical pressure (stress) on the diaphragm the displacement between the diaphragm and the bottom electrode (plate) fluctuates yielding a capacitance variation. Ignoring the fringe electrostatic field flux lines, the capacitance variation is governed by [4],

$$C = \frac{\epsilon_r \epsilon_o A}{d} \quad (1)$$

Where, ϵ_r is the relative permittivity of the dielectric material, ϵ_o is the permittivity of free space, A is the cross-sectional area of the diaphragm and d is the distance between the electrodes (plates) of the capacitive sensor. The diaphragm deforms under the influence of applied pressure, as a result of the distributed stress and strain. However, due to the edge clamping using the clamp springs the diaphragm deflects in a non-uniform manner. Consequently, the change in the distance between the diaphragm and the bottom electrode is not uniform along the sensor cross-sections, and hence (1) must be obtained by surface integration over the 2D (spatial) distance between the electrodes, which can be expressed as [4],

$$C = \iint [\epsilon_r \epsilon_o / \{d_o - D(x, y)\}] dx dy \quad (2)$$

Where, d_o is the distance between the plates at zero pressure and $D(x, y)$ is the incremental change in the separation after diaphragm deflection at a spatial location (x, y) . The effective top-plate deflection (w) for an elliptic diaphragm can be expressed as,

$$w = [1/(\pi \cdot r_1 \cdot r_2)] \iint D(x, y) dx dy \quad (3)$$

Where, r_1 and r_2 are respectively the radii of the semi-minor and semi-major axis, while the effective deflection, w in the z direction is determined by averaging the spatially integrated deflection over the entire surface area of the elliptic diaphragm. The diaphragm thickness is very small compared to its other dimensions, and, hence assumption of Kirchoff's hypothesis [5] is considered in the stress analysis of its deflection. Furthermore, the diaphragm displacement will usually be around half its thickness, so that, 2D plane stress analysis of thin plates is well-suited in this design. The stress tensor components σ_z , σ_{xz} and σ_{yz} becomes null in

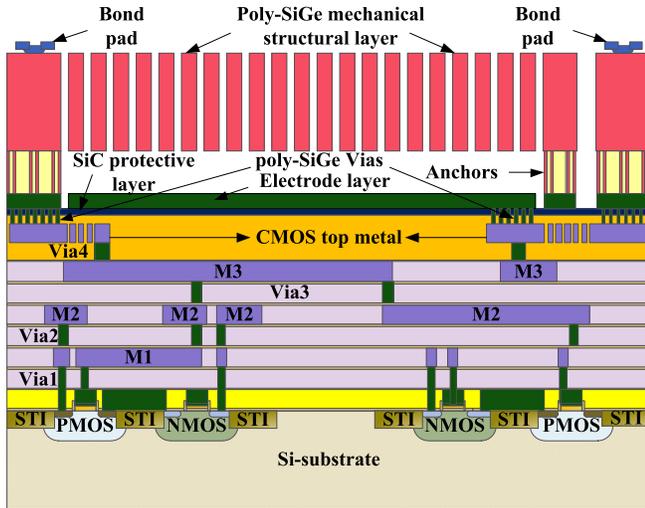


Fig. 3. Cross-section of the target CMOS integrated SiGe-MEMS process for integrated MEMS pressure sensor.

such an analysis and the stress tensor matrix reduces [5] to:

$$\sigma = \begin{bmatrix} \sigma_x \\ \sigma_y \\ \sigma_{xy} \end{bmatrix} \quad (4)$$

Assuming the diaphragm material is isotropic, its stress-strain behavior can be considered to be linear within the range of its elastic limit. This stress-strain linearity assumption up to the elastic limit is based on the well-known Hooke's law and can be given by [5],

$$\sigma = E\varepsilon \quad (5)$$

Where, σ is the stress due to the applied pressure, ε is the resulting strain, and E is the Modulus of Elasticity. An elliptic structure can be considered to be a special case of a circular structure pulled along the opposite sides in order to be stretched, and hence, the radius along that direction increases (becomes the semi-major axis), while the area of the structure remains unchanged. The deflection, stress and strain analysis of the elliptical structure is thus assumed to be similar to that of an edge clamped circular structure.

B. SiGe Fabrication Process and Diaphragm Structure

Fig. 3 shows a cross-section of the CMOS integrated SiGe-MEMS process technology for implementing the pressure sensor (available through *Europractice*). This SiGe process has a $0.6 \mu\text{m}$ minimum feature size. An elliptical structured diaphragm using the top poly-SiGe material is clamped at the semi-major axis for the curvilinear deformation of the entire diaphragm at low pressure loads. In comparison, the deflection of an all-edge clamped diaphragm at very low applied pressure is almost negligible yielding poor sensitivity and low dynamic range [3]. The proposed diaphragm structure is fabricated by stacking ("piggybacking") on top of the CMOS signal conditioning circuit. The low thermal fluctuation of the poly-SiGe material properties for the MEMS structure ensures minimal thermal drift in the

MOS device performance of the underlying conditioning circuit. The interconnection between the MEMS diaphragm and the CMOS circuit is through low resistivity poly-SiGe vias. The top aluminum metal layer of the back-end-of-line (BEOL) CMOS process is used to connect the electrodes of the capacitive MEMS sensor to bonding pads for test and measurements. The electrical isolation between the MEMS structure and the CMOS circuitry is achieved through a 400 nm thick silicon carbide (SiC) passivation layer. Poly-SiGe anchors firmly fixes the clamp spring at the edges of the elliptical diaphragm along the semi-major axis. The Poly-SiGe L-clamp springs have much lower thermal conductivity of 11 W/m-K compared to aluminum and polysilicon [25] (the commonly used material for diaphragms). Further, it has a very low thermal expansion coefficient of $5 \times 10^{-6} \text{ m/m-K}$ [25]. These thermal specifications ensure very low thermal expansion of the clamp springs compared to aluminum and polysilicon. Hence, mismatch in the thermal expansion of the four springs will be minimal. In addition, this extremely low imbalance is counter-balanced by anchoring the tips of the semi-major axis of the elliptical plate in opposite sides. The clamp springs (along with the planar perforations) overrides the necessity for reducing the thickness of the structure, thus overcoming the sensitivity vs. linearity trade-off. Various anchor arrays are explored for obtaining specific bending moments at the edges of the diaphragm that can tolerate a specified pressure range. Since the anchors are semi-conductive, the bottom electrode has to be designed carefully in order to avoid possible leakage and/or short circuit. The sacrificial oxide layer under the diaphragm (to be replaced by air-gap dielectric) is etched out through the front-side diaphragm perforations, using these cavities as structure release holes/vias as well. The release holes/perforations are $10 \mu\text{m} \times 10 \mu\text{m}$ in dimension and are spaced at $10 \mu\text{m}$ pitch throughout the diaphragm structure. As a consequence, the diaphragm exhibits relatively less deflection in the high pressure range. COMSOL analysis indicate a diaphragm displacement of $2 \mu\text{m}$ for an applied pressure of 1000 hPa , which is half the diaphragm thickness ($\approx 4 \mu\text{m}$). The narrow $3 \mu\text{m}$ separation between the two electrodes (determined by the process constrained sacrificial oxide layer thickness) limits the dynamic range of the sensor, and as a consequence further thin plate analysis assumption also does not allow larger deflections (beyond the $2 \mu\text{m}$ range in this case). In general, deflection beyond half the diaphragm thickness can lead to short circuit/leakage due to electrostatic pull-in [6]. However, the perforated elliptic design reduces the possibility of early pull-in considerably due to reduced surface-area of the capacitance, thus providing further improvement in the linearity and dynamic range of the proposed SiGe-MEMS sensor fabrication. Finite element analysis (using COMSOL) revealed that a deflection of up to $2.2 \mu\text{m}$ does not significantly deteriorate the sensor performance. The deflection (w) of the elliptical diaphragm in thin plate analysis can be conveniently developed by modifying the analysis for a circular diaphragm in [5] as follows,

$$w = [S_o/64Dr_2^2](r_2^4 - r^2r_2^2) \quad (6)$$

Where, S_o is the applied pressure, r_2 is the length of the semi-major axis, r is the polar coordinate and D is the flexural rigidity. As per (6) the diaphragm deflection increases with an increase in the length of the semi-major axis (r_2) of the elliptic diaphragm. The maximum deflection is at the center of the diaphragm ($r = 0$) and is given by [7]:

$$w = S_o r_2^2 / 64D \quad (7)$$

In addition, the flexural rigidity, D is given by [8],

$$D = Et^3 / 12(1 - \nu^2) \quad (8)$$

Where, t and ν are respectively the diaphragm thickness and the Poisson's ratio. Substituting (8) into (7), the maximum deflection at the center of the plate can be given by,

$$w = (r_2^2 / t^3) [\{3S_o(1 - \nu^2)\} / 16E] \quad (9)$$

It is evident from (9) that the ratio between the length of the semi-major axis and the elliptic diaphragm thickness directly determines the deflection at the center of the diaphragm. Thin diaphragms can deflect more yielding good sensitivity, however linearity is penalized, hence more importance was given to the characterization of the radial dimensions of the diaphragm, r_1 and r_2 . The poly-SiGe material with its low Modulus of Elasticity (Young's Modulus) of around 130 GPa [9] provides increased deflection even at a very low applied pressure of 100 Pa. This provides the advantage of low minimum detectable pressure, and hence increasing the dynamic range of the capacitive sensor using a SiGe diaphragm. In addition, for the same surface area, the elliptic diaphragm element deflects more under a very low applied pressure compared to a circular diaphragm structure.

III. CMOS CONDITIONING CIRCUIT IMPLEMENTATION

The on-chip sensor interface signal conditioning circuit is required to convert the weak (μV range) noisy transduced sensor output to an amplified useful electronic signal with a low noise factor [10]. The low-level sensor signal is also somewhat degraded due to the RC transmission line effect of the electrical interconnect metal lines from the MEMS diaphragm micro-structure to the CMOS signal conditioning circuit. Thus the CMOS sensor signal read-out circuit design is a significant challenge and the overall performance of the sensor module largely depends on this implementation. The targeted CMOS circuit performance parameters are high gain, low noise, low power dissipation, high linearity and reduced area. The capacitance variation due to applied pressure on the diaphragm is converted into an electrical signal through a variable charging/discharging input signal current into a front-end trans-impedance amplifier as shown in Fig. 4. For this purpose the bottom plate of the capacitive sensor is excited by a DC bias voltage. An internally generated constant bias current I_{bias} is passed through a pair of diode-connected CMOS devices to set up this DC bias voltage (also shown in Fig. 4). In addition, a parallel CMOS transmission gate is employed to be able to momentarily discharge the bottom plate at the beginning of a sensing period. More details of the

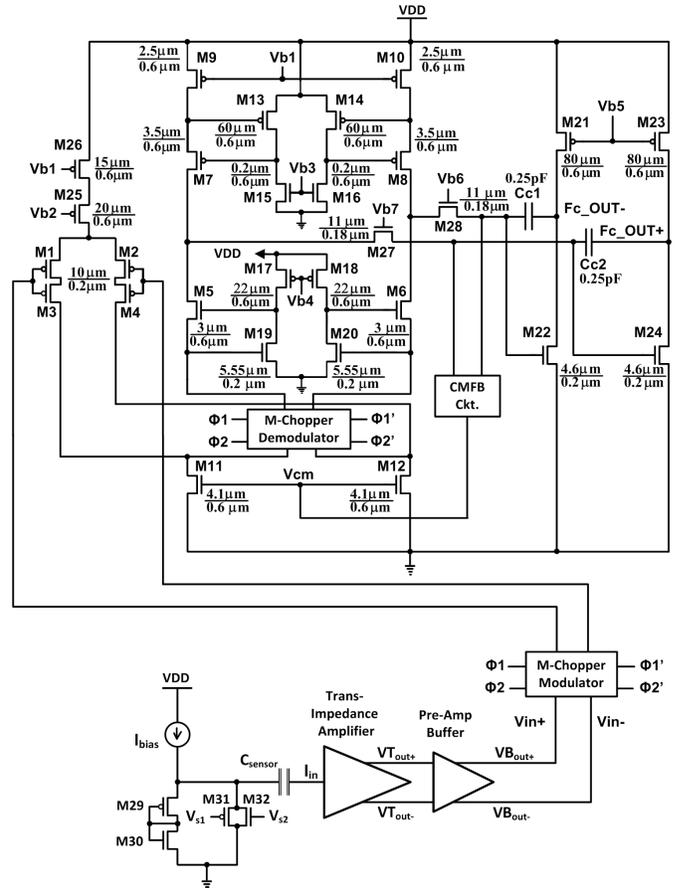


Fig. 4. Composite folded cascode opamp along with sensor front-end and chopper stabilization.

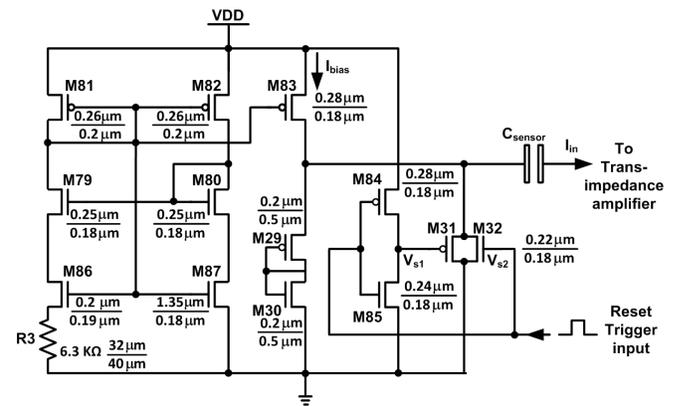


Fig. 5. Sensor startup, bias and transduction circuitry.

bias current generator and the signal transduction front-end are shown in Fig. 5. After signal transduction, the three main circuit components in the CMOS interface are the modified chopper stabilized op-amp, Gm-C low-pass filter and the self biased buffer stage. The $0.18 \mu\text{m}$ TSMC CMOS technology was used for the circuit design whose low voltage requirement constrained the achievable accuracy and linearity. In addition, the low supply voltage also results in limited input common mode range [11]. The two stage op-amp design for the readout circuit utilizes a doubly gm-booster folded cascode (FC) as

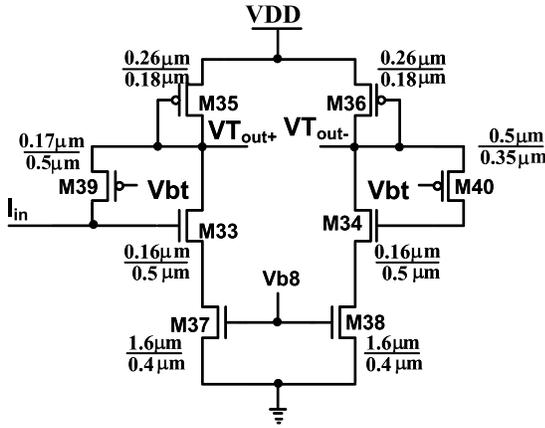


Fig. 6. Transimpedance amplifier and single-ended-to-differential converter of the sensor front-end.

the first stage. The composite gain enhancement is achieved by employing the g_m -boosting gain, A_c . If g_{mFC} is the overall transconductance of the FC input stage, and g_m the input differential pair transconductance, then, $g_{mFC} = g_m(1 + A_c)$ [12]. The negative feedback utilized within the doubly g_m -boosting cascode stage elevates the output impedance which also aids in the gain enhancement. The implemented doubly g_m -boosted FC op-amp yields a higher gain-bandwidth (GBW) product than the conventional FC structure, without increasing the power dissipation. Stacked PMOS input devices are employed in the FC stage for further enhancement of the transconductance. Since the noise injected by PMOS devices is an order of magnitude lower than NMOS devices, a relatively low input referred noise is achieved [11] by the opamp. The implemented two stage fully differential FC op-amp as shown in Fig. 4 provides large output swing and is less susceptible to common-mode noise compared to a single-ended version. Fig. 6 shows the low-noise transimpedance amplifier which converts the sensed current due to sensor capacitance variation into a voltage. It also performs the single-ended-to-differential conversion of the sensed signal. The total input referred noise voltage power of the FC op-amp can be approximately derived as,

$$\begin{aligned} \overline{V_{in_noise_{tot}}^2} &= 8kT \left(\frac{2}{3g_{m1,2}} + \frac{2}{3} \cdot \frac{g_{m5,6}}{g_{m1,2}^2} + \frac{2}{3} \cdot \frac{g_{m9,10}}{g_{m1,2}^2} \right) \\ &+ \left[\frac{2 \cdot K_P}{(WL)_{1,2} \cdot C_{ox} \cdot f} + \frac{2 \cdot K_N}{(WL)_{5,6} \cdot C_{ox} \cdot f} \cdot \frac{g_{m5,6}^2}{g_{m1,2}^2} \right. \\ &\quad \left. + \frac{2 \cdot K_P}{(WL)_{9,10} \cdot C_{ox} \cdot f} \cdot \frac{g_{m9,10}^2}{g_{m1,2}^2} \right] \end{aligned} \quad (10)$$

Where, K_P and K_N are respectively the PMOS and NMOS flicker noise coefficients with f being the operating frequency. Also, k is the Boltzman constant, and, T is the ambient temperature in K. In addition to the thermal noise, considering the proximity of the low operating frequency to the noise corner frequency, the flicker noise is a major component that increases the noise floor of the FC op-amp. In order to reduce the overall noise in accordance with (10); g_m of the

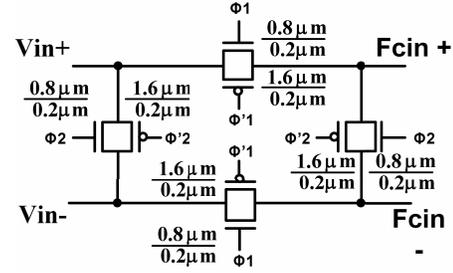


Fig. 7. Modified chopper network using differential transmission gate chopping.

input transistors is appropriately increased, while, on the other hand, the effective g_m of the current source and cascoding devices are kept somewhat low, while not restricting the drain current, I_D (in order to maintain reasonable slew rate). As the reduction in the g_m of current source/cascode devices usually undermines the output impedances with a consequent reduction in the overall voltage gain, a careful overall gain vs. noise design trade-off was considered. The employment of the fully differential chopper stabilization circuit (with a modified chopping scheme) within the composite FC op-amp structure enables improved output signal precision and significant noise reduction, thereby increasing the sensitivity of the CMOS front-end. In comparison, the conventional chopper introduces random spikes at the output causing a residual offset noise voltage of up to $500 \text{ nV}/\sqrt{\text{Hz}}$, which is significantly high for precision sensor application. The improved chopper stabilization is implemented using a transmission gate block so that negligible spikes remain after demodulation. The chopper stabilization is not utilized in the trans-impedance stage as spikes introduced by the chopper demodulator at the output of the trans-impedance amplifier would be amplified by the subsequent FC op-amp stage. Further, if a low pass filter is used to remove the spike residuals at the trans-impedance amplifier output, the overall power dissipation will be high. Thus, avoiding chopper stabilization at the trans-impedance stage, contributes to both area and power minimization without compromising the performance. Fig. 7 shows the differential transmission gate chopping circuit with in-phase and out-of-phase chopping frequencies. The employment of two different chopping frequencies along with complementary PMOS choppers makes possible the reduction of the residual offset spike noise voltage to the range of $100 \text{ nV}/\sqrt{\text{Hz}}$. The theoretically achievable improvement in residual offset noise is given by the ratio of $f_{\text{chophigh}}(\Phi_2)$ and $f_{\text{choplow}}(\Phi_1)$ [11]. In addition, the gain accuracy of the modified chopper is also found to be quite high. The implemented differential source-follower pre-amplifier buffer and the differential difference amplifier common-mode feedback (CMFB) circuit is shown in Fig. 8 and Fig. 9 respectively.

The stability and frequency compensation of the CMOS signal conditioning circuit was explored by locating the poles and zeros introduced by the parasitic capacitances. The pole-zero doublet inserted by the g_m -boosting stage degrades the transient response of the op-amp. This doublet appears as a slowly varying exponential term in the step

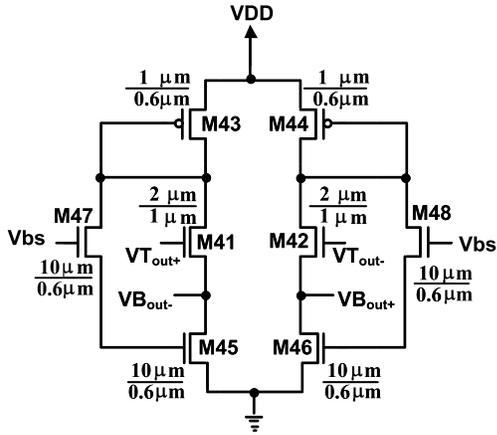


Fig. 8. Differential source-follower preamplifier buffer.

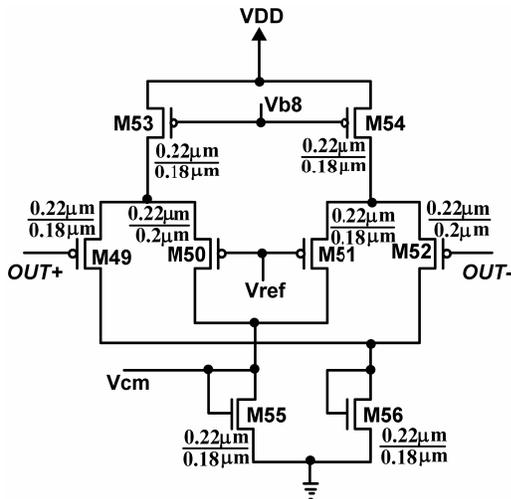


Fig. 9. Differential difference common-mode feedback circuit.

response thus increasing the settling time of the op-amp. In order to make the transient response similar to that of a single pole system, the zero, ω_z was pushed to a higher frequency by increasing the drain current (bias current) of the g_m boosting stage. The g_m of this stage was also appropriately adjusted (by varying the device aspect ratios) to transform the pole, ω_p into a complex conjugate pair [16], thus eliminating the slow response introduced by this stage. In addition, pole splitting through miller compensation provides stability to the two stage op-amp [13]. However this compensation introduces the penalty of a RHP zero. Increasing the impedance in the feed-forward path can push this RHP zero to a higher frequency, thereby restoring the enhanced stability [14]. Hence, an NMOS transistor biased in the triode regime (M27 and M28 in Fig. 4), in series with the compensation capacitor is utilized to yield improved stability over the conventional miller compensation technique. Appropriate settling behavior is ensured by proper choice of the coupling capacitor, C_c (C_{C1} and C_{C2} in Fig. 4) steering the phase margin above 45° . On the other hand, pronounced phase margin causes bandwidth limitations, and hence, a

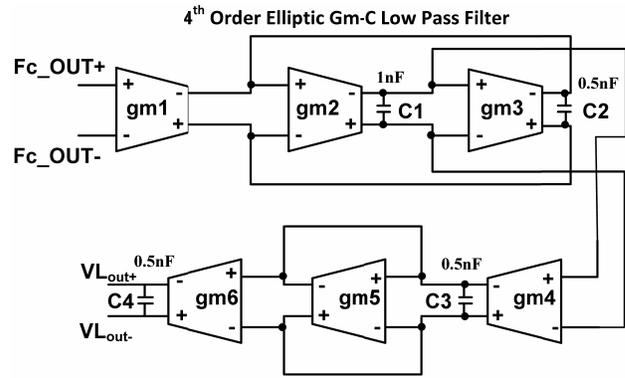
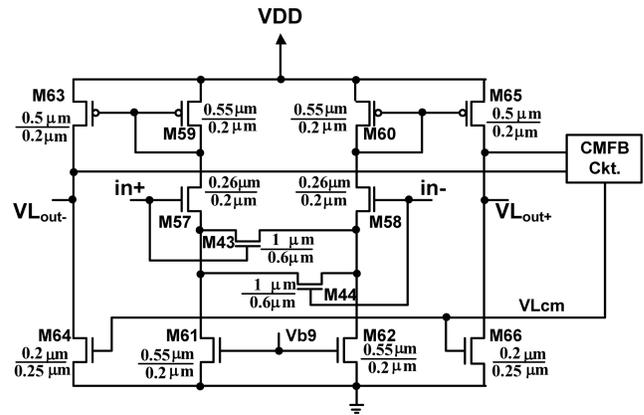
Fig. 10. A fourth-order elliptic low-pass G_m -C filter for sensor readout (after the FC chopper amplifier).

Fig. 11. Circuit diagram of the filter transconductance amplifier.

careful bandwidth vs. stability trade-off was considered in the implementation. Common mode feedback using the differential difference circuit is employed to set the common mode DC output level in order to achieve large output signal swing [14]. The common source (CS) second stage provides additional gain to improve the overall gain of the op-amp. The compensation capacitors effectively shorts the CS stage amplifying NMOS device into diode-connected loads for high frequency chopper residuals, thus suppressing these artifacts in the output compared to the sensed pressure signal. However, a high roll-off low-pass filter was needed to completely remove the chopping frequency remnants from the output. Continuous-time G_m -C filters provide adequate roll-off behavior even with lower order structures, and is thus well-suited for sensor signal conditioning. A 4th order CMOS G_m -C low-pass filter was cascaded at the output of the composite chopper stabilized amplifier. Fig. 10 shows the block diagram of the G_m -C filter. An active resistance ($1/gm5$) is employed in the final transconductance stage of the filter in order to reduce attenuation, so that, an overall low attenuation of -3 dB is achieved for this filter design. The circuit diagram of the filter trans-conductor is shown in Fig. 11. Usually, the final signal conditioned sensor output is required to drive an off-chip analog-to-digital converter (ADC) for display or for feed-back actuation purpose. The high output impedance at the output of the low-

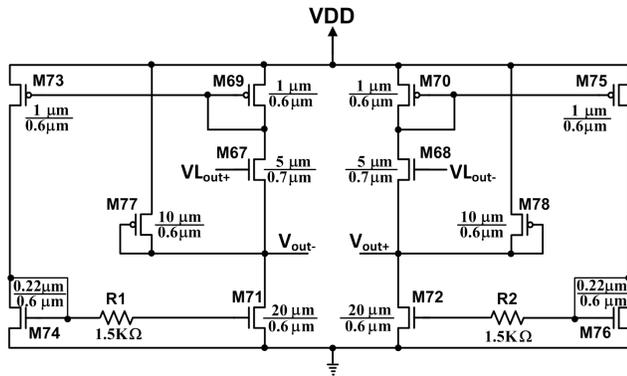


Fig. 12. Self-biased current-feedback output buffer.

pass filter is not suited to drive these off-chip components, and hence a low output impedance buffer driver circuit is utilized without sacrificing the overall linearity. Although simple unity-gain buffers can be realized using source followers, they are however, limited by non-zero offset and nonlinearity. Nonlinearity can be reduced by employing negative feedback but gate-to-source voltage drop of the source follower still introduces offset [15]. Current feedback can be used to significantly reduce the output impedance without the need for large device aspect ratios, so that an overall reduction in area and power consumption is achieved. A self-biased differential source follower buffer is designed using this technique as shown in Fig. 12, which can drive a large off-chip load of up to 15 pF.

IV. SENSOR AND CIRCUIT SIMULATION TECHNIQUES

In order to optimize the dimensions of the elliptic geometry diaphragm, finite element analysis (FEA) was carried out in COMSOL Multiphysics [28]. This versatile CAD tool provides electro-mechanics interface to combine solid mechanics and electrostatics modules. Two important parameters were targeted in optimizing the dimensions (semi-major and semi-minor axis) of the elliptic diaphragm for optimal deflection. Firstly, to achieve the desired linear capacitance variation with the applied axial (normal to the surface) pressure, and, secondly, to maximize the corresponding center deflection for wide dynamic range without causing touchdown (shorting the plates of the capacitive device) that limits the achievable dynamic range. To comply with the thin plate analysis, the dimensions of the elliptic diaphragm were optimized to get a maximum displacement of around $2 \mu\text{m}$ (for a fixed $4 \mu\text{m}$ diaphragm thickness as per the SiGe process specification [25]). Perforated elliptic geometries are not predefined in the CAD tools, further no option for creating such model directly in the 3D work plane of the geometry model tool is available. Hence the elliptic geometry is drawn in the 2D work plane with the desired dimensions, and then, multiple tiny 2D square blocks were drawn and difference Boolean operation was invoked to create perforations on the elliptic 2D structure. Extrude tool was then employed to create the 3D model of this geometry and material properties were assigned for the diaphragm. Further boundary conditions were

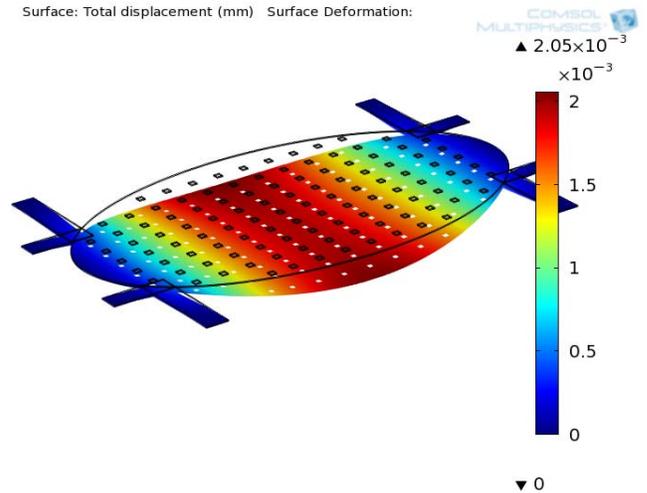


Fig. 13. COMSOL deflection analysis of the perforated SiGe-MEMS diaphragm.

applied and tetrahedral mesh size was optimized for sectorized FEA analysis. Linearly elastic material model was used to characterize the sensor. Solid mechanics physical analysis was utilized to study the displacement of the membrane for applied load pressure. The final optimized semi-major axis was $525 \mu\text{m}$, while the semi-minor axis was $310 \mu\text{m}$. Further, the optimized dimensions were found to provide a suitable pull-in voltage of around 35 V. The capacitance variation with applied axial load pressure (stress) and the corresponding vertical diaphragm displacement for the entire load sweep was explored in this solid mechanics analysis. For the parametric pressure sweep, axial load from 10 hPa to 1000 hPa in steps of 10 hPa, resulted in displacement variation from $0.09234 \mu\text{m}$ to $2.05 \mu\text{m}$. Deformed geometry interface [28] that uses Arbitrary Lagrangian-Eulerian (ALE) method to deform the mesh, was used to visualize the nature of the model deflection. A separate rectangular structure (block) to represent the air dielectric medium between the capacitive electrodes was designed. This helped in forming a moving mesh physical model between the top and the bottom solid mechanics plate models in order to extract the varying simulated capacitance under the applied pressure. Electrostatic physical analysis was then carried out to acquire the diaphragm surface capacitance and the instantaneous capacitance variation. The incremental capacitance variation (ΔC) was between 0.0463 pF to 0.8213 pF (a fluctuation over the no-load “resting” diaphragm capacitance of 2.57 pF) due to the deflection of the diaphragm, under pressure load from 50 hPa to 1000 hPa. The simulated sensitivity of the sensor is thus around 0.775 fF/hPa (with around 1% non-linearity). The COMSOL simulated deflection analysis of the perforated SiGe diaphragm is shown in Fig. 13. Figs. 14 and 15 displays the simulated sensor characteristics in terms of capacitance variation (ΔC) vs. pressure, and, diaphragm displacement (Δz) vs. applied pressure load (in the range of 50 hPa to 850 hPa) respectively. The simulated results indicate performance enhancement in terms of dynamic range, minimum detectable pressure (stress) and diaphragm elastic limit.

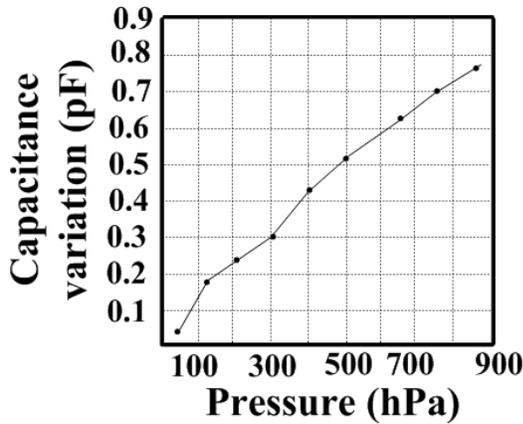


Fig. 14. Capacitance variation with applied pressure.

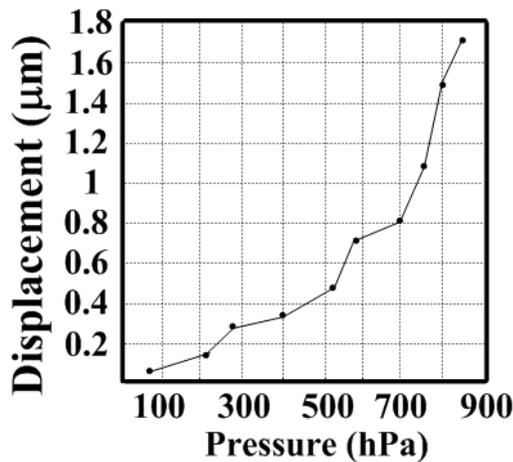
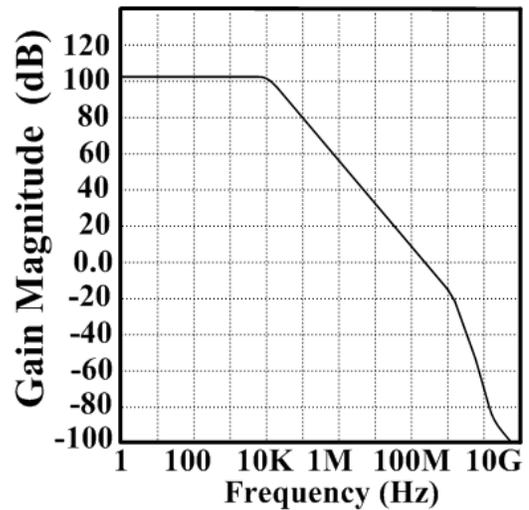


Fig. 15. Inter-electrode displacement variation with applied pressure.

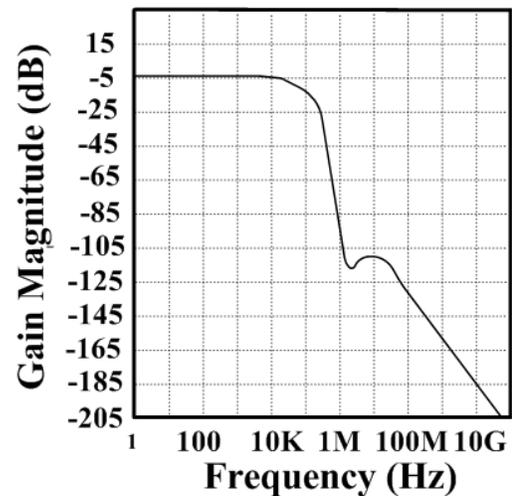
Circuit design and analysis of the CMOS signal conditioning circuit in 0.18 μm TSMC technology was carried out using the Tanner T-SPICE. Simulations indicate that a gain of 105 dB along with 64° phase margin and $100 \text{ nv}/\sqrt{\text{Hz}}$ input referred noise is achieved by the implemented sensor amplifier. An unity gain bandwidth of 200 MHz is also achieved which is adequate for the pressure sensor duty cycle in this application. The phase margin of 64° proves that the operational amplifier is stable in a closed loop configuration despite the significant open loop gain. Figs. 16 (a), (b) and (c) depicts the frequency response of respectively the FC op-amp, the low-pass 4^{th} order G_m -C filter (pass-band gain $\approx -3\text{dB}$) and the output buffer (pass-band gain $\approx 0\text{dB}$). The modified transmission-gate chopper used 10 kHz and 100 kHz chopping frequencies (assuming $1/f$ flicker noise corner frequency at 1 kHz). It offered lower spikes compared to a conventional chopper when excited with a sinusoidal input signal. Simulation results plotted in Fig. 17 indicate a high overall sensitivity of 0.17 mV/hPa (@1.4 V supply voltage) for the integrated sensor system.

V. SENSOR FABRICATION AND EXPERIMENTAL RESULTS

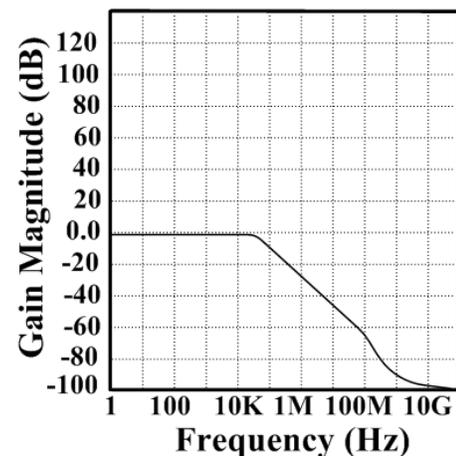
The CMOS integrated poly-SiGe MEMS diaphragm with the signal conditioning electronics was fabricated and



(a)



(b)



(c)

Fig. 16. AC analysis of: (a) composite chopper FC op-amp, (b) G_m -C low-pass filter, and (c) self-biased output driver/buffer.

post-processed through the Europractice MPW foundry (run no: 3499, imec SiGeMEMS). A photo of the ESD-protected, wire-bonded and DIL28-packaged

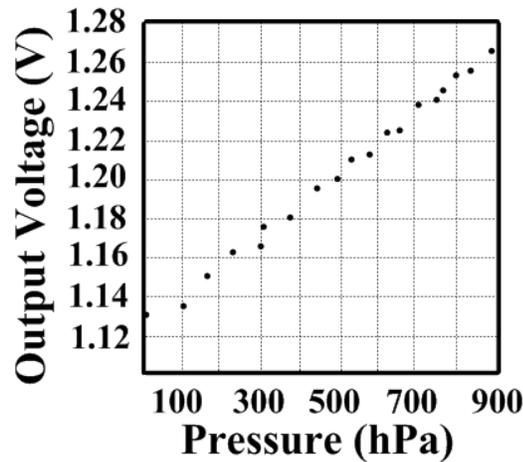


Fig. 17. Applied pressure versus output sensor voltage using a 1.4 V supply.

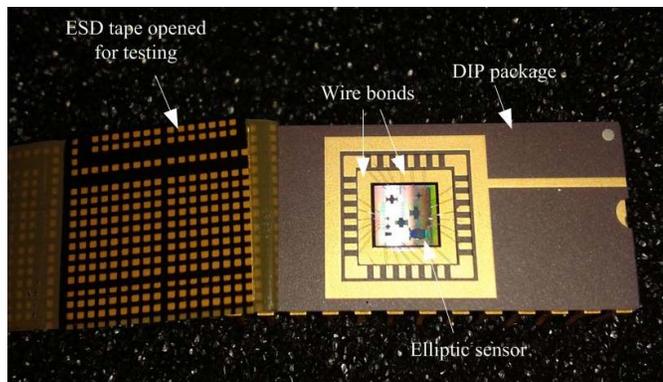


Fig. 18. Photo showing the ESD-protected, wire-bonded and DIP-packaged, SiGe-MEMS-CMOS capacitive pressure sensor.

CMOS-SiGeMEMS capacitive pressure sensor chip is shown in Fig. 18. With the cross-section of the co-hosted CMOS-SiGe process indicated earlier in Fig. 3, the microphotograph of the experimental chip (top view outlining the diaphragm) is shown in Fig. 19. The location of the underlying CMOS signal conditioning circuit is also indicated on the chip photo by the broken-line rectangular box. The “piggyback” structure effectively reduces the combined sensor and conditioning circuit implementation area of the intelligent sensor chip to around $750\mu\text{m} \times 750\mu\text{m}$ (including the anchors). This is thus a more compact intelligent sensor system compared to that in [18] where the signal condition circuit could not be place directly under the metal diaphragm due to back-end-of-line (BEOL) layout and thermal issues. Fig. 20 shows the mask layout of the CMOS signal conditioning circuit in 180 nm TSMC CMOS with labels indicating the location of the various circuit components.

The standard TSMC 0.18 μm technology MPW run uses 8 inch (100) silicon wafer with around $725\mu\text{m}$ thickness. The p-substrate has a resistivity of $0.01\ \Omega\text{-cm}$. The FEOL process mainly consists of n-diffusion, p-diffusion, n-well, polysilicon gate, gate oxide, shallow trench isolation (STI), substrate contact, n-tiedown and p-tiedown. The NMOS, PMOS and the resistor devices are designed using these layers. The circuit

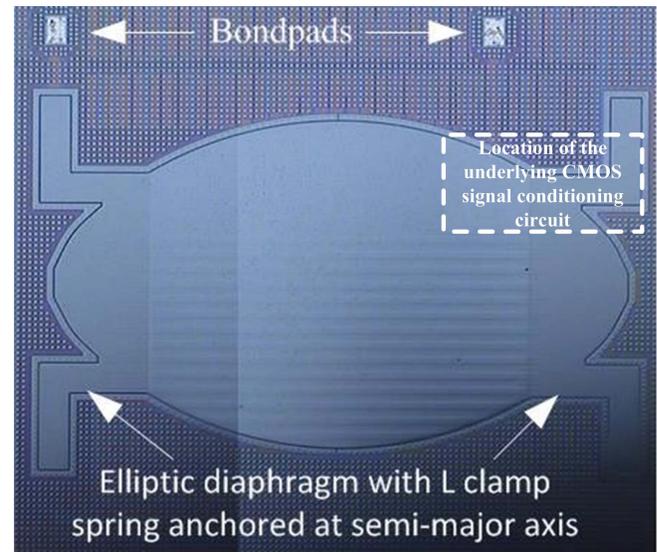


Fig. 19. A photo-micrograph of the fabricated poly-SiGe elliptic diaphragm in CMOS integrated SiGe-MEMS process. Location of the underlying CMOS signal conditioning circuit is also indicated by the broken-lined rectangular box.

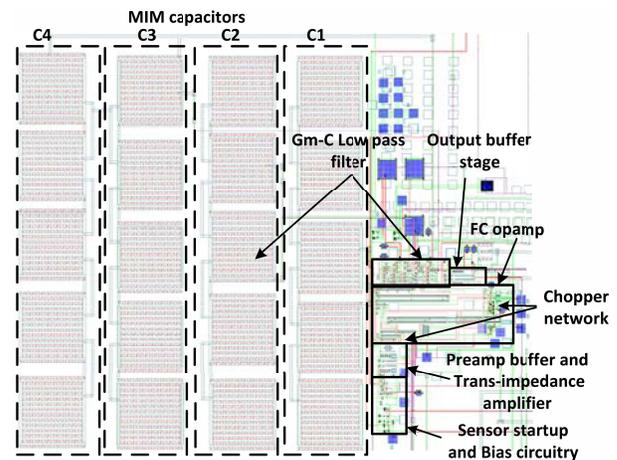


Fig. 20. Layout of the signal conditioning circuit showing details of the CMOS components fabricated in 180 nm TSMC CMOS substrate beneath the poly-SiGe-MEMS diaphragm.

interconnects and MIM capacitors are designed using 2 thin and 2 thick metal BEOL layers. The top (4th) metal layer is designed appropriately to accommodate interconnections with the MEMS devices. Once the CMOS implementation is complete, the wafer is subjected to the SiGeMEMS process which uses the CMOS wafer as the starting substrate. The first process starts with the patterning of the top CMOS metal layer for MEMS device interconnections. Then planarization oxide layer is deposited extending 600 nm above the CMOS top metal for better isolation. Next, a SiC protection layer is deposited to protect the underlying CMOS circuitry from the HF based release etchant. Vias are then developed to make the interconnections between the CMOS top metal and the MEMS device. Next SiGe electrode layer is deposited and patterned to make interconnections to the bondpads. This electrode layer is also patterned to form the MEMS capacitive

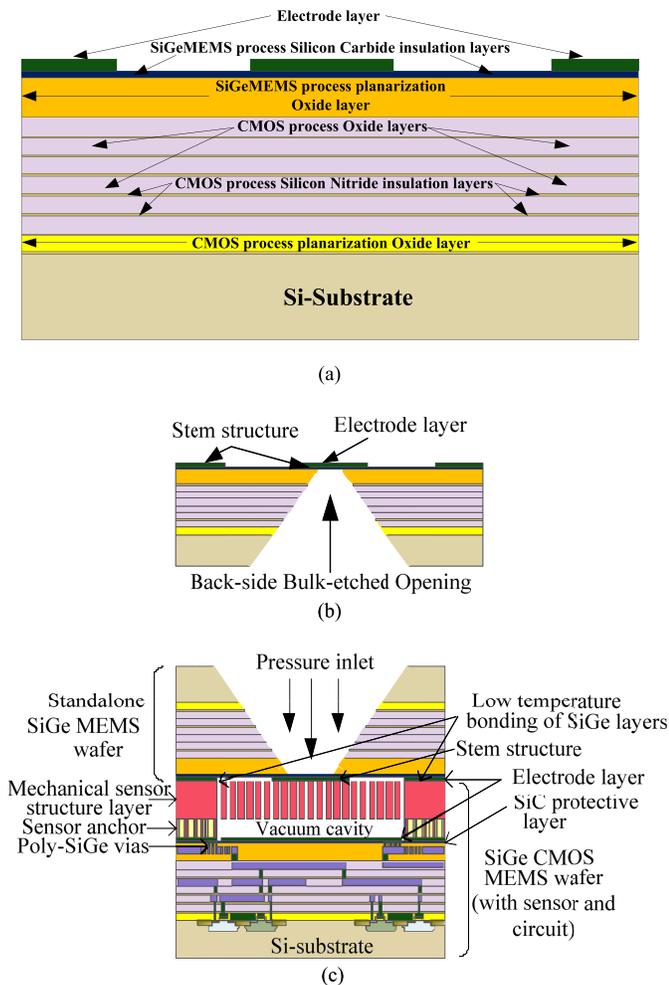


Fig. 21. Vacuum sealing of the CMOS integrated SiGe-MEMS pressure sensor: (a) standalone substrate material with the electrode patterning, (b) standalone substrate material after back-side bulk etching for pressure inlet, and (c) bonded wafers for experimental measurement.

device bottom plate. The process is then continued with the deposition of sacrificial planarization oxide and then the anchors are formed. A $4\ \mu\text{m}$ SiGe structural (mechanical) layer is then deposited and patterned to achieve the designed MEMS device. Next, passivation openings are created for bondpad contacts followed by the bondpad metal deposition. Release holes are then patterned and finally the structural mechanical layer is released.

A. SiGe Sensor Sealing

Device sealing is necessary for operation of the fabricated structure as an absolute pressure sensor. It was undertaken by utilizing a separate substrate material subjected to a wafer process that is compatible with the SiGe-CMOS-MEMS chip processing steps [25]. Firstly, a standalone SiGeMEMS process is carried out on a isolated Si substrate, with the process being terminated after patterning the electrode layer as the top layer for this wafer (carried out at Europractice). This sealing substrate material with the electrode patterning is shown in Fig. 21(a). Next silicon substrate back-side bulk etching (*in the form of a rectangular funnel*) is performed on this wafer material as shown in Fig. 21(b). Once this standalone wafer element docks on top of the previously processed

SiGe-CMOS-MEMS sensor device, its back side opening acts as a pressure inlet passage for the main sensor device. The backside etching of the standalone substrate material must open the passage just up to the point of exposure of the silicon carbide (SiC) layer. Hence, deep reactive ion etching (DRIE) is carried out for the sealing substrate preparation in Fig. 21(b). Sulfur-hexafluoride (SF_6) and octafluorocyclobutane (C_4F_8) plasma are used alternatively for etching Si, while fluoroform (CHF_3) plasma is used for oxide etch. Since the wafer has a $\langle 100 \rangle$ orientation the anisotropic etch cuts along the $\langle 111 \rangle$ direction. As the electrode layer is patterned mostly into a shallow structure with central and edge stems, the SiC layer must be preserved to keep intact the underlying layers and hold the wafer element as a mechanical support. However, since the terminal conical backside etch is very much confined to the central stem structure region, wafer damage due to backside etch is negligible. A direct bonding between the SiGe-CMOS-MEMS wafer and the back-side bulk-etched standalone SiGe wafer is then carried out under high vacuum to form the absolute capacitive pressure sensor. As the top layer of both the wafers are composed of SiGe (with 70% Ge in the $\text{Si}_{1-x}\text{Ge}_x$ super-lattice) material, bonding temperature exceeding the SiGe deposition temperature may change the material properties of the mechanical device layer. Furthermore, CMOS circuit metal interconnects can withstand temperatures of up to around $500\ ^\circ\text{C}$. Considering the above limitations, low temperature plasma activated direct bonding is performed after initial pre-processing by chemical mechanical polishing (CMP) to planarize the top layers of both the wafers. Annealing is then performed at a temperature within $400\ ^\circ\text{C}$ to enhance the strength of the bonding. The cross section of the composite bonded wafers is shown in Fig. 21(c). The central stem of the electrode layer on the top standalone SiGe wafer is employed to transfer stress onto the diaphragm (capacitive sensor's mechanical layer) hosted by the bottom wafer under external applied pressure through the back-side inlet of the top stand-alone wafer. In addition, since the maximum deflection occurs at the center of the elliptic diaphragm, the top electrode layer of the standalone SiGe-MEMS wafer (top wafer in Fig. 21(c)) is designed to transfer the applied stress mostly at the center of the poly-SiGe diaphragm underneath (bottom wafer in Fig. 21(c)). To increase the bonding profile, additional dummy poly-SiGe mechanical layers with anchors were fabricated throughout the top un-structured region (vacant regions where the target diaphragm is not present) of the SiGe-CMOS-MEMS wafer without exceeding the maximum pattern density. This technique provides additional freedom in patterning stem electrode structure on the standalone SiGe-MEMS wafer solely for transferring stress on to the target diaphragm with applied pressure. With such a bonding profile, the bonding strength of the sealed cavity does not have to solely depend on the bonding between just the stem structure and the diaphragm, as there is a high probability that bonding strength between these two target layers may diminish. This is due to stress by the repeated application of pressure loads during testing. This technique thus ensures that the functionality of the sensor device will be maintained even under such circumstances.

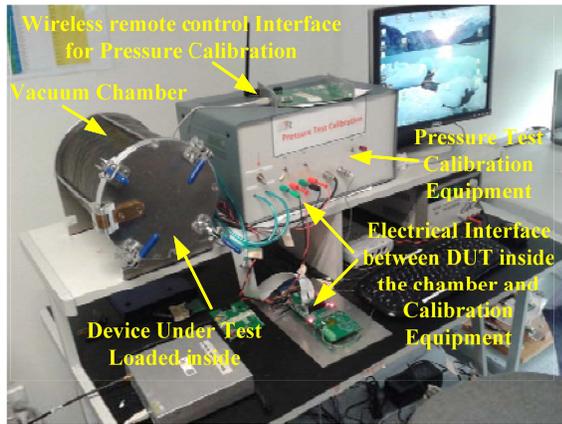


Fig. 22. Pressure test calibration equipment setup for experimental measurements.

B. SiGe-CMOS Capacitive Sensor Experimental Test Results

The fabricated SiGe sensor diaphragm as shown in the photomicrograph in Fig. 19 had semi-major and semi-minor axis dimensions of $485 \mu\text{m}$ and $280 \mu\text{m}$ respectively. The vacuum cavity below the diaphragm has a height of $3 \mu\text{m}$. The diaphragm being $4 \mu\text{m}$ thick can yield to a linear pressure sensitivity range with displacement of up to $1.5 \mu\text{m}$ in accordance with thin plate theory as discussed in section II. The wire-bonded CMOS integrated sensor chip is kept in a vacuum chamber for experimental analysis of device sensitivity, linearity, hysteresis and repeatability. This setup is shown in Fig. 22. The sensor capacitive transduction measurement under a wide pressure range was performed using the lead transfer from the chip to the external LCR meter through the electrical interface of the vacuum chamber. A 1.4 V DC from regulated power supply was utilized to power the on-chip signal conditioning circuit and to excite the integrated capacitive pressure sensor. A pump was used to create the initial vacuum inside the device-under-test (DUT) chamber while a nitrogen source was used to increase the pressure from the initial vacuum condition. The pressure test calibration equipment shown in Fig. 22 controls the vacuum pump and the nitrogen gas source. The observed sensor capacitance and the signal conditioning circuit output voltage under a wide pressure variation range are depicted in the Figs. 23 and 24 respectively. The linear capacitive sensing range of the diaphragm device during pressure up from 4 to 900 hPa was 0.1 to 0.69 pF with a device sensitivity of 0.0065 pF/hPa . Again, during pressure down the sensing range is from 900 to 7 hPa and the sensitivity is marginally higher being 0.0066 pF/hPa . This range is slightly lower compared to the simulated capacitive sensing range in Fig. 14. The observed device hysteresis, and repeatability (*test-retest reliability*) were 0.038% and 0.024% respectively which are similar to other recent designs using metal diaphragms [18], but the poly-SiGe diaphragm allows higher dynamic range with very low non-linearity of around 1%. The repeatability of 0.024% indicates that the difference in stresses on the four L-springs over time are within the limit of satisfactory performance of the device. The offset

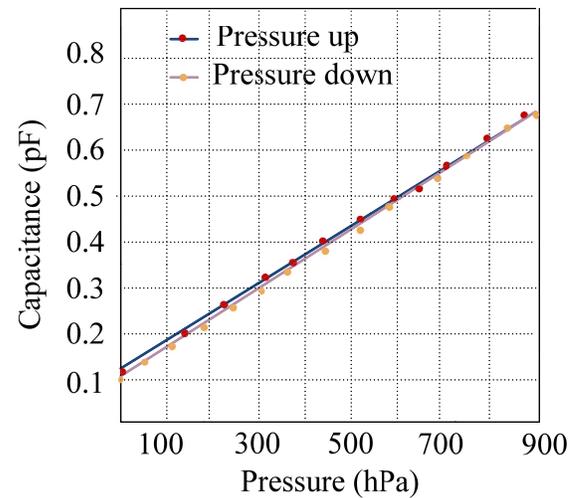


Fig. 23. The plot of measured capacitance versus applied pressure for the elliptic poly Si-Ge diaphragm.

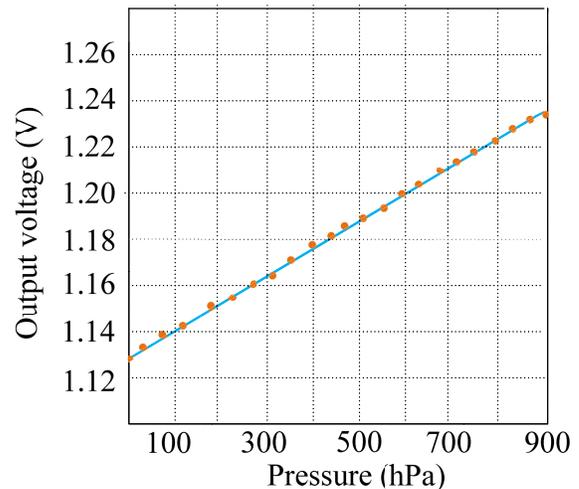


Fig. 24. The plot of the measured conditioning circuit output voltage vs. applied pressure for the composite CMOS integrated SiGeMEMS Sensor.

capacitance if any can be effectively compensated using an off-chip reference capacitor. The measured output voltage of the signal conditioning circuit indicate an overall sensor system sensitivity of around 0.12 mV/hPa along with a wide dynamic range of around 900 hPa. The measured results appear to closely agree with the simulation in Fig. 17. The slight deviation in the linear sensing range and the overall sensitivity compared to the simulation may be due to residual stress and surface capacitance variation as a result of sealing and wafer bonding. Experiments indicate that the sensor's cavity (under the diaphragm) bear some residual pressure even-though the sealing is performed under nominal vacuum condition. This is possibly due to some gaseous residues being trapped inside the cavity during sealing. Residual pressure test (pressure scanning test) [17] conducted by lowering the pressure below 4 hPa indicate a residual pressure of around 2 hPa (@ $24 \text{ }^\circ\text{C}$). This is due to the outward deformation of the diaphragm with the pressure inside the cavity becoming higher than the applied

TABLE I
COMPARISON OF SEVERAL CAPACITIVE SENSOR DIAPHRAGMS

| Device design (diaphragm) reported | Process technology | Device (diaphragm) geometry | Sensitivity | Nominal linear dynamic range | On-chip signal conditioning | Off-chip lead transfer | Minimum detectable pressure (MDP) | Non-linearity |
|------------------------------------|--------------------|-----------------------------|-------------|------------------------------|-----------------------------|------------------------|-----------------------------------|---------------|
| This Work | SiGe-CMOS MEMS | Elliptical | 0.12 mV/hPa | 100 hPa to 1000 hPa | Yes | Not required | 4 hPa | <2% |
| [17] | MEMS | Square | 0.08 pF/kPa | 80 kPa to 106 kPa | No | Required | 10 kPa | <2.3% |
| [19] | MEMS | Circular | 150 aF/Pa | 1000 Pa to 2000 Pa | No | Required | 3 hPa | N/A |
| [20] | MEMS | Circular | 26.7 fF/hPa | 600 hPa to 800 hPa | No | Required | 30 hPa | N/A |
| [21] | CMOS MEMS | Square | 0.14 mV/kPa | 0 to 300 kPa | Yes | Not required | N/A | <5.16% |
| [22] | SOI-CMOS MEMS | Rectangular | 2 mV/kPa | 0 to 180 kPa | Yes | Not required | N/A | N/A |
| [23] | CMOS MEMS | Square | 2.84 fF/hPa | 700 hPa to 1100 hPa | No | Required | 100 hPa | <1.1% |

pressure after becoming just equal to it. Hence the minimum applicable pressure (MAP) is around 2 hPa. In case of metal or poly-Si diaphragm of similar size the MAP will be around 15 hPa or higher. Hence, low-pressure sensing is not suitable using such diaphragms. For other larger diaphragms the MAP may be as high as 1000 hPa. At an applied driving voltage of 33.2 V between the plates, the perforated diaphragm touches the bottom electrode due to the electrostatic deflective force. This pull-in voltage is found to be around 64% less than that of a similar geometry non-perforated clamped diaphragm (with 51 V pull-in voltage) in [23]. In addition it is also lower than the 38 V pull-in voltage of the slotted diaphragm in [24]. The low pull-in voltage indicates that the perforated diaphragm has low internal stress and stiffness, which is a vital performance parameter for enhanced sensor transduction. The overall measured pressure range, sensitivity and pull-in voltage of the capacitive sensor demonstrate that a vacuum sealed perforated elliptic SiGe diaphragm anchored at semi-major axis yields optimal performances with minimal residual pressure compared to other reported diaphragm sensors. Linear buckling analysis performed prior to fabrication indicated that the structure can withstand a high stress of around 210 MPa. The regular placement of $10 \mu\text{m} \times 10 \mu\text{m}$ perforations throughout the diaphragm has effectively lowered the residual stress. The residual stress that can limit the performance of the diaphragm is found to be only around 7 MPa. Thus the designed structure is considered to be reliable and robust.

Table I shows a comparison of several capacitive diaphragm sensors with the fabricated capacitive sensor. The presented sensor achieves minimal detectable pressure while providing on-chip signal conditioning, as well as, high sensitivity and linearity compared to the other designs.

The performance was also investigated in comparison to commercially available pressure sensors. The low pressure sensing capability of the fabricated device is an order of magnitude less than the 60 kPa minimum sensing achieved by a commercial pressure sensor such as KP236N6165 [26]. Further, the 5.5 V supply voltage required by KP236N6165

is quite high compared with the 1.4 V used in this proposed device. In addition, the sensitivity per Volt of supply voltage for the proposed low-voltage pressure sensor is also higher when compared to the sensitivity of the KP236N6165. Another commercial pressure sensor with part-name PS-AN13 [27], is found to be limited by poor low pressure sensing capability of only up to 6.9 MPa. Also, it requires a power supply of 4.5 V and hence has a higher dissipation than the proposed device. The achieved performance of the designed device is thus significant without compromising the dynamic range.

The higher prototyping cost of the proposed device owing to the use of two separate processes (CMOS and SiGe) can be amortized through volume (mass) production. A possible shortcoming could be the diminishing bonding strength between the stem structure and the diaphragm over time; however, proper bonding profile is implemented on the other regions of the die to maintain the device integrity. Another possible shortcoming is that, any spatial SiGe process variations in the regions of the four L-clamp springs could lead to imbalance of the elliptic diaphragm. However, in order to overcome this, the tip edges at the opposite sides of the diaphragm's semi-major axis are anchored, while ensuring that the deflection due to the spring action of the L-clamps is not hampered. This anchoring also lowers the sensitivity towards mechanical noise. Further, only a cluster of less than 10 anchors is used so that the desired minimum detectable pressure is achieved. The vacuum sealing of the sensor and the clamp springs, along with the transfer of applied pressure only on to the diaphragm center through a stem structure, ensures that there is no undesired pressure on any sections or directions on the diaphragm.

VI. CONCLUSION

A highly sensitive integrated capacitive pressure sensor is designed, fabricated and characterized through measurements using a $0.6 \mu\text{m}$ feature-size SiGe MEMS process. The on-chip co-hosted signal conditioning circuitry is fabricated in $0.18 \mu\text{m}$ TSMC CMOS process vertically integrated (in 3D) with the MEMS process. The capacitive pressure sensor is simulated and measured under a range of pressure loads. The novel perforated elliptic diaphragm, clamped to anchors at the semi-major axis exhibited linear operation in a wide dynamic range. Clamp springs designed to edge clamp the poly-SiGe diaphragm increased the sensitivity significantly without degrading the linearity performance. A high gain precision conditioning circuit is fabricated to cater for the low supply-voltage and weak sensor signal. Non-linearity of around 1% was achieved by the fabricated sensor for the full scale range of applied pressure. This integrated pressure sensor, based on the measured performance characteristics (with overall sensitivity of 0.12 mV/hPa @ 1.4 V supply voltage), can be used for biomedical applications such as catheter pressure monitoring and intraocular pressure measurement.

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A Transconductance Doubling CMOS Regulated Folded Cascode (TD-RFC) for Micro-Sensor Readout

S. Ananiah Durai and S. M. Rezaul Hasan

The requirement of high gain and low noise for sensor readout amplifier is addressed in this letter. A novel current cross mirroring technique is employed to enhance the small signal current. The small signal current is increased by a factor that depends on the input stage current mirroring ratios F and H of the proposed Recycled Folded Cascode (RFC) operational amplifier. The increased small signal current doubles the transconductance (g_m) thus yielding very high single stage gain. Four fractionally split input differential pair transistors are used for achieving further increase in gain without compromising the unity gain bandwidth. Bias current splitting yielded better slew rate and faster settling time at reduced DC power dissipation. Simulation results using the 130 nm IBM CMOS technology demonstrated a gain of 86.4 dB for the single stage fully differential mode of the proposed amplifier. A significantly wider open loop bandwidth of 210 MHz was also achieved for an 82.5° phase margin. In addition, an input referred noise level as low as 48.3 μ Vrms was also achieved.

Introduction: Operational Transconductance Amplifier (OTA) dominates the micro-sensing system circuit design due to its high transconductance (i_{out}/v_{in}) gain and negligible harmonic distortion. Telescopic and Folded cascode (FC) OTA topologies are the major building block for various CMOS amplifier stages, with FC being the preferred topology due to better gain and signal swing. The inherent advantages such as low flicker noise, low common mode level and higher non-dominant poles, makes PMOS transistors more appropriate as FC input stage [1]. A number of techniques were reported for improving the performance of the FC opamp [1]-[4], however power budget was significantly high. Unity gain bandwidth was also compromised by scaling down the size of the input transistors, e.g., in [1]. On the other hand, using multistage amplifiers for achieving higher amplification introduces additional noise and pole-zero pairs, thus degrading the performance of a sensor readout circuit. Switched Capacitor (SC) OTAs are another alternative, but their aliasing issue makes them unsuitable for low frequency transducers such as in a pressure sensor application. Moreover, SC amplifier in a sensing system application needs an output filter stage for eliminating the unwanted spikes. The proposed design overcomes the above discussed limitations. Transconductance of the input stage is doubled by a novel current cross mirroring technique, thus significantly increasing the gain of a single stage Recycled Folded Cascode (RFC) amplifier. Transmission gate chopper stabilization circuit that ensures negligible high frequency spikes is employed to reduce the input referred noise. The aspect ratios of the input and the output driving transistor are chosen appropriately for low power consumption without compromising bandwidth.

Circuit Design and Analysis: It was demonstrated in [1] that the g_m of an RFC is improved by splitting the input transistors and recycling the current. However, since the current flows through only half the aspect ratio (or *fractional aspect ratio*) compared to the conventional FC input transistors, it experiences a high resistance path ($r_o=1/\lambda I_D$), which limits the small signal current and hence the overall g_m . Alternatively, a similar technique but with multiple cross mirroring is employed in this proposed design which compensates the trade-off between output resistance and g_m of the input stage, allowing the unconstrained enhancement of g_m .

The input stage of the proposed g_m doubling RFC is shown in Fig. 1. The conventional FC input pair are split into four fractional pairs; hence no compromise is made in terms of silicon area and power. The aspect ratios of the four split input transistors are in the ratio $P: Q: Q: P$, where Q is kept very small in order to achieve negligible change in the output resistance of the splitted input stage when compared to [1]; hence, I_D is not affected. The bias current $2I_b$ that flows through the cascode current source $M25$ and $M26$ is divided by the aspect ratios of the input transistors by a factor of 3 on either branch of the input transistors. Considering one half of the differential circuit i.e. $M1a, M1b, M1c$ and

$M1d$, the device aspect ratios are chosen such that $I_b/3$ flows through $M1a$ and $M1d$ and $I_b/6$ flows through $M1b$ and $M1c$. When all the input transistors are in saturation, considering the small signal current for differential operation, current through $M1c$ is mirrored with a ratio of H by transistors $M3c$ and $M4d$. This increased current is again summed with the currents of transistors $M2c$ and $M1d$ and cross mirrored with a ratio of F by transistors $M3a$ and $M3b$. Bias current that flows through the output stage can be given as

$$I_o = I_z = \frac{I_b}{6} [F(3-H) - 2] \quad (1)$$

Finally, the small signal currents through $M3a$ and $M1a$ combine and flows into the output stage. The small signal output current of the proposed RFC (after differential to single-ended conversion by the output stage) is then given by, $i_{out,diff} = g_{m1a,2a} \cdot v_{in,diff} [(FH)/2 + F/2 + F + 1]$ that flows through the output current summing network in Fig. 1.

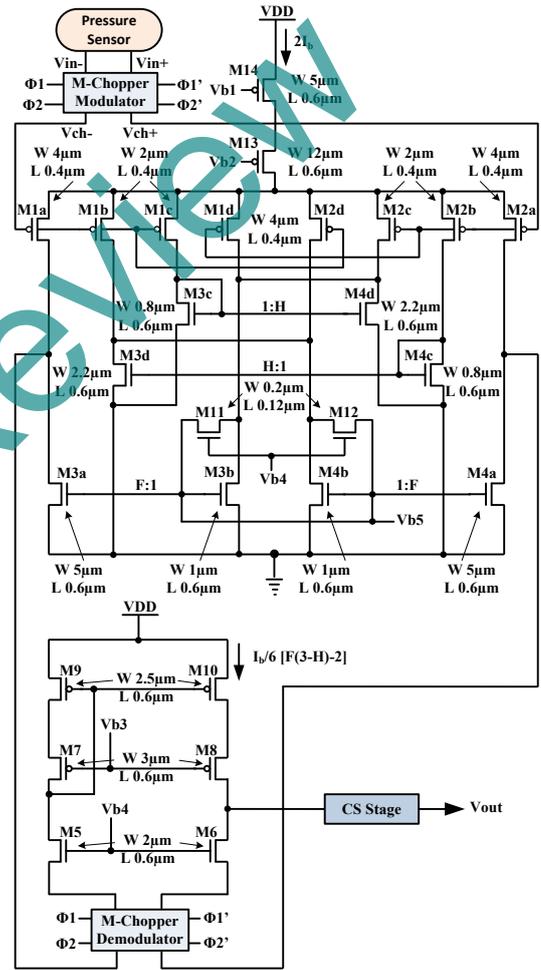


Fig. 1 Proposed Transconductance doubling RFC

The transconductance given by the RFC in [1] for the input stage is,

$$G_m = (g_m/2) [K - 1] \quad (2)$$

Whereas, for the proposed circuit it is found from fig.2 as

$$G_m = (g_m/3) \left[\frac{F(H+1) + N(F+1)}{N} \right] \quad (3)$$

where g_m is the transconductance of the conventional FC and N is the transistor aspect ratio scaling factor (between each inner device with the outer device, being 2 in Fig. 1). It was found that when the scaling factor N is set to 2 along with the mirror factors F and H being set close to 2, the transconductance actually doubles in accordance with (3) when

compared to [1]. The ratios F & H being 2 does not hold true for the biasing aspect of the output stage, as can be noted from (1) that I_o becomes zero. Hence ratio F is increased for achieving proper output bias current without driving the input transistors to triode region. Current mirror ratio H is kept constant at 2 to ensure proper values of V_{GS} and V_{DS} of the input stages, so that even with process variation the transistors are not driven out of saturation. It was found that with F being varied from 6 to 10, all the transistors were in saturation and the circuit is significantly stable with a high open loop gain of 88 dB. Moreover, it is evident that increasing the output impedances of $M6$ ($M5$), $M8$ ($M7$) and $M10$ ($M9$) in the cascoding differential-to-single-ended converter provides additional increase in the overall gain. However, considering the power dissipation and the bias current limitations, the aspect ratios of these devices are kept reasonably low. Additionally, reduction in the size of $M1a$ ($M2a$) and $M3a$ ($M4a$) due to bias current splitting further increases the output impedance of the input stage [1], [2]. Thus, an overall increase in gain of 14 to 16 dB is achieved for this single stage amplifier. Another advantage is that the increased resistance at the high impedance nodes pushes the non-dominant poles to higher frequency yielding better phase margin and stability. Higher phase margin causes a better roll-off in the gain curve beyond the dominant pole. Thus a significant improvement in the unity gain bandwidth is also achieved. In addition, increase in the gain also results in better Power-Supply-Rejection-Ratio (PSRR).

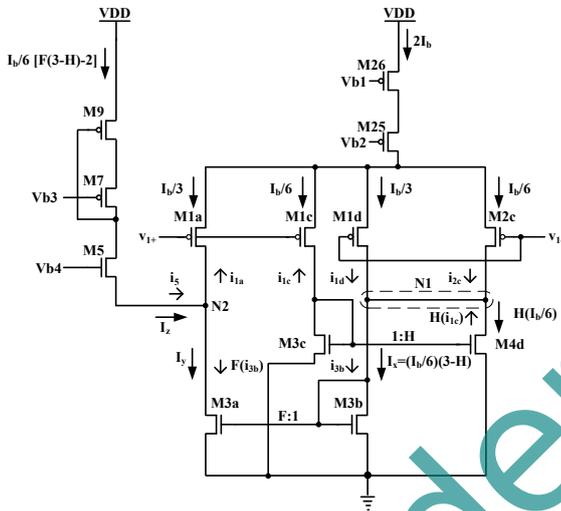


Fig. 2 One half of the proposed transconductance doubling RFC

The critical parameter that directly affects the settling time and linearity apart from thermal effects is the slew rate. In fig.1, when v_{i+} increases so as to switch off the transistors $M1a$, $M1b$, $M1c$, and $M2d$, bias current $2I_b$ flows entirely through $M2a$, $M2b$, $M2c$, $M1d$, thus the slew rate can be given as

$$SR = \frac{[F(3-H)-2]I_b}{3C_L} \quad (4)$$

Increase in bias current due to current cross mirroring ratios enhances the slew rate by two and a half times with $F = 10$ and $H = 2$ when compared to conventional FC op-amp. Moreover while comparing to RFC the symmetrical slew rate has increased by a factor of 1/2 when the signal input is within the transient limit. This is achieved by keeping the aspect ratios of the differential output load transistor pair equal, for the single ended output design shown in fig. 1. For the differential mode output to achieve symmetric slew rate, CMFB circuit can be employed to balance the differential output charge/discharge rates, thus the overall speed of the proposed sensor readout is significantly increased with same area and power. The CMFB circuit must be carefully designed to obtain better loop gain and bandwidth in fully differential mode operation. Fig.3 shows the slew rate response comparison between RFC and gm enhanced RFC with a pulse excited amplifier. It can be noted that the overshoots during the rise and fall of the pulse are significantly reduced in the proposed amplifier, the positive and negative slew rate has substantially increased.

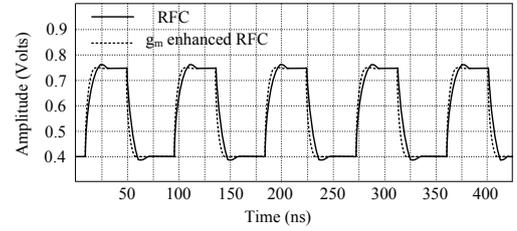


Fig. 3 Pulse response of the proposed amplifier

Implementation and Simulation results: Area and power are critical parameters in CMOS sensor readout circuit design. Considering the sensor readout requirement, a 130 nm CMOS technology (e.g., the 8RF-DM process available from IBM) was preferred, as further channel length scaling can result in low transconductance and hence low gain. The sizes of $M1b$, $M1c$, $M2b$ and $M2c$ whose currents are cross-mirrored from one half of the differential pair to other are kept low in order to achieve the proper current mirroring ratio for the indirect transconductance enhancement. Aspect ratios of devices $M1a$, $M1d$, $M2a$ and $M2d$ are kept higher for the direct transconductance enhancement. The sizing of these devices was given critical consideration so that their small signal impedances didn't lower the unity gain bandwidth. BSIM4 sub-100 μm regime model using Mentor Graphics platform was employed for the simulations. The diode connected devices $M3b$ and $M4b$ are implemented using the triode regime linear active switches $M11$ and $M12$ respectively. The devices $M11$ and $M12$ are sized so as to provide proper drain voltages for $M3b$ and $M4b$ respectively that ensures the devices remain in saturation. This helps to avoid non-linearity and hence achieve the proper (desired) small signal current mirroring ratio. An overall gain of 86.4 dB and a phase margin of 82.5 degree (@ 0 dB gain) was achieved for the single stage amplifier as depicted in Fig. 2. A unity gain bandwidth of 210 MHz was also achieved without compromising gain or stability. The proposed g_m -doubling RFC stage thus meets the critical performance requirements of a sensor readout amplification circuit. In addition, a high output voltage swing of 0.8 V for the 1.2V supply-voltage was obtained as shown in fig. 5 by using a common-source (CS) output stage. The cascode biasing stage was designed to ensure good upper and lower bounds of the slew rate (i.e. $SR+$ and $SR-$) achieving a high slew rate of 27.2V/ μs . The input referred noise was lowered to 48.3 μVrms by employing dual frequency transmission-gate choppers. The amplifier also achieved a very high THD (Total Harmonic Distortion) of -75 dB for a 1kHz input as shown in Fig. 6.

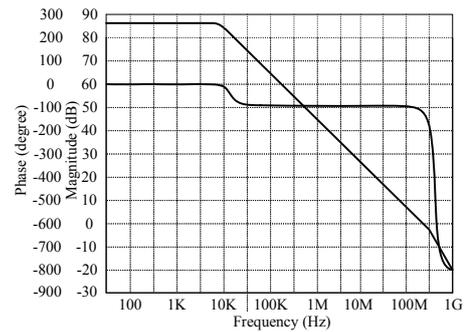


Fig. 4 AC analysis of the proposed Enhanced- g_m RFC

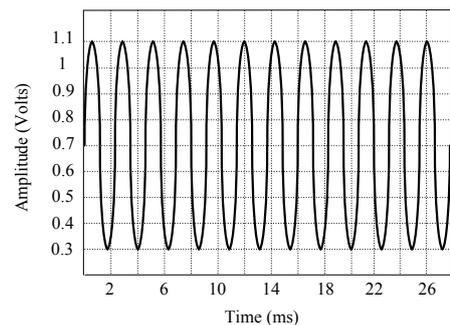


Fig. 5 Transient response of the proposed amplifier

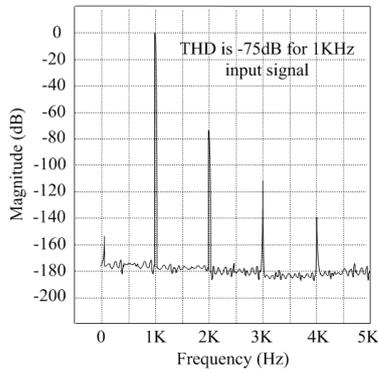


Fig. 6 THD analysis for the proposed Enhanced- g_m RFC

Experimental Results: The g_m boosting RFC amplifier was fabricated in IBM 130 nm CMOS process utilizing the low supply option of 1.2 V. Fig. 7 shows the amplifier experimental test setup. A Tektronix AFG 3252C dual signal generator was used to supply the input signal and the output was captured using a Tektronix TDS 6154C oscilloscope. To preserve the high output impedance of the amplifiers and limit the DC output current drawn, RC load setup was done externally with R set to 350 k and the two capacitances (C1 and C2) set to 3.3 pF and 4.2 pF, respectively (the value includes 0.14 pF pad capacitance). Along with 0.5 pF of the Tektronix P6960 single ended active probe, the overall load is approximately 7.7 pF. The amplifier is configured such that the output will have the maximum swing. The GBW of the proposed two stage amplifier design is found to be around 82 dB. The observed low gain when compared to the simulation could be due to process variation and inherent error due to chopper residuals. However a high single stage gain of around 75 dB is observed that demonstrates the achieved gain enhancement due to current cross mirroring. The phase margin at this GBW is calculated to be around 82.5 degree, which is slightly higher than the simulation result. In addition, amplifier exhibited no ringing in transient performance. To measure the gain bandwidth of the amplifier experimentally, a small signal step, 100 mVpp at 10 MHz was applied to the input and the 1% settling time (4.6 time constants) was measured. The small signal step response of the amplifier found to have similar bandwidth as that of RFC; however, the 1% settling times of 11.7 ns is significantly low when compared to 20.8 ns settling time of RFC. This is in good agreement with the simulation result. The DC gain of the amplifier extracted from the peak to peak amplitude of the step response is almost similar to that of RFC with around 56 dB. For the slew rate measurement, a large step input of 1 Vpp at 1 MHz was applied to the amplifier. The average slew rate for this g_m enhanced RFC is found to be significantly low with 28.3 V/ μ s than FC and RFC for the same bias current. Furthermore, no signs of ringing are noted in the step response, which shows that the addition of multiple current mirrors in the RFC amplifier input stage has negligible effects on the amplifier's phase margin. The linearity of the amplifiers can be measured through their distortion behavior. A 1 Vpp two tone test centered at 500 KHz and separated by 100 kHz (100 mVpp at 400 KHz and 100 mVpp at 600 KHz) were applied to the amplifier. The FFT data of the output revealed that the third intermodulation distortion IM3 is around -65 dB. The improved IM3 performance denotes that the amplifier is highly linear compared to the FC and RFC designs. According to the slew rate results presented earlier, the proposed amplifier can support signals up to 100 MHz without slewing. Hence a significant decrease in gain is noted in the experimental result when compared to the simulation; however its bandwidth is still comparatively higher than FC and RFC amplifiers. This wider bandwidth in the proposed design yielded a higher gain around 500 KHz and hence the improved IM3 performance.

Conclusion: It has been demonstrated that by using the proposed current cross mirroring technique a significant gain increment of 15.9 dB was achieved compared to [1], without compromising the unity gain bandwidth. Using lower bias drain and area budget the proposed amplifier achieves adequate slew rate and settling time, which is critical for the low frequency sensor readout application. Table I provides the performance comparison between FC, RFC and the proposed g_m -

doubling RFC. The design parameters such as device sizes, bias voltages, and the values of F, H and N are carefully assigned to ensure that the proposed design is robust against process, supply voltage and temperature variation.

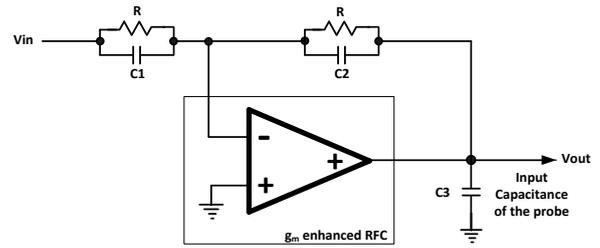


Fig. 7 Experimental setup for the proposed Enhanced- g_m RFC

Table 1: Performance comparison of different RFC circuits

| Parameters | Folded Cascode [1] | Recycled Folded Cascode [1] | Improved RFC [2] | g_m Doubling RFC [This Work] |
|-------------------------------------|--------------------|-----------------------------|------------------|--------------------------------|
| Bias Current (μ A) | 260 | 260 | 260 | 185 |
| C_L (pF) | 7 | 7 | 7 | 7 |
| Gain (dB) | 41.1 | 60.9 | 70.2 | 75 |
| UGBW (MHz) | 70.7 | 134.2 | 83 | 210 |
| Slew Rate (V/ μ s) | 42.1 | 94.1 | 59.6 | 27.2 |
| 1% Settling Time (ns) | 20.7 | 11.2 | - | 11.3 |
| Input Referred Noise (μ V rms) | 53.2 | 48.5 | - | 48.3 |
| Phase Margin | 83 | 77 | 70.2 | 82.5 |

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High sensitive Absolute MEMS Capacitive Pressure Sensor in SiGeMEMS Process for biomedical applications

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Abstract- A high sensitive CMOS Micro-electro-mechanical rectangular capacitive pressure sensor in SiGeMEMS process (Silicon Germanium Micro-electro-mechanical System process) is designed and analyzed. Polycrystalline Silicon Germanium (Poly-SiGe) having low fatigue and high strength is effectively used as the sensor diaphragm material to achieve better reliability. The designed perforated diaphragm clamped only at the short sides, yielded high sensitivity, large dynamic range and better linearity. On-chip signal processing circuit in 0.18 μm TSMC CMOS technology is designed to achieve a high single stage gain of 86 dB. A higher sensitivity of 8.72 mV/V/hPa, with a non linearity of less than 1% for the full scale range of applied pressure load is achieved. The diaphragm having a wider dynamic range of 2 hPa – 500 hPa has increased low pressure capability for pulmonary wedge pressure measurement. With the underlying design of CMOS circuitry the micro-system has a reduced chip area for implantable device application.

Keywords: Poly SiGe, Microstructure, Bondpad, Stress, Strain CMOS, Perforation, TSMC, Chopper.

I. INTRODUCTION

CMOS circuit integration with the mature MEMS capacitive devices is an increasingly researched area for implantable and non implantable bio-medical applications in recent years. A substantial improvement in the performance of the micro-sensor system through integration has greatly influenced this growth in the rapid product development of on-chip sensors and actuators. Eventhough the production of these devices are increased over the past decade, improvement in terms of sensitivity and dynamic range compounded with the reduced area of the sensor is still a concern. Further, the commercial products available do not provide accurate low pressure sensing capability. Moreover, the invasive and non-invasive bio-medical pressure measurements pose a greater challenge in designing a miniaturized sensor with high performance. Most commercialized pressure sensor either use capacitive and piezoresistive sensing principle [1]. Reduced process and fabrication steps combined with its low temperature variation and environmental effects have popularized the implementation of capacitive sensing technique over piezoresistive. However lowering the parasitic effects remains a greater design challenge of this versatile

sensing device. This made the on-chip integration of readout and sensor devices as one of the mandatory design target [2].

Hybrid and monolithic are the two integration techniques used. The nonlinearity and poor reliability over time made hybrid technique a poor choice for integration of sensor devices and the associated readout circuitry. On the other hand, monolithic integration eventhough has long time from production to tape-out; it has become popular as it offers low production and packaging cost [3]. The emerging SiGeMEMS monolithic integration of sensor devices directly on top of the CMOS (Complementary Metal Oxide Semiconductor) circuit (Silicon Germanium Micro- electro - mechanical System) has become popular, as it effectively miniaturized the micro-sensor system. Further, due to the low temperature material properties, MEMS post-processing can be easily performed without degrading the CMOS circuit and interconnects.

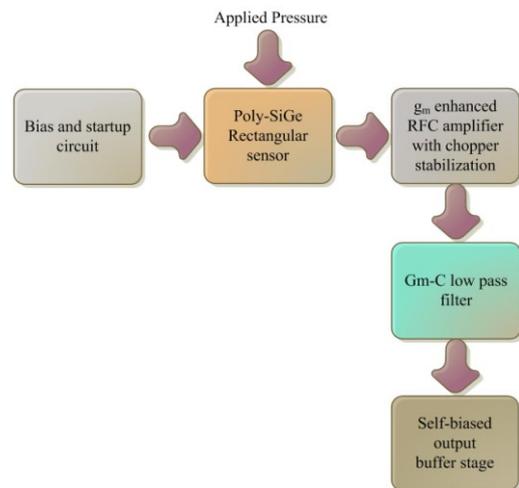


Figure 1. Functional Block Diagram

Various efforts are underway with varied diaphragm geometries and dimensions to optimize the performance of the device. The researches over the decades are improving the performances such as device sensitivity, system linearity and overall dynamic range [1] to [4]; however as the device is bulky it posed limitations for use in implantable bio-medical

applications. Reducing the device thickness for system miniaturization and improved sensitivity has resulted in good low pressure sensitivity; however it has significantly increased the non-linearity [2]. A unique integration process that overcomes this trade-off with improved sensitivity is proposed in this design. The rectangular perforated poly-SiGe diaphragm clamped only at the short-side edges provides better low pressure sensing capability as well as better linearity. The functional block diagram of the proposed micro-sensor system is shown in figure 1. The random extremely low and weak noisy signal from the capacitive sensor is amplified with a significantly low noise g_m enhanced RFC opamp (Recycling Folded Cascode operational amplifier). Higher order Gm-C low pass filter removes the high frequency chopper residuals at the output of the amplifier. Finally, the output buffer stage is utilized to drive an off chip load of up to 15pF. The design target for the short-side edge clamped rectangular structure is to achieve wider dynamic range, without compromising sensitivity and linearity. This paper is organized as, in section II, the structural and fabrication aspect of the micro-sensor is described, in section III, the model analysis and characteristics study of the microsensor is given, finally conclusion of the entire study is presented in section V.

II. DESIGN AND CHARACTERIZATION OF SENSOR DEVICE

The reduced parasitic effect due to CMOS integration resulted in extremely low noise capacitive device. This sensing technique is a relatively simple method that uses varying distance thereby varying current to pick up the physical quantity. Although this technique is less cumbersome to harsh environment over Piezoresistive counterpart; proper structural design can provide relatively low hysteresis and greater stability.

A. Theory

The rectangular structured diaphragm of the capacitive pressure sensor is designed with regular perforations for increased deflection and to reduce electrostatic pull-in. Further, clamping only at the short side edges of the diaphragm enables increased low pressure sensitivity compared to the all edge clamped sensor. When the pressure load is applied on the diaphragm, the distance between the diaphragm and the bottom electrode decreases, this causes the capacitance to increase. The capacitance due to fringe capacitance is made negligible by increasing the length of the diaphragm; hence capacitance variation ignoring fringing effects can be given as [4];

$$C = \frac{\epsilon_r \epsilon_0 A}{d} \quad (1)$$

Where ϵ_r is relative permittivity of the dielectric material, ϵ_0 is the permittivity of free space, A is the Area of the diaphragm and d is the distance between the electrodes. The effective area of the diaphragm is reduced by increasing the perforations for minimizing fringe effect on the capacitance variations. Increase in the applied pressure increases the stress and strain distribution on the diaphragm, which in turn causes increased deformation. The two-sided edge clamping allows the diaphragm to deflect more in the center, whereas a gradual decrease in deformation can be noted near the clamped edges.

This results in a non uniform change in the distance between the diaphragm and the bottom electrode. Capacitance thus is also not uniform throughout the area, hence integrating (1) over the 2D distance between the electrodes will give the exact total capacitance. This can be given as [4];

$$C = \iint [\epsilon_0 / d_0 - D(x, y)] dx dy. \quad (2)$$

Where d_0 is the distance between plates at zero pressure and $D(x, y)$ is the distance after deflection. The plate deflection for a rectangular diaphragm with a concentrated lateral pressure load of P can be expressed as;

$$w(x, y) = (4P / \pi^4 Dab) \sum_{m=1,3,5,\dots} \sum_{n=1,3,5,\dots} \frac{\sin m\pi x / a \sin n\pi y / b}{(\frac{m^2}{a^2} + \frac{n^2}{b^2})^2} \sin m\pi x / a \sin n\pi y / b \quad (3)$$

where a is the length of long side of the rectangular diaphragm, b the length of the short side, m is the bending moment in x direction, n is the bending moment in y direction and w the effective deflection in z direction is integrated over the entire area of the rectangular diaphragm. The parameters to be determined for effective deformation analysis are displacements, strains and stresses. The in-plane components are assumed to be uniform through the plate thickness as the diaphragm is of homogeneous material. Hence the dependence on z becomes negligible and all the components become functions of x and y only. The in plane stress tensor can then be given by [5];

$$\sigma(x, y) = \begin{bmatrix} \sigma_{xx}(x, y) \\ \sigma_{yy}(x, y) \\ \sigma_{xy}(x, y) \end{bmatrix} \quad (4)$$

The diaphragm thickness is very small compared to the other dimensions, hence assumption of Kirchhoff's hypothesis is considered in the analysis of deflection. Further the maximum displacement will be half the thickness of the diaphragm, therefore 2D plane stress analysis of thin plate is best suited. The stress components and the stress matrix can be simplified as [5];

$$\sigma = \begin{bmatrix} \sigma_x \\ \sigma_y \\ \sigma_{xy} \end{bmatrix} \quad (5)$$

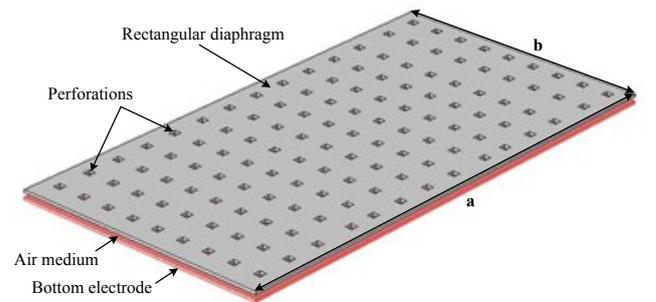


Figure 2. Perforated Elliptical diaphragm, clamped at the major axis using clamp spring

Assuming the diaphragm material to be isotropic, the linear behavior within the elastic limit region can be considered. The assumptions of stress and strain relationship based on Hook's law up to the elastic limit can be given by [5];

$$\sigma = E\varepsilon. \quad (6)$$

σ , is the stress due to applied pressure, ε the strain due to stress and E the modulus of elasticity.

B. Structural description and fabrication

Rectangular structured diaphragm using Poly-SiGe material of dimension $130 \mu\text{m} \times 258 \mu\text{m}$ and thickness $4 \mu\text{m}$, is clamped at both the short side edges for curvilinear deformation of the diaphragm at low pressure loads. On contrary, the deflection of diaphragm clamped at all four sides is almost negligible at very low applied pressure yielding poor sensitivity and low dynamic range [3]. CMOS sensor readout chip is used as the starting substrate for developing this low pressure sensitive microstructure. Reduced interconnection length is achieved by this type of monolithic integration which led to reduced parasitic effect and improved signal pick off strength. Otherwise the micro-ampere signal from the sensor is degraded due to the large resistance in the long interconnection metal wires from CMOS circuit to microstructures. The excellent material properties and low deposition temperature of poly-SiGe material is highly compatible with the CMOS part, hence there will be no drift in the performances of the underlying PMOS and NMOS transistors.

The interconnection of microstructure and CMOS circuit is done through a less resistive poly SiGe vias. The Top Aluminum metal layer of CMOS process is used as the interconnection metal wire to connect electrodes of capacitive sensor to the bondpad. The protection between the MEMS structure and CMOS circuits is achieved through a 400 nm thick silicon carbide (SiC) layer. Multiple poly-SiGe anchors of height $3 \mu\text{m}$ and width $0.8 \mu\text{m}$ firmly clamps the diaphragm at either short side edges. Arrays of anchors are used for obtaining a specific bending moments at the edges that can withstand the specified high pressure range. As Anchors are semiconductive, precautions are taken in designing the bottom electrode to avoid short circuit.

The oxide sacrificial layer is etched out through the perforation on top side of the diaphragm, using it as the release holes. The dimension of the release hole being $10 \mu\text{m} \times 10 \mu\text{m}$ is spaced $10 \mu\text{m}$ apart throughout the entire diaphragm, thus obtaining relatively less deflection at high pressure ranges. The displacement of the diaphragm is $2 \mu\text{m}$ for an applied pressure of 100 kPa , which is half the thickness of the diaphragm. The narrow distance of $3 \mu\text{m}$ between two plates limits the dynamic range of the sensor, further thin plate analysis assumption also does not permit larger deflections (beyond $2 \mu\text{m}$ in this case). Generally, deflection beyond half the thickness of diaphragm can lead to short circuit due to pull in voltage [6], however the perforated diaphragm design has reduced the electrostatic pull-in substantially due to less surface capacitance, thus providing further increase in the linearity and dynamic range. The analysis revealed that deflection up to $2.2 \mu\text{m}$ does not affect sensor performances.

The maximum deflection that occurs at the center of the rectangular diaphragm can be given in the thin plate regime as [5];

$$w_{\max} = \alpha \frac{Pb^4}{Eh^3} \quad (7)$$

where α is a constant that depends on the ratio of short side and long side length of the diaphragm, P is the applied pressure, b the short side length of the rectangular diaphragm, E is the young's modulus and h the thickness of the diaphragm. From (7), it can be noted that the deflection of the diaphragm increases with increase in length of the short side of the rectangular diaphragm. The maximum stress at the centre of the diaphragm can be given as [7];

$$(\sigma_{yy})_{\max} = 0.4974 \frac{Pb^2}{h^2} \quad (8)$$

The comparatively low young's modulus of 130 GPa in poly-SiGe material offers low flexural rigidity that contributes to increased deflection. This is evident from (8) below;

$$D = Eh^3 / 12(1-\nu^2). \quad (9)$$

where, ν is the poison's ratio. From (7) it is evident that the increased value of the length of the diaphragm, the deflection increases; however for improved linearity a nominal value of 2 is chosen. Substituting the value of α for the length ratio 2, (7) can be given as

$$w_{\max} = 0.0277 \frac{Pb^4}{Eh^3} \quad (10)$$

From '(9)' it is evident that the ratio between length of short side and thickness of the rectangular diaphragm directly influences the deflection at any point. Thin diaphragms can deflect more yielding good sensitivity, however linearity is penalized, hence more importance was given for characterization of the diaphragm dimension such as a & b. The fabricated device is shown in fig. 5, the location of the underlying CMOS circuitry is also marked with a rectangular box.

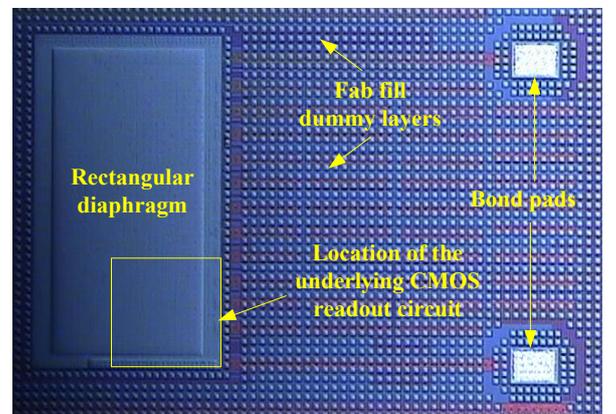


Figure 5. Microscope photograph of Perforated rectangular diaphragm

III. SIMULATION RESULTS

Finite Element Analysis was carried out in COMSOL Multiphysics for optimizing the dimensions of the rectangular diaphragm. Two important aspects were considered in this analysis. Firstly, to study the variation of capacitance to the applied pressure and secondly, to observe the amount of displacement that causes the change in capacitance for the load sweep. The later is critical in studying the linearity of the device. The dimensions of the diaphragm were also optimized to reduce fringing capacitance [8] & [9]. Linear elastic material model assumptions were used to characterize the sensor. Solid Mechanics physics was utilized to study the displacement of the membrane for the pressure load applied.

For the parametric pressure sweep load from 1 hPa to 500 hPa in steps of 50 hPa, the displacement varied from 0.0454 μm to 1.6 μm . Moving mesh model physics for the dielectric layer was assigned between the top and bottom solid mechanics model to extract the varying capacitance under the applied pressure. Electrostatic physics analysis was carried out to pick up the surface capacitance and the instantaneous capacitance. For the bias voltage of 1.4 V, the capacitance varies from 0.0565 pF to 0.838 pF due to the deflection of the membrane, under pressure load from 100 Pa to 500 hPa. The sensitivity of the sensor is calculated to be around 0.0016 pF/hPa. Figures 6 to 8 depicts the sensor's characteristics, linearity and performances. The result shows improved performances in terms of dynamic range, minimum detectable pressure and diaphragm elastic limit.

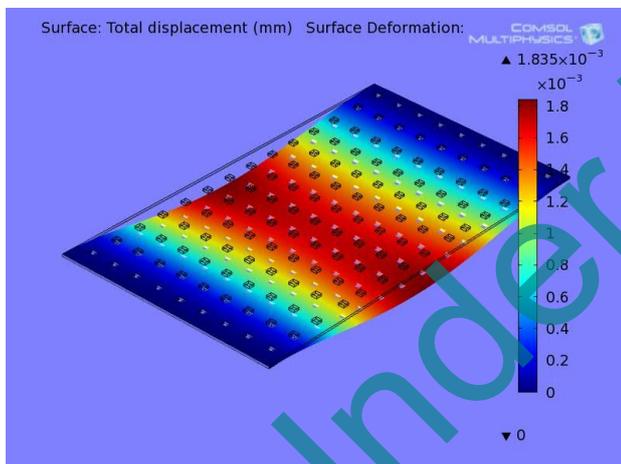


Figure 6. Deflection Analysis of Perforated diaphragm

Design and analysis of CMOS Signal processing circuit in 0.18 μm CMOS TSMC technology is carried out utilizing Tanner tool. The g_m enhanced RFC opamp with chopper stabilization provided a substantial increase in the gain; hence an appreciable increase of around 10 dB in the gain over the previous work is achieved. The single ended closed loop opamp gain is 86.4 dB and the overall gain of the sensing circuit is 95.6 dB at the buffer output. The closed loop gain for the fully differential configuration is calculated to be 105dB. A phase margin of 82° proves that the operational amplifier is stable despite the tremendous increase in the open loop gain. A high overall sensitivity of 4.765mV/V/hPa is successfully achieved for the integrated sensor system.

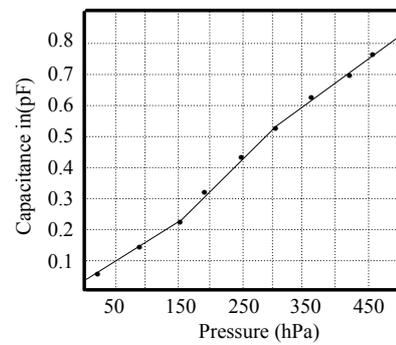


Figure 7. Capacitance Variation with applied Pressure

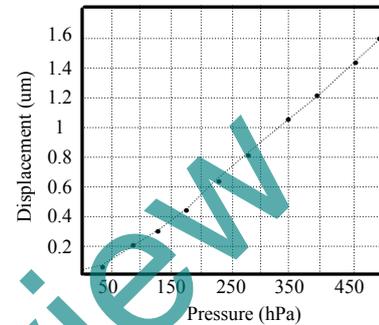


Figure 8. Displacement variations for applied pressure

IV. CONCLUSION

A highly sensitive integrated capacitive pressure sensor is designed and characterized with a 0.6 μm feature size; the on-chip signal processing circuitry is designed in 0.18 μm TSMC CMOS technology. The Capacitive Pressure sensor is analyzed under range of pressure loads. The perforated rectangular diaphragm, clamped only at the short sides yielded wider dynamic range. the two sided edge clamped diaphragm offered increased sensitivity without degrading the linearity performances. High gain Sensing circuit is designed to cater for the low and weak output signal of the sensor. This integrated pressure sensor, based on the observation of the performance characteristics proves that, if proper packaging steps are considered, the device can be configured appropriately for biomedical application such as pulmonary arterial pressure measurement, catheter pressure monitoring and intraocular pressure measurement.

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Under Review

A Low Power 4th Order Low Pass Gm-C Filter in 130nm CMOS

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Abstract: A Low Voltage, Low Power 4th order Gm-C Elliptic filter is proposed in this paper. For supply voltage of 1.4V, the Operational Transconductance Amplifier is designed to dissipate low Power of 1.4mW. The two stage fully differential Operational Transconductance Amplifier is designed in 130nm CMOS technology for high linearity and large Output Voltage swing. The Filter is designed using Mentor Graphics tools and the simulation for an input voltage of 150mV (PP), a Total Harmonic Distortion of less than -60dB is achieved.

Keywords: Transconductance, Elliptic Filter, Biquad, Harmonic distortion, Common Mode Feedback, Continuous Time, Voltage Swing.

I. INTRODUCTION

Two Methods of filtering technique are widely used in most of the applications, Switched capacitor filter and Continuous Time filter. The former has the advantage of accurate corner frequency; however, it has issues such as aliasing, trade-off in choosing sample rate, effects of sample and hold circuit and noise [1]. This has led to the design complexity of these filters, Moreover the power consumption is more and occupies large silicon area. The later even though does not have accurate corner frequency; it can be designed for a wider dynamic range. Gm-C filter is one of the popular continuous time filters which is widely used in both higher frequency range applications of up to 2GHz and Low frequency range applications from 0.1 Hz. Applications such as WiMax, Hand held devices, Sensor's readout circuit, Medical signal conditioning, Seismic and other Wireless Communications are attracted towards these filters.

One of the major challenge in designing the Gm-C filter in Deep Submicron technology is the short channel effects [2], [3], this can cause non linearity, ways to reduce this nonlinearity must be found. Also there is a variation in cut-off frequency due to temperature and supply voltage variations. Even though Gm-C filters are preferred for their ease of full integration on chip capability; their power dissipation is very high. In most of the previous work, in order to reduce the power consumption, supply voltages are reduced and the transistors are scaled down, however these filters designed

with Operational Transconductance Amplifier provides only maximum of 400mV Output Voltage swing. This is due to the increase in overdrive voltage of the transistors. This paper proposes a design which overcomes all these limitations with low noise.

The paper is organized as, in section II the design of OTA is discussed, in section III the Overall design of the Elliptic Filter topology is described and in section IV Simulation results are proved.

II. OTA DESIGN

In most of the design where filter's attenuation is critical, the Transconductance of the OTA must be designed carefully so that it must not affect the gain provided by the previous stage [4]. To maintain the gain of the previous Transconductance stage of the filter, it is important to maintain a proper biasing current. The biasing current will decide the gm of the particular stage.

There is a trade-off between biasing current and the output voltage swing. As the biasing current is chosen appropriately to obtain a proper gm, overdrive voltage increases as they are inversely proportional and hence the output voltage swing decreases. A two stage fully differential OTA is designed in this paper to achieve an output voltage swing of 600mV. Also in Deep Submicron technology to reduce the second order effects, the aspect ratio of the transistors must be designed appropriately. The design of OTA with Common mode feedback circuit is shown in Figure 1[4].

Transistors Q1 to Q6 forms the fully differential first stage of the OTA, Q1 and Q2 are the input transistors and has diode connected loads Q5 & Q6. Cascoded load is avoided so that there will be sufficient headroom for the desired output swing. The bias current for this stage is provided by transistors Q3 & Q4. A bias circuit was also designed with NMOS transistors as a current source and PMOS as current mirror circuit, so that the design will have robustness to corner frequency variation because of temperature and power supply variations.

The Biasing Circuit in Figure 3 is designed to bias the OTA. Transistor Q21 acts as a current source and the drain current of Q21 is copied and scaled by Q23 & Q27; the drain outputs of these transistor provides stable biasing current and their drain voltages Vb1 and Vb2 biases the OTA transistors Q3, Q4 and Q13, Q14 respectively. Transistors Q24 – Q27 are designed as a cascode current source to scale down the biasing voltage to obtain V_{ref} , which is the Common mode reference voltage to the CMFB Circuit.

III. FILTER DESIGN

Elliptic filters are important in applications requiring sharp magnitude response. They are preferred in wireless communication and sensor readout circuit because their ripples are divided in both pass band and stop band unlike Chebyshev filter. Biquad Circuit has the advantage of ease in cascaded design; hence a Biquad structure is used as the first stage [6],[7].

The Topology of the 4th order elliptic filter is shown in figure 4. Three Transconductance gm_1 , gm_2 and gm_3 with C_1 and C_2 , forms the second order Biquad structure [6],[7]. This Biquad structure is preferred for its low power consumption unlike the Biquad in [4]. Two first order filters are cascaded in the later stages instead of cascading Biquad, thus further reducing the area and power requirement. Transconductance gm_4 and gm_5 is a first order structure with negative resistance load which improves the Output impedance, the passive resistance in [6] is replaced by an active resistance thus improving the impedance by keeping the attenuation low. Another advantage of using the active resistance is, during design the gm can be varied for the desired resistance without affecting the gain and cut-off frequency. The third stage is a lossless fully differential Integrator which will introduce a further 20dB/decade roll-off.

The Transfer function of the second order Biquad Structure is given by

$$H_2(s) = \frac{K\omega^2}{s^2 + \omega/Qs + \omega^2} \quad (2)$$

Where,

$$K = \frac{gm_1}{gm_3} \quad (3)$$

$$\omega_o = \frac{\sqrt{gm_3 gm_2}}{C_1 C_2} \quad (4)$$

$$Q = \sqrt{\frac{C_1}{C_2} \times gm_3 gm_2} \quad (5)$$

The transfer function of the first order section with negative resistance is given by

$$H_1(s) = \frac{gm_4 \times 1/gm_5}{1 + sC_3/gm_5} \quad (6)$$

The Transfer function of lossless Integrator is given by

$$H_o(s) = \frac{gm_6}{sC_4} \quad (7)$$

Transconductance gm_6 is varied to compensate for the attenuation caused by the previous stages. One of the Major advantages of using a gm-C filter is it has a wider bandwidth [8].

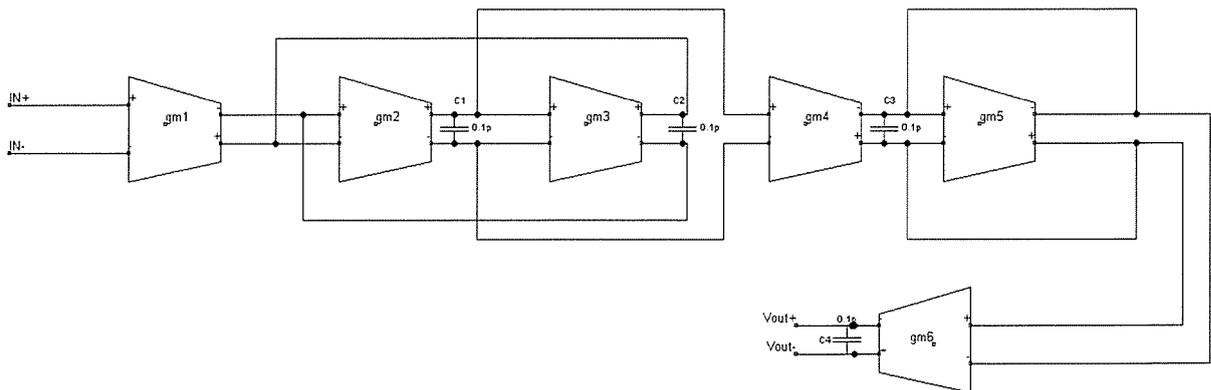


Figure 4. Fourth Order Elliptic Filter Topology

Gm-C filter has excellent gain-bandwidth properties and cascading these structures is quite simple and easy. In this design the passive elements are replaced by their active counterpart, which will give lower sensitivity due to component variations [9].

IV. SIMULATION RESULTS

Mentor Graphics tool is used to design the filter in 130nm CMOS technology. Making use of the advantage of fully differential amplifier, the short channel effects and the noise is reduced.

A larger cut-off frequency of 22 MHz with high linearity is obtained by appropriately designing the OTA. Phase response in figure 5 shows that the filter is linear throughout the wider cut off frequency of 22MHz. Even if the cut-off frequency is increased by altering the value of the capacitance in the design, it is found that the filter’s response is still linear up to GHz range. The supply Voltage of 1.4V is used and the power consumption is reduced to 1.4mW. The Filter design has a Total Harmonic Distortion of -60dB for an input voltage of 150mV. The Transconductance of the OTA is adjusted to get a fully differential Output Voltage swing of 600mV Peak to Peak. The complete simulation results are listed in table1 below.

V. CONCLUSION

The Low power 4th order gm-C filter has been designed to overcome limitations such as high Power Consumption, non linearity, and low output Voltage swing. The fully differential OTA in 130nm CMOS technology has also been designed in 1.4V supply voltage with CMFB. The simulation result shows a roll-off of 80dB/decade and high linearity of the filter for a wider frequency bandwidth. The Total Harmonic Distortion observed for a differential input voltage of 150mV peak to peak is -60dB, which is less than 1%.

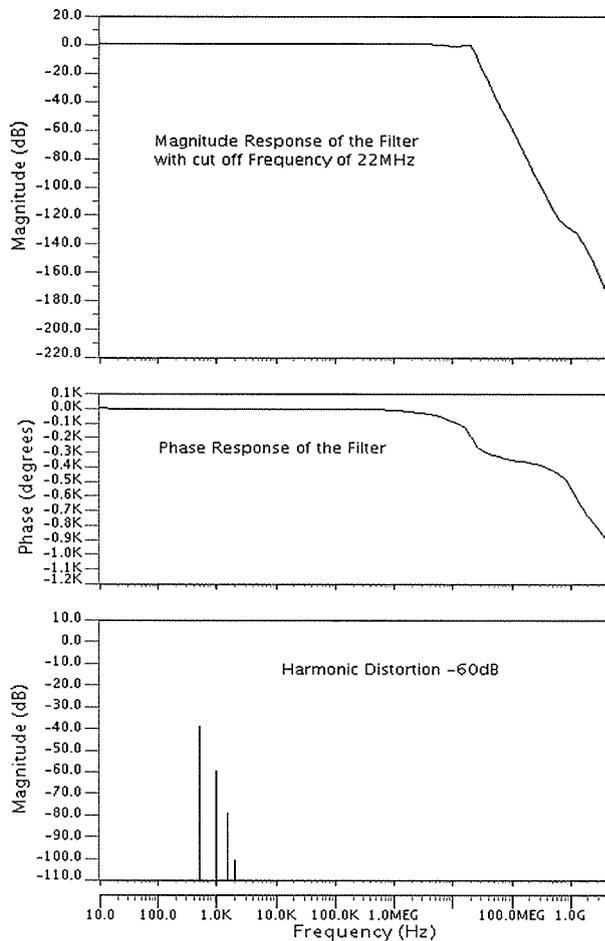


Figure 5. Simulation Output of Magnitude, Phase response & Harmonic distortion

Furthermore, fully differential amplifier design can also suppress even order harmonics and increase output voltage swing [10] – [12], which is most appropriate for the 4th order filter design. Thus as shown in Figure 5 the magnitude response of the filter having a roll off of 80db/decade is achieved well with the use of the proposed gm-C topology.

TABLE 1 SIMULATION RESULTS

| | |
|---|--------------------------------|
| Technology | 130 nm CMOS |
| Supply Voltage | 1.4 Volts |
| Filter type | 4 th Order Elliptic |
| Power Consumption | 1.4mW |
| THD(@150mV) | -60dB |
| Output voltage swing (fully differential) | 600mV (P-P) |
| Current Consumption (static) | 0.7mA |
| No. of gm-C unit | 6 |
| Total On chip Capacitance | 0.4pf |
| Cut off Frequency of the Filter | 22MHz |
| Total no. of Transistors per OTA | 20 |
| Area of the Filter in Layout | 0.5mm ² |

TABLE 2 COMPARISONS OF DIFFERENT FILTER DESIGNS

| References | Filter Parameters | | | | | |
|------------|-------------------|----------------|--------------------------------|-------------------|-----------------|------------------------------------|
| | Technology | Supply Voltage | Filter Type | Power Consumption | THD@150mV input | Output Voltage Swing (fully diff.) |
| [4] | 65nm CMOS | 1.8V | 5th Order Bessel | 21.6mW | -40dB | 400mV |
| [5] | 180nm TSMC CMOS | 1.8V | 5 th Order FLF | 67mW | -40dB | 400mV |
| [6] | 120nm CMOS | 1.5mV | 3 rd Order | 14.25mW | -49dB | 400mV |
| [10] | 90nm CMOS | 0.9V | 5 th Order Elliptic | 1.5mW | -66dB | 300mV |
| [11] | 180nm CMOS | 1.8V | 2 nd Order | 8.1mW | -40dB | 450mV |
| [12] | 0.35um CMOS | 1.0V | 1 st Order | 005nW | -40.3dB | |
| This Work | 130 nm IBM CMOS | 1.4 Volts | 4 th Order Elliptic | 1.4mW | -60dB | 600mV |

The Parameters of various filter designs are compared in Table 2 and it is evident that this work has contributed an overall best filter design with a very good Output voltage swing and minimum Power consumption.

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A CMOS Integrated MEMS Capacitive Pressure Sensor design in a 3D SiGeMEMS Process

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Abstract- A novel CMOS integrated Micro-Electro-Mechanical capacitive pressure sensor in SiGeMEMS (Silicon Germanium Micro-Electro-Mechanical System) process is designed and analyzed. Excellent mechanical stress-strain behavior of Polycrystalline Silicon Germanium (Poly-SiGe) is utilized effectively in this MEMS design to characterize the structure of the pressure sensor diaphragm element. The edge clamped elliptic structured diaphragm uses semi-major axis clamp springs to yield high sensitivity, large dynamic range and good linearity. Integrated on-chip signal conditioning circuit in 0.18 μ m TSMC CMOS technology (forming the host substrate base for the SiGe MEMS) is also implemented to achieve a high gain of 100.5dB for the MEMS sensor. A high sensitivity of 4.65mV/V/hPa, with a non linearity of less than 1% for the full scale range of applied pressure load is achieved. The diaphragm with a wide dynamic range of 10hPa – 1000hPa stacked on top of the CMOS circuitry, effectively reduces the combined sensor+conditioning implementation area of the intelligent sensor chip.

Keywords: Poly SiGe, Microstructure, Bondpad, Stress, Strain CMOS, Perforation, TSMC, Chopper stabilization.

I. INTRODUCTION

Integration of micro-structure devices with signal conditioning circuit has been in tremendous research interest for the past few years. Significant improvement in the performance of the sensing and actuation system has greatly influenced this growth in prototype development of on-chip sensors and actuators. However, their production and utilization is still in the budding stage. Micro-Pressure sensors have been in great demand in numerous fields such as Bio-medical, Automobile, Industrial safety, Aeronautics etc. for the past few decades. Capacitive and Piezoresistive transduction are the two well known techniques of commercialized pressure sensor implementation [1]. Ease of fabrication steps and insensitivity to temperature variation as well as environmental effects have made the capacitive sensing principle more preferable over the Piezoresistive implementation. However, parasitic effects result in significant degradation of the capacitive sensing, hence it requires on-chip readout and conditioning circuitry for performance enhancement [2].

Efforts in the hybrid Integration of sensor devices and associated conditioning circuitry in a single package has

mostly resulted in poor performance of the sensing system due to the serious issues of nonlinearity, unreliability and environmental degradation. Even though monolithic integration usually has a longer time to market compared to hybrid systems; it offers lower overall production and packaging cost [3]. The unique monolithic integration of SiGe MEMS sensor device on top of the CMOS (Complementary Metal Oxide Semiconductor) circuit (also forming the host substrate for the SiGeMEMS) in this CMOS integrated SiGeMEMS process (Silicon Germanium Micro-electro-mechanical System) has immensely miniaturized the proposed

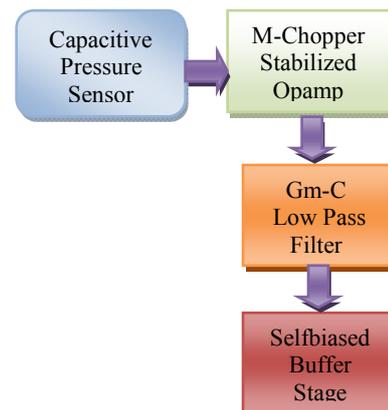


Figure 1. System Block Diagram.

pressure sensor system. The low temperature material properties of polycrystalline SiGe enables the post processing of the sensor devices on top of the CMOS circuit.

Different diaphragm shapes and structures with varied dimensions and thickness have been in research for the past decade for improving the overall system performance parameters such as sensitivity, linearity and dynamic range [1]-[4]. Reduced thickness in the diaphragm has yielded improved sensitivity, however, the trade-off have been poor linearity [2]. This proposed design has focused to overcome this sensitivity-linearity trade-off. The system block diagram of this integrated sensor is shown in Fig. 1. The low amplitude weak noisy sensor signal is amplified utilizing a significantly low-noise modified chopper-stabilized Opamp (operational amplifier). The high frequency chopper residuals (artifacts)

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are filtered out by the steep roll off Gm-C filter. The filter is followed by a self-biased buffer output stage which can drive an off chip load of up to 15pF. The design target for the edge clamped elliptic diaphragm structure is to achieve wider dynamic range, without compromising sensitivity and linearity. In order to achieve this performance, clamp type spring is utilized as shown in Fig. 2 which has not been reported before.

This paper is organized as follows: In section II, the structural and fabrication aspects of the micro-sensor is described, in section III, the detailed description of the requirements and the design analysis of the on chip signal conditioning circuit is explained, while in section IV, the model analysis and study of the integrated system characteristics is provided. Finally concluding remarks are presented in section V.

II. DESIGN AND CHARACTERIZATION OF SENSOR DEVICE

The capacitive sensing technique which is an inherently less noisy transduction mechanism is also a relatively simple method that uses either a varying displacement or a varying parallel-plate surface-area principle to pick up the desired physical quantity. Although this technique is less resilient to harsh environment compared to its piezoresistive counterpart; proper structural design can contribute to a relatively lower hysteresis and greater stability as a distinct advantage.

A. Theory

The elliptic structured diaphragm of the capacitive pressure sensor is designed with copious planar perforations in order to achieve better linearity. Clamping only at the semi-major axis edges using clamp springs enables better low pressure sensitivity compared to an all edge clamped sensor structure. As vertical pressure is applied on the diaphragm the separation between the diaphragm and the bottom electrode varies yielding a fluctuation in the capacitance. Ignoring the fringe electrostatic field, the capacitance variation is governed by [4],

$$C = \frac{\epsilon_r \epsilon_0 A}{d} \quad (1)$$

Where, ϵ_r is relative permittivity of the dielectric material, ϵ_0 is the permittivity of free space, A is the cross-sectional area of the diaphragm and d is the separation between the electrodes/plates. Under the influence of applied pressure, the diaphragm deforms due to the distributed stress and strain. The edge clamping using the clamp spring causes the diaphragm to deflect in a non uniform manner. As a result the change in distance between the diaphragm and the bottom electrode is not uniform throughout the cross-section, and hence (1) must be obtained by integration over the 2D distance between the electrodes, which can be written as [4],

$$C = \iint [\epsilon_0 / \{d_0 - D(x, y)\}] dx dy \quad (2)$$

Where d_0 is the distance between the plates at zero pressure and $D(x, y)$ is the incremental change in the distance

after deflection. The effective plate deflection for an elliptic diaphragm can be expressed as,

$$W = (1 / \pi.r1.r2) \iint D(x, y) dx dy \quad (3)$$

Where, $r1$ and $r2$ are respectively the radii of the semi-minor and semi-major axis, while the effective deflection W in the z direction is integrated over the entire area of the elliptic diaphragm. The diaphragm thickness is very small compared to the other dimensions, hence assumption of Kirchoff's hypothesis [5] is considered in the analysis of the deflection. Furthermore, the displacement will usually be around half the thickness of the diaphragm, therefore, 2D plane stress analysis of thin plates is best suited in this design. The stress tensor components σ_z , σ_{xz} and σ_{yz} becomes null and the stress

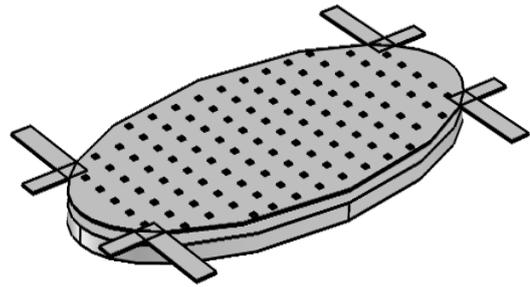


Figure 2. Perforated elliptic diaphragm, clamped at the semi-major axis using clamp springs.

tensor matrix reduces to [5],

$$\sigma = \begin{bmatrix} \sigma_x \\ \sigma_y \\ \sigma_{xy} \end{bmatrix} \quad (4)$$

Assuming the diaphragm material to be isotropic, its stress-strain behavior can be considered to be linear within the range of its elastic limit. This stress-strain linearity assumption up to the elastic limit is based on the Hook's law and can be given by [5],

$$\sigma = E \epsilon \quad (5)$$

Where, σ , is the stress due to the applied pressure, ϵ the strain due to stress and E the modulus of elasticity. Elliptical structure can be viewed as a circle pulled along the opposite sides to be stretched, hence the radius in that direction increases (becomes the semi-major axis), however the area remains unchanged. The deflection, stress and strain analysis is assumed to be similar to that of an edge clamped circular structure.

B. Structural description and fabrication

An elliptical structured diaphragm using PolySiGe material of spatial dimensions $100\mu\text{m} \times 250\mu\text{m}$ and thickness of $4\mu\text{m}$, is clamped at the semi-major axis for curvilinear

deformation of the entire diaphragm at low pressure loads. On the contrary, the deflection of all edge clamped diaphragm at very low applied pressure, is almost negligible yielding poor sensitivity and low dynamic range [3]. This low pressure sensitive microstructure is fabricated on top of the CMOS conditioning circuit used to improve the strength of the sensed signal. The weak signal from the sensor is otherwise degraded due to the RC transmission line effect of the long interconnect metal wires from the microstructure to the CMOS circuit. The low thermal variation of poly SiGe material used for the MEMS sensor structure offers minimal drift in the performances of the underlying CMOS transistors of the conditioning circuit. The interconnection of microstructure and CMOS circuit is through low resistive poly-SiGe vias. The top aluminum metal layer of the CMOS process is used to connect the electrodes of the capacitive MEMS sensor to the bond-pad for test access. The electrical isolation between the MEMS structure and the CMOS circuits is achieved through a 400nm thick silicon carbide (SiC) layer. Poly-SiGe anchors of height 3 μ m and width 0.8 μ m firmly fixes the clamp spring at the edges of elliptic diaphragm along the semi-major axis. The clamp spring overrides the necessity of reducing the thickness of the structure, thus overcoming the sensitivity and linearity trade-off. Various arrays of anchors are used for obtaining specific bending moments at the edges of the diaphragm that can withstand a specified pressure range. As the anchors are semiconductive, precautions are taken in designing the bottom electrode to avoid possible leakage and/or short circuit.

The oxide sacrificial layer (replaced by air-gap dielectric) is etched out through the top-side perforations of the diaphragm, using them as the structure release holes/vias. The dimension of the release holes are 10 μ m X 10 μ m and are spaced 10 μ m apart throughout the entire diaphragm plane, which as a consequence results in relatively less deflection in the high pressure ranges. The displacement of the diaphragm is 2 μ m for an applied pressure of 1000hPa, which is half the thickness of the diaphragm. The narrow 3 μ m separation between the two plates (determined by the process constrained width of the oxide sacrificial layer) limits the dynamic range of the sensor, and as a consequence further thin plate analysis assumption also does not permit larger deflections (beyond the 2 μ m range in this case). Generally, deflection beyond half the diaphragm thickness can lead to short circuit/leakage due to pull in voltage [6], however, the perforated elliptic design reduces the pull in voltage substantially due to lower surface-area of the capacitance, thus providing further improvement in the linearity and dynamic range of the MEMS sensor. The analysis revealed that deflection of up to 2.2 μ m does not deteriorate the sensor performance. The deflection of the elliptic diaphragm in thin plate analysis can be easily developed by modifying the analysis for circular diaphragm in [5] as follows,

$$w = [S_o / 64Dr_2^2](r_2^4 - r^2r_2^2) \quad (6)$$

Where, S_o is the applied pressure, r_2 is the length of the semi-major axis, r is the polar coordinate and D is the flexural rigidity. The deflection of the diaphragm increases with an

increase in the length of the major axis (r_2) of the elliptic diaphragm. The maximum deflection is at the center of the diaphragm and is determined as follows [7] :

$$w = Sor_2^4 / 64D \quad (7)$$

Also, the flexural rigidity, D is given by [8],

$$D = Et^3 / 12(1 - \nu^2) \quad (8)$$

Where, t and ν are thickness of the diaphragm and Poisson's ratio respectively. Substituting (8) into (7), the deflection of the plate can be given by

$$w = (r_2^4 / t^3) \{ \{ 3S_o(1 - \nu^2) \} / 16E \} \quad (9)$$

From (9) it is evident that the ratio between the length of the semi-major axis and the elliptic diaphragm thickness directly influences the deflection at the center of the diaphragm. Thin diaphragms can deflect more yielding good sensitivity, however linearity is penalized, hence more importance was given to the characterization of the radial dimensions of the diaphragm, r_1 and r_2 . Poly-SiGe material having low modulus of elasticity of around 130Gpa [9] gives increased deflection at a very low applied pressure of 100Pa. This offers the advantage of low minimum detectable pressure, thus increasing the dynamic range of the sensor. For the same surface area, the elliptic diaphragm deflects more under a very low applied pressure compared to the circular diaphragm structure.

III. READ OUT CIRCUIT DESIGN

The On chip sensor interface circuit is a crucial component that converts low-level transduced sensor outputs to useful electronic signals with low noise factor [10]. The weak sensor signal poses a significant challenge in designing a comprehensive frontend circuit. The overall performance of the sensor module largely depends on the readout circuit design. The circuit performance parameters that are targeted for enhancement are high gain, low noise, low power, reduced area and high linearity. The three main circuit components involved are Modified Chopper stabilized Opamp, Gm-C low pass filter and self biased buffer stage. Design using the 0.18 μ m CMOS deep submicron technology enables higher speed of analog circuits but makes high gain OTA design more challenging. Accuracy and linearity is deteriorated due to associated low voltage constraints. Further, the low supply voltage constraint results in limited input common mode range that degrades the opamp performance over the input range [11]. The proposed high gain two stage opamp design for the readout circuit utilizes gain enhanced folded cascode as the first stage. The composite gain enhancement is achieved by controlling the gain A_c of the doubly g_m -boosted cascode. If g_{mFC} is the overall transconductance of the folded cascode amplifier, and g_m the input stage transconductance, then,

$g_{mFC} = g_m(1+A_c)$ [12]. The negative feedback utilized in the doubly g_m -boosting cascode stage elevates the output impedance leading to gain enhancement. The proposed FC (Folded Cascode) Opamp yields a higher gain-bandwidth product (GBW) than the conventional folded cascode structure, without increasing the power budget. Stacked PMOS devices are utilized as the input stage of the FC opamp to further enhance the transconductance. The noise injected by these PMOS devices is an order of magnitude lower than the NMOS devices, and hence a relatively low input referred noise is achieved at the input stage [11]. The proposed two stage fully differential operational amplifier shown in Fig. 3 provides large output voltage swing and is less susceptible to common-mode noise compared to the single-ended version. The total input referred noise of the FC Opamp can be approximately derived as,

$$\overline{V^2}_{in_{tot}} = 8KT \left(\frac{2}{3g_{m1,2}} + \frac{2}{3} \cdot \frac{g_{m5,6}}{g_{m1,2}^2} + \frac{2}{3} \cdot \frac{g_{m9,10}}{g_{m1,2}^2} \right) + \left[\frac{2K_p}{(WL)_{1,2} \cdot C_{ox} \cdot f} + \frac{2K_N}{(WL)_{5,6} \cdot C_{ox} \cdot f} \cdot \frac{g_{m5,6}^2}{g_{m1,2}^2} + \frac{2K_p}{(WL)_{9,10} \cdot C_{ox} \cdot f} \cdot \frac{g_{m9,10}^2}{g_{m1,2}^2} \right] \quad (10)$$

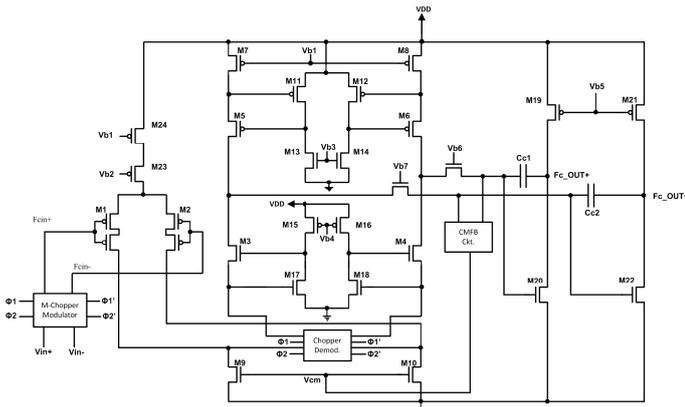


Figure 3. Modified Chopper Folded Cascode Opamp.

Thermal and flicker noise are the dominant factors that increase the noise floor of the FC opamp. Two methods were employed to reduce the overall noise, g_m of the input transistors is appropriately increased to reduce the thermal and flicker noise and g_m of the current sources is kept somewhat low to reduce noise while not minimizing I_D (in order to maintain reasonable slew rate). Reduction in g_m of the current sources reduces the output impedance resulting in reduction of the voltage gain, hence, a careful overall gain-noise design trade-off is necessary. The composite design of the fully differential chopper stabilization within the folded cascode opamp structure enables output precision and significant noise reduction, thereby increasing the sensitivity of the opamp. The conventional chopper introduces random spikes at the output causing a residual offset of up to $500\text{nv}/\sqrt{\text{Hz}}$, which is

significantly high for precision sensor application. Modified Chopper technique which utilizes a transmission gate block (as shown in Fig. 4) to modulate the input signal, introduces negligible spikes when demodulated. In addition, using complementary PMOS choppers, and employing two different chopping frequencies makes it feasible to reduce the residual offset to the range of $100\text{nv}/\sqrt{\text{Hz}}$. The theoretically achievable improvement in residual offset is the ratio of $f_{\text{chophigh}} (\Phi_2)$ and $f_{\text{choplowlow}} (\Phi_1)$ [11]. Furthermore, the gain accuracy of the modified chopper is found to be quite high. The differential transmission gate chopping network operating with in phase and out of phase chopping frequencies is shown in Fig. 4.

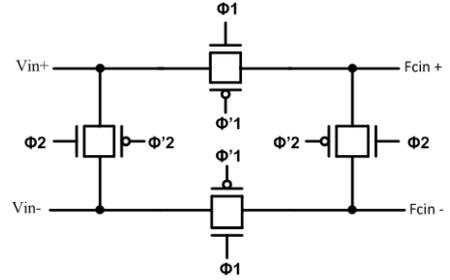


Figure 4. Modified chopper network.

The stability and frequency compensation of the signal conditioning circuit is analyzed to find the location of poles and zeros introduced by the parasitic capacitance at different stages. Pole zero doublet introduced by the gain booster degrades the transient response of the opamp. This doublet appears as a slow exponential term in the step response increasing the settling time of the opamp. In order to make the transient response behavior similar to that of a single pole system, the zero, ω_z must be pushed to a higher frequency by increasing the drain current of the g_m boosting stage. The g_m of this stage is appropriately varied to split the pole into a complex conjugate pair [16], thus eliminating the slow response introduced by this stage. Pole splitting achieved by miller compensation provides stability to a two stage opamp [13], however it introduces RHP zero. Increasing the impedance in the feed-forward path pushes the RHP zero to a higher frequency, thereby increasing the stability [14]. Hence an NMOS transistor biased in the triode region, in series with the compensation capacitor is used to yield an improvement in stability over the conventional miller compensation technique. Proper choice of the coupling capacitor, C_c enables the under damping of the oscillation by setting the phase margin above 45° . However, the increased phase margin causes bandwidth limitations, and hence, a careful bandwidth-stability trade-off is required. Differential difference amplifier (DDA) common mode feedback is employed in the design to set the common mode output of the opamp in order to achieve large output swing [14]. The required output voltage swing is achieved using the common source (CS) second stage which provides additional gain to improve the overall gain of the opamp. Simulation results indicate that a gain of 105dB along with 64° of phase margin and $100\text{nv}/\sqrt{\text{Hz}}$ input referred noise is achieved by the designed opamp. A wide unity gain bandwidth of 200MHz which is sufficient for the pressure sensor duty cycle is also achieved in this design.

The compensation capacitors effectively shorts the CS stage NMOS amplifying devices into diode-connected loads for high frequency chopper residuals, thus suppressing these artifacts compared to the sensed pressure signal. However, simulations indicate that a better roll-off low-pass filter is inevitable to completely remove the chopping frequency. Gm-C filters provide better roll-off behavior even with lower order structures, and is well-suited for sensor signal conditioning. A 4th order low-pass Gm-C filter is thus implemented at the output of the chopper stabilized opamp. An active resistance is employed in the final transconductance stage of the filter in order to reduce attenuation, and hence, low attenuation of -3dB is achieved for this filter design.

Generally, the sensor readout circuit has to drive an off chip analog-to-digital converter (ADC) circuit for display or actuation purpose. The high output impedance of the opamp together with the low pass filter is not suited to drive these off-chip end-user devices, and hence a low output impedance buffer driver circuit is required without degrading the linearity. Although simple unity-gain buffers can be realized using source followers, they are limited by nonzero offset and nonlinearity. Nonlinearity can be reduced by employing negative feedback but gate-to-source voltage drop of the source follower still introduces offset [15]. Current feedback can be employed to significantly reduce the output impedance without the need for increased device aspect ratios, so that a reduction in the overall area and power consumption is realized. A self biased two stage source follower is designed using this technique which can drive a load of up to 15 pF.

IV. SIMULATION RESULTS

Finite Element analysis was carried out in COMSOL Multiphysics for optimizing the dimensions of the elliptic diaphragm. Two important characteristics were targeted in this analysis. Firstly, to study the variation of capacitance with the applied pressure and secondly, to observe the displacement that causes the change in capacitance for the entire load sweep. The later is critical in studying the linearity of the device as linearly elastic material model assumptions were used to characterize the sensor. Solid Mechanics analysis was utilized to study the displacement of the membrane for the load pressure applied.

For the parametric pressure sweep load from 10hPa to 1000hPa in steps of 10hPa, the displacement varied from 0.09234 μ m to 2.05 μ m. Moving mesh physical model was assigned for the dielectric layer between the top and bottom solid mechanics model in order to extract the varying capacitance under the applied pressure. Electrostatic physical analysis was then carried out to pick up the surface capacitance and the instantaneous capacitance. For the bias voltage of 1.4V, the capacitance varies from 0.0954pf to 0.2798pf due to the deflection of the membrane, under pressure load from 100Pa to 1000hPa. The sensitivity of the sensor is calculated to be 4.786Ff/hPa. Figs. 5 to 7 depicts the various sensor characteristics in terms of deflection, capacitance linearity and displacement performances respectively. The results indicate improved performances in terms of dynamic range, minimum detectable pressure and diaphragm elastic limit.

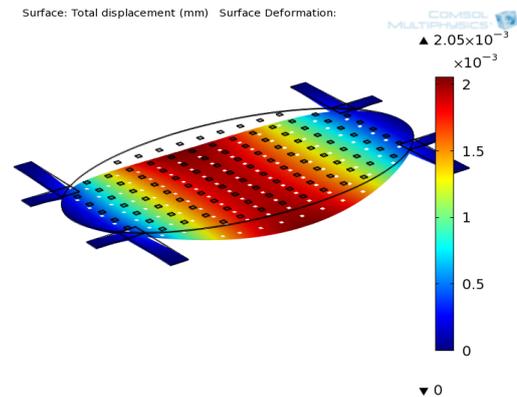


Figure 5. Deflection analysis of perforated diaphragm.

Design and analysis of CMOS signal conditioning circuit in 0.18 μ m CMOS TSMC technology is carried out utilizing Tanner tools. The folded cascode opamp with the modified input stage and double g_m -boosting provided an increased transconductance. The single ended closed loop opamp gain was found to be 96.77 dB and the overall gain of the sensing circuit was 94.5 dB at the buffer output, as seen in Fig. 8. The closed loop gain for the fully differential configuration was calculated to be 100.5dB. A phase margin of 64 $^\circ$ was achieved which proves that the operational amplifier is stable despite the significant increase in the open loop gain.

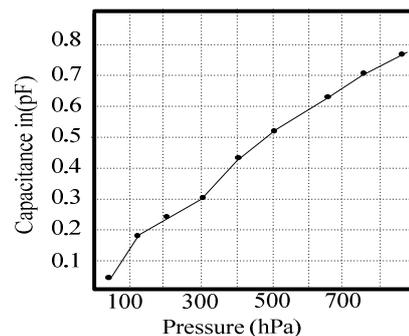


Figure 6. Capacitance Variation with applied Pressure

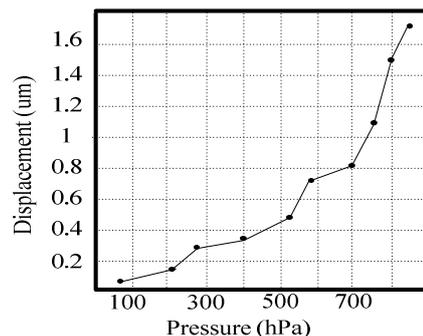


Figure 7. Displacement variations for applied pressure.

The modified transmission gate chopper using 10kHz and 100kHz chopping frequencies (assuming 1/f noise corner frequency at 1kHz) offered lower spikes compared to conventional chopping as shown in Fig. 9 (lower plot) when

excited with a sinusoidal input signal. A high overall sensitivity of 4.765mV/V/hPa is achieved for the integrated sensor system.

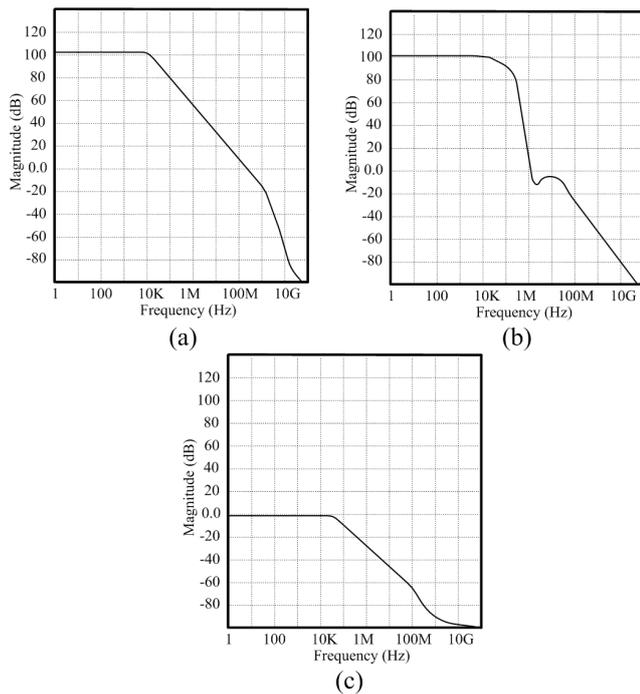


Figure 8. AC Analysis of (a) M-Chopper FC Opamp, (b) Gm-C low-pass filter and (c) Self-biased buffer.

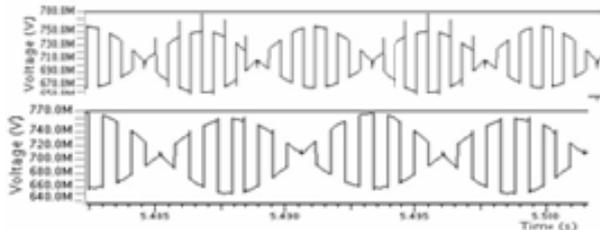


Figure 9. Modulated input signal by Conventional and Modified chopper showing less spikes.

V. CONCLUSION

A highly sensitive integrated capacitive pressure sensor is designed and characterized with a 0.6 μm feature size; the on-chip signal conditioning circuitry is designed in 0.18 μm TSMC CMOS technology. The capacitive pressure sensor is analyzed under a range of pressure loads. The novel perforated elliptic diaphragm, clamped at the semi-major axis yielded a wider dynamic range. Clamp spring designed to edge clamp the diaphragm increased the sensitivity significantly without degrading the linearity performance. High gain sensing circuit is designed to cater for the low-voltage and weak output signal of the sensor. Simulation of the CMOS circuit is carried out by sinusoidal excitation at the input stage. Non linearity of less than 1% is achieved for the full scale range of applied pressure. This integrated pressure sensor, based on the observed

performance characteristics, if appropriately packaged, can be used for biomedical applications such as catheter pressure monitoring and intraocular pressure measurement.

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Multi - Recycled Folded Cascode Amplifier for Sensor Readout

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Abstract- The requirement of high gain and low noise amplifier for sensor readout is addressed in this paper. Current cross mirroring technique is employed in this work to enhance the transconductance by a factor that depends on the value of current mirroring ratio F&H of the input current mirrors of the folded cascode operational amplifier. The input differential pair transistors are split for achieving increased gain without compromising unity gain bandwidth. The increased bias current due to the increased transconductance has yielded a better slew rate and thereby faster settling time. Simulation results for the 130nm IBM CMOS technology designed amplifier showed a gain of 86.4dB for the single stage fully differential multi recycled folded cascode amplifier. A larger open loop bandwidth of 210MHz is achieved for an 85.2° degree phase margin. The input referred noise level is also lowered to 48.3 μ Vrms.

Keywords: Recycled Folded Cascode Opamp, Transmission gate Chopper Stabilization, Transconductance, Current Cross Mirroring, Slew Rate, Settling Time, Unity Gain Bandwidth.

I. INTRODUCTION

Operational Transconductance Amplifier remains the better choice for sensing technology over the decades due to its high gain. Telescopic & Folded cascode topologies became the major building block for various CMOS amplifier stages, former suffers from serious issue of low voltage swing, hence Folded Cascode is preferred. The inherent advantages such as low flicker noise, low common mode and higher non dominant poles, made PMOS transistors more appropriate as input stages [1]. Many works were reported for improving and enhancing the performances of this folded cascade opamp [1]-[4], however power budget was significantly high. Unity Gain bandwidth is also compensated by scaling down the input & the driving transistors in [1]. Multistage amplifiers are widely used for sensor readout circuit for achieving higher amplification; however additional stages yielded additional noise and pole zero pairs, thus degrading the performances of the readout circuit. Switched Capacitor (SC) operational transconductance amplifiers are another alternative, but their aliasing issues are not suitable for low frequency pressure sensor application. Moreover in certain applications SC needs an output stage filters for eliminating the unwanted high frequency spikes.

The proposed design overcomes all these limitations. Improvement in transconductance by current cross mirroring in the input stages is done to significantly increase the gain. Transmission gate chopper stabilization circuit that provides negligible high frequency spikes is employed to reduce the input referred noise. Input & driving transistor's aspect

ratios are chosen appropriately for low power consumption without compromising bandwidth. The paper is organized as in section II the design and theoretical analysis of the proposed design is described. Section III details the implementation and results; the work is concluded in section IV.

II. DESIGN AND ANALYSIS

A. Circuit Design

It was demonstrated in [1] that gm of Recycled Folded Cascode (RFC) is improved by splitting the input transistors and recycling the current. Since the current flows through half the aspect ratio as compared to the usual input transistors, it experiences a high resistance path, which limits the current and hence the gm. Alternatively, a similar method with different topology is employed in this work which demonstrates that gm is increased without substantially limiting I_D , thereby the trade-off between output resistance of the input stages and their transconductance is compensated.

The proposed enhanced gm RFC is shown in Figure 1. The total aspect ratios of the input PMOS pairs do not exceed the aspect ratio of usual Folded Cascode input pairs. Thus gm is increased without compromising power. The aspect ratios of the four split input transistors are in the ratio P : Q : Q : P, where Q is kept very small so that negligible change in output resistance is obtained, hence I_D and thus gm is not affected. The bias current $2I_b$ that flows through the transistors M25 & M26 is divided by the aspect ratios of the input transistors by a factor of 3. Considering one half of the differential circuit, when all the input transistors are at saturation, current through M1c is mirrored with a ratio of H by transistors M3c & M4d. This increased current is again summed with the currents of transistors M2c & M1d and crossed mirrored with a ratio of F by transistors M3a & M3b. The output current that flows through the current summing network is given by $I_b/6 [FH+F-2]$. In this proposed design bias current and hence the transconductance increases 3 times if F&H are chosen to be 4. The transconductance in this design is found to be

$$Gm = gm_{1a} \left[\frac{FH + F(N+1)}{N} - 1 \right] \quad (1)$$

Even though the transistors are scaled down by splitting for the purpose of current cross mirroring, the transconductance is not reduced by half as in [1]. It can be shown that the bandwidth is also increased.

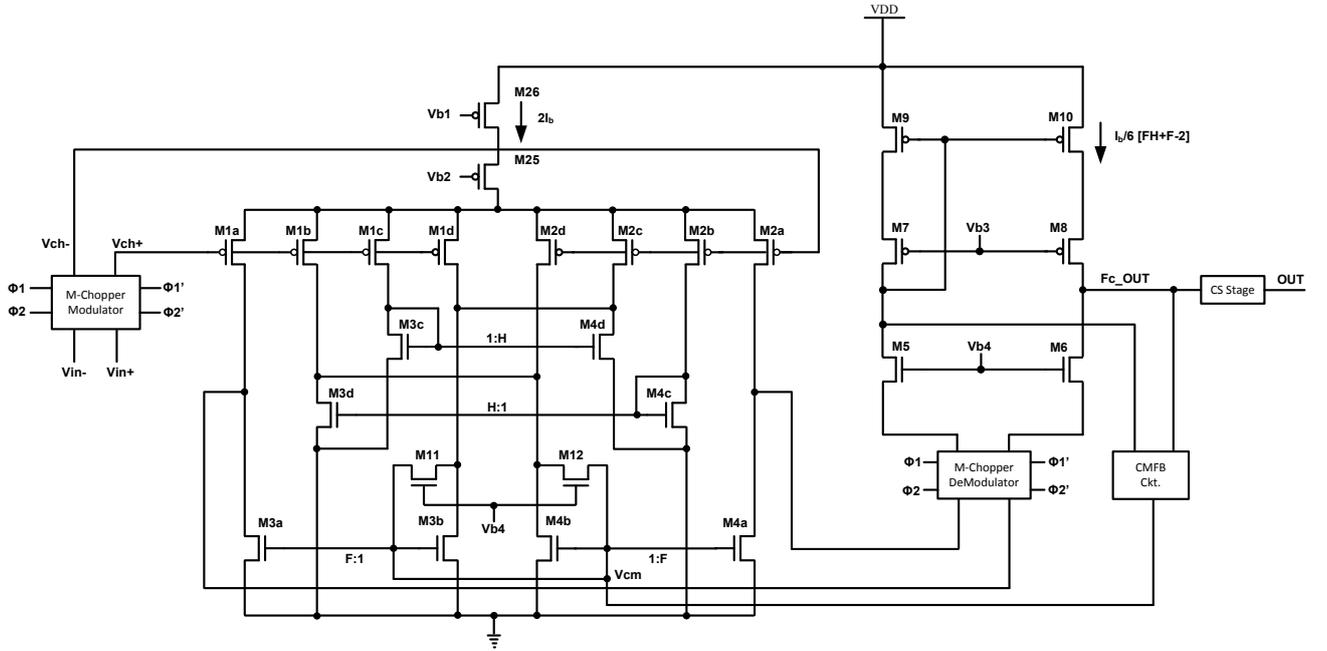


Figure 1. Proposed Multi Recycled Folded Cascode Opamp Amplifier.

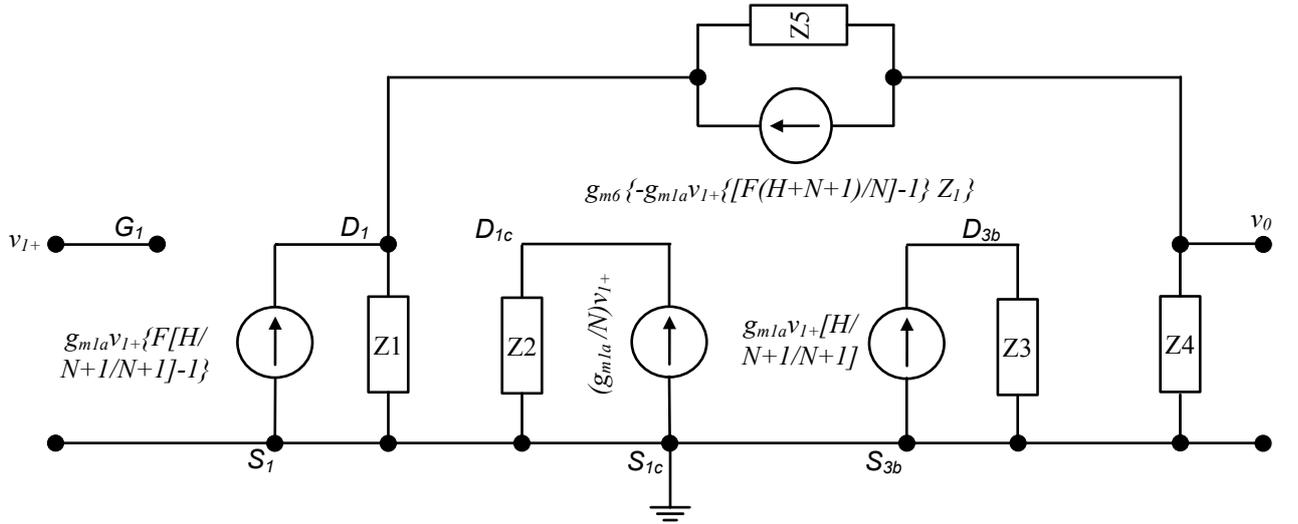


Figure 2. Small Signal Model Enhanced-gm Folded Cascode Operational Amplifier

B. Small Signal Gain

The complete Small signal model for half of the differential circuit is shown in Figure 2. The current sources and the impedances can be combined for simplification purpose. The small signal model is associated with two nodes a. and b., for this simple one stage amplifier. Using nodal analysis the simplified low frequency gain can be given by

$$\frac{V_o}{V_{I+}} = G_m \left[\frac{Z_4(1+1/g_{m6}Z_5) - Z_5(2+1/g_{m6}Z_1)}{(1+1/g_{m6}Z_1 + 1/g_{m6}Z_5)} \right] \quad (2)$$

Where \$Z_1\$ & \$Z_5\$ the small signal impedances can be given as

$$Z_1 = R_{o1} // R_{o3} \quad \& \quad Z_4 = R_{o8} // R_{o10} \quad (3)$$

$$Z_5 = R_{o6} // sC_{gs6} \quad (4)$$

An increase in the gain of 10dB is achieved when compared to [4]. From equation 2 it is evident that increasing impedances \$Z_4\$ & lowering \$Z_5\$ can significantly increases the gain, however considering the power dissipation and the current limitation, the aspect ratios of \$M_6, M_8, \& M_{10}\$ are marginally reduced. The low frequency output resistance can be given as

$$R_{out} = (g_{m6} + g_{mb6})(r_{ds}Z_1) // (g_{m8} + g_{mb8})r_{ds8}r_{ds10} \quad (5)$$

Where R_{01} , R_{03} & R_{06} are the output impedances of M_{1a} , M_{3a} & M_6 devices respectively. C_{gs6} is the parasitic effect of M_6 . G_m is the overall transconductance of the multi recycled folded cascode given in equation (1).

Even though the size of the input devices are kept larger than the current summing devices, the overall output impedance is compensated at the output stage. The chopper circuit being cross coupled switches is assumed to be closed for this AC analysis and their chopping frequencies are neglected as these higher frequencies can be filtered out at the output.

The reduction in the size of M_{1a} & M_{3a} has further increased the overall output resistance [1] & [2], thus providing an overall increase in gain of 12 to 14 dB for this single stage amplifier. Another advantage of this increased resistance is that it pushes the non-dominant pole to higher frequency yielding better phase margin and stability. Higher phase margin causes a better roll off in the gain curve beyond the low frequency dominant pole. Thus a significant improvement in unity gain bandwidth is achieved. Moreover the additional increase in the gain due to appropriate sizing of the device length provided better PSRR.

The critical parameter that directly affects the settling time and linearity apart from thermal effects is the slew rate. As the current I_B is mirrored from M_{1c} & M_{2b} by a factor of $(FH+F-2)/N$, the slew rate is increased by that same factor. Further the current at output transistors is further mirrored by the addition of current from M_{1a} ; the total enhancement in the slew rate can be given in terms of the bias current as

$$SR = \frac{[FH + F - 2]}{N} C_L I_B \quad (6)$$

Hence when F & H are 4 and N kept at the value 6, slew rate is increased more than one and a half times.

III. IMPLEMENTATION AND RESULT

The area and power constrain is very critical in the CMOS design of sensor circuit, hence the design is implemented in 130nm IBM CMOS technology. Scaling down the transistors for area minimization can result in low transconductance and hence low gain. The input differential stages consist of three pairs connected parallel on each half of the circuit. The transistors aspect ratios are P: Q: Q: P for the purpose of current cross mirroring. The transistor that is cross coupled from the other half of the differential pair is scaled down, as it just used for current mirroring rather than directly influencing the increase in transconductance of the input stage. Transistors M_{1a} , M_{1d} & M_{2a} , M_{2d} are kept at higher aspect ratios for direct enhancement of gain. The designs of these transistors are given higher importance so that their small signal impedances must not lower the unity gain bandwidth.

BSIM4 sub-100 micron regime model using Mentor Graphics tool is employed for simulation. Gain of 6dB increase is observed compared to the RFC & FC. All transistors are kept in saturation. The diode connected transistors M_{3b} and M_{4b} are connected through linear active switches M_{11} and M_{12} respectively. The size of M_{11} and M_{12} is chosen appropriately to provide proper drain Voltages to maintain M_{3b} and M_{4b} at saturation. This helps

to avoid non linearity and proper ratio of small signal current mirroring.

The gain of 86.4dB and a phase margin of 85.2 degree is depicted in figure 3. The unity gain bandwidth of 210MHz is achieved without compromising gain or stability. This is of critical importance for the sensor readout circuit. Two second stage CS amplifier is included at both the differential output of Enhanced-gm RFC to get higher output swing. The output swing obtained was 0.8V for the supply Voltage of 1.2V as shown in figure 4. A cascode biasing stage is designed to bias the current summing devices and the folding node devices to get a good upper and lower bound of slew rate (i.e. SR^+ and SR^-). A high slew rate of $27.2V/\mu s$ is achieved. Input referred noise is lowered to $48.3 \mu V_{rms}$ by employing dual frequency transmission gate chopper.

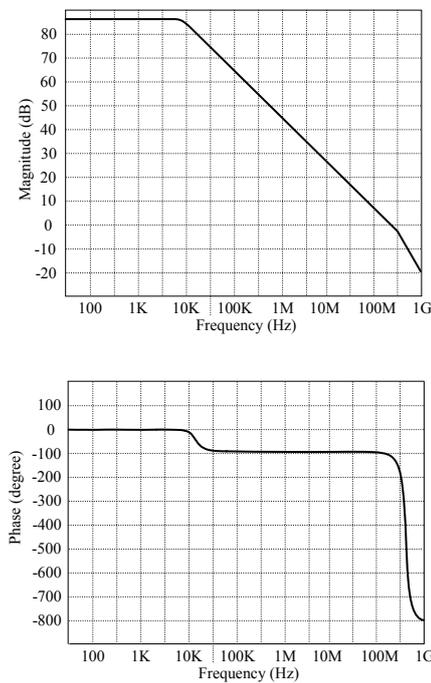


Figure 3. AC analysis of Enhanced-gm RFC

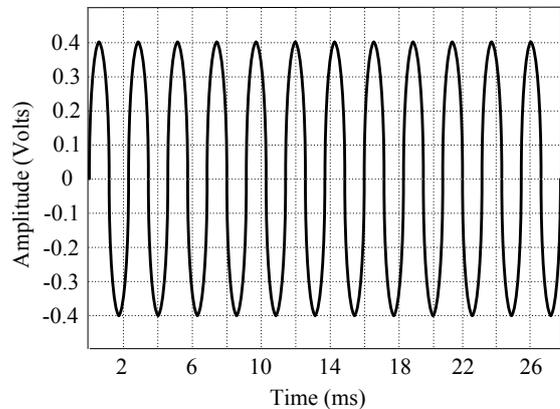


Figure 4. Transient analysis of Enhanced-gm RFC

IV. CONCLUSION

A single stage Enhanced-gm RFC is proposed in this work to obtain high gain for the sensor read out circuit application. It has been demonstrated that by current cross mirroring technique a gain of 10dB is increased as compared to [2], without compromising unity gain bandwidth. For the same power and area budget the amplifier's slew rate is improved and hence the settling time, which is critical for the low frequency sensor readout application. Table I gives the performance comparison between FC, RFC and Enhanced-gm RFC. The design parameters such as device sizes, biasing circuitry voltages, and values of F, H & N are carefully designed to be process variation proof.

TABLE I
PERFORMANCE COMPARISON

| Parameters | Folded Cascode [1] | Recycled Folded Cascode [1] | Improved RFC [2] | Enhanced-gm RFC [This Work] |
|---|--------------------|-----------------------------|------------------|-----------------------------|
| Bias Current (μA) | 260 | 260 | 260 | 185 |
| C_L (pF) | 7 | 7 | 7 | 7 |
| Gain (dB) | 41.1 | 60.9 | 70.2 | 86.4 |
| UGBW (MHz) | 70.7 | 134.2 | 83 | 210 |
| Slew Rate ($\text{V}/\mu\text{s}$) | 42.1 | 94.1 | 59.6 | 27.2 |
| 1% Settling Time (ns) | 20.7 | 11.2 | - | 11.3 |
| Input Referred Noise (μV_{rms}) | 53.2 | 48.5 | - | 48.3 |
| Phase Margin | 83 | 77 | 70.2 | 82.5 |

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