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RESEARCH ARTICLE

A Process-Based Temperature Compensated On-Chip CMOS VHF VCRO in 130-nm Si-Ge BiCMOS by Implementing an Empirical Control Equation

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ABSTRACT This paper presents a low-power CMOS temperature and process compensated 150.9 MHz Very-high-frequency (VHF) voltage-controlled-ring-oscillator (VCRO) for on-chip integration. The design employs a CMOS temperature-sensor and novel feedback control circuitry to generate the internal control-voltage for the VCRO which ensures oscillation in the vicinity of the desired frequency despite variations in temperature. The control circuitry is the implementation of an empirical equation expressing a temperature sensor-voltage into a specific control-voltage for three different process corners using three different switches. The control-voltage calibrates against temperature variation for the specific process-corner in order to maintain the same frequency of oscillation. Simulations shows that the proposed design maintains the oscillator's frequency within 0.39% from -10°C to 90°C . The fabricated chip implemented in 130-nm GF 8HP Si-Ge BiCMOS process, occupies an area of 0.0242-mm^2 and consumes $325\ \mu\text{W}$ while operating with a 1 V supply-voltage. The performance was verified through experimental immersion of DUT (device-under-test) in a temperature-controlled water-bath in the range 22.5°C – 70°C .

INDEX TERMS Analog CMOS circuits, temperature compensation, process compensation, voltage-controlled-ring-oscillator, circuit design, VHF, radio-frequency, water-bath.

I. INTRODUCTION

Frequency stability is a critical criterion for any clock generation circuit in CMOS implantable devices. This is mostly achieved through the integration of a phase-locked-loop (PLL) design with external crystal-oscillator and other control circuitry. This method of clock implementation requires considerable power-dissipation and silicon-area, and in-addition the packaging technique may also add extra-weight to the overall device. Advancement and miniaturization of implantable very high frequency (VHF) radio-frequency-identification (RFID) tags [1] demands very low-power and small footprint implementation. Thus

micro-power on-chip (crystal-free) clock generation circuit along-with significant frequency stability is required. VCRO is one of the simplest and lowest power consuming oscillator and hence suitable for on-chip frequency synthesis, given its frequency could be stabilized in terms of temperature variation and supply-voltage fluctuation. In this article, a novel design is proposed to stabilize the ring-oscillator frequency with respect to temperature variation considering various process-corners in a CMOS implementation. The prior-art of temperature-compensated oscillator design mostly dealt with generating temperature-invariant current-source or temperature-independent voltage reference circuit for the oscillator [2], [3]. In this new scheme, the oscillator maintains the center-frequency for a wide-range of temperature variation by monitoring the silicon-substrate

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temperature and dynamically adjusting the bias-current through the VCRO depending on the ambient temperature through the circuit implementation of an empirical equation. The empirical equation is implemented for three different process corners employing three different switches. The switch position for which the temperature variation is minimum corresponds to the circuit implemented empirical equation for the process-corner for which the actual fabricated (manufactured) process is the closest match. In this article, section II provides the design concept and the circuit implementation technique, section III provides simulation results, section IV discusses experimental methods and results, and, finally section V provides the concluding remarks.

II. DESIGN CONCEPT AND CIRCUIT IMPLEMENTATION

Temperature change makes the frequency instability of a ring-oscillator prominent due to the variation in the rise and fall time of the inverter-stages in the oscillator. Fig. 1 shows the variation in a VCRO's free-running frequency due to temperature fluctuation in the range -10°C to 90°C . The oscillator is a 3-inverter-stage 150.9 MHz VCRO designed for nominal operation at 27°C and typical-typical (tt) process corner. The figure shows the variations for the fast-fast (ff), typical-typical (tt) and slow-slow (ss) process corners for the 130-nm GF 8HP Si-Ge BiCMOS process. For all the 3 process-corner cases, the frequency increases linearly with temperature and this could be brought back to the desired value (150MHz in this case) for all thermal variations in the stipulated range through specific feedback to the oscillator with the appropriate control-voltage as shown in the Fig. 2. The equation representing each control-voltage ($V_{control}$) line with slope and intercept for each process is also shown in the figure. Here, the key idea is to insert a dynamic feedback-control circuit which can sense the silicon-substrate temperature surrounding the VCRO and generate the required control-voltage, $V_{control}$ that adjusts the bias-current in the VCRO to maintain its oscillation near its desired center-frequency for the specific process-corner. The generated $V_{control}$ signal thus specifically calibrates against temperature variation to maintain the same frequency of oscillation for different process-corners. Fig. 3 shows the architectural block diagram of the proposed new design of the feedback control circuit using empirical equation implementation. It consists of a temperature-sensor, the feed-back control-circuit, the core-oscillator and an output buffer-driver. The complete temperature compensation system has 3 separate power-supply domains. VCC for the temperature sensor, VDD_C for the control-circuitry, and, VDD_O for the oscillator and the buffer-driver, with VCC set at 800mV. The separate power-supply for the oscillator prevents supply-noise injection due to the switching of transistors in other parts of the circuitry [1]. There is no reliability issue if the 3 voltage supplies power-on in different orders. The temperature-sensor [4] is primarily a PMOS and an NMOS diode-connected transistor-pair (voltage-divider) as shown in the Fig. 3 which transduces a change in temperature into a change in the voltage-divided

output voltage. The top PMOS device is 25 times wider than the bottom NMOS device in order to keep the PMOS in the sub-threshold region while the NMOS is in the saturation region. The voltage resolution of the sensor with temperature variation depends greatly on their aspect-ratio. Fig. 4 displays the voltage variation of the sensor output versus temperature for different process corners for the 130-nm GF 8HP Si-Ge BiCMOS process. The equation representing each sensor output-voltage line for each process-corner with slope and intercept is also shown in the figure. The sensed-voltage, V_{sensor} , in this case has a positive temperature coefficient and varies linearly with temperature and hence can be expressed in the well-known, $y = mx + c$ straight line equation form as:

$$V_{sensor} = aT + b \quad (1)$$

where, T is the temperature in the absolute-scale (Kelvin), while, a (slope) and b (intercept) are the coefficients whose values depend on the particular process-corner as indicated by the 3 equations in the Fig. 4. The proposed control circuit maps V_{sensor} to the required control-voltage $V_{control}$ in the Fig. 2. This is achieved through the op-amp based implementation of an empirical equation expressing $V_{control}$ in terms of V_{sensor} with the variation in temperature for the three specific process-corners. This circuit implementation is composed of 3 op-amp stages with negative-feedback as shown in the Fig. 5. The first stage op-amp takes the input from the temperature-sensor and matches the slope while the other 2 stages adjust the voltage-level, and matches the intercept to finally generate a voltage equal to the required control-voltage in the Fig. 2 for a specific process. In the first-stage R_2 is essentially a trimming resistive circuit [2] whose value is to be opted using one of 3 pass-transistor switches to match the slope for a specific process-corner among the three different process corners. The output-voltage of the last-stage, $V_{control}$ can be expressed in terms of V_{sensor} through the opamp circuit implementation in the Fig. 5 of the following empirical equation:

$$V_{control} = V_{cm} \left(3 + \frac{R_2}{R_1} \right) - \frac{R_2}{R_1} V_{sensor} - (V_1 + V_2) \quad (2)$$

Here, V_{cm} is the common-mode voltage applied for amplifier biasing, V_1 and V_2 are the voltages applied for shifting the level of the control-voltage for intercept-control, and R_1 and R_2 are the gain-ratio resistors in the first-stage. The complete derivation of (2) from the Fig. 5 is provided in the appendix. In the Fig. 6, the top diagram shows the 2-stage folded-cascode differential-input and single-ended output CMOS operational-amplifier along-with the biasing and common-mode-feedback (CMFB) circuitry shown in the bottom diagram. The op-amp simulated in the 130-nm GF 8HP BiCMOS has a gain of 90dB, and, the CMFB circuit ensures high linearity. Two separate instances of the CMFB circuit are employed for the two stages of the folded-cascode amplifier in order to ensure high performance.

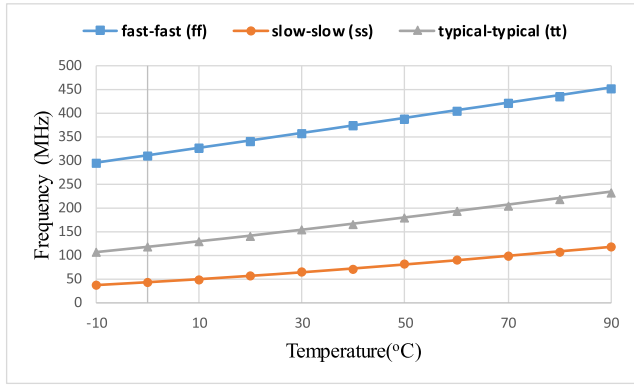


FIGURE 1. Frequency variation of the 150 MHz VCRO (designed for operation @27°C, and, tt process corner) with temperature fluctuation for different process corners for the 130-nm GF Si-Ge BiCMOS process.

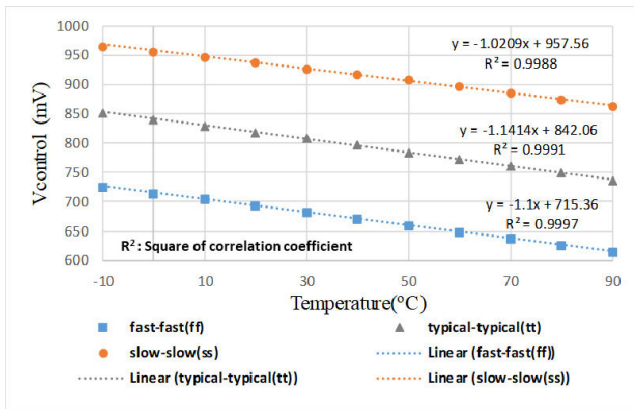


FIGURE 2. The required control-voltage ($V_{control}$) in the temperature variation range -10°C to 90°C for the VCRO to oscillate at 150MHz for the three different process corners.

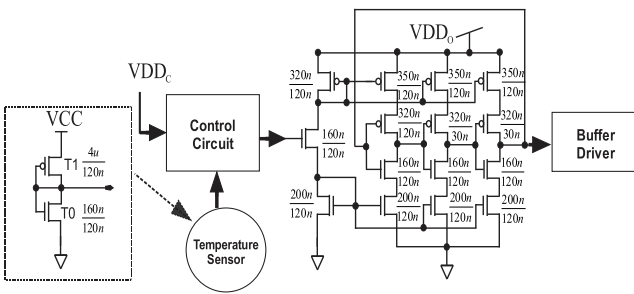


FIGURE 3. An architectural block-diagram of the proposed new temperature compensated VCRO, for three different process corners, complete with control-circuit through empirical equation implementation of control-voltage, temperature-sensor and output buffer-driver.

III. SIMULATION RESULTS

The proposed temperature-compensated CMOS ring-oscillator was implemented in 130-nm GF 8HP BiCMOS process and the post-layout simulation was carried out by including all the layout-parasitics. Fig. 7 shows the complete circuit layout which occupies an area of around $310 \times 78 \mu\text{m}^2$, excluding the test pads. The complete design consumes $325 \mu\text{W}$ using a 1V supply-voltage (V_{DDc} and V_{DDo})

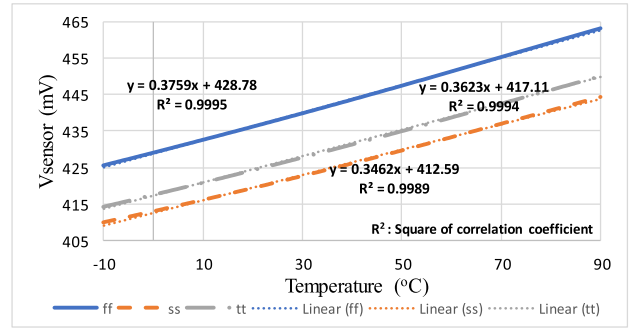


FIGURE 4. Post-layout simulated CMOS temperature sensor output-voltage versus temperature for three different process corners for the 130-nm GF 8HP Si-Ge BiCMOS process.

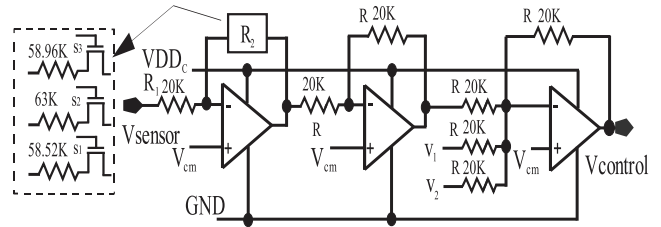


FIGURE 5. The 3 op-amp stage control-block for the generation of control-voltage ($V_{control}$) of the temperature compensated VCRO from the temperature-sensor output-voltage (V_{sensor}). Each pass-transistor switch setting (control) is for specific process-corner to set the specific slope, while, V_1 and V_2 are used for intercept control.

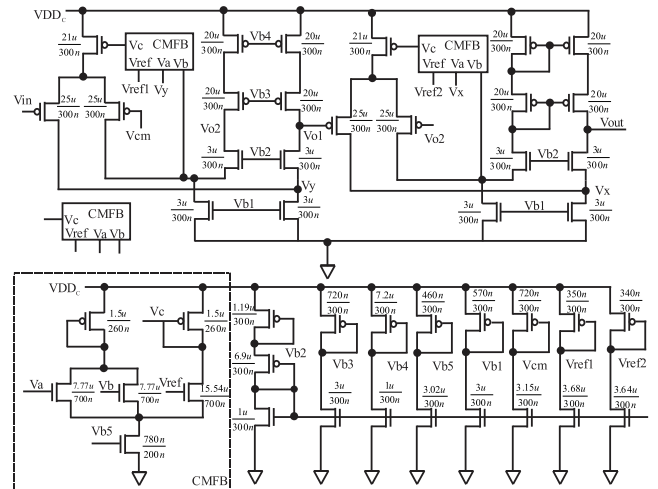


FIGURE 6. Design of the op-amp employed in the 3 op-amp stages in the Fig. 5. A 2-stage folded-cascode operational-amplifier with common-mode-feedback (CMFB) (upper circuit block), along-with, bias-voltages and common-mode-feedback (CMFB) generation circuitry (lower circuit block) in the 130-nm GF 8HP BiCMOS process.

along-with 0.8V sensor-voltage (V_{CC}), and, @ 150.6 MHz, for tt process-corner. The supply-voltage can be adjusted to set the frequency @150MHz for different process-corners. The simulated compensated frequency variation of the VCRO for 3 different process-corners with corresponding switch settings, switch-position 2 for “tt”, switch-position 1 for “ff”, and switch-position 3 for “ss” for a wide temperature

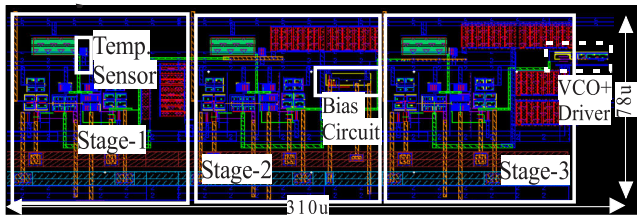


FIGURE 7. Complete layout of the proposed temperature-compensated CMOS ring-oscillator along-with the control circuit employing the temperature sensor and the 3 op-amp stage implementation of the empirical equation in (2) as shown in the Fig. 5.

TABLE 1. Simulated frequency variation for the process-based temperature compensated VCRO in the temperature range -10°C to 90°C for different process-corners and corresponding switch settings for temperature compensation, with switch-position 2 for “tt”, switch-position 1 for “ff” and switch-position 3 for “ss”.

Process corner	Switch Position-setting	Frequency(f) (MHz) @ 25°C	$\Delta(f_{\text{min}}-f_{\text{max}})$ (MHz)	Variation(%) -10°C to 90°C
tt	2	150.94	0.59	0.393
ff	1	150.6	0.68	0.527
ss	3	150.11	3.6	2.4

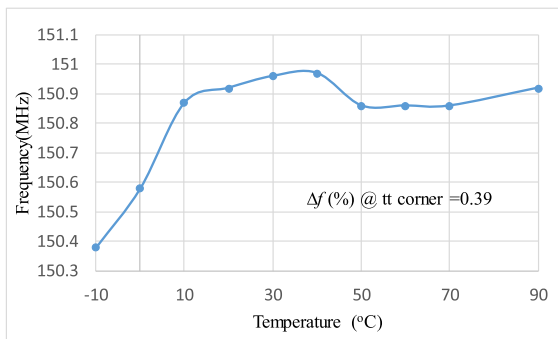


FIGURE 8. Post layout simulated frequency variation of the temperature compensated 150MHz VCRO at typical-typical process corner.

variation is shown in the Table 1. Fig. 8 plots the variation in the oscillator frequency at the typical-typical process corner employing the designated switch- position 2 for the “tt” corner. It is found to vary less than 0.39% for a set frequency of 150.9 MHz in the temperature variation range of -10°C to 90°C . Fig. 9 shows the simulated phase noise spectrum of the oscillator at 150.9 MHz indicating a very low phase-noise of -76.5 dBc/Hz at 1MHz frequency offset. The performance of the proposed design is summarized and compared with the prior arts in the Table 2. This novel design provides a superior performance in frequency stabilization with temperature variation at the set frequency of 150.9 MHz, and also, uses the lowest overall power per-cycle of the oscillator frequency.

IV. EXPERIMENTAL METHODS AND RESULTS

The process-based temperature compensated CMOS VCRO was fabricated on one corner section of a multi-project chip

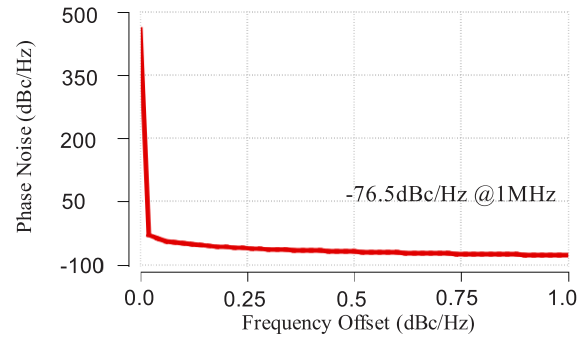


FIGURE 9. Phase noise vs frequency offset of the VCRO at 27°C and tt process corner.

TABLE 2. Comparison of this work with prior arts.

References	EL 2007 [2]	CICC 2007 [5]	ISSCC 2015 [6]	EL 2016 [3]	MWSCAS 2018 [7]	This work
Technology (nm CMOS)	350	130	180	180	130	130
Frequency(MHz)	1	1250	4.7	1.9	13.4	150.9
Supply Voltage	3	3.3	1.4	3	1.2	1
Power (mW)	N/A	19.8	0.053	0.39	0.701	0.325
Power/ cycle (uW/MHz)	N/A	15.84	11.27	205.26	52.3	2.16
Area(mm^2)	0.162	0.014	0.086	0.22	0.0848	0.0242
Freq. Variation [%] with Temp	3.3 @ 0°C to 100°C	5 @ -40°C to 125°C	0.7 @ -40°C to 125°C	1.16 @ -40°C to 80°C	0.175 @ -40°C to 80°C	0.39 @ -10°C to 90°C
Freq. Variation with Process	N/A	5%	N/A	$\pm 2.5\%$	1.19%	2.40%
Phase noise@1MHz dBc/Hz	N/A	-88	N/A	N/A	N/A	-76.5

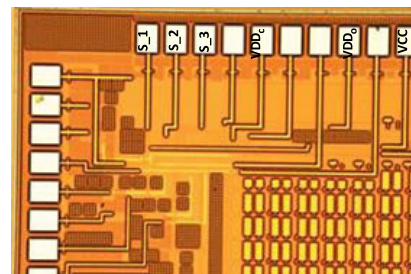


FIGURE 10. Photomicrograph of the fabricated temperature-compensated CMOS ring-oscillator along with the temperature control circuit in 130nm GF 8HP CMOS.

in the 130-nm GF 8HP Si-Ge BiCMOS process through MOSIS. The Fig. 10 shows the photomicrograph of the fabricated temperature-compensated VCRO along with the I/O pad labels. The pass-transistor switches are set by connecting to VDD (Logic “High”). In order to achieve minimal layout footprint the resistors were implemented using salicide-blocked OP P+ polysilicon resistors available in the 8HP BiCMOS library. Some process layers are hidden by GF CMP fill layer. The experimental setup consisted mainly of a Fisher-Scientific Isotemp precision electric water-bath with temperature control in the range (22.5°C - 100°C).

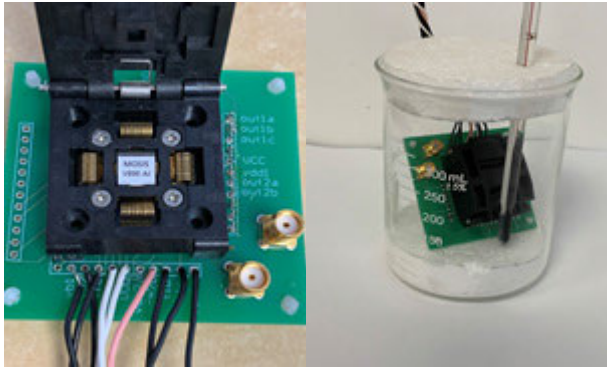


FIGURE 11. (a) The fabricated chip mounted in QFN package and assembled on a strip of PCB (the test jig), (b) the test jig lodged inside a 400 ml beaker along-with a thermometer touching it.

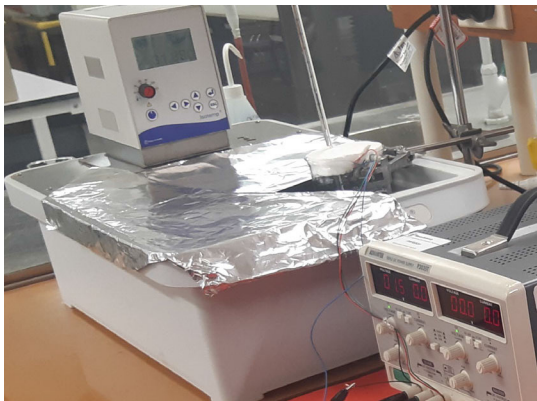


FIGURE 12. The 400 ml beaker along-with a thermometer immersed in the temperature-controlled Fisher-Scientific Isotemp precision electric water-bath.

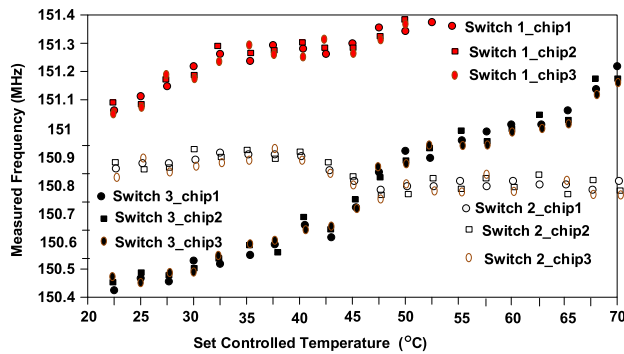


FIGURE 13. Experimental variation in frequency of the VCRO with temperature in the water-bath set temperature range of 22.5°C - 70°C.

The fabricated chip (MOSIS V89E-AJ) was assembled in an OCP_QFN_7X7_48A SMT leadless package and was mounted in a Yamaichi 0.5mm pitch 48-way through hole QFN test-socket as shown in the Fig. 11(a). To facilitate I/O access for measurements a PCB was fabricated and the test-socket containing the chip was mounted and soldered to it. The composite PCB test jig along-with a thermometer was then lodged inside a 400-ml beaker with the thermometer in close contact with the test-board as shown in the Fig. 11(b). Two circular cut-to-fit polystyrene pieces were placed at

the top opening and at the bottom of the beaker tightly fitting (“snugging”) the circular perimeter. This enclosed environment was created inside the beaker in order to hold the chip temperature inside the beaker at a constant value. The beaker with the test jig was then submerged in the insulated electric water-bath. Wiring leads from the VCRO-under-test (DUT) protruding from the top of the beaker was connected to a power-supply (ADV@NTEK P3035T DC power-supply) and an oscilloscope (Rohde&Schwarz, HMO3002 400 MHz 4 GSa/s oscilloscope), for frequency measurements. To record a reading the water-bath was set at a certain test temperature and around 30 minutes was allowed to obtain an equilibrium temperature for the thermometer reading inside the beaker. The beaker immersed in the water-bath is shown in the Fig. 12. The thermal sensitivity of the VCRO’s time-period was measured in the range 22.5°C - 70°C. MOSIS provided 5 SMT packaged chips and measurements were carried out employing 3 chips and all the three switch positions one at a time. There were 20 measurement points in the temperature scale in the range 22.5°C - 70°C, resulting in a total of 180 measurements. Fig. 13 shows that the switch position 2 produces the minimum variation in the measured frequency being under 0.08% which is in close agreement with the simulated frequency variation within this temperature-range for the typical-typical process corner as shown in the Fig. 8. All the 3 chips demonstrated a minimum frequency variation of under 0.1% for the switch position 2. Switch positions 1 and 3 produced much more frequency dispersion with temperature variation, indicating typical-typical process corner for the packaged chips supplied by MOSIS.

V. CONCLUSION

A temperature-compensated VCRO with a novel control circuit that ensures stable oscillations has been presented. There is only 0.39% variation in frequency with temperature and the circuit dissipates only 2.16μW/MHz compared to other recent prior arts. Experimental verification shows that the fabricated temperature compensated VCRO operates in close agreement with the simulation.

APPENDIX

Let V_{out1} and V_{out2} be the outputs of the 1st and the 2nd op-amp while $V_{control}$ being the output of the last op-amp. Then for the 1st op-amp:

$$V_{out1} = V_{cm} + \frac{R_2}{R_1} V_{cm} - \frac{R_2}{R_1} V_{sesnsor} \tag{A.1}$$

Next for the 2nd op-amp,

$$V_{out2} = 2V_{cm} - V_{out1} \tag{A.2}$$

Or,

$$V_{out2} = V_{cm} - \frac{R_2}{R_1} V_{cm} + \frac{R_2}{R_1} V_{sesnsor} \tag{A.3}$$

Finally for the 3rd op-amp,

$$V_{control} = 4V_{cm} - (V_1 + V_2) - V_{out2} \tag{A.4}$$

Or,

$$V_{control} = V_{cm} \left(3 + \frac{R_2}{R_1} \right) - \frac{R_2}{R_1} V_{sensor} - (V_1 + V_2) \quad (A.5)$$

REFERENCES

- [1] M. Kumari and S. M. R. Hasan, "A low duty cycle burst-mode telemetry signal generation technique for VHF insect tracking and its CMOS implementation," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 28, no. 3, pp. 833–837, Mar. 2020.
- [2] K. N. Leung, C. H. Lo, P. K. T. Mok, Y. Y. Mai, W. Y. Leung, and M. J. Chan, "Temperature-compensated CMOS ring oscillator for power-management circuits," *Electron. Lett.*, vol. 43, no. 15, pp. 786–787, Jul. 2007.
- [3] S. Zhang, A. Li, Y. Han, L. Jie, X. Han, and R. C. C. Cheung, "Temperature compensation technique for ring oscillators with tail current," *Electron. Lett.*, vol. 52, no. 13, pp. 1108–1110, Jun. 2016.
- [4] R. Häggglund and L. Wanhammar. *Tuning and Compensation of Temperature Effects in Analog Integrated Filters*. [Online]. Available: https://www.academia.edu/47613594/Tuning_and_Compensation_of_Temperature_Effects_in_Analog_Integrated_Filters
- [5] K. R. Lakshmikumar, V. Mukundagiri, and S. L. J. Gierkink, "A process and temperature compensated two-stage ring oscillator," in *Proc. IEEE Custom Integr. Circuits Conf.*, San Jose, CA, USA, Sep. 2007, pp. 691–694.
- [6] J. Lee, P. Park, S. Cho, and M. Je, "A 4.7 MHz 53 μ W fully differential CMOS reference clock oscillator with –22 dB worstcase PSNR for miniaturized SoCs," in *Dig. Tech. Papers IEEE Int. Solid-State Circuits Conf.*, San Francisco, CA, USA, Feb. 2015, pp. 1–3.
- [7] K. Xiao, B. Wang, X. Lin, and C. Qiu, "A balanced hybrid ring oscillator for precise temperature compensation," in *Proc. IEEE 61st Int. Midwest Symp. Circuits Syst. (MWSCAS)*, Windsor, ON, Canada, Aug. 2018, pp. 336–339.



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