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**VLSI Design, Fabrication and Testing of an Ultra-Wideband
Low Noise Amplifier Microchip using Nanometric CMOS
Technology**

Doctor of Philosophy

in

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ABSTRACT

The wide operating bandwidth of the ultra-wideband (UWB) signal leads to new circuit design challenges and methodologies. Similar to any other RF system, the most critical component of the UWB receiver is the low noise amplifier (LNA). Contrary to the narrow-band LNAs, the single-tone assumption is not valid for defining the SNR of an UWB LNA where the input signal encompasses several GHz. Defining the UWB LNA system's SNR as the matched filter bound (MFB) is an appropriate approach to deduce its noise figure (NF). Using this approach, a mathematical model is proposed to achieve optimal NF, employing the g_m -boosted common gate (CG) LNA topology along with a passive noise matching input network. Besides the low noise performance, the other challenges in the design of the UWB LNA include adequate input match and forward power gain with low power dissipation. Considering the superior performance of the g_m -boosted CG amplifier topology for UWB, a new single-ended (SE) g_m -boosted CG UWB LNA architecture is proposed in this research. In the SE LNA architecture, the power dissipation is further minimized by sharing the bias current between the g_m -boosted CG and the active g_m -boosting amplifier stages in a current-reuse fashion ("*piggyback*" g_m -boosting). The proposed *piggyback* g_m -boosted CG LNA, operating in 3-5 GHz range, is fabricated using 130nm RFCMOS process with adequate results. The noise optimization mathematical model proposed in this thesis is applied to the new *piggyback* g_m -boosted CG LNA architecture by including an intervening noise matching passive network at the input of the LNA. The bandwidth of the noise matched *piggyback* g_m -boosted CG LNA is extended using series peaking technique to the complete UWB band from 3.1 to 10.6 GHz. The proposed full-band noise matched UWB LNA is fabricated in a differential manner using 130nm RFCMOS process and exhibited excellent performance improvements with figure of merit (FOM) of 2.86.

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