Micro-Threading And FPGA Implementation Of A RISC Microprocessor

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In loving memory of my mother, the late Zahra Ridha Witwit

MICRO-THREADING AND FPGA IMPLEMENTATION OF A RISC MICROPROCESSOR

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Abstract

This thesis is the outcome of research in two areas of computer technology: microprocessor and multi-processor architectures (specifically from the perspective of how differently they tolerate highly-latent and non-deterministic events), and hardware design of complex digital systems containing both datapath and control (particularly microprocessors).

This thesis starts by pointing out that in order to achieve high processing speeds, current popular superscalar microprocessors (e.g. Intel Pentiums, Digital Alpha, etc) rely heavily on the technique of speculating the outcome of instruction flow in order to predict the behaviour of non-deterministic computing operations (as in loading operands from high-latency memory into the processor). This is fine only if the speculation is correct. But, what if it isn't? If the speculation fails, this would mean that the processor has to abandon its current decision (which now proved to be the wrong one) for the instruction flow path taken and to start all over again with the other path (the actual correct one). This is a waste of valuable processing time and hardware resources and a reduction of performance when speculation fails. Therefore, these processors can achieve high performance only when the majority of speculations are successful (being able to predict the right path).

In an attempt to overcome the above shortcomings, the first part of this thesis is an investigation of the novel vector micro-threading architecture as an alternative approach to the current superscalar-based speculative microprocessor designs. Micro-threading is based on the not-so-novel multithreading technique, which avoids speculation altogether and instead, starts running a different thread of instructions while waiting for the non-determinism to be resolved. This utilizes the chip resources more efficiently without waste of any processing power.

The rest of this thesis focuses on the baseline RISC processor platform, the MIPS R2000, which is reviewed first then partially synthesized from the RTL (Register Transfer Level) description using VHDL and then simulated and tested. This is conducted in order for future research to build upon and add the micro-threading architectural add-ons and modifications.

Keywords:

Micro-threading, Latency Tolerance, FPGA Synthesis, RISC Architecture, MIPS R2000 processor, VHDL.

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Publications

Publications prepared during the course of the research for this thesis are as follows:

1. F M Al-Ali and C R Jesshope, 2000, *Survey of High-latency Tolerance in Contemporary Microprocessor Architectures*, Proc. 7th Annual New Zealand Engineering and Technology Postgraduate Conference, pp339-346, ISBN 0-473-07224-6, Massey University, Palmerston North, New Zealand, 23rd & 24th Nov.

2. F M Al-Ali and C R Jesshope, 2001, *Survey of High-latency Tolerance in Future Microprocessor Architectures*, Proc. New Zealand Computer Science research Students' Conference (NZCSRSC 2001), pp86-97, TR-COSC 02/01, University of Canterbury, Christchurch, New Zealand, 19th & 20th April.

3. F M Al-Ali and R F Browne, *Behavioural VHDL Model of a Vector Micro-threading Chip-multiprocessor,* Proceedings of the 6th International Conference/Exhibition on High Performance Computing in Asia-Pacific Region (HPC Asia 2002), Bangalore, 16-19 December 2002, Vol.2, pp 518-521, Tata McGraw-Hill Publishing Company Ltd., New Delhi, India, ISBN 0-07-049992-6.

4. F. M. Al-Ali and R. F. Browne, *An FPGA Implementation of a RISC Microprocessor*, Proceedings of the 11th Electronics New Zealand Conference (ENZCon'04), 15-16 Nov, 2004, p 106-111, ISBN 0-476-01106-X, Massey University, Palmerston North, New Zealand.

5. F. M. Al-Ali and R. F. Browne, *VHDL Modelling of a RISC Microprocessor: Synthesis, Assembler, Loader, and Testing*, Proceedings of the 12th Electronics New Zealand Conference (ENZCon'05), 14-15 Nov, 2005, pp 63-68, ISBN 0-473-10634-5, Manukau Institute of Technology, Manukau City, Auckland, New Zealand.

CHAPTER ONE

INTRODUCTION

This chapter outlines the motivation behind this thesis, followed by the scope and logical structure of the research work undertaken. The key ideas to be presented in the body of the thesis are introduced and the contents of the chapters and appendices are briefly outlined.

1.1 How It All Started

So, why did I decide to do my MSc? And, why did I choose this particularly challenging yet equally inspiring subject of Microprocessor Design?

It all started back in Christmas of 1991; only a few months after I graduated with a B.Sc. degree in Electronics Engineering and Communications. It was the subject of microprocessor design, which really mesmerized my imagination! It was the idea of how powerful the human spirit is, how creative the minds of scientists are, and how today's technology is so developed to the point of conceiving such powerful inventions while keeping them tamed to the point of advancing our lives.

So, I wanted to design microprocessors! I wanted to sit in front of the screen and design the internal interconnections, components, and wiring diagram of the microprocessor. Although back then in 1991 it seemed to me no more than a dream, but the following 15 years led to the successful fruition of this MSc thesis in the FPGA implementation of a RISC microprocessor.

Embarking on this 15-year quest towards achieving my dream, my first job after graduation was as a PC Repair Technician. I did not know what exactly I had to do in the short term (with PCs), but I knew exactly where I am headed to in the long run (with designing microprocessors). Coming from an engineering background was the main drive behind my involvement in the hardware aspects of PCs as the starting point. Being involved with PCs, I learned of Intel's line of the then-popular microprocessors (8086/8088, 80286, 80386, 80486…).

The main events behind turning my dream of designing microprocessors into an actual MSc dissertation took place between 1991 and 1996. That was the time when I started to take notice of the fact that a great percentage of Intel's microprocessors were actually fabricated in Malaysia, where Intel has the largest chip manufacturing facility in the world, located on the industrial island of Penang in the northern part of Malaysia. Therefore, my dream of designing microprocessors became then synonymous with another one: working as a chip design engineer at Intel Malaysia. So, it was time to pay Malaysia a visit!

So, I arrived in Malaysia in October 1996. A few days later, I paid Intel Penang's office a visit. That was a historic event! I could not believe that I was finally walking into the offices of the Holy Grail of the microprocessor industry and the largest chip designer and manufacturer in the world! I asked the receptionist for a job application form. Instead, she got the human resources manager to come down and see me. He told me that Intel would not hire me unless I have, at the least, a Masters in VLSI/Chip/Microprocessor Design.

THAT was the moment when my dream became even more focused: to have a Masters in Microprocessor Design!

Of course, I did not end up getting any job at Intel back then but I continued to look out for any opportunities to pursue my MSc studies in this field. This opportunity did finally arise in 2000 at Massey University. It brings me so much pride now that this MSc dissertation is the end of that 15-year quest.

Now that the story behind this research has been told, the next section elaborates on the scope of this research and thesis overview.

1.2 Scope of This Research: Thesis Overview

This thesis is the outcome of research in two areas of the computer technology: microprocessor and multi-processor architectures (specifically from the perspective of how differently they tolerate highly-latent and non-deterministic events), and hardware design of complex digital systems containing both datapath and control (particularly microprocessors).

As a result, the key achievements of this work are based on the three key areas of research investigated and covered in this thesis. These are:

- The problems associated with tolerating highly latent and non-deterministic events in existing microprocessor and multi-processor architectures.

- The high level behavioural VHDL (Very High Speed Integrated Circuit Hardware Description Language) description of the novel vector micro-threading chip multi-processor architecture, which is proposed to efficiently tolerate such high latency and non-determinism. The starting point for the design of this micro-threading architecture is the popular MIPS RISC (Reduced Instruction Set Computing) processor architecture.

- The hardware implementation involving the VHDL description, synthesis and simulation of the MIPS R2000 RISC microprocessor onto an FPGA (Field Programmable Gate Array) chip. The MIPS microprocessor is an existing architecture and is implemented in this research to provide the baseline processor platform for the future micro-threading architectural add-ons and modifications.

This thesis shows that in order to achieve high processing speeds, current popular superscalar microprocessors (e.g. Intel Pentiums, Digital Alpha, etc) rely heavily on the technique of speculating the outcome of instruction flow in order to predict the behaviour of non-deterministic computing operations (as in loading operands from high-latency memory into the processor). This is fine only if the speculation is

correct. But, what if it isn't? If the speculation fails, this would mean that the processor has to abandon its current decision (which now proved to be the wrong one) for the instruction flow path taken and to start all over again with the other path (the actual correct one). This is a waste of valuable processing time and hardware resources and a reduction of performance when speculation fails. Therefore, these processors can achieve high performance only when the majority of speculations are successful (being able to predict the right path).

A part of the focus of this research is an investigation of the novel vector micro-threading architecture as an alternative approach to the current superscalar-based speculative microprocessor designs. Micro-threading is based on the not-so-novel multithreading technique, which avoids speculation altogether and instead, starts running a different thread of instructions while waiting for the non-deterministic outcome of the instruction execution to be resolved. This utilises the chip resources more efficiently without waste of any processing power.

As this research progressed, the baseline RISC processor platform, the MIPS R2000, was reviewed first then synthesized from the RTL (Register Transfer Level) description using VHDL and then simulated and tested. This was conducted in order for future research to build upon and add the micro-threading architectural add-ons and modifications.

One outcome of this research is the publication of a total of five papers (refereed and non-refereed) in five different conference proceedings within New Zealand [2, 4, 5, 6] and abroad [3]. It is worth mentioning here that [3] was a refereed publication in the conference proceedings of an international conference of high standing.

The next section briefly looks at the contents of the rest of the chapters in this thesis.

1.3 Contents of the Chapters

Chapter Two:

Survey of High-Latency Tolerance in Contemporary and Future Processor Architectures

This chapter provides the necessary background and motivation for this research work by addressing the first of the three key areas of research investigated and covered in this thesis. Therefore, in this chapter, existing material and literature is surveyed in order to shed the necessary light on the problem at hand: the shortcomings of existing and future processor architectures in terms of their tolerance for high-latency and non-determinism. The architectures surveyed are the Superscalar, VLIW (Very Long Instruction Word), EPIC (Explicitly Parallel Instruction Computing), Dataflow, and the different Multi-threading variants.

Consequently, this sets the scene for the introduction of the micro-threading architecture (which will be introduced in chapter three).

Chapter Three:

Introducing Micro-threading as a Solution to the Problem of High-Latency

In this chapter, the Micro-threading architecture as a proposed solution to the problems of high-latency and non-determinism, is formally introduced and described. The material presented here is based mainly on research work carried out by Jesshope [13, 32] and Jesshope and Luo [34, 39, 33] and then surveyed by the author [5, 6].

Chapter Four:

Hardware Design Methodology and EDA Design Tools

This chapter outlines the hardware design methodology, processes, challenges, CAD/EDA design tools, and lessons learnt from synthesizing a MIPS R2000 RISC microprocessor onto an FPGA VLSI chip. The chapter starts with an overview of the design process and hierarchical partitioning. Then, the issues of implementing the datapath (combinational logic) and memory (sequential logic) components onto the chosen Xilinx Virtex-II FPGA, are discussed. This determines the efficiency with which a design can be implemented on an FPGA chip.

Chapter Five:

Review of MIPS R2000 Architecture

This chapter presents a brief review of the basics of the MIPS R2000 microprocessor Instruction Set Architecture (ISA), or simply, Architecture. This is the interface between the highest layer of the microprocessor hardware and the lowest layer of the software. The basics outlined in this chapter constitute the foundation on top of which the rest of the chapters are based. This chapter is extracted mainly from excerpts from [47]. Wherever necessary and possible, reference to the relevant page numbers will also be made. This chapter is annotated with the author's comments and tailored adaptation for the context of this research.

Chapter Six:

VHDL Description and Synthesis of MIPS R2000 Microprocessor

This chapter presents a brief review of the Register Transfer Level (RTL) description of the MIPS R2000 microprocessor followed by the author's own work on implementing this description in VHDL. This VHDL description (also called RTL Model) of the MIPS R2000 microprocessor includes synthesis onto the target Xilinx Virtex-II FPGA chip followed by simulating a machine language code running on this microprocessor. Again, this chapter is based on and complements the material presented in [47] and [48] and is annotated with the author's comments and tailored adaptation for the context of this research. The details are covered in Appendices A to C (on the *Companion CD*).

Chapter Seven:

Assembler/Loader for the Synthesised MIPS R2000 Microprocessor

This chapter presents a novel and unconventional way of writing an assembler/loader for the MIPS R2000 microprocessor synthesized in chapter six, using the VHDL language. This was simulated in Model Technology Inc. (MTI) ModelSim XE.

Chapter Eight:

VHDL Description of the Micro-threading Chip Multi-processor

This chapter briefly describes how the micro-threading architectural add-ons and components are added to the standard MIPS architecture to build the micro-threading microprocessor and also the chip multiprocessor. The micro-threading VHDL description presented in this chapter is at a high level of abstraction as it is a behavioural description augmented with algorithms. Some VHDL pseudo-code is also included. As elaborated in chapter four, this is the first step of the hardware design process for the micro-threading microprocessor/multiprocessor and, therefore, paves the way for future research in which these algorithms and high level descriptions are utilized in designing the final micro-threading microprocessor and/or chip multiprocessor.

Chapter Nine:

Conclusions and Future Work

This chapter concludes this thesis by reviewing the summaries of the key points from the previous chapters along with the important areas of research covered by the thesis. Conclusions are drawn and further areas of enhancement and future research work are listed.

A glossary is also provided following the list of references. The next section briefly looks at the contents of the appendices found on the accompanying *Companion CD*.

1.4 Contents of the Appendices (on the Companion CD)

Appendix A:

VHDL Description and Synthesis of MIPS R2000 Datapath Basic Building Blocks

This appendix presents a brief review of the Register Transfer Level (RTL) description of the basic building blocks for the datapath of the MIPS R2000 microprocessor followed by the author's own work on implementing this description in VHDL. This VHDL description (also called RTL Model) of these datapath basic building blocks includes simulation and synthesis onto the target Xilinx Virtex-II FPGA chip. Again, this appendix is based on and complements the material presented in [47] and [48] and is annotated with the author's comments and tailored adaptation for the context of this research. This appendix is the basis on which Appendix B builds upon to create the VHDL description and synthesis of the finalized full MIPS R2000 microprocessor in chapter 6.

Appendix B:

VHDL Description and Synthesis of MIPS R2000 Complete Datapath

This appendix presents the development of the Register Transfer Level (RTL) description of the complete datapath (without the control unit yet) of the MIPS R2000 microprocessor. The datapath concepts are first reviewed and then followed by the author's own work on implementing this description in VHDL. This VHDL description (also called RTL Model) of this complete datapath includes simulation and synthesis onto the target Xilinx Virtex-II FPGA chip. Again, this appendix is based on and complements the material presented in [47] and [48] and is annotated with the author's comments and tailored adaptation for the context of this research. This appendix is the basis on which Appendix C builds upon to create the VHDL description and synthesis of the finalized full MIPS R2000 microprocessor in chapter 6.

Appendix C:

VHDL Description and Synthesis of MIPS R2000 Control Unit

This appendix presents the development of the Register Transfer Level (RTL) description of the control unit of the MIPS R2000 microprocessor. The control unit concepts are first reviewed and then followed by the author's own work on implementing this description in VHDL. This VHDL description (also called RTL Model) of this control unit includes simulation and synthesis onto the target Xilinx Virtex-II FPGA chip. Again, this appendix is based on and complements the material presented in [47] and [48] and is annotated with the author's comments and tailored adaptation for the context of this research. This appendix is the last

piece of the big picture used to create the VHDL description and synthesis of the finalised full MIPS R2000 microprocessor in chapter 6.

Appendix D:

Supplementary Material for Chapter Six

This appendix covers the supplementary material for Chapter Six. This includes, higher resolution figures, diagrams, and detailed VHDL code.

Appendix E:

Published Conference Proceedings

This appendix is a collection of the five papers generated by this research and published in conference proceedings. These papers are:

- *Survey of High-latency Tolerance in Contemporary Microprocessor Architectures [5]*
- *Survey of High-latency Tolerance in Future Microprocessor Architectures [6]*
- *An FPGA Implementation of a RISC Microprocessor [2]*
- *VHDL Modelling of a RISC Microprocessor: Synthesis, Assembler, Loader, and Testing [4]*
- *Behavioural VHDL Model of a Vector Micro-threading Chip Multi-processor [3]*

1.5 Summary and Conclusions

This chapter outlined the motivation behind this thesis, along with the scope and structure of the research work undertaken. The key ideas to be presented in the body of the thesis were introduced and the content of each chapter was briefly outlined.

The next chapter surveys high-latency tolerance in contemporary and future microprocessor architectures and the problems associated with that.