# Investigation, Design and Fabrication of Miniaturized CMOS Novel Active RFID Tags

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# ABSTRACT

The drastic decline in the bee population in the past few years is alarming given the quantity and quality of global food reliance on these insect pollinators. To ensure sustainable crop production and maintain biodiversity, it has become an important area of research for entomologists to study the factors involved in the dramatic population decline of these tiny insects. Understanding the insect's biology and their foraging behavior tracking in the agricultural landscape is crucial. However, due to the large size of the available PCB-based tracking tags knowing their true behaviours in the presence of various chemical fertilizers and pesticides is still a challenge.

In this research, a very new VHF radio telemeter architecture has been developed which could facilitate tracking of a large number of small insects and bees wirelessly in real-time at a distance of around 1km. The architecture is based on a novel circuit topology to generate an extremely low duty cycle signal digitally which for the first time does not require any passive elements. This digital generation technique of the low duty cycle has made it possible to realize the complete telemeter design on 1mmX 1mm ASIC chip, except for the antenna and the battery, and eliminated the need for discreet components which are mounted on PCB.

Due to inconsistent fabrication facilities, the telemeter circuit parts were implemented in CMOS8RF-130nm and 8HPP-28nm, but the final ASIC telemeter prototype is realized in TSMC 65nm process technology and the fabricated chip is experimentally tested in the lab to verify its performance in the manufacturing environment. The design consists of a digital core circuit to generate 8-bit binary-coded 0.0078 duty-cycled burst mode signaling and a full on-chip analog power management circuit to locally generate the required voltage supplies with predefined dependence on temperature for the digital circuitry with the compensation for the temperature variation on the telemeter performance.

A white paper calculation has been presented to package the insect telemeter ASIC, along with 10cm antenna directly over 80mg, 5mmX5mmX1mm silver oxide battery to yield a 95mg complete telemeter package, making it to be the world's smallest and the lightest VHF radio telemeter.

# ACKNOWLEDGMENT

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| | |
|---|---|
| ADC | Analog to Digital Converter |
| ASIC | Application-Specific Integrated Circuit |
| CLK | Clock |
| CMOS | Complementary Metal Oxide Semiconductor |
| CTAT | Complementary To Absolute Temperature |
| DIP | Dual Inline Package |
| DRC | Design Rule Check |
| ESA | Electrically Small Antenna |
| ESD | ElectroStatic Discharge |
| FD | Frequency Divider |
| FIB | Focused Ion Beam |
| FSK | Frequency Shift Keying |
| FFT | Fast Fourier Transform |
| IC | Integrated Circuits |
| LDC | Low Duty Cycle Signal |
| LDO | Low Drop-Out Regulator |
| LPF | Low Pass Filter |
| LVS | Layout Versus Schematic |
| MATLAB | MATrix LABoratory |
| OTA | Operational Transconductance Amplifier |
| PCB | Printed Circuit Board |
| PEX | Parasitic EXtraction |
| PISO | Parallel Input Serial Output |
| PIT | Passive Integrated Transponder |

| | |
|---|---|
| PMU | Power Management Unit |
| PSRR | Power Supply Rejection Ratio |
| PSS | Periodic Steady-State |
| PTAT | Proportional To Absolute Temperature |
| PVT | Process Voltage Temperature |
| QFN | Quad Flat No-leads |
| RFID | Radio Frequency Identification |
| RMS | Root Mean Square |
| SMT | Surface Mount Technology |
| VCDCG | Voltage Controlled Duty Cycle Generator |
| VCRO | Voltage Controlled Ring Oscillator |
| VHF | Very High Frequency |
| VLSI | Very Large-Scale Integration |
| VREF | Voltage Reference |

# CHAPTER 1

# INTRODUCTION

There was a time when even having a camera in a phone or combining a microphone and speaker with a watch seemed challenging. Such technological advancement has relied on "Moore's law" to miniaturize electronics devices and include several complex electronics functions within minimum size and weight. Various approaches have evolved to keep up with the golden rule for the doubling of transistors on ICs. With the slowdown of Moore's law over the past few years, engineers, and researchers have come up with several other matches, including System-on-Chip (SOC), System-In-Package (SIP), System-On-Package (SOP). These advances have actively been applied to the computing world including mobile phones, computers, and are also being extended in biomedical applications to devices capsule size implants to monitor human health or to aid people with disabilities.

This thesis explores another such field - Wildlife Radio Telemetry, where these technological advancements could be pursued to miniaturize the telemeter size and extend the tracking ability of these devices beyond animals and birds, to a wide range of small species, especially flying insects and bees which has huge potential to benefit humankind in the most surprising ways.

## 1.1 Background

A radio telemetry system for tracking wildlife and insects consists of three main components [1] as described below and is shown in Fig. 1.1. (*This research work focuses on the miniaturization of radio tags and therefore, the detailed description has been limited to the transmitter part only*.)

1) The transmitter tag

2) The radio receiver

3) The antenna system with associated cabling

The Transmitter is basically an RFID (Radio Frequency Identification) tag that is affixed to the test species. This could be active or passive depending on the requirements of the study. Active tags have a power source, i.e. a battery or a solar cell within the tag and they can be tracked to a far for distances. These telemeters are mostly operated at Very High Frequency (VHF) - 30MHz to 300MHz range and their circuitries consists of 4 prime components:

**1) A power source (battery or solar cells):** Battery (power source) is the main component which controls the operating life of the tag and since the transmitter electronics circuitry has been almost the same for all transmitter, it is the size and weight of the battery that governs the overall size and weight of the transmitter tag. For a smaller tag, the battery size also affects the operation range of the transmitter due to the limited availability of the substrate ground for the transmitting antenna.

**2) Electronics package (PCB and crystal oscillator):** The electronic package consists of the transmitter circuitry, crystal oscillators, antenna matching components, etc. all mounted together on the PCB. Again, for the smaller tag, this electronic package has a significant contribution to the total weight and size of the package.

**3) Transmission antenna**: Antennas affect the operational range of the tag and hence to optimize the range they are cut and designed to a specific length. Also, depending on the frequency to be transmitted proper impedance matching is done with the transmitter circuitry to obtain higher efficiency.

**4) Attachment method:** Depending on the test species, there are various kinds of attachment techniques available, such as neck collars for mammals and large birds, back harness with a leg strap for smaller birds, glue on for small insects, and many more.

The location of the test species could be located by tracking these mounted tags using airplane mounted or hand-held antennas and following the direction of beeps sound by the receivers. Another very convenient technique to track the species is using the triangulation method used in an automated tracking system as shown in Fig. 1.2. This requires three or more sets of antenna-receiver units to triangulate the location of the tag. Depending on the strength of the transmitted signal received by these receivers the distance of the tag from each receiver is calculated by using inverse $r^2$ and from there the actual location is determined by the common

intersection of the distance from all the receivers. This method allows more precise detection of the tag location (having errors within a few meters which makes it more suitable for tracking flying insects) and also features simultaneous detection of a large number of tags.


(a) (b) (c)

Fig. 1. 1. Components of radio telemeter (a) transmitter (b) receiver and (c) antenna pictures reproduced from [2]

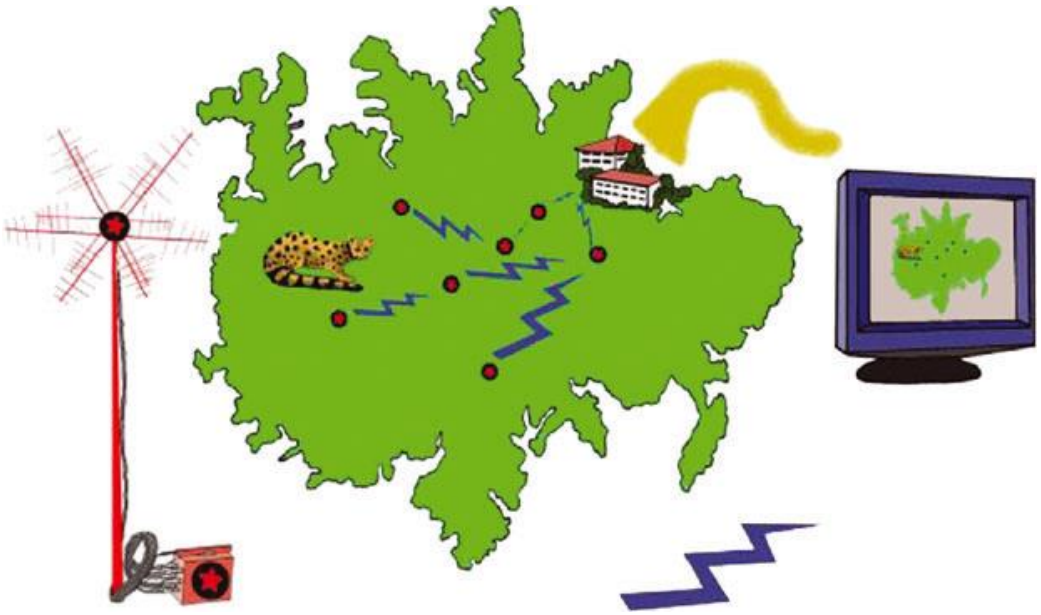


Fig. 1. 2. Triangulation technique to locate tag position using three or more antennas and receiver units. (Picture has been reproduced from Kays et al., 2011 [3])

There have always been concerns raised by various researchers regarding the effect of tracking devices on constraining species behavior and how these tags' weight

affects them over time. Further research has shown that in order to get correct data from the tagged species, without affecting their normal homing activity, the tag weight must not exceed 3-5% of the animal's weight [4, 5] and 10% of the insects' weight [6]. As per the literature, until now, the 200mg active telemeter has been used to track large insects and study their foraging behaviors. It is known that bees are good at carrying weight and could carry weight almost the same as their own weight. Therefore, efforts have also been made to use these tags to wirelessly track bumblebees and orchard bees weighing (200mg – 500mg) [7] to study their movement and space use while foraging. However, these tags weighed about 40% to 100% of bees weight and therefore telemeter attachment showed a significant effect on their activities including an increase in their rest time and a decrease in the number of flower visits. In order to successfully track these bees and tiny other flying insects, there is a need for a significant reduction of both size and weight of the active radio telemeter.

The current lightest active insect tag being commercialized by Lotek Ltd. [8] and ATS telemetry [9] weighs 130-150mg and has a dimension of 11mm X 3mm X 3mm. Like all other telemeter tags, this insect telemeter design also employs discrete components packaged over a PCB and uses a 3V lithium battery. The research proposed in the thesis shows a viable solution to shrink the telemeter size by over 50% and reduce the tag weight by 27% (95mg) by implementing the telemeter design completely on the ASIC which would provide a higher integration and scalable capabilities than the discreet components-based design. Further, the fast development of CMOS process technology, extensive prior work on Radio Frequency (RF) integrated circuit (IC) design, and implementation of RFID tag especially, passive tags on IC chip have laid a solid foundation for the realization of the VHF radio telemeter into ASIC. Fabricating the telemeter tag on the IC chips will also facilitate the benefit of lower power consumption and continued dimensional scalability of the tag which comes with the advances in every new generation CMOS process technology.

## 1.2 Motivation

A large amount of food supply will be required to meet the increasing demand of booming population growth in our planet and alongside, the diminishing bees and

other natural pollinators population due to the use of chemicals and pesticides in agriculture, climate change and expansion of agricultural area are leading to a potential global pollination crisis. The severity of the situation can be gauged by analysis done by researchers which estimates that there is almost 60% decline in the managed honey bee hives in North America since the 1940s [10], given the fact that 90% of one-third of the food that we consume are dependent on these pollinators, this scenario is raising a serious threat to our global food security. An analysis of the effect of pollinators population decline on the long-term trend of crop production, published by Marcelo A. Aizen *et al*. [11] revealed that it requires a 6% increase in cultivation area in developed countries and the worst, 8% in the developing countries to compensate the food supply deficit generated just due to the diminishing pollinators' population. This food supply deficit is contributing to accelerated deforestation and increased pressure on the natural and semi-natural ecosystem.

Entomologists and researchers around the world are working hard to understand the cause of the drastic decline in the pollinators population which involves studying their foraging activities, their response to a different environment, and their behaviors when subjected to various chemical pesticides and fertilizers. This demands a tiny and very light electronic device that can track their activities wirelessly in real-time and over large landscape and agricultural fields. This will help in developing agriculture protocols and chemicals that are pollinators friendly and protect their population to obtain sustainable crop production.

Moreover, advances in these electronics devices will take these tags beyond just tracking tiny creatures. It will allow employing bees as a biosensor to exploit their extraordinary sensing capability by training them to pollinate specific crops in particular regions for higher food yield [12] and to detect chemicals that would help in other areas like military, security, and locating land mines. The current ongoing project called "Insect Allies" supported by Défense Advanced Research Projects Agency (DARPA) where insects will be deployed with genetically modified viruses to edit the plant genes in already planted crops in the field to protect them from unprecedented natural threats like drought, frost, pathogens, etc. This has raised serious concerns among lots of research societies regarding the biosecurity and biosafety of such programs. This makes the insect tracking telemeter very crucial for reducing the danger of such biohazard so that these insects carrying the synthetic

virus could be traced in case they escape from the closed laboratories, greenhouse, or research facility.

Therefore, to synthesize better and pollinator-friendly pesticides and fertilizers which in turn will allow us to use both natural and man-made products for high productivity of best quality fruits and vegetables and to increase the crop productivity by training bees for pollination and to increase biosecurity of the advanced agricultural protocols developed to protect crops in the fields, miniaturization of insect telemeter is very important.

## 1.4 Research Objective

The prime objective of this research is to develop a miniaturized CMOS active RFID tag which unlike other RFID tags is capable to track and identify very small insects and bees without hampering their biological process over a large distance (up to 1km). To achieve this goal, the research follows the enlisted steps:

1. An investigation into the design of active VHF radio tag for wildlife and insect radio telemetry, and the latest development in the miniaturization of the telemeter to wirelessly track and identify small flying insects.

2. Design analysis and simulation of the smallest available VHF radio telemeter circuitry to understand the waveform required for tracking insects and to study the feasibility of the implementation of such telemeter device into ASIC to miniaturize the tag size for tracking small flying insects.

3. Exploration of the transmitter design using a digital approach without using passive components and crystal oscillators. Development of a new technique to generate extremely low duty cycle signals and employing the new methodology in the design of the VHF digital transmitter to generate burst mode signaling.

4. Fabrication of the transmitter circuit into ASIC in CMOS8RF 130nm process technology, followed by test board design, chip testing, and studying its performance in terms of frequency stability and power consumption.

5. Exploration of methods and techniques to simulate the circuit operating at a very high-frequency signal with an extremely low duty cycle as it has been a challenging task to simulate such kind of signal for a complete-time period due to time and huge memory constraints.

6. Design of the 8-bit code-based identification system to make the identification technique robust to frequency variation and investigation of proper modulation technique for transmitting code and using the carrier signal to find the location employing triangulation technique.

7. Implementation of the developed digital coded insect telemeter design into CMOS 28-nm 8HP process technology and study the frequency stability in terms of supply noise and Process Voltage and Temperature (PVT) variation and its effect on the telemeter performance.

8. Kit installation and getting familiar with the new process technology to redesign and fabrication of proposed digital 8-bit coded insect telemeter in TSMC 65nm process node.

9. Fabrication of the digital coded insect telemeter in 65nm technology, test board design, and telemeter chip testing for the very low duty-cycled FSK modulated burst mode signal generation.

10. Design of low quiescent current, power management unit for providing power supply from 1.55V battery to the digital telemeter core circuit at much lower voltage while compensating for the effect temperature and process variations on the on-chip oscillator frequency.

11. Fabrication of the final prototype circuit in TSMC 65nm technology node. Testing of the prototype chip to verify the performance of the insect telemeter with change in supply voltage and the ambient temperature.

12. An investigation into the lightweight packaging option for the ASIC chip over the battery to miniaturize the complete insect telemeter package.

## 1.5 Organization of the thesis

This report has been organized as follows:

**Chapter 2** This chapter presents an overview of the historical development and miniaturization trend in the VHF active radio telemeter. It also briefs on the presently available technologies and the technique being employed for studying very small insects like honeybees, etc. with their technical limitations in monitoring these creatures. The chapter also details the design analysis of the smallest VHF radio telemeter (200mg) tag available in the literature, its simulated waveform with adjusted design parameters, and discusses the feasibility of telemeter design realization on ASIC.

**Chapter 3**. In this chapter, a novel method to generate a low duty cycle signal is demonstrated. The technique uses a digital approach which proves suitable for the miniaturization of insect telemeter and is realized to achieve burst mode signal signaling for telemeter application. The circuit is designed without using any passive element and features complete implementation of the tag circuitry in ASIC. The design is implemented and fabricated in CMOS8RF 130nm process technology. The chapter also presents the test board PCB design for the fabricated chip testing in the laboratory and discusses experimentations and the test result of the QFN packaged IC chip.

**Chapter 4**. In this chapter, an 8-bit RF-coded transmitter design is proposed. The tag uses code for individual identification and the carrier signal strength is employed to track the location of the tag remotely. The design is implemented in 28nm 8-HPP process technology. The design is extensively simulated in nanometer IC design tool to study the performance in terms of Process, Voltage and Temperature (PVT) variation, and provide power supply noise analysis of the oscillator. Due to the very high fabrication cost of the 28nm process, the complete proposed digital telemeter was redesigned on TSMC 65nm process technology and the ASIC chip was fabricated and QFN packages for the testing. The chapter also discusses the PCB test board design for the testing and design verification of the fabricated chip in the lab and provides a detailed analysis of the experimentally measured results.

**Chapter 5**. This chapter demonstrates the final insect telemeter prototype circuit which consists of the new digital telemeter circuit presented in chapter 4, as well as the complete low-power Power Management Unit (PMU) developed to provide the right supply voltage rail for the ASIC digital telemeter core circuit from a single 1.55V (silver oxide battery ) power supply. The PMU is designed to produce the voltage rail for the digital circuit in a way that it adjusts its voltage level according to the ambient temperature to compensate for the effect of temperature variation on the telemeter performance. The design is implemented in TSCM 65-nm process technology and the circuit performance is analyzed in terms of process, temperature, and voltage variation along with a detailed study on stability and noise performance. The chapter presents the prototype testing and experimentally measured results of the DIP package fabricated against supply voltage and temperature variation. Moreover, the chapter also discusses the paper study for the telemeter packaging without using PCB to build the lightest telemeter package

**Chapter 6** In this chapter antenna design has been explored for the insect telemeter application. The chapter discusses the simulation and impedance matching of the electrically short antenna (ESA) for the telemeter application.

**Chapter 7** This chapter summarizes the contribution of this work and further outlines the direction for future work to make this insect telemeter design a real product.

# CHAPTER 2

# INSECT TELEMETRY OVERVIEW

## 2.1. Introduction

The rapid development of technology, expansion of cities, deforestation, climate change, etc, have endangered the life of many valuable species. Being aware of the importance of these species and in order to maintain the survival of these species humans started studying their behavior, movement, lifespan, food habits, the effect of various survival conditions, migration patterns, physiological and psychological patterns, etc. by tagging and tracking them. Rapid advancement in technology has facilitated tracking and study of diverse species and at the same time shrinking of tag size has remarkably increased the utility of tags and expanded the range of species being tracked. This chapter gives a brief insight into the historical development and miniaturization of the VHF radio telemeter over time and introduces the presently available small insects and bees tracking alternatives and the limitations and challenges posed by these approaches.

## 2.2. Development and Miniaturization in VHF Radio Telemetry

The study of animals by tagging them started a long time back. However, collecting data from the tagged animals had always been a difficult challenge. To retrieve the data, the animals had to be searched in their burrows and every other place where they were expected to live and many a time the animals were not found there. The whole process of collecting data became a time-consuming and tiresome activity, especially for the smaller animals. For the larger animals also, it got tedious to keep track of the species. The problem of recollecting data became quite evident in 1956-1957 while gathering data from the tagged woodchucks [14]. To solve this enduring problem of data recollection, researchers started exploring and working on real-time data acquisition.

The first Radio tracking tag for animals was developed by Cobert D. LeMunyan et al. [13] in the year 1959 after getting inspired by the work of Barr [14] and the work of Mackay and Jacobson [15]. In the year 1954 Bar had found that the information from the pilot in jet craft could be telemetered to the laboratory and recorded on devices.

The information from the pilot was converted to an electrical signal using a transducer for radio transmission using UHF modulated transmitters. Since the size and weight of these units were not suitable to use on animals, in the year 1957, Mackay and Jacobson developed an extremely small transmitter called the endoradiosonde. This tag when swallowed could be tracked down through the body and can be used to do in vivo animal experiments.

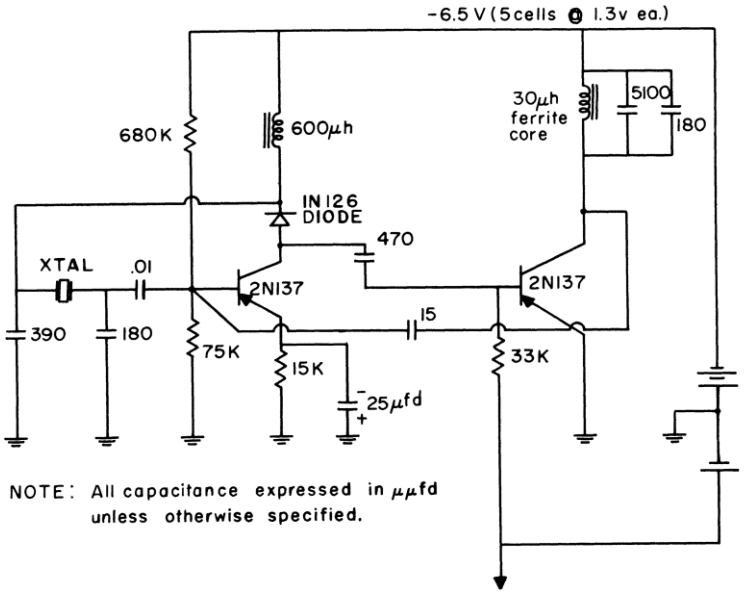



Fig. 2. 1. Schematic of the world's first wildlife VHF transmitter developed in 1959 as presented in [13 Fig.1].

Influenced by their work, Cobert D. LeMunyan et al created a first-ever transmitter that was capable of tracking the location of tagged, free-roaming animals in real-time. The original model was designed using one 2N137 transistor and used a mercury battery. In order to conserve power, the transmitter sent a pulsating signal. Crystal oscillator was used for the purpose of frequency stability; however, it introduced the problem of loss of range because of its limited current pulling capability. This issue was fixed by using an additional 2N137 transistor which acted as a class C amplifier. Fig. 2.1 shows the schematic of the transmitter circuit. The weight of the complete transmitter along with the power supply was 122.5 grams with a volume of 7.5cm X 4.0cm X 1.4cm. Since the transmitter was in the early development stage it suffered from several issues like a small operational distance range of 25 yards (~ 23m), viable only for the large animals due to the heavyweight of the tags, etc.

In the year 1963, W.W. COCHRAN and R. D. LORD [16] designed another transmitter that provided a great improvement in the size, range, life, electrical stability, and other important parameters. The transmitter was a single transistor-based, crystal-controlled oscillator with a tank coil which also acted as a dipole antenna. The schematic of the transmitter circuitry is shown in Fig. 2.2. The complete transmitter without batteries weighed approximately 10grams. In the transmitter variety of transistors could be utilized, however, the most extensively employed were 2N588 transistors, capable of handling power from around 1 mW to about 10 mW and 2N1023 transistors, which could handle power from around 2 mW to 50 mW.

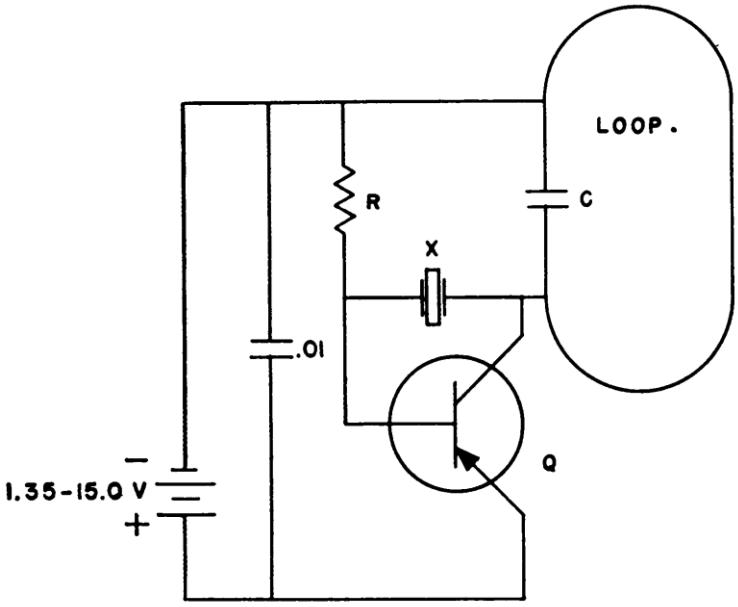



Fig. 2.2. The basic circuit of the transmitter circuit developed by W.W. Cochran and R. D. Lord as presented in [16 Fig. 5]

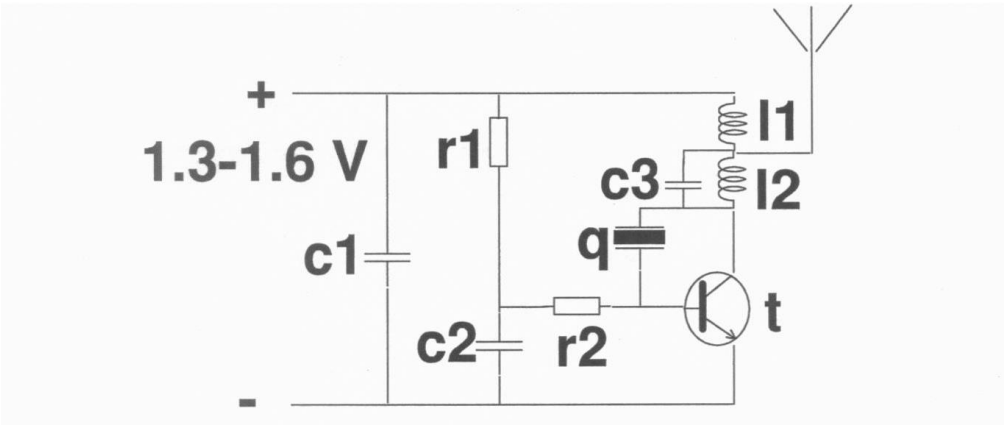



Fig. 2.3. The circuit used in 260mg (without power cell) telemeter designed by B.N. Daenzer in the year 1993 as illustrated in [17 Fig. 1].

Thereafter, another remarkable shrink in the telemeter size appeared in the year 1993 when B. Neaf Daenzer developed a new transmitter weighing around 260mg without the power cell and this was much smaller than the then commercially available smallest transmitter which weighted 500-650 mg [17] without battery. The lesser mass was achieved mainly by utilizing the smallest passive components for the surface mount technology and the smallest possible crystal but the basic transmitter circuit topology of this telemeter (shown in Fig. 2.3) remained the same as other heavier telemeters. The telemeter employed 120-140mm long antenna and had a detection range of about 300m in a dense forest to up to 1,000m in the open. The complete transmitter with the smallest battery available weighed 320mg and could be utilized to track animals weighing 7g or more.

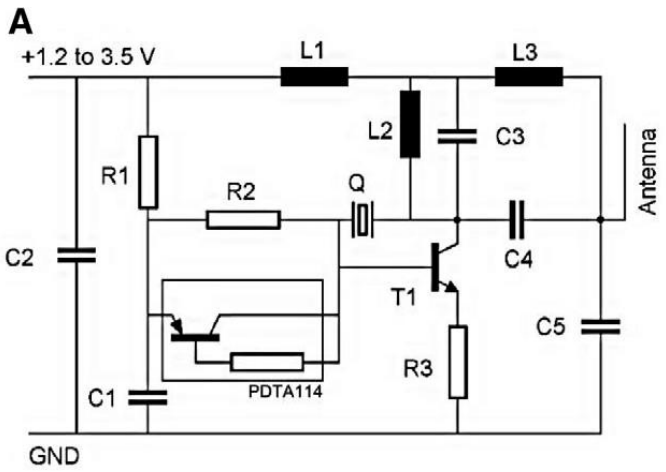



Fig. 2.4. The telemeter circuit of the smallest (200mg) VHF radio tag as shown in [18 Fig. 1(A)]

Thereafter, many further developments in designs followed, however, the technical limitation to track smaller species still prevailed until B. Neaf Daenzer along with other collaborators developed the ever-smallest active radio telemetry tag [18] in the year 2005. The tag has been commercialized by the company Advanced Telemetry Systems (ATS) [19] and consists of a 1.55V silver oxide battery manufactured by Sony, a 10 cm whip antenna. The transmitter circuitry uses a crystal oscillator, two bipolar RF transistors, and other passive components as shown in Fig. 2.4 to transmit a VHF signal pulse train with a very low duty ratio. All the components are mounted on a PCB and connect to the battery. The tag weighs 120 mg without battery and 200mg with the smallest possible battery. This smallest tag created a breakthrough by expanding the utility of the active VHF radio tag in the study of entomology and

facilitated the study of large insects like bumblebees, hornets, etc. The tag developed by B.N. Daenzer et al. is shown in Fig. 2.5.

It is quite interesting to note that the VHF radio telemeter size has gradually decreased for about 12,000 times in around 40 years' time span from 1963 to 2005, however, after 2005 there is only a 70mg reduction in the weight of telemeter in the period of last 16 years. This is because the tag size reduction has all along been achieved mainly due to the advancement in the surface mount devices and through the developments in the device mounting techniques. Further miniaturization in the tag size gets quite difficult with the same technique and in order to reduce the tag weight and size significantly, the VHF radio telemeter needs a new design approach. Fig. 2.6 Illustrates the miniaturization trend in active VHF Radio tag size over fifty-years' time span. The VHF radio tag weight reduced from 10g (without battery) in the year 1963 to 120mg(without battery) in 2005 enabling the tracking facilities for wide varieties of species as shown in the picture.

The idea to reduce the tag size by realizing the telemeter design on ASIC is explored in the coming chapters. Fig. 2.7 shows the vision of VHF tag, where the 120mg PCB circuit would be replaced with the 1-2mg ASIC and will be packaged over 80mg silver oxide battery to yield less than 100mg VHF radio telemeter for tracking flying insects and bees.

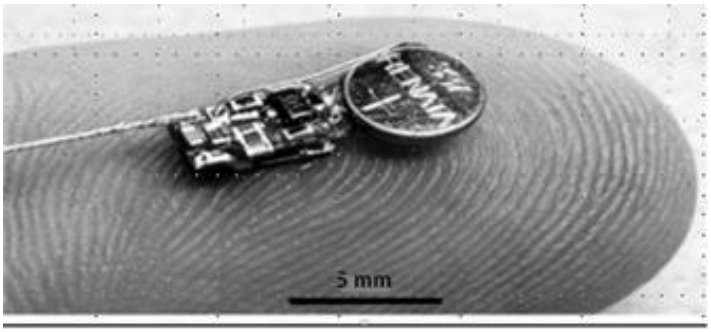



Fig. 2.5. The smallest active VHF telemeter tag developed by B.N. Daenzer et al. [18 Fig. 1(B)]

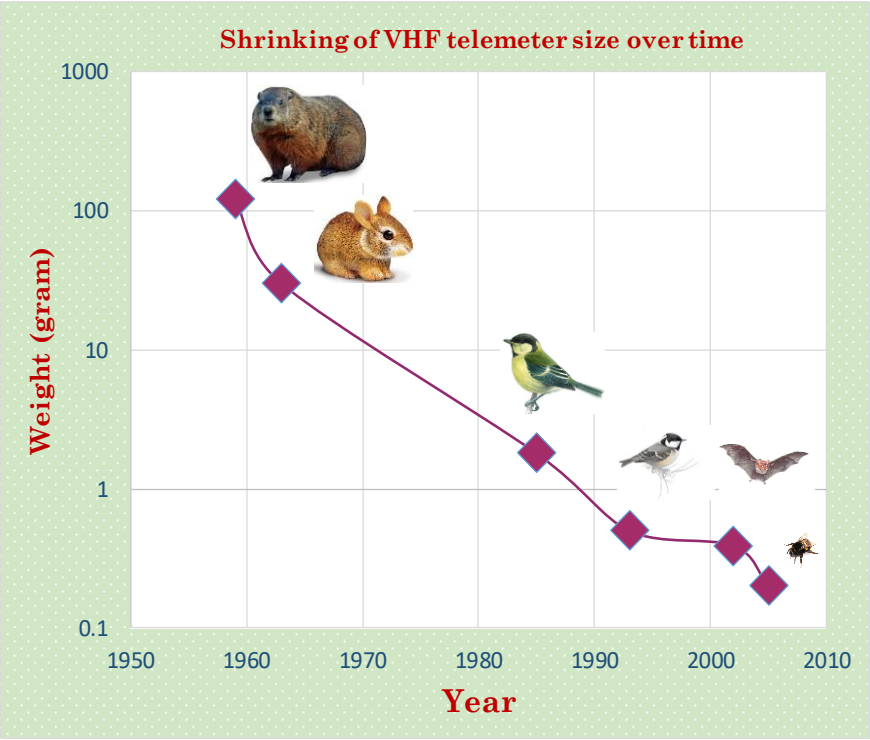



Fig. 2.6. VHF Radio telemeter size miniaturization trend over time.

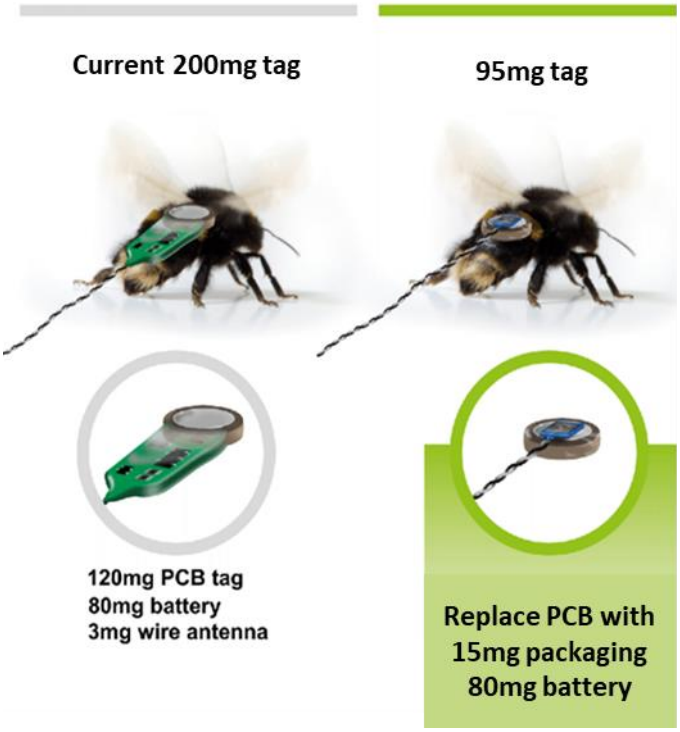



Fig. 2.7. The vision of the miniaturized 100mg active VHF telemeter consisting of ASIC chip mounted over the silver oxide 1.55V battery.

## 2.3. Present technological approaches and issues in tracking bees and small insects.

Because of their extremely small size, tracking bees has always posed a difficult challenge. Due to the growing necessity to study these species, various techniques like mark-recapture, feeder experiments, homing experiments and the interpretation of the bee dance, etc. have been employed to track their activities. However, acquiring the accurate behavioral data of these tiny creatures in their natural or agricultural landscape is still far from reality. This section briefs on the prevailing alternative methodologies employed to get an insight into the insects' world, and the technical limitations faced in the process.

### 2.3.1 Harmonic radar System

Radar technology could be applied for tracking small insects [20-22]. In this technique, a non-linear junction, such as a diode is mounted on the target that automatically sends a signal to the Radar System. The diode is small enough for small insects to carry them and it can be used and detected even without any battery at a distance of around one kilometer. However, the Harmonic Radar system faces serious limitations. Firstly, there is a high chance of false detection because the operating environment has materials made up of metals or alloys which might send the frequency response the same as the target. Secondly, individual identification is an important feature required to study these small insects. Since all the tags in this system work at the same frequency, it limits the remote individual identification. Thirdly, the frequencies used in harmonic radar are in the microwave range [23] and thus the signals get highly suppressed by vegetations and this greatly limits the tracking process.

### 2.3.2 Passive Integrated Transponders (PIT) tags

These PIT tags are basically Passive RFID tags and they do not have any power source of their own. These tags are primarily RFID transceivers which receive radio signals from the receiver, and this provides energy for the tag to send the information back to the receiver. It is an easy and cost-effective method to collect

detailed information about the foraging behavior of the bees [24,25] and other very small insects. Moreover, it provides the benefit of the unlimited number of codes for the tags which allows large numbers of recording at the same time, fast reading even through materials like wood, etc. These RFID transponders are so tiny and weigh around 3mg and are attached to the dorsal part of the bees.

For tracking the movement of bees, the receivers/scanners are placed near the entrance of the beehive. An artificial feeder is also designed a few meters away from the hive entrance. Since the operating frequency of these tags is 13.56 MHz, the reading distance of this technology is hardly 1m. The bee needs to enter the hive with specific alignment for detection and proper identification. Further, the whole setup is tried to be as close to the natural forging environment still the actual behaviors of bees in the natural environment could not be discovered.

### 2.3.3 Video Tracking

The advancements in image processing and computer vision techniques have facilitated the tracking of the target without needing any attachment. This methodology is called video tracking and is being used by various researchers to study the effects of pesticides on bees [26,27]. In this technique, individual honey bees are studied in a small arena which could be even the Petri dishes. Their movements are video recorded using a camera over a certain time and their total distance traveled within the arena and the rest time is analyzed employing automatic tracking video software [28].

The downside of this method is that it is a very time-consuming process and detecting the target's path becomes difficult under different environmental conditions. Implementing this technique to track small species like honeybees in the outdoor environment is very difficult due to the tiny size of the bees. Moreover, the capability of the camera to detect the motion velocity limits the application of the technique.

(a) (b)

Fig. 2.8. Picture showing prevailing technology for tracking bees and small insects. (a) tag attached on the bee for tracking using radar technology. [Picture credit: Andrew Martin] (b) a passive RFID tag on a bee [Picture credit: Tom Newman].

## 2.3 Design Investigation, Simulation, and Analysis of the Smallest VHF Radio Telemeter

In order to know the shape of the transmitted signal waveform from a VHF radio telemeter to track flying insects and bees, to understand the telemeter circuit functionality and behavior, and to study the weight and size miniaturization feasibility of such tracking devices by implementing the design into ASIC using CMOS technology, the smallest VHF radio telemeter circuit (weighing about 200mg) developed by B.N. Daenzer et al were investigated and analyzed using Cadence, Spectre tool. This section details its analysis, circuit modeling challenges, and simulation results.

The smallest VHF radio telemeter circuit as shown in Fig. 2.9 (a) is basically a crystal-based pierce oscillator [29] designed to transmit a signal burst at a nominal frequency of 148.5 MHz with an extremely low duty cycle. The circuitry consists of a crystal oscillator, 2 bipolar transistors and employs a number of passive components including inductors, capacitors, and resistors to control the duty cycle of the transmitted signal as well as for other purposes. In the circuit shown in Fig. 2.9 (a), C2 is basically a decoupling capacitor and grounds any ac signal coming from the source and inductor, L1 is for preventing the ac signal from the circuit feeding back to the source which is a 1.55V battery. Components L3, C4, C5 connected at the antenna terminal are basically matching elements to prevent the reflection of the signal from the antenna at the connecting point and provide efficient signal

transmission. In the transmitter circuit, R1 and C1 are the timing elements and determine the off-time duration of the transmitter. While the capacitor, C1 is charging the transmitter does not produce any oscillatory signal and no signal is transmitted. When the capacitor is charged it turns on the two bipolar transistors (as shown in Fig. 2.9 (a)) and the Barkhausen criteria for the oscillation is satisfied. This kick starts the crystal oscillator to generate a 148.5 MHz signal and in the meanwhile the capacitor, C1 starts discharging. The circuit oscillates until the capacitor, C1 is discharged through the crystal oscillator and thereafter the transmitter goes in the sleep state again until the C1 is charged up through the resistor, R1. In the telemeter circuit PDTA114, which is basically a PNP transistor with a resistance connected at the base is employed in the design to half the width of the signal burst while maintaining the same time interval between the bursts, this is to further reduce the duty cycle of the transmitted signal.

### 2.3.1 Telemeter Circuit Simulation Challenges

The 200mg VHF telemetry circuit (as shown in Fig. 2.9 (a)) was modeled to be simulated using a nanometer IC design tool. Four serious challenges were faced in the simulation process to achieve the exact simulated transmitter waveform with the assigned circuit parameter provided in the transmitter design. These challenges are discussed as follows:

1. One of the major problems faced was the appropriate modeling of a crystal oscillator (148 MHz) to filter out the right harmonic. The correct modeling of such crystals with very high-frequency oscillation is a complex process and the company keeps the "know-how" of the crystal oscillators as the trade secret for commercial reasons. Generally, crystals are modeled with a series-connected inductor ($L_Q$), capacitor ($C_Q$), and resistor ($R_Q$) [30,31], and a shunt capacitance ($C_o$) connected in parallel series-connected components as shown in Fig. 2.10. Here, $C_o$ is the static capacitance and constitutes the capacitance between the electrodes of the crystal oscillator, plus the capacitance for the crystal holder and the lead. To model the high-quality factor of the crystal, the value of the inductor is kept quite high. Crystal oscillators have a set of resonating frequencies comprising fundamental and its odd harmonic frequencies. For frequencies ranging up to around 30 MHz crystal's fundamental frequency is used whereas its

overtones are utilized for higher frequencies. Therefore, for a telemetry circuit where crystal oscillates at a frequency of 148.5 MHz, which is almost 3 times the fundamental resonant frequency of the crystal oscillator, L2 and C3 [in Fig. 2.10 (a)] are employed to filter and favor these 3rd harmonics. This all together enhances the circuit's complicacy and simulation difficulties.

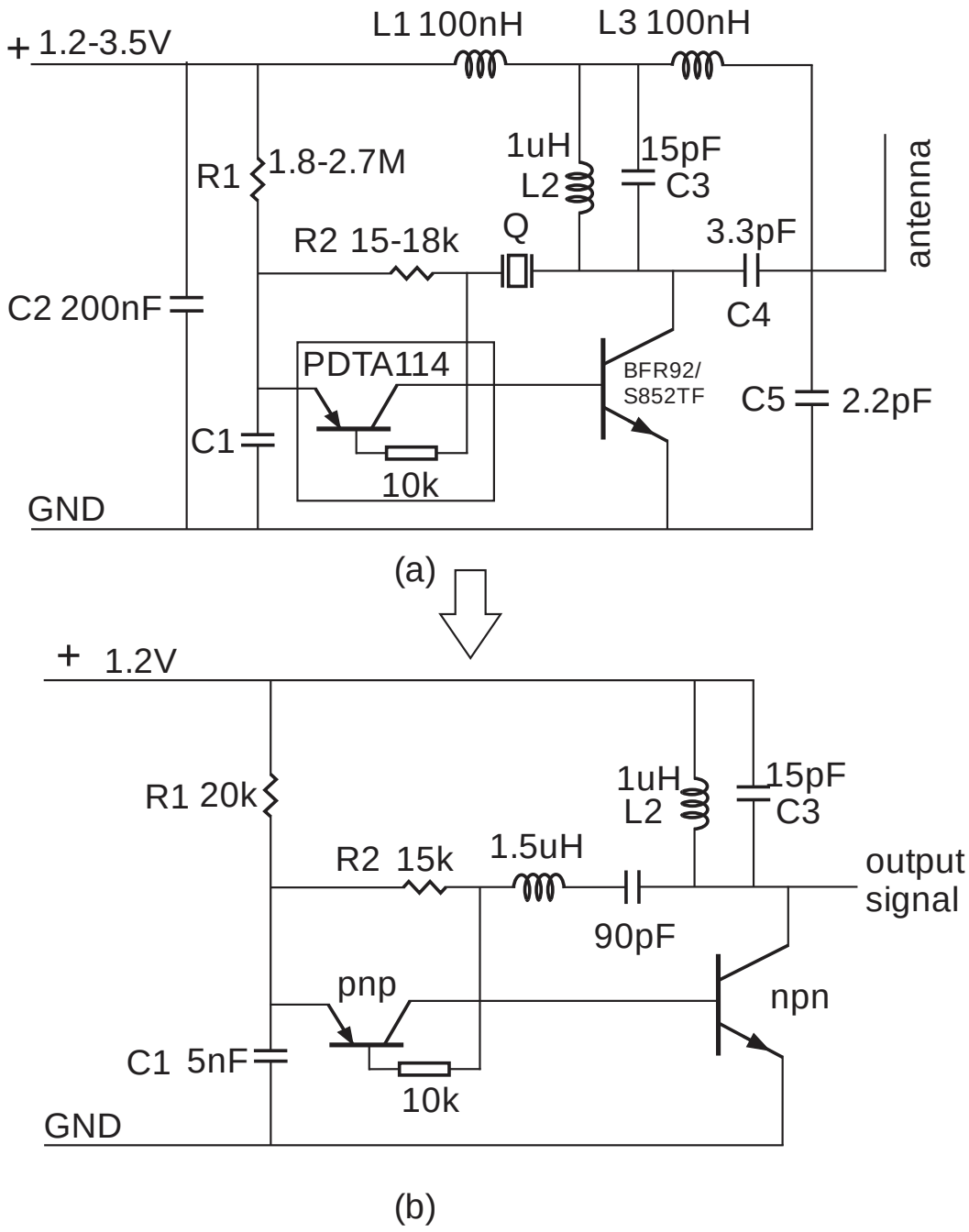



Fig. 2.9 Schematic of (a) the transmitter circuit of the 200mg tag and (b) simplified transmitter circuit model to achieve low duty cycle bust signal simulation.

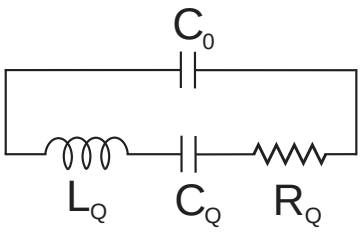



Fig. 2.10 Crystal model

2. The second challenge faced was the time and memory constraints for the one-cycle simulation of the low duty-cycled burst mode signal. The transmitter waveform is supposed to have a signal burst of width 15-20ms after an interval of 1000-1200 ms and in order to observe one complete cycle of the signal the total simulation time needs to be around 1200ms, however, at the same time, detection of 148.5 MHz signal requires extremely small time-step which is less than 100 pico-second. This means to detect the 148.5 MHz, 15-20ms wide burst signal in a 1-2 second time frame the simulation has to be run for 1-2 second with few pico-second timesteps. This requires enormous time (several months) and an extremely huge amount of memory (several Terabits) in the system to save the data points. Moreover, the problem gets worse when the correct modeling of the crystal to pick the right harmonic is not known. Therefore, circuit simulation for one-time period of the signal with the assigned parameters of the elements and with an extremely small time-step is not possible, and therefore the strategy cannot be employed to design a telemeter circuit on ASIC. In order to understand the transmitter waveform, the circuit was simulated with lots of adjustments in the component's parameters. The timing elements (capacitance, C1, and resistance, R1) value were scaled down to reduce the burst signal width and the time interval between the bursts. Other elements involved for matching the antennas(L3, C4, and C5), decoupling capacitor, C1 and inductor, L1 used for stopping the noise being fed to the battery were removed to reduce the node points in the circuit and to increase simulation speed.
3. The third challenge was due to not having the same RF transistor model parameter used in the telemeter for the simulation in the nanometre IC design tool. The transistors S852TF and BFR92 used in the circuit were not available for the simulation and the PDTA114 datasheet does not exist online either. So, for the simulation general model of NPN and PNP transistors were used instead of S852TF/BFR92 and PDTA1114 respectively. The electrical parameter values for these transistors are given in appendix-A.

4. The fourth major challenge in the simulation of the telemeter circuit was detecting the circuit oscillation. To make an oscillator circuitry work one needs to do lots of manipulation with the circuit to come up with the right component's requirements. Given the inconvenience with the simulation due to time and memory constraints, and not having the right model for the 148.5 MHz crystal oscillator, tuning the circuitry and achieving the right component parameter had been a very difficult challenge. Due to the low duty cycle nature of the signal, the oscillation burst signal did not appear immediately and in fact, sometimes it required a lot of time for the burst to appear. This made it difficult to know if the circuit has been tuned right to produce the oscillation burst or not. Values of various components in the circuit were varied by trial and error method until the burst mode oscillation was observed. This trial and error on low duty cycle burst signal made the process of tuning the circuit extremely tedious.

### 2.3.2 Schematics of the simulating circuit.

Due to the above challenges, the telemeter circuit parameters were adjusted for the simulation. Fig. 2.9 (b) shows the modified schematics. Here, the crystal is modeled using a series inductor and capacitors, LC network was simplified by removing the filtering components (C2 and L1) and the antenna matching elements, (L3, C4, C5) from the transmitter circuit. Moreover, values of other parameters were reduced many fold to reduce the overall time period of the output signal. These parameter values were varied and thousands of simulations were performed to understand the circuit performance and achieve the burst signal waveform.

**Parameters used:**

1. R1= 20k Ω, R2=15k Ω, C1=5nF, L2=1uH, C3=15pF
2. In place of the crystal, a series-connected inductor and capacitor with values L=1.5uH and C= 90pF were employed.
3. Parameters of the employed NPN and PNP transistors are given in Appendix A.

### 2.3.3 Simulation Results and Discussion

Fig. 2.11 shows the transient waveforms of the simulated transmitter circuit. At the input supply voltage of 1.2V, timing capacitor (C1) charges from 190mV to 0.6Volt and then discharges at a faster rate. During the discharge time of the capacitor, the transmitter produces the signal burst and therefore the width of the burst signal is the same as the discharge time of the capacitor, and the interval between the signal burst is the same as the charging time of the capacitor. Lowering the value of this capacitor reduces both the time interval and the width of the signal burst. Under the above conditions, the time period of the output waveform was measured to be 68.6$\mu$s with a duty ratio of 0.32. The measured average current drawn from the supply is 1.18mA while the circuit utilized 50$\mu$A current during the sleep mode and 3.6mA during the on-state mode while the bursts were generated. With this, the average current for the duty cycle of 0.008 is calculated which comes out to be 68.48$\mu$A. Fig.2.12 plots the signal waveform inside the burst. The signal oscillates from 80mV to 2.2V with a DC offset of 1.2V. Interestingly, here the frequency inside the burst is observed to be 84 MHz, which is completely different from the resonating frequency of the circuit employed in place of the crystal. The reason for such behavior could not be understood. It seems like the transmitter output is oscillating at some different overtone of the modeled crystal frequency and filtering the right harmonic is itself a difficult task.

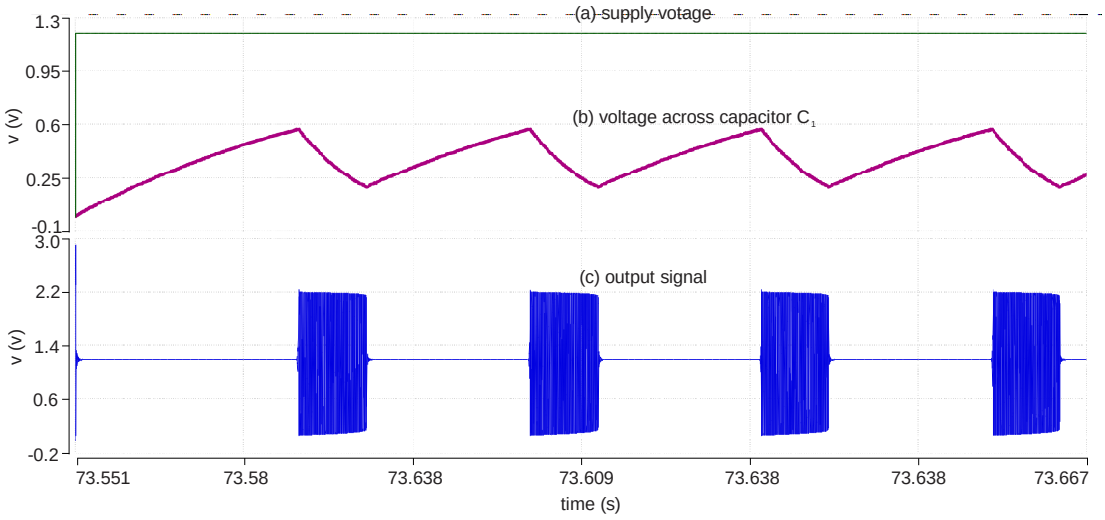



Fig. 2.11 Transient waveform of the modified transmitter circuit. The output waveform has a duty cycle of 0.32.

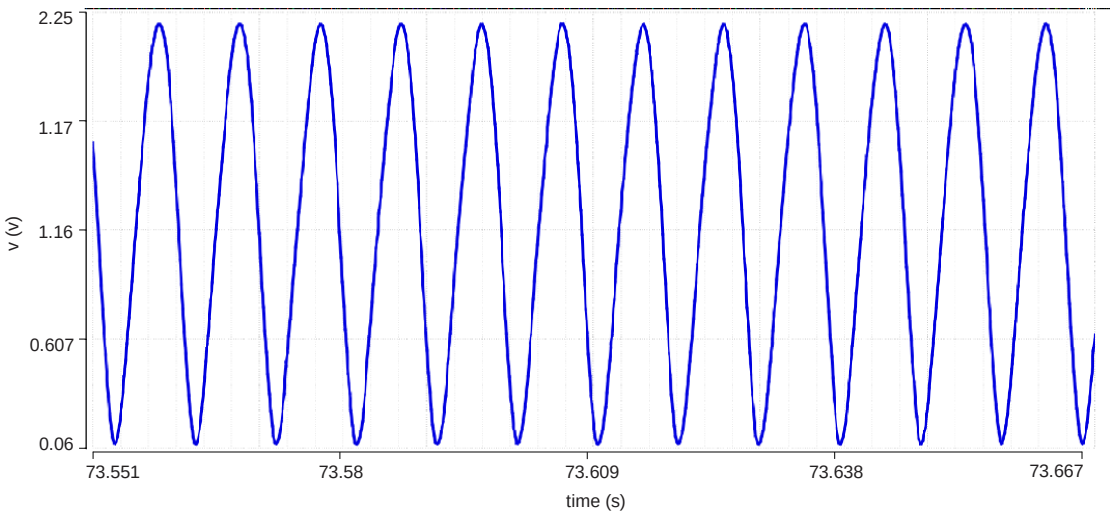



Fig. 2.12 Zoomed in view of the signal inside the burst waveform.

## 2.4 Conclusion

The chapter provided a technical overview of the developments in the miniaturization of VHF radio transmitter tags over the period. It is evident that the basic design of the tag has not changed much. Since its inception, all the major shrink in the size and weight of the tag have been acquired mainly by modifying the attachment techniques, development of miniaturized Surface Mount Technology (SMT) devices and the battery size. Moreover, no further size reduction has occurred for around two decades. To track smaller insects some alternative techniques are being employed as presented in the chapter. However, all these alternative techniques have their technical limitations and none of them are capable of real-time tracking of small insects while providing individual identification and home range analysis at the same time.

The chapter also investigated the design of the smallest commercially available VHF radio tag, (200mg). It is seen from the initial analysis that the simulation of such an oscillator is a challenging task, especially when there is no literature available to give an insight into the complex oscillator circuitry in terms of the circuit parameters and the resonance frequency. Simulating the circuit using the trial and error method is tedious and it is difficult to obtain optimization using this process.

The design analysis of the telemeter showed that in order to detect insects we need a burst mode signal with a very low duty cycle to conserve power and extend the battery life. To obtain a longer time interval i.e. of a few seconds between the signal bursts and to get a reasonable width of the burst signal for proper remote detection, the timing components (RC) need to be quite large. These large passive components require a larger area on the silicon chip and defeat the main purpose of the ASIC implementation to miniaturize the tag.

One approach to solve this issue could be by reducing the size of the components which will increase the operating frequency of the device and will also reduce the time interval between the burst signals. However, the downside of this method will be increased power requirement and smaller battery life since the sleep interval between the burst mode gets reduced. Moreover, a higher frequency has a smaller wavelength and hence suffers more scattering in the environment. This reduces the operating distance of the tag and also it makes the application of the triangulation technique difficult to detect the tag's location.

Therefore, further research to reduce the size of the transmitter circuitry while obtaining similar output waveform explores in the direction of digital circuit design which would be able to feature both individual identification and home range analysis to provide unprecedented tracking of very small insects and pests.

# CHAPTER 3

# LOW DUTY CYCLE GENERATION AND BURST MODE SIGNALING

## 3.1 Introduction

Duty cycle is defined as the portion of the on-time of a system or a signal to the total time-period of the system or signal respectively [32]. It is generally expressed as a ratio or percentage. Duty cycle as the ratio is expressed as follows:

$$D = \frac{T_{on}}{T_{on} + T_{off}} \tag{3.1}$$

Here, $T_{on}$ and $T_{off}$ are the on-time and the off-time of the signal respectively. $T = T_{off} + T_{on}$ is the time period of the signal and D is the duty cycle. So, if the duty cycle is 10% or 50% then it means that the signal is on for 10% and 50% of the time respectively as illustrated in Fig. 3.1.

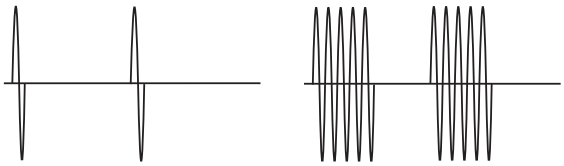



Fig. 3.1. 10% and 50% duty cycle of the system.

In the field of electrical or electronics, it is frequently needed to control the power delivery and regulate voltage through a variety of electrical circuitries. This could be achieved by using signals with different duty cycles. The duty cycle of a signal has great application in the PWM (pulse width modulation) which provides a low-cost and efficient power switching solution to control a variety of devices. The utility of the duty cycle could range from controlling the speed of motors to optimizing the performance of some circuitry on ICs. One of the important advantages it offers is the facilitation of the low power consumption goal. Since, in a CMOS circuitry for a signal with frequency f, voltage V, transistor capacitance C, and duty cycle D the average power dissipated is given by

$$P_{avg} = C * V^2 * f * D \quad (3.2)$$

It could be seen from (3.2) that the lower the duty cycle, the lower will be the average power consumption. This concept has also been heavily utilized in the tracking of wildlife using active RFID tags. wherein, signal bursts are transmitted for a certain duration after a fixed interval of time to locate the position of the species. The on-time of the burst is decided according to the capability of the receiver to detect the signal. For example, if it is a manual tracking system then the width of the burst needs to be around 10-30ms, however, for a computerized tracking system, few milliseconds of burst windows are also detectable. Further, the dead time intervals of the tags are optimized depending on the type of animal being tracked and are kept large enough to detect the observable movement of these beings.

Here, in this chapter, a new technique to generate a low duty cycle signal has been presented and is further employed to produce low duty cycle VHF signal burst for insect telemetry. The design uses a digital approach and employs simple logic gates and counters to obviate the need for passive elements. This facilitates easy implementation of the telemeter circuitry into ASIC and proves to be the most viable solution for telemeter miniaturization. The transmitter design is realized in IBM CMOS8RF 130nm process technology and the packaged fabricated chip is tested, and a detailed analysis of the experimentally measured result is presented in the chapter.

## 3.2 Generation methodology for low duty cycle

There have been several methods employed in the past to generate various duty cycles. One of the simplest and the most common method is employing multivibrators and among them, the 555 timer circuit [33] is the most frequently used. It comprises a voltage divider circuit consisting of 3 equivalent resistors, two comparators, a flip-flop, a transistor, and a driver. The circuit operates in monostable mode and when it enters the unstable state it produces one shot of pulse and then returns to the stable state. It can generate a range of duty cycles and has been used in various applications like an electronic metronome, infra-red firefly, etc. The main disadvantage of 555 timer circuit is that the use of passive components makes it unsuitable for the miniaturization when the area and size is the prime parameter.

Another method to generate the low duty cycle could be by using counters followed by reset circuitry [34]. In this, the predetermined time is counted using flip-flops, and then reset circuitry generates the required pulse. Again, the need for reset circuitry incorporates the use of passive components, which when implemented in ASIC increases the total chip area.

Also, there are works done even to generate programmable duty cycle [35] using voltage-controlled duty cycle generator (VCDCG), low pass filter (LPF), analog to digital converter (ADC), and operational transconductance amplifier (OTA). This circuit can generate a user-defined duty-cycle signal from the input signal of any duty cycle and is designed mainly for the on-chip application. It employs several devices requiring higher power and in no way suitable for use in telemetry applications.

For the telemeter application, the off-time of the signal transmission is kept quite large compared to the on-time. The operating principle of the conventional VHF Radio telemeter, especially the smaller tags, is based on the pierce oscillator, and the low duty cycle is achieved by using large passive components to control the off time of the transmitter.

From the thorough literature search, it was found that the conventional methods for the generation of duty cycle involved the use of passive components or circuitries which will require larger space on the silicon chip, and hence their direct implementation on the ASIC chip will not serve the purpose of miniaturization of the VHF tag.

## 3.3 Proposed Circuit for Low Duty Cycle Burst Mode Signaling

Fig. 3.2 shows the block diagram of the low duty cycle (LDC) burst-mode signal generator/transmitter circuitry. It comprises a Voltage-Controlled Oscillator (VCO), series of frequency divider flip-flops (FD), seven input AND logic Gate, to generate the low duty cycle signal. Further, this low duty cycle (LDC) signal is ANDed with the output signal of the VCO to get the burst of signals appearing at the predefined interval of time. In this method, a clock signal of frequency $f_0$ is generated from the VCO by using the Vcontrol pad as shown in Fig.3.3 and is fed to the series of frequency dividers (FD) which are basically divide-by-two ripple counters. These FDs successively halves the original frequency $f_0$, thirteen different times. The final

frequency achieved by this division is $\frac{f0}{2^{13}}$ which is about 16.1kHz, for the original frequency ($f_0$ =132MHz) (See Table 3.1, the 6th. Column, the first row, and the last row to understand how the frequencies are reduced) In Table 3.1 the output from all thirteen Frequency Dividers is shown. In this, column 1 is the identifier of all the frequency dividers. The frequencies $f_0$, $f_1$,… $f_{13}$, are identified as 0,1,2..,13 respectively in column 1. This Table is actually used to show how one can achieve the lowest duty cycles. The first four columns were used to generate low frequencies, where the fundamental/reference frequency ($f_0$) of the ring oscillator was 3.2MHZ and the last four columns were used for the fundamental/reference frequency ($f_0$) is 132MHz.

In Fig. 3.3 V_CONTROL pad of the VCO circuit controls the current through the five stages of the ring oscillators, which in turn increases or decreases the reference frequency of these five-stage ring oscillators. In Table 3.1, the second, third and fourth columns show the frequency, time period, and also one-half of the pulse time of various signals coming out from each of the thirteen frequency dividers. Our circuit is designed to have all the outputs from the 7$^{th}$ FD to 13$^{th}$ FD, and then fed through a 7-Input AND Gate (see Fig. 3.2), when that happens, we get a signal from the output of that "7 Input AND gate". This signal has a pulse width of ½ the time period of the $f_7$ signal, which is $T_7$ and it repeats at a time interval, $T_{13}$, which is the period of the signal that comes out of the 13$^{th}$ FD. Therefore, the duty ratio will be exactly equal to ($0.5T_7/T_{13}$). This value of the duty ratio is close to 0.0078. This is the way we have generated the Low Duty Cycle (LDC) signal. The timing diagram of this 7-input multiplication operation, which is shown in Fig. 3.1, is demonstrated in detail in Fig. 3.4. This Low Duty Cycle signal is then multiplied with the 3.2MHz or 132 MHz signals tapped from the output of VCO (reference/fundamental signal ($f_0$) for getting the burst mode periodic signals. Approximately, 20 $\mu$sec and 485nsec pulse width should be observed when the reference frequencies are 3.2MHz and 132MHz respectively. This data is shown in Table 3.1 in blue and green colour. In both cases, the duty cycle will be close to 0.0078. The output of the "2 Input AND Gate" then goes through the 4-stage tapered CMOS inverters to drive an 8pf load, which is an over-approximation of the whip antenna [36] which would be used. In reality, the loading capacitance will be much less than 2pF for the whip antenna.

Another alternative way to generate a low-duty cycle bust mode signal using a 7-input NAND gate followed by a NOR gate, instead of using AND logic gates. In this

case, signals passed through the NAND gate first generate an extremely high duty cycle signal instead (0.9922), and then this signal with $f_0$ (see figure 3.2) when followed through NOR logic gate, produces low duty cycle burst mode signal. Unlike generation of the low duty cycle signal using AND logic, in this case, the signal inside the burst will have frequency $f_0$ but with 180 out of phase. This does not affect the function of the tag, on the other hand, this approach would further reduce 4 transistors in total in the burst modes signal scheme and hence will reduce the power and enhance the time response to some extent.

### 3.3.1 Telemeter Circuit Design and Simulation Consideration

For the VHF telemetry application especially for tracking small insects, the on-time of the system requires to be around 14ms for the proper detection of the tags by the audio tracking receivers. VHF tracking receivers could also detect the tags with on-time of around 3ms to 4ms without audio tracking. The off-time of the tag could be 1-2 seconds depending on the speed of the flying insect, and therefore duty cycle of around 0.008 is chosen. Due to the nature of the very low duty cycle signal burst in which very high-frequency signals are transmitted after long time intervals, various simulation difficulties were faced. To detect very high-frequency signal (like 132MHz or 150MHz) by the simulator during transient simulation requires a very small time step size (less than 100 peco-sec) and since these bursts appear after a very long time interval (1s to 2s) the computer requires to store huge data (several Terabyte) and too much time (around one year) to simulate the complete one time period of the waveform. Therefore, due to the time and memory constraints, the design was scaled down to achieve the same duty ratio but with a much smaller on-off time period by using 13 FDs (scaled-down version) instead of 28 FDs required (for achieving around 1.79s at $f_0$=150MHz) for the real telemeter design implementation.

Moreover, the frequency of the transmitted signal in the 200mg telemeter is generally around 48MHz to 167MHz in the VHF range, and hence clock signal's frequency $f_0$ is chosen to be 150MHz for the simulation. However, while testing the fabricated chip in the lab, due to the non-availability of measuring equipment in that frequency range, the fabricated circuit was tested at 132MHz and 3.2MHz.

#### Simulation

The design was implemented in CMOS8RF, 130nm process technology. The circuit schematic was simulated using a nanometer IC design tool. The post-layout

simulation of the circuit was also done by including the parasitic components extracted from the design layout by PEX tool. Interestingly, a huge difference was noticed between the pre and post-layout simulation results. In the schematic simulation, 150 MHz was obtained at the supply voltage of 0.6 volts and control voltage of 425mV and it draws the average current of 5.56$\mu$A while consuming 4.9$\mu$A during the sleep mode. However, in the post-layout simulation, at the above the

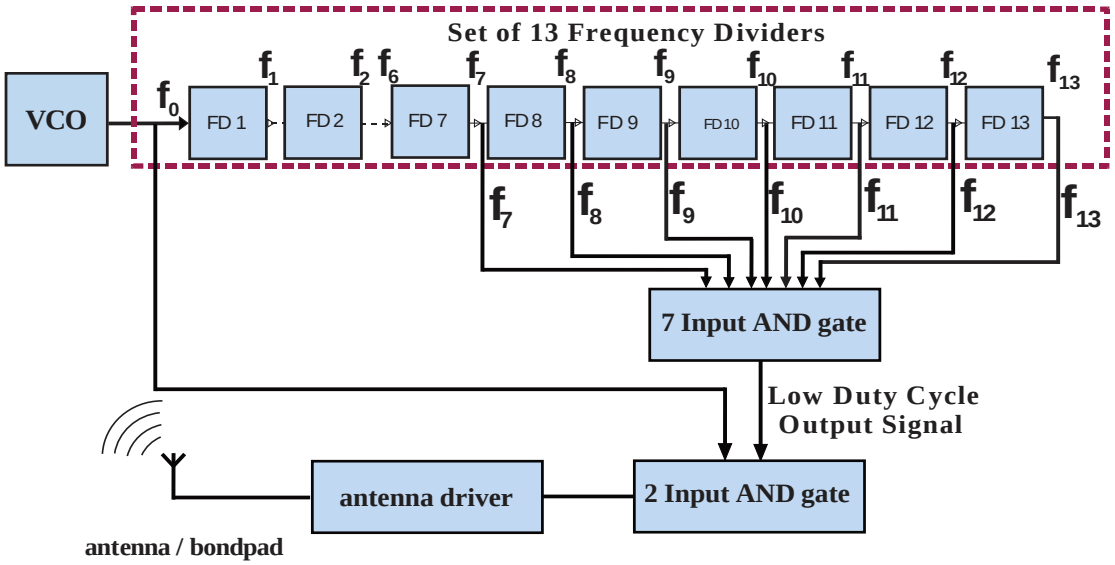



Fig. 3.2 Schematic showing the generation of low duty cycle using frequency dividers and its application in producing burst mode signaling.

Table 3.1

The frequency, time-period, and pulse duration of signals output from a cascade of 13 frequency dividers (FDs) for a 132MHz/3.2MHz input reference signal

| VDD=0.38V V_Control=0.31V | | | | VDD=0.6V V_Control=0.34V | | | |
|---|---|---|---|---|---|---|---|
| At $f_0$=3.2MHz | | | | At $f_0$=132MHz | | | |
| FDs | Freq(Hz) | T(sec) | $T_{PULSE}$ (sec) | FDs | Freq(Hz) | T(sec) | $T_{PULSE}$ (sec) |
| 0 | 3.20E+06 | 3.13E-07 | 1.56E-07 | 0 | 1.32E+08 | 7.58E-09 | 3.79E-09 |
| 1 | 1.60E+06 | 6.25E-07 | 3.13E-07 | 1 | 6.60E+07 | 1.52E-08 | 7.58E-09 |
| 2 | 8.00E+05 | 1.25E-06 | 6.25E-07 | 2 | 3.30E+07 | 3.03E-08 | 1.52E-08 |
| 3 | 4.00E+05 | 2.50E-06 | 1.25E-06 | 3 | 1.65E+07 | 6.06E-08 | 3.03E-08 |
| 4 | 2.00E+05 | 5.00E-06 | 2.50E-06 | 4 | 8.25E+06 | 1.21E-07 | 6.06E-08 |
| 5 | 1.00E+05 | 1.00E-05 | 5.00E-06 | 5 | 4.13E+06 | 2.42E-07 | 1.21E-07 |
| 6 | 5.00E+04 | 2.00E-05 | 1.00E-05 | 6 | 2.06E+06 | 4.85E-07 | 2.42E-07 |
| 7 | 2.50E+04 | 4.00E-05 | 2.00E-05 | 7 | 1.03E+06 | 9.70E-07 | 4.85E-07 |
| 8 | 1.25E+04 | 8.00E-05 | 4.00E-05 | 8 | 5.16E+05 | 1.94E-06 | 9.70E-07 |
| 9 | 6.25E+03 | 1.60E-04 | 8.00E-05 | 9 | 2.58E+05 | 3.88E-06 | 1.94E-06 |
| 10 | 3.13E+03 | 3.20E-04 | 1.60E-04 | 10 | 1.29E+05 | 7.76E-06 | 3.88E-06 |
| 11 | 1.56E+03 | 6.40E-04 | 3.20E-04 | 11 | 6.45E+04 | 1.55E-05 | 7.76E-06 |
| 12 | 7.81E+02 | 1.28E-03 | 6.40E-04 | 12 | 3.22E+04 | 3.10E-05 | 1.55E-05 |
| 13 | 3.91E+02 | 2.56E-03 | 1.28E-03 | 13 | 1.61E+04 | 6.21E-05 | 3.10E-05 |

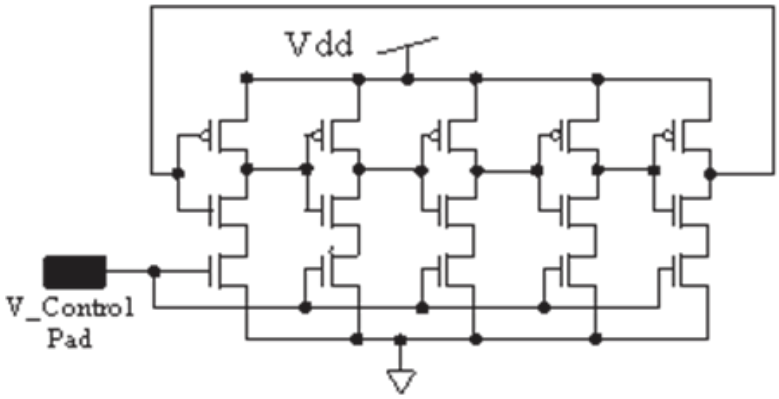



Fig. 3.3 The Voltage Control Oscillator (VCO) using 130nm CMOS for generating the 150MHz/132MHz/3.2MHz Fundamental/Reference frequency ($f_0$).

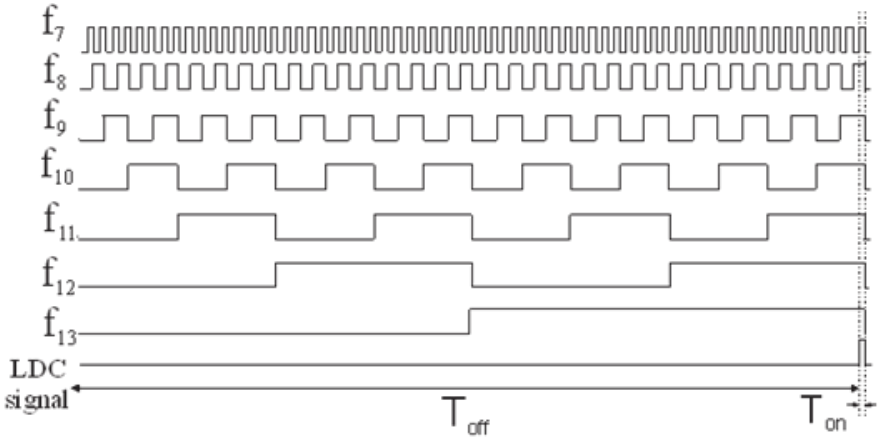



Fig. 3.4. Generation of the low duty-cycle (LDC) signal using $f_7$ to $f_{13}$. The output signal is high only when all the signals are high at the same time otherwise it is low.

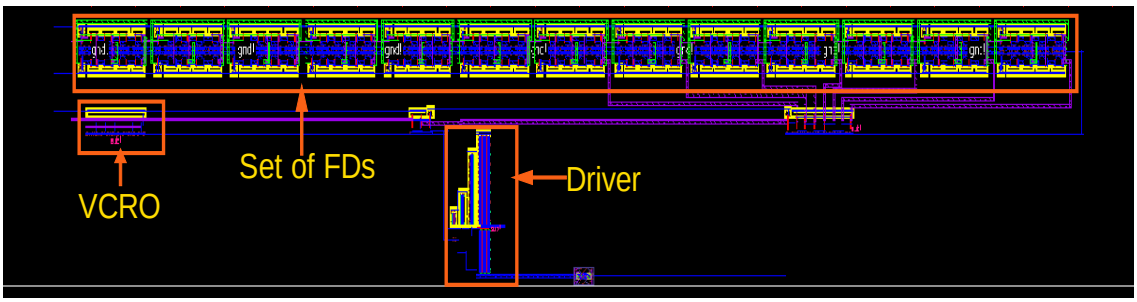



Fig. 3.5. The layout of the proposed digital VHF telemeter circuit in 130nmCMOS process occupying an active area of 0.028-mm$^2$.

supply and control voltage, the oscillator frequency reduces to 79 MHz which is nearly half of the pre-layout simulation frequency. In the post-layout simulation, the clock frequency of 150 MHZ is achieved at the control voltage of 510mV and the average current measured is 9.6 $\mu$A. It is observed that the average current of the design is nearly similar to the sleep mode current which is 9.5 $\mu$A in the post-layout simulation and this is mainly because of the low duty cycle of the transmitter circuit.

### 3.3.2 Critical Design Parameters

One of the most important design criteria for making this circuit to work and to have a well-defined value of duty ratio is described in Fig. 3.6 and also in Table 3.1. The time when $f_{n+1}$ is falling, that time should exactly match with the falling edge of fn. This is shown in Fig. 3.6(a). Normally, $f_n$ is double in value than $f_{n+1}$ or equivalently, $2T_n=T_{n+1}$. But practically, we have the falling edges of $f_{n+1}$ may not match with the fn. This is also shown in Fig. 3.6(b). There is an offset in time, which we call Δi, this parameter is also described in Fig. 3.6(b), Where, i represents various falling edges of the continuous signals $f_n$ and $f_{n+1}$. We have collected various values of Δi [i=1,2,3…..K], where K is the largest number of samples that we can collect through simulation. After that, we took the average values of all these Δi (let us call that average value α) to understanding how much offset we can have in our duty cycle value. We also calculated the standard deviations, $\sigma_\Delta$. This variation occurs due to the FD delay and variations due to the power supply noise. In order to have a solution for a well-defined duty cycle, which will have a constant value independent of $\alpha$, $\sigma_\Delta$, and process variation, we need the shadow of the blue region within the $(T_{n+1}/2)$ region, which is shown in Fig. 3(b). Shadow is shown by the red shaded region. Therefore, to generate a consistent duty ratio that will be independent of process variation and power supply fluctuation, with 99.99% confidence level, one should have the following criteria.

$$\alpha + 3\sigma_\Delta < (T_n/2) \tag{3.3}$$

On the other hand, one will not have a consistent value of duty ratio, when $(\alpha + 3\sigma_\Delta)$ satisfy the following equation below,

$$(T_n/2) < \alpha + 3\sigma_\Delta < 2(T_n/2) \tag{3.4}$$

There will be no burst mode signal under the following condition which is shown in (3.5) below

$$\alpha + 3\sigma_\Delta > 2(T_n/2) \tag{3.5}$$

The condition as described in (3.5) is a very unstable condition. Under condition (3.5) one may see burst mode signals, but it will not be periodic. And it can be fully erratic. The application for such erratic random jitter dependence solutions has not been investigated in this thesis.

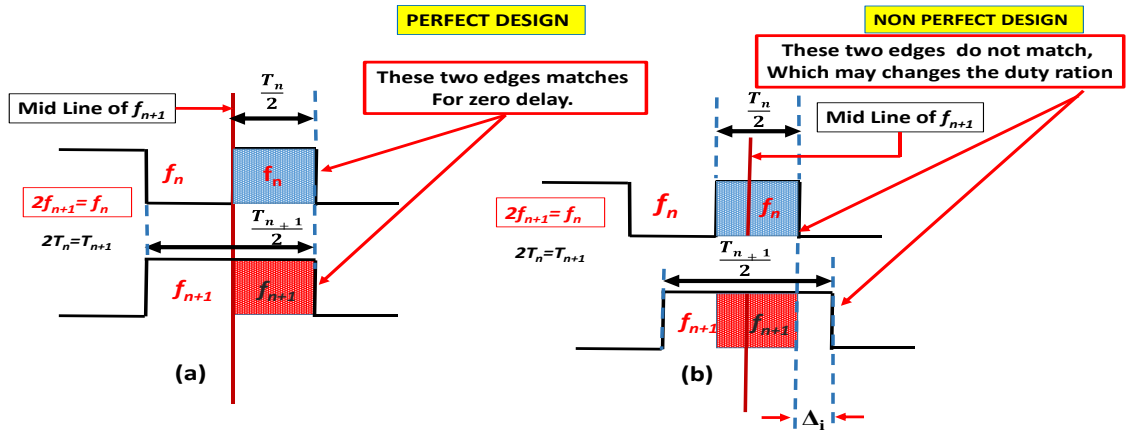



Fig. 3.6. This figure shows the challenges one will face while using continuously the frequency dividers. The falling edge of the outputs from the FD n, call it $f_n$ and from the FD (n+1), call it $f_{n+1}$ should exactly match as shown in Fig. 3.6(a). But in realty all Δis at every falling edge are not zero. The actual offset is shown in Fig. 3.6(b).

### 3.3.3 Design Verification and Chip Fabrication

Design Verification is one of the most important procedures to detect and fix errors before fabrication. Before the chip tap-out, the design was checked using design verification tools both at CHIP and CELL levels. The layout of the complete chip is shown in Fig. 3.7. with the telemeter circuitry location marked on it. The circuit is connected to the 5 bond pads, 1 ground pad, 2 power supply pads (VDD for the circuit and V_DRIVER for the output buffer circuit), 1 V_CONTROL pad to set the oscillator frequency, and 1 output signal pad as shown in Fig. 3.7. The wire-bond pads over the BFMOAT ground plane were used for I/O Pads because BFMOAT provides the lowest parasitic capacitance than the other two ground plane options [Polysilicon (PC) and Active layer (RX)] available.

To check and ensure that the connections of the transistors in the layout are the same as in the simulated circuit schematics, LVS (Layout versus Schematics) check was performed and satisfied. Furthermore, PEX (Parasitic EXtraction) tool was run to extract parasitic resistance and capacitance of the interconnect metal line and connecting vias from the design layout. These parasitic elements were then included in the post-layout simulation to analyze the more accurate design behavior of the layout and the required adjustment was done in the design to maintain the desired circuit performance.

The layout of the complete circuit was verified using DRC (design rule check) tool. The antenna rules were also satisfied for the large interconnect metal lines connecting to the gate of the transistor to prevent gate oxide damage due to a large

amount of charge build-up on the metal line during the wafer processing. To avoid this, large metal lines were tied down to substrate forming reversed biased diode called a "tie-down" diode and are basically n+/ substrate or p+/n-well diodes which proved the current path for the charge build-up during fabrication.

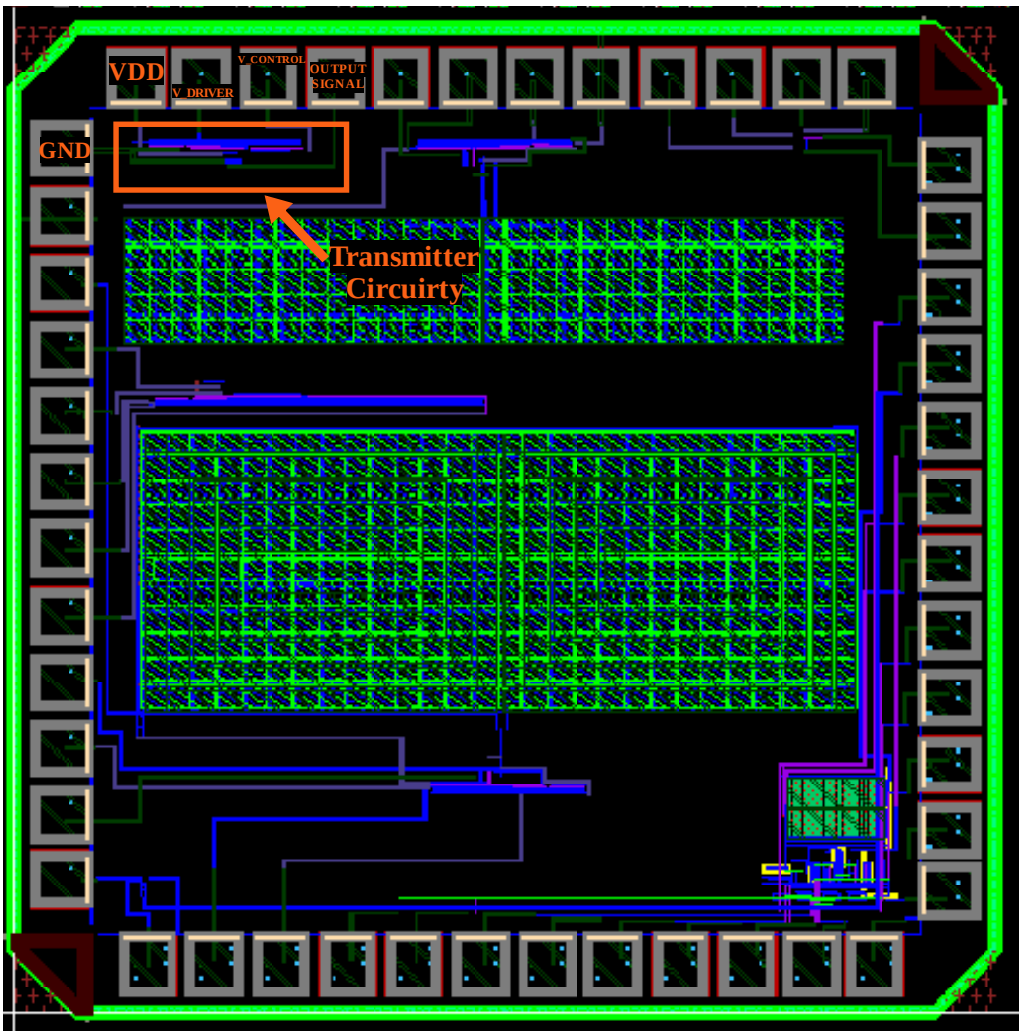



Fig. 3.7. Layout of the complete chip in CMOS8RF 130nm process with bond pads and beveled (chamfered) cornered Chipedge.

In the CMOS8RF 130nm technology, the latch-up and ESD rules are an optional requirement and not compulsory. Hence, because of the shortage of time, these rules were ignored. Density rules were satisfied at the CHIP level and the density pattern fill for the last three layers was done manually while the other layers were autofilled by the foundry. The mask descriptions of the DRC and LVS clean chip were generated in GDS II stream format and sent to the foundry for the tap out of the chip.

The returned fabricated chip is packaged in QFN_7X7_48A, (the packaging only option available under the educational program for us) is shown in Fig. 3.8. This is

basically a 48 pin, Quad Flat No-lead package with an air cavity and the dimension of the package is 7mm X 7mm. However, for the final insect telemeter, the packaging for the insect telemeter is discussed in section 3.6 which would offer the smallest size and lightweight. Fig. 3.9 shows the bonding diagram illustrating the connection of the final chip pads with the lead frame pins of the QFN package.

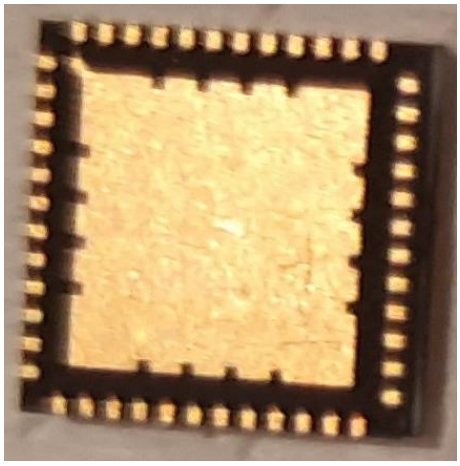


Fig. 3.8. QFN_7X7_48A chip package.

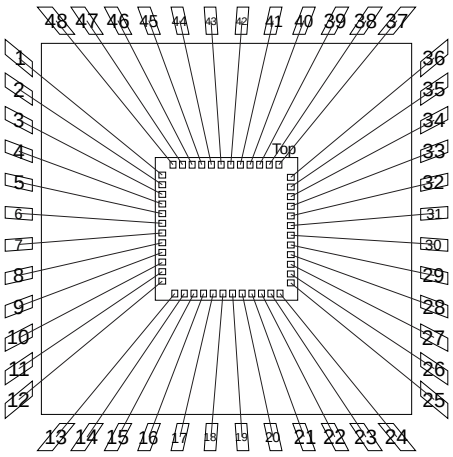



Fig. 3.9. Bonding diagram for connecting chip bond pads to the package lead frame pins.

## 3.4 Chip Testing

To detect the fault in the circuit and verify the functioning of the IC chip, testing of the chip occurs at various levels of the design and manufacturing process like wafer-level, packaged chip level, board level, system-level, and field level. However, detection of the fault and malfunctioning of the chip at the lower level also keeps the manufacturing cost low. It is important to consider the mechanism of the test in advance otherwise manufacturing tests might get extremely time-consuming and expensive. Broadly speaking, IC testing is classified into three categories as follows.

1. **Functional testing:** It is done before the tape out of the chip to verify the logical functionality of the chip. During this process, a number of debug features are built while designing the chip. It might include the addition of some special circuits such as scan chains to connect all flip-flops, built-in-self-test [37] and analog probe circuits, spare gates, etc.
2. **Debugging:** It is the testing process done after the chip returns from the foundry. During this procedure, the tests are run using commercial software and post-fabrication edits can be done on silicon using Focused Ion Beam (FIB) [38]. However, this is a very expensive process and can fix only one die at a time.
3. **Manufacturing test:** This test is done to check the reliability of individual parts for mass scale shipment.

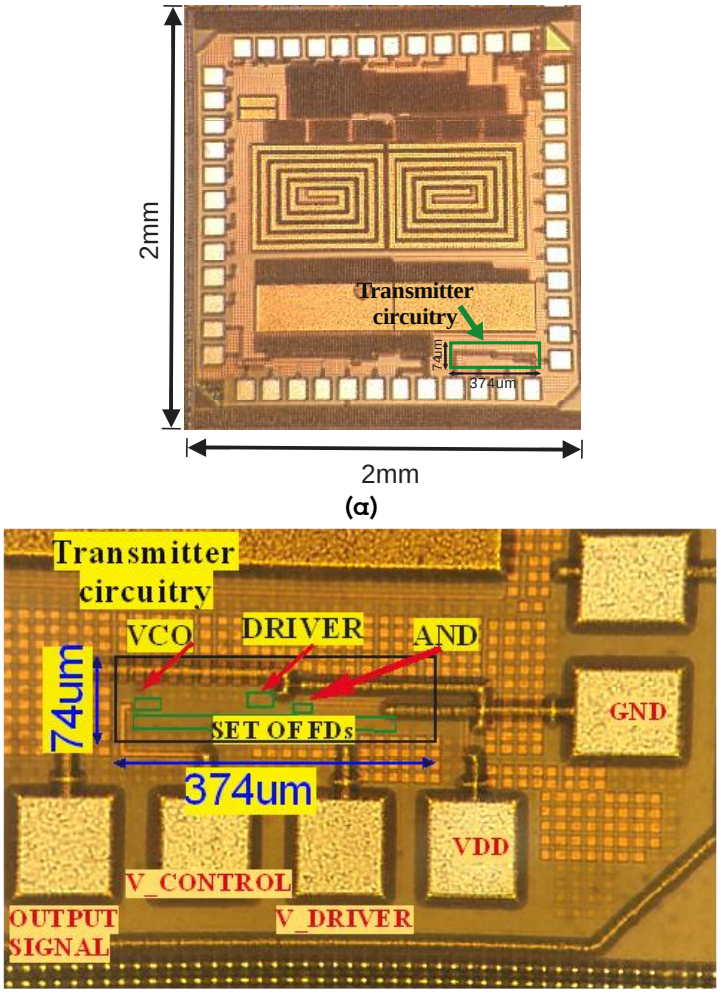
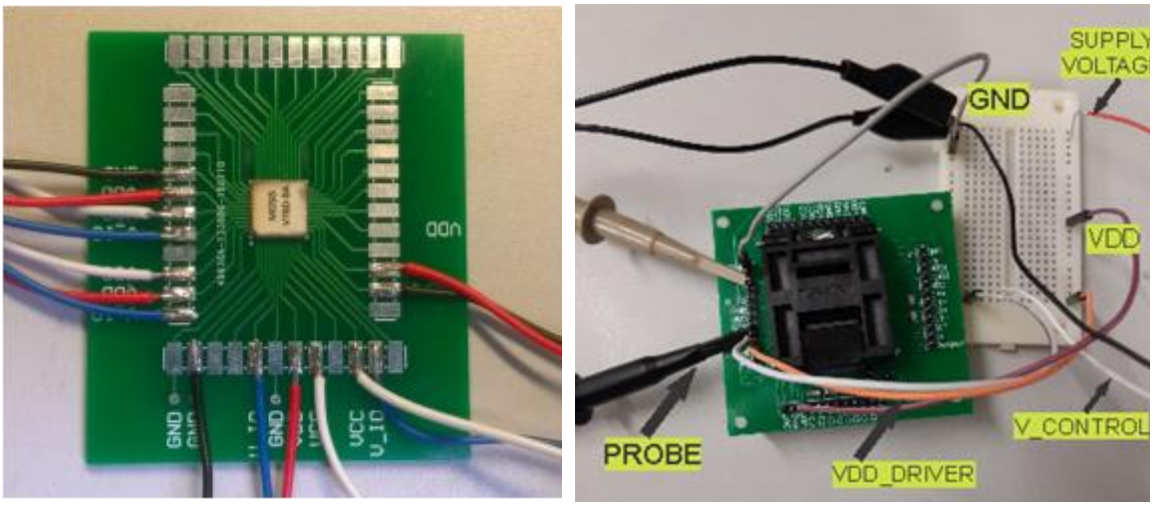



Fig. 3.10. Picture of (a) CMOS8RF 130nm chip die. (b) Picture of transmitter circuit on the chip.

For the fabricated chip, the functionality of the chip was verified through an extensive simulation process. Thereafter, the chip package returned from the foundry was tested in the lab, and experiments were done.

### 3.4.1 Test Board Design

Testing of the chip was done by two different methods. First by surface mounting the chip package of the PCB board. For this, a two-layer PCB board was designed using the Altium software tool and fabricated to surface mount the 7mm X 7mm QFN_7X7_48A packaged parts received from MOSIS. Fig. 3.11 (a) shows the top view of the PCB board with the mounted packaged chip. The top layer consists of all the signal and control routing connections, as well as power supply and probe pads. The bottom layer consists of the ground plane shorting all the ground pins. The 0.5mm pin pitch of the QFN package was fanned out into a PCB pad pitch of 2.54 mm for measurement convenience. However, in this method of testing the control voltage for controlling the frequency of the oscillator did not show any variation in the frequency. This might be due to improper mounting of the IC package on the PCB. Therefore, the package was also tested employing 0.5mm pitch 48 way through hole clamshell-type QFN test sockets. The socket was mounted on PCB and the pins of the sockets were fanned out to connect to the through-hole mounted header pins on the PCB. In this, the chip package is locked in the test socket and power supply and control voltage are provided to the corresponding pin header using jumper wires as shown in Fig. 3.12 (b).




(a) (b)

Fig. 3.11. (a) QFN_7X7_48A packaged part mounted on the PCB board. (b) QFN socket used for the experiment.

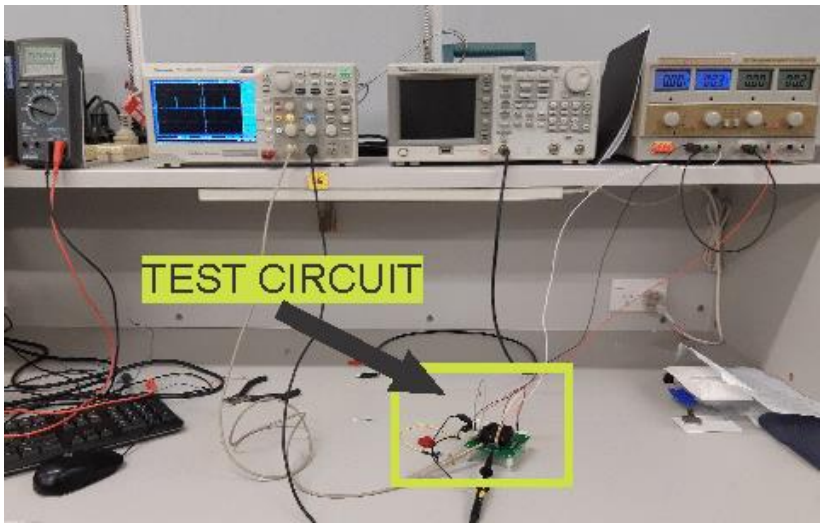


Fig. 3.12. Experimental setup

### 3.4.2 Test Setup

To perform the test, the Tektronics oscilloscope, TDS2012 featuring 100MHz 1GS/s and ESCORT EDM-89S Digital Multimeter were used for the measurement, and Regulated Power Supply (RPS) was used for providing the supply and control voltages through the following three pads, VDD, V_CONTROL, and V_DRIVER. The test equipment setup and the test board with the mounted prototype part are shown in Fig. 3.12. The yellow square block in Fig.3.12, has the test circuit. This same test circuit is magnified and shown in Fig 3.11(b). We used the TDS2012 Tektronix oscilloscope for testing our design for manufacturability. ESCORT EDM-89S Digital Multi-meter has been used for the measurement of various voltages and currents from the power supply to understand the power consumed by this chip that we have fabricated. The power is supplied to the device under test, by a Regulated Power Supply (RPS).

### 3.4.3 Experimentally Measured Results

To determine the value of α and σΔ we have chosen the output of FD 7 and FD 8 (Fig.3.2) which are designated by $f_7$ and $f_8$ in Table 3.1. Then we have determined all the various values of Δi's at every falling edge of the signals $f_{n+1}$ and $f_n$ from the simulated result, for n=7. We have selected n=7 because the multiplication of the signals from $f_7$ to $f_{13}$ will generate the desired 0.0078 duty cycle which will obey (3.3) and will make a bulletproof duty cycle, almost independent of the device size

variations for α given process corner. From the calculated values of Δis we determined the average values α and standard deviation, σΔ . In principle, the value of σΔ should be zero and the value of α will be the delay between the input and output of every FD. Thus, edge-to-edge variation will happen due to power supply noise and also due to the ambient temperature variation. And on top of this, it depends on the delay between two consecutive FD's. In this TAG, the power is in the range of micro-watts, thus, the junction temperature will be almost the same as the ambient temperature. Under ideal conditions, this chip draws an average current in the vicinity of 12$\mu$A. The maximum operating frequency of the chip will be about 132MHz. If we assume the current ramps in our chips in (10-12) clock cycles [39,40] and if we estimated the total inductance of the power and ground loop [41] will be close to 3nH or less while considering the thin 3-5$\mu$m chip is bonded on the top of paper battery [42], which is called down bonding. This will have the smallest wire loop length, maybe less than 10$\mu$m, and will generate α very low inductive interconnect. Given the above conditions, one can get α maximum, about 540nV power and ground noise, due to L[dI/dt] switching noise. This noise is capable of shifting the operating frequency [40] by 0.001MHz. Since we have found that the frequency shifts about 2.2MHz [39] per mV power and ground loop noise. Thus, this frequency change is negligible while the chip is running close to 132MHz, which is in our present design.

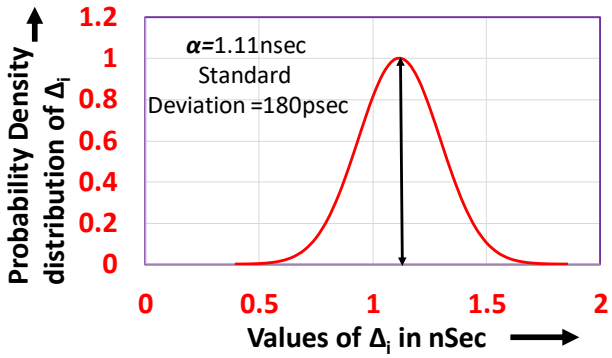



Fig. 3.13. This figure shows that the average values of $\Delta_i$'s are close to 1.11nsec and the standard deviation is about 0.18nsec. The Time period of the output corresponds to $f_7$ 20000nsec, therefore, 1nsec offset in time will change the duty cycle by an amount that will be negligible.

In Fig. 3.13 we show the plot of the average value of Δi's, which is α, and the standard deviation (σΔ) between the two outputs $f_7$ and $f_8$ for various falling edges at various times. This was done with an assumption that power supply voltage VDD is

fluctuating around 0.6V, the magnitude of that fluctuation is assumed to be 1.5$\mu$V. This is due to power and ground noise [540nV, LdI/dt noise]. On top of that, we also added LdI/dt noise, the Johnson noise, or normally called thermal noise [43]. The maximum value of the Johnson noise for all the devices was added up as white noise. This value was estimated to be around 1000nV. Actual Johnson noise will be much less due to the lower frequency of our design. In Fig. 3.13 we show the probability density distribution of $\Delta i$ as a probability density distribution function [44] for the various value of $\Delta i$. The average is about 1.1nsec and the standard deviation is close to 180psec. The width (or half period) of the signal $f_7$ from Table 3.2 can be found, approximately 20,000nsec for 3.2MHz ($f_0$) and it is about 485nsec for 132MHz ($f_0$). Therefore, it can be seen that the value of $\alpha + 3\sigma\Delta$ is about 1.5nsec, which is much less than (Tn/2), close to 20,000nsec or 485nsec. This is for the 0.0078 duty cycle. It may be important to mention, at this point, for this 130nm process file, if we multiply $f_0$ to $f_{13}$ for the generation of an extremely low duty cycle, which is about 0.00006, then that is also feasible as it will obey (1) and for this, the value of $\alpha + 3\sigma\Delta$ is equal to 1.5nsec but the half-width of $f_0$ is 3.9nsec, which is much larger than 1.5nsec. Thus, this method is proven here to produce the lowest duty cycle ever reported in the industry without shutting the power off. This is also a periodic burst mode signal with high timing accuracy (less than 1-2nsec). On the other hand, the other different kinds of tags which shut the power off for a few days, to save battery power, with almost zero duty cycles will be hard to synchronize the previous burst and present burst (after a few days) to repeat within 1-2nsec out of two or three days. These kinds of tags are not periodic and also, when these tags get turned on for operation, it will take a large time before they start generating the desired duty cycles, normally called latency. These delays can be quite large and can vary from a few microseconds to a msec. Normally, these tags are also very large and can never be used in inset telemeter applications.

The power supply used to drive this antenna had a separate isolated power supply and this supply was connected to the driver pad (V_DRIVER), as shown in Fig. 3.10. In this Fig. 3.10, we show the actual chip with bonding pads, which was encapsulated in a Quad Flat No-Lead (QFN) package [45, 46]. In reference to Fig. 3.10, this chip has a total of 5 bond pads. There is another pad [Fig. 3.10] which is called V_CONTROL [described also in Fig. 3.3], this pad controls the current demand of VCO to control the operating frequency of the oscillator. The design has only one output pad. This pad is called the OUTPUT SIGNAL [see Fig. 3.10] where

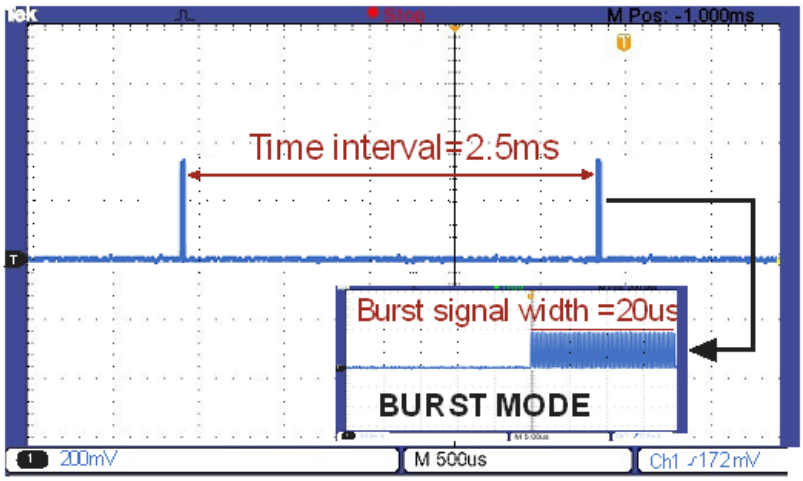



Fig. 3.14. This figure shows that burst mode is appearing at every 2.5msec as predicted initially from Table 3.1

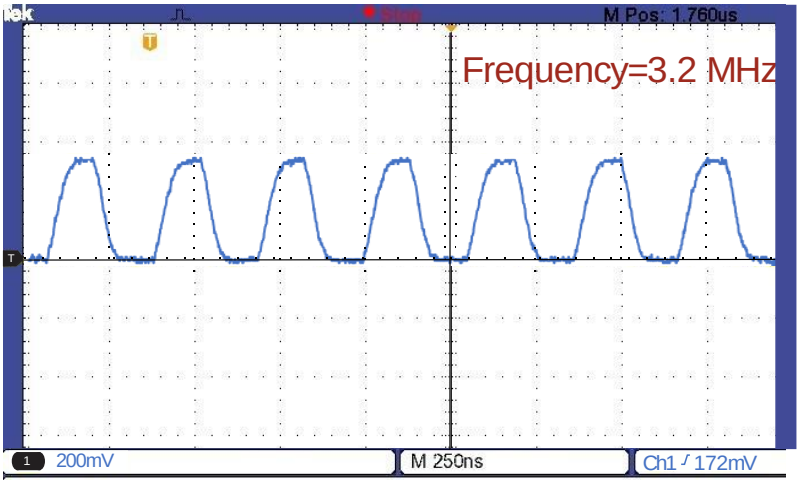



Fig. 3.15. The burst mode 3.2MHz signal appearing only for 20$\mu$sec. The amplitude of the signal is approximately 360mV only 20mV less than VDD.

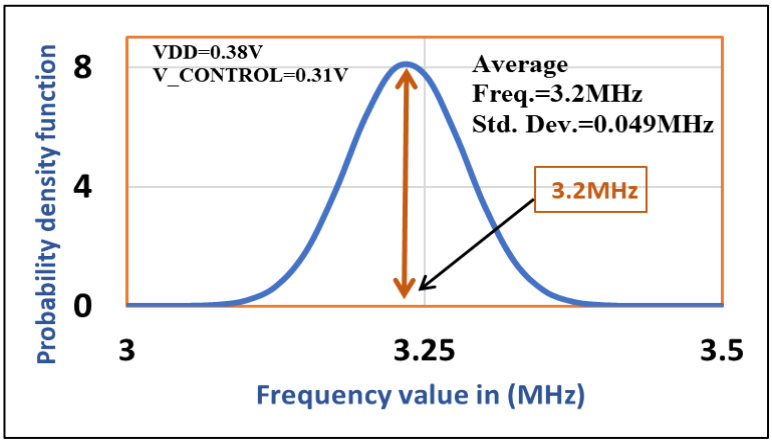



Fig. 3.16. This figure shows that the average frequency is about 3.2MHz and the standard deviation is close to 0.05MHz.

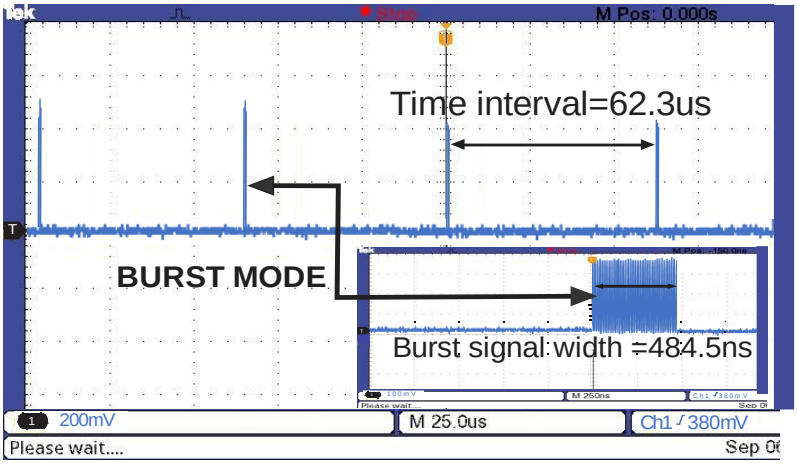



Fig. 3.17. In this figure, we show the result of 132.5MHz. The time interval for burst mode is 62.3$\mu$sec and it stays on for about 484.5nsec.

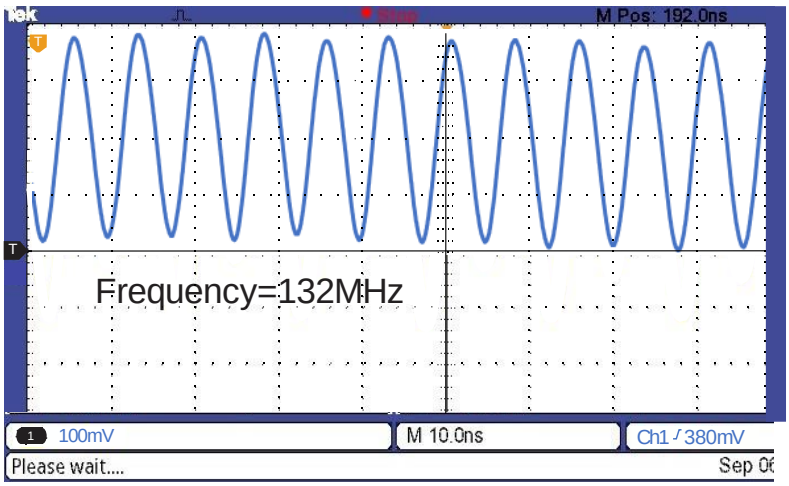



Fig. 3.18 The measured burst mode signals, the maximum amplitude of the signal received was 0.4V peak to peak. The actual average frequency is 132MHz and having a standard deviation 2.8MHz approximately.

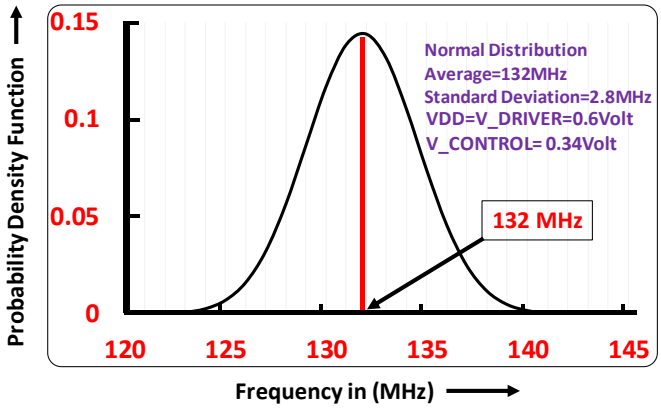



Fig. 3.19. Shows the average frequency is 132MHz and the standard deviation is 2.8MHz. This frequency is the reference/fundamental frequency from the output of the VCO.

the burst mode signal is measured. For all the FD's and VCO circuits, we have used a separate power supply (VDD, see Fig. 3.10). These three power supplies used are isolated from each other to prevent noise injection from one circuit to another. There is only one ground pad, GND is allocated for this chip. This ground is bonded to the ground (or negative) of the battery (Normally a negative terminal) and also uses substrate taps to pump the part of the current through the silicon substrate. The experiment is performed at two different frequencies (3.2MHz and 132MHz) and which were set by controlling the value of VDD and V_CONTROL.

Initially, the circuit performance was checked at 3.2MHz. During that time, VDD and V_DRIVER both were fixed at 380mV and V_CONTROL was set at 310mV). Table 3.1 shows the expected parameters including exact pulse duration and the burst time from the simulation. It predicts that the burst mode time will be close to 20$\mu$sec. This measured value matches exactly with the value in the 4th column and 8th row for 3.2MHz as fundamental/regulated frequency, $f_0$. In Fig. 3.14 the experimentally measured values were observed to be very close to the predicted values, which was exactly 20$\mu$sec. The time interval between the two consecutive burst signals experimentally was found to be 2.5msec, this is also shown in Fig. 3.14. This value should be close to the time period of the output from the $13^{th.}$ Frequency Divider (FD). In Table 3.1, the $3^{rd}$ column and $14^{th}$ row show the calculated value should be close to 2.56msec. The width of these small two vertical blue lines in this figure is approximately 20$\mu$sec. The signals, which are inside these two small lines, having 20$\mu$sec time width are shown in Fig. 3.15. This is a periodic burst mode signal having an operating frequency $(f_0)$ close to about 3.2MHz**.** The jitter of the above 3.2MHz measured signal (shown in Fig. 3.15), was measured from the above experimental data. The average frequency and the standard deviations of the above periodic signal, as shown in Fig. 3.15, inside 20$\mu$sec burst mode is shown in Fig. 3.16. In this Fig. 3.16, we show the distribution plot of the frequency to see how far we are off from the predicted simulated values, given our experimental result. This data is remarkably good, due to such a small standard deviation. It basically says that the method developed in this paper works well for the generation of lower frequency, around 3.2MHz, having a standard deviation 0.049MHz, even though there are 13 Frequency Dividers. This data also considers the power and ground noise due to *LdI*/*dt* and the white Johnson Noise. Thus, there is a 99.99% confidence level that one will have the frequencies ranging from 3.05MHz to 3.35MHz. This can be considered a quite stable frequency for any small range telemeter application. Most

importantly, the duty cycle matches with the predicted number, which is 0.0078. The average current and the corresponding power consumptions when measured were found to be approximately 4.62$\mu$A and 1.76$\mu$W respectively. The loss of amplitude of the signal by 20mV (since VDD is 380mV) as shown in Fig. 3.15, can be due to the voltage drop in active devices. The voltage drops may also be due to interconnect resistance (R). This resistance does not allow any input gates to get charge fully, due to the RC time constant. Here, C is the capacitance of the input gates.

In the next experiment, we have attempted to understand the behavior of our chip while working at 132MHz. For this case, we have used 0.6V for both VDD and V_DRIVER and correspondingly we used 0.34V for V_CONTROL. The values of VDD and V_DRIVER were increased which increased the operating frequency. The oscillator had been optimized to generate signals at the VHF range for the telemeter applications at 600mV. For generating low frequency, like 3.2 MHz by changing V_CONTROL did not generate the symmetric waveform (~50% Duty Cycle) for the upper and lower half cycle of the signal, therefore, for 3.2MHz signal, the supply voltage was also lowered. On the other hand, reducing the supply voltage gives an additional advantage of the reduced total power consumption and also allows us to get the operating frequency in the range of 1MHz to 150MHz. The simulation result shows that when VDD/V_DRIVER is 0.6V, one should have a burst mode signal, which is inside those four lines shown in Fig. 3.17. In this case, the power drawn from VDD is increased and the average power is measured to be approximately 7.07$\mu$W. It is worth mentioning that during the burst mode the current increased to its largest value $I_t$, which was found experimentally to be about 625$\mu$A. But that high current lasts only for 485nses, this timing is shown in Fig. 3.17. The current reduces to $I_s$ = 7uA, during the sleep state. From this the average current was determined to 11.78uA at 0.0078 duty ratio with 485nsec as on time, $T_{ON}$ (burst generation mode) and 62.3usec as off time, $T_{OFF}$ (sleep state) using the equation below.

$$I_{avg} = \frac{T_{ON} I_t + T_{OFF} I_S}{T_{ON} + T_{OFF}} \tag{3.6}$$

In Fig. 3.17, at the bottom, the small curve shows the "Burst Mode" signal. This is shown by a red arrow. Next, we have attempted to understand the stability of this 132MHz signal and the corresponding sigma of the signal which is shown in Fig. 3.18. This is the signal inside burst mode having a time width of 485nses and an operating frequency of about 132MHz. Fig. 3.19 shows the plot of the average

frequency and the standard deviation of the burst mode at 132MHz. The intervals between the two consecutive burst modes were found to be 62.3$\mu$sec [see Fig. 3.17]. That makes the measured duty ratio close to (0.485/62.3=)0.0078. This is the lowest ever duty ratio one designed, in any manufacturing environment using a large number of serial Frequency Dividers which does not have any passive components neither in package nor in silicon for 132MHz signal. These passive components normally increase the weight of the TAGS. In Fig 3.19 we have shown the actual frequency as measured experimentally from our fabricated chip, by going in detail into the burst signals (as shown in Fig. 3.18). This value measured, was 132MHz and the corresponding standard deviation was found to be 2.8MHz. Thus, with a 99.99% confidence level, we will have the value of $f_0$ in this design ranging from 124MHz to 140MHz approximately. These are the three-sigma results. For this, three sigma data, we have taken about 34 different chips and packaged exactly the same way for all these thirty-four chips and also measured approximately 2000 rising and falling edges from each chip to estimate the standard deviation of the frequency data as we have described in Fig. 3.16 for 3.2 MHz and Fig. 3.19 for 132MHz. We had about 68,000 the total number of data samples from all packaged samples and also from all rising and falling edges for estimating the standard deviation and average value of the frequency.

The point one can make here is that it is possible to design a radio telemeter using purely a digital design since it will help to reduce the total weight of the TAG less than what an insect and animal can bear. Also, the operational range of the insect tag will depend on the duty cycle. At an extremely low duty cycle (0.00006) the range will reduce by about 90% from its maximum operational range of 1-2km. But even this can give the tracking range of about 10m which would be useful to studies these insects in a small area, helping while pollinating. In the next section, we will discuss the novelty of our design in terms of the total possible weight of the tag if designed using the present circuit design method *vs.* other analog insect telemeter designs.

## 3.5 Analysis of the data measured in terms of performance

In this section, we will show the difference between the 132MHz sinusoidal signal and our measured data. Mathematically it can be written by the following expression,

$$\varepsilon = F_0(t) - \frac{A_0 Sin(2\pi f_0[t+\Delta t])}{2} - \frac{A_0}{2} \quad (3.7)$$

In the above equation, $F_0(t)$ is the actual measured signal which appears in the burst mode, shown in Fig. 3.18 and $A_0$ is the amplitude of the signal. In this case, it is about 400mV which can be seen from Fig. 3.18. Or, a data fit can be done to determine the actual value of this $A_0$ by measuring the peak point and the lowest point from Fig. 3.18. The fundamental/reference frequency is $f_0$ in (3.7), which is generated by the VCO. The value of ε is the difference between the actual measured data and the pure sinusoidal data. In this, the parameter Δt was optimized to align the phase ( $2\pi f_0 \Delta t$ ) of the ideal sinusoidal signal with that of the measured signal such that the first peak of both the signals overlap. This is shown in the equation above. ε represents the superimposed noise in the measured signal. This is shown in Fig. 3.20. The root-mean-square of this voltage data shows that all the frequency components other than 132MHz use only the amount of energy that comes from the signal ε which is determined to be 24mV. The remaining power stays with a 132MHz signal only. This shows that only 1% of the total power is lost and that 1% of the power is distributed in all the other frequencies (not in 132MHz), which is shown in the probability density distribution function, in Fig. 3.19. Thus, we can say that if we tune the receiver perfectly at frequency $f_0$, we will be able to get the actual energy of a given tag, which is attached to a bee or insect to determine its location while using triangular methods.

There are always concerns for not using the crystal to have an accurate frequency for a given telemeter tag manufacturing process. While using a crystal oscillator, it requires special circuits to force the crystal to vibrate at its natural frequency, and then by using a PLL [47] one can get the desired frequency which will have a well-defined frequency. This also requires more power and that is a complete "no" for these battery-operated tags. The new method shows experimentally that we have a manufacturing solution without Crystal Oscillator together which comes with another circuit to make the crystal oscillate and a PLL for better frequency performance of "$f_0$". PLL design may also need a crystal to oscillate at a lower frequency, external to the chip. That crystal will then also be required to be mounted on the top of the battery as shown in Fig. 3.21. Such design will require more power and larger weight for very stable frequency and is not suitable for bee or inset telemeter applications.

Thus, this new method can be considered a better method and approach towards telemeter applications.

There are other issues on temperature fluctuations for a given freewheeling CMOS ring oscillator. It has been observed that bees like to come out [48] when the environmental temperature ranges from 14°C to 38°C. During this temperature range, bees will be working for their foraging. Thus, the part has to work during these temperature variations. But ironically, the frequency of the freewheeling ring oscillators increases with the increase in temperature [49]. This value is about 1-3MHz/°C. This problem can be solved only by generating codes for each bee and performing frequency-shift keying (FSK) modulations. In this modulation technique, the coded data for a given bee or inset will be modulated with the reference fundamental frequency $f_0$, even though it may be different at different temperatures. But at the receiver, by tuning the frequencies to various values of $f_0$, which corresponds to the estimated temperature range (since we do not know the temperature the bees or insect is observing) we will be able to detect the code for a given bee. This coded telemeter design is implemented and is demonstrated in chapter 4.

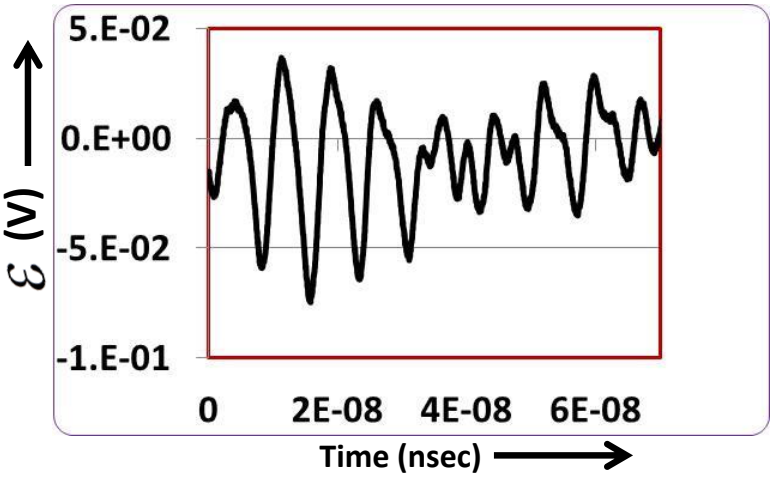



Fig. 3.20. This figure shows the difference between an actual 132MHz sinusoidal signal and the measured signal.

## 3.6 Conclusion

This chapter presents a novel method to generate a very low duty cycle signal which is employed to design a very LDC burst mode signaling scheme for insect telemeter application. The insect radio-telemeter, operating on burst mode is designed by using digital logic which occupies a very small area of 0.028-mm$^2$ on the chip. This

simple circuit is scalable and has a huge margin for the generation of the burst mode signals while still satisfying the equation (3.3). The lowest ever duty cycle for this design was found to be around 0.00006 for periodic signals. But the silicon chip was designed for the duty cycle of 0.0078 and fabricated in 130nm technology and packaged it to show the method works. It was also demonstrated that due to the large margin of 20,000nsec *vs.* 1.5nsec, the duty cycle will be consistent and will have only one value 0.0078. This may not change, due to the variation of device sizes for a given process corner. This low-duty cycle saves power for longer battery life. The IBM CMOS8RF 130nm [50] process technology is used to build these units which are encapsulated in the QFN package and are experimentally tested in the lab.

# CHAPTER 4

# CODED DIGITAL INSECT TELEMETER

## 4.1. Introduction

To track multiple tags simultaneously, tags are required to have some identification methodology. In conventional telemetry individual tag identification is based on the transmitted signal frequency. Wherein, each tag is assigned a frequency range *i.e.* {*f* to *f+df.*}. Generally, this frequency window, *df* is kept around 0.5MHz. So, if one tag operates at 150MHz-150.5MHz the other tag will operate at 150.5MHz to 151MHz. and so on. This identification methodology poses several disadvantages and makes the frequency stability of the transmitted signal a prime concern for the proper operation of the tracking system. For detecting a large number of insects, the assigned frequency range for each tag requires to be narrower which makes frequency stability a more crucial parameter, or else the number of tags that can be used for any available VHF frequency bandwidth gets limited. Besides, these tags experience frequency drift over time as the output voltage of the tag battery does not stay precisely the same and this could potentially interfere with the correct identification of the tagged insect. Moreover, the transmitted signals being analog are more susceptible to phase noise and other environmental interferences. These impediments and drawbacks have been seriously looked upon and telemetry manufacturers have tried solving these issues by including various coding schemes into the transmitted signal.

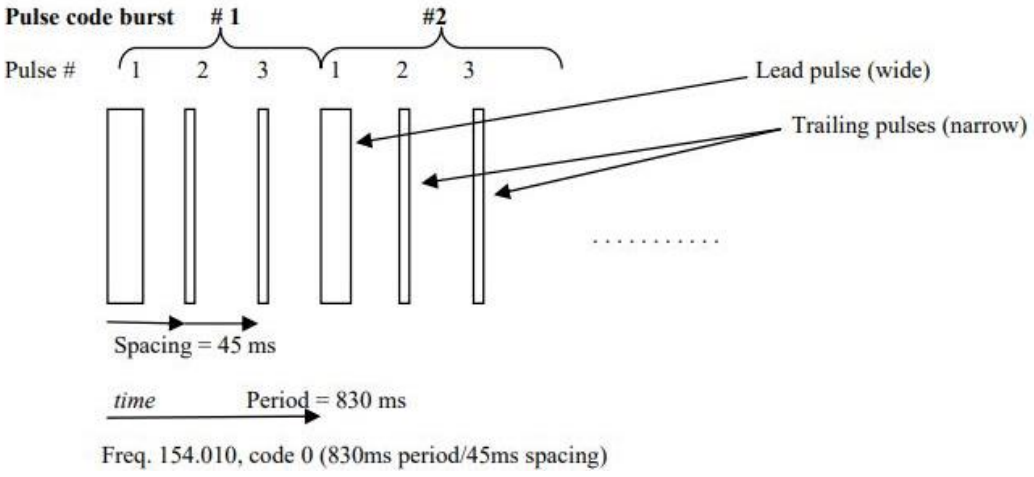



Fig.4.1 Pulse coding technique used in VHF telemeters for tag identification.

A very typical coding scheme most commonly used in the telemeter industry is illustrated in Fig. 4.1 [51]. It consists of three pulses; the first pulse is the lead pulse and the other two short pulses are used for identification purposes. The spacing between the two short pulses is altered for each tag to define a unique identification code. Additionally, the spacing between the encoded pulse burst is also varied for each telemeter to avoid the signal overlap from the other transmitters operating at the same time. The downside of these coding techniques is that it increases the telemeter design complexity and is infeasible for implementation on the smaller tags. These tags require a microprocessor to code the transmitted signals which increases the tag size, weight and doubles the power consumption resulting in heavier tags with reduced tag life for the same size battery.

In this chapter, a novel telemeter architecture has been presented which encodes the transmitted signal burst with an 8-bit digital code without the need for a microprocessor. Unlike state-of-the-art, this digital coded telemeter design has been implemented on the ASIC and does not need PCB for the integration of the design. This keeps the tag size and weight very small. The design employs an NRZ coding scheme for baseband line encoding with FSK (Frequency Shift Keying) modulation [51] to transmit the coded burst signal at a very low duty cycle. In the second section of the chapter, various coding and modulation schemes are discussed with the best suitable option for its implementation in the insect telemeter. The third section demonstrates the new architectural design of an 8-bit digital insect telemeter implemented in HPP 28-nm CMOS process technology. The monolithic chip-tag occupies an active die-area of 1012-$\mu$m2 and consumes 6.54-$\mu$W at a throughput of 576b/s. The design, however, could not be fabricated in the 28nm process due to a very high fabrication cost. The telemeter circuitry is redesigned in TSMC 65-nm process and is fabricated and successfully tested in the lab. Section four presents the design implementation in 65nm with the experimental data and section five concludes the chapter.

## 4.2. Line Encoding and Modulation

Line encoding is the technique for generating baseband digital signals from digital data for data transmission. The most common line encoding [52] used in RFID tags are Non-Return to Zero (NRZ), Manchester (bi-phase), Unipolar RZ, DBP (differential bi-phase), Miller, and differential coding and are illustrated in Fig.4.2. In NRZ

coding binary 1 is represented by high and binary 0 is represented by low voltage level. In Manchester coding, binary one is represented by negative transition if the voltage level is from high to low and binary 0 is represented by a positive transition of the voltage level that is from low to high. Unipolar RZ coding scheme generates a high signal for the first half period to code binary 1. For binary 0 no signal is generated throughout the period. DBP codes binary 0 by a signal transition in half bit period while binary one is represented by the absence of signal transition. Additionally, in DBP signal level is altered at the beginning of every bit period to facilitate easy reconstruction of the pulses on the receiver side. In the miller coding scheme, binary 1 is coded by signal level transition within the half bit period and 0 is coded by the continuation of the signal level over the next bit if the previous bit is 1 otherwise the signal level toggles if it is 0. Modified Miller coding is the variation of

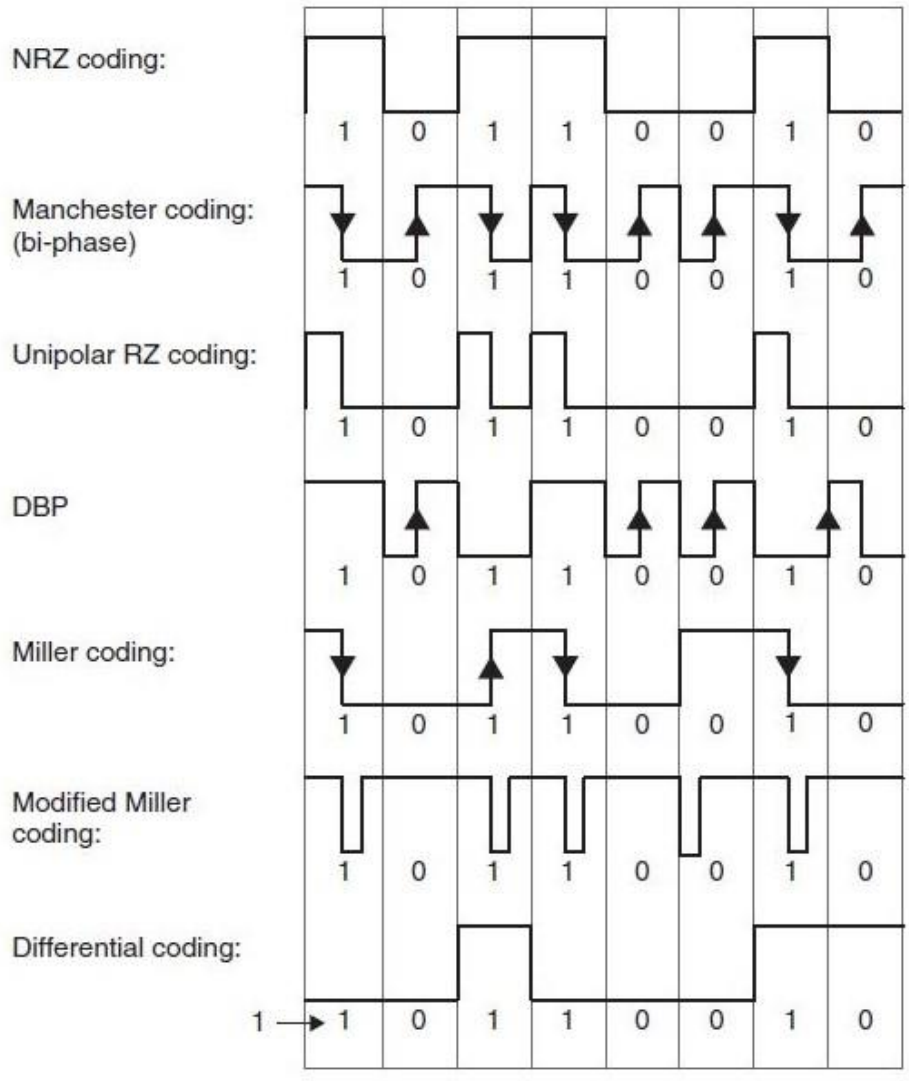



Fig.4.2. Common line coding schemes used in RFID tags.

Miller coding in which each level transition is replaced by a negative pulse making it suitable for continuous power transfer in inductively coupled RFID tags. In the Differential encoding scheme, binary 1 is represented by the toggle of the signal level whereas for binary 0 signal level remains unchanged.

Generally, depending on the application and bandwidth of the transmission media suitable encoding scheme is selected. Due to simplicity and low implementation cost for the insect telemetry NRZ encoding is used to code the 8-bit tag identification code into the transmitted signal burst.

In RFID the digital data signal cannot be directly communicated from the tag to the receiver because of its much lower frequency spectrum and uses a radio wave called carrier signal to transmit the digital signal. The digital signal is used as a base band signal to modulate the carrier signal by varying some of its properties (like phase, amplitude, or frequency) for the purpose of data transmission. The most common modulation schemes used in RFID system are:

1. Amplitude Shift Keying (ASK)- In this, the amplitude of the carrier signal is switched between two voltage levels by the binary digital code.
2. Phase Shift Keying (PSK)- Here, the phase of the carrier signal is switched between 0 and 180 depending on binary 1s and 0s to be transmitted.
3. Frequency Shift Keying (FSK)- In this, the information is transferred by switching the frequency in the carrier signal. Binary FSK (BFSK) is the most commonly used FSK scheme for telemetry applications. In this, two discrete frequencies carrier signals are transmitted depending on binary 0s (called space-frequency) and binary 1 (called mark frequency). Due to its simplicity in implementation and robustness, this modulation scheme is employed for transmitting the coded signal burst in the proposed insect telemetry. Fig.4.3 shows the BFSK modulation technique.

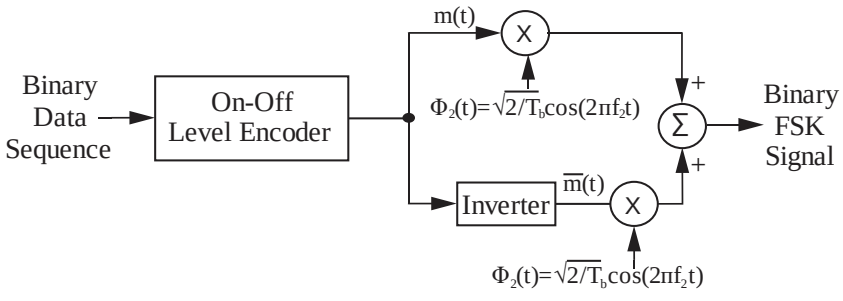



Fig.4.3. Binary FSK modulation.

## 4.3. The Architectural Design of The New Telemeter

The overview of the architectural component of the proposed new digital telemeter design with an 8-bit coding scheme is shown in Fig. 4.4. Here, primarily, three functions are being implemented. First, the low duty-cycle (LDC) pulse signal generation, second, the generation of 8-bit tag identification code, and third, the FSK modulation of the carrier signal with the 8-bit code for aerial transmission.

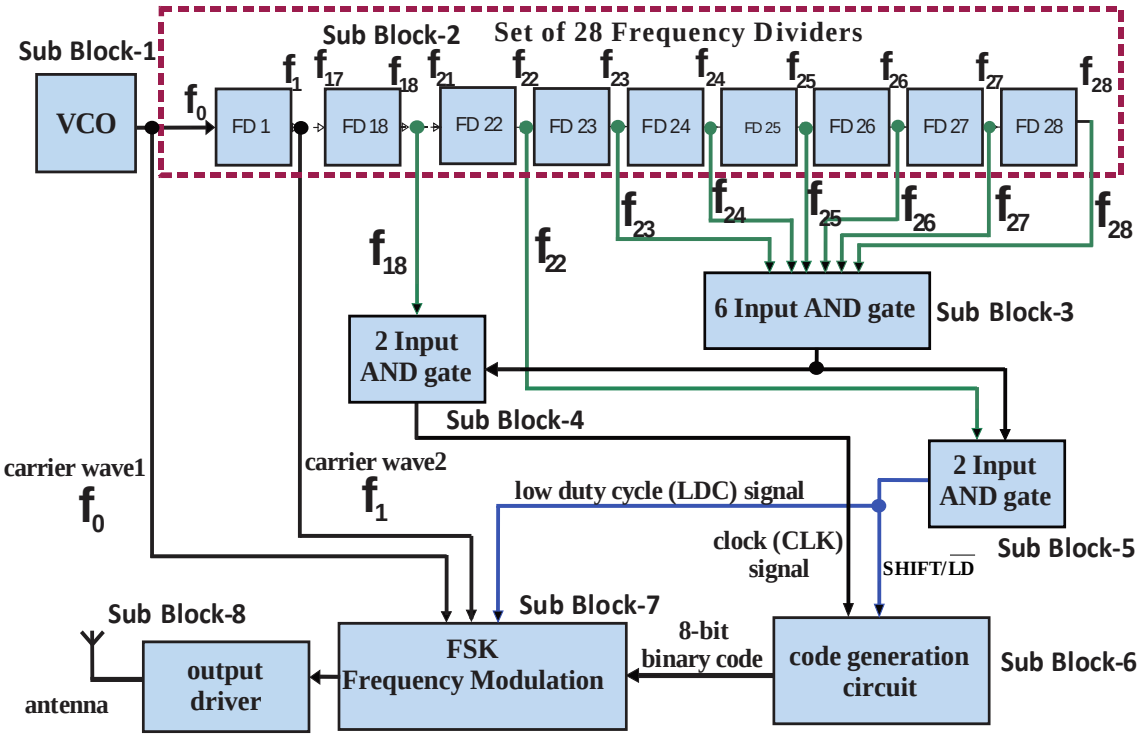
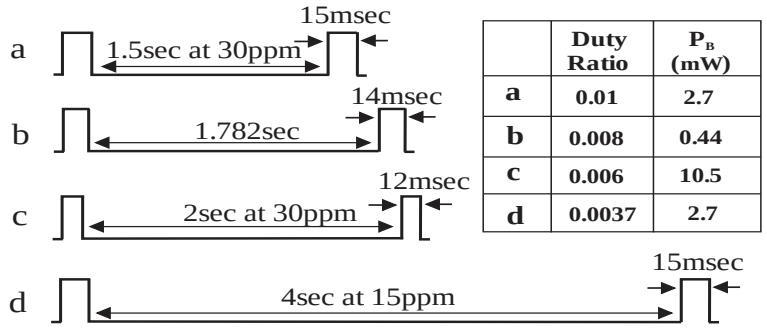



Fig. 4.4. An architectural block diagram of the proposed transmitter circuit.

The LDC signal controls the synchronized transmission of the tag identification code since the codes are generated and transmitted only when this signal goes high. This is done by using it as a shift (strobing) signal in the code generation circuit. Since for tracking bees, transmitted signal bursts of around 10ms – 15ms are needed for easy signal detection by receivers, and, since the insect/tag location needs to be tracked every few seconds, a duty-cycle of around 0.008 is chosen as appropriate for transmission. If the duty-cycle gets too low, it creates an issue in the detectability of the signal in the field and reduces the operational range of the tag [53]. Also, in [18], it is mentioned that it is difficult to track tags with a duty-cycle less than 0.008. However, presently, the lowest duty-ratio being used in the commercial tag is 0.0037. Hence taking the above into consideration, the duty-ratio of 0.008 was chosen which would provide enough operational distance (~1km) at a low power budget. The

duty-ratio, ON-time, and the interval between the burst pulses for the currently available smallest active commercial VHF tags and the proposed tag are shown in Fig. 4.5. There are VHF signals inside each burst square-wave pulse but are not shown in the illustration for simplicity. Pulse (a) and (d) show the pulse signals for the A2412 tag [19] at two different duty-ratios, 0.01 and 0.0037 respectively; pulse (b) shows the signal of the proposed insect-tag, while pulse (c) is the signal of the PicoPip tag [54]. The figure also shows a comparison of the power being dissipated by the tags during the generation of the burst-mode independent of the duty-ratio. From the comparison table in Fig. 4.5, it is evident that the proposed new insect tag design not only conserves battery-life by employing a very low duty-cycle but in addition consumes 83.7% less power than the next best A2412 tag during just the burst pulse duration alone.




| | Duty Ratio | $P_B$ (mW) |
|---|---|---|
| a | 0.01 | 2.7 |
| b | 0.008 | 0.44 |
| c | 0.006 | 10.5 |
| d | 0.0037 | 2.7 |

*$P_B$- Power dissipation during the creation and transmission of the signal*
*ppm- pulse per minute*

Fig. 4.5. The burst signal pulse-interval and pulse-width for various smallest commercial active VHF tags and the proposed tag, (a) A2412 (duty-ratio = 0.01), (b) the proposed insect-tag (this work), (c) PicoPip, and (d) A2412 (duty-ratio = 0.0037).

Another use of this signal is to turn-off the switching devices when there is no transmission to reduce the average power consumption, and this is done in the FSK modulation sub-block. The sub-blocks 1, 2, 3, and 5 in Fig. 4.4 are employed for the LDC signal generation using the technique described in Chapter 3.

Sub-block 1: This is a current-starved voltage-controlled ring oscillator (VCRO) which is set to generate the required reference VHF frequency, say, $f_0$ (150MHz in this case). The output of this oscillator has two purposes. First, to generate the LDC signal, and second, to provide the carrier signal for modulation by the identification code.

To optimize the frequency stability at the targeted frequency, designs of VCRO are investigated. Fig. 4.6 depicts the schematics of two VCRO designed in 28nm process technology. Type "a", consisting of seven stages voltage-controlled ring oscillator, was found to draw an average current of 1.5uA at 150MHz frequency which is slightly lower than the average current drawn by Type "b" oscillator which is around 1.8uA. However, the frequency jitter of type a is quite large compared to type b and is shown in Fig. 4.8. Therefore, type b which is a 5-stage VCRO is employed in the telemeter design, and its layout is shown in Fig. 4.10(a). Here, $V_{control}$ is a bias voltage that controls the current mirror reflecting the bias current through every inverter in the ring to set the desired frequency.

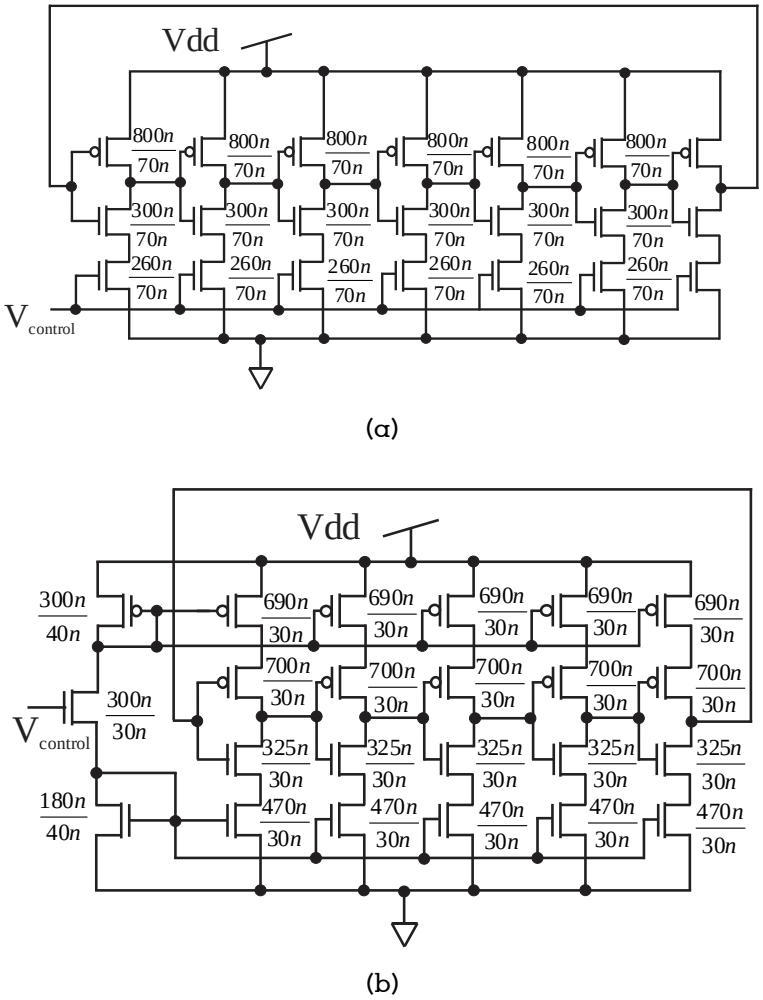



Fig. 4.6. The VCRO in 28nm CMOS for generating the 150MHz reference signal

Sub-block 2: It comprises of 28 "divide-by-2" frequency-divider (FD) flip-flops (a ripple counter). This block takes the reference VHF signal from VCRO (in this case 150MHz) and successively halves the frequency to eventually generate a 0.56Hz signal. The counter is implemented using the falling edge triggered master-salve D

flip-flops as shown in Fig. 4.9 and Fig. 4.10(b) shows its layout designed using NAND gate and inverters in 28 nm process technology. Other flip-flop designs [55] were also investigated. However, the simulation result of the flip-flops did not show a significant difference in the performance in terms of power and delays.

Signals with a range of frequencies can be tapped from the set of 28 counters which are further combined to generate other signals in the circuit. Table 4.1 illustrates the signal frequency at each FD tapping point along with its time-period and pulse duration. Here, for the insect telemetry application, a duty-cycle of around 0.008 is chosen and hence signals from $f_{22}$ to $f_{28}$ are multiplied to generate the duty cycle of $T_{22}$ / $2T_{28}$ which is 0.0078 in this case.

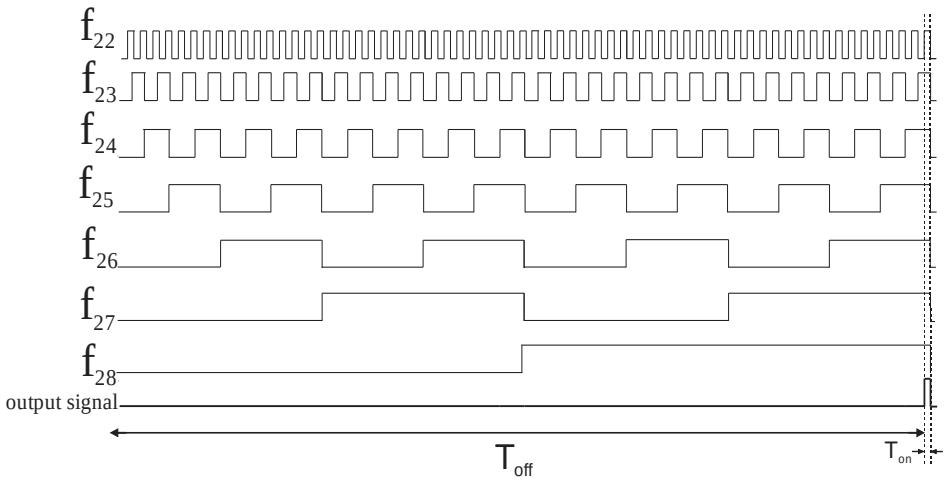



Fig. 4.7. Generation of the low duty-cycle (LDC) signal using $f_{22}$ to $f_{28}$. The output signal is high only when all the signals are high at the same time otherwise it is low.

Sub-blocks 3, 4, and 5: Sub-block 3 consists of a 6-input AND gate as shown in Fig. 4.11 and its layout is shown in Fig. 4.12. This takes the signals ($f_{23}$ to $f_{28}$) tapped from sub-block 2 and multiplies them to enable two separate down-stream signals. The output is ANDed with $f_{22}$ (sub-block 5) to produce the LDC. The LDC signal goes high only when all the signals from $f_{22}$ to $f_{28}$ are high. It also serves as the SHIFT/$\overline{\text{LD}}$ signal for the code generation circuit (sub-block 6). The sub-block 3 output is separately ANDed with $f_{18}$ (sub-block 4) to produce a clock signal (CLK) for the code generation circuit. This choice of tapped signals results in the duty-cycle of CLK being double that of the LDC signal so that its pulse arrives beforehand and sub-block 6 has enough time to load the hardwired code in the flip-flops before the code shifting occurs.

Sub-block 6: This is the circuit for the generation of 8-bit code for the tag so that 256 unique individual tags could be assigned. The schematic for this circuit and its

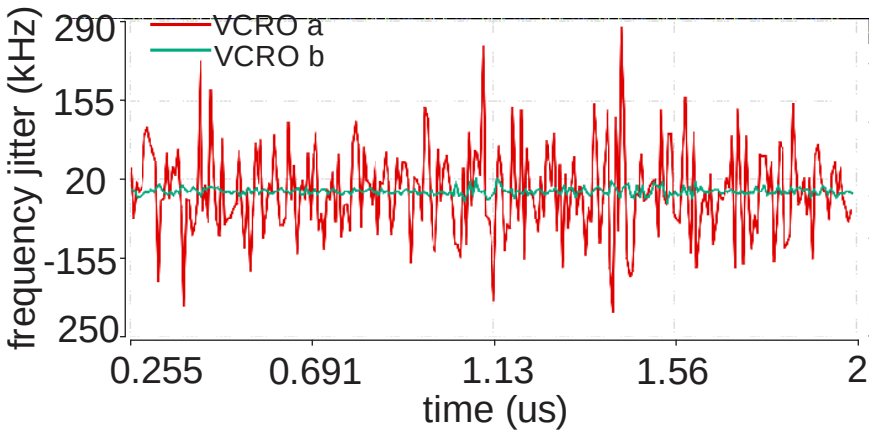



Fig. 4.8. Frequency jitter of the two types of VCRO design at 150 MHz frequency.

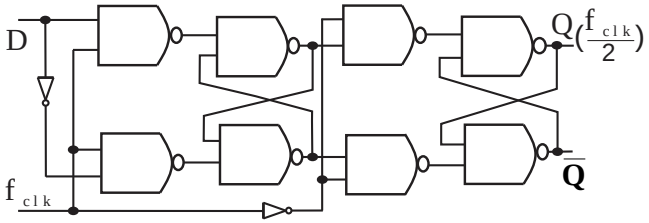
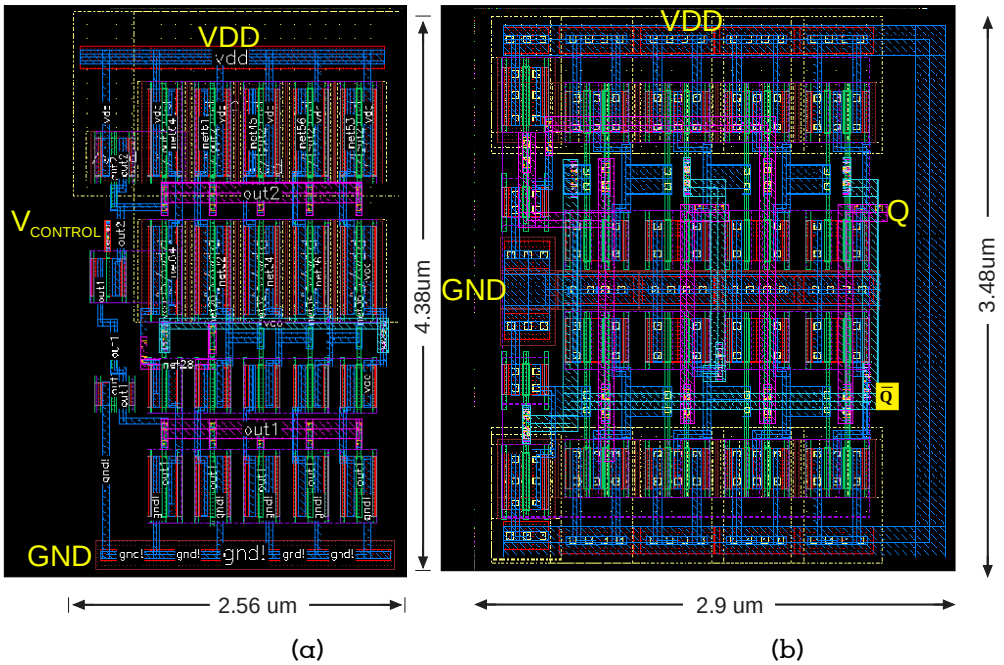



Fig. 4.9. Schematic of falling-edge triggered master-slave D- flip-flop used as frequency divider when $\overline{Q}$ is connected to D. This flip-flop is also used in the design of PISO shift-register in block 2.




(a) (b)

Fig. 4.10. Layout of (a) VCRO (type b) (b) falling-edge triggered master-slave D- flip-flop in 28nm CMOS process.

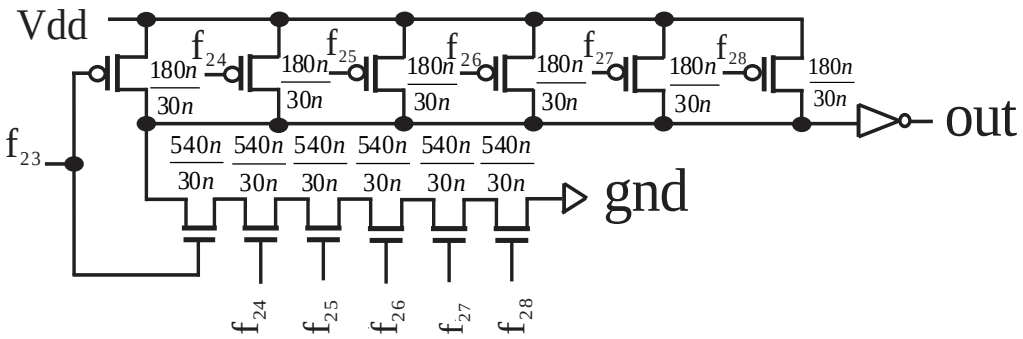



Fig. 4.11. Schematic of 6 input AND gate in 28nm CMOS used to multiply the tapped signals from $f_{23}$ to $f_{28}$.

Table 4.1

The frequency, time-period and pulse duration of output signals from each frequency divider (FD) tapping point for a 150 MHz input through a cascade of 28 frequency dividers.

| FDs | Freq(Hz) | T(sec) | $T_{PULSE}$ (sec) | FDs | Freq(Hz) | T(sec) | $T_{PULSE}$ (sec) |
|---|---|---|---|---|---|---|---|
| 0 | 1.50E+08 | 6.67E-09 | 3.33E-09 | 15 | 4.58E+03 | 2.18E-04 | 1.09E-04 |
| 1 | 7.50E+07 | 1.33E-08 | 6.67E-09 | 16 | 2.29E+03 | 4.37E-04 | 2.18E-04 |
| 2 | 3.75E+07 | 2.67E-08 | 1.33E-08 | 17 | 1.14E+03 | 8.74E-04 | 4.37E-04 |
| 3 | 1.88E+07 | 5.33E-08 | 2.67E-08 | 18 | 5.72E+02 | 1.75E-03 | 8.74E-04 |
| 4 | 9.38E+06 | 1.07E-07 | 5.33E-08 | 19 | 2.86E+02 | 3.50E-03 | 1.75E-03 |
| 5 | 4.69E+06 | 2.13E-07 | 1.07E-07 | 20 | 1.43E+02 | 6.99E-03 | 3.50E-03 |
| 6 | 2.34E+06 | 4.27E-07 | 2.13E-07 | 21 | 7.15E+01 | 1.40E-02 | 6.99E-03 |
| 7 | 1.17E+06 | 8.53E-07 | 4.27E-07 | 22 | 3.58E+01 | 2.80E-02 | 1.40E-02 |
| 8 | 5.86E+05 | 1.71E-06 | 8.53E-07 | 23 | 1.79E+01 | 5.59E-02 | 2.80E-02 |
| 9 | 2.93E+05 | 3.41E-06 | 1.71E-06 | 24 | 8.94E+00 | 1.12E-01 | 5.59E-02 |
| 10 | 1.46E+05 | 6.83E-06 | 3.41E-06 | 25 | 4.47E+00 | 2.24E-01 | 1.12E-01 |
| 11 | 7.32E+04 | 1.37E-05 | 6.83E-06 | 26 | 2.24E+00 | 4.47E-01 | 2.24E-01 |
| 12 | 3.66E+04 | 2.73E-05 | 1.37E-05 | 27 | 1.12E+00 | 8.95E-01 | 4.47E-01 |
| 13 | 1.83E+04 | 5.46E-05 | 2.73E-05 | 28 | 5.59E-01 | 1.79E+00 | 8.95E-01 |
| 14 | 9.16E+03 | 1.09E-04 | 5.46E-05 | | | | |

**These frequencies are multiplied using AND Gate for Duty cycle D =$T_{22}/2T_{28}$**

layouts are depicted in Fig. 4.13 and Fig.4.14(a), respectively. It consists of the parallel-input-serial-output (PISO) shift-register and set of 8 wires from B0 to B7 which are connected to the ground for "0" s or to the power supply (VDD) for "1" s to set the unique (distinct) binary code for each tag. These wires are fed to the 2:1 mux of the PISO shift-register. The CLK and SHIFT/$\overline{LD}$ signals are determined based on the word-length of the code. Here, for 8-bit code, the LDC signal is chosen to be the SHIFT/$\overline{LD}$ signal, while, the output of the sub- block 4 is chosen as the CLK. The code is loaded into the flip-flops when SHIFT/$\overline{LD}$ is low, and, when SHIFT/$\overline{LD}$ goes high, at every clock-cycle, one bit of the code is transferred to the output.

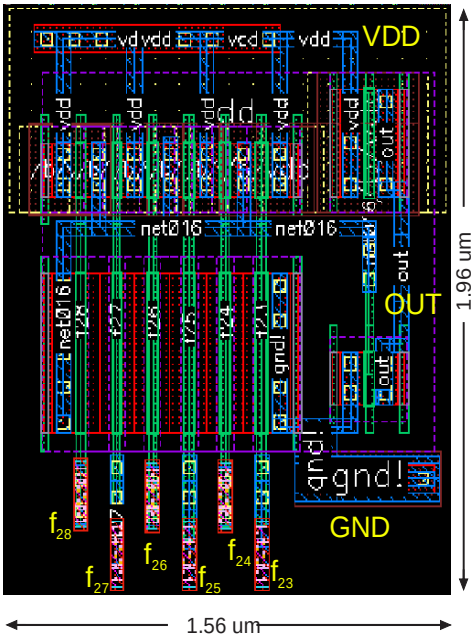



Fig. 4.12 Layout of 6 input AND gate in 28nm CMOS.

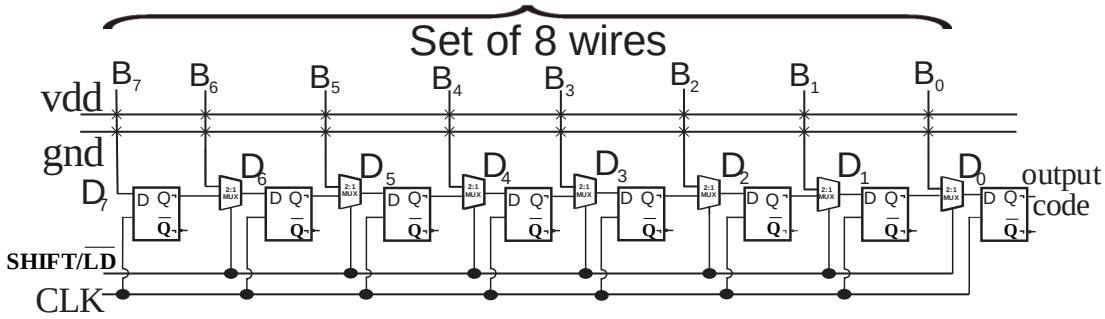



Fig. 4.13 Schematic for the generation of 8-bit code using PISO shift-register and set of 8 wires which would be connected to the fuse to set binary 0 or binary 1 by connecting it to GND or VDD respectively.

Sub-block 7: This block takes the output code from the sub-block 6 and employs it as the base-band signal for carrier modulation, followed by the transmission of the carrier signal. For this purpose, the Frequency-Shift Keying (FSK) modulation technique has been chosen so that the transmitted signal has maximum power and it could be employed in the triangulation technique [56] to find the location of the tag for insect tracking. In FSK modulation, a pair of frequencies are used to transmit 0s and 1s. The frequency used for transmitting 1s is called mark frequency and the frequency used for the transmission of 0s is called space frequency. The schematic of the circuit is shown in Fig. 4.15 (a) where a 2:1 multiplexer output carriers $f_0$ and $f_1$ for the transmission of 1s and 0s respectively. Before being fed into the MUX, the carriers are first multiplied with the LDC signal so that the modulated signal is

transmitted only when the LDC signal is high, and the power consumption is reduced by preventing unwanted rapid switching of the transistors in this block. In Fig. 4.14 (b) layout for the modulation block is shown. Fig. 4.16 illustrates the creation of windowed carriers $f_0$ and $f_1$ before they are fed to the MUX circuitry. Fig. 4.17 (a) demonstrates FSK modulation for the code 10001110 and Fig. 4.17 (b) illustrates bursts of the carrier with identification code transmitted between sleep intervals.

Sub-block 8: It consists of the final transmission driver which is a set of four inverters as shown in Fig. 4.15 (b). For power reduction, the telemeter supply-voltage is kept at 0.6V. However, the output driver is designed for a 1.2V supply so that the transmitted signal is sufficiently strong for employing the triangulation method. Hence, the first inverter in the driver acts as the level-shifter with wider NMOS compared to the PMOS to translate the voltage from 0.6V to 1.2V. The other three inverters constitute a 28nm tapered buffer circuit. The drivers last-stage is sized such that the triode-

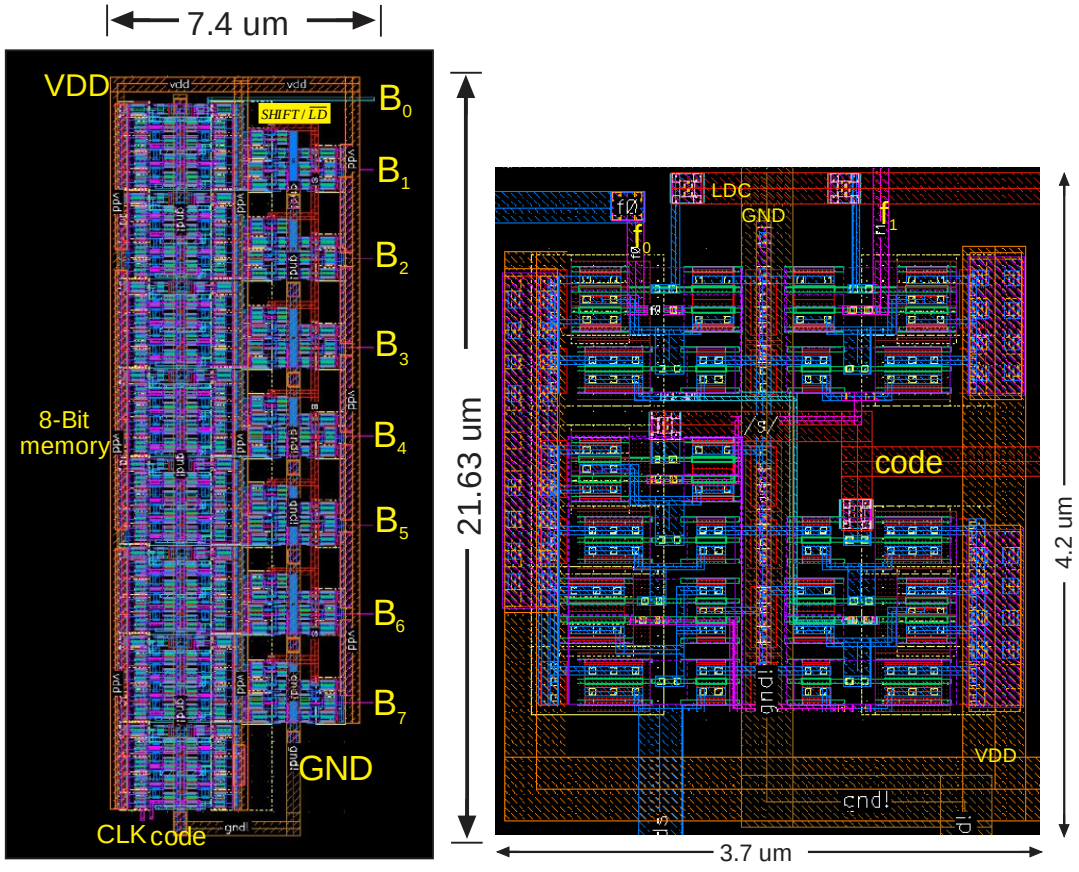



Fig.4.14. The layout of (a) PISO shift register in 28nm for generation of 8-bit code and (b) modulation circuitry.

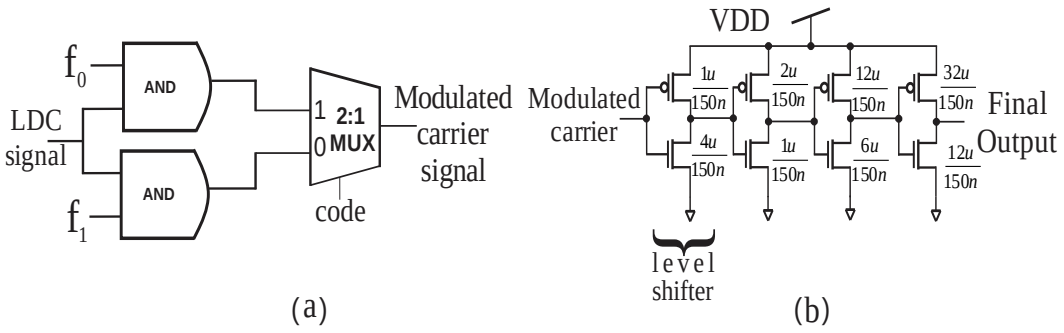



Fig. 4.15 (a) FSK Modulation using a 2:1 Mux, and, (b) schematic for making the code to appear in burst mode.

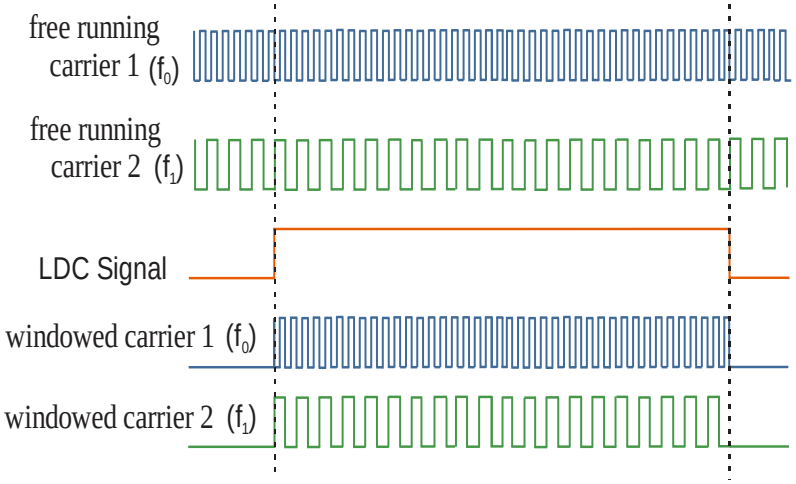



Fig. 4.16. Illustration of FSK modulation for the code 10001110, $f_o$ and $f_1$ is used for sending

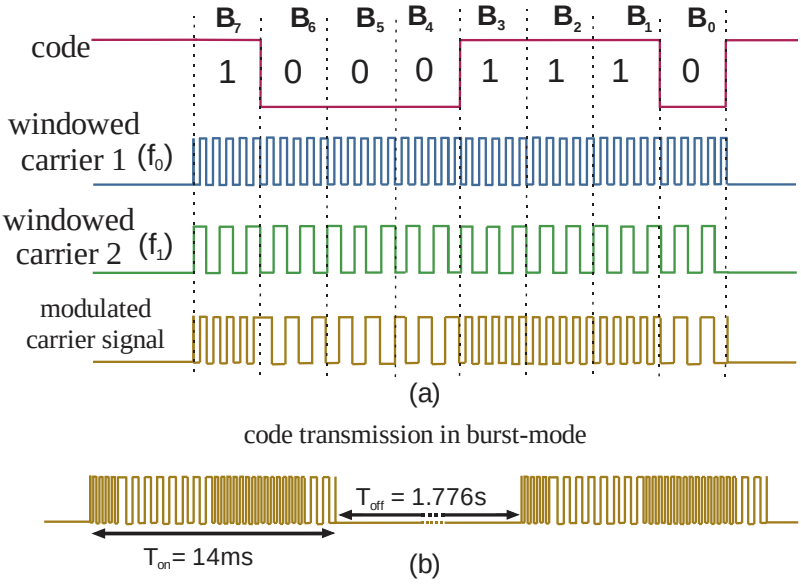



Fig. 4.17. (a) Illustration of FSK modulation for the code 10001110, $f_0$ and $f_1$ is used for sending 1s and 0s respectively, and, (b) the coded burst-mode signal to be transmitted at the tag antenna.

mode output impedance during pull-up (through PMOS) and pull-down (through NMOS) are closely matched to 50 Ω resistance for the broadband transmission of the coded burst pulse signals. The layout of transmission driver is shown in Fig. 4.18.

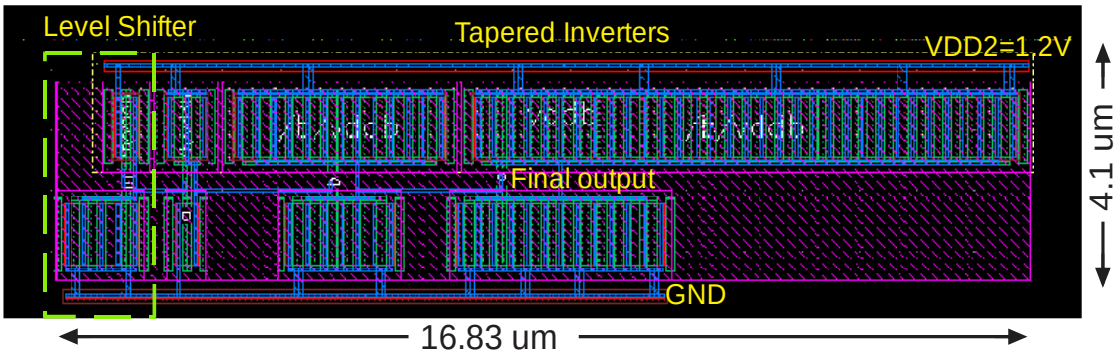



Fig.4.18. Layout of the transmission driver comprising level shifter and tapered buffers.

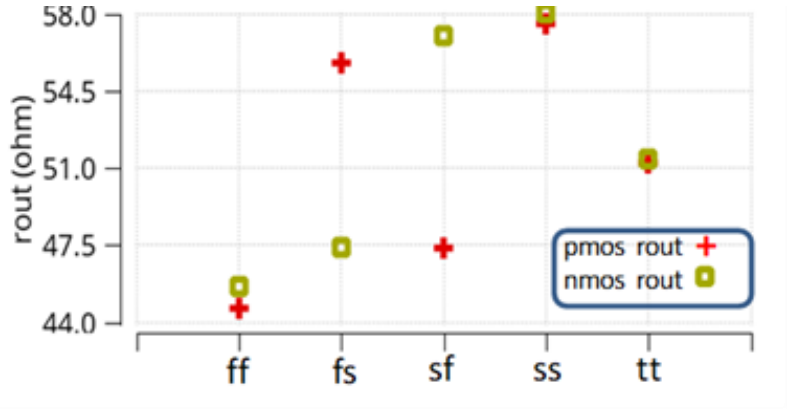
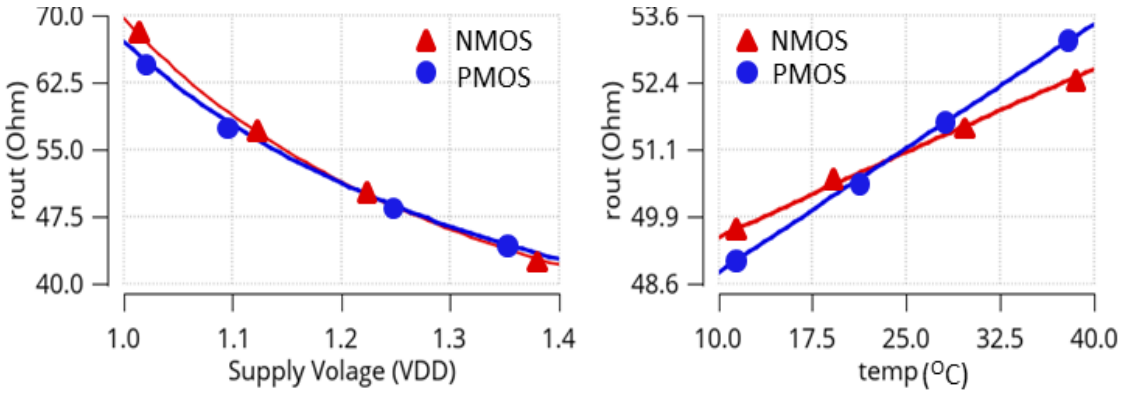



Fig. 4.19. Process corner variation effect on the matched 50-ohm output resistance of the last stage transistors.




(a) (b)

Fig. 4.20. Effect of (a) power supply and (b) temperature variations on the matched 50-ohm output resistance of the output buffer's last stage transistors.

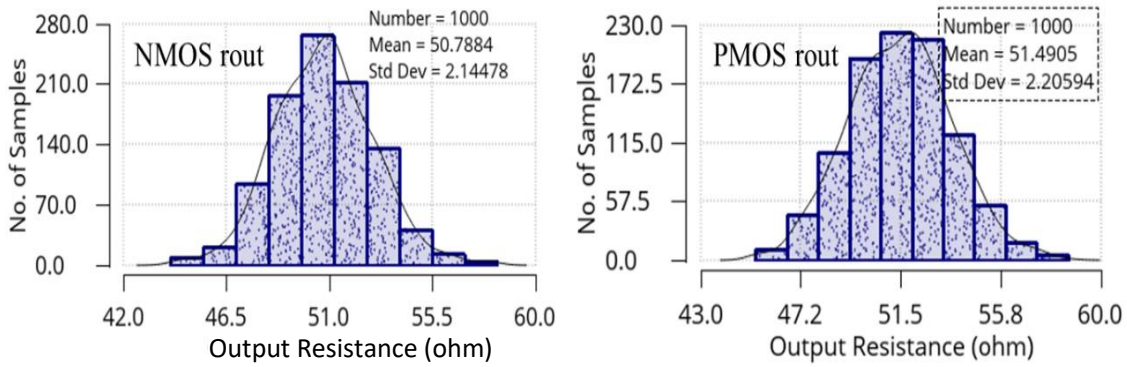



Fig. 4.21. Monte Carlo simulation for matched 50-ohm output resistance.

The process, voltage and temperature (PVT) variations is shown in Fig.4.19, Fig.4.20 (a), and Fig.4.20 (b). Monte Carlo analysis to study distribution of output resistance due to the effect of process corner variation has been performed on the last stage of the buffer and is shown in Fig.4.21.

### 4.3.1. Frequency Stability Analysis

The ring oscillator is one of the simplest and easy to implement oscillators. However, in general, the use of a free-running ring oscillator as a clock circuit is restrained due to large power-supply noise and frequency jitter [57]. Also, due to this reason, PLL or other control circuitries are implemented along-with the ring-oscillator to stabilize the oscillator frequency. This enhancement additionally requires an external reference clock which along with the PLL increases the size and the power requirement of the composite ring oscillator. In the insect telemeter tag implementation, where power dissipation and chip-area are highly constrained, the inclusion of PLL (with a few mW of power budget by itself) [58] and other control circuitry with the ring oscillator is not feasible for the miniaturization and to preserve the battery life of the tag. Moreover, this insect tag is extremely minute compared to the present-day VLSI chips where millions of transistors may be switching simultaneously to generate a large Ldi/dt voltage across the power supply rails and hence creating supply noise in the oscillators. And therefore, as will be seen in the following subsection, due to the small active-area of the tag and the small current drawn by the tag oscillator, the supply noise affecting the frequency stability of the ring oscillator will be negligible. On top of this, the embedding of 8-bit code in the transmitted LDC signal burst makes the identification process more robust, and slight variation in operating frequency is no longer a major concern. Consequently,

at present, the use of VCRO to generate the reference frequency ($f_o$) is the only viable solution for the insect telemeter design.

To justify the suitability of the ring oscillator as the reference frequency in the insect telemeter tag design, the stability of the ring oscillator is analyzed with respect to the supply noise. Details on the effect of Process-Voltage-Temperature (PVT) variation and their impact on the performance of the tag are also provided.

#### 4.3.1.1 Supply noise

The running frequency of a ring oscillator is given by the equation (4.1)

$$f_{os} \cong \frac{1}{2n\tau(VDD_{O1})} \tag{4.1}$$

Here, n is the odd number of inverter stages, τ is the time delay of individual inverters in the ring oscillator at a given temperature and supply voltage [59]. VDDO1 is the effective supply voltage seen by the oscillator circuit. Hence, ideally, at a particular temperature and at a fixed supply-voltage the frequency of the ring oscillator should remain constant. However, due to the Ldi/dt reactive-loss [60] in the interconnect path, the effective supply-voltage fluctuates and hence changes the time-period, thus, making the ring oscillator less reliable as a reference clock. The Ldi/dt drop becomes particularly significant when there are millions of transistors on a single chip and the transient switching current drawn by these devices is quite high and can rise to 100A [58]. In such a case, the effective supply voltage can vary

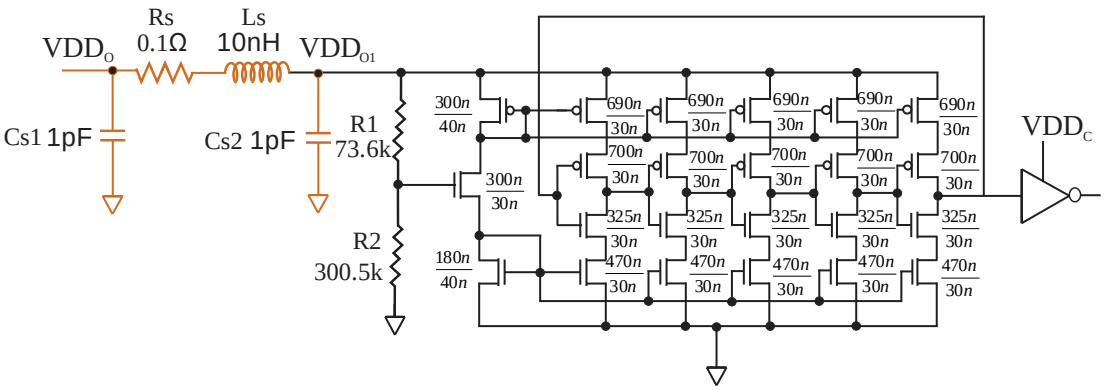



Fig. 4.22. Equivalent lumped element representation of the interconnect with the VCRO design.

up to 100mV thus affecting the performance of the circuit considerably. The supply noise deteriorates even more with increasing operating frequency. However, in the proposed insect transmitter tag, the size of the circuit is many orders of magnitude smaller and draws a very small current. Also, to prevent supply noise, a separate power supply is provided for the oscillator circuit which draws only around 3.6$\mu$A dynamic current. At 150 MHz, such a minute current along-with associated low package parasitic does not deteriorate the frequency stability in any significant way.

To analyze the effect of Ldi/dt drop on the oscillator frequency, the parasitic impedance of the package components is modeled and simulated along-with the 5-stage VCRO as shown in Fig. 4.22. The package parasitic model is indicated with brown colored lines in the front-end of the oscillator. Here, Ls, Rs, and, Cs1 and Cs2 are the parasitic inductance, resistance, and capacitances of the first and second level interconnections of the package components [60, 61] in the supply-voltage path, with nominal values of 10 nH, 0.1Ω, and, 1pF for each capacitance, respectively. The parasitic capacitances and inductances in the Fig. 4.22 are based on a lumped-$\pi$ external interconnect path model from on-chip pad-to-package pin based on the reference [59] in the paper, as well as further papers in open literature such as [62], [63], [64] and the encapsulation manufacturer's data sheet such as [65] below. The inductor Ls lumps (combines) the lead-frame inductance and the bond-wire inductance, the capacitance Cs2 is the parallel combination of the pad parasitic capacitance and the junction (depletion) capacitance of any ESD protection diode. Also, Cs1 is the lead-frame capacitance. If the lumped model and the model component values in [62] are used in the simulation, its loading effect on the power supply path is quite benign. Hence, to further explore the interconnect loading effect, higher component values for various lead-frame-based packages were employed. The value of Ls=10nH is based on [64] and [65], for example, for a PQFP type package and the series resistance of Rs= 0.1ohm was chosen to explore the effect of high-Q inductor that can impinge higher oscillatory effect on the supply-line. The value of Cs2=1pF is based on IC design consideration for maximum possible parasitic Bond-pad capacitance. The value of Cs1=1pF is the maximum possible lead frame capacitance, for example for plastic DIP type lead-frame package based on [63] or for PQFP type lead-frame package based on [65]. The higher assumption was also employed to include further testing traces including probes that will have inductances.

The oscillator is followed by a buffer to drive the rest of the circuit. VDDO is the nominal supply-voltage and VDDO1 is the supply-voltage that the ring oscillator receives after the interconnect drops. The buffer inverter has a separate power supply (VDDC) in isolation from the VCRO to reduce the switching current drawn from the power supply, VDDO. This distributed power-supply scheme reduces the Ldi/dt drop affecting the oscillator. Here, the resistive voltage divider (R1, R2) consumes far less power compared to an active (MOS) biasing circuit in generating the control voltage for the insect-tag oscillator.

Fig. 4.23 shows the simulated effect of power-supply noise on the oscillator. Here, the topmost signal is the oscillator output which takes around 12.5 nsec for the oscillation to build-up. The second signal from the top shows the di/dt waveform due to the switching of inverters in the ring oscillator. This has the maximum value of 8k A/sec and corresponds to the maximum Ldi/dt voltage variation of 80$\mu$V in the supply line. The third signal in the figure shows the fluctuation in the supply voltage, VDDO1 of the VCRO. Noise is injected due to the switching of the transistors in the oscillator circuit. At 600mV of source voltage (VDDO), the applied effective supply voltage to the oscillator (VDDO1) wiggles around 599.69mV. The bottom-most signal in Fig. 4.23 illustrates the control voltage of the oscillator which also has supply noise superimposed on it.

The effect of the fluctuation in the supply and control voltages on the frequency jitter of the oscillator is shown in Fig. 4.24. This is the deviation in the operational frequency from the average value of the oscillator signal frequency, fa (150.87 MHz in this case). The graph shows that the maximum jitter in the VCRO's frequency, represented as $\Delta$f, is around 450 kHz. From this frequency jitter, the maximum period jitter, Tp at 150.87 MHz is determined using equation (4.2) as below:

$$\frac{1}{f_a} - \frac{1}{f_a + \Delta f} = T_p \qquad (4.2)$$

From the above, the Tp value is found to be around 20 psec for the time-period of 6.63nsec. Also, the throughput of the code inside the burst signal is 576b/s which varies around 0.67 % per MHz change in the oscillator frequency as per Table 4.2. At this bit-rate, the 20psec oscillator jitter is extremely low to influence the performance of the insect-tag.

The effect of this jitter has also been analyzed in terms of the probability density distribution of the oscillator frequency. From the simulated frequency data, the mean frequency, $\mu$ is determined to be 150.8MHz with 0.157MHz standard deviation ($\sigma$). Fig. 4.25 shows the normal distribution plot of the oscillator frequency. It can be seen from this plot that due to the small $3\sigma$ value which is 0.47MHz, 99.7% of the time the oscillator frequency varies within a very small frequency range of 150.5MHz to 151.2MHz. This confirms that the power supply noise will not be an issue in this miniaturized insect-tag design.

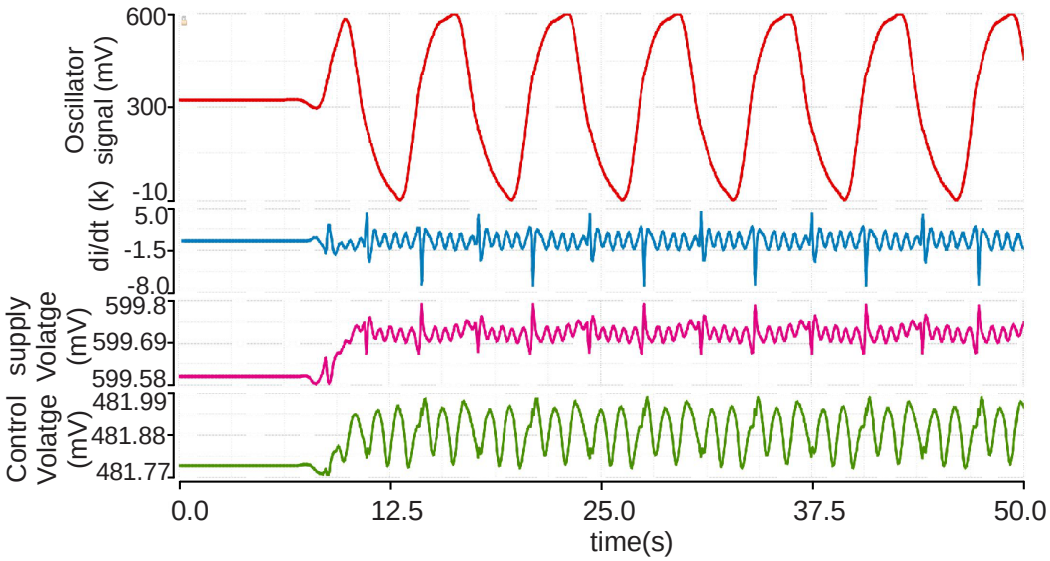



Fig. 4.23. Transient waveforms, illustrating the build-up of oscillation and the effect of supply noise on the supply-line and control-voltage-line of the VCRO.

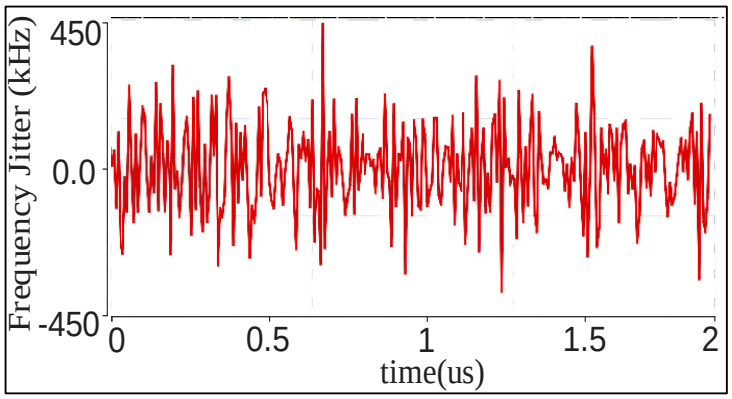



Fig. 4.24. Frequency jitter of the Ring Oscillator including random noise and power supply noise.

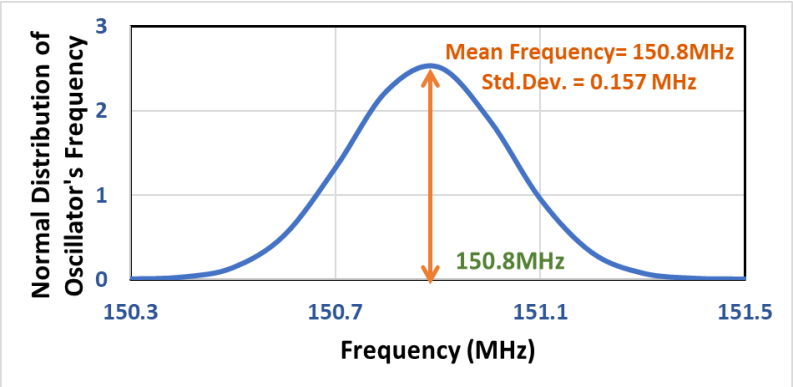



Fig. 4.25. Normal distribution plot of the oscillator frequency with mean of 150.8 MHz and standard deviation of 0.157 MHz.

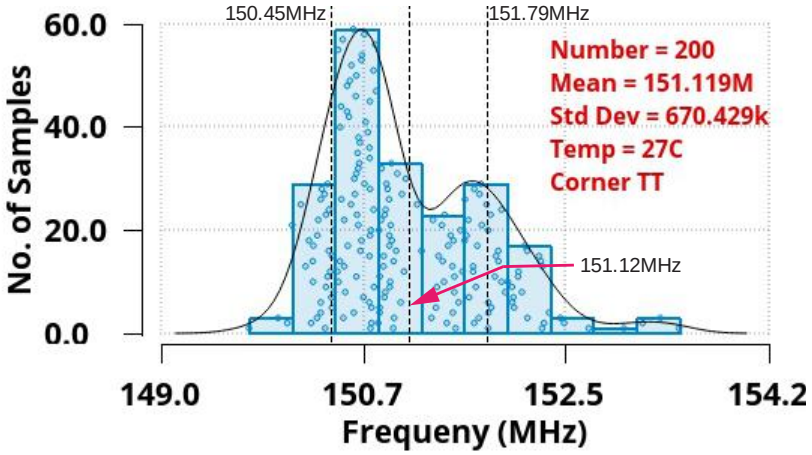



Fig. 4.26. Monte Carlo analysis plot showing the effect of mismatch variation in the resistive voltage divider.

The mismatch effect of the voltage-divider resistors in generating the control-voltage of the VCRO is analyzed with the Monte Carlo simulation result for 200 samples indicating the effect of resistance mismatch variation on the VCRO frequency at typical-typical (TT) process corner and is shown in Fig.4.26. The mean frequency and the standard deviation for this graph are 151.12MHz and 0.67MHz respectively. From this plot, it is quite clear that the reference frequency for 99.7% of the tags will be in the range of 149.07MHz to 153.09MHz. Hence, the voltage-divider resistor-mismatch will not be a bottle-neck issue in the operation and performance of the insect telemeter. The VCRO control-voltage may also be adjusted externally (external trimming) using the probe-pad if at all required.

Power-supply-rejection-ratio (PSRR) is extracted from the VCRO output using the Cadence SpectreRF PSRR characterization testbench for VCRO. The PSS (periodic steady-state) followed by PXF (periodic transfer function) analysis engines in

SpectreRF were employed for this purpose. The resistive divider is used to provide the V_Control and the output is loaded by the input capacitance of the buffer that drives the frequency divider. Fig. 4.27 shows the simulated PSRR for the oscillator over the frequency domain up to around 1.5GHz as an offset from the base frequency of around 150.87 MHz.

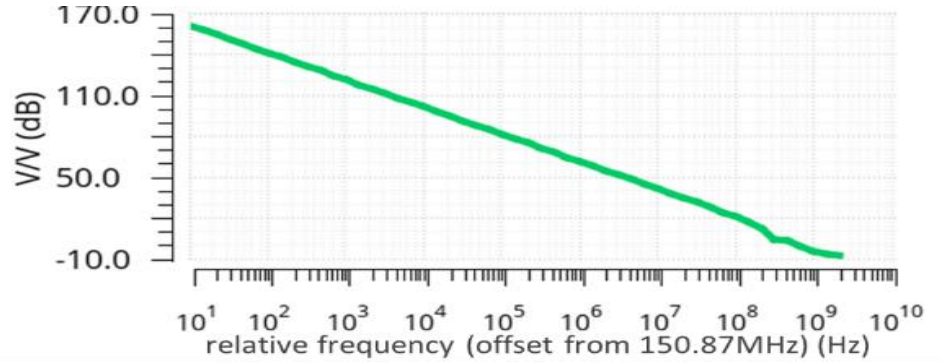



Fig. 4.27. PSRR for the VCRO at an offset of up to 1.5GHz

### 4.3.1.2 Temperature variation

The foraging activity of bees and other insect pollinators normally occur within an environmental temperature range of 14°C to 38°C [48, 66]. Hence, to understand the operation of the tag in this temperature range, simulations were performed for temperature variation from 10°C to 40°C. Fig. 4.28 shows that in the operational temperature range, the tag's frequency varies between 118.43MHz and 185.11MHz. This is around 2.78MHz change per degree centigrade fluctuation in the temperature, and Table 4.2 shows the parameters of the tag in this frequency range. From this table, it can be seen that with the change in environmental temperature, the sleep-time, burst-signal width, and data-rate will vary considerably, but, as long as the frequencies are detectable by the receiver, this will not have any impact on the insect tracking, as the tag identification codes are frequency invariant. This is an additional benefit of this digitalized telemeter insect-tag over the conventional analog-based telemeter where the frequency stability is stringent and paramount for the correct identification of individual insects.

### 4.3.1.3 Voltage variation

Fig. 4.29 depicts the effect of supply-voltage fluctuation on the oscillator frequency at typical-typical process corner and 27°C ambient temperature. It changes at the rate 1.3MHz per mV change in the supply-voltage. However, as discussed in the above

section 4.3.1.1, due to the skeletal telemeter circuit-size and isolated power supply-line provided for the oscillator, a significant fluctuation in the supply-voltage due to power-supply noise is not expected.

Table 4.2
Performance of the tag at various frequencies

| REFERENCE FREQUENCY (MHz) | TIME PERIOD (s) | BURST SIGNAL WIDTH (ms) | SLEEP TIME (s) | BASEBAND DATA RATE (b/s) |
|---|---|---|---|---|
| 115 | 2.334221357 | 18.23610435 | 2.315985252 | 438.6901855 |
| 125 | 2.147483648 | 16.777216 | 2.130706432 | 476.8371582 |
| 135 | 1.988410785 | 15.53445926 | 1.972876326 | 514.9841309 |
| 145 | 1.851279007 | 14.46311724 | 1.83681589 | 553.1311035 |
| 150 | 6.66667E-09 | 13.98101333 | 1.775588693 | 572.2045898 |
| 155 | 1.731841652 | 13.5300129 | 1.718311639 | 591.2780762 |
| 165 | 1.626881552 | 12.71001212 | 1.614171539 | 629.4250488 |
| 175 | 1.533916891 | 11.98372571 | 1.521933166 | 667.5720215 |
| 185 | 1.451002465 | 11.33595676 | 1.439666508 | 705.7189941 |

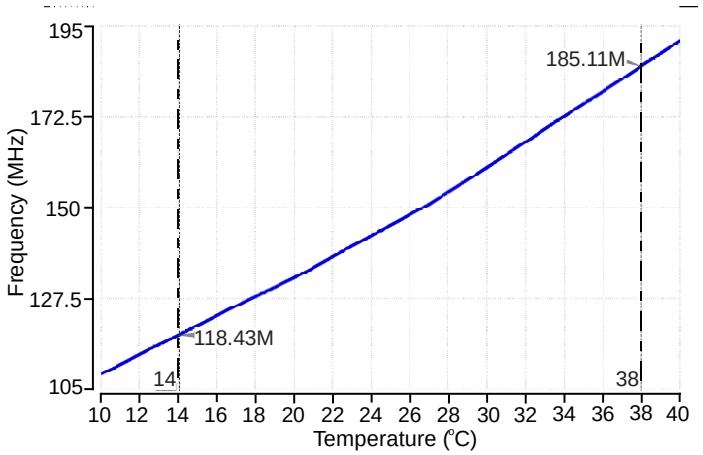



Fig. 4.28. Simulated frequency drift due to environment temperature variation.

### 4.3.1.4 Process variation

Process variation is the change in the transistor attributes in terms of width, length, oxide-thickness, and threshold-voltage during fabrication. This variation has always been a serious concern to the designer in the yield of working chips, particularly when the size of the circuit is quite large [67]. To consider the effect of process variation on the running frequency, the VCRO in Fig. 4.21 (with OP-resistors) was simulated at various process corners, Slow-Slow (SS), Slow-Fast (SF), Typical-Typical (TT), Fast-Slow (FS), and Fast-Fast (FF). The results are plotted in Fig. 4.30. Here, for this oscillator the frequency varies significantly with process variation, but,

this variation always has an associated statistical distribution with mean and standard deviation [68]. The TT corner is essentially the mean of this distribution. Since the size of the circuit is very small in this insect-tag design, a reasonable yield for this telemeter chip can be delivered [58]. The yield for this telemeter design is

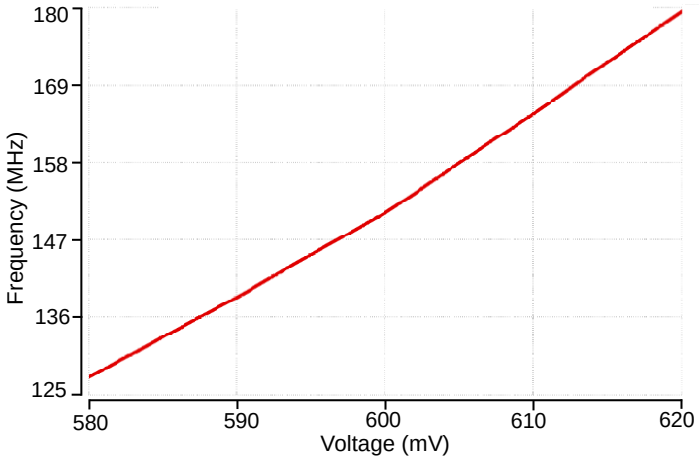



Fig. 4.29. The influence of supply-voltage variation on oscillator frequency (@ typical-typical process corner and 27$^0$C temperature).

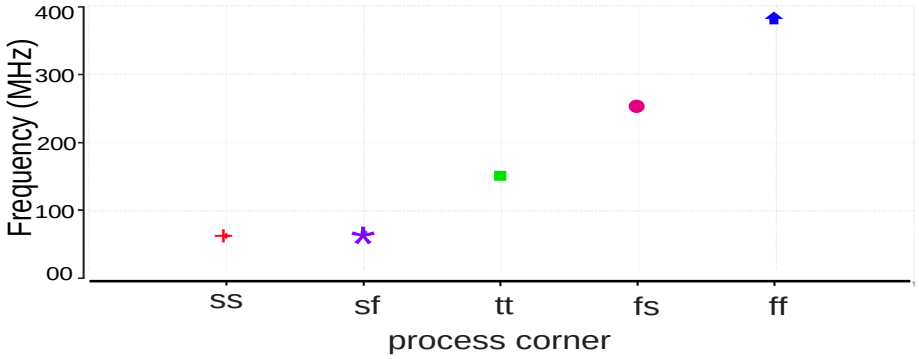



Fig. 4.30. Frequency variation for the VCRO (with OP-resistors) at various process corners.

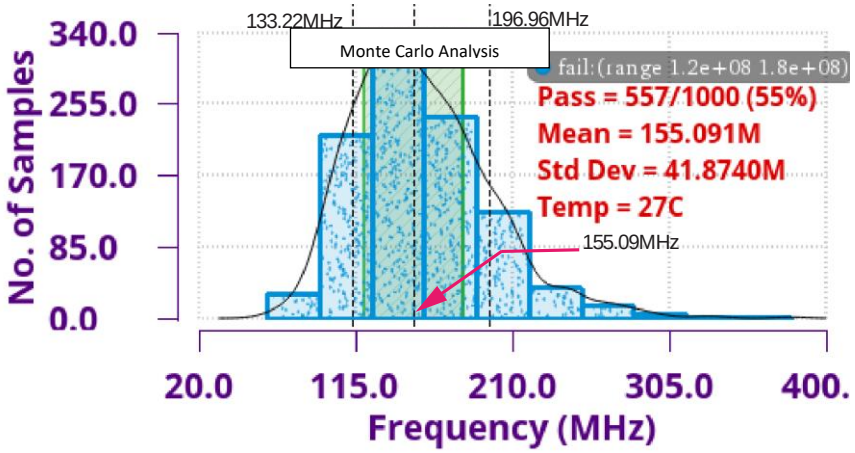



Fig. 4.31. Monte Carlo simulation result of sample distribution vs. frequency for various process corners.

predicted by running the full Monte-Carlo simulation for 1000 sample points. The tags with frequencies in the range 120MHz to 180MHz will be binned for the telemeter application and the rest will be discarded. Fig. 4.31 shows the Monte-Carlo simulation result with 55% (557/1000) successful yield. The passing range is shown by the green shaded region in the figure. The associated mean frequency and standard deviation are 155MHz and 42MHz respectively.

### 4.3.2. Circuit Simulation and Discussion

The new insect telemeter circuit design was simulated in 28-nm Global Foundries (GF) HPP CMOS process technology. The total chip-size along with the bond-pads is 1mm$^2$ [Fig. 4.32] and the actual transmitter circuitry occupies only around 1012 $\mu$m$^2$ as shown in Fig. 4.34. With such miniaturization, the weight of the silicon die will be negligible, and tag load will be constituted by battery, antenna, and any packaging. The circuit employs 13 bond-pads as labeled on the die photo. An off-chip matched external wire antenna will be deployed with the fabricated die.

The complete transmitter circuit was extensively simulated using Cadence spectra. Parasitic extracted post-layout simulation was also carried out and performance difference compared with the pre-layout simulation was found to be negligible. Since the entire circuitry, except the output driver, employs 0.6V supply-voltage, the VCRO is in particular quite sensitive to process variation [69]. To ensure that stable 150MHz oscillation is achievable in all cases, Periodic Steady-state (PSS) simulation was carried out for the VCRO for various process corners. Fig. 4.33 shows the V_Control vs. frequency plot where it can be seen that with process variation the running frequency of the oscillator changes considerably. However, the tuning range of the oscillator is wide enough to allow V_Control to set the frequency to 150MHz in each case.

The performance of the circuit is demonstrated for the tag code 10001110 with Fig. 4.35 showing the timing diagram for the PISO in strobing the code. Fig. 4.36 provides all the waveform diagrams in the generation of the final burst-mode low duty-cycle modulated output signal. The circuit simulated duty cycle comes out to be 0.00785 with the baseband data rate of 572.6b/s which is very close to the theoretically desired duty-cycle of 0.008. The code appears only when the LDC signal is high, that is between the interval T1=1.768s and T2=1.782s as shown in Fig. 4.36 (a) and in agreement with the PISO strobing waveform in Fig. 4.35. Fig. 4.36 (a) also illustrates

the carrier frequency in accordance with the logical values of the baseband signal (tag identification code). Table 4.3 summarizes the average dissipation by various circuit blocks in the transmitter's power budget. It is observed that after the 14th FD (flip-flop) the average power of successive FD remains roughly the same at 16.2nW. This could be mainly because at lower frequency static power consumption becomes more significant than dynamic power. The total power consumed is around 6.54$\mu$W while only 2.57$\mu$W is utilized during sleep mode with the rest being attributable to the transmission burst.

The necessity for the low duty-cycle signal in the proposed design could be explained using the following equation,

$$P_{avg} = DP_t + (1-D)P_S + P_C \tag{4.3}$$

Where, $D$ is the duty-ratio, $P_{avg}$ is the total average power dissipated by the tag, $P_c$ is the continuous power dissipated by the sub-blocks 1 to 5 as shown in Fig. 4.4, which is measured to be 4.21742$\mu$W. Next, $P_s$=0.596 $\mu$W is the power consumed by the sub-blocks 6 to 8 during the sleep-state and these same sub-blocks dissipate comparatively much larger power of $P_t$=434$\mu$W during the code generation and transmission mode. Hence, from (3) the average power consumption, $P_{avg}$ for this tag, at 0.0078 duty-ratio (D=0.0078) can be determined to be 8.2$\mu$W. On the contrary, if the LDC signal was not used to shut-off these most power-consuming sub-blocks (from 6 to 8), and the consequent code generation and transmission mode are not intermittent (periodic), the total average power dissipation ($P_{avg}$) would have been 438$\mu$W. There is thus over 50 times reduction in power dissipation due to the LDC signal, and it enables a 4mAh [26] battery to gain 53 times longer life than a tag design without the LDC signal.

Table. 4.3
Power consumption by various circuit blocks in 28nm CMOS process technology

| Transmitter Block | | Average power consumption (µW) |
|---|---|---|
| SUB BLOCK1 | VCRO | 1.083 |
| SUB BLOCK2 | set of 28 frequency dividers | 1.479 |
| SUB BLOCK3 | AND | 0.00271 |
| SUB BLOCK4 | AND (LDC) | 0.00135 |
| SUB BLOCK5 | AND (CLK) | 0.00136 |
| SUB BLOCK6 | CODE GENERATOR | 0.2 |
| SUB BLOCK7 | MODULATOIN | 0.024 |
| SUB BLOCK8 | DRIVER | 3.745 |
| TOTAL | | 6.53642 |

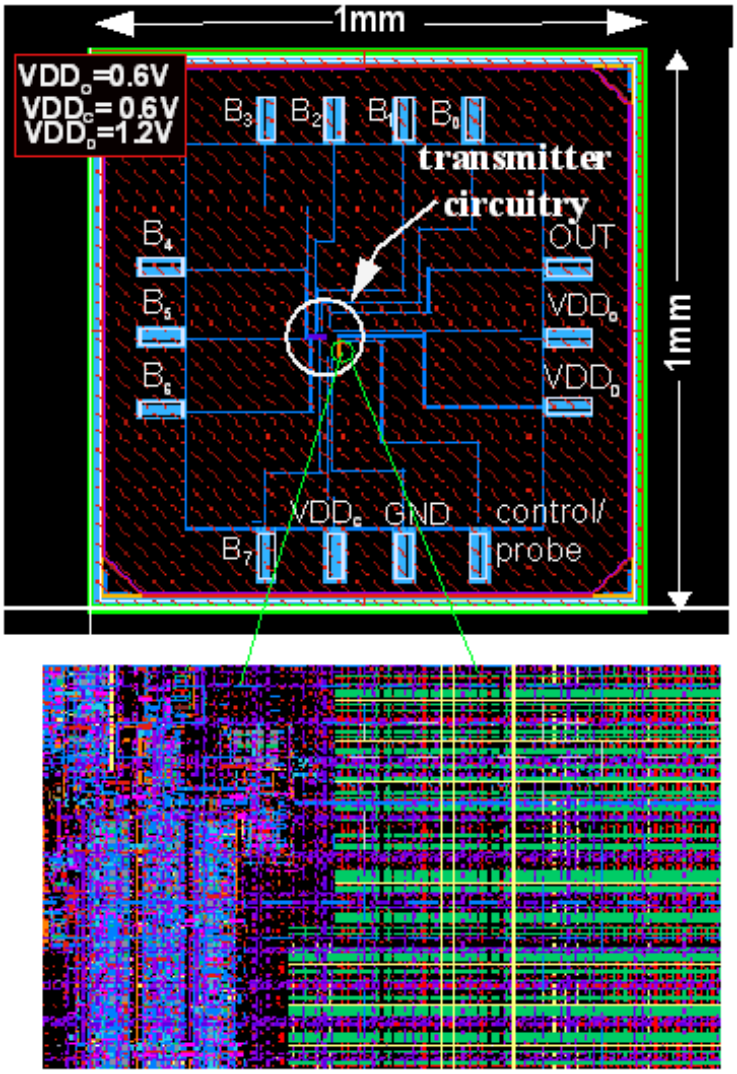



Fig.4.32. Layout of the die with bond pads along-with zoomed-in view of fill pattern-density for Rx, poly, n-well and all the 11 metal layers.

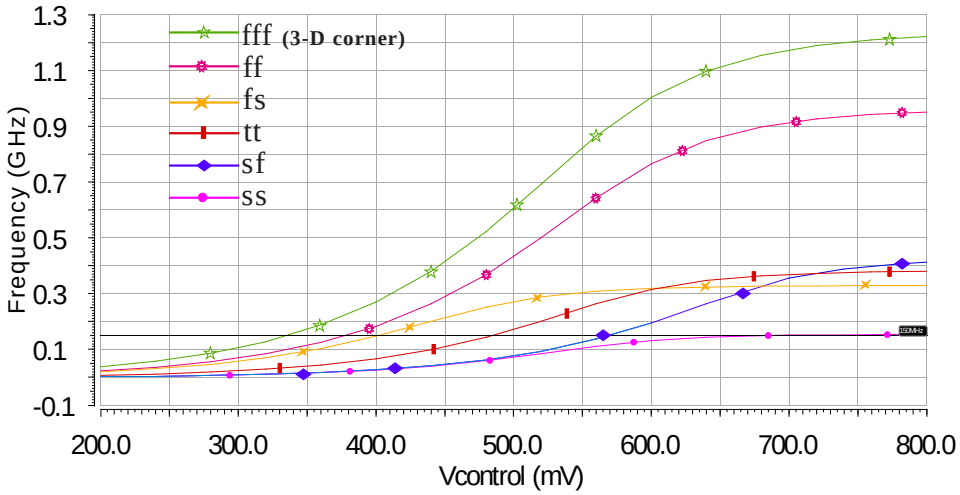



Fig. 4.33. Frequency versus V_Control for various process corners.

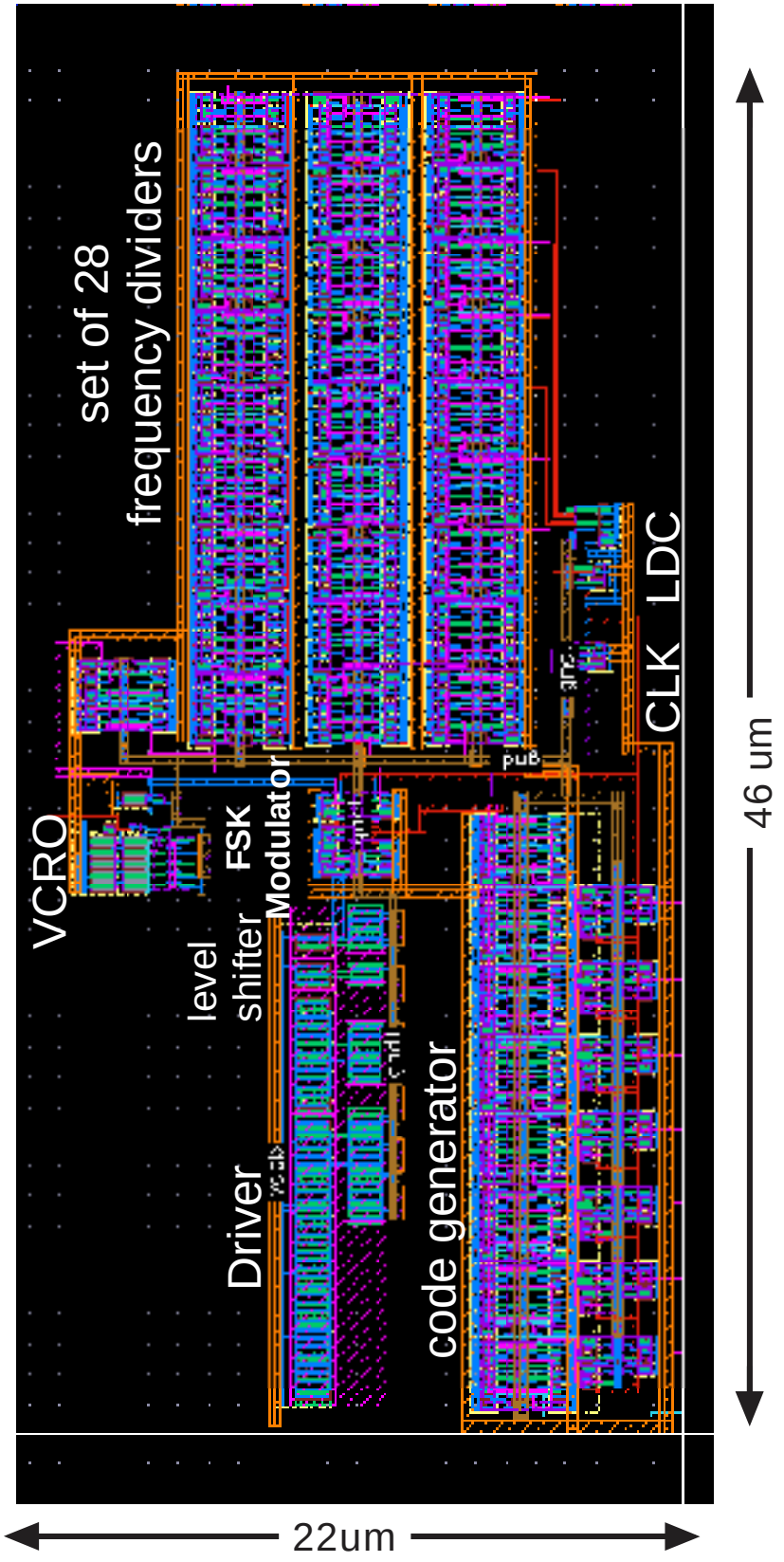



Fig. 4.34. Zoomed in layout of the transmitter circuit.

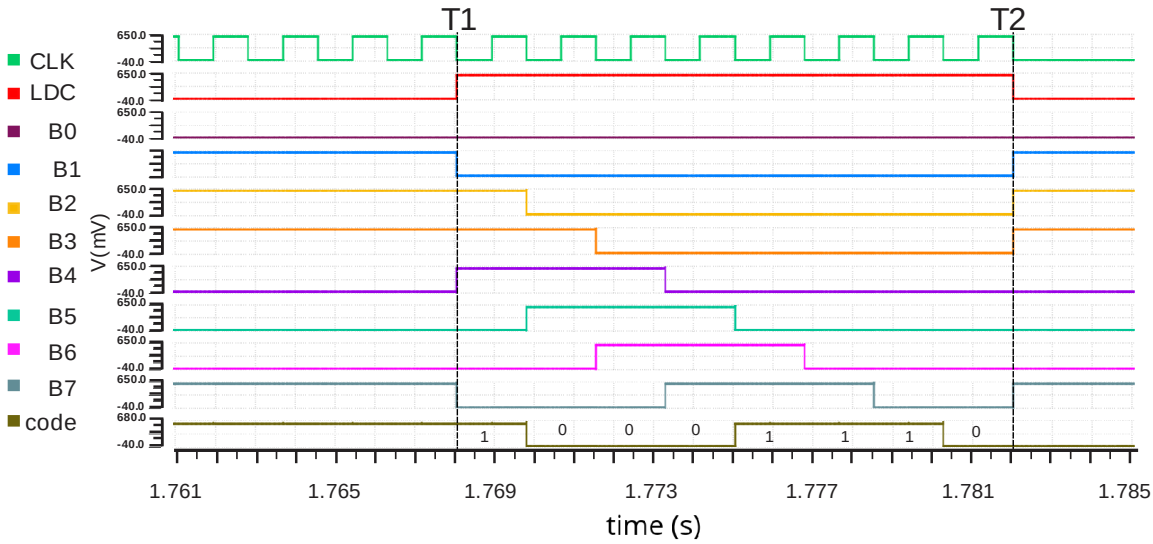



Fig. 4.35. The timing diagram for the generation of the code of 10001110.

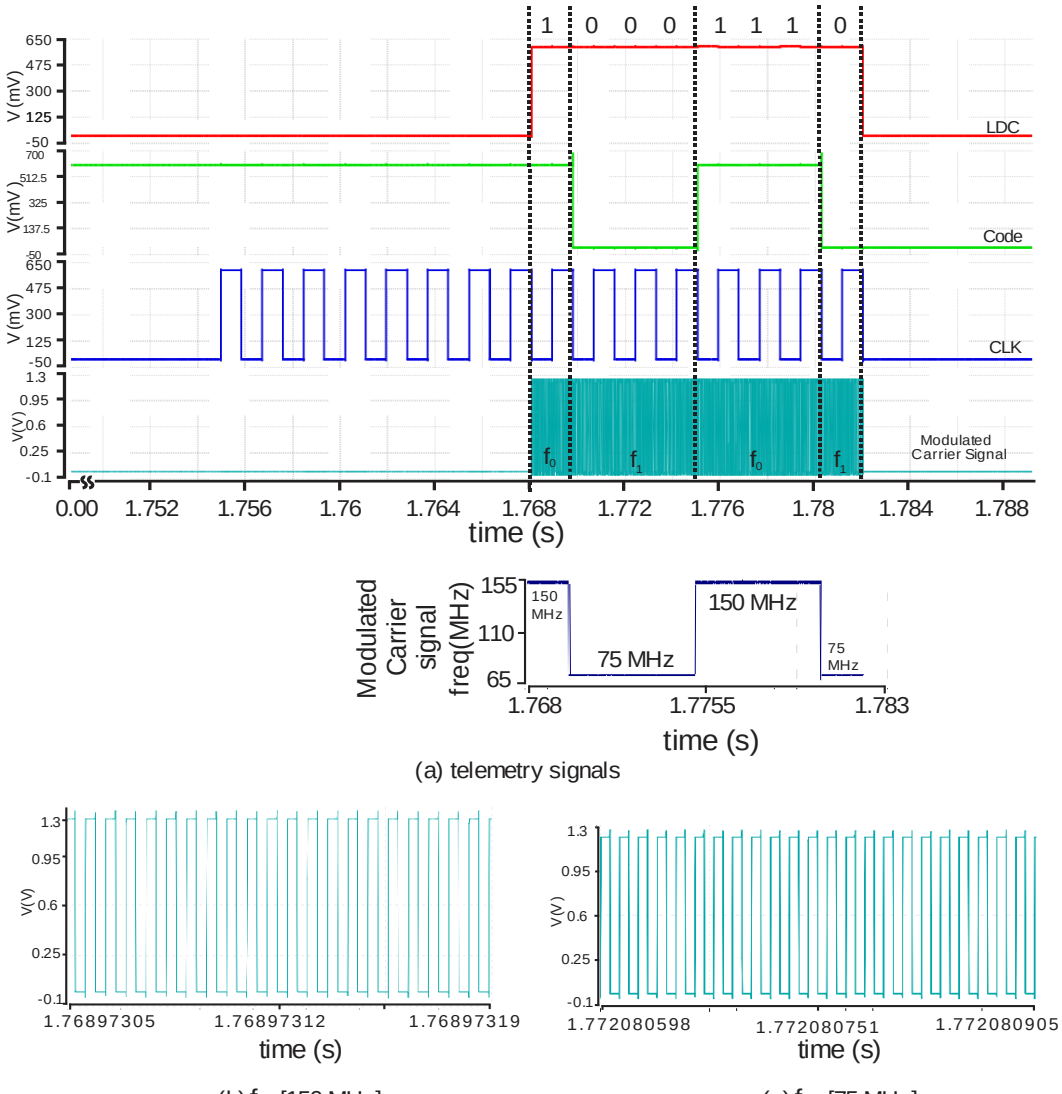



Fig. 4.36. The transient waveform of the transmitter for code 10001110.

Table 4.4

Performance Comparison of the proposed VHF telemeter and VHF prior arts

| Reference | [17] | [18] | [70] | [71] | This Work |
|---|---|---|---|---|---|
| Weight Without Battery(mg) | 270 | 120 | NA | 140 | **< 15** |
| Weight With Battery(mg) | 390 | 200 | 240 | 220 | **< 95** |
| Frequency(MHz) | 148-149 | 148.5 | 147-168 | 148-220 | 150-75‡ |
| Power during burst mode(mW) | 1.15 | 2.7 | NA | 3.15 | **0.44** |
| Pulse width (msec) | 10 | 10-20 | 20 | 20 | 14 |
| Pulse interval (sec) | 0.1-0.25 | 0.8-1.5 | 2 | 1.5 | 1.78 |
| Tag Dimensions | 86mm X 4mm X 4mm | 12mm X 5mm X 1.5mm | 9.6mm X 5mm X 3mm | 8mm X 4mm X 2.8mm | **5mm X 5mm X 2.5mm** |
| Avarage Current (μA) | 45-70 | 9-35 | NA | NA | **8-10** |
| Lifespan (Days) | 5-6 | 9-22 | 13 | 4-8 | 16 |
| Implementation | LDE | LDE | ASIC [2.8mm$^2$] | LDE | ASIC [1mm$^2$] |
| Binary code | NO | NO | YES | NO | YES |

‡ 150MHZ and 75 MHz are the two carrier frequencies for the FSK transmitter. **LDE**- lumped discrete elements. **ASIC**- Application Specific Integrated Circuit

### 4.3.3. Performance comparison of the proposed VHF insect telemeter with VHF prior art

The complete insect-tag would consist of, a 4 mAH silver-oxide Sony battery which weighs around 80 mg, a 10 cm long thin-wire whip-antenna weighing 3 mg, and the transmitter circuit on 1mm$^2$ silicon-chip weighing under 2mg. Hence, the total weight of the composite tag consisting of all the components mounted over the battery along-with glob-top epoxy encapsulation (packaging), is expected to be around 95mg or less. This would reduce the VHF tag weight by at least 52% and the volume by 58% of the presently existing smallest active 200mg VHF telemeter-tag on PCB [69], and hence, achieve the original objective of this work. The comparison of the new CMOS VHF telemeter in terms of tag weight, dimensions, average current, frequency, power during signal generation and transmission, pulse width, pulse interval, and life span with previous VHF telemeters are provided in Table 4.4. The table includes a commercial Nano-tag [70] which uses a 2.8 mm$^2$ ASIC chip implementing a digital-code for the tag identification and weighs 250mg. This design is 50mg heavier than the tag in [18] even after some ASIC implementation, most likely due to the use of discrete oscillator components in addition to the ASIC chip, and hence is not suitable for tracking small insects. The core novelty of this telemeter circuit lies in the digital low duty-cycle clock generator replacing the analog signal generator of [18] which enables the ultimate goal of reduced tag weight and size to facilitate tracking of tiny creatures. In addition, it will transmit

digitally coded signals allowing a large number of tags to be identified at the same frequency and will also eliminate the need for a very stable clock for tag identification. This is achieved with a much smaller ASIC chip-size compared to the ASIC digital code incorporated in Nano-tag [70] as well as a much smaller tag weight compared to [18].

### 4.3.4. Frequency Spectral Analysis of The Modulated Burst-Mode signal

The frequency spectrum of the transmitted burst is now analyzed considering here for simplicity a sine-wave approximation (at the matched external wire antenna output) of the burst-mode modulated carrier signal, *f(t)* so that,

$$f(t)=\begin{cases} V\left(\sin(\omega_0 t)+1\right) & \textit{for logic 1} \\ V\left(\sin(\omega_1 t)+1\right) & \textit{for logic 0} \end{cases} \tag{4.4}$$

Here, $\omega_0$ and $\omega_1=\omega_0/2$ are the two carrier frequencies with *V* (*half of the peak-to-peak carrier signal*) being the amplitude and DC offset. The Fourier series analysis of the signal is possible because the two carrier signals have a common multiple $\omega_1$ and are phase synchronized which allows the signal to be periodic [72]. The Fourier even-coefficients ($a_n$) and odd-coefficients ($b_n$) of the 8-bit coded signal are derived as follows:

For each logic "1" at $k_1^{th}$ bit-position from left to right where $0 \le k_1 < 8$:

$$a_n=\frac{2V}{T}\int_{\frac{K_1T}{8}}^{\frac{(K_1+1)T}{8}}\left(\sin\left(\omega_0 t\right)+1\right)*\cos\left(\frac{2n\pi t}{T}\right)dt \tag{4.5}$$

When $n \neq 2^{20}, 2^{21}$ the integral in (2) collapses to,

$$a_n=\frac{8V\omega_0 T}{\left(T\omega_0\right)^2-\left(2n\pi\right)^2}\left[\sin\left(\frac{n\pi}{8}\right)*\sin\left(\frac{n\pi}{8}\left(2K_1+1\right)\right)\right] \tag{4.6}$$

$$b_n=\frac{2V}{T}\int_{\frac{K_1T}{8}}^{\frac{(K_1+1)T}{8}}\left(\sin\left(\omega_0 t\right)+1\right)*\sin\left(\frac{2n\pi t}{T}\right)dt \tag{4.7}$$

When n ≠ $2^{20}$, $2^{21}$ the integral in (4) collapses to,

$$b_n = \frac{4V\omega_0 T}{\left(T\omega_0\right)^2 - \left(2n\pi\right)^2}\left[\sin\left(\frac{n\pi}{8}\right) * \cos\left(\frac{n\pi}{8}\left(2K_1 + 1\right)\right)\right] \tag{4.8}$$

For each logic "0" at $k_0^{th}$ bit-position from left to right where $0 \le k_0 < 8$:

$$a_n = \frac{2V}{T}\int_{\frac{K_0 T}{8}}^{\frac{(K_0+1)T}{8}} \left(\sin\left(\omega_1 t\right) + 1\right) * \cos\left(\frac{2n\pi t}{T}\right) dt \tag{4.9}$$

When n ≠ $2^{20}$, $2^{21}$ the integral in (6) collapses to,

$$a_n = \frac{4V\omega_0 T}{\left(\frac{T\omega_0}{2}\right)^2 - \left(2n\pi\right)^2}\left[\sin\left(\frac{n\pi}{8}\right) * \sin\left(\frac{n\pi}{8}\left(2K_o + 1\right)\right)\right] \tag{4.10}$$

$$b_n = \frac{2V}{T}\int_{\frac{K_0 T}{8}}^{\frac{(K_0+1)T}{8}} \left(\sin\left(\omega_1 t\right) + 1\right) * \sin\left(\frac{2n\pi t}{T}\right) dt \tag{4.11}$$

When n ≠ $2^{20}$, $2^{21}$ the integral in (8) collapses to,

$$b_n = \frac{2V\omega_0 T}{\left(\frac{T\omega_0}{2}\right)^2 - \left(2n\pi\right)^2}\left[\sin\left(\frac{n\pi}{8}\right) * \cos\left(\frac{n\pi}{8}\left(2K_0 + 1\right)\right)\right] \tag{4.12}$$

When n = $2^{20}$, $2^{21}$; $a_n = 0$ and $b_n = \frac{V}{16}$ for every bit in the code. In the above equations,

$T = \frac{2^{21} * 2\pi}{\omega_0}$ stands for the time frame of the 8-bit code, and n is the $n^{th}$ harmonic of the fundamental frequency, (*1/T*). The above equations could be combined to find the consolidated Fourier series coefficients of any 8-bit coded signal. For example, it has been implemented here for the code 10001110 as shown below:

$a_0 = V$ ,

$$a_n = \frac{-8V}{\omega_o T} * \left( \frac{2\left(\frac{2\pi n}{\omega_o T}\right)^2 + 1}{\left(1 - 4\left(\frac{2\pi n}{\omega_o T}\right)^2\right) * \left(1 - \left(\frac{2\pi n}{\omega_o T}\right)^2\right)} \right) * \sin\left(\frac{n\pi}{8}\right) *$$
$$\left[ \sin\left(\frac{n\pi}{8}\right) + \sin\left(\frac{9n\pi}{8}\right) + \sin\left(\frac{11n\pi}{8}\right) + \sin\left(\frac{13n\pi}{8}\right) \right] \quad (4.13)$$

for n ≠ $2^{20}$, $2^{21}$; and, $a_n = 0$ for n=$2^{20}$, $2^{21}$

Also,

$$b_n = \begin{cases} 0 & for\ n \neq\ 2^{20},\ 2^{21} \\ \frac{V}{2} & for\ n=\ 2^{20},\ 2^{21} \end{cases} \quad (4.14)$$

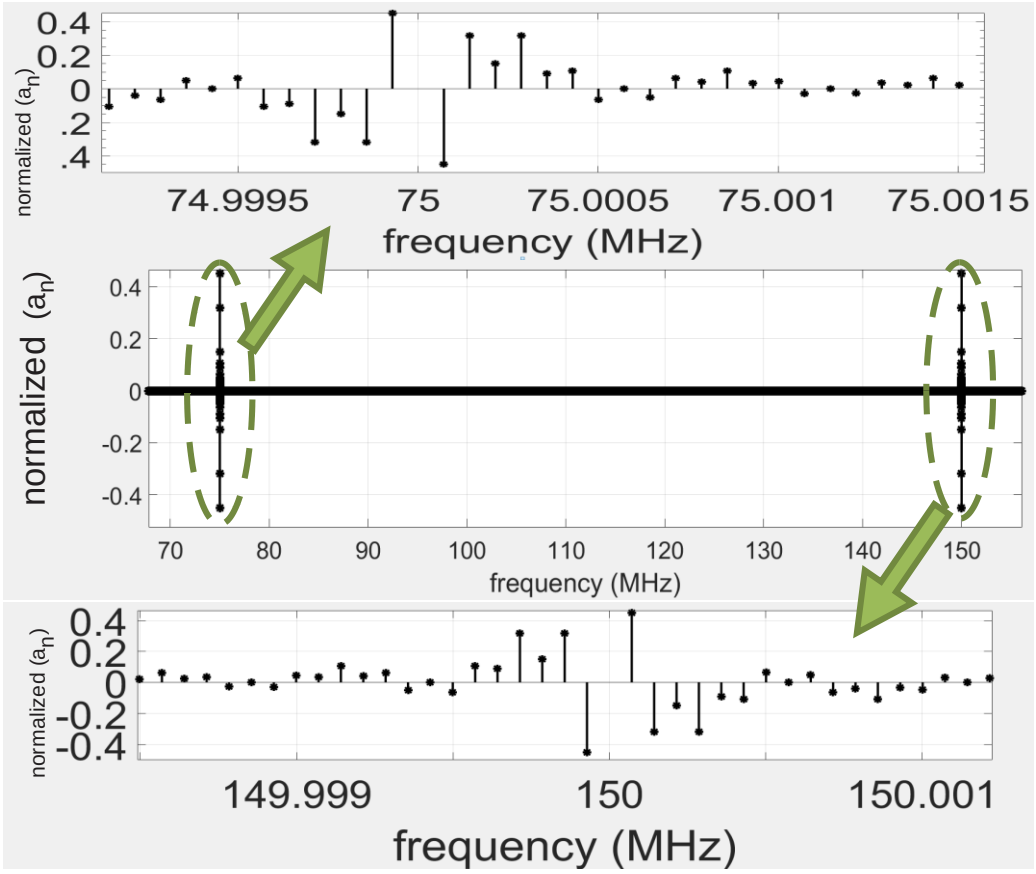



Fig. 4.37. The plot shows the normalized $a_n$ with respect to V versus frequency.

In the above analysis, n=$2^{21}$ and n=$2^{20}$ correspond to the angular frequencies $\omega_0$ and $\omega_1$ respectively with $f=n/T$. The normalized MATLAB plot of (10) with respect to $V$ is

calculated and shown in Fig. 4.37 to visualize the relative strength of $a_n$ for various frequencies. By looking at the values of the Fourier coefficients as derived above it can be seen that maximum power spread is present around the two carrier frequencies $\omega_0$ and $\omega_1$ as expected in FSK modulation.

For all the process corners and for various control voltage, Fourier series of the signal were performed, and the even and odd coefficients were calculated and analyzed with the help of MATLAB.

## 4.4. Design Implementation on TSMC 65nm Process

The chip designed in IBM 8HPP 28nm process technology could not be fabricated due to the extremely high fabrication cost. Therefore, the complete digital telemeter circuit was redesign in TSMC 65nm process technology. This section discusses the digital telemeter circuit implementation and fabrication in 65nm technology.

Fig. 4.38 shows the layout of the complete digital telemeter circuit consisting of Voltage Controlled Ring Oscillator (VCRO), LDC generation circuit, Clock (CLK) generation circuit, sets of 28 Frequency Dividers (FDs), Parallel Input Serial Output (PISO) shift register, Frequency Shift Keying (FSK) Modulation circuit, and tapered inverters as the output driver. The VCRO was placed in a triple well to isolate it from the main substrates to reduce supply noise. Due to the chip size and limited numbers of bond pads that can be placed on the 1mm X 1mm chip, the 8 wire lines which set the 8-bit digital code for the telemeter were alternatively shorted among themselves leaving only four 8-bit code setting options, that is. 11111111, 10101010, 01010101, and 00000000. However, for the real telemeter, electrical fuses will be used for setting the 8-bit telemeter code. In this, a high current will be sent to blow off the fuse and keep the connection of the 8 wire lines either with the supply voltage VDD or with the ground (GND) to set unique binary codes for each tag.

For the experimental purpose, 3 circuits were placed on the 1mm X 1mm chip. The first circuit is a simple circuit to generate 0.0078 duty-cycle burst mode signaling using 28-FDs without any digital coding scheme on it. The second circuit is the complete digital telemeter circuit to produce the coded burst mode signaling but without any kind of ESDs and the third circuit consists of the complete digital telemeter circuit along with ESDs and on-chip decoupling capacitors [73, 74] placed

on VDD_RO and VDD_D power lines as marked in Fig. 4.39. The circuit layout following complete verification including DRC and LVS check and post-layout performance simulation after including the PEX extracted data from the layout was set for tape out. Fig. 4.39 shows the complete layout of the 1mm X 1mm chip including the three circuits and ESD and corner cells [75] in a ring structure for better ESD and latch-up protection. The fabricated chip was packaged in 28 lead open cavity Quad Flat No-lead (QFN) and its bounding diagram is shown Fig. 4.40. Fig. 4.41 shows the picture of 1mm X 1mm fabricated silicon chip and the complete digital telemeter circuit with corresponding bond pads are marked on the picture.

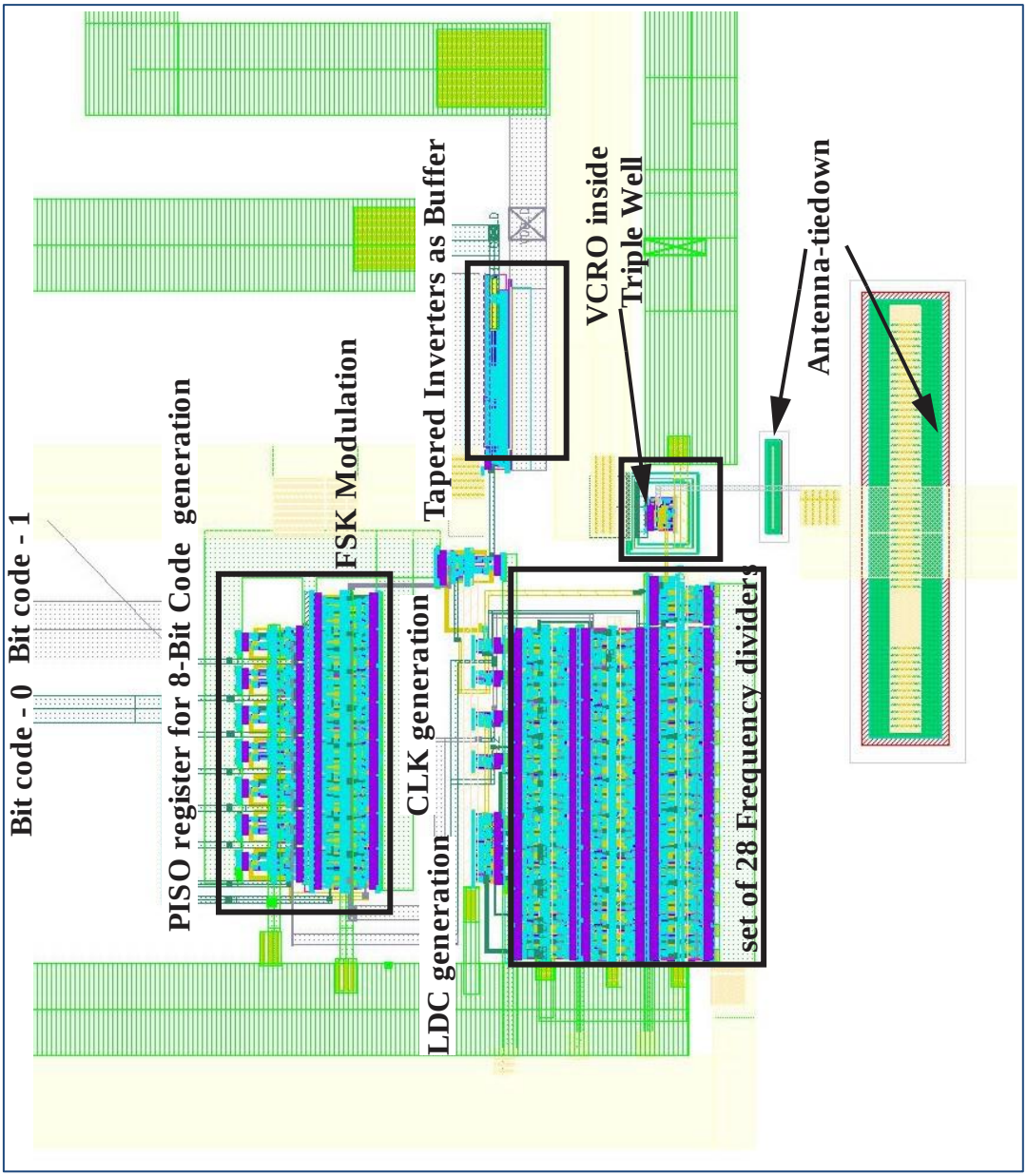



Fig. 4.38. Complete digital telemeter circuit layout in TSMC 65nm process technology.

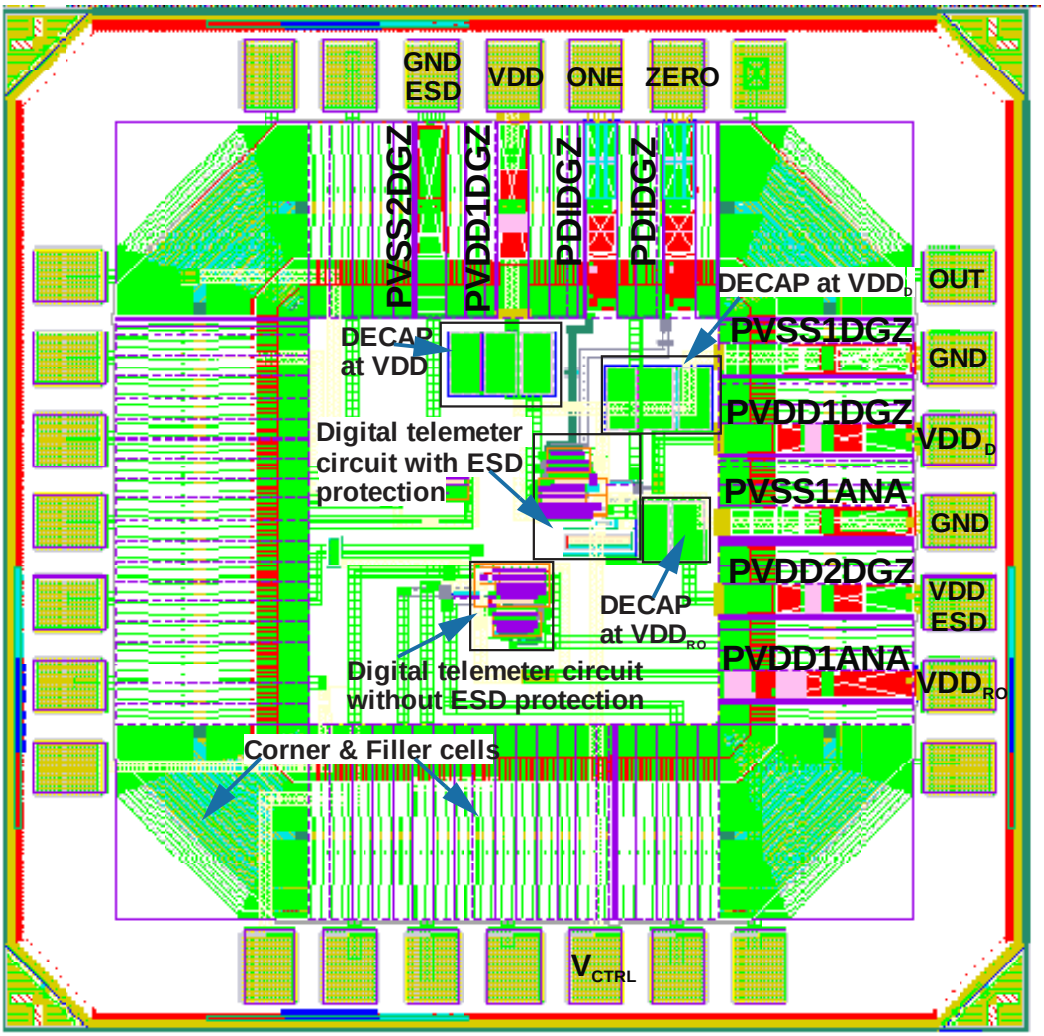



Fig. 4.39. 1mm X 1mm complete chip layout with searing, bond pads, and ESD filler and corner cells.

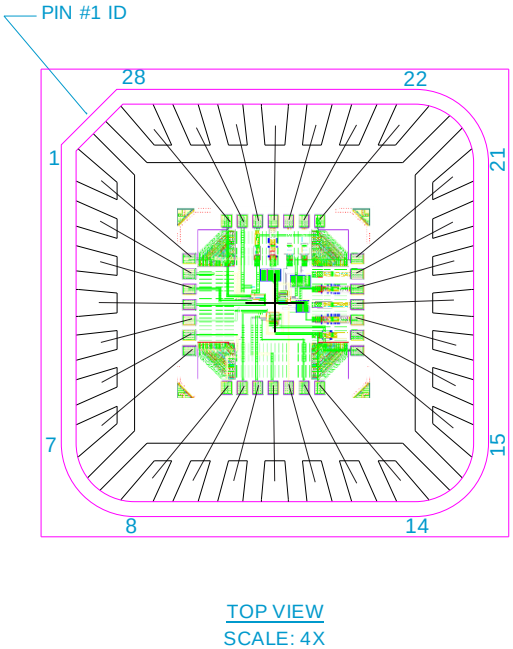



Fig. 4.40. Bonding Diagram of 4mm X 4mm QFN 28 Lead open Cavity package. Part no. QP-QFN28-4MM-4MM.

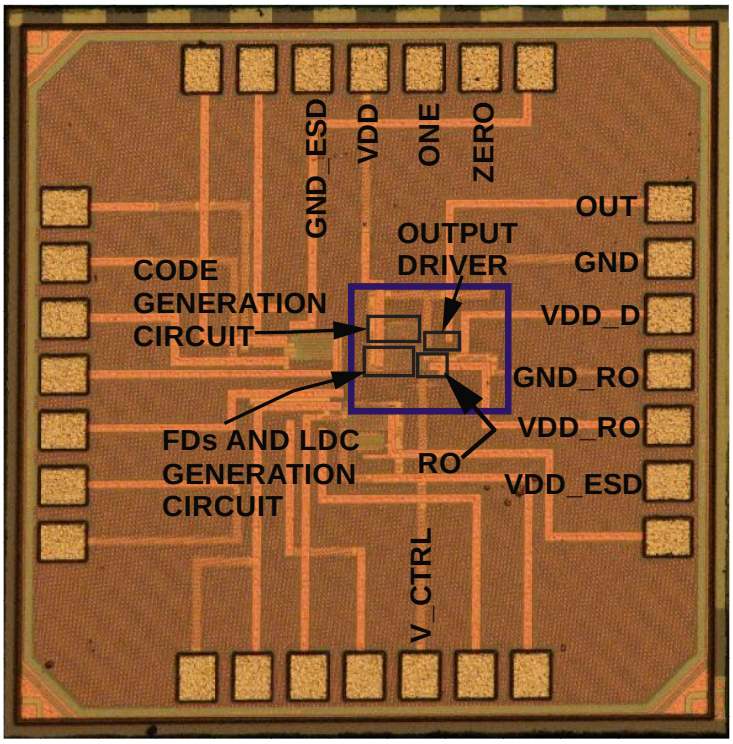



Fig.4.41. TSMC 65nm 1mm X 1mm chip die picture.

## 4.5. Experimental Analysis

### 4.5.1. PCB Test Board Design

The chip received from the foundry was packaged into a 5mm X 5mm, 0.5mm pitch 28 lead open cavity QFN Package which cannot be tested directly due to the very small size of the package lead. Hence, a two-layer PCB test board was design using the Altium Designer tool and was fabricated. The PCB consists of a through-hole mounting type 28 (4 x 7) Pos QFN Socket, decoupling capacitors, 50-ohm SMA connector. Fig. 4.42 shows the schematic of the components used in the PCB. The top PCB layer has mounted QFN socket dimensioned 30mm X 30mm with 0.5mm mate pitch, and SMA connector as shown in Fig.4.43 and the bottom layer of the PCB consists of decoupling capacitors and ground plane as shown in Fig. 4.44. Power supply tracks of 1mm width were routed on the top layer but for routing the signal track both top and bottom layers were used. The socket footprint was designed with a plated round through-hole of diameter 1.2mm with a hole size of 0.8mm for the lead. The pitch of the adjacent hole was kept 1.5mm. Decoupling capacitors were used to reduce the impact of supply noise due to the long routing wire inductance coming from the power supply to the socket. Four capacitors were placed in parallel

connected between each supply voltage line and the ground plane. For this SMD 0805 (2.0mm x 1.3mm) ceramic capacitor footprint is used and is placed as close as possible to the socket lead to reduce the line inductance effect.

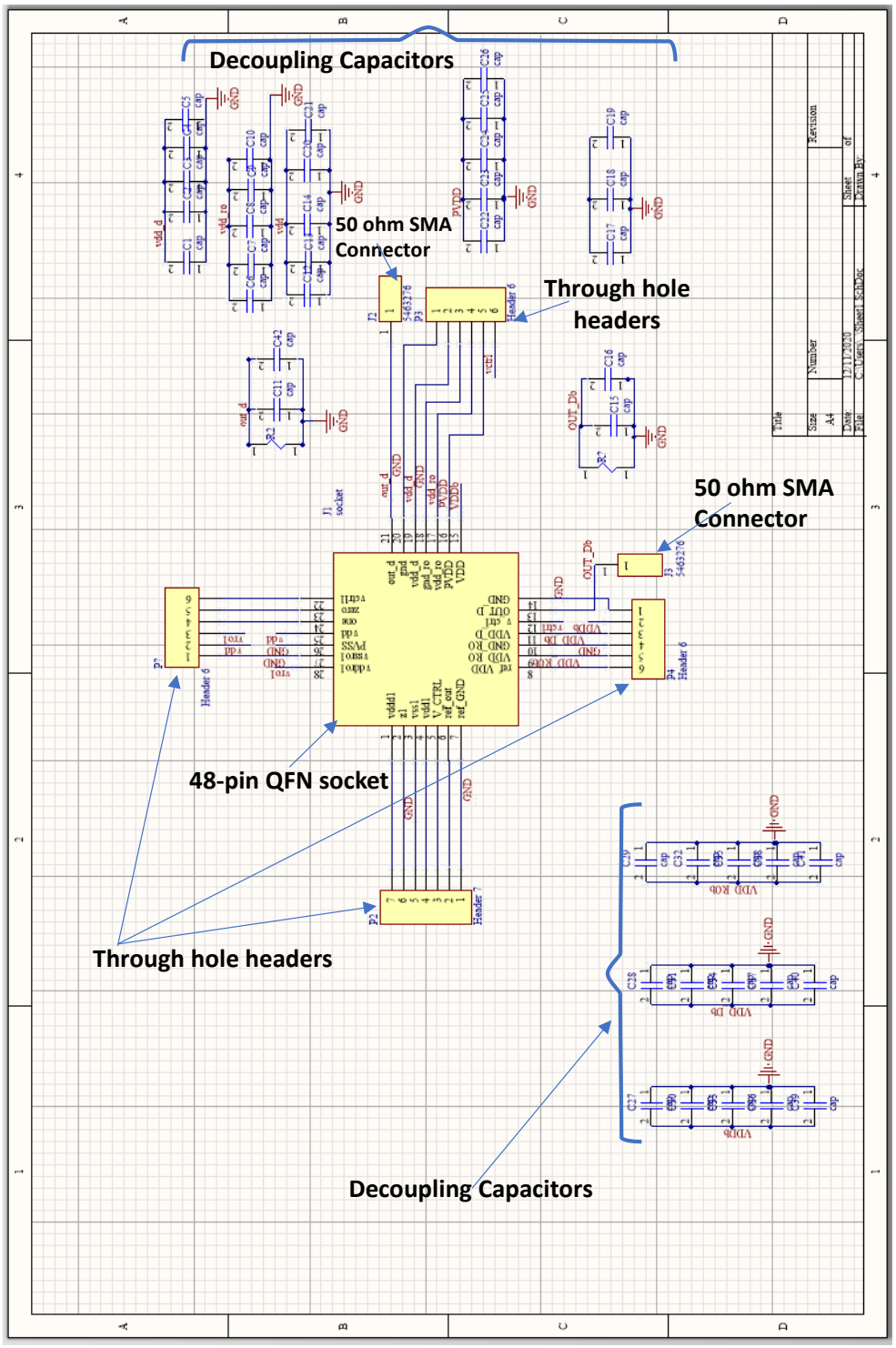



Fig. 4.42. Schematic of the fabricated 2-layer PCB board for testing the chip.

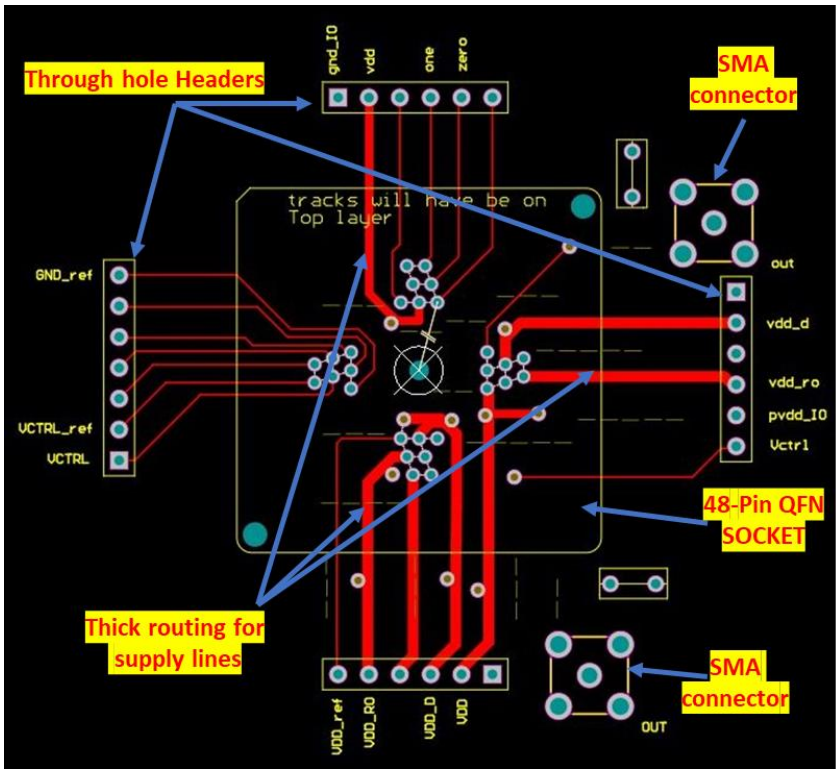



Fig.4.43 Top metal layer layout of the PCB board

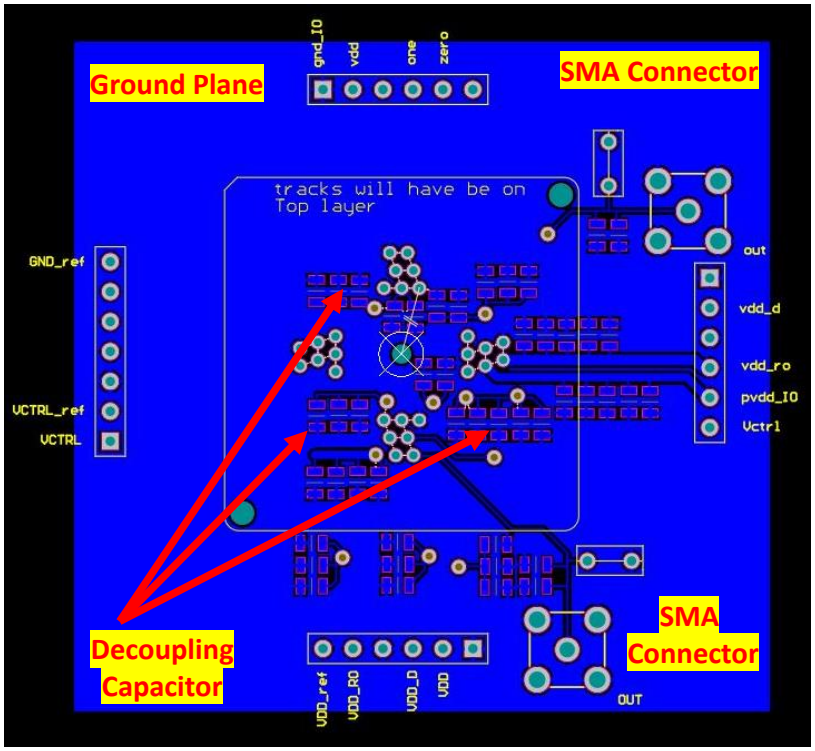
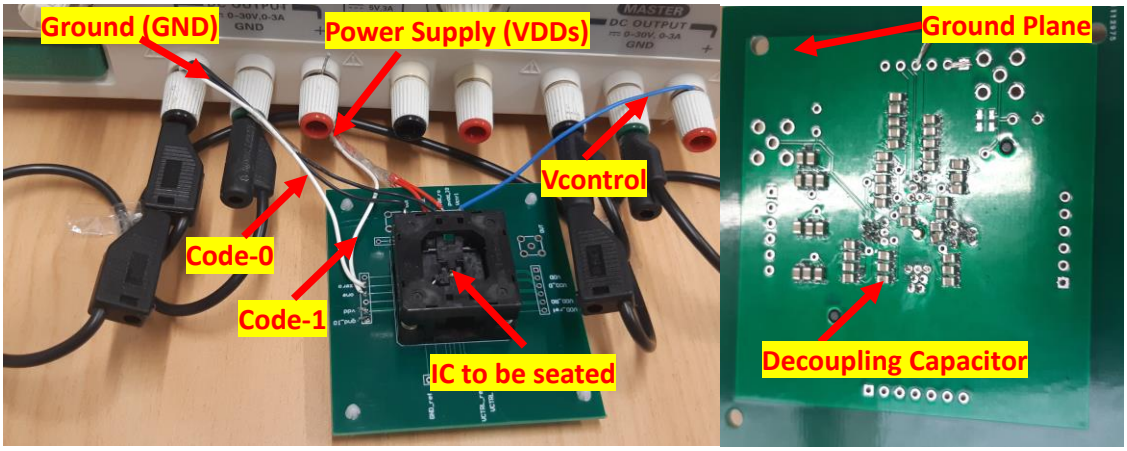



Fig. 4.44 Bottom metal layer layout of the PCB board

The PCB is designed to test both the circuits, the one with ESD and the one without ESD. For each circuit, one 50-ohm SMA connector was connected to the signal output to keep the option for testing the circuit with 50-ohm matched testing instruments. The test board layout was made DRC clean and sent for fabrication. On the received PCB board first, decoupling capacitors were soldered using the reflow solder technique. For this first solder paste was applied at the bottom side of the board and capacitors were placed and put into an oven at 240°C for 50 seconds. After cooling it down, the socket and wires were soldered. Fig. 4.45 (a) shows the top view and Fig. 4.45 (b) shows the bottom view of the board.




(a) (b)

Fig. 4.45. (a) the top view of the IC test board with mounted QFN socket and power supply lines. (b) the bottom view of the test socket with soldered SMD 0805 ceramic capacitor

## 4.5.2. Test Setup

To perform the test, Rohde & Schwarz oscilloscope, HMO3002 featuring 400MHz 4GSa/s [76] and Tektronix P2200 1X/10X Passive Probe [77] featuring 200MHz was used for the measurement, and ADV@NTEK P3035T DC power supply was used for providing the necessary supply voltages (VDD_RO, VDD, VDD_D, and VDD_ESD) and control voltage (V_CTRL) to the circuit. The test equipment setup and PCB test board with the prototype chip on it are shown in Fig. 4.46. The test was performed at room temperature set at 21°C.

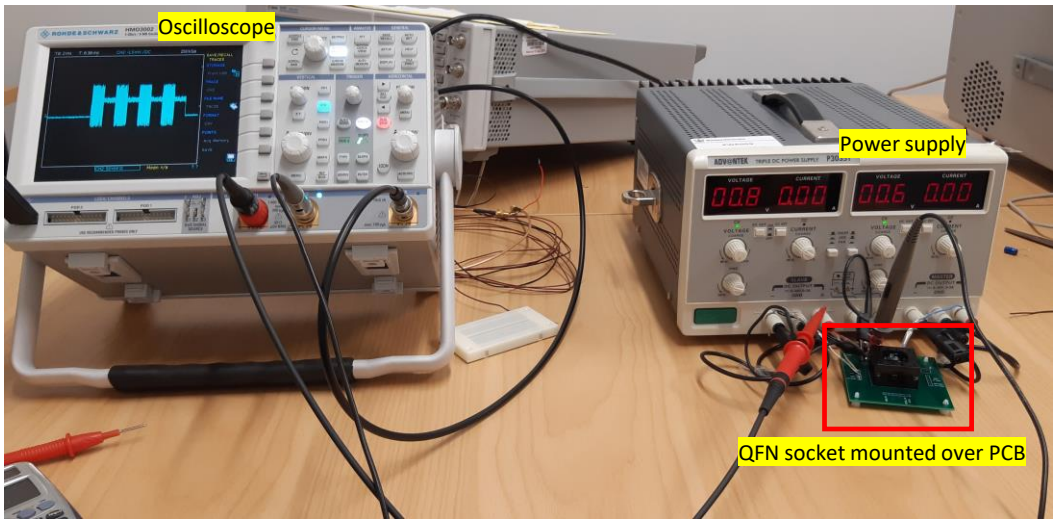



Fig. 4.46. Test setup for testing the fabricated telemeter ASIC chip. The 1mm X 1mm chip is QFN packaged for testing and is inside the QFN socket.

### 4.5.3. Measurement Result and Discussion

The fabricated chip was tested in the lab and out of the three circuits, only the circuit which had the ESD [78] protection cells worked well proving that TSMC 65nm circuit was highly sensitive to ESD and necessary precautions were taken while testing the chips. Another difficult challenge in testing the circuits was in triggering the extremely low duty cycle burst mode signal on the oscilloscope. The DC power supply regulator not being fast enough to maintain the fixed voltage at its output terminal caused significant fluctuation in the on-chip oscillator frequency. This led to some inconsistency in the burst appearing in the scope making it difficult to sample and capture the signal at the right moment. The chip testing was done at two different frequencies (158.86MHz and 4.4MHz) and are discussed below:

#### 4.5.3.1. Measurement @ VDD = 790 mV & V_CTRL=652mV

The working of the chip is demonstrated using the pictures captured in the oscilloscope. Fig. 4.47, Fig. 4.48, and Fig. 4.49 were taken with supply voltage (VDD, VDD_RO, VDD_ESD, and VDD_DRIVER) set at 790mV and control voltage (V_CTRL) at 652mV. This tag circuit is configured for the digital code 01010101. Since the 8-bit codes in the burst signal are Frequency Shift Keying (FSK) modulated, it has 2 frequencies, 158.86MHz for 1s and 78.95MHz for 0s as carrier frequencies. The coded signal burst appeared after every 1.7 sec with a burst window width of

13.28msec this is shown in Fig. 4.47 and Fig. 4.48, respectively. It is important to understand here that in Fig. 4.48, the burst window looks like amplitude modulated with alternates of large and small-signal amplitudes for 0s and 1s, respectively. But in reality, it is FSK modulated with Logic-1 represented by 158.86MHz and Logic-0 with 78.95MHz and the amplitude of the signals generated by the chip driver at both frequencies are the same inside the chip. But due to the limited bandwidth of the testing scope and probe used for the

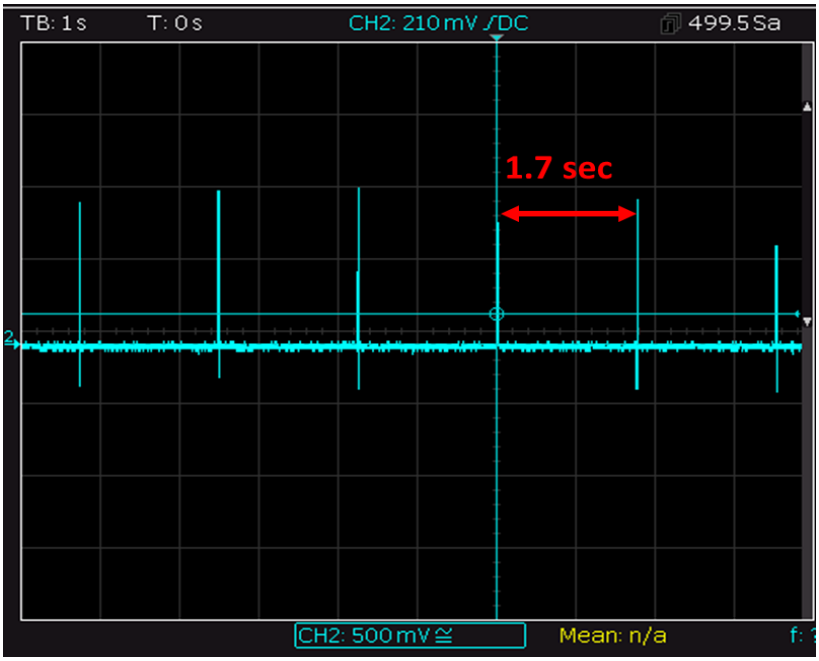



Fig. 4.47. Coded burst mode signaling appearing at every 1.7sec.

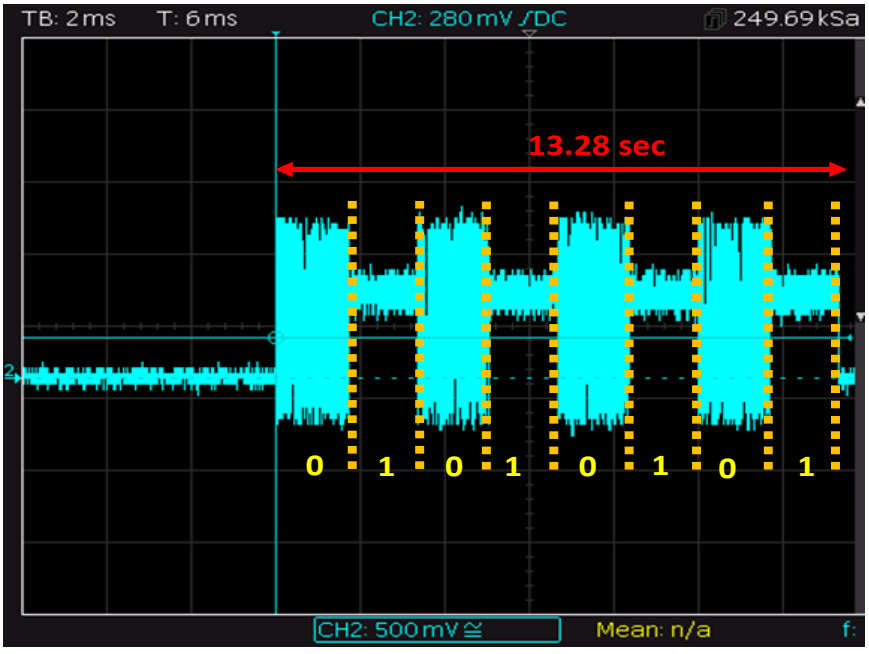



Fig. 4.48. FSK modulated 8-bit coded burst window width 13.28msec for Chip code-01010101

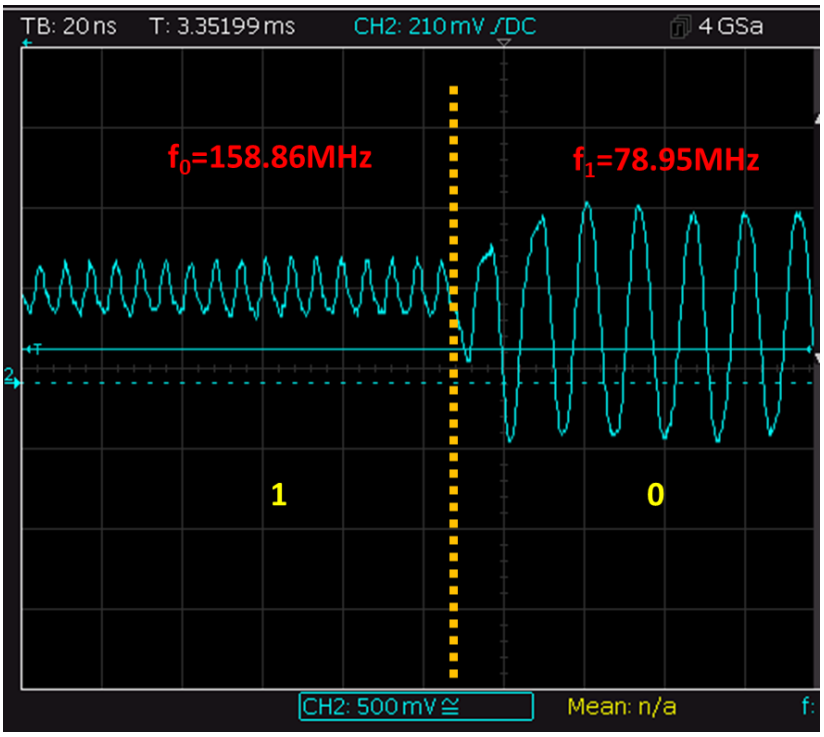



Fig. 4.49. FSK modulation scheme with 158.86 MHz representing Logic-1 and 78.95 MHz representing Logic-0

measurement attenuated the signal with higher frequency. That is why the signal amplitude at Logic-1 (being at a much higher frequency, 158.86MHz) appears very much smaller than signal amplitude at Logic-0 (at a lower frequency, 78.95MHz). Fig. 4.49 shows the zoom-in view of signal inside burst mode to show the FSK modulation.

### 4.5.3.2. Measurement @ VDD = 410 mV & V_CTRL=338mV

To verify the circuit functionality, the measurement data was also taken at a very low oscillator frequency, 4.54MHz which does not suffer from the problem of the limited bandwidth of the testing equipment. This was obtained at supply voltage (VDD, VDD_RO, VDD_ESD, and VDD_DRIVER) of 410mV and control voltage (V_CTRL) set at 338mV. In this case, Logic-1 and Logic-0 are represented by 4.48MHz and 2.24MHz respectively and the coded burst signal appears every 60sec with a window width of 466.24msec and this is shown in Fig. 4.50 and Fig. 4.51, respectively. Fig. 4.52 shows the zoomed-in view of the FSK modulated signal and shows the shift in the frequency from 2.24MHz at bit Logic-0 to 4.48MHz at bit Logic-1. Unlike the attenuated amplitude of burst signal in Fig. 4.49, in Fig. 4.52 the signal amplitude is

the same for both Logic-1 and Logic-0 in the code and only the frequency varies according to FSK modulation depending upon the Logics in the burst.

Fig. 4.53 shows the probability density distribution of the oscillator frequency ($f_0$) when the supply voltage, VDD is set at 410mV & Control Voltage, V_CTRL at 338mV. Its mean frequency is 4.54MHz and has a standard deviation of 149KHz which means the frequency stays within (4.54±0.596) MHz with a 95.45% confidence level.

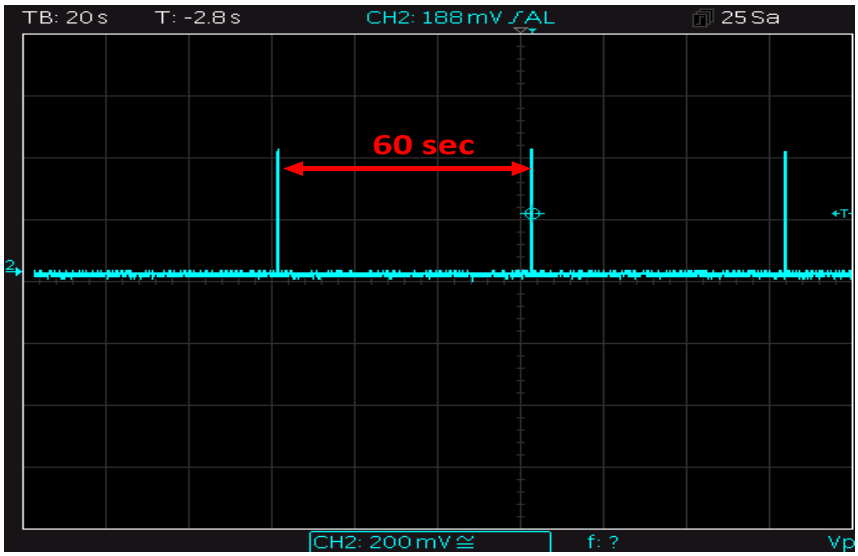



Fig. 4.50. FSK coded signal burst appearing at every 60sec. This measurement was taken with 1MΩ termination of the oscilloscope.

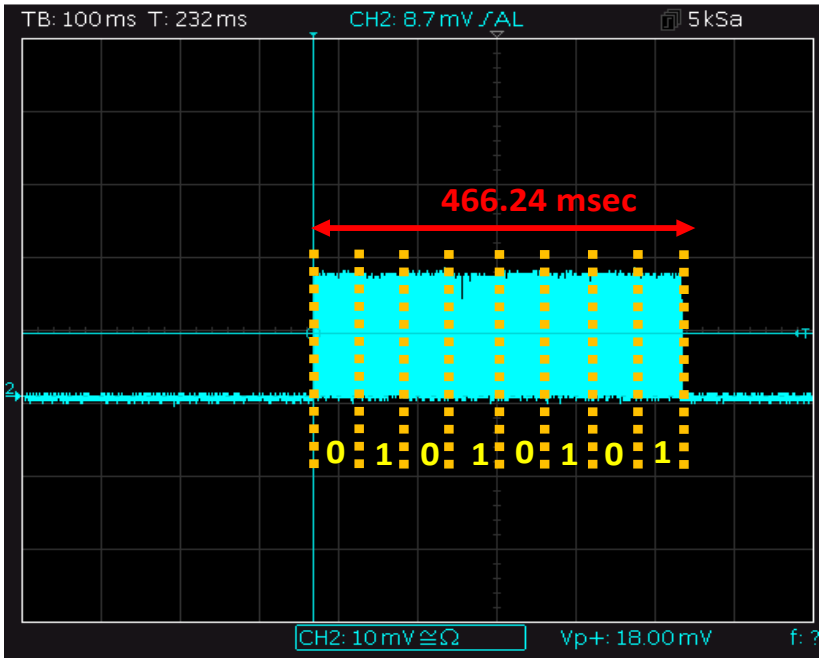



Fig. 4.51. 8 bit coded burst window width of 466.24msec, measured with 50Ω termination of the oscilloscope

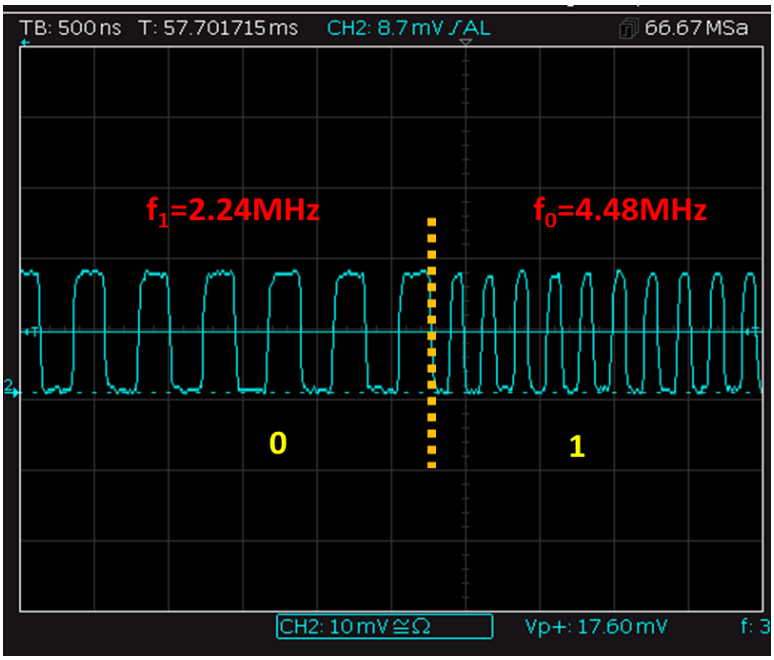



Fig. 4.52. FSK modulation with 2.24MHz signal representing Logic-0 and 4.48MHz signal representing Logic-1. The zoomed-in measurement was taken with 50Ω termination of the oscilloscope.

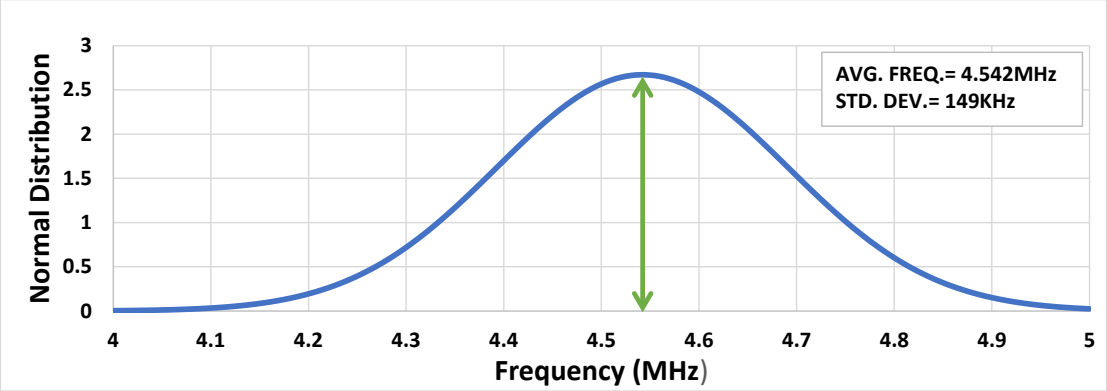



Fig. 4.53 Probability density distribution of the oscillator frequency with VDD at 410mV and V_CTRL at 338mV. The mean frequency was determined to be 4.45MHz with a 149KHz standard deviation

To verify the tuning of the oscillator and its dependence on the control voltage, V_CTRL at fixed VDD, frequency measurements were taken at various V_CTRL values and is plotted in Fig. 4.54. Also, it was found that connecting the V_CTRL to VDD rather than providing separate control voltage and varying the VDD value provides quite a good tuning of the oscillator frequency which later proved to be useful in designing the temperature compensation of the oscillator frequency at various process corners (slow-slow, typical-typical and fast-fast). Table 4.5 shows a

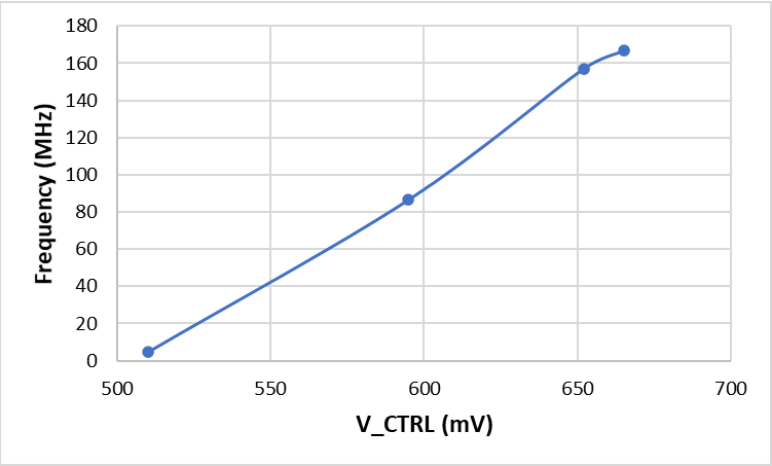



Fig. 4.54. Oscillator frequency versus Control Voltage (V_CTRL) with supply voltage (VDD) set at 790mV.

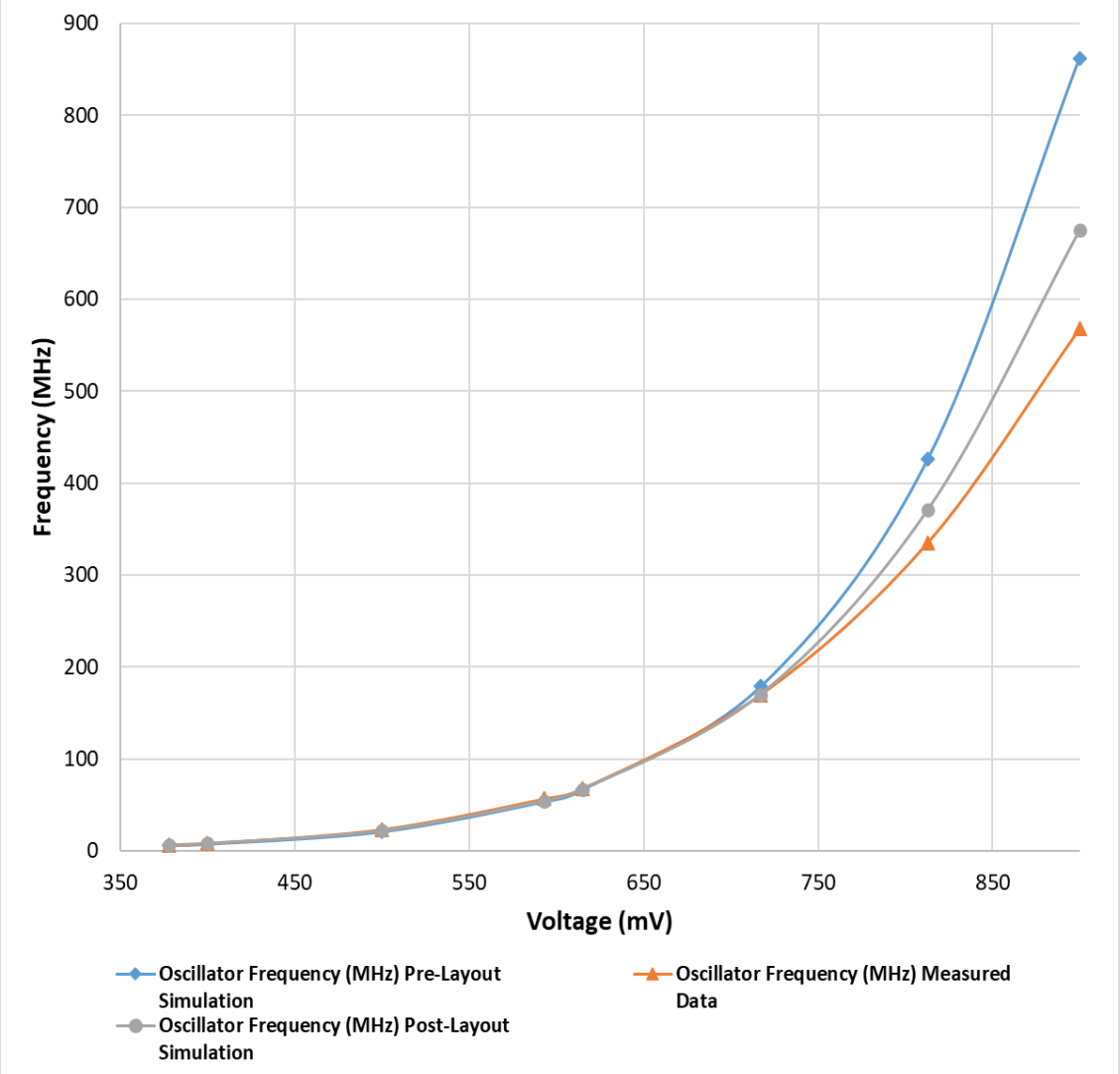



Fig. 4.55. Graph of Oscillator frequency versus supply voltage (VDD) with a control voltage (V_CTRL) connected to VDD

Table 4.5

Oscillator frequency versus Supply voltage (VDD) with a control voltage (V_CTRL) of the oscillator is connected to the supply voltage.

| Voltage (mV) | Oscillator Frequency (MHz) | | |
|---|---|---|---|
| | Pre-Layout Simulation | Measured Data | Post-Layout Simulation |
| 378 | 6 | 6.1 | 6.34 |
| 400 | 7.53 | 8.26 | 7.9 |
| 500 | 20.97 | 23.42 | 21.7 |
| 593 | 53.56 | 56.69 | 54.15 |
| 615 | 66.59 | 67.98 | 66.85 |
| 717 | 178.6 | 170 | 169.91 |
| 813 | 426 | 335.42 | 371 |
| 900 | 862 | 568 | 674.8 |

comparison of the frequency versus VDD for the simulated circuit without parasitic in 2nd column from left, measured data in 3rd column and the simulated data with parasitic of the layout included in the right most column. The same is plotted in Fig. 4.55. It could be seen here that the measured data matches with the simulated data at a lower frequency but deviates a lot at higher frequencies and the measured frequency is less than even the post-layout simulation data. This could be due to process variation effects and in parts due to the effect of the ESD devices and their parasitics elements which were not taken into consideration during the simulation and their effect becomes more prominent at a higher frequency. However, at the frequency range of interest (around 160MHz), the difference is not significant.

## 4.6. Conclusion

The chapter discussed a new architecture of the digital telemeter for insect tracking. It produces FSK modulated 8-bit coded burst signals at 0.0078 duty cycle. The design was first developed in IBM HPP 28nm technology but later due to high fabrication cost, it was redesigned in 65nm technology for fabrication and experimental verification of the circuit. The QFN packaged chip was tested in the lab and the measurement data proved the successful working of the design methodology in the manufacturing environment.

# CHAPTER 5

# FINAL INSECT TELEMETER PROTOTYPE

## 5.1. Introduction

The design presented in the previous chapter provides a solution to implement the telemeter design on ASIC to miniaturize telemeter size for tracking tiny insects and bees. The ASIC chip is conceptualized to be mounted on top of a 4mAh silver oxide battery whose output voltage drifts from 1.6 volts to 1.55 volts over time. The circuit operation requires a much lower and stable voltage (maximum 1 volt in 65nm process), to achieve the desired performance. Also, the telemeter design includes an on-chip VCRO which makes the oscillator frequency very sensitive to voltage level and supply noise. To solve this issue an on-chip power management unit (PMU) is designed to step down the voltage from 1.6 -1.55 volt to the desired and stable voltage.

Moreover, as seen in the previous chapter, the frequency of the chip varies significantly with temperature and this limits the number of tags employed in the field at a given time. This problem has also been addressed through power management design by delivering the supply voltage to the circuits in a fashion that counters the effect of ambient temperature change and keeps the oscillator frequency within a narrow range.

This chapter presents a final prototype of the insect telemeter circuit design which consists of the digital circuit discussed in previous chapters along with the power management unit to step down the battery voltage to the required level and to compensate for the effect of temperature as well as process variation on the device performance. The chapter also discusses the performance analysis, simulation data, and measured results of the tag fabricated in TSMC 65nm process technology.

## 5.2. Power Management Overview

The power management unit (PMU) is the backbone of every electronic device and is critical to the overall device performance. It occupies a major portion of the device and mostly consists of discrete components. The key solution to device miniaturization is that the power management unit should also be compact and

efficient with a fast-transient response. This becomes one of the most challenging parts of device miniaturization, especially while fully integrating the PMU on the same chip as that of ASIC and completely removing off-chip passive components. This is also called zero mass solution and in this, the required voltage is generated locally to achieve a smaller, thinner, and lighter device solution. Mainly two kinds of voltage regulators are used in implementing fully integrated power management circuits, namely switching regulators and linear regulators and are discussed as follows.

## 5.2.1. Switching Voltage Regulators

They are based on frequent switching of a series of elements on and off at certain duty-cycles. They use inductors or capacitors, or both depending on the design topology to temporarily store the energy which is released at the output at the required voltage level. The duty cycle of the switching frequency decides the amount of charge stored in the elements in a cycle. The efficiency is very high for these kinds of regulators because the elements are either fully conducting or completely off with minimum loss. They are basically, of three types (a) Switched inductor [79] (b) Switched capacitor [80] (c) hybrid converter [81] and are shown in Fig.5.1. Switched

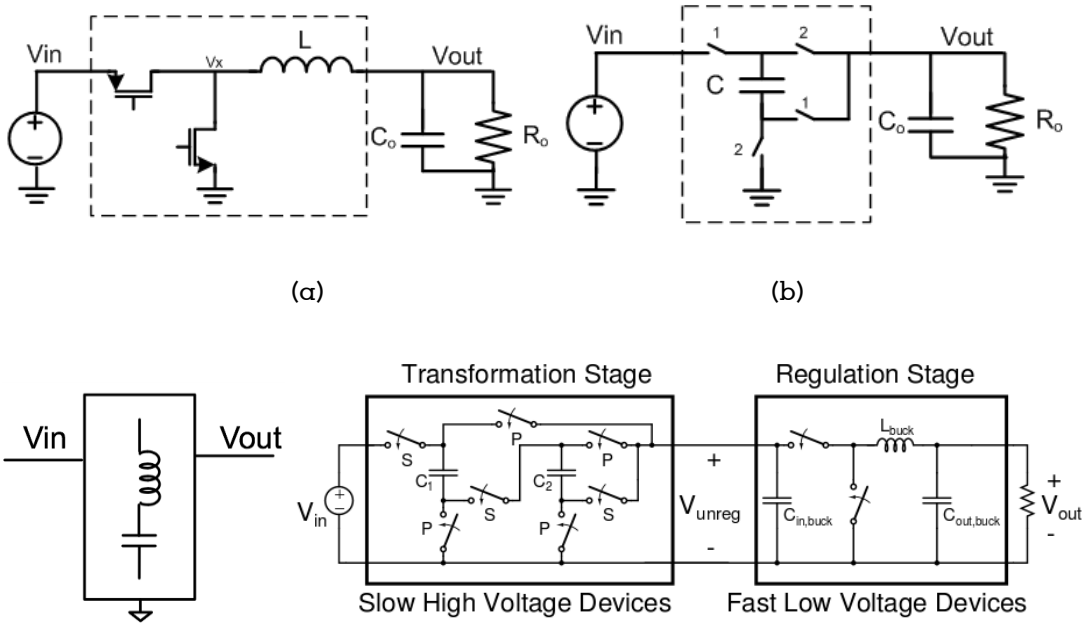



Fig.5.1. Switching regulators, (a) switched inductor (b) switched capacitor (c) Hybrid regulator

inductor as shown in Fig.5.1 (a) consists of 2 switches at the input, an inductor, and a capacitor. It transfers charge from input to output in form of current in the inductor and can provide efficient and fine voltage regulation. However, its transient speed gets limited by its switching frequency and is difficult to integrate on IC because of the inductor size. Lots of effort is being made by both industry and academia to integrate switched inductor regulators by integrating the inductor within the package and by integrating it in the silicon or the interposer layer. This can provide higher current density, but at a very high switching frequency and the efficiency cannot be optimized. These issues could be solved by a switched-capacitor dc-dc converter as shown in Fig.5.1 (b). In this, the charge is transferred from input to output in form of voltage. This could be readily integrated on-chip including the fly capacitor and can achieve fast response. But it has the drawback of efficiency degradation in fine regulation. The third kind of converter called hybrid converter combines the benefit of a switched inductor and switched capacitor to achieve peak efficiency at optimal conversion ratio and an example of this is shown in Fig. 5.1 (c).

### 5.2.2. Linear Voltage Regulators

Linear regulators are very much preferred for the application where the output voltage level is very close to the supply voltage. They use non-switching and linear methods to regulate the voltage and is shown in Fig. 5.2. In this, the switch on-resistance is adjusted in accordance with the load using an error amplifier to regulate the output voltage. This type of regulator is called a low dropout (LDO) regulator and provides a simple and noise-free solution. However, the biggest drawback is lower power efficiency which gets limited by output to input voltage ratio. The power loss ($P_{loss}$) in LDO is given by equation (5.1)

$$P_{loss} = (V_{in}\text{-}V_{out}) \cdot I_{load} + V_{in} \cdot I_{qn} \quad (5.1)$$

Here, $V_{in}$ and $V_{out}$ are the input and output voltage of the regulator respectively and $I_{load}$ and $I_{qn}$ are the load and quiescent current of the LDO. As it could be seen from equation (5.1) the loss increases significantly with the increase in the voltage difference between the output and the input, and also with the increase in the load current. In addition to this, there is always a constant loss of $V_{in} \cdot I_{qn}$ power due to the quiescent current in the internal circuitry of the LDO.

Despite the huge power loss in LDO compared to switching regulators, LDO has been preferred for the application in the telemeter design due to several reasons. Firstly, it would cost extra power as well as silicon area overhead to generate an on-chip switching signal which has to be the high frequency for full on-chip integration of the regulator. Moreover, switching regulators have switching noise which would need filter design to remove those noise and might require additional LDO to achieve fine regulation for the on-chip oscillator. All this additional circuitry put together; a switching regulator won't benefit much in terms of power but on the contrary, it would increase the telemeter size. Secondly, the insect telemeter circuit draws load current at an extremely small duty cycle (0.008) and the other time, during the sleep state the current requirement of the circuitry is comparatively very small which reduces the overall power. Thirdly, LDO provides flexibility to compensate for the effect of temperature variation on the device performance by adaptively changing the regulator output voltage level as per ambiance temperature to maintain the oscillator frequency within a reasonable range. Additionally, LDO provides several other advantages over the switching regulators like very simple to implement and achieves a fast-transient response, easy regulation, very low noise, area-efficient, and scalable with process technology. Therefore, it turned out to be an ideal choice for the fully integrated power management design for the insect telemeter circuit.

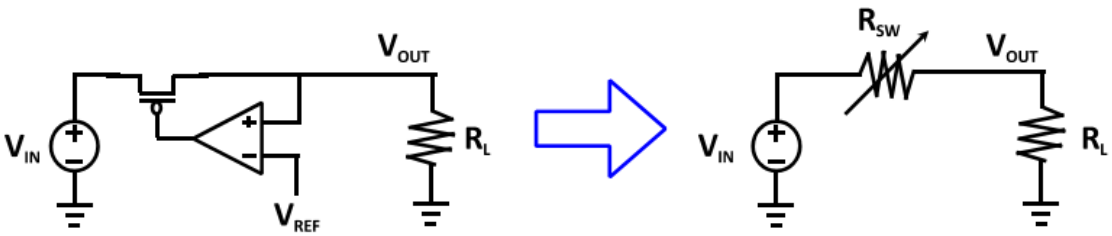



Fig.5.2. Linear regulator

## 5.2.3. Fundamentals on Voltage Reference

The Linear regulator requires a voltage reference, Vref (as shown in Fig. 5.3) which is copied to the other terminal of the error amplifier to maintain the desired voltage at the output. The stability of this reference voltage is very critical to the regulators' performance and its accuracy in the voltage conversion. Therefore, voltage reference must not exhibit much dependence on supply voltage or process variation and should show defined dependence on temperature variation.

There are many ways to realize an on-chip reference voltage like by using buried Zener diode, bipolar transistors, CMOS only transistors, or using both CMOS and bipolar transistors to generate mixed voltage reference. Buried Zener diode provides one of the accurate voltage references which is the least sensitive towards stress and long-term drift [82] but it requires a minimum 6.5V supply voltage for its operation and the process required to build this is quite more expensive than the standard CMOS process. Bandgap voltage reference provides a good alternative to this and could be implemented at a much lower supply voltage. This extracts the negative temperature coefficient of the base-emitter voltage (Vbe) of the bipolar transistor (this is also used as CTAT voltage reference) and generates a positive temperature coefficient by exploiting the difference between base-emitter voltages of the two bipolar transistors (also used as PTAT voltage reference) and combines them to obtain the temperature-independent bandgap voltage reference.

Due to serious push towards a single chip design integration, numerous CMOS-only voltage reference topologies have also been designed. These usually employ the threshold voltage of the transistor to produce supply independent voltage and use other parameters like polysilicon resistance, mobilities, etc. to define the temperature dependence of the reference voltage. However, due to their heterogeneous origin, there is no well-defined method to combat process variation. This seriously limits the device yield [83]. That is why mixed voltage reference provides the best solution for achieving high accuracy and yield while integrating the design with the standard CMOS process and has been implemented in the design to generate the reference voltage.

## 5.3. Complete Insect Telemeter Architecture

The digital core telemeter circuit, presented in the previous chapter needs three external supply voltages VDD, VDD_DRIVER, and V_CONTROL to operate the circuit and these voltage levels are required to be much less than the battery voltage (1.6-1.55 volt). Therefore, to complete the telemeter circuit, a power management circuit is designed to generate these required voltages locally from the battery supply. This section details the complete architecture of the telemeter circuit and presents the simulated results and performance analysis.

The functional block diagram of the telemeter circuit is shown in Fig. 5.3. It consists of the Power Management Unit (PMU) with temperature compensation, the digital

core circuit, and the output driver. The power management unit includes supply independent current reference circuit, Complementary to Absolute Temperature (CTAT) voltage reference, bandgap voltage reference, and two linear Low Dropout (LDO) voltage regulators, LDO1 and LDO2, to locally generate the required voltage levels for the digital core circuit and the output driver, respectively. LDO1 provides CTAT regulated voltage to compensate for the temperature variation in the on-chip oscillator and minimize the frequency drift. It uses CTAT voltage output from the voltage reference circuit as a reference voltage for the error amplifier. The regulated CTAT voltage from LDO1 driving the digital core circuit causes the amplitude of the intermediate signals in the circuitry to fluctuate with ambiance temperature. Therefore, to level the final amplitude of the burst signal transmitted from the telemeter, the second LDO i.e. LDO2 is designed to generate a fixed voltage supply (1-volt), independent of temperature or process variation to power the level shifter and the driver circuit. The error amplifier of the LDO2 uses bandgap voltage reference from the voltage reference circuit. The supply independent current reference circuit provides bias currents to operational transconductance amplifiers (OTA) used in voltage reference circuits. The voltage reference circuit also provides the biasing voltages required in the two LDO circuits.

### 5.3.1. Power Management Circuit Description

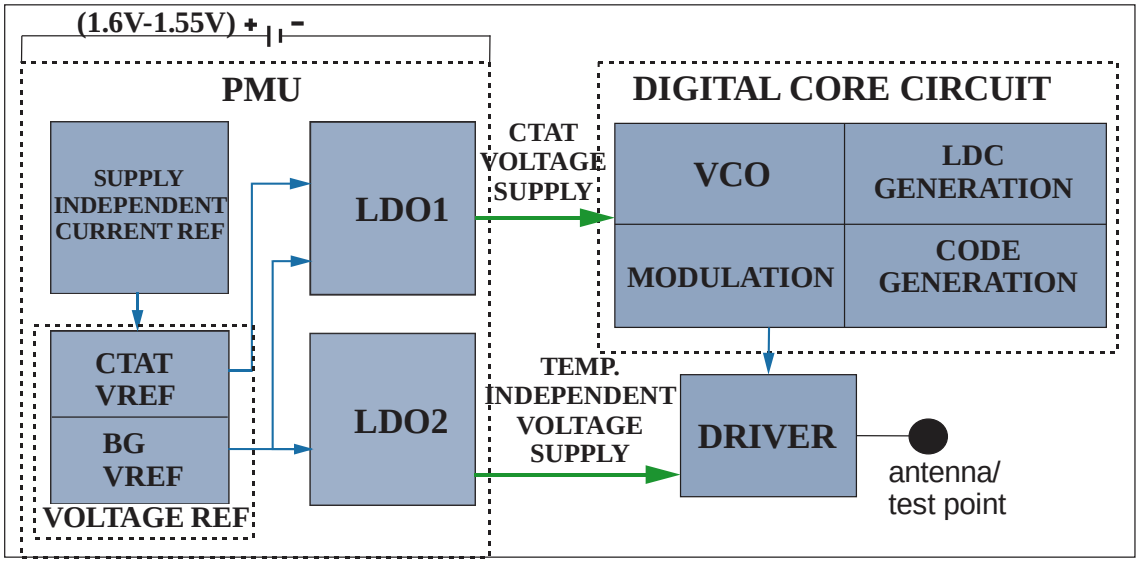



Fig.5.3. Block representation of the telemeter circuitry

### 5.3.1.1. Voltage Regulator (LDO1) Design

Oscillator frequency in the telemeter circuit fluctuates with temperature due to the variation of current in the oscillator and this could be balanced out by varying the supply voltage of the oscillator accordingly. The rate at which this frequency changes also varies with the process variation. Fig.5.4 shows the frequency variation plot with temperature for slow-slow (ss), typical-typical (tt), and fast-fast (ff) process corners. It could be seen here that frequency increases with the rise in temperature at the highest rate for ff corner and at the lowest rate for ss corner. This drift could be compensated by reducing the supply voltage of the oscillator as a linear function of temperature and is expressed through the equation (5.2). Here, V(T) is the voltage function of temperature, T, c are the intercepts, and s is the slope of the linear function.

$$V(T) = c - sT \tag{5.2}$$

However, it becomes very challenging for the current starved oscillator to obtain such a linear supply voltage function, V(T) which reduces at a fixed rate with temperature rise for all process corners so that the frequency drifts can be compensated just by shifting the voltage level (intercept, c) of the linear function. After numerous simulations, it was found that such a function could only be obtained for the designed VCRO by shoring the control voltage (V_CTRL) of the VCRO with the supply voltage of the oscillator (VDD_RO). Otherwise, if the control voltage of the

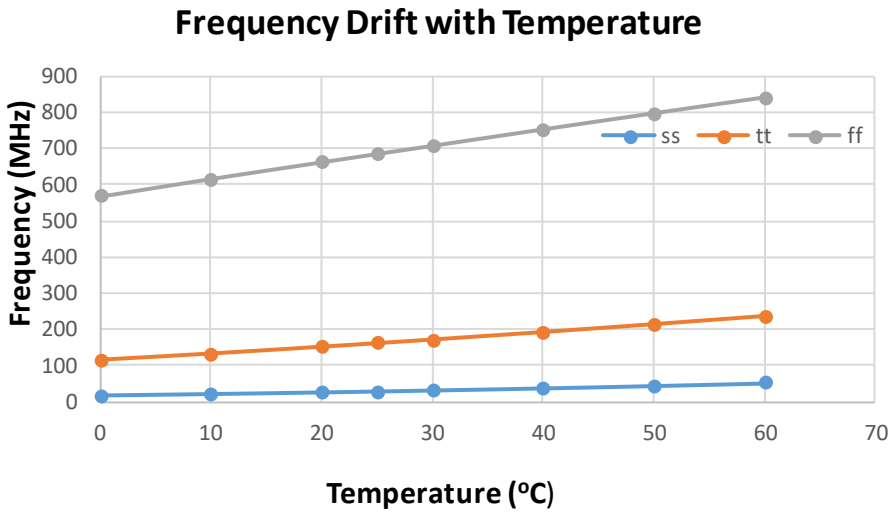



Fig.5.4. VCRO frequency drift with ambient temperature variation for slow-slow(ss), typical-typical(tt) and fast-fast(ff) process corners.

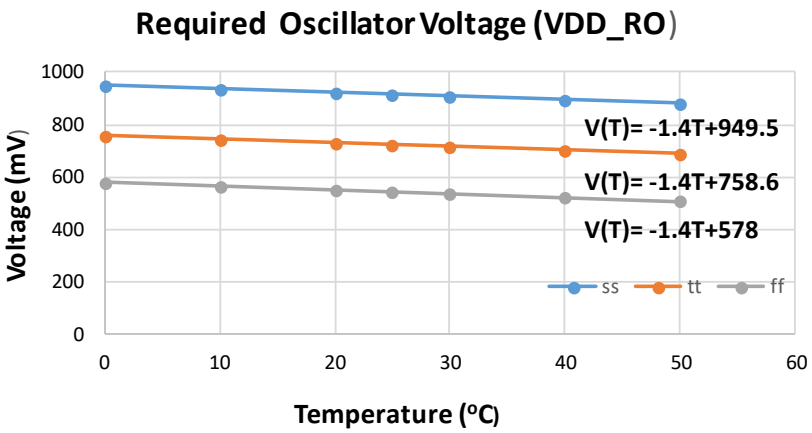



Fig.5.5. The regulated voltage that LDO1 is required to supply to the RO to compensate for the ambient temperature variation and minimize the oscillator frequency drift for slow-slow(ss), typical-typical(tt), and fast-fast(ff) process corners.

oscillator is assigned a voltage different from VDD_RO then for different process corners the slope of the function required for the temperature compensation also differs making it difficult to design a voltage regulator to provide such a voltage demand. Fig.5.5 shows the regulated voltage that LDO1 is required to supply to the oscillator to compensate for the ambient temperature variation and minimize the oscillator frequency drift for slow-slow(ss), typical-typical(tt), and fast-fast(ff) process corners. It also illustrates that these required linear supply voltages have the same slopes for the three process corners, i.e. 1.4mV/C and only the DC offset level is needed to be adjusted depending on the process variation.

The linear regulator, LDO1 is designed to provide the required voltage level to the digital telemeter circuit at various process corners. It is realized using 2.5V under-drive 1.8V nominal VT CMOS I/O transistors and would be operated at a voltage range from 1.6V to 1.55V (battery voltage). The regulator as shown in Fig.5.6, consists of a low power OTA as an error amplifier whose output controls the current through PMOS pass transistor $M_P$ while maintaining the output voltage same as reference voltage VREF1 which is the CTAT voltage reference, and the biasing voltage VB1 is provided by the bandgap voltage reference circuit discussed later in the section. The design operates to maintain the telemeter performance at a temperature range from $0^{\circ}C$ to $50^{\circ}C$ by adjusting the reference voltage of the amplifier through CTAT reference which could be trimmed for all the process corners providing a higher yield.

In general, the low power regulator can be implemented easily by designing the circuits in the subthreshold region but here low power design has been realized by keeping the gate length quite large to obtain better noise performance at low current at the cost of silicon area. The device sizes are shown in Fig.5.6. The quiescent current drawn by the LDO is only 295nA and can deliver load current from 3uA to 3mA while maintaining the output voltage regulation within 0.4% error.

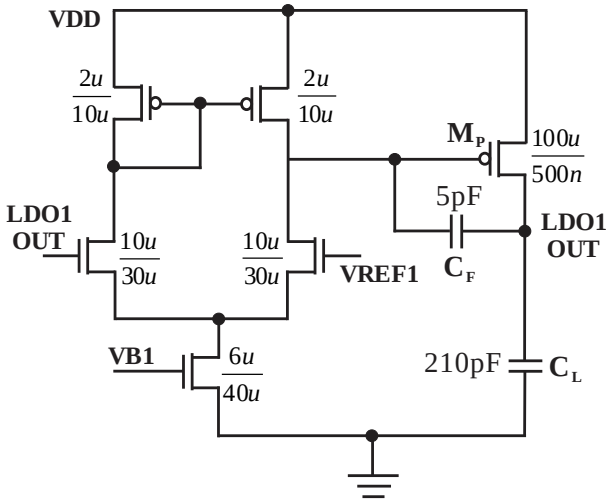



Fig.5.6. Linear voltage regulator, LDO1 schematic.

The open-loop stability analysis of the LDO is performed by connecting the circuit as shown in Fig.5.7 [84, 85]. The feedback loop for the ac signal is opened at the LDO1OUT node by connecting a 10GH inductor in between the positive terminal of the amplifier and the LDO1OUT node which continues to provide DC biasing voltage to the amplifier. An AC voltage is fed into the positive terminal of op-amp through a

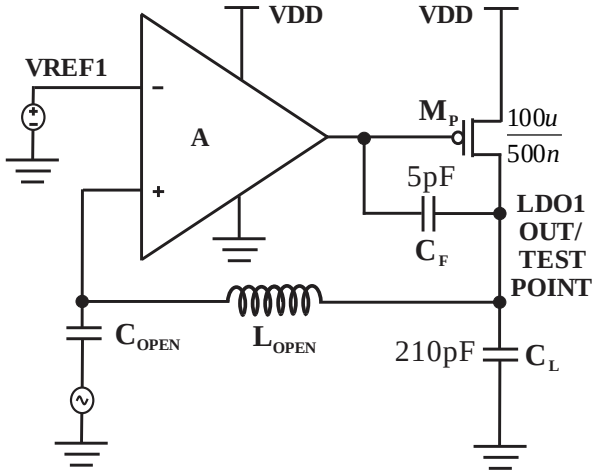
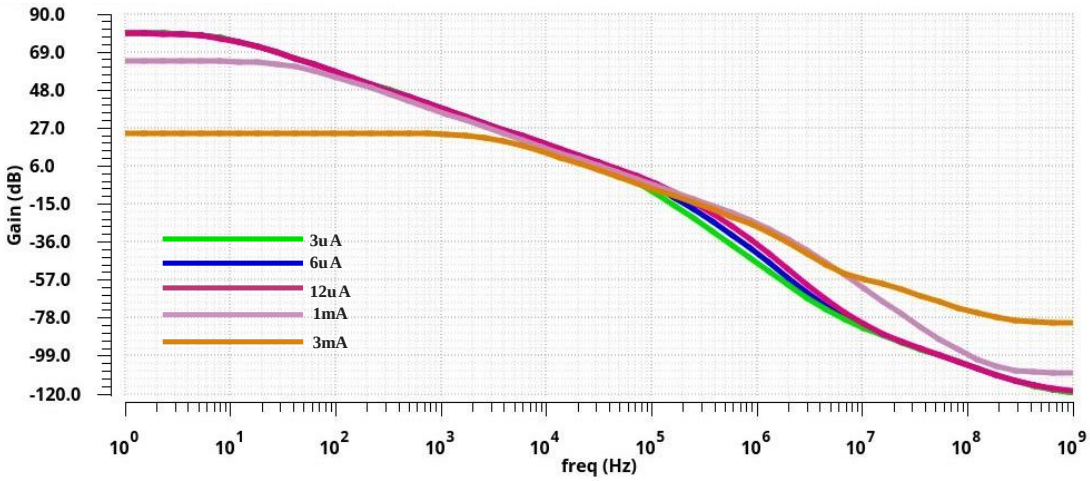
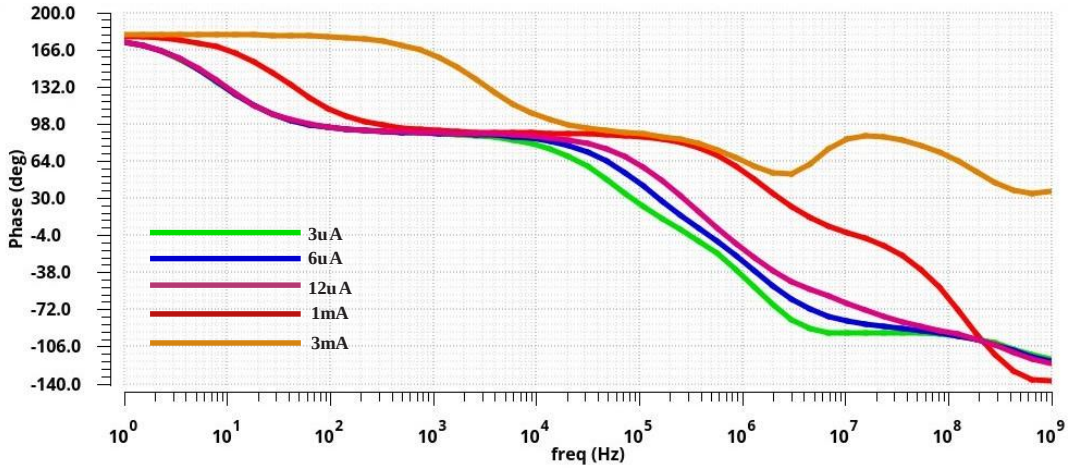



Fig.5.7. Schematic for the open-loop stability analysis of Linear voltage regulator, LDO1.




(a)




(b)

Fig.5.8. Simulated open-loop (a) gain and (b) phase plot of the linear voltage regulator for various load currents at 25°C and typical process, with VDD=1.55V and $C_L$=210pF.

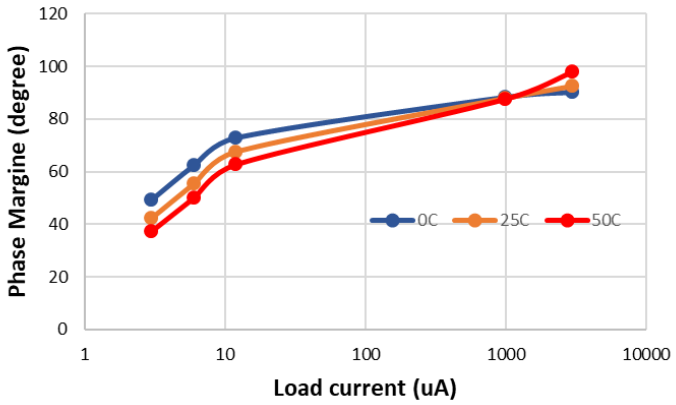



Fig.5.9. The simulated open-loop phase margin of the regulator at various temperature conditions.

10F capacitor, $C_{OPEN}$ as shown in Fig.5.7. The bode plot is illustrated in Fig.5.8 (a), and (b), which show the open-loop gain and the phase of the amplifiers for different

load currents with $C_L$ at 201pF at 25°C. A 5pF feedback capacitor, $C_F$ is connected across the gate and source of the power transistor, $M_P$ to improve the phase margin and the regulator stability. Fig. 5.9 shows the phase margin of the regulator at three temperatures, 0°C (showed in blue color), 25°C (showed in orange color), and 50°C (showed in red color).

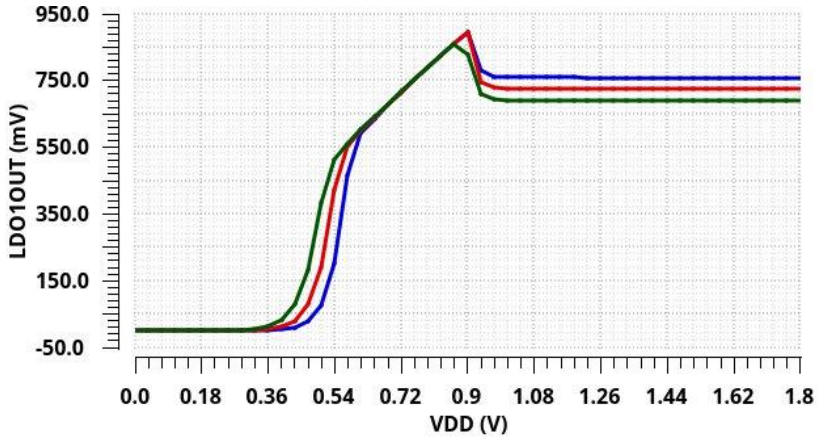



Fig.5.10. Simulated output regulation at 0°C (green), 25°C (red) and 50°C (blue) ambiance temperature with VREF1 @ 758.6mV, 723.49mV and 688mV, respectively

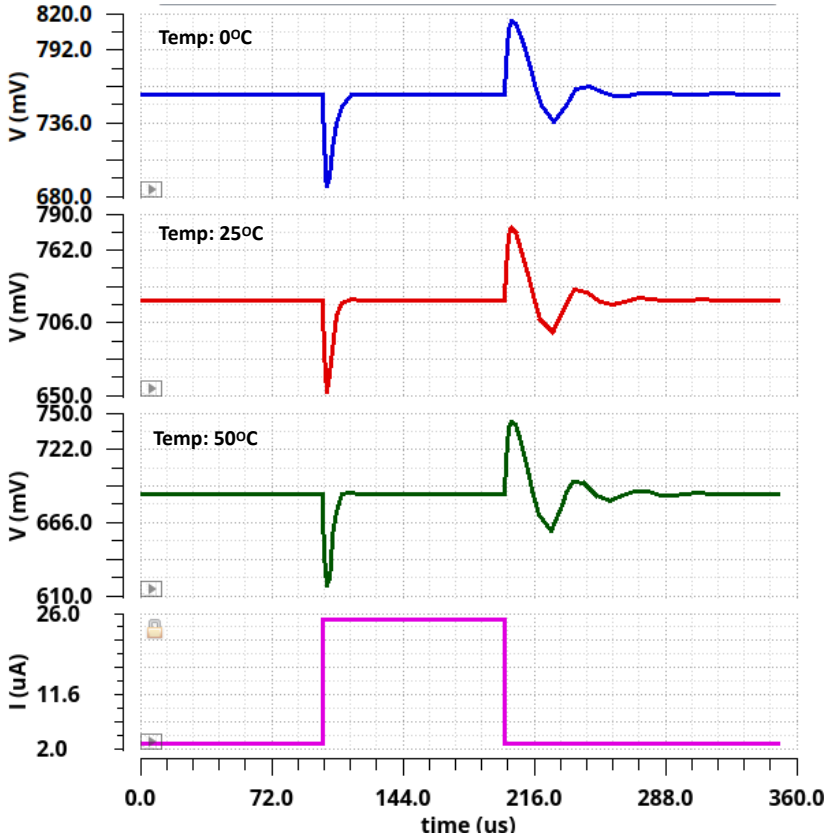



Fig.5.11. Post layout simulated load transient response at $I_{Load}$= 3uA to 20uA at 0°C, 25°C and 50°C with VREF1 set @ 758.6mV, 723.49mV and 688mV, respectively.

The output regulation plot [86] is the LDO1 at 0°C, 25°C, and 50°C are shown in Fig. 5.10. Due to the CTAT nature of the voltage reference, the regulator dropout voltage (the difference between the minimum input voltage the regulator can attain and the output regulated voltage) in the input rail range of 800mV, increases with temperature and is determined to be 213.4mV at 0°C, 248.5mV at 25°C and 284mV at 50°C.

Fig. 5.11 illustrates the load transient response at the 3 temperature conditions as marked in the picture. The topmost graph which is at 0°C is operating at an output regulated voltage of 758.6mV, the second graph from the top is at 25°C and has an

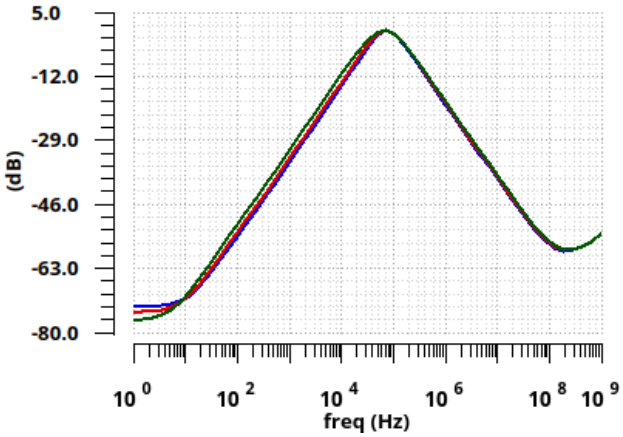



Fig.5.12. Post layout simulated LDO1 PSRR plot at 0°C (green), 25°C (red), and 50°C (blue) ambiance temperature.

TABLE 5.1.

LDO Electrical Characteristics @ VDD=1.55V, $C_L$=210pF unless otherwise noted.

| Parameter | Simulation Condition | Symbol | 0C | 25C | 50C | Unit |
|---|---|---|---|---|---|---|
| Reference Voltage | - | $V_{REF}$ | 758.6 | 723.5 | 688 | mV |
| Input Voltgae Range | - | VDD | 1-1.8 | 1-1.8 | 1-1.8 | V |
| Output Voltage | Temperature Dependent | $V_{LDO1OUT}$ | 758.6 | 723.5 | 688 | Mv |
| Load current maximum | $V_{LDO1OUT}$=99% $V_{LDO1OUT(NOM)}$ | $I_{LOAD(max)}$ | 3 | 3 | 3 | mA |
| Load current minimum | - | $I_{LOAD(min)}$ | 3 | 3 | 3 | uA |
| Quiescent Current | $I_{LOAD}$=0 | $I_Q$ | 250 | 360 | 460 | nA |
| Dropout Volatge | $I_{LOAD}$=25u | $V_{DO}$ | 213.4 | 248.5 | 284 | mV |
| Load Regulation | $I_{LOAD}$ = 12uA to 150uA | $Load_{Reg}$ | 2.8 | 2.91 | 3.27 | uV/uA |
| Line Regulation | VDD = 1V to 1.8V | $Line_{Reg}$ | 1.47 | 3 | 3.57 | mV/V |
| Settling Time | $I_{LOAD}$ = 3uA to 150uA | $t_{SETTLING}$ | 104 | 124 | 118 | us |
| Power Supply Rejection Ratio | f=1kHz, $I_{LOAD}$ = 15uA | PSRR | -31.3 | -33.5 | -34 | dB |
| Overshoot | $I_{LOAD}$ = 3uA to 150uA | $V_{OVERSHOOT}$ | 56 | 55.4 | 55.7 | mV |
| Undershoot | $I_{LOAD}$ = 3uA to 150uA | $V_{UNDERSHOOT}$ | 70 | 70 | 70 | mV |

output regulated voltage of 723.49mV and the third graph from the top has an output regulated voltage of 688mV at 50°C.

The power supply Rejection Ratio (PSRR) of the voltage regulator over a frequency range of 1GHz is shown in Fig. 5.12 and an overview of the electrical characteristic of the designed low power low dropout voltage regulator, LDO1 is summarized in Table 5.1.

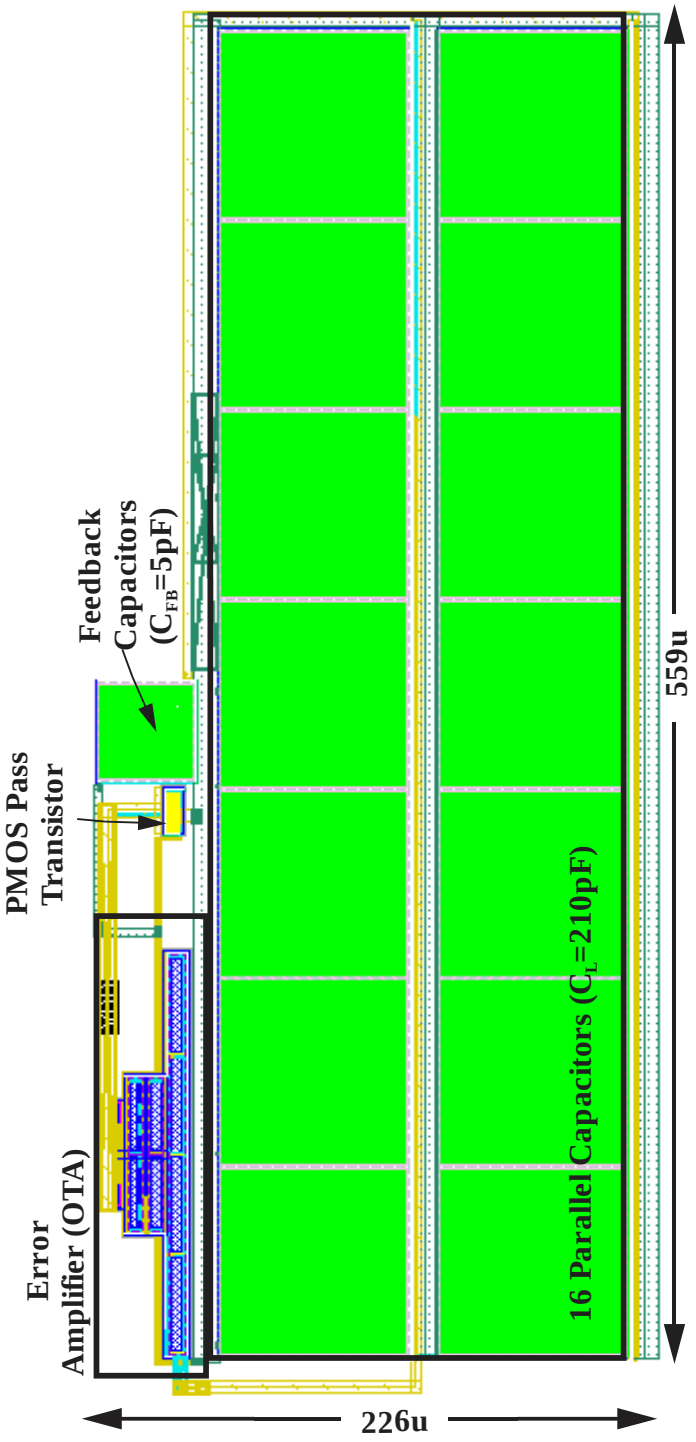



Fig.5.13. Linear voltage regulator, LDO1 layout

### 5.3.1.2. Voltage Reference Circuit Design

Fig. 5.14 shows the mixed voltage reference circuit employing both bipolar and CMOS transistors to obtain CTAT and bandgap voltage reference for the telemeter circuit. Bandgap voltage is obtained by first producing PTAT and CTAT voltages and then adding them to achieve the temperature-independent voltage reference. The design uses two PNP transistors, B1 and B2, available in the 65nm CMOS process, particularly for the bandgap reference design. Their base and collector terminals are shorted to the ground to achieve diode-like voltage behavior. In Fig. 5.14, CMOS transistors M4, M5, and M6 drive current through these bipolar transistors. The base-emitter voltage of B1 ($V_{be1}$) at the terminal 'a' is copied to the top terminals of R1 using an operational transconductance amplifier consisting of transistors M0, M1, M2, and M3. The emitter of B2 connects to the bottom terminal of R1 providing base-emitter voltage of B2, $V_{be2}$. $V_{be1}$ and $V_{be2}$ are given by the equations (5.3) and (5.4).

$$V_{be1} = V_t \ln(\frac{I_1}{I_{s1}}) \tag{5.3}$$

$$V_{be2} = V_t \ln(\frac{I_2}{I_{s2}}) \tag{5.4}$$

In the above equations, $V_t$ is the thermal voltage and is equals to $\frac{kT}{q}$, where $\frac{k}{q}$ is the Boltzmann's constant and T is the absolute temperature. $I_1$ and $I_2$ are the emitter currents in B1 and B2, respectively, and $I_{s1}$ and $I_{s2}$ are the saturation currents in the two transistors.

Thus, by assuming the off-set voltage of the OTA to be zero, the voltage across R1, $V_{R1}$ is the difference between the two base-emitter voltages and is given by equation (5.5) as shown below:

$$V_{R1} = \Delta V_{be} = V_t \ln(\frac{I_1 I_{s2}}{I_2 I_{s1}}) \tag{5.5}$$

The off-set voltage of the op-amp, however, post chip fabrication is never exactly zero, and therefore to minimize the error induced due to off-set voltage the $\Delta V_{be}$ is maximized [87] by sizing transistors M6, M4, and M5 in a way to produce $I_1 = 4 \cdot I_2$

and sizing B1, 10 times larger than B2 to produce $I_{s2}=10 \cdot I_{s1}$. Substituting these ratios in (5.5) and dividing it by R1 yields the current through the resistor, $I_{R1}$, which could be expressed as follows:

$$I_{R1} = I_{PTAT'} = \frac{kT}{qR_1} \ln(20) \tag{5.6}$$

As can be seen, in (5.6) $I_{R1}$ is proportional to absolute temperature but is pseudo-PTAT current due to the temperature dependency behavior of the resistor. This dependency cancels out later while realizing bandgap voltage reference by adding this current to pseudo-CTAT current and passing them through another resistor of the same kind showing the same temperature coefficient.

The base-emitter voltage of a bipolar transistor is inherently negative temperature coefficient, and this has been exploited to obtain pseudo-CTAT current to produce the bandgap voltage for biasing the circuits and reference voltage for the voltage regulator, LDO2, and to generate CTAT voltage reference, VREF2 for the voltage regulator, LDO1. The base-emitter voltage, $V_{be1}$ at 'a' is reflected across resistor R2 using OTA consisting of M10, M11, M12, M13, and M14. The output of the amplifier adjusts the gate voltage of M15 to yield pseudo-CTAT current in R2 and could be written as:

$$I_{R2} = I_{CTAT'} = V_{be1} = \frac{kT}{qR_2} \ln(20) \tag{5.7}$$

Bandgap voltage is obtained by adding $I_{CTAT}$ and $I_{PTAT}$ using M16 and M17 respectively and passaging the current through series of resistors R2, R3, R4, R5 and R6 to obtain VREF2, VB2, VB1, and VB2X respectively. These resistors, including R1 from the PTAT circuit, have been realized using 'P+ poly without salicides' resistor and common centroid layout configuration ABCDEFEDCBA [88] has been employed to minimize the stress-induced mismatch between these interdigitated arrays of resistors. This is shown in the layout picture of the reference circuit in Fig. 5.15. Here, A, B, C, D, and E refer to R1/2, R2/2, R3/2, R4/2 and R5 resistors respectively and these segments are connected in series in a way that cancels the thermoelectrics. The bandgap voltages generated are used as the reference voltage (VREF2) for LDO2 and as bias voltages for the amplifier transistors in LDO1 and LDO2.

CTAT voltage reference with specific slope and intercept voltage is required as VREF1 for the regulator, LDO1 to compensate for the temperature variation effect on

the on-chip oscillator. However, this (the slope and the intercept) is different from the CTAT reference designed for the bandgap voltage. Therefore, another CTAT reference is designed for LDO1 and is implemented using transistors M18 to M30 as shown in Fig. 5.14. This basically, first generates a pseudo bandgap current reference ($I_{BR'}$) using transistors M18 to M21, and the correct ratio of this current, $I_{BRM'}$ is added (using transistors M23 to M29 depending on the process corner) with the pseudo-CTAT current ($I_{CTAT2'}$) ( which is mirrored from $I_{CTAT'}$ using transistor M30) to achieve the desired CTAT reference voltage which would be the voltage reference of LDO1, (VREF1) could be expressed by the equation below:

$$V_{CTAT} = VREF1 = (I_{CTAT2'} + I_{BRM'}) \bullet R7 \tag{5.8}$$

The CTAT voltage reference ($V_{CTAT}$) gradient to the temperature required for the digital telemeter temperature compensation is decided by $I_{CTAT'}$·R7 and stays the same for all the process corners (slow-slow, typical-typical, and fast-fast). It is the intercept voltage level of $V_{CTAT}$ set by $I_{BRM'}$·R7 is needed to be adjusted depending on the process variation to achieve a higher yield. This is achieved by setting the required $I_{BRM'}$ current (since R7 value is fixed as per $V_{CTAT}$ gradient to temperature) using transistors from M23 to M29 as shown in Fig. 5.14. These transistors are connected to VDD through fuses (F1 to F7, respectively) and the $I_{BRM'}$ current could be set by blowing off the required fusses depending on the process corners. The current mirror transistors M23 to M29 could be adjusted to mirror 1 to 35 times the $I_{BR'}$ current to obtain needed $I_{BRM'}$. Table 5.2 shows the fuse that needs to be blown off to set the correct pseudo bandgap reference current ($I_{BRM'}$) for the simulated fast-fast, typical-typical, and slow-slow process corners. These fuses could also be adjusted to achieve different current ratios of $I_{BRM'}$ for other corners which were not simulated. Table 5.3 lists the device sizes of all the transistors used in the voltage reference circuit design.

Table 5.2.

The fuses required to be blown off for various process corners to achieve desired $I_{BRM'}$

| Process Corner | The required $I_{BRM}$ current | Fuses to be blown off |
|---|---|---|
| fast-fast | $I_{BRM'}$=2 X $I_{BR'}$ | F1, F3, F4, F5, F6, F7 |
| typical- typical | $I_{BRM'}$=12 X $I_{BR'}$ | F1, F3, F4, F5, F6 |
| slow-slow | $I_{BRM'}$=29 X $I_{BR'}$ | F2, F3, F4, F5, F6, F7 |

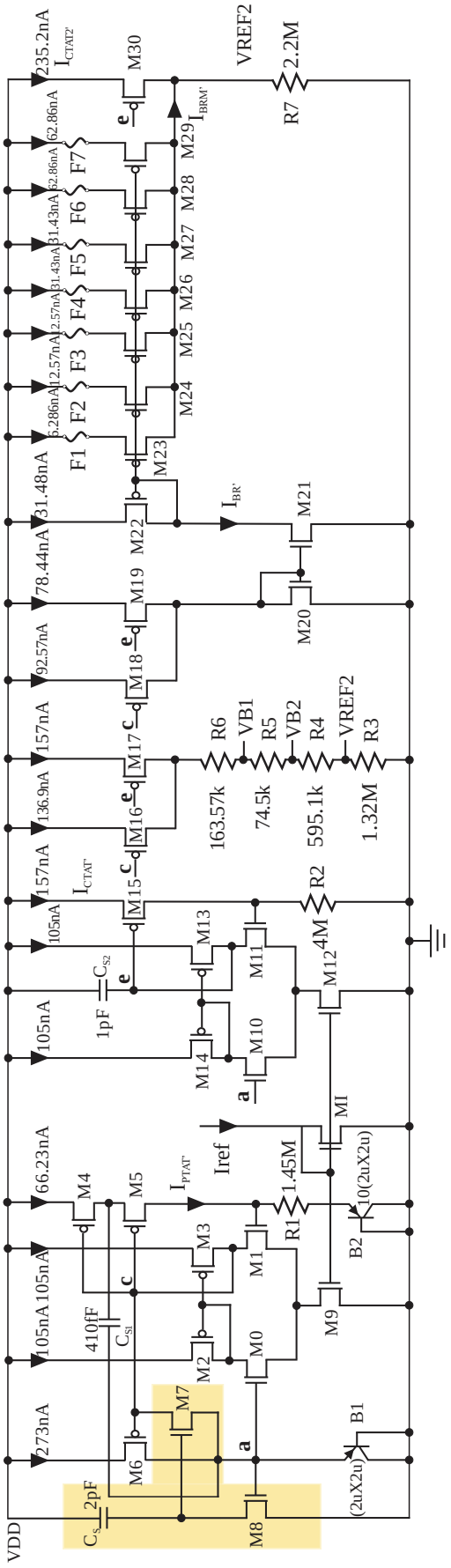



Fig. 5.14 Circuit for generating supply and temperature independent voltage reference plus the CTAT voltage reference.

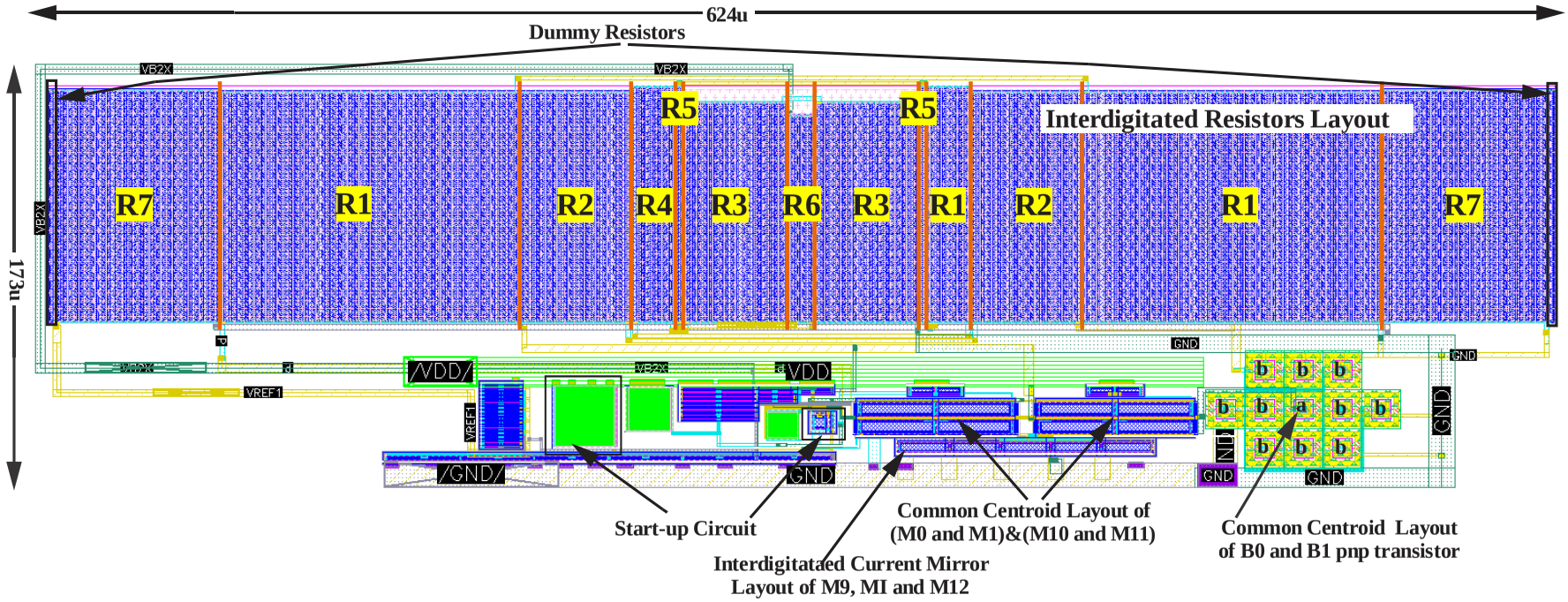



Fig. 5.15 Layout of Bandgap and CTAT reference voltage generation circuit

The yellow shaded circuit region in Fig. 5.14 is the startup circuit [89] consisting of M7, M8, and Cs employed to drive the self-biased opamp out of the degenerate point. The fabricated chip sent by the foundry was supposed to be a typical-typical corner and the IP for the electric fuse being very expensive the chip has been realized only for a typical-typical process corner and without using any fuse. Fig. 5.15 shows the layout of the implemented voltage reference design in 65nm technology. In this, proper design care has been taken to minimize the mismatches between the resistors. All the resistors (R1 to R7) are designed with the same segment width and since the random mismatch error decreases inversely with the square root of the resistor area, it was kept significantly large and also wide (4 times the minimum required width). Dummy resistors with the same width as resistor segments are placed on either side of the resistor arrays to provide the same etching environment to all the resistor segments and are marked with black rectangles in the layout picture. Layout design considerations were also taken to minimize the mismatches among various transistors of the op-amps and between BJT using a common centroid layout technique as marked in Fig. 5.15.

Fig. 5.16 plots the post layout simulated frequency sensitivity of the on-chip oscillator towards supply voltage variation for $0^{O}C$, $25^{O}C$, and $50^{O}C$ temperature. The graph shows a frequency sensitivity of 1.47-2 MHz/mV to the supply voltage, VDD.

Table 5.3

The aspect ratio of devices used in the CTAT and Bandgap voltage reference circuit

| Devices | Size | Devices | Size |
|---|---|---|---|
| M0 | 10u/30u | MI | 3.5u/20u |
| M1 | 10u/30u | M16 | 2u/30u |
| M2 | 2u/10u | M17 | 1u/30u |
| M3 | 2u/10u | M18 | 1u/30u |
| M4 | 1u/15u | M19 | 0.5u/30u |
| M5 | 1u/15u | M20 | 5u/30u |
| M6 | 2u/15u | M21 | 1u/30u |
| M7 | 5u/260n | M22 | 5u/15u |
| M8 | 5u/5u | M23 | 1u/15u |
| M9 | 7u/20u | M24 | 2u/15u |
| M10 | 10u/30u | M25 | 2u/15u |
| M11 | 10u/30u | M26 | 5u/15u |
| M12 | 7u/20u | M27 | 5u/15u |
| M13 | 2u/10u | M28 | 10u/15u |
| M14 | 2u/10u | M29 | 10u/15u |
| M15 | 1u/30u | M30 | 1.5u/30u |

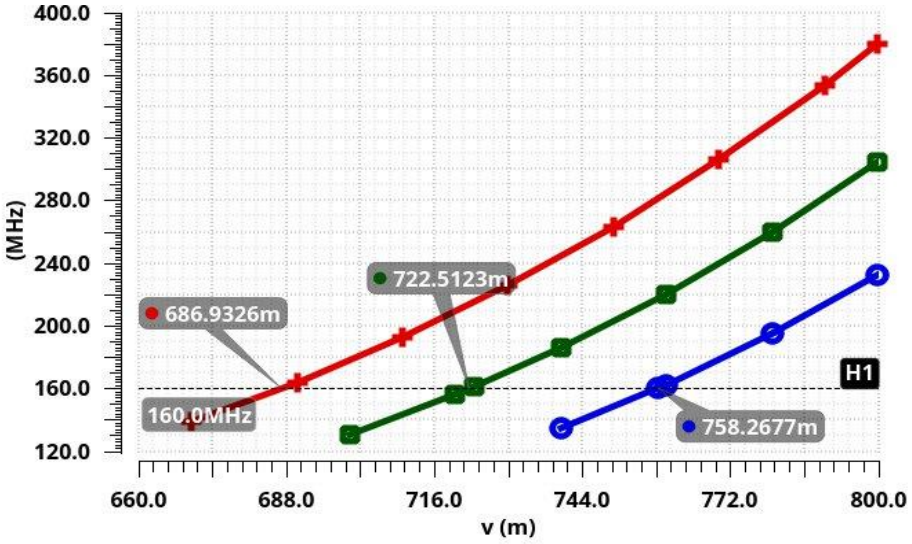



Fig.5.16. The sensitivity of the oscillator frequency to supply voltage variation (VDD) at 0°C (blue), 25°C (green), and 50°C (red) temperature.

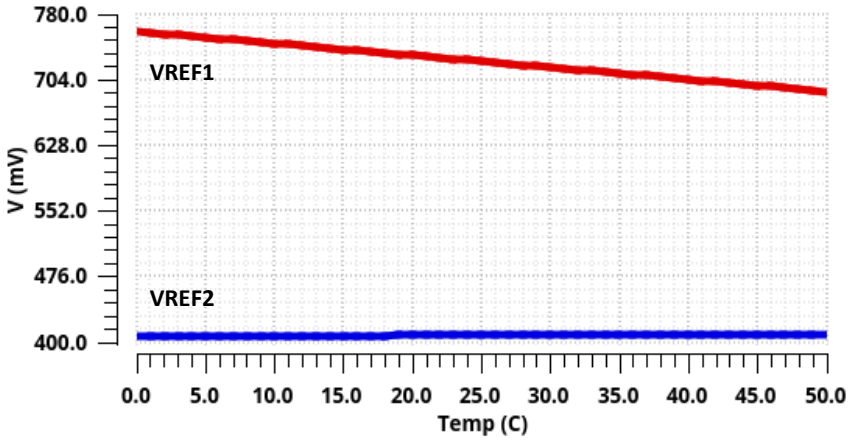



Fig.5.17. CTAT and Bandgap reference voltage generation for the digital telemeter circuit.

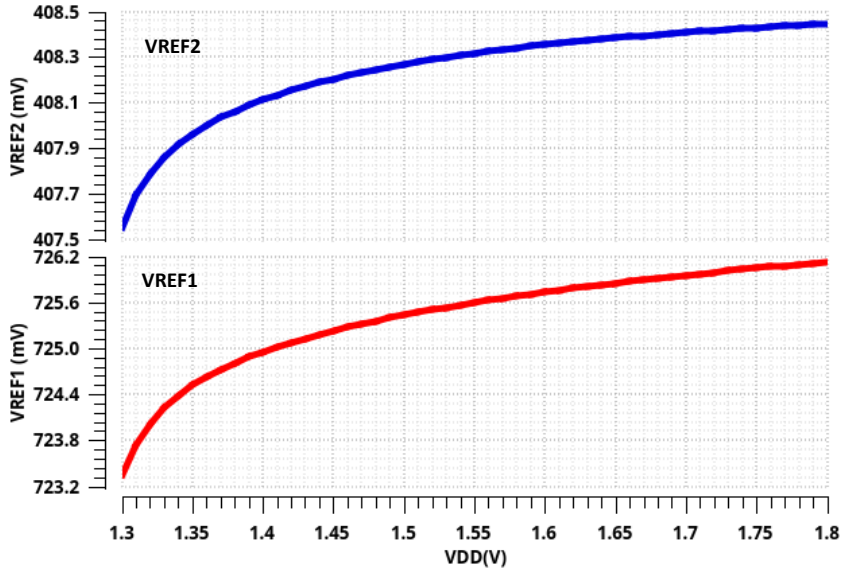



Fig.5.18. Effect of supply voltage variation on the CTAT and Bandgap voltage reference.

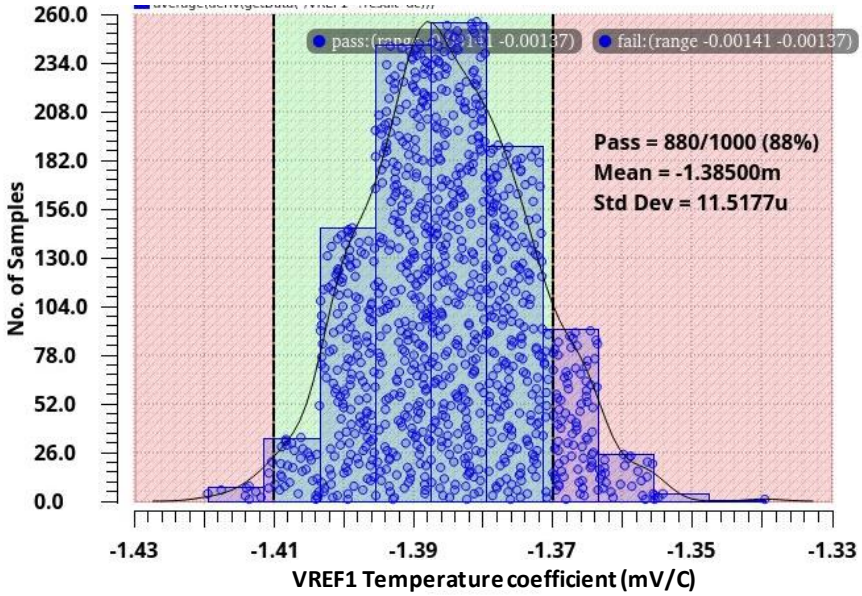



Fig.5.19. Monte Carlo Simulation of the temperature coefficient of the CTAT voltage reference VREF1 for 1000 samples.

The red-colored line in Fig. 5.17 shows the simulated CTAT voltage reference (VREF1) for the voltage regulator, LDO1 versus temperature variation, and bandgap voltage reference (VREF2) for the voltage regulator, LDO2 is shown with the blue-colored graph. The CTAT curve, VREF1 designed has its intercept voltage of 760mV at $0^{O}$C with a temperature coefficient of -1.385mV/$^{O}$C. The bandgap reference (VREF2) design has a very small dependency on temperature which is 37uV/$^{O}$C and this would not have any impact on the telemeter performance. The effect of supply voltage (VDD) variation on these reference voltages was also simulated across 1.3V to 1.8V supply voltages and is shown in Fig. 5.18. The overall sensitivity of VREF1 and VREF2 to VDD in the simulated range is 26mV/V and 18mV/V respectively. This is quite good due to the logarithmic behavior of the BJTs employed in the design.

The yield for the design has been predicted through Monte Carlo simulation based on the temperature coefficient of the CTAT voltage reference, VREF1. This is a very critical parameter to decide the allowable range of frequency variation within the operating temperature range. Fig. 5.19 shows the Monte Carlo result of 1000 samples for the temperature coefficient of VREF1 which estimates a yield of 88% by accepting the temperature coefficient from -1.41 to 1.37 mV/C. This temperature coefficient range will have a maximum frequency variation of ±1.1MHz across the temperature range of $0^{O}$C to $50^{O}$C.

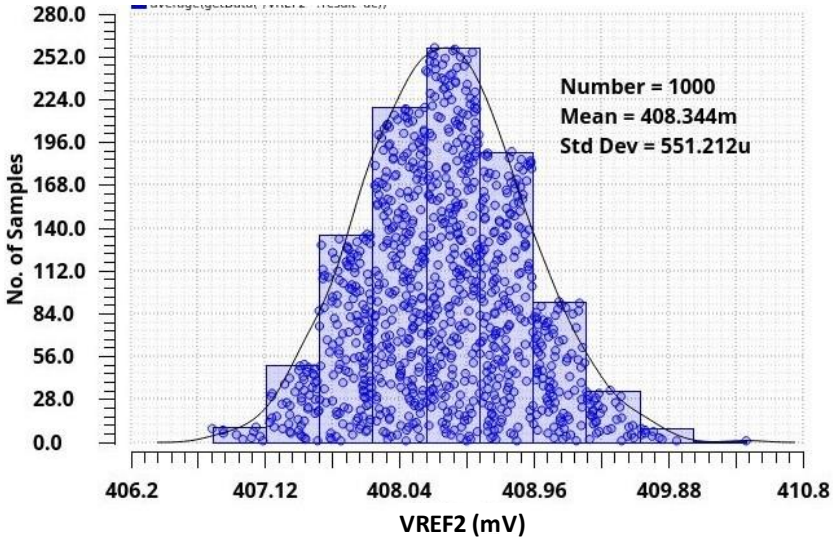



Fig.5.20. Monte Carlo Simulation of the Bandgap voltage reference, VREF2 for 1000 samples.

Fig. 5.20 shows the simulated Monte Carlo results of 1000 samples for bandgap voltage reference, VREF2 against process variation. The mean for the plot is 408.344mV with only 551.212uV standard deviation, which means that 99.73% of the fabricated chips will have a fixed output amplitude of 1.016V to 1.025V.

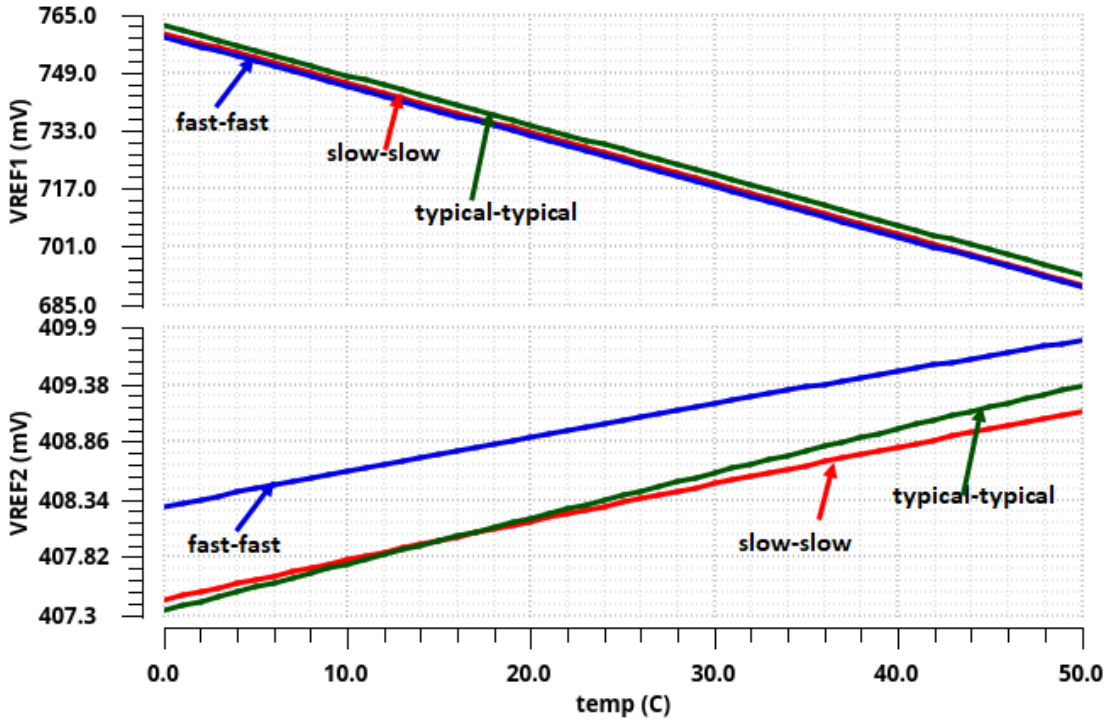



Fig.5.21. CTAT voltage reference (VREF1) and Bandgap voltage reference (VREF2) versus temperature for slow-slow (red), typical-typical (green), and fast-fast (blue) process corners.

The effect of process variation on the reference voltages is plotted in Fig. 5.21. The top picture in this figure illustrates the VREF1 against temperature variation for fast-fast, typical-typical, and slow-slow process corners which are shown by blue, green, and red graphs respectively. The bottom graph shows the same for reference voltage VREF2 for fast-fast, typical-typical, and slow-slow process corners also shown by blue, green, and red graphs respectively. The variation of reference voltages, VREF1 is not significant with the process variation which implies that to make the skewed IC chips work at the same oscillator frequency as that of non-skewed one (typical-typical process), the technique described above to adjust VREF1 through equation (5.8) and Table 5.2 is required to be implemented. Fig. 5.22 shows adjusted VREF1(through simulation without using any fuse) for slow-slow (red-colored graph), typical-typical (green-colored graph), and fast-fast (blue-colored graph) process corners.

Fig. 5.23 illustrates the startup transient behavior of the voltage reference circuit of nodes a, b and d as marked in Fig. 5.14. In the simulation the supply voltage ramps up from 0 to 1.55V in 100us time. To increase the stability and reduce the settling time of the voltages at these nodes, capacitors, $C_{s1}$and $C_{s2,}$ and split transistor [90] topology have been employed using M4and M5 transistors as shown in Fig. 5.14.

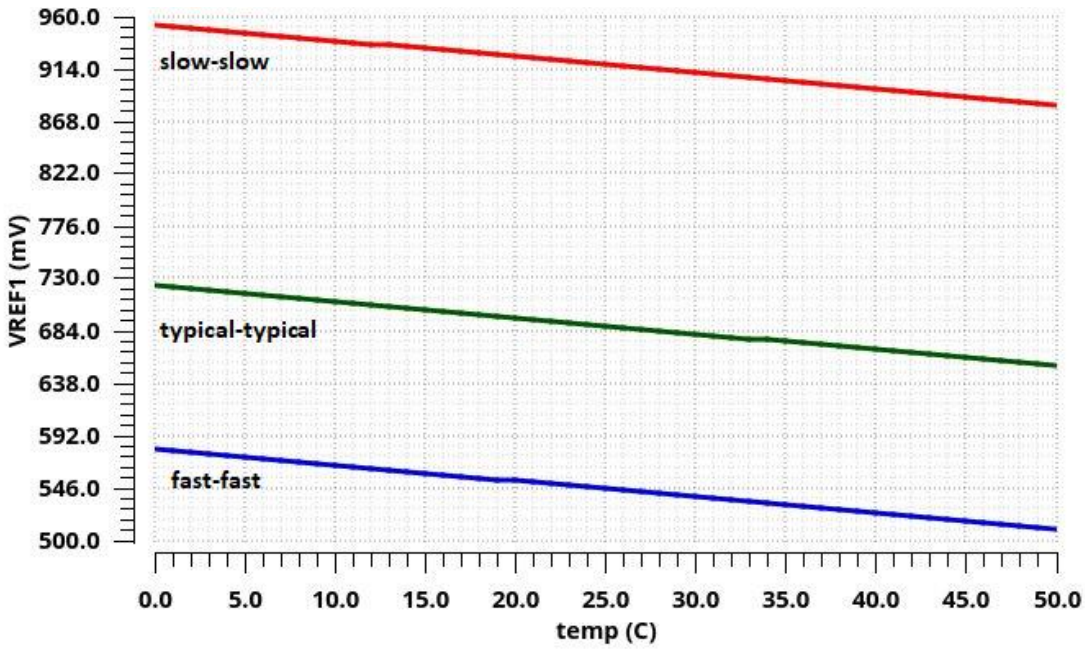



Fig.5.22. CTAT voltage reference (VREF1)) versus temperature for slow-slow, typical-typical and fast-fast process corners after level shifting.

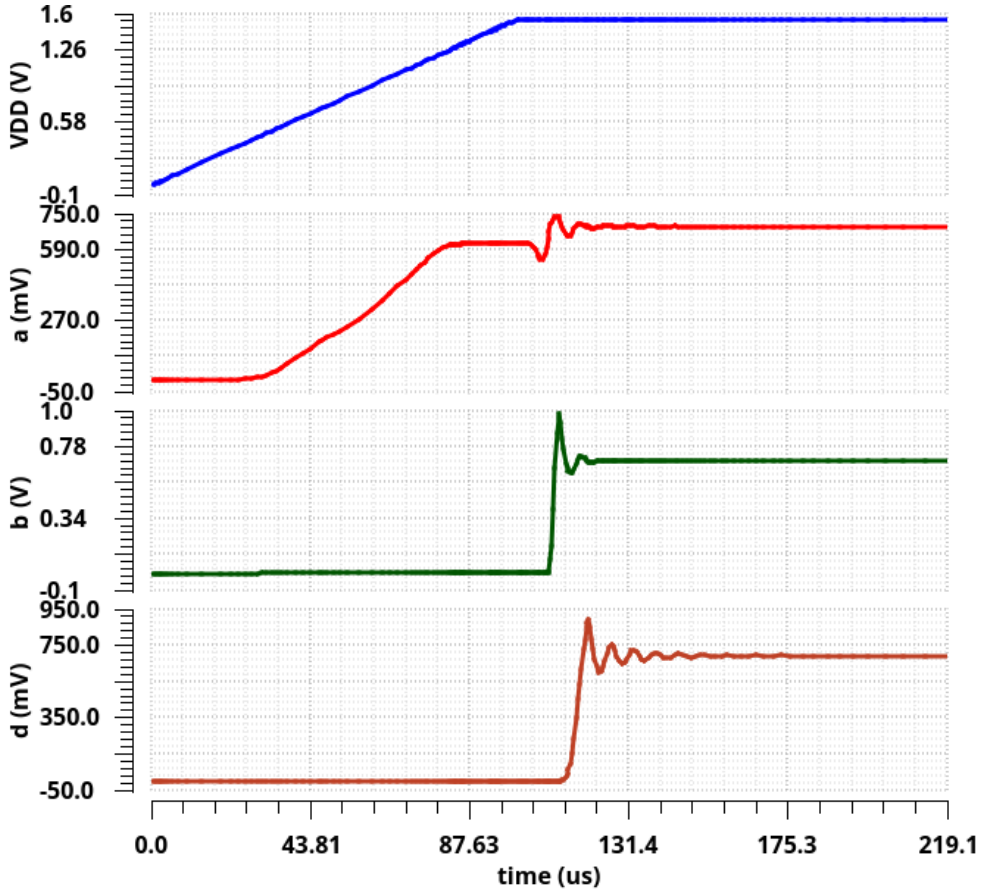



Fig. 5.23. The simulated waveform of voltage at nodes a, b, and in d (nodes marked in Fig. 5.14) during startup when the supply voltage (VDD) steps up from 0 to 1.55V at time t=100us.

### 5.3.1.3. Supply Independent Current Reference

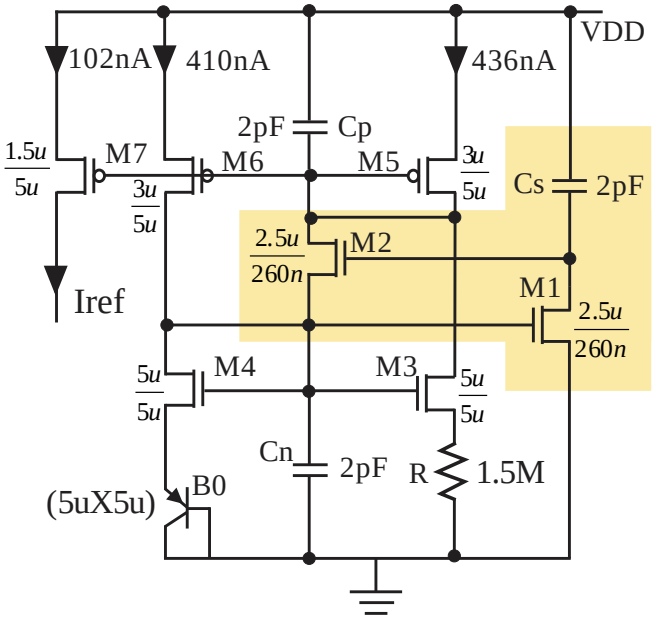



Fig.5.24. Schematic of supply independent current reference

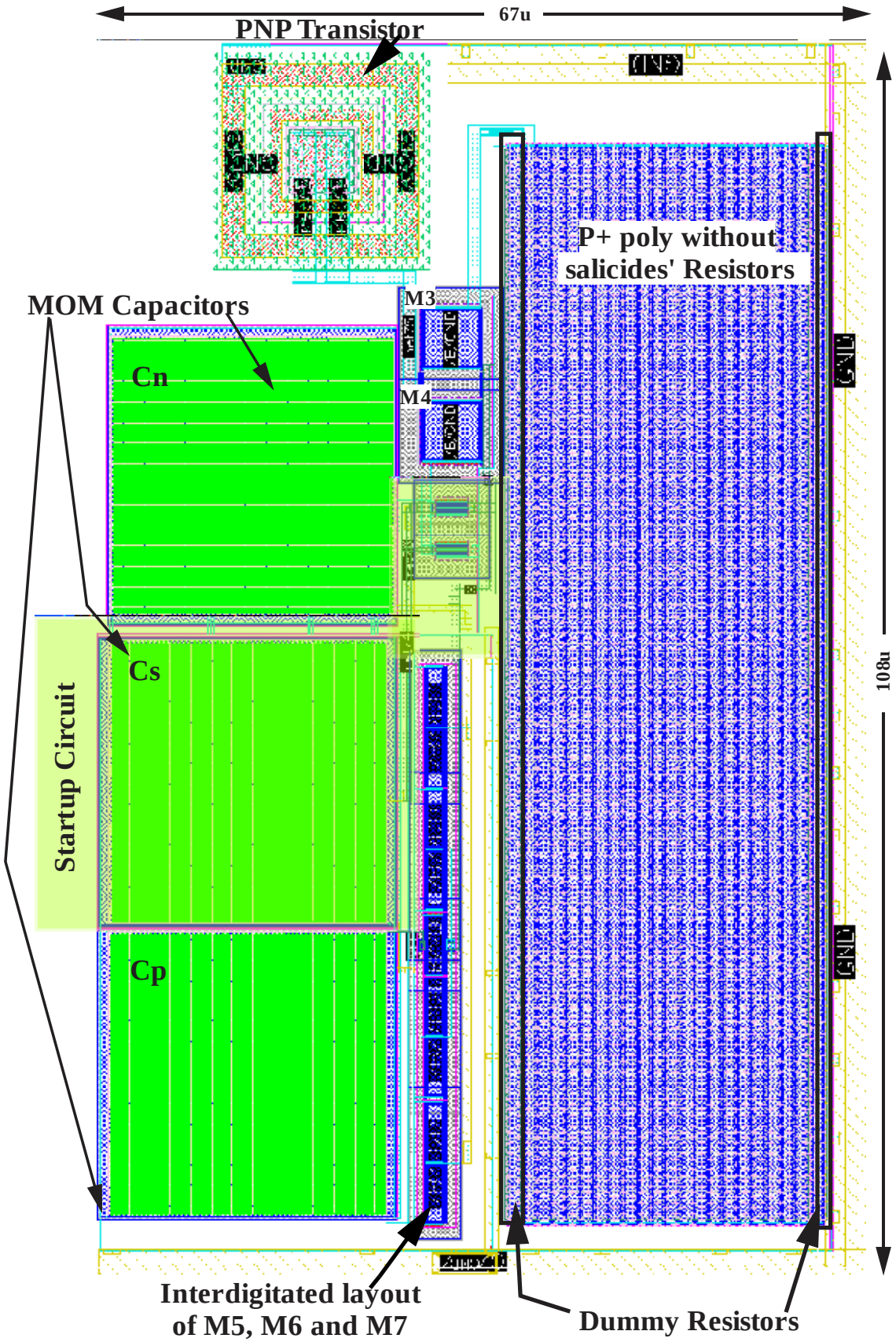



Fig.5.25. Layout of supply independent current reference.

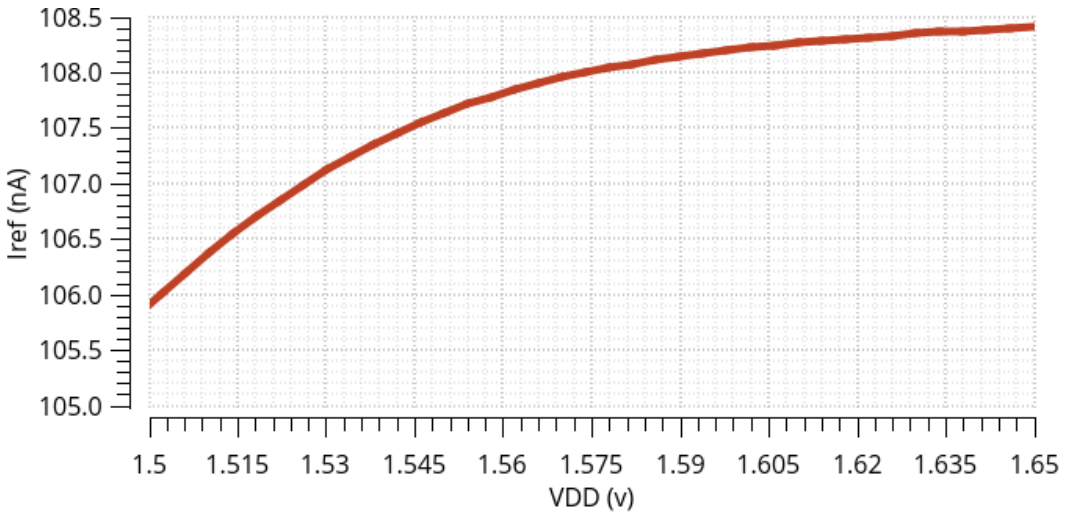



Fig. 5.26. Bias current, Iref variation with a sweep in supply voltage at 25°C

The supply independent current reference is designed to bias the OTAs of the bandgap reference and CTAT voltage reference circuit. It ensures the biasing of the OTAs in the saturation reason irrespective of fluctuation in the supply voltage and hence maintains the design operation. Fig. 5.24 shows the circuit for supply independent current reference generation circuit. This basically copies the base-emitter voltage, Vbe of the BJT, B0 (which is independent of the supply voltage) across the 1.5MΩ resistor as shown in the figure by bootstrapping the current in the two branches, using transistors M3 to M6. The capacitors, Cp and Cn in the design are used for filtering out the noise, and M1, M2 and Cs are the start-up circuit (shaded in yellow) designed to consume zero current once the current reference circuit pulls out of the degenerate biasing point.

The reference circuit is designed using a 1.8V transistor for it to work at 1.55V to 1.6V battery supply voltage and employs P+polly without silicide Resistor, MOM capacitors, and PNP bipolar transistor. The design layout is shown in fig. 5.25. To minimize the design mismatch among the current coping transistors (M5, M6, and M7) interdigitated layout topology has been used. Also, dummy P+ poly resistors were added on the two edges of the resistor R to provide uniform etching during the wafer processing.

The circuit draws a total current of 1uA at 25°C and produces a current reference, Iref of around 108nA to bias the OTAs of the voltage reference circuit. Fig. 5.26 plots the current reference variation, Iref with the change in supply voltage, and achieves the current sensitivity of 16.77nA/°C. The reference current varies from 100nA to

111nA at VDD=1.55V for the temperature variation from 0°C to 50°C. The OTAs (used in the voltage reference circuit in section 5.3.1.2) were simulated with the bias current for the temperature range from 0°C to 50°C to ensure the amplifiers stay in the saturation region at all these temperature conditions.

### 5.3.1.4. Voltage Regulator (LDO2) Design

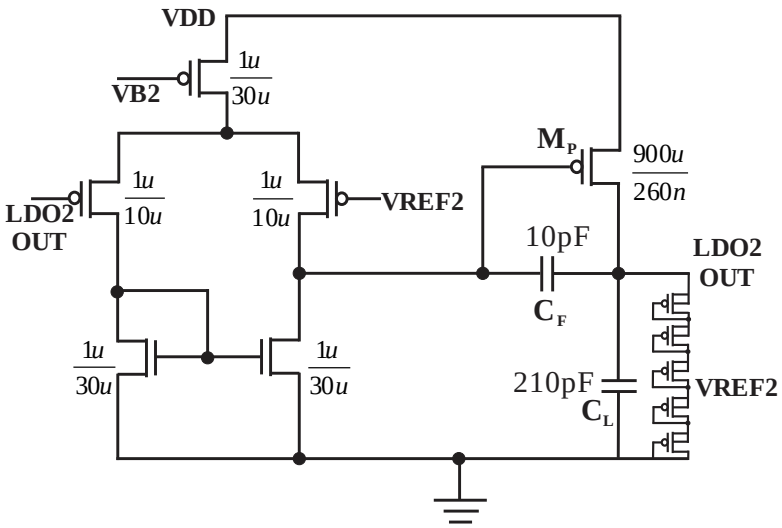



Fig. 5.27. Schematic of the voltage regulator, LDO2 to provide fixed 1V supply rail voltage for the level shifter and O/P buffer.

To drive the final level shifter and the output buffer voltage regulator, LDO2 is designed which unlike the voltage regulator, LDO1 described in section 5.3.1.1 (which provides CTAT voltage), provides fixed supply rail voltage, 1V. The schematic of the circuit with the device size is shown in Fig. 5.27 The circuit uses PMOS operational amplifier and employs the bandgap reference voltage, VREF2 discussed

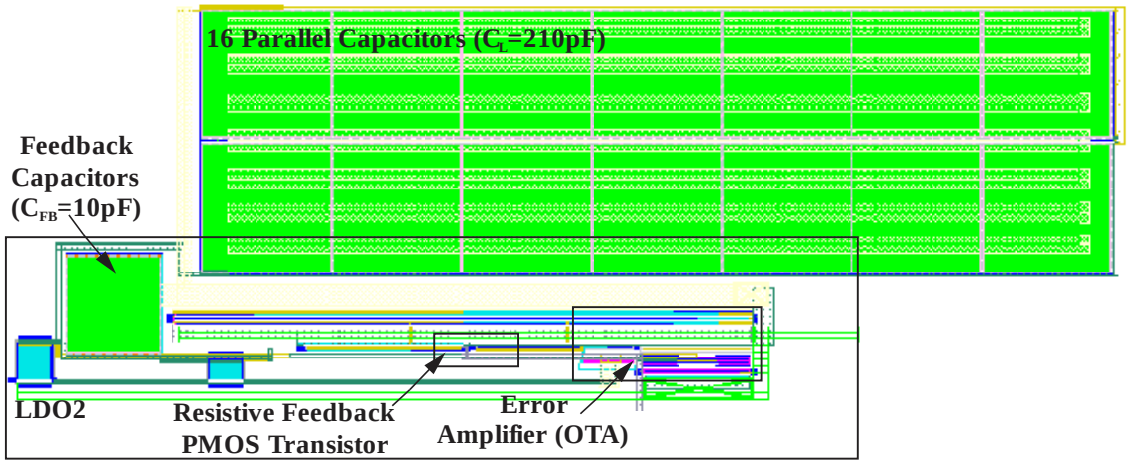



Fig. 5.28. The layout of the voltage regulator, LDO2 for the level shifter and I/O buffer

in section 5.3.1.2 as the reference voltage for the error amplifier. The resistive feedback circuit is implemented using five Low Threshold Voltage (LTVT) PMOS transistors with its body connected to the source of the transistors. The layout of LDO2 is shown in Fig. 5.28.

## 5.3.2. Level Shift and Driver Circuit Design

The complete digital telemeter circuitry works at the voltage rail decided by the voltage regulator, LDO1 which changes according to the ambient temperature to compensate for the effect of the temperature variation on the telemeter performance. This, however, results in the inconsistent voltage amplitude of the code burst signal generated for the transmission and would create a problem in the triangulation technique for the tag location in the field, since the location in this technique is decided based on the signal strength of the received wave from the transmitter.

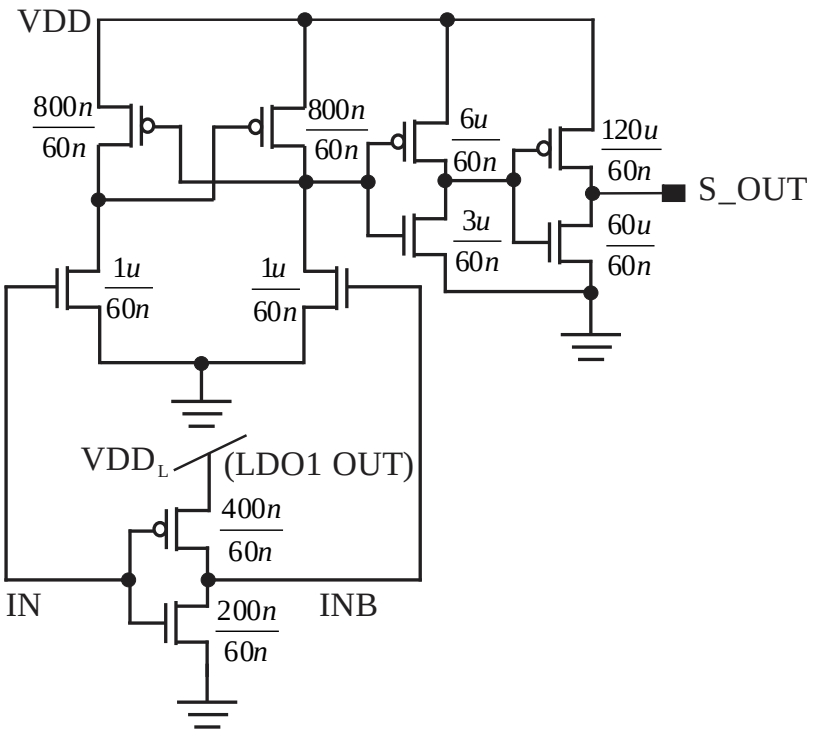



Fig. 5.29. Schematic of level shifter and tapered inverter as output driver.

To level the final output voltage amplitude of the transmitted coded burst signal independent of the temperature, a classic level shifter [91] is designed, and this is followed by a tapered inverter as an output buffer. Fig. 5.29. shows the schematic of the circuit. The size of the tapered inverter is kept very large as marked in Fig. 5.29.

to achieve low output impedance for the testing purpose (to match it to the 50Ω termination in the oscilloscope). The tapered inverters consume 863$\mu$A current during the burst mode signal transmission state at 5pF (which is an overestimation of the antenna) load while the level shifter consumes only 4.4$\mu$A. At sleep state, the driver leakage current is 4$\mu$A. It is important to note that this large current is due to the strong output driver design for the testing purpose and would not be there in the final circuit for the real telemeter. The level shifter was simulated to ensure the performance from 0$^{O}$C to 40$^{O}$C temperature with 160MHz input signal frequency (IN) having a

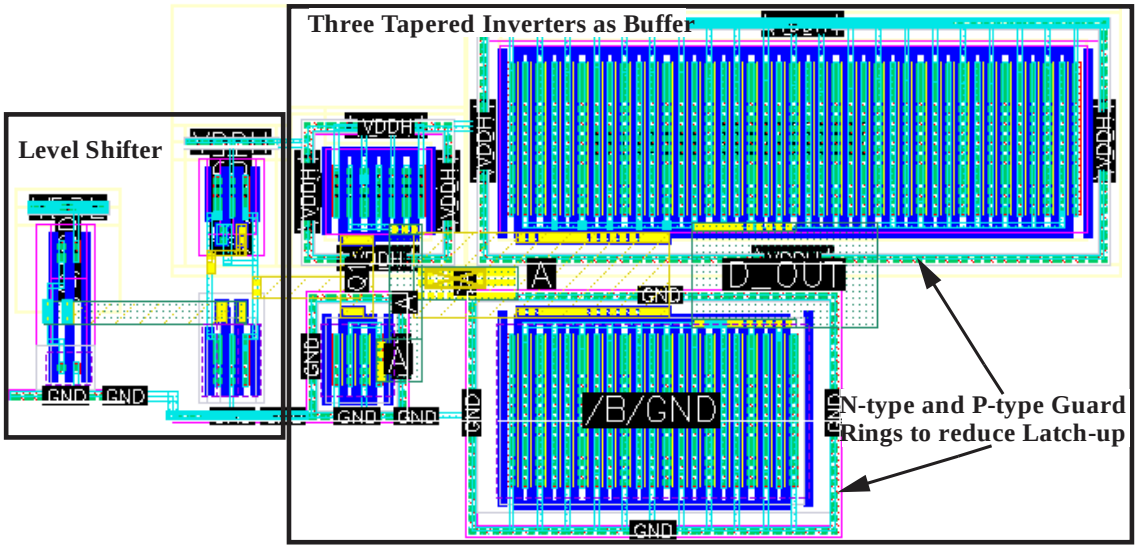



Fig. 5.30. The layout of the level shifter and output driver.

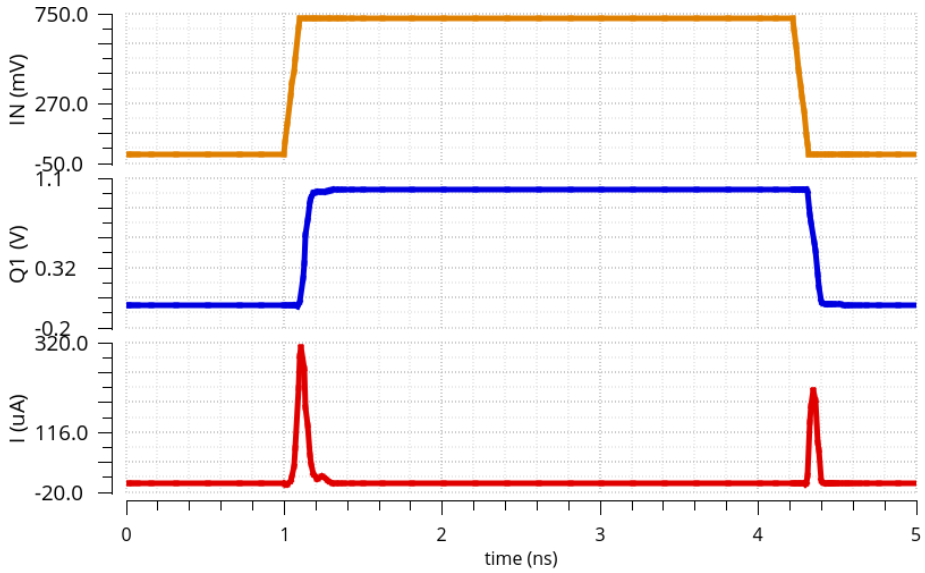



Fig. 5.31. Level shifter performance with160MHz input (IN) frequency at 25$^{O}$C and 1.55V.

voltage level of 758mV to 690mV at 0$^{O}$C and 50$^{O}$C respectively. Fig. 5.31 depicts its transient performance at 25$^{O}$C. In this, the top waveform is the input signal to the level shifter and the middle waveform (Q1) is the output signal and the bottom waveform shows the current during the switching of the signals.

### 5.3.3. Final Telemeter Circuit Integration and Chip Tape-out

The complete circuit consisting of the power management unit and the digital core telemeter circuit is integrated on the 1mm X 1mm IC chip and its layout picture is marked and shown in Fig. 5.32. The chip has 14 bond pads (with ESD), out of which two are for ground pad (GND), two for power pads (VDD) to provide 1.55V-1.6V supply from the battery, four pads for setting the 8-bit digital code for the telemeter (CODE), one separate power pad for the ESD (ESD VDD) and a separate ground pad for the ESD (ESD GND). For the experimental testing purpose, one pad is assigned to the regulator output LDO1 (LDO1) and two for the regulator output LDO2 (LDO2), and one is the telemeter signal output pad (S_OUT). Depending on the signal types each bond pad is connected with a specific ESD protection circuit as shown in Table 5.4. with its leakage power and pin capacitance [92]. These ESD cells are designed on the Metal 1 to Metal 7 metal layer leaving the top 3 metal layers (Metal 8 and Metal 9 and top AP layer) available for routing in a case to prevent electromigration problems. Separate power and ground schemes are considered to provide separate power and ground to the ESD cells and to the Internal circuit to ensure clean ground and power supply to the internal circuits. To achieve robustness of ESD and Latch-up protection, all the ESD cells are connected through fillers cornered cells.

If the I/O supply turns on before the core voltage the I/O cells could reach an unknown state which might cause a high crowbar current in the I/O. To prevent I/O cells from an undetermined state, the Power On Control (POC) [93] signal is distributed to the I/O cells. The signal is generated by POC circuitry located in the power cell PVDD2POC. This puts the I/O cells in a High Z state and once the core supply reaches high POC signal gets 0 and then the I/O cells become functional.

Table 5.4

Bond pads with their corresponding ESD cells

| Bond Pad | ESD Cell | Leakage Power (nW) | Pin Capacitance (pF) |
|---|---|---|---|
| VDD | PVDD1DGZ | 2200.3 | 4.176 |
| GND | PVSS1DGZ | 0.1139 | 1.7255 |
| S_OUT | PDO02CDZ | 710.851 | 0.0946 |
| CODE | PDIDGZ | 738.5491 | 3.7669 |
| LDO1 | PDO02CDZ | 710.851 | 0.0946 |
| LDO2 | PDO02CDZ<br>PVDD1DGZ | 710.851<br>2200.3 | 0.0946<br>4.176 |
| ESD VDD | PVDD2POC | 18424.9 | 2.2563 |
| ESD GND | PVSS2DGZ | 0.1089 | 0.5016 |

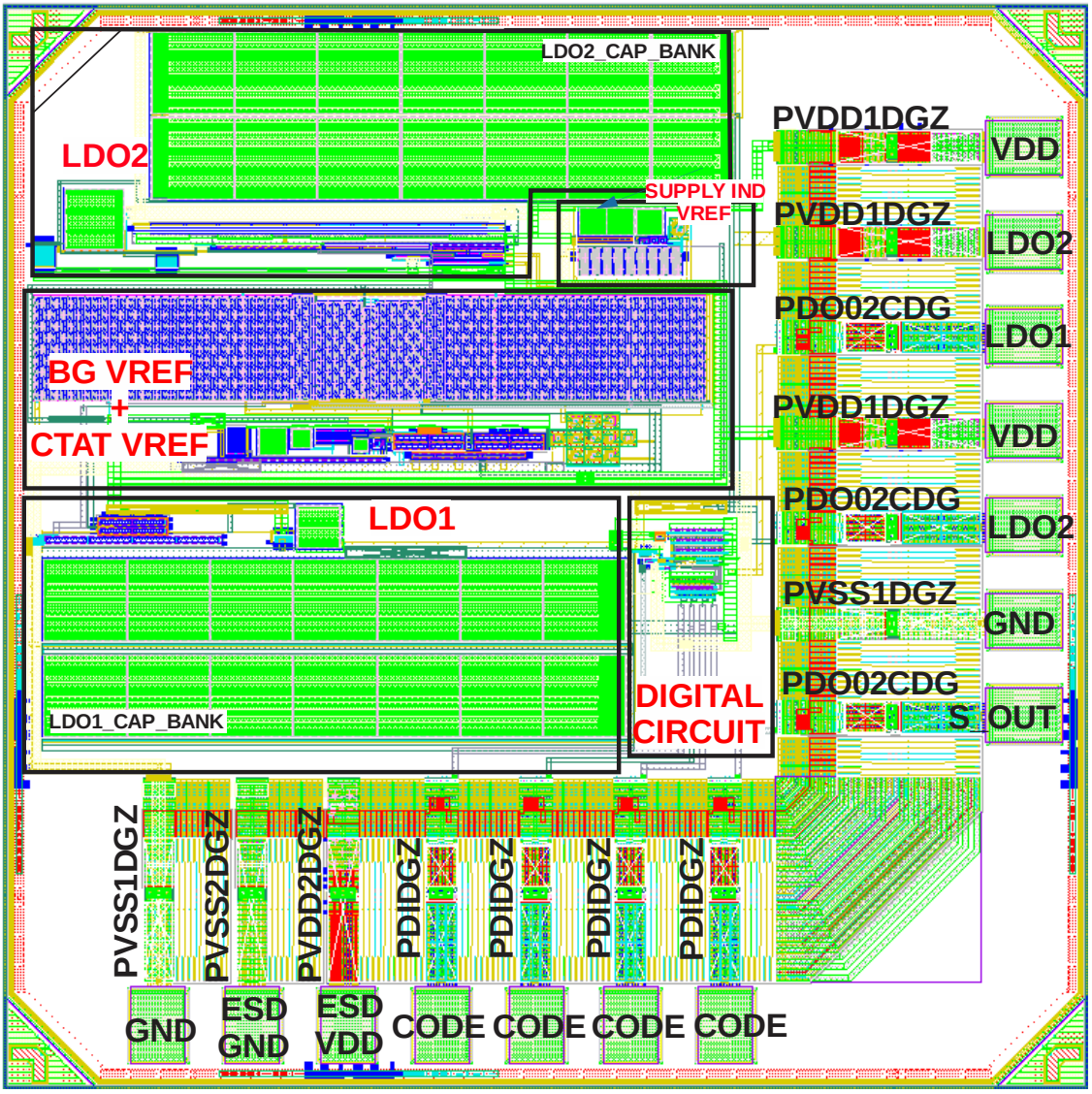



Fig.5.32 Complete 1mm X 1mm insect telemeter chip layout

For the final chip fabrication, full-chip design rules were satisfied and metal density fill utility is run to fulfill the OD, Poly and 10 metal layer (M1-M9 plus AP metal layer)

density requirement to prevent the thermal expansion stress due to density differences within the chip. Antenna rule check was run to make sure the large metal interconnect lines (which can hold lots of charge during the fabrication process and destroy the transistors if it is connected to the transistor gate) are tied down to the substrate using free wheel diode. To prevent the Latch-up problem, the CMOS transistors whose drain were directly connected to the bond pads (specifically the output driver) were placed in separate P-type or N-Type guard rings. Layout versus Schematic (LVS) verification check was run to ensure the layout has the same connections among the transistors as that in the simulated circuits. To achieve circuit simulated result closer to the expected performance of the fabricated chip, parasitic resistance and capacitance of the metal interconnect lines were extracted by running the Caliber Parasitic EXtraction (PEX) utility and these parasitic elements were included to perform the post-layout simulation. DRC waiver was requested for MOM capacitor design rule (MOM.A.2) which limited the number of capacitors to be placed in the chip due to the risk of induced charging damage to the dielectric material in the chip. Since the rule applies for 3.3V operation and the designed telemeter circuit will operate at much lower voltage, especially the capacitors will operate at 1V to 750mV, no charging damage is expected at these voltage levels. The DRC and LVS cleaned chip was sent in GDSII format to the TSMC foundry for chip fabrication.

#### 5.3.3.1 Post Layout Simulation of The Complete Telemeter Chip

Simulation of the demonstrated digital telemeter circuit has always been a difficult challenge, especially due to the extremely low duty cycle nature of the burst signal having a Very High Frequent (VHF) signal in it. The difficulty gets worse with post-layout simulation due to the addition of millions of parasitic elements to it. To overcome this challenge the circuit's functional test verification, with the parasitic element included in the circuit, was performed by setting the initial conditions of the last 10 Frequency Divider (i.e. FD19-FD28) in the circuit using the initial condition set feature of the ADEL simulator. This allowed simulating a very tiny fraction of the low duty-cycled burst signal in a reasonable time (2-3 days). The circuit was simulated at $14^{O}C$, $25^{O}C$, $27^{O}C$ and $50^{O}C$ temperature with all the parasitic included to see the performance of the proposed telemeter design with the temperature variation. Table 5.5 illustrates the details of the obtained post-layout simulation results in terms of frequency, the output voltage level of the voltage regulator, LDO1 and its settling

time, current drawn by the circuit at sleep state, and during burst mode signal generation state (shown in row 3 to row 8 respectively), for different supply voltages (VDD), temperature and output load condition as listed in the first 3 rows of the table, respectively. It could be seen from the table that the post layout simulated (including the effects of parasitic) frequency sensitivity towards temperature variation is around 0.076 MHz/$^{O}$C in the frequency range 25$^{O}$C to 50$^{O}$C compared to 2.82 MHz/$^{O}$C (shown in Fig. 5.4). Fig. 5.33. shows the simulated oscillator frequency probability density distribution at 27$^{O}$C and 1.55V ideal supply voltage to the circuit with 5pF load. This frequency variation does not include the effect of any noise present in the oscillator supply voltage due to the thermal and flickering noise added by the integrated voltage regulator.

Table 5.5
Simulated post layout telemeter circuit performance

| | | | | | | |
|---|---|---|---|---|---|---|
| VDD (V) | | 1.55 | 1.4 | 1.55 | 1.55 | 1.55 |
| Temperature ($^{O}$C) | | 14 | 25 | 25 | 27 | 50 |
| Output Load (pF) | | 5p | 5p | 10p | 5p | 5p |
| Frequency (MHz) | | 154.7 | 154.9 | 155.3 | 155.5 | 156.8 |
| LDO1 voltage level (mV) | | 735.45 | 720.4 | 721.5 | 718 | 686.5 |
| LDO1 t-settling (us) | | 190 | 246 | 190 | 200 | 232 |
| Current (uA) | sleep-state | 17.2 | 19.7 | 18 | 18.8 | 23.5 |
| | burst mode state | 635 | 490 | 570 | 575 | 620 |

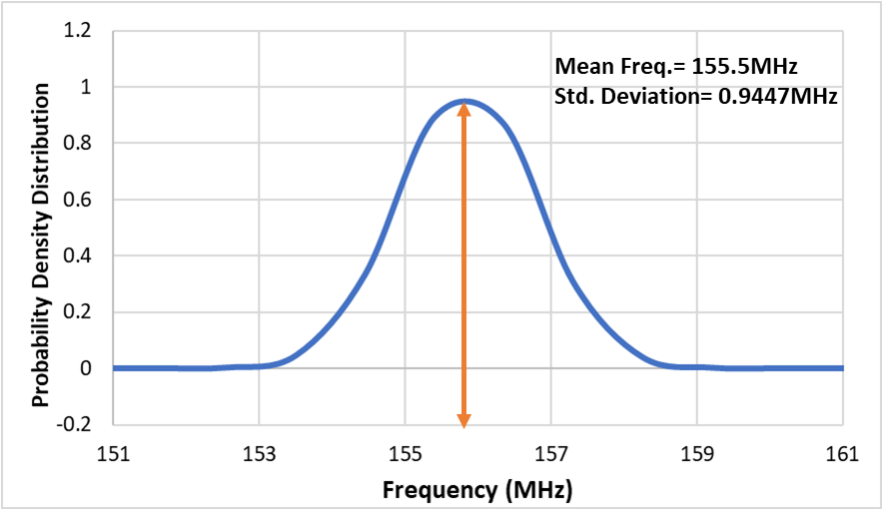



Fig. 5.33. The graph shows the simulated oscillator frequency probability density distribution at 27$^{O}$C 1.55V ideal supply voltage with 5pF load.

## 5.4. Low Power Design Challenge and Performance Tradeoffs

The insect telemeter circuit presented in the thesis consists of mostly digital circuits and an analog power management unit. The digital circuits are quite robust against noise except for the on-chip ring oscillator whose frequency would be quite sensitive to the power line voltage fluctuation. Being low power design, the analog circuitry consisting of the voltage reference and integrated voltage regulators are the only source of device electronic noise which would affect the oscillator frequency and hence device operation. Designing low-power voltage regulators with reasonable performance is a difficult challenge especially when it comes to their noise behavior. Chopping techniques [94] prove to be an efficient design approach in reducing the (1/f) flicker noise of the CMOS amplifiers but its implementation costs extra power to employ amplifiers with bandwidth higher than the switching frequency. Also, the additional necessity of a filter circuit to remove the switching noise and the requirement of the on-chip switching clock signal with a certain frequency does not prove to be much advantageous in the power stringent insect telemeter application.

One of the very common practices to lower the power consumption in the circuit is by designing the circuit in the subthreshold region [95, 96] also called the weak inversion region. This could be very easily achieved by operating a normal size CMOS transistor with gate-source voltage (Vgs) very close to its threshold voltage (Vth). However, these circuit topologies being operated at very low current significantly decrease the signal-to-noise ratio and affect the circuit performance. Therefore, the telemeter power management circuit has been realized with all the transistors in the saturation region while taking into account the design considerations for noise minimization.

The low device current in the presented PMU circuit has been accomplished by employing a larger transistor channel length, L (almost 115 times larger than the nominal size). This offers several advantages in terms of device electronic noise reduction. Firstly, thermal noise also called the white or Johnson noise arises due to the random motion of electrons in the conductor and the thermal noise in the transistor channel is the most significant source of thermal noise in a CMOS transistor. In the case of a constant current application, a larger channel length lowers the CMOS transconductance (gm) and reduces CMOS channel thermal noise. Secondly, a larger channel length also lowers the flicker noise, which is due to

the dangling bonds between the gate oxide and the silicon substrate and has a very significant noise contribution at a lower frequency. Additionally, larger channel length also benefits from the issues due to channel length modulation.

Apart from using larger channel length, other design strategies have also been considered to lower the device noise, like using multi-finger transistor with gate being connected at the two ends in the layout. This significantly reduces gate resistance and hence the associated thermal noise. Moreover, larger device sizes (both larger transistor width and length dimensioned up to several hundred square microns in 65nm process technology) have been used to increase the area and minimize the thermal noise.

The output noise voltage spectrum of the CTAT voltage reference at the output node, VREF1 is illustrated in fig. 5.34. The noise figure of VREF1 is very important for the device's performance as it acts as the reference voltage for the integrated linear regulator (LDO1) to provide a supply line for the oscillator. This noise is amplified by the regulator gain and adds to the supply voltage of the oscillator (at LDO1OUT). The device noise performance has been simulated by enabling the noise flags FNOIMOD=1 and TNOIMOD=1 [97] in the BSIM4 specter model to include the contribution of all parameters of noise in the flicker and thermal noise of the transistor, respectively. The noise voltage when integrated in the frequency band from 1Hz to 10Hz yields 20.2μV RMS voltage and corresponds to 134.13μV peak-peak noise voltage. This when compared to the present state of the art [98], low power Texas Instruments REF33xx (quiescent current: 3.9-μA, 1Hz to 10Hz noise: 35μVpp) voltage reference, the designed CTAT voltage reference achieves 4.3 times lower quiescent current (0.9μA) at the cost of 3.8 times higher noise figure.

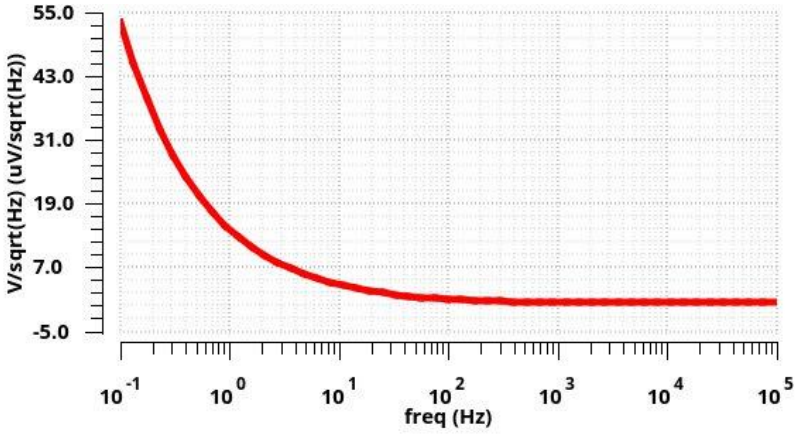



Fig. 5.34. CTAT voltage reference (VREF1) output voltage noise spectrum @ 25°C.

Fig. 5.35. shows the output voltage noise spectrum of the low power linear regulator, LDO1 which provides the power rail for the on-chip oscillator and the digital circuitry. This noise spectrum includes the noise figure of the CTAT voltage regulator and when integrated in the frequency band 1Hz to 30KHz yields RMS voltage of 179.6μV which corresponds to the 508μV peak to peak voltage and this would cause only around ±0.75MHZ fluctuation in the oscillator frequency across its nominal frequency. This small fluctuation in the oscillator frequency in the new telemeter design topology with the 8-bit digital code in the transmitted signal would not hinder the telemeter identification process.

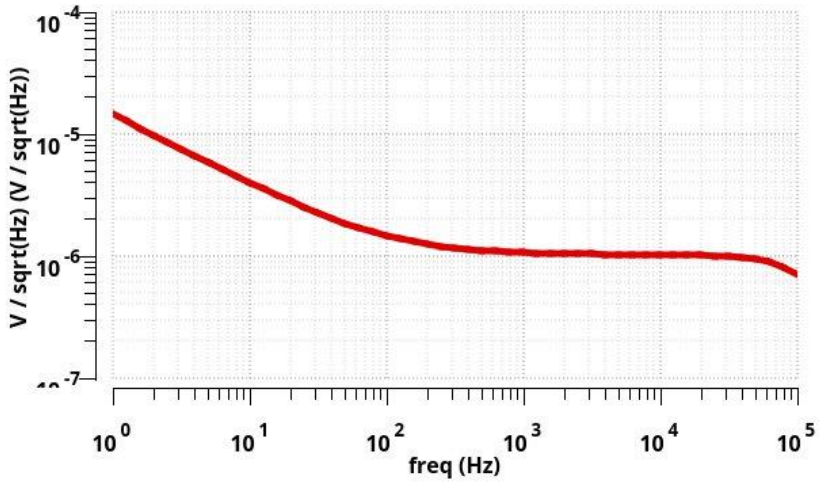



Fig. 5.35. Output voltage noise spectrum of the voltage regulator, LDO1 including the voltage reference, VREF1 noise @ 25°C with regulator output load current=150uA

## 5.5. Experimental Results and Discussion

The fabricated final IC chip was cased in Dual-In-Line (DIP) package for the prototype chip testing. The IC consisting of 14 bond pads was packed in the 18- lead DIP package and the bonding diagram of the packaged chip is shown in Fig. 5.36. Out of 18 leads in the package 14 (lead 5 to 18) were bonded to the bond pads on the chip die and the rest were left floating. Since the lead inductance is different for different leads in the dip package with leads at the corners having the larger lead inductance (pin number 8-11, 17 and 18,) while the leads at the center having the smaller inductance (pin number 5,6 and 13 to 15), it was ensured that the supply and ground pads do not bond to the leads with larger parasitic inductance to avoid the supply noise [99]. In Fig. 5.36 lead 5, 6, and 13 are the ground pin, lead 7 is the ESD supply (ESD_VDD) pin, lead 8 to 12 is the lead for setting 8-bit digital code for the tag. Lead 12 is the output signal pin, lead 14 and 17 are for the LDO1regulator

output, lead 16 is the LDO1 regulator output and lead 15 and 18 are the supply (VDD) pins.

### 5.5.1. Test-Setup

The test was conducted at first to verify the functional operation of the chip and its performance against power supply voltage variation and later against temperature variation. The test set-up used for testing the prototype chip is shown in Fig. 5.37. It uses an ADV@NTEK P3035T DC power supply to provide supply voltage to the chip, Rohde & Schwarz oscilloscope, HMO3002 featuring 400MHz 4GSa/s and Tektronix P2200 1X/10X Passive Probe featuring 200MHz for measuring the burst signal. Digital multimeter was used to measure current, and Fisher Scientific, Isotemp water bath featuring 20$^{O}$C and above temperature range to study the chip behavior at various temperatures.

The final telemeter prototype chip consists of on-chip voltage regulators to provide necessary voltage levels to the telemeter circuit. This simplifies the test board design which requires only one external supply voltage (1.55V). Chip performance against VDD was tested by setting up the circuit connection on a breadboard as shown in Fig. 5.38 (a). To examine the performance against temperature, a PCB test board was developed with the chip package fitted on a DIP socket mounted over the PCB via through-hole. This board with long supply, ground, and code, and output signal wires was put inside a glass beaker and to maintain a different temperature from the room the top of the beaker was insulated with a Polystyrene sheet as shown in Fig. 5.38 (b). A thermometer was also fitted to measure the temperature inside the beaker which is altogether put into the water bath and is shown in Fig. 5.37 with a red rectangle marked on the picture.

### 5.5.2. Measurement Results

Several packaged chips were tested in the lab to study the detailed performance of the developed telemeter IC. Unlike the previous testing performed for the digital telemeter circuit, this time due to the reduction in power supply noise provided by the integrated voltage regulator, triggering the low duty cycle burst mode signal on the oscilloscope was quite easier. Fig. 5.39 shows the measured burst mode signal result of a chip with the oscillator operating frequency ($f_0$) at 156 MHz for the 8-bit code set

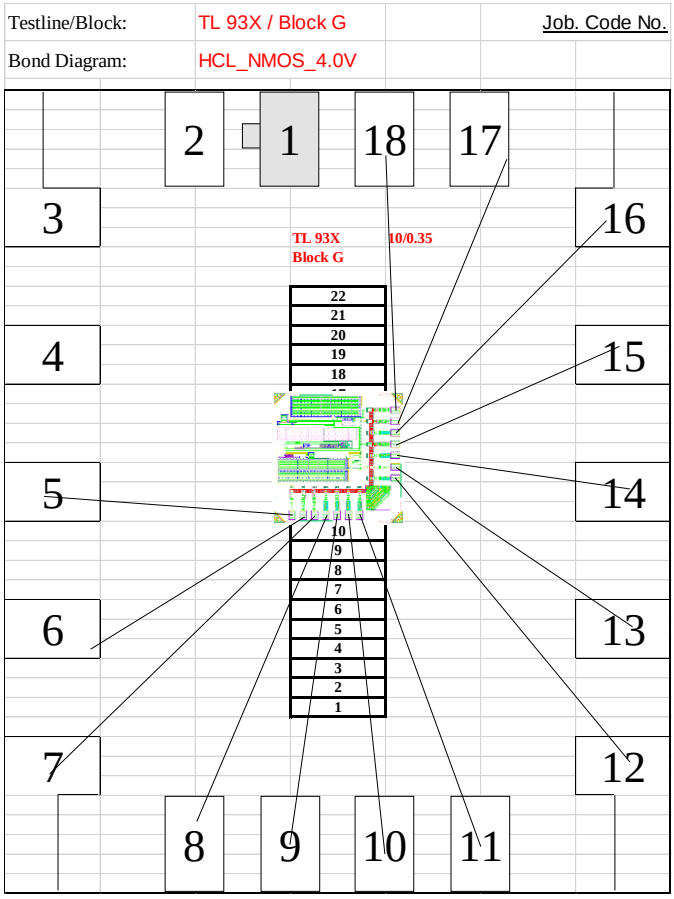



Fig. 5.36. Bonding diagram of an 18 lead DIP package for casing 1mm X 1mm telemeter chip with 14 bond pads. The 4 pins, i.e the lead number from 1 to 4 (as marked in the figure) are floating and not connected to any bond pads while the lead numbers 5 to 18 are wire bonded to the 14 bond pads on the chip as shown in the picture.

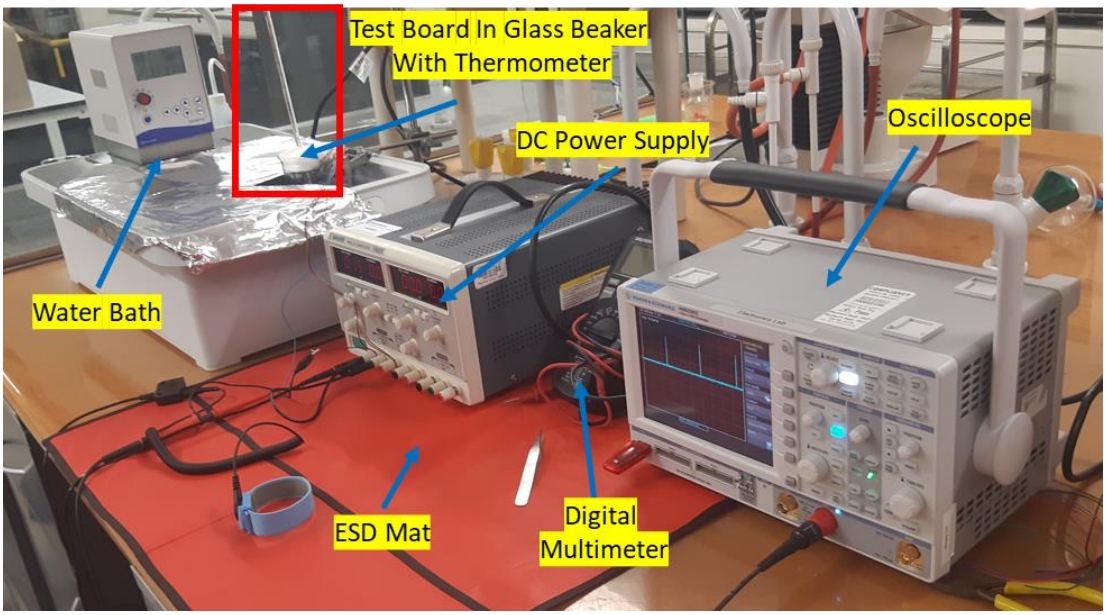



Fig. 5.37. The test set-up used for measuring the temperature variation effect on the telemeter chip.

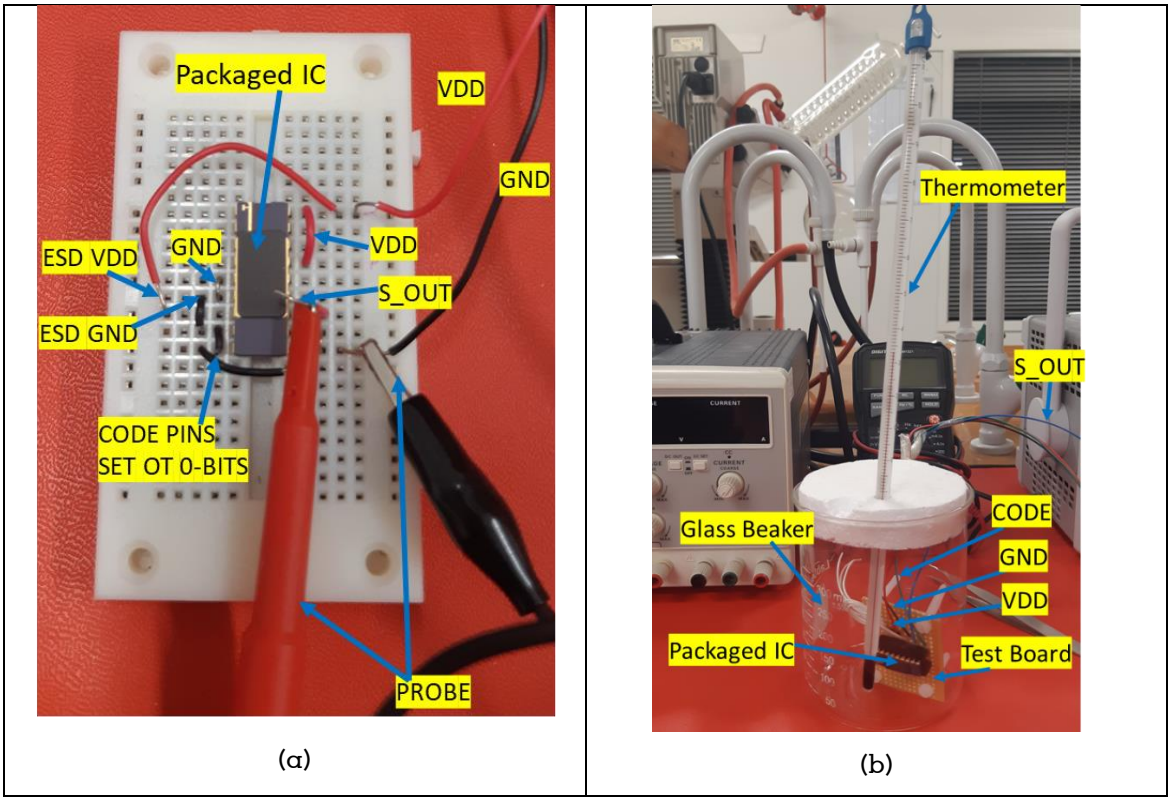



Fig. 5.38. (a) 18 lead DIP packaged telemeter chip on a breadboard for testing tag performance with supply voltage variation. (b) The packaged chip affixed on PCB test board with a thermometer inside the glass beaker packed with Polystyrene at the top

at 00000000 and at 1.55V supply voltage and 24$^{O}$C temperature. All the 8-bits of the code were set at binary 0 because, the space-frequency assigned to the FSK modulated burst signal code is $f_1$ (equal to $f_0/2$), and this halves the bandwidth of the burst signal than that for the code bits with binary 1s in it, facilitating easier and more accurate measurement. Fig. 5.40 shows the Fast Fourier Transform (FFT) of the signal inside the burst observed in the scope. The bursts were observed at every 1.7177s with the burst signal width of 13.42ms as shown in Fig. 5.40. The burst signal time period showed a variation of only a few microseconds (example 8$\mu$s difference out of 1.7177s shown between the two consecutive cycles in Fig. 5.39). This could be due to the small jitter in the oscillator frequency and also due to the small sampling error caused by the oscilloscope. The measured signal inside the burst was analyzed to determine the mean frequency which is 78.05MHz with 0.915MHz of standard deviation. The frequency determination from the measured signal is shown in Appendix B. This shows that the 95.45% of signal frequency inside the burst signal will be within 78.05 ± 1.83MHz which would be good enough for the telemeter application. From this, the Probability density distribution function of the oscillator

frequency was determined and plotted as shown in Fig. 5.42. The mean and standard deviation of the frequency are 156.117MHz and 1.83MHzrespectively. This means that the on-chip ring oscillator frequency would be within the 156.117±3.66MHz range with a 95.45% confidence level.

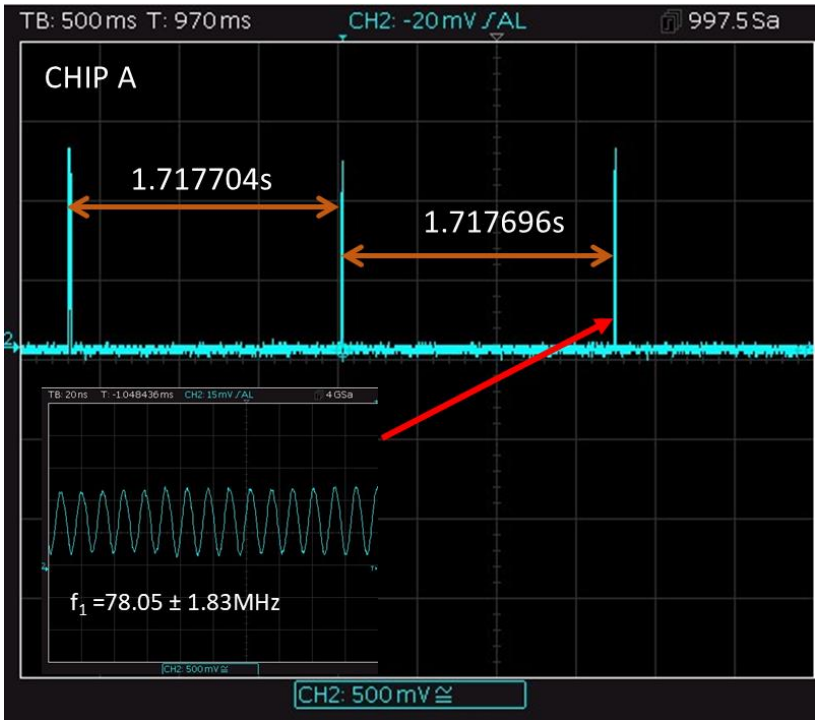



Fig. 5.39. The measured very low duty-cycled burst mode signaling for the telemeter code 00000000 operating at 156MHz at 1.55V supply voltage and 25°C ambiance temperature.

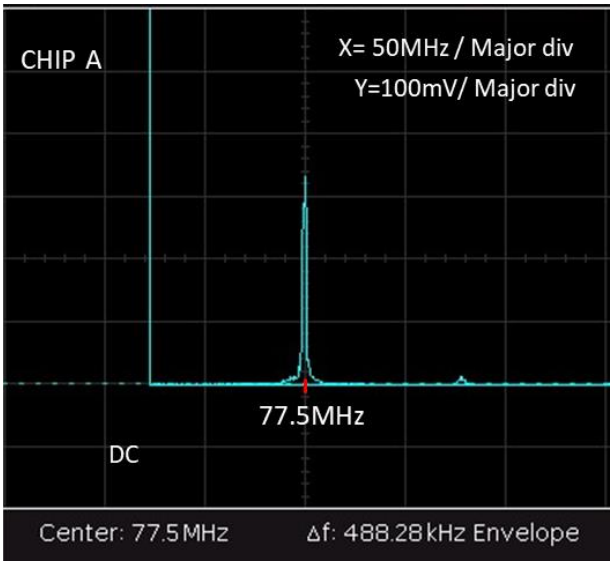



Fig. 5.40. Frequency spectrum of the burst mode signal for the tag operating at 156MHz with 8-bit identification code 00000000.

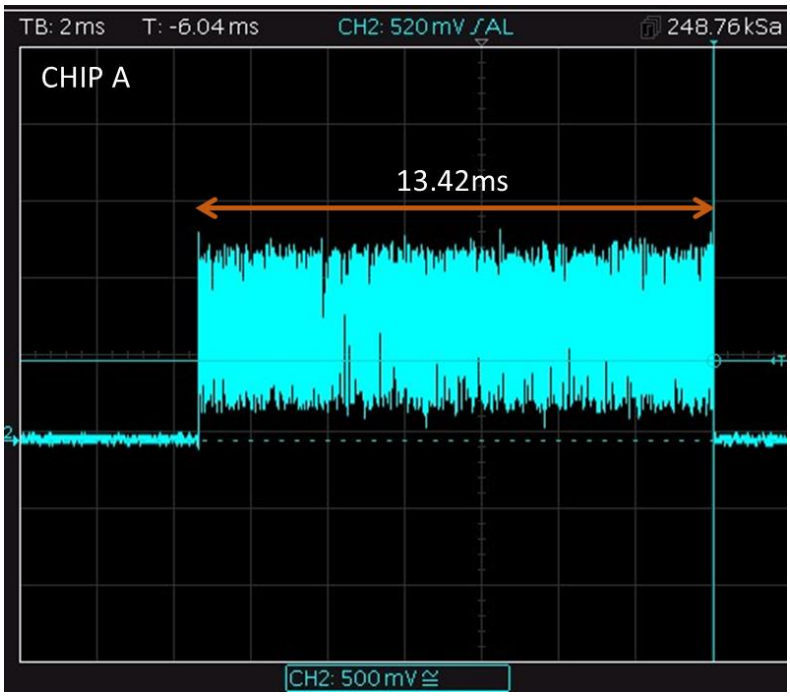



Fig. 5.41. The measured very low duty-cycled burst mode window width of the telemeter operating at 156MHz with 8-bit identification code 00000000.

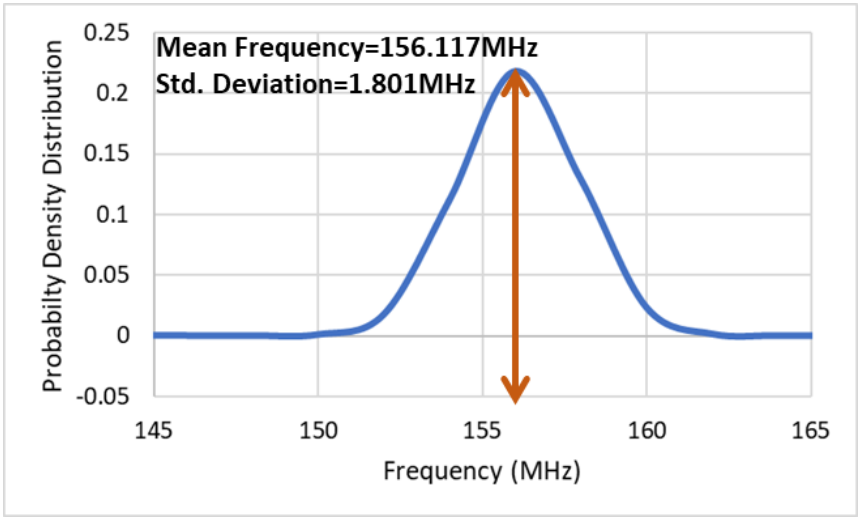



Fig. 5.42 Probability Density Distribution curve for the on-chip ring oscillator with the mean frequency of 156.117MHz and standard deviation of the frequency is 1.83MHz

The measure signal dispersion over the frequency spectrum looks quite large and therefore to determine the distribution of the signal energy over the frequency spectrum as noise, the measure signals were analyzed using the method developed equation in (3.7) and reproduced here in terms of measured space frequency of the FSK modulated signal as follows.

$$\varepsilon = F_0(t) - \frac{A_0 Sin(2\pi f_1[t+\Delta t])}{2} - \frac{A_0}{2} \quad (5.9)$$

Here, Ɛ is the noise signal present in the frequencies other than ideal sine signal with frequency $f_1$, $F_0(t)$ is the experimentally measured signal with the highest amplitude $A_0$. This is illustrated using a picture shown in Fig. 5.43. Here, the blue curve is the signal measured in the scope and has a maximum amplitude of 1200mV and the orange color signal is the ideal sinusoidal signal with DC amplitude of $A_0/2$ and frequency $f_1$ equals to 78.049MHz. The noise signal, Ɛ that is the difference between the measured and the expected ideal signal is depicted in Fig. 5.44. From this, the RMS value of the noise signal is determined to be 65.159mV and the ratio of signal power distribution in other frequencies to the ideal frequency is calculated which is only about 3.397%. This proves that most of the signal energy that is 96.6% is in the 78.049MHz and hence the jitter present in the oscillator frequency has a negligible effect on the frequency stability.

To verify the operation of the designed low power PMU, the circuit performance of four prototype chips was tested against the power supply voltage variation. Table 5.6 shows the chip behavior in terms of the measured time period, frequency, measured burst signal width, expected burst signal width, and the measured duty cycle of the burst mode signaling for the four tested chips (numbered in the first column from the

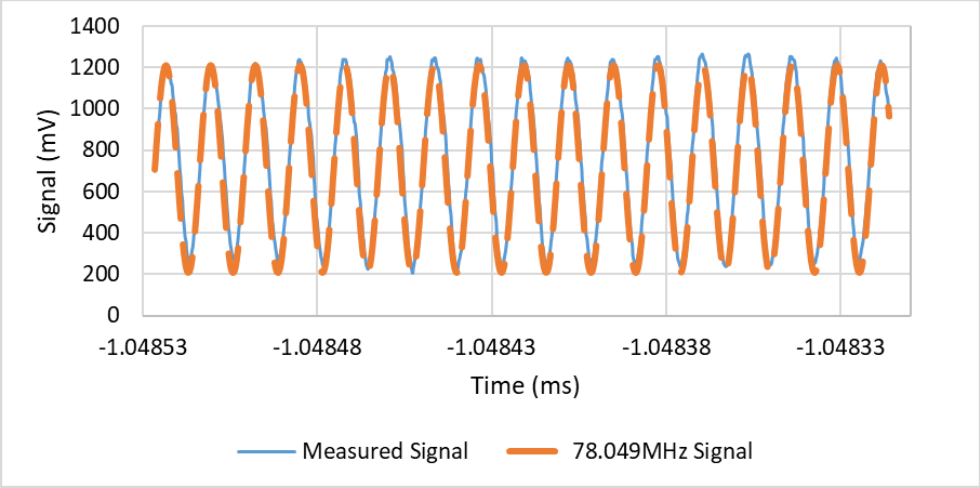



Fig. 5.43. The plots of the measured signal inside the burst window shown sa solid line in blue color and the ideal expected sinusoidal signal with DC amplitude, shown with a dashed line in orange color for the determination of the signal noise.

left) against three supply voltages (1.4V, 1.5Vand 1.6V) which are listed in the second column. These four chips worked at four different frequencies but showed good consistency in their frequencies at all three voltages. This means that the supply independent PMU designed works well against the voltage variation. The experimentally measured data for the four chips are shown in Appendix C. The measured burst width listed in 5$^{th}$ column from the left is not exactly the same as the expected one which is shown in 6$^{th}$ column. This could be due to the sampling error caused by the oscilloscope. The last column lists the measured duty cycle which is very close to 0.0078, the one achieved through the simulation.

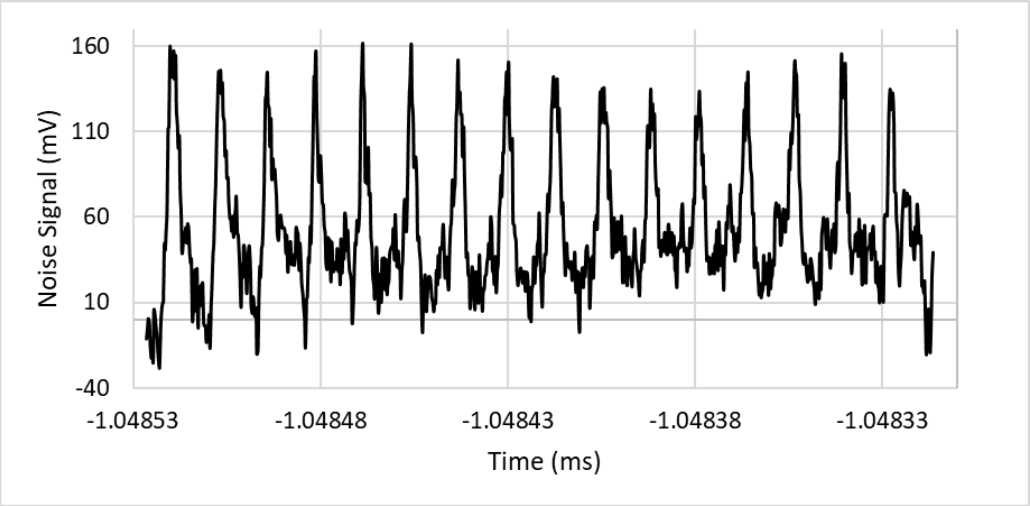



Fig. 5.44. The transient plot of the noise signal, ε present in the burst mode signaling for the tag code 00000000

Table 5.6
Measured performance of the prototype chips against supply voltage variation

| Test Chip | VDD (V) | Time Period (sec) | Frequency (MHz) | Measured Burst Width (msec) | Calculated Burst Width (msec) | Duty Cycle |
|---|---|---|---|---|---|---|
| 1 | 1.4 | 1.57006459 | 170.9709666 | 12 | 12.2661294 | 0.007643 |
| | 1.5 | 1.571458233 | 170.819475 | 12.3 | 12.27700764 | 0.00782712 |
| | 1.6 | 1.564616433 | 171.5663023 | 12.505 | 12.22356589 | 0.00799237 |
| 2 | 1.4 | 1.616585667 | 166.0511739 | 12.75 | 12.62955239 | 0.00788699 |
| | 1.5 | 1.615751133 | 166.137019 | 12.55 | 12.62302654 | 0.00776729 |
| | 1.6 | 1.6149537 | 166.2187085 | 12.25 | 12.61682285 | 0.00758536 |
| 3 | 1.4 | 1.964365 | 136.6526855 | 14.03333333 | 15.3465846 | 0.00714395 |
| | 1.5 | 1.9641479 | 136.6676401 | 14.34666667 | 15.34490534 | 0.00730427 |
| | 1.6 | 1.960855 | 136.8971474 | 15.4 | 15.31917969 | 0.00785372 |
| 4 | 1.4 | 1.473127 | 182.2215301 | 11.75 | 11.50880469 | 0.00797623 |
| | 1.5 | 1.474166667 | 182.0930259 | 11.25 | 11.51692653 | 0.00763143 |
| | 1.6 | 1.47145446 | 182.42881 | 11.525 | 11.49572811 | 0.00783239 |

Table 5.7
Chips performance against temperature variation

| TEMP ($^{O}$C) | CHIP A Frequency (MHz) | CHIP B Frequency (MHz) |
|---|---|---|
| 20 | 155.3 | 182.53 |
| 25 | 156.27 | 183.31 |
| 30 | 157.28 | 184.02 |
| 35 | 158.26 | 184.7 |
| 40 | 159.25 | 184.9 |
| 45 | 159.92 | 185.5 |
| 50 | 160.97 | 186.07 |
| 55 | 162.02 | 187.03 |
| 60 | 162.97 | 188.2 |

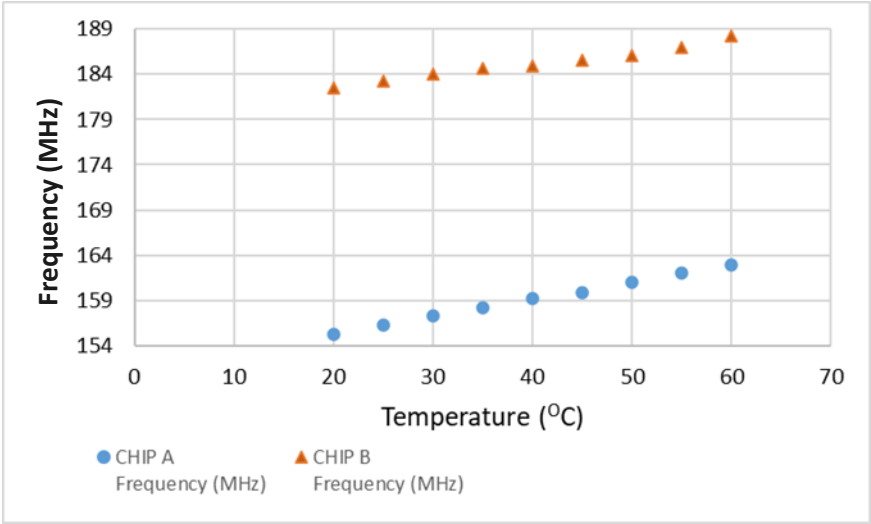



Fig. 5.45. Measured frequency variation for the chips operating at 156MHz (CHIP A) and 183MHZ (CHIP B) against temperature variation.

The effect of temperature variation on the performance of on-chip oscillator frequency is shown in Table 5.7 and plotted in Fig. 5.45 for the chips operating at 156MHz and 183MHz for the temperature from 20$^{O}$C to 60$^{O}$C. The measurement for Chip A showed an average of 0.188MHz/$^{O}$C drifts in frequency over the temperature range of 25$^{O}$C to 50$^{O}$C. This is 2.47 times larger than the post layout simulated average value in the same temperature range which is around 0.076MHz/ $^{O}$C. This could happen due to several reasons like process variation, the differences in the transistor simulation model, and the real fabricated transistor behavior which could happen partly because of the design rule waiver applied in the fabricated design, etc.

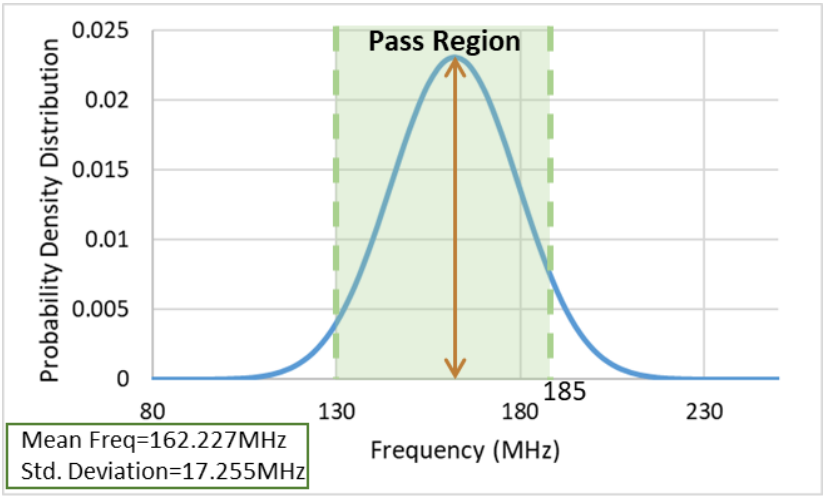



Fig. 5.46. Estimation of the chip yield for the telemeter application from the tested chips.

For the telemeter application for tracking bees, the device operating temperature range would be from 14$^{O}$C to 38$^{O}$C as bees do not prefer foraging activities at a temperature lower or higher than this range. At this temperature range, the telemeter frequency swing would maximum be around (156.25± 2.26) MHz only which would be good enough for the application. This frequency swing otherwise without temperature compensation would have varied around (162.61±25.34) MHz in the same temperature range. Another chip, CHIP B was also tested against temperature variation which shows an average frequency drift of 0.11MHz/$^{O}$C which means in the temperature range from 14$^{O}$C to 38$^{O}$C the maximum frequency swing for this chip would only be around (183.42±1.33)MHz.

Even though the fabricated chips were supposed to come from the typical- typical lot, all the prototype chips that were tested in the lab without any post-fabrication adjustment or trimming showed some distribution over their operating frequencies. This has to be due to the effect of the process variation. Also, in some of the tested chips, the carrier frequency in an alternative binary bit within the coded burst signal showed some difference in the DC level while most of the chips worked perfectly well. Ignoring these minor defects and considering only the operating frequency of the fabricated chips the yield of the prototype chip for the insect telemeter application was estimated as shown in Fig. 5.46 through the probability density distribution curve. Here the mean frequency of all the tested chips was determined to be 162.27 MHz with a 17.255MHz standard deviation. This means if chips from frequency 130MHz to185MHz are employed for insect tracking application this would yield 88.9% of the chip working.

## 5.6. The Final Size and Weight of The Digital Telemeter

The work described in the thesis, for the generation of the 8-bit coded low duty cycled FSK modulated burst mode signaling, has no off-chip discrete passive components, unlike others [17, 18, 19] where large resistors, capacitors, and transistors are used. In reality, there are multiple such passive components in a single radio telemeter design. All the components of the newly developed telemeter are on the silicon chip. The silicon chip can be grounded up to 5$\mu$m thickness and mounted directly on the silver oxide battery having the smallest size, maybe no more than 5mmX5mmX1.5mm. This design will have three metal pads, one for the Ground (GND), one for power (VDD) and one output pad on which antenna would be attached. By employing the present day's advanced packaging technology [69], this silicon chip with the antenna can be mounted directly on the negative side of the battery. The bond pads on the silicon chips could be wire bonded to the metal pads (or it could also be Kapton tape). The paper study shows that the proposed design will have a maximum weight of no more than 15mg (without battery). The tag will have a silver-oxide battery [100] having a capacity of 4 mA-hours. This battery will weigh no more than 80 mg. The whip-antenna having a total length of 10cm (3.94inch) and having a total weight less than or equal to 3mg will be used in this tag. The transmitter circuit will have an area of 1mm$^2$ and the estimated weight will be less than 2mg. The epoxy glob-top on the top of the die and wire bond will be used for silicon die encapsulation. This way the tag dimension and its weight will be the lowest ever achieved. This tag will also have the duty cycle of 0.0078 which will minimize the total power consumption and enhance the battery life. The white paper calculation of the packaging estimates the package size will be close to 5mmX5mmX1.5mm and the total estimated weight will be around 95mg, which is far better than any existing analog design. As shown in Fig. 5.47, the battery is the substrate of the package. The power pad (VDD) and output signal metal pads will be attached to it using non-conductive adhesive while the ground pad (GND) would be attached using the conductive adhesive. The metal pad or Kapton tape used to build the antenna pad can also be used to put active components for building the matching circuits for the antenna. That might increase the weight up to some extent. Fig. 5.47 shows all the dimensions and geometries for the proposed 95mg packaging with epoxy Glob-Top.

To give an idea of how small the final telemeter tag will look like, a picture of the 200mg VHF radio telemeter is shown in Fig. 5.48 along with the 1mm X 1mm ASIC telemeter chip. The 200mg tag consists of an 80mg battery and a 120mg PCB-based circuit. In the proposed telemeter package this 120mg PCB part will be replaced with the ASIC chip which will sit on top of the battery and the complete package with the battery will be only 95mg.

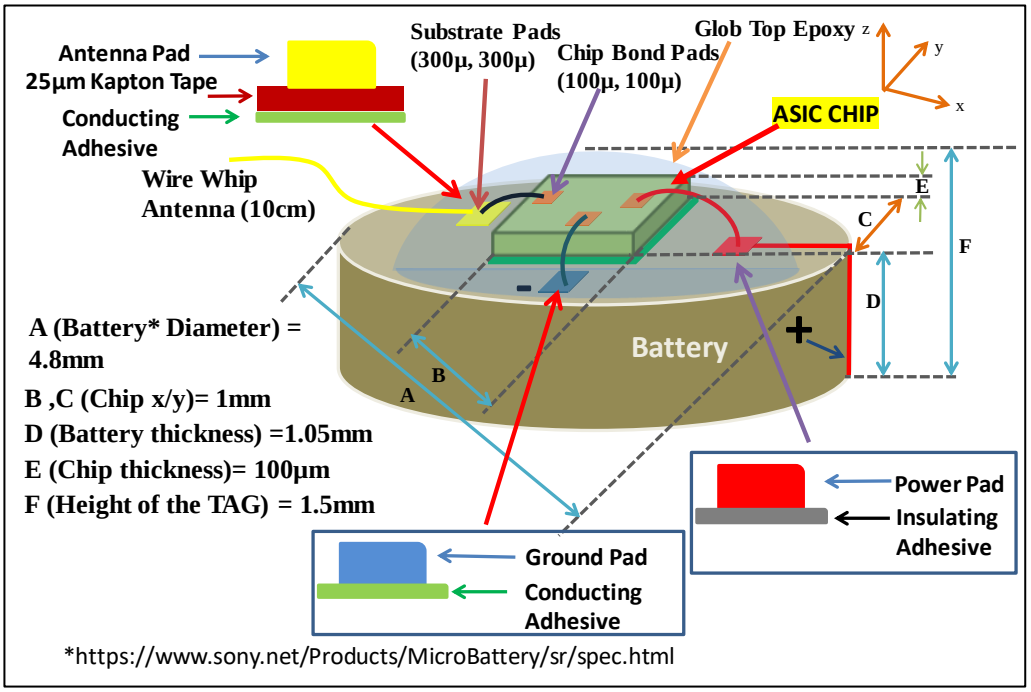



Fig. 5.47. The geometry of the telemeter packaging having a total weight of less than 95mg. This was made possible since we could design the radio frequency close to 132MHz without any passive component.

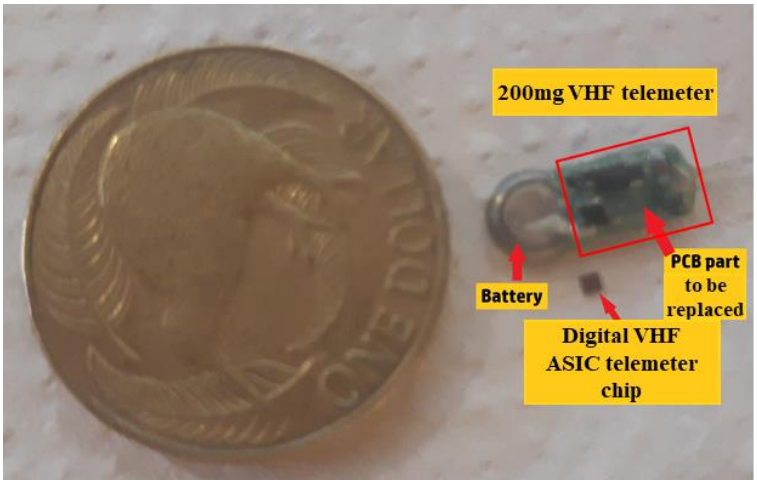



Fig. 5.48. Illustrating the relative size of the miniaturised VHF radio telemeter ASIC chip (1mm X 1mm) and the existing 200mg VHF radio telemeter having 80mg battery and 120mg PCB circuit.

## 5.7. Conclusion

A digital VHF radio insect telemeter ASIC chip is designed and fabricated in TSMC 65nm process. The tag generates an 8-bit coded burst mode signal at 0.078 duty cycle and is powered by a single supply voltage of 1.55V (silver oxide battery voltage which will be used in the insect telemeter). The 1mm X 1mm ASIC chip has a core digital telemeter circuit and low power analog power management circuits to locally generate various voltage levels required by the core digital circuit. The chip also consists of temperature compensation circuitry to minimize the effect of temperature variation on the on-chip oscillator. The DIP packaged ASIC performance is successfully tested in the lab. The fabricated chips showed some variation in their operating frequencies due to the process variation which when implemented for the product could be adjusted to increase the product yield. The ASIC performance was experimentally tested against voltage and temperature variation and the analysis of the measured data showed promising results. Most importantly this design does not require any off-chip passive component which makes the newly developed tag the lightest VHF radio tag, having an estimated weight of only 15mg without a battery and 95mg with a battery and epoxy glob-top.

# CHAPTER 6

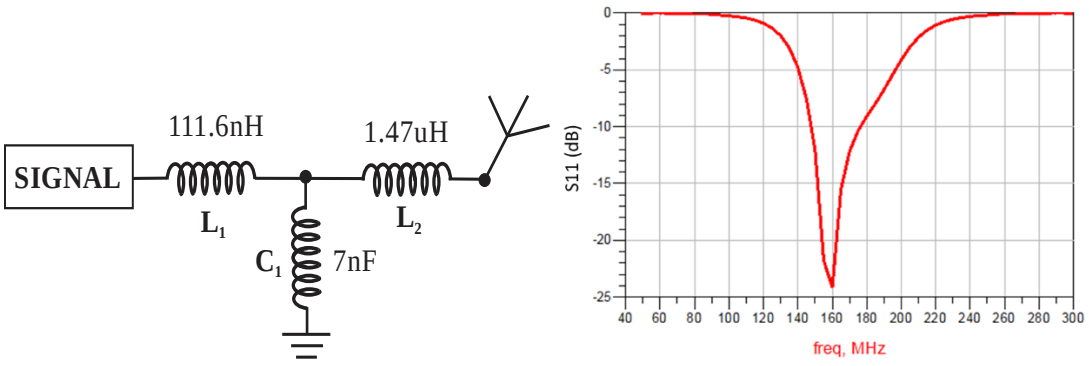
# VHF TELEMETER ANTENNA

## 6.1. Introduction

In a VHF radio telemeter, an omnidirectional whip antenna is used for transmitting the generated low duty-cycled burst signal, and its efficiency, as well as directivity, plays a crucial role in deciding the operating rage of the telemeter and for applying the triangulation technique to locate the tag position in the field. VHF antenna design for the digital insect telemeter would be another difficult task due to the small size of the antenna length and availability of the proper ground plane for the whip antenna. In the chapter, some basic simulation study is presented on electrically small monopole and loop antennas (as both are omnidirectional antenna), however for real antenna implementation would require proper research in this area.

## 6.2. Antenna Impedance Matching

The 10cm long copper wire antenna is modeled and simulated using the HFSS tool. Based on the bee's size [101, 102], the ground plane area was chosen to be 4mm X 15mm while the copper wire diameter being 2mm.




(a) (b)

Fig. 6.1 (a) Impedance matching network for whip antenna tuned at 160MHz. (b) S11 parameter simulated in ADS.

The 30um thin copper wire loop antenna was modeled with a loop diameter of 4.8mm (same as battery diameter) and is shown in Fig. 6.2. For the FSK modulated digital telemeter signal a matching network based on Direct Antenna Modulation [103] was tried to overcome the bandwidth limitation for an electrically small antenna. Here for the simulation ideal switches were used while impedance

matching and the S11 plot is shown in Fig. 6.5 (a) and the electrically small loop antenna directivity is shown in Fig. 6.5(b).

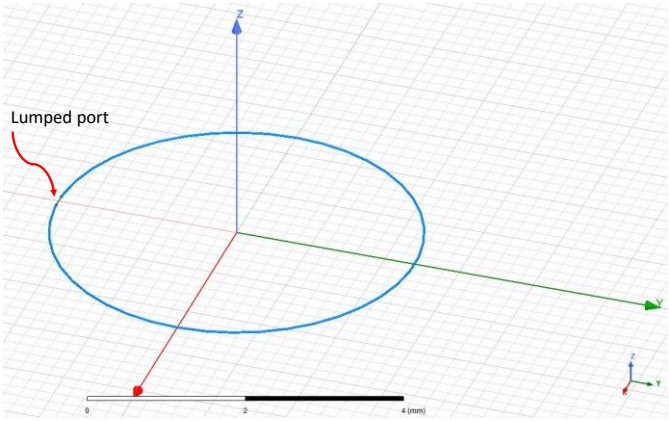



Fig. 6.2.Electrically Small Loop antenna model in HFSS

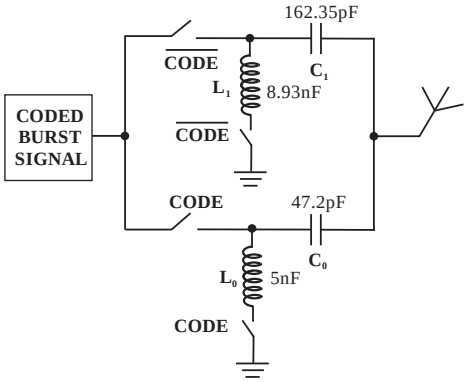



Fig. 6.3. Matching network for Loop antenna using Direct Antenna Modulation technique

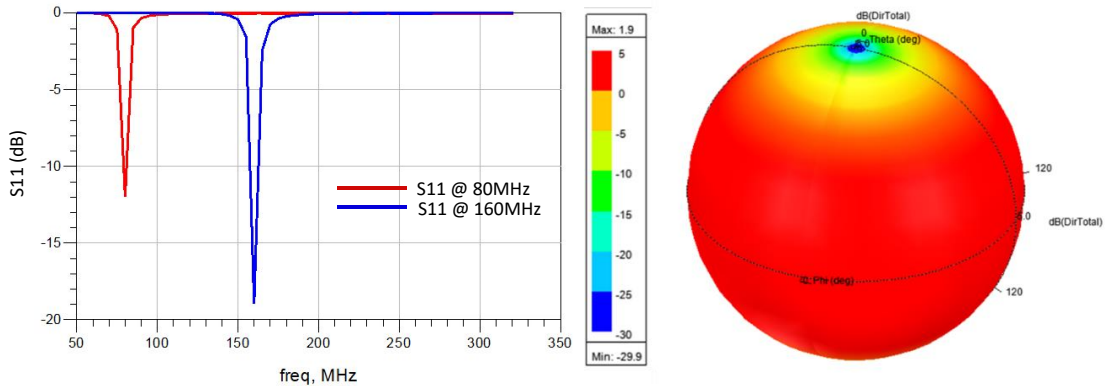



Fig. 6.4. (a) S11 parameter simulated in ADS (b) directivity for electrically Small Loop antenna.

## 6.3. Conclusion

Electrically small monopole and loop antennas were modeled and simulated in HFSS and it was found that for transmitting FSK modulated telemeter signal further research needs to be done.

# CHAPTER 7

# Conclusion and Future Works

## 7.1. Thesis Summary

The primary objective of this research is to develop a CMOS based very tiny insect VHF telemeter tag capable to track small flying insects and bees in real-time over a large distance and it must also have the individual tag identification feature to facilitate tracking of multiple tags in the field at the same time.

In order to achieve this, first, a thorough and complete study of the existing telemeter technology was done with a special focus on the field of miniaturization of the VHF radio tag. Also, a detailed analysis of the present state-of-the-art was conducted to understand the feasibility of such a design on ASIC chips. With the thorough investigation, it was discovered that the smallest present state-of-the-art which works on the principle of the crystal-based Pierce oscillator transmits signals in burst mode at a very low duty cycle. The circuit employs several passive components like inductors, capacitors, and resistors to control the duration of the bursts and the time interval between the successive burst. The tag consists of a 10cm whip antenna to transmit the signal and 1.55 volts, 80mg, silver oxide battery to powers the tag. Apart from the battery, the rest of the circuitry and packaging materials weigh around 120mg, and hence the idea to shrink the transmitter size by implementing the complete circuity, except the antenna and the crystal, into the ASIC was explored. The analysis revealed that transforming the complete existing analog circuitry into ASIC is not feasible. The bottleneck arises from the use of large passive components to control the interval time and the duration of the burst mode. Therefore, further research was done to explore and develop a digital approach to solve the device miniaturization challenge.

A new method to generate an extremely low duty cycle signal was developed to transmit a very low duty-cycled signal in burst mode for telemetry application. Unlike all the exiting design methodology to generate low duty cycle signals the new methodology proposed in this thesis is completely digital and does not require any passive elements. Implementation of this technique in insect's telemeter shows a viable direction for the tag miniaturization and the methodology was realized on

IBM CMOS8RF 130nm technology to produce 150MHz burst mode signaling with a duty cycle of 0.0078. Due to simulation inconvenience, the design was realized using 13-FDs instead of 28-FDs and the chip was fabricated after the complete DRC and LVS verifications followed by PEX extraction and the post-layout simulation of the circuit. The schematic simulation and the post-layout simulation results revealed a huge difference in the performance of the circuit. This is primarily due to the parasitic component introduced in the layouts. The fabricated chip was QFN packaged and a PCB test board was designed with QFN socket mounted on it to experimentally test the packaged chip in the lab. Due to not having the right frequency bandwidth scope for the testing, the performance was analyzed at 132MHz and 3.2MHz to study the performance in the manufacturing environment. The standard deviation of the chip tested at a mean frequency of 132MHz was calculated to be 2.8MHz. However, from the measured results it was also determined that 99% of the burst mode signal energy is in the 132MHz frequency and the rest only 1 % energy is distributed in all other frequencies which proves the jitter of the on-chip oscillator is not significant and the proposed method which requires only 0.028mm$^2$ on active chip area works good for low duty cycle burst mode signaling and could replace the classic telemeter design for miniaturizing the tag size and weight.

To make the tag identification more robust to frequency variation, a new telemeter architecture was designed which would transmit 8-bit coded RF burst mode signals at an extremely low duty cycle. Each tag will be coded differently before packaging the chip for individual identification and the modulated carrier wave will be utilized for triangulation technique to find the location of the tag and hence of the insects. PISO shift resistor was utilized for the generation of the 8-bit code which is further FSK modulated for transmitting the signal in burst mode at 0.0078 duty ratio. This design was implemented on 8HHP 28nm process technology using 28-FDs. The design being digital, simulation of one complete cycle with 28 FDs was made possible by simulating the design in parts while modeling the equivalent load capacitance of the further digital blocks. The complete layout of the design was done including the DRC and LVS verification and the density requirement was satisfied for the chip taped out. Further, PEX tool was run to extract the parasitic components from the layout and was included in the post-layout simulation. In this process technology, the pre and post-layout simulation results were very close, and it showed the process file has taken care of the parasitic components quite well in the

pre-layout simulation. In order to analyze the effect of process variation on the oscillator frequency, PSS analysis is also done for all the process corners and for various control voltage. Also, PSRR and power supply noise analysis were performed to study the stability of the oscillator against supply noise. Various other analysis was done to see the effect of PVT variation on the performance of the telemeter. However, the chip could not be fabricated in a 28nm process due to very high fabrication cost and the complete design was reimplemented on TSMC 65nm technology. Three variants of the circuits (one simple burst mode signaling using 28-FDs, another one with coded digital design without ESD, and the third one with the coded digital design and ESD protection) were put into the 1mm X 1mm chips for the experimental analysis and the chip was fabricated after the complete design verifications including DRC and LVS check and the post-layout simulation including the PEX extracted components from the layout to see the more accurate result. The fabricated chip was QFN packaged and a PCB test board was designed with the QFM socket mounted on it for the chip testing. Out of the three, only the circuit with ESD protection worked and the coded burst mode signal was with FSK modulation was captured in the oscilloscope at an oscillator frequency of 157MHz and 4.47MHz. However, due to the slow transient response of the DC power supply huge variation in the oscillator frequency was observed for 157MHz measurement which generated some inconsistency in the burst mode signaling. Therefore, design operation was also verified at 4.47MHz which matched quite well with the simulated data.

The digital design developed required three external power supply, at three different voltage levels, and also the oscillator frequency changes significantly with the change in temperature which would affect the telemeter performance. Therefore, to power the telemeter circuit with a single 1.55V supply and to address the issue with temperature variation final telemeter prototype was developed in TSMC 65nm technology. This consisted of the digital design along with the low power, power management unit to generate the required voltage levels locally using integrated voltage regulators. and also, bandgap and CTA voltage reference were used for the temperature compensation of the oscillator. The fabricated prototype chip was cased in a DIP package and performance was experimentally tested against power supply voltage variation and temperature variation. The analysis of the measured results showed a very slight change in circuit performance with the voltage variation and has a maximum of ±2.26MHz variation in frequency within the operating temperature range ($14^{O}$C to $38^{O}$C) of the telemeter. These small variation guarantees

no trouble in the telemeter operation and identification process in the field and validates the successful prototype performance in the manufacturing environment.

## 7.2. Possible Future Scope

This thesis has shown a new design architecture prototype that for the first time could implement a VHF radio telemeter into a single ASIC chip to yield the world's smallest VHF radio telemeter for insect tracking. To take this insect telemeter prototype towards the commercial production certain area (packaging and antenna design) requires further work and slight improvements could be made at the circuit level to optimize the performance. In this section, some future direction is shown in those areas to complete a VHF insect telemeter tag.

### 7.2.1. Packaging

In this thesis, a white paper study has already been presented to develop the telemeter packaging over the silver oxide battery which requires hands-on work to find the right metallization for the metal pads which could be directly wire-bonded to the bond pads in the ASIC chip.

### 7.2.2. Antenna Design

The transmission of the FSK coded burst mode signal would require proper research into electrically short antenna design with a good radiation efficiency and bandwidth to transmit the signal at high efficiency. This would include the impedance matching of the antenna with the output driver which could be done on-chip or directly over the battery using the output metal pad.

### 7.2.3. Power Reduction and Performance Improvement

The telemeter circuit consumes low power due to very low duty cycle operation and low quiescent current PMU. This could be further reduced many folds by designing the digital circuit near-threshold voltage operation, reducing down the duty cycle even further, and optimizing the power of the analog circuitry. The final ASIC would also require to include the fuse to program the 8-bit code in each tag. Also, the temperature compensation and the chip yield could be optimized further by including the adjustment (described in chapter 5) against process variation.

# BIBLIOGRAPHY


[1] The Migratory Connectivity Project- Radio Telemetry [online]. Available: http://www.migratoryconnectivityproject.org/vhf-radios/#automated-tracking

[2] ATS tracking products [online]. Available: https://atstrack.com/tracking-products.html

[3] R. Kays, *et al.*, "Tracking animal location and activity with an automated radio telemetry system in a tropical rainforest" The Computer Journal 54, 1931–1948, 2011.

[4] R. Kays, M. C. Crofoot, W. Jetz and M. Wikelski, "Terrestrial animal tracking as an eye on life and planet," Science, vol. 348, issue 6240, Jun. 12, 2015.

[5] D. L. Murray and M. R. Fuller, "Research Techniques in Animal Ecology: Controversies and Consequences." Columbia Univ. Press, New York, 2000, pp. 15-64.

[6] E. T. Cant *et al.*, "Tracking butterfly flight paths across the landscape with harmonic radar," Proc. R. Soc. London B, vol. 272, pp. 785-790, Apr. 2005.

[7] W. Daniel Kissling, David E. Pattemore and Melanie Hagen, "Challenges and prospects in the telemetry of insects", Biol. Rev., 89, pp. 511–530, 2014.

[8] Lotek Nanotags for Insects [online]. Available: https://www.lotek.com/products/nanopin/

[9] Advance Telemetry System (ATS)- T15 Tiny Transmitters [online]. Available: https://atstrack.com/tracking-products/transmitters/product-transmitters.aspx?serie=T15

[10] Jaboury Ghazoul "Buzziness as usual? Questioning the global pollination crisis," Trends in Ecology and Evolution, Vol.20 No.7, July 2005

[11] M. A. Aizen, L. A. Garibaldi, S. A. Cunningham and A. M. Klein, "How much does agriculture depend on pollinators? Lessons from long-term" trends in crop production," Annals of Botany, pp. 1579-1588, Apr. 2009.

[12] Jerry J. Bromenshenk, et al., "Method and Aparatus for conditioning Honey Bees" US 6,896,596 , May 2005

[13] C. D. Lemunyan, W. White, E. Nyberg and J. J. Cristian, "Design of a Miniature Radio Transmitter for Use in Animal Studies," J. Wildlife Management, vol. 23, pp. 107-110, Jan. 1959.

[14] L. N. Barr, "The radio transmission of physiological information," The Military Sergeon, vol. 114(2), pp. 79-83, 1954.

[15] R. S. Mackay and B. Jacobson, "Eendoradiosonde," Nature, vol. 1957, pp. 1239-1240, Jun. 1957.

[16] W. W. Cochran and R. D. Lord, "A radio tracking system for wild animals," J. Wildlife Management, vol. 27, pp. 9-24, 1963

[17] B. Naef-Daenzer, "A new transmitter for small animals and enhanced methods of home-range analysis," J. Wildlife Management, vol. 57, pp. 680-689, 1993.

[18] B. Naef-Daenzer *et al.*, "Miniaturization (0.2 g) and evaluation of attachment techniques of telemetry transmitters," Journal of Experimental Biology, 2005.

[19] Advance Telemetry System (ATS)- Transmitters [online]. Available: https://atstrack.com/tracking-products/transmitters/product-transmitters.aspx?serie=A2405

[20] Q. S. Lea, J. Kim, Jimsu Kim, H. I. Son, "Report on Work in Progress of Small Insect Tracking System using Autonomous UAV," 14th Int. Conf. Ubiquitous Robots and Ambient Intelligence (URAI), Jeju,Korea, Jul. 2017.

[21] N. L. Carreck, J. L. Osborne, E. A. Capaldi and J. R. Riley, "Tracking bees with radar," Bee World, vol. 80(3), pp. 124-131, Jan. 1999.

[22] E. A. Capaldi et al, "Ontogeny of orientation flight in the honeybee revealed by harmonic radar," Nature, vol. 403, pp. 537-540, Feb. 2000.

[23] SicVision, Inc.- Harmonic Radar Frequency Selection. [online] available: https://www.scivision.co/harmonic-radar/

[24] C. W. Schneider, J. Tautz, B. Grunewald, S. Fuchs, "RFID Tracking of Sublethal Effects of Two Neonicotinoid Insecticides on the foraging Behavior of *Apis Mellifera*," PLoS ONE, vol. 7, issue 1, Jan. 2012.

[25] Mickeal Henry et al., "A Common Pesticides Decrease Foraging Success and Survival in Honey Bees," Science, vol. 336, pp. 348-350, Apr. 2012

[26] M. Charreton et al., "A locomotor Deficit Induced by Sublethal Doses of Pyrethoid and Neonicotinoid Insecticides in the Honeybees *Apis mellifera*," PLoS ONE, vol. 10, issue 12, Dec. 2015.

[27] A. T. Alkassab and W. H. Kirchner, "Assessment of acute sublethal effects of clothianidin on motor function of honeybee workers using video-tracking analysis," Elsevier Ecotoxicology and Environment Safety, vol. 147, pp. 200-205, Aug. 2017.

[28] N. R. Larson and T. D. Anderson, Video Tracking Protocol to Deterrent Chemistry for honey bees, [online] Available: https://www.jove.com/video/55603/video-tracking-protocol-to-screen-deterrent-chemistries-for-honey-bees

[29] Marvin E. Frerking, "Oscillator Circuit," in Crystal Oscillator Design and Temperature Compensation, NY, USA, 1st ed., VNR, 1978, pp. 56-110.

[30] E. A. Vittoz, M. G. R. Degrauwe and S. Bitz, "High-Performance Crystal Oscillator Circuits: Theory and Application," *IEEE J. Solid-State Circuits*, vol. 23, no. 3, pp. 774-783, Jun. 1988.

[31] Maxim Integrated- Design a crystal oscillator to match your application, [Online] Available: https://www.maximintegrated.com/en/app-notes/index.mvp/id/5265

---

[32] Jeremy Blum, "Digital Inputs, Outputs, and Pulse-Width Modulation," Exploring Arduino, Wiley, 2018.

[33] R. Kumar, Dahiya and K. Kumar. "Design and implementation of Actable Multivibrators for Different Applications in Communication System," Int. J. Advances in Elect. Electr. Eng. (IJAEEE), vol. 2, no. 2, pp. 274-282, 2013.

[34] Seals David George et al., "Radio telemetry monitoring system," EP Patent, 0407776A2, Jan. 16, 1092

[35] Atallah et al., "Precise and programable duty cycle generator," U.S. Patent, 6,593,789, Jul. 15,2003.

[36] Ryusuke Kato, Katsuyuki Fujii *and Masayuki Asanuma, "A Simplified Model for Designing Whip Antenna", 2017 IEEE 6th Global Conference on Consumer Electronics (GCCE 2017),* Nayoga, Japan, Oct. 2017.

[37] N. H. Weste and D. M. Harris, "Testing, Debugging and Verification," CMOS VLSI Design, Addison Wesley, NY, USA, 4th ed., pp. 659-697,2011.

[38] Taqi Mohiuddin, "Focused Ion Beam (FIB) Circuit Edit," ASM Int., vol. 16, no.3, pp. 20-23, 2014

[39] Bidyut K. Bhattacharyya, AlexLevin ; Gang Huo, "A semi-empirical approach todetermine the effective minimum current pulse width (t) for an operating silicon

chip", 2007 International Power Engineering Conference (IPEC 2007), pp. 922-927, Singapore, Dec. 2007.

[40] Bidyut K. Bhattacharyya ; Debasis Baral ,"Method to Simulate Rise Time of Current Drawn by a Microprocessor", IEEE Transactions on Components, Packaging and Manufacturing Technology Year: 2013 , Volume: 3 , Issue: 10 Page s: 1731 – 1736

[41] D. Mallik ; B.K.Bhattacharyya, "High-Performance PQFP", page no. 494-503 Proceedings., 39th Electronic Components Conference, Houston, TX, USA, May 1989.

[42] Wire bond impedance and attenuation [online]. Available: https://www.microwaves101.com/encyclopedias/wirebond-impedance-and-attenuation.

[43] Nathan E. Flowers-Jacobs , Alessio Pollarolo , Kevin J. Coakley, Adam C. Weis , Anna E. Fox , Horst Rogall1 , Weston L. Tew , and Samuel P. Benz, "The NIST Johnson Noise Thermometry System for the Determination of the Boltzmann Constant", Journal of Research of the National Institute of Standards and Technology, Volume 122, Article No. 46 (2017) https://doi.org/10.6028/jres.122.046

[44] R.H. Evans, "What does a 1-sigma, a 3-sigma or a 5-sigma detection mean?" the curious astronomer, 26/06/2014 [online]. Available: https://thecuriousastronomer.wordpress.com/2014/06/26/

[45] QFN Socket [online]. Available: https://docs-apac.rs-online.com/webdocs/0d52/0900766b80d527bf.pdf

[46] Jiyuan Luan ; Campbell Blackie , "Analysis and Experimental Study of the Package Stresses in a QFN Plastic-Encapsulated Package", IEEE Transactions on Components, Packaging and Manufacturing Technology ,Year: 2014 , Volume: 4 , Issue: 8 Page s: 1303 – 1308

[47] M. Amourah and M. Whately, "A novel switched-capacitor-filter based low-area and fast-locking PLL", IEEE Conf. Custom Integrated Circuit (CICC), Sept. 28-30, 2015.

[48] Bee keeping organization. [online]. Available: https://www.uky.edu/Ag/Entomology/ythfacts/4h/beekeep/basbeop.htm

[49] Shruti Suman and Prof. B.P. Singh, "Design of Temperature Sensor Using Ring Oscillator", International Journal of Scientific & Engineering Research Volume 3, Issue 5, May-2012 1 ISSN 2229-5518.

[50] CMC MICROSYSTEM, "DESIGN KIT: GF (IBM) 0.13 $\mu$M CMOS" https://www.cmc.ca/en/WhatWeOffer/Products/CMC-00000-48598.aspx

[51] Joseph Allen, "Use of Coded Transmitter Schemes to Overcome Radio Frequency Spectrum Constraints in Terrestrial Wildlife Tracking". [online]. Available: https://atstrack.com/assets/documents/Use-of-Coded-Transmitters-in-Wildlife-Telemetry-Systems.pdf

[52] Klaus Finkenzeller, R F I D H and book: Fundamentals and Applications in Contactless Smart Cards, Radio Frequency Identification and Near- Field Communication, 3rd edition, John Wiley & Sons, Ltd., 2010, pp.- 179-188

[53] Bird Radio Tag. [Online]. Available: http://www.lotek.com/bird+batradio-beeper-tags.pdf

[54] The Smallest VHF Tag Commercially Available. [Online]. Available: http://www.biotrack.co.uk/update_pip.19.php

[55] M. Pedram, Q. Wu and Z. Wu, "A new design of double edge triggered flip-flops," Proc. Asia and South Pacific- Design Automation Conf., Feb.1998,

[56] G. C. White and R.A. Garrott, "Estimating Animal Locations," Analysis of wildlife radio-tracking data, London: Academic Press Limited, 2012.

[57] L. Goldberg, H. F. Taylor, J. F. Weller, and D. M. Bloom, "Microwave signal generation with injection-locked laser diodes," IET Electron. Lett., vol. 19, no. 13, pp. 491–493, Jun. 1983.

[58] M. Amourah and M. Whately, "A novel switched-capacitor-filter based low-area and fast-locking PLL," in Proc. IEEE Conf. Custom Integr. Circuit (CICC), Sep. 2015, pp. 1–6

[59] S. Bhowmik, S. N. Pradhan, and B. K. Bhattacharyya, "Clock jitter reduction and flat frequency generation in PLL using autogenerated control feedback," IEEE Trans. Compon. Packag. Manuf. Technol., vol. 7, no. 11, pp. 1832–1841, Nov. 2017.

[60] K. B. Unchwaniwala and M. F. Caggiano, "Electrical analysis of IC packaging with emphasis on different ball grid array packages," in Proc. 51st Electron. Compon. Technol. Conf., Orlando, FL, USA, 2001, pp. 1496–1501

[61] J. Li and S. M. R. Hasan, "Design and performance analysis of a 866-MHz low-power optimized CMOS LNA for UHF RFID," IEEE Trans. Ind. Electron., vol. 60, no. 5, pp. 1840–1849, May 2013.

[62] P. J. Sullivan, B. A. Xavier, and W. H. Ku, "An integrated CMOS distributed amplifier utilizing packaging inductance," IEEE Transactions on Micro-wave Theory and Techniques, Vol. 45, No.10, pp. 1969-1976, Oct. 1997.

[63] Jack Li and S. M. Rezaul Hasan, "Design and Performance Analysis of a 866 MHz Low-Power Optimized CMOS LNA for UHF RFID," IEEE Transactions On Industrial Electronics, vol. 60, no. 5, pp. 1840-1849, May 2013.

[64] Debendra Mallik and Bidyut K. Bhattacharyya, "HIGH-PERFORMANCE PQFP" 39th Electronic Components Conference, Houston, TX, USA, 1989

[65] AN-1205 Electrical Performance of Packages, [Online]. Available: https://www.ti.com/lit/an/snoa405a/snoa405a.pdf

[66] *Waikato Domestic Beekeepers Association. [Online]. Available: http://www.waikatobeekeepers.org.nz/bee-information/bee-facts/*

[67] A. J. Barker and E. L. Russell, "Multidimensional process corner derivation using surrogate based simultaneous yield analysis," U.S. Patent 7 716 023 B2, May 11, 2010.

[68] T. McConaghy, K. Breen, J. Dyck, and A. Gupta, 3-Sigma Verification and Design. New York, NY, USA: Springer, 2013. [Online]. Available: https://m.eet.com/media/1177441/variation-aware%20ch4a.pdf

[69] S. Paul *et al*., "A Sub-cm$^3$ Energy-Harvesting Stacked Wireless Sensor Node Featuring a Near-Threshold Voltage IA-32 Microcontroller in 14-nm Tri-Gate CMOS for Always-ON Always-Sensing Applications" *IEEE J. Solid-State Circuits*, vol. 52, no. 4, pp. 961–971, Apr. 2017.

[70] Product Features NTQB2s [Online]. Available: https://www.lotek.com/products/nanotags/

[71] Holohil Transmitters. [Online]. Available: https://www.holohil.com/ transmitters/lb-2x/

[72] Digital image processing-University of Cape Town. [online]. Available: http://www.dip.ee.uct.ac.za/~nicolls/lectures/eee482f/13_fsk_2up.pdf

[73] Mikhail Popovich and Eby G. Friedman, "Nanoscale On-Chip Decoupling Capacitors," IEEE International SOC Conference, Newport Beach, CA, USA, 17-20 Sept. 2008

[74] Mikhail Popovich, Eby G. Friedman , Michael Sotman, Avinoam Kolodny and Radu M. Secareanu "Maximum Effective Distance of On-Chip Decoupling

Capacitors in Power Distribution Grids," GLSVLSI '06: Proceedings of the 16th ACM Great Lakes symposium on VLSI, April 2006, Pages 173–179.

[75] TSMC Universal standard I/O Library General Application Note, Version 2.00, April 2008, pp.-69.

[76] Digital Oscilloscope¸ HMO3000 Series User Manual [online]. Available: https://cdn.rohde-schwarz.com/hameg-archive/HAMEG_MAN_EN_HMO3000.pdf

[77] Tektronix P2200 1x/10x passive probe manual. [online]. Available: http://www.mdc.umn.edu/facility/files/electrical/Elec%20Manuals/Tektronix%20P2200%20Passive%20Probe%20Manual.pdf

[78] System Level ESD: Design: On-Chip ESD Protection Strategies [online]. Available: https://www.industrial-electronics.com/controlstatic-net/S-L_ESD_1b.html

[79] N. Sturcken et al., "A Switched-Inductor Integrated Voltage Regulator With Nonlinear Feedback and Network-on-Chip Load in 45 nm SOI," in IEEE Journal of Solid-State Circuits, vol. 47, no. 8, pp. 1935-1945, Aug. 2012, doi: 10.1109/JSSC.2012.2196316.

[80] H. Le, M. Seeman, S. R. Sanders, V. Sathe, S. Naffziger and E. Alon, "A 32nm fully integrated reconfigurable switched-capacitor DC-DC converter delivering 0.55W/mm2 at 81% efficiency," 2010 IEEE International Solid-State Circuits Conference - (ISSCC), San Francisco, CA, USA, 2010, pp. 210-211, doi: 10.1109/ISSCC.2010.5433981.

[81] K. Kesarwani, R. Sangwan and J. T. Stauth, "4.5 A 2-phase resonant switched-capacitor converter delivering 4.3W at 0.6W/mm2 with 85% efficiency," 2014 IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC), San Francisco, CA, USA, 2014, pp. 86-87, doi: 10.1109/ISSCC.2014.6757349.

[82] V. Bucur, G. Banarie, S. Marinca and M. Bodea, "A Zener-Based Voltage Reference Design Compensated Using a ΔVBE Stack," 2018 25th International Conference "Mixed Design of Integrated Circuits and System" (MIXDES), Gdynia, Poland, 2018, pp. 116-120, doi: 10.23919/MIXDES.2018.8436687.

[83] A. Parisi, A. Finocchiaro, G. Papotto and G. Palmisano, "Nano-Power CMOS Voltage Reference for RF-Powered Systems," in IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 65, no. 10, pp. 1425-1429, Oct. 2018, doi: 10.1109/TCSII.2018.2857626.

[84] Everett Rogers, "Stability analysis of low-dropout linear regulators with a PMOS pass element," Texas Instruments Incorporated [online]. Available:

https://www.ti.com/lit/an/slyt194/slyt194.pdf?ts=1616772193728&ref_url=https%253A%252F%252Fwww.google.com%252F

[85] T. Coulot, E. Lauga-Larroze, J. Fournier, M. Alamir and F. Hasbani, "Stability Analysis and Design Procedure of Multiloop Linear LDO Regulators via State Matrix Decomposition," in IEEE Transactions on Power Electronics, vol. 28, no. 11, pp. 5352-5363, Nov. 2013, doi: 10.1109/TPEL.2013.2241456.

[86] Edgar Sánchez-Sinencio, Low Drop-Out (LDO) Linear Regulators: Design Considerations and Trends for High PowerSupply Rejection (PSR) [online]. Available: https://site.ieee.org/scv-sscs/files/2010/02/LDO-IEEE_SSCS_Chapter.pdf

[87] Behzad Razavi, Design of Analog CMOS Integrated Circuits, Indian Edition, McGraw Hill Education (India) Private Ltd., 2002, pp. 386-388.

[88] Alan Hasting, The Art of Analog Layout, 2nd Edition, New Jersey, Pearson Prentice Hall, 2006, pp. 277-283.

[89] S. Mandal, S. Arfin and R. Sarpeshkar, "Fast startup CMOS current references," 2006 IEEE International Symposium on Circuits and Systems, Kos, Greece, 2006, pp. 4 pp.-, doi: 10.1109/ISCAS.2006.1693217.

[90] R. Jacob Baker and Vishal Saxena, " High Speed Op-amp Design: Compensation and Topologies for Two and Three Stage Designs," [online]. Available: https://cmosedu.com/jbaker/papers/talks/Multistage_Opamp_Presentation.pdf

[91] S. Kabirpour and M. Jalali, "A Power-Delay and Area Efficient Voltage Level Shifter Based on a Reflected-Output Wilson Current Mirror Level Shifter," in IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 67, no. 2, pp. 250-254, Feb. 2020, doi: 10.1109/TCSII.2019.2914036.

[92] TPZN65GPGV2OD3 TSMC 65nm Standard I/O Library Databook, Version 200A, April 13, 2010

[93] TSMC Universal standard I/O Library General Application Note, Version 2.00, April 2008, pp. 11-15.

[94] Massimo Alioto, Enabling the Internet of Things from Integrated Circuits to Integrated Systems, Springer International Publishing, 2017, pp. 346-355

[95] Somnath Paul, Vinayak Honkote, Ryan Kim, Turbo Majumder, Paolo Aseron, Vaughn Grossnickle, Robert Sankman, Debendra Mallik, Sandeep Jain, Sriram Vangal, James Tschanz and Vivek De, "An energy harvesting wireless sensor node for IoT systems featuring a near-threshold voltage IA-32 microcontroller in

14nm tri-gate CMOS", Page 1-2, 2016 IEEE Symposium on VLSI Circuits (VLSI-Circuits).

[96] S. Lee, J. Jun and C. Kim, "A near-threshold all-digital PLL with a bootstrapped DCO using low-dropout regulator for mitigating PVT-variations," 2017 International SoC Design Conference (ISOCC), Seoul, Korea (South), 2017, pp. 180-181, doi: 10.1109/ISOCC.2017.8368869.

[97] Navid Paydavosi, et al., BSIM4v4.8.0 MOSFET Model -User's Manual, University of California, Berkeley, 2013, pp.86-93. [online]. Available: http://www.srware.com/xictools/docs/model_docs/bsim4.8.0/BSIM480_Manual.pdf

[98] Texas Instruments, REF33xx Voltage Reference. [online]. Available: https://www.ti.com/lit/ds/symlink/ref3333.pdf?ts=1611061052190&ref_url=https%253A%252F%252Fwww.ti.com%252Fpower-management%252Fvoltage-reference%252Fseries-voltage-reference%252Fproducts.html

[99] Kella Knack, Altium: Noise Margin Analysis Part 1 [online]. Available: https://resources.altium.com/p/noise-margin-analysis-part-1

[100] *Sony SR Micro Battery*, Accessed: 2019, [online] Available: https://www.sony.net/Products/MicroBattery/sr/spec.html.

[101] Martin Streinzer, Axel Brockmann, Narayanappa Nagaraja and Johannes Spaethe, "Sex and Caste-Specific Variation in Compound Eye Morphology of Five Honeybee Species" Plos One, 2017, https://doi.org/10.1371/journal.pone.0057702

[102] [online]. Available: https://www.orkin.com/stinging-pests/bees/honey-bees

[103] R. Zhu, S. P. Selvin, Y. Wang and N. Guo, "Frequency shift keying for direct antenna modulation (DAM) with electrically small antenna," 2017 IEEE International Symposium on Antennas and Propagation & USNC/URSI National Radio Science Meeting, San Diego, CA, USA, 2017, pp. 1203-1204, doi: 10.1109/APUSNCURSINRSM.2017.8072644.

# APPENDIX A

```
model npn bjt
   type=npn
  is=10e-13
bf=100 va=58.8
 ikf=5.63e-3
    rb=700
    rbm=86
    re=3.2
cje=0.352e-12
   pe=0.76
   me=0.34
 tf=249e-12
cjc=0.34e-12
   pc=0.55


model pnp bjt
   type=pnp
  is=10e-13
    bf=200
   va=58.8
 ikf=5.63e-3
    rb=700
    rbm=86
    re=3.2
cje=0.352e-12
   pe=0.76
   me=0.34
 tf=249e-12
cjc=0.34e-12
   pc=0.55
```

# APPENDIX B

Determination of the frequency and jitter from the measured data from a typical-typical chip operating at 25 $^{O}$C :

| Time | Time Period (s) | Frequency(MHz) |
|---|---|---|
| -0.001048526 | | |
| -0.001048514 | 1.27E-08 | 78.74015748 |
| -0.001048501 | 1.28E-08 | 78.125 |
| -0.001048488 | 1.3E-08 | 76.92307692 |
| -0.001048475 | 1.27E-08 | 78.74015748 |
| -0.001048462 | 1.28E-08 | 78.125 |
| -0.001048449 | 1.3E-08 | 76.92307692 |
| -0.001048437 | 1.27E-08 | 78.74015748 |
| -0.001048424 | 1.28E-08 | 78.125 |
| -0.001048411 | 1.3E-08 | 76.92307693 |
| -0.001048398 | 1.25E-08 | 80 |
| -0.001048386 | 1.27E-08 | 78.74015748 |
| -0.001048373 | 1.3E-08 | 76.92307693 |
| -0.00104836 | 1.28E-08 | 78.125 |
| -0.001048347 | 1.3E-08 | 76.92307692 |
| -0.001048334 | 1.27E-08 | 78.74015748 |
| -0.001048321 | 1.28E-08 | 78.125 |
| | | |
| | AVG_FREQ ($f_1$) | 78.059MHz |
| | STDDEV_FREQ ($f_1$) | 0.915086MHz |
| | | |
| | AVG_FREQ ($f_0$) | 156.118MHz |
| | STDDEV_FREQ ($f_0$) | 1.830172MHz |

Here, $f_o$ is the oscillator frequency and $f_1 = (f_o)/2$

# APPENDIX C

Measurement result from the test chips are listed below:

| Test Chip | VDD (V) | Pulse | Puse Record Time (s) | Time Period (s) | Frequency (MHz) | Burst Width (ms) |
|---|---|---|---|---|---|---|
| 1 | 1.4 | P1 | -2.16405487 | - | - | 12 |
| | | P2 | -0.59370536 | 1.57034951 | 170.9399432 | 12 |
| | | P3 | 0.9761714 | 1.56987676 | 170.9914197 | 12 |
| | | P4 | 2.5461389 | 1.5699675 | 170.9815369 | 12 |
| | | Mean | - | 1.57006459 | 170.9709666 | 12 |
| | 1.5 | P1 | -2.3002426 | - | - | 12.1 |
| | | P2 | -0.73039737 | 1.56984523 | 170.9948541 | 12 |
| | | P3 | 0.84287154 | 1.57326891 | 170.6227424 | 12 |
| | | P4 | 2.4141321 | 1.57126056 | 170.8408286 | 13.1 |
| | | Mean | - | 1.571458233 | 170.819475 | 12.3 |
| | 1.6 | P1 | -2.0840526 | - | - | 12 |
| | | P2 | -0.52013502 | 1.56391758 | 171.6429686 | 13.02 |
| | | P3 | 1.0439401 | 1.56407512 | 171.62568 | 12 |
| | | P4 | 2.6097967 | 1.5658566 | 171.4304209 | 13 |
| | | Mean | - | 1.564616433 | 171.5663023 | 12.505 |
| 2 | 1.4 | P1 | 0 | | | 13 |
| | | P2 | 1.618536 | 1.618536 | 165.8507787 | 13 |
| | | P3 | 3.2362249 | 1.6176889 | 165.9376262 | 12 |
| | | P4 | 4.849757 | 1.6135321 | 166.3651166 | 13 |
| | | Mean | - | 1.616585667 | 166.0511739 | 12.75 |
| | 1.5 | P1 | -2.2409371 | | | 12.1 |
| | | P2 | -0.62212902 | 1.61880808 | 165.8229035 | 13 |
| | | P3 | 0.99066257 | 1.61279159 | 166.4415028 | 13 |
| | | P4 | 2.6063163 | 1.61565373 | 166.1466507 | 12.1 |
| | | Mean | - | 1.615751133 | 166.137019 | 12.55 |
| | 1.6 | P1 | -2.2629374 | | | 12 |
| | | P2 | -0.6484727 | 1.6144647 | 166.2690154 | 12 |
| | | P3 | 0.96587172 | 1.61434442 | 166.2814036 | 12 |
| | | P4 | 2.5819237 | 1.61605198 | 166.1057066 | 13 |
| | | Mean | - | 1.6149537 | 166.2187085 | 12.25 |

| Test Chip | VDD (V) | Pulse | Puse Record Time (s) | Time Period (s) | Frequency (MHz) | Burst Width (ms) |
|---|---|---|---|---|---|---|
| 3 | 1.4 | P1 | -0.58563 | - | - | 14 |
| | | P2 | 1.3808 | 1.96643 | 136.5090321 | 13 |
| | | P3 | 3.3431 | 1.9623 | 136.796339 | 15.1 |
| | | Mean | | 1.964365 | 136.6526855 | 14.0333333 |
| | 1.5 | P1 | -2.4422549 | - | - | 15 |
| | | P2 | -0.47828569 | 1.96396921 | 136.6800735 | 15.04 |
| | | P3 | 1.4860409 | 1.96432659 | 136.6552066 | 13 |
| | | Mean | | 1.9641479 | 136.6676401 | 14.3466667 |
| | 1.6 | P1 | -0.66641 | - | - | 16.1 |
| | | P2 | 1.295 | 1.96141 | 136.858411 | 15 |
| | | P3 | 3.2553 | 1.9603 | 136.9359057 | 15.1 |
| | | Mean | - | 1.960855 | 136.8971474 | 15.4 |
| 4 | 1.4 | P1 | 2.3904158 | | | 11 |
| | | P2 | 3.864347 | 1.4739312 | 182.1221072 | 12 |
| | | P3 | 5.3367435 | 1.4723965 | 182.3119357 | 12 |
| | | P4 | 6.8097968 | 1.4730533 | 182.2306471 | 12 |
| | | Mean | - | 1.473127 | 182.2215301 | 11.75 |
| | 1.5 | P1 | -2.1344938 | - | - | 11 |
| | | P2 | -0.66050283 | 1.47399097 | 182.1147222 | 11 |
| | | P3 | 0.81338496 | 1.47388779 | 182.1274712 | 11 |
| | | P4 | 2.2880062 | 1.47462124 | 182.0368843 | 12 |
| | | Mean | - | 1.474166667 | 182.0930259 | 11.25 |
| | 1.6 | P1 | 0.35334332 | - | - | 12 |
| | | P2 | 1.8254806 | 1.47213728 | 182.3440379 | 12.1 |
| | | P3 | 3.2981536 | 1.472673 | 182.2777059 | 11 |
| | | P4 | 4.7677067 | 1.4695531 | 182.6646863 | 11 |
| | | Mean | - | 1.47145446 | 182.42881 | 11.525 |

# APPENDIX D

## List of Publications

- Meera Kumari and S. M. Rezaul Hasan, "A Low Duty-Cycle Burst Mode Telemeter Signal Generation Technique for VHF Insect Tracking and Its CMOS Implementation," *IEEE Transactions on Very Large-Scale Integration Systems*, available on-line, Oct. 2019. DOI: 10.1109/TVLSI.2019.2947696

- Meera Kumari, B. K. Bhattacharyya and S. M. Rezaul Hasan, "First Ever Lowest Duty Cycle for Periodic Burst Mode Signals for Insect Telemeter Package Design," *IEEE Transactions on Components, Packaging and Manufacturing Technology*, vol. 9, no. 10, pp. 2006 -2015, Aug. 2019. DOI: 10.1109/TCPMT.2019.2933830

- Meera Kumari and S. M. Rezaul Hasan, "A New CMOS Implementation for Miniaturized Active RFID Insect Tag and VHF Insect Tracking" *IEEE Journal of Radio Frequency Identification*, vol. 4, pp. 124-136, Jan. 2020, DOI: 10.1109/JRFID.2020.2964313

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|---|---|
| Name of candidate: | Meera Kumari |
| Name/title of Primary Supervisor: | Assoc. Prof. Rezaul Hasan |
| Name of Research Output and full reference: | |
| • Meera Kumari, B. K. Bhattacharyya and S. M. Rezaul Hasan, "First Ever Lowest Duty Cycle for Periodic Burst Mode Signals for Insect Telemeter Package Design," IEEE Transactions on Components, Packaging and Manufacturing Technology, vol. 9, | |
| In which Chapter is the Manuscript /Published work: | Chapter 3 and 5 |
| Please indicate: | |
| • The percentage of the manuscript/Published Work that was contributed by the candidate: | |
| and | |
| • Describe the contribution that the candidate has made to the Manuscript/Published Work: | |
| The research work was carried out by Meera Kumari under the supervision of principle supervisor (Assoc. Prof. Rezaul Hasan) | |
| For manuscripts intended for publication please indicate target journal: | |
| | |
| Candidate's Signature: | Meera Kumari Digitally signed by Meera Kumari Date: 2021.04.08 15:09:06 +12'00' |
| Date: | 08/04/2021 |
| Primary Supervisor's Signature: | Associate Professor Rezaul Hasan Digitally signed by Associate Professor Rezaul Hasan Date: 2021.04.08 15:42:52 +12'00' |
| Date: | 08/04/2021 |

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| Name/title of Primary Supervisor: | Assoc. Prof. Rezaul Hasan |
| Name of Research Output and full reference: | |
| • Meera Kumari and S. M. Rezaul Hasan, "A Low Duty-Cycle Burst Mode Telemeter Signal Generation Technique for VHF Insect Tracking and Its CMOS Implementation," IEEE Transactions on Very Large-Scale Integration Systems, | |
| In which Chapter is the Manuscript /Published work: | Chapter 4 |
| Please indicate: | |
| • The percentage of the manuscript/Published Work that was contributed by the candidate: | |
| and | |
| • Describe the contribution that the candidate has made to the Manuscript/Published Work: | |
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| Name of Research Output and full reference: | |
| • Meera Kumari and S. M. Rezaul Hasan, "A New CMOS Implementation for Miniaturized Active RFID Insect Tag and VHF Insect Tracking" IEEE Journal of Radio Frequency Identification, vol. 4, pp. 124-136, Jan. 2020 | |
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| Primary Supervisor's Signature: | Associate Professor Rezaul Hasan Digitally signed by Associate Professor Rezaul Hasan Date: 2021.04.08 15:43:44 +12'00' |
| Date: | 08/04/2021 |

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