The Design and Construction of an Electronically Beam Steered Phased Array Antenna.

A Thesis presented in partial fulfilment of the requirements for the degree of

Master of Science in Physics

at

Massey University
New Zealand

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1996

Abstract.

The design and construction of a simple beam steered phased array antenna was undertaken to demonstrate the operational principles behind such devices. The antenna can be used as a receiver or transmitter, however power requirements dictated that the antenna be tested as a receiver. The design is modular to allow for redevelopment without complete reconstruction. The array is made up of the control module, voltage controlled attenuators and a phase shifting unit. The antenna consists of 16 quarter wave monopoles arranged in a 4X4 square array on an aluminium ground plane. Practical considerations lead to a carrier frequency of 200 MHz.

The heart of a phased array antenna is the phase shifting device. This device controls the direction in which the main radiation lobe propagates. Several phase shifting principles were investigated but time did not allow for an exhaustive investigation of every kind of phase shifter. Initially, a relatively new and novel approach was attempted. When this proved to be unachievable a more traditional (but far less elegant) method was used.

During the phase shifting process, the signal necessarily suffers attenuation as well as the designed phase shift, consequently it is necessary to tailor the signal amplitudes of each array element. The required amplitude control is achieved through the use of 16 voltage controlled attenuators.

A computer package is used to control the phase shifter and attenuators. The design of this package depends on only three factors. The first is the interface between the hardware and the computer (via a serial port in this case). The second factor is the type of control signal the phase shifter and attenuators respond to (in this case a dc voltage). The third factor is the range of voltage required for the phase shifter and attenuators so that their full range can be utilised. This is realised through the use of a microprocessor, a "sample and hold" circuit and several D/A converters.

The antenna and computer control package are essentially independent of each other. If an 8 bit digital phase shifter were to be employed later, the hardware could be used to control this with minimal alteration. In this case the advantage of a modular design is apparent. Various parts of the device can be incrementally improved without alteration to the remaining system. Radical change can be accommodated with minimal adjustments.

Acknowledgements.

I wish to thank my supervisor, Assoc. Prof. Neil Pinder, for his advice, encouragement and interest. I would also like to thank Dr. Anthony Burrell for his assistance in chemistry. Thanks also to other staff who gave advice and interest. Finally, I would like to thank my parents and Donna for their help and encouragement. This work was made possible through the financial assistance of the Telecom Users Association of New Zealand.

Contents

Chapter 5.
Control Software.

Chapter 6
Hardware.

Chapter 7

Chapter 8

Chapter 9
Testing Methodology.

Chapter 10
Test Results.

Chapter 11
Conclusion.

Appendicies

Table of Figures and Tables

Chapter 1
Introduction.

1.1 Introduction to Phased Array Antennas.

A phased array antenna is a group of small radiating elements which, together combine to make a much more directive antenna. This sort of technology, when fully developed, will find many applications in telecommunications.

There are two direct impacts on telecommunications. The first relates to maritime satellite communications. The standard method to communicate VIA a satellite link is to have a dish shaped antenna mounted on a movable platform. To communicate, one orientates the antenna in the direction of a satellite (one that is oriented in your direction) and starts broadcasting. This works very well provided the satellite is not overhead and the sea is not too rough. When the sea is very rough the antenna can not respond to the ship's movement and the satellite link can be continually interrupted. This problem is exacerbated as the antenna points closer to vertical[1].

A phased array antenna offers two distinct advantages in this situation. First, an array of similar directivity to that of a dish can be lighter and have a much smaller moment of inertia. Hence any physical steering equipment can be built lighter and smaller (a consideration on pleasure cruisers etc.). The phased array can be oriented in the direction of a satellite by a combination of electronic and physical steering. This achieved, the antenna can maintain the satellite link in rough seas because the electronic steering can reorientate continually as the ship moves with the swell. Also, since the antenna is lighter it is much more stable when pointed close to the vertical (which is a major problem in dish antenna).

Phased array antennas are already used on satellites as they are smaller and lighter than conventional dish antennas. However these arrays radiate in a fixed direction and the satellite is moved when the antenna needs to be reoriented. This places an upper limit on satellite life time. When the fuel supply for the manoeuvring rockets is exhausted the satellite is no longer useful.

If the satellite could steer its antenna electronically then the required energy could be generated by the satellite solar panels, thereby extending the satellite life time. The only manoeuvring fuel expended will be in maintaining or changing the satellite orbit.

There have been attempts to manufacture cheap phased array antennas for the consumer market. These attempts have failed due to the considerable technical difficulties. One of the most famous failures concerned the 'squarial fiasco.' In 1988 BSB (British Satellite Broadcasting) unveiled its new household satellite television phased array receiver. The antenna (called the squarial) comprised an array of 250 microstrip elements backed by a flat reflector and connected to a converter. After spending considerable amounts of time and money the original design proved to be impossible to manufacture. In 1990 a British electronics company redesigned the squarial (see figure 1.1). This design failed to produce the promised perform-

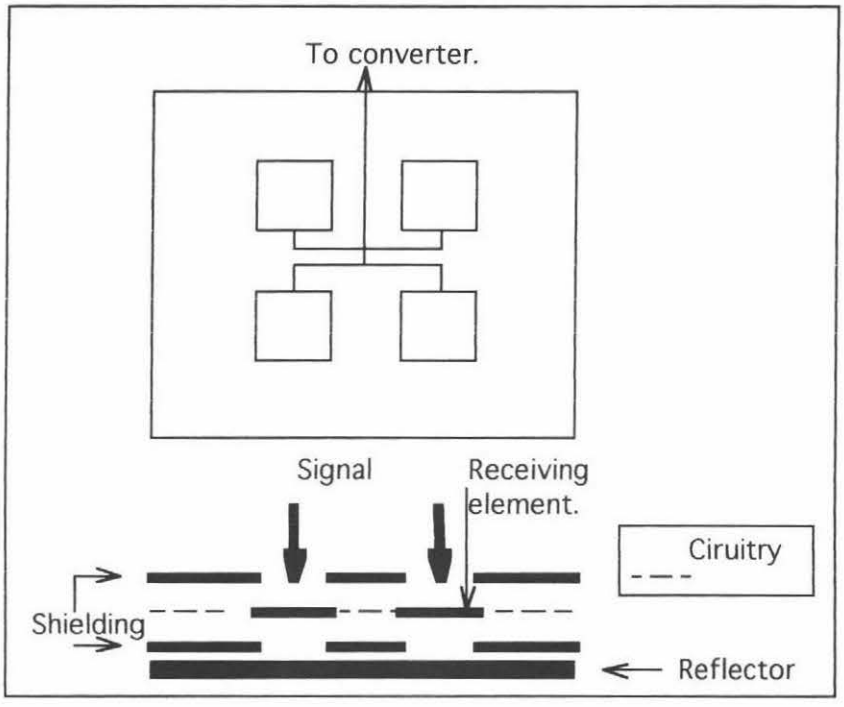

Figure 1.1. The proposed design of the "squarial". The elements are all connected VIA tracks in the printed circuit board. The length of the track must be the same for each element. The shielding is to prevent the tracks from detecting spurious signals either directly or from the reflector. This design is difficult to produce because of the accuracy required in the printed tracks.

ance. With a carrier frequency of 12 GHz even very small errors in production severely degraded the receiver performance. BSB had stopped supporting the "squarial" before the company went into receivership in 1992[14],[15]. The failure of BSB to design a successful mass produced phased array antenna demonstrates the difficulty in designing such devices.

Phased array antennas are used by the military in a variety ways. Every aircraft radar is made up of several small phased array antennas mounted on a moving platform (to provide the beam steering). On the ground, the phased array antenna

is used in observatories (see ref. 2) and early detection systems. These antenna occupy large areas and the controlling equipment is contained within multistory buildings.

The phased array antenna has proved to be an expensive luxury that only the military and the space industry can afford. The applications for a beam steered phased array antenna are numerous. The subject of current research is to produce an affordable and compact antenna for civilian purposes. A thorough understanding of the theory behind such devices is necessary before a phased array can be designed and built. The following describes the basic operational principals of an array antenna.

1.2. Elementary theory.

Consider two isotropic sources with an arbitrary relative phase, ψ, radiating at equal power. The radiation pattern (radiated power plotted as a function of angle) is not isotropic due to the mutual interaction of the sources. The path difference due to the unequal path lengths from each source to the point of interest plus the initial phase difference must sum to an integral number of wavelengths for a maximum to occur in the radiation pattern (see fig. 1.2 and equation 1.a). This implies that as the relative phase between the sources changes, the direction of the maximum in the radiation pattern changes also. The control system for a phased array antenna controls the phase of the elements and hence it controls the direction in which the antenna radiates maximum power.

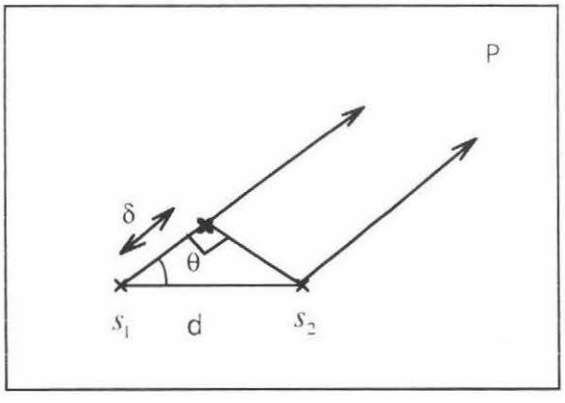

Figure 1.2. Two isotropic sources S_1 and S_2 radiating with an arbitrary phase difference will not produce an isotropic radiation pattern. The condition for a radiation maximum in the direction of P is that $2\pi\delta/\lambda$, the path difference in radians and ψ, the phase difference sum to an integral number of wave lengths. See equation 1.a.

$$2n\pi = \beta d\cos\theta + \psi \qquad \text{Equation 1.a}$$

Where n is an integer and the phase constant $\beta = \frac{2\pi}{\lambda}$

For developmental purposes such an array must be portable and, initially, operate at a frequency low enough for readily available electronics (the frequency can be increased after the circuitry has been optimised). The antenna can be no wider than a meter (approximately) as it must fit through doors. Spacings greater than $\lambda/4$ will make the array too large (or the frequency too high) as well as increasing the necessary phase shifts to steer the major radiation lobe. Closer spacing of the array elements reduces the necessary phase shifts but makes the array more sensitive to loss resistance[2].

Introducing a variable phase shift at high frequencies has always been a challenging problem. An elegant solution is to change the dielectric of a transmission line and hence introduce a change in the phase velocity. This has become achievable in recent years with the development of ceramics with variable permittivity[3]. Considerable time was spent trying to produce a usable ceramic. Since ceramic production was problematic a second phase shifter option was considered, the use of PIN diodes to impose the phase shift. PIN diodes have high insertion losses so they are not utilised in practical array antennas.

1.3. Coupling Between Antenna Elements.

The distance between the elements is of the order of a wavelength or less, thus the dominant fields are the induction fields. The induction field from each element effects the fields of the other elements (mutual impedance) and its own fields (self impedance). The self and mutual impedance of each element alters the phase and the amplitude of the signal of each element slightly. This distorts the radiation pattern. Mutual impedance can be made negligible by spacing the elements so far apart that coupling is negligible (not an option in this case). Mutual impedance can be reduced by adjusting the spacing between the elements to minimise the fields interacting with each element. This solution is not very useful because the minima of the induction fields would vary as the antenna is steered, furthermore the element spacing would not be regular making the control software and hardware more complex. Another solution is to calculate the effects of mutual and self impedance on each element and use the control software to compensate.

The impedance of an element is determined by the element's self impedance and the impedance due to other elements. The self impedance is determined by the ratio of the element input voltage and total current.

$$Z_{ii} = \frac{V_i}{I_i} \qquad \text{Equation 1.b.}$$

This is not very useful because the voltage along the element is unknown. An expression for the voltage is

$$dV_z = -E_z dz \qquad \text{Equation 1.c.}$$

where E_Z is the electric field in the z direction (see figure 1.3.). Using the rules of infinitesimals a new expression can be obtained

$$Z_{ii} = \frac{1}{I_i^2}\int E_i dz \qquad \text{Equation 1.d.}$$

The integral is over the length of a thin element. Now expressions for I and E_Z are needed. The current in the line feeding each element varies sinusoidally in time. The current at the end of the element will be zero (infinite impedance) but the feed current is not zero (by choice) hence the current along the element is sinusoidal.

$$I_z = I_i \sin(\beta z) \qquad \text{Equation 1.e.}$$

All that remains is to find an expression for the electric field in the z direction. E_Z can be shown to be (see ref. 2, pages 413-420)

$$E_z = -j30I_i\left(\frac{(e^{-j\beta r_1}}{r_1} + \frac{e^{-j\beta r_2}}{r_2}\right) \qquad \text{Equation 1.f.}$$

At the antenna $r_1 = z$ and $r_2 = L - z$ (see figure 1.3) so E_Z becomes

$$E_z = -j30I_i\left(\frac{(e^{-j\beta z}}{z} + \frac{e^{-j\beta(L-z)}}{L-z}\right) \qquad \text{Equation 1.g.}$$

From this expression and knowing the value of the radiation resistance of a centre fed, λ/2 dipole, the self impedance can be obtained

$$Z_{ii} = 73 + j42.5\Omega$$

The mutual impedance between two elements is defined as

$$Z_{ij} = \frac{V_{ij}}{I_i} \qquad \text{Equation 1.h.}$$

Using the same principles as in the case of self impedance, an expression for the mutual impedance can be obtained as

$$Z_{ij} = \frac{-1}{I_i} \int E_{ij} \sin(\beta z) dz \qquad \text{Equation 1.i.}$$

Of course E_{ij} is yet to be determined. For a more complete derivation of the expression for the mutual impedance see appendix 1.

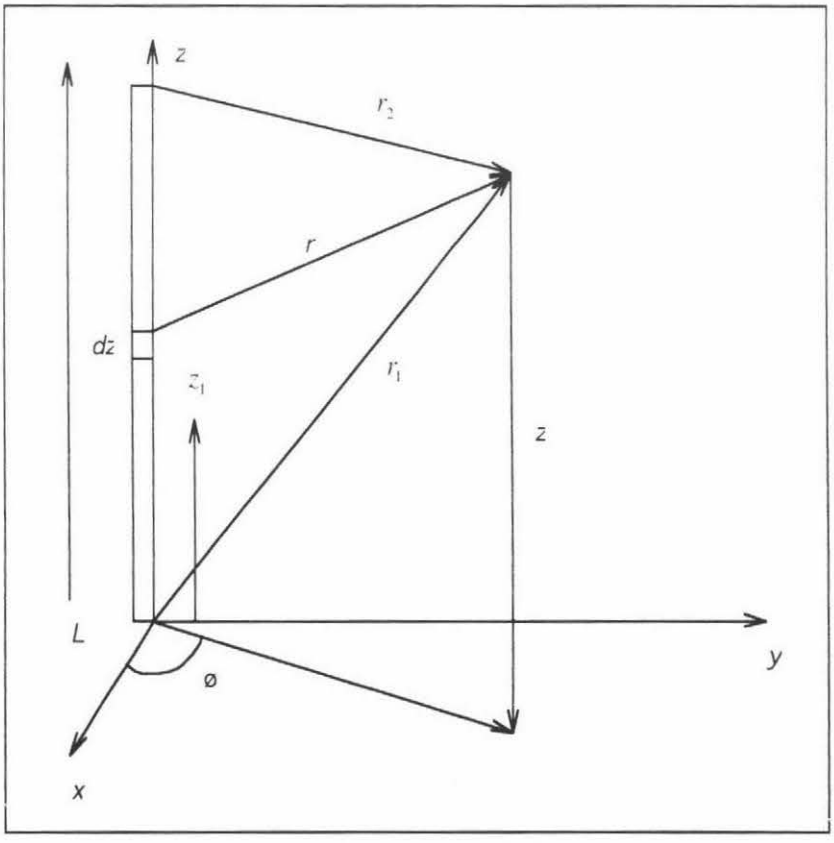

Figure 1.3. The coordinate system used for calculating the self and mutual impedances between two elements.

All the elements in the array are identical, hence, ignoring manufacturing differences, the self impedance of each element will be approximately the same. If the self impedance is the same for all elements then the phase and amplitude change will be the same for each element. Phase and amplitude differences between elements are important so the self impedance can be ignored. However the mutual impedance for each element pairing will be substantially different. The mutual impedance will depend upon the spacing of the pairs and the direction of the major radiation lobe. Mutual impedance is both resistive and reactive, meaning both phase and amplitude are effected. These changes must be calculated so that the phase and amplitude can be recalculated to counter these effects. The integral in equation 1.i is not a trivial one and must be solved for each of the 16 elements paired with every other element. However each element is parallel to every other element and an expression depending only on the distance between elements is available (provided half wave dipoles are used as elements).

$$R_{ij} = 30\left\{2Ci(\beta d) - Ci\beta\left[\sqrt{d^2+L^2}+L\right] - Ci\beta\left[\sqrt{d^2+L^2}-L\right]\right\} \qquad \text{Equation 1.j.}$$

$$R_{ij} = 30\left\{2Si(\beta d) - Si\beta\left[\sqrt{d^2+L^2}+L\right] - Si\beta\left[\sqrt{d^2+L^2}-L\right]\right\} \qquad \text{Equation 1.k.}$$

where† β is the phase constant (see equation 1.a), d is the distance separating elements and

$$Z_{ij} = R_{ij} + jX_{ij}$$

These equations represent the mutual impedance between a pair of elements. The total mutual impedance for a single element is a sum over the elements.

$$Z_i = R_i + jX_i + \sum_{j\neq i}^{j=n}(R_{ij} + jX_{ij}) \qquad \text{Equation 1.l.}$$

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† Here Si and Ci are the modified sine and cosine integrals $Ci(x) = \int_0^x \frac{\cos v}{v}dv \quad Si(x) = \int_0^x \frac{\sin v}{v}dv$

Thus the phase change introduced by the mutual coupling between paired elements is

$$\tau = \arctan\left(\frac{X_i}{R_i}\right)$$ Equation 1.m.

The total phase shift (relative to a reference element) is simply

$$\psi = \tau + \delta$$ Equation 1.n.

Where δ is the phase shift imposed by the phase shifting device.

Mutual coupling also introduces amplitude variations. These are directly proportional to the magnitude of the mutual impedance since

$$Z_i = I_i Z_i$$ Equation 1.o.

Thus the relative amplitudes can be calculated from the relative mutual impedances. The phase shifter will also introduce amplitude changes. Differences in amplitude between elements will effect the direction the main lobe radiates as well as effecting the size of the main lobe and side lobes. Amplitude control can be used to control side lobe levels or produce a very narrow main lobe (at the expense of side lobe control).

Chapter 2
Methods of Phase Shifting.

Methods for adjusting the phase of high frequency radiation are summarised in the following paragraphs. Not all of the methods described are applicable to the particular array constructed here but these methods are representative of the different approaches which have been explored.

2.1. Jindalee B Phased Array Antenna.

The Jindalee stage B array[5] is a wide bandwidth (6-25 MHz) RADAR antenna commissioned by the US Navy in Australia. The antenna is a wide band transmitting and receiving array. The initial phase adjustments are produced by changing the path lengths between the antenna elements. The path length differences are introduced by switching cables on a rack of coaxial cable at each antenna element. This is a 10 bit phase shifter but it is inconvenient to do all the phase shifting this way because the maximum cable length becomes excessive (~100m)[5]. Once the time delay is set then phase shifting devices are used to further refine the direction of the main lobe. Phase shifters are used as secondary devices as the necessary phase shift is not frequency independent thus effecting the bandwidth of the array. No details are given concerning the phase shifter.

2.2 Digital Phase Shifters.

The Australia Telescope Compact Array is a receiving array for astronomical purposes[6]. In this array, steering is achieved by correlating the data in a digital manner. The signal at the elements is digitised and sent to the central control unit as serial data at 512Mbitss^{-1}. At the central control unit the data are stripped of the clock signals introduced by each element using Manchester decoding.[6] The start of each integration period is marked by a bit sequence relative to which all phase adjustments are made.

From the decoder the data are sent into a 32 bit shift register. Aside from being a serial to parallel converter, the shift register can be used to introduce very small delays to the signal by loading the register on different clock pulses. If two registers load one clock pulse apart then the data from the second shift register are delayed by one word (2ns). The maximum delay from this is one integration cycle which is 64 ns.

The data are now synchronised by sending them into a First In First Out register (FIFO) (See fig. 2.1). The data need to be synchronised because each element has its own clock and the clocks operate at slightly different rates. Loading of the

registers can be delayed by a varying number of words. This is, in effect, throwing away data until they are synchronised. Each FIFO's unloading is triggered by a common clock so the data are delayed by the time they have spent in the FIFO. The minimum delay is one word-time (64 ns). The maximum delay time is determined by the length of the FIFO, in this case 64 μs[6].

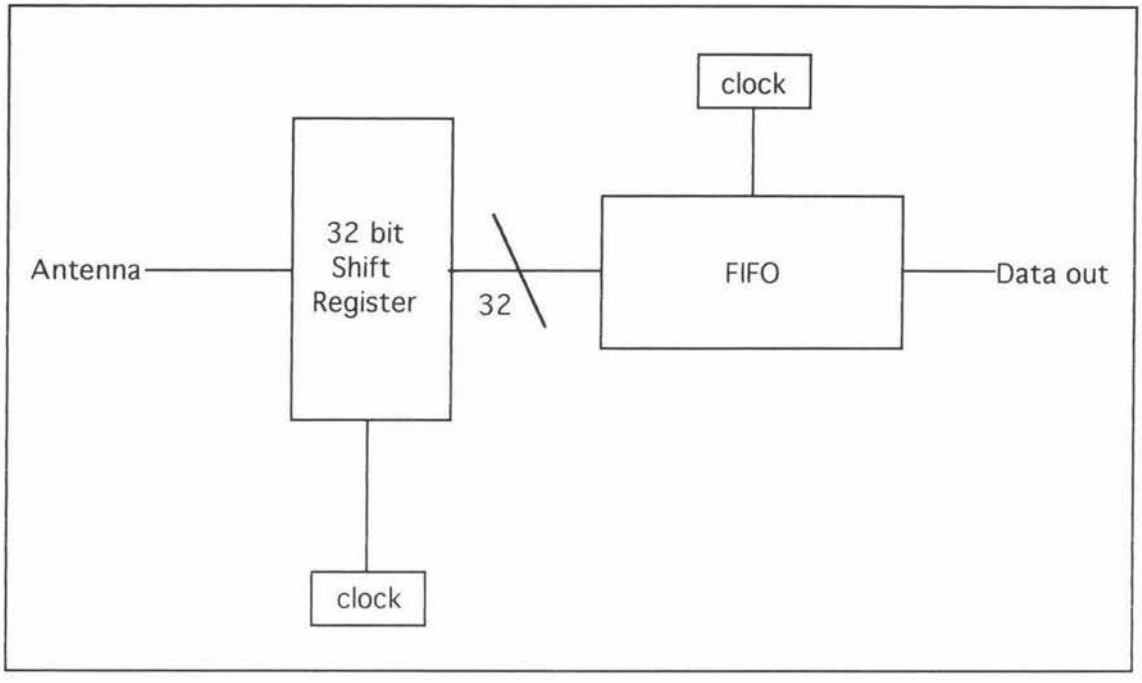

Figure 2.1. This digital phase shifter delays the data by causing the shift register and FIFO to ignore some clock pulses. The minimum delay is one clock pulse between shift registers (2ns). At 200 MHz this would be a phase step of approximately 150° which is too coarse.

2.3. Phase Locked Loop Phase Shifters.

Phased Locked Loops (PLL) have an intrinsic phase error introduced by the amplifier offset (see fig 2.2a). This phase error can be increased by adding to the amplifier offset (see fig 2.2b) [7]. The amplifier output controls a VCO, trying to keep its phase locked to the incoming signal. An added voltage upsets this, forcing the needed 'phase error' to occur. For an antenna operating at frequencies lower than 500MHz this is an ideal phase shifting mechanism. This option was unsuitable as the intention was to build a phase shifter that could be extended to higher frequencies. The PLL has to perform at the operating frequency of the antenna, which is normally too high for present day electronics, or cascaded networks of PLL's must be used, which is a very complex process and propagates the inherent phase noise in each PLL.

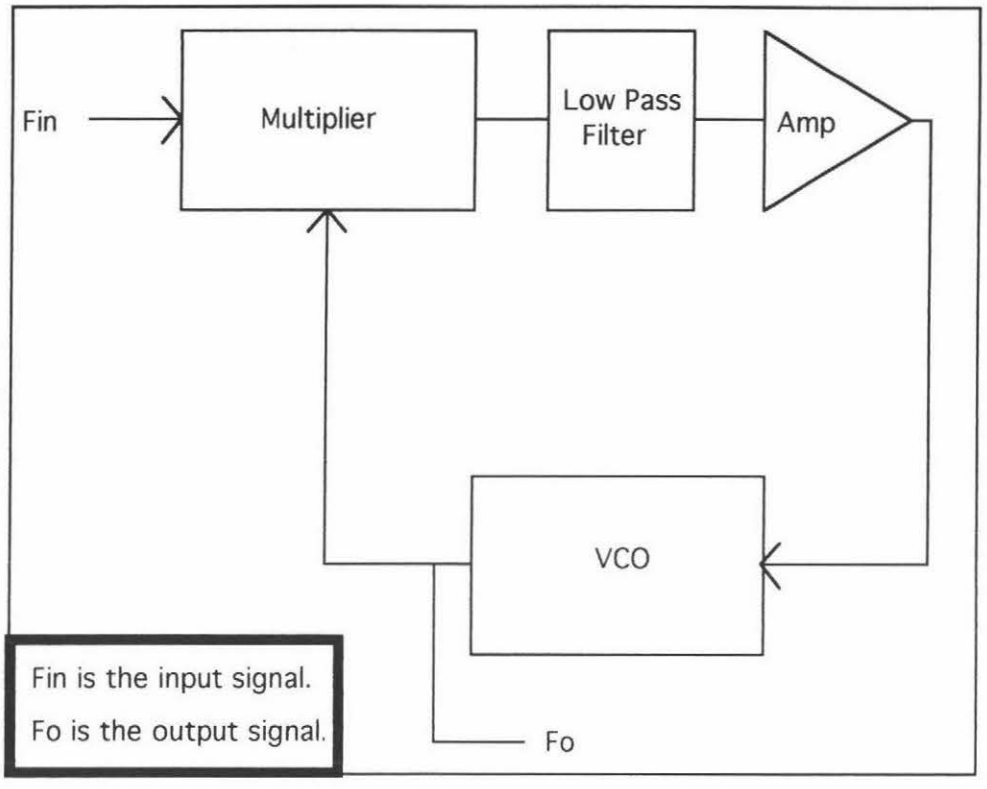

Figure 2.2a. A schematic diagram of a phased locked loop.

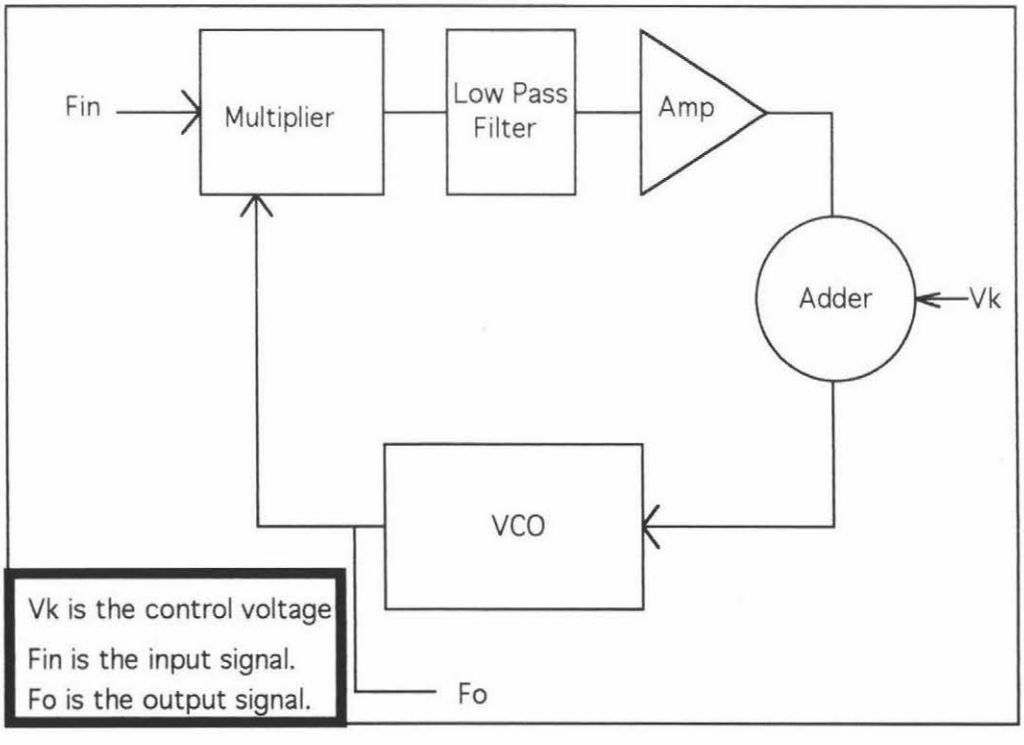

Figure 2.2b. A phase locked loop with an external voltage added. This forces the VCO to operate at a non zero relative phase to the input.

A second method employs a phase detector instead of a multiplier (see fig 2.2c). Here the output of the PLL is phase shifted using the method described above, however, it is then used to modulate an rf signal. The signal is sent through a single side band filter and the resulting output is phase shifted by the same amount as the PLL output [8]. The advantage of this system over the previous arrangement is that the PLL operates at a lower frequency than the antenna (for example see ref. 8) so the available electronics are adequate. Using a PLL as a phase shifter has two advantages. First, the phase shift is linearly related to the applied voltage. Secondly, the PLL is a reliable much used device with well known properties that are stable against temperature and humidity variation.

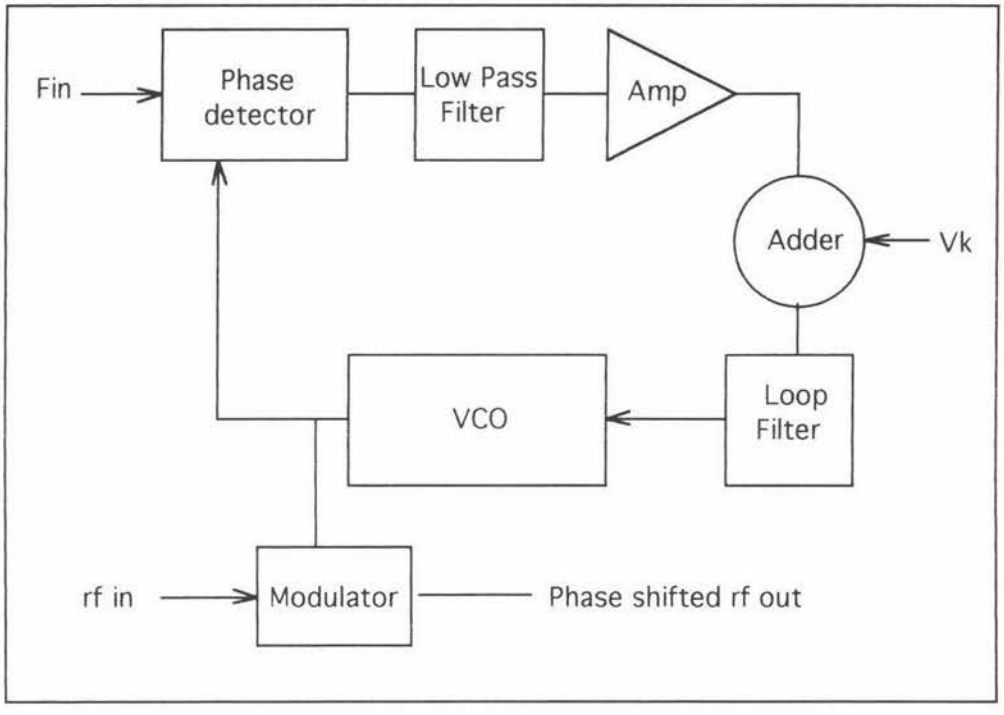

Figure 2.2c. The phased locked loop is used to modulate a higher frequency signal. The modulated signal is phase shifted by the same amount as the PLL signal.

2.4. Distributed Amplifier Phase Shifter.

The development of GaAs technology has produced amplifiers with very large bandwidths. This in turn has led to new possibilities in phase shifting technology, in particular the distributed amplifier phase shifter[9]. Two artificial transmission lines are produced from lumped capacitors and inductors, the lines are periodically coupled through a GaAs amplifier (MESFET). (See figures 2.3a and b). The gate - source capacitance forms a shunt capacitor for one line while the drain - source

impedance effects the second line. This is a well known arrangement and in forward gain mode it provides large, constant gain over a large frequency range because the different paths through the transmission line are all the same length[9].

There is a second gain mode, known as reverse gain, that is not normally used because it has low gain (usually less than unity). In this mode the path lengths differ, hence a relative phase shift is introduced. This phase shift is given by[9]

$$\beta = \sin\left(\frac{f}{f_c}\right)$$

Where f is the operating frequency of the transmission line and f_c is the amplifier upper cutoff frequency. This system can be used as a digital or analogue phase shifter. Digital operation is quite simple. One of the MESFETs can be switched on by applying the appropriate voltage to the gate (pushing the MESFET into the pinch off region) hence phase shifts of ß,2ß,4ß... can be achieved[9]. Analogue operation is a little more complex, two MESFETs are biased into the pinch off region to achieve a phase shift. To vary the phase continuously one simply varies the bias between the two MESFET's differentially. As the phase shift between the two increases the magnitude of the output decreases to an unsatisfactory level. This is obviated by coupling a third MESFET between the gate of the first and the drain of the second[9] (see figure 2.3c.). Most of this technology is still in the simulation stage, however, some 4 bit phase shifters have being constructed. The phase shifters constructed have used 16 MESFETs to produce a 4 bit phase shifter with low noise and minimal insertion losses[13].

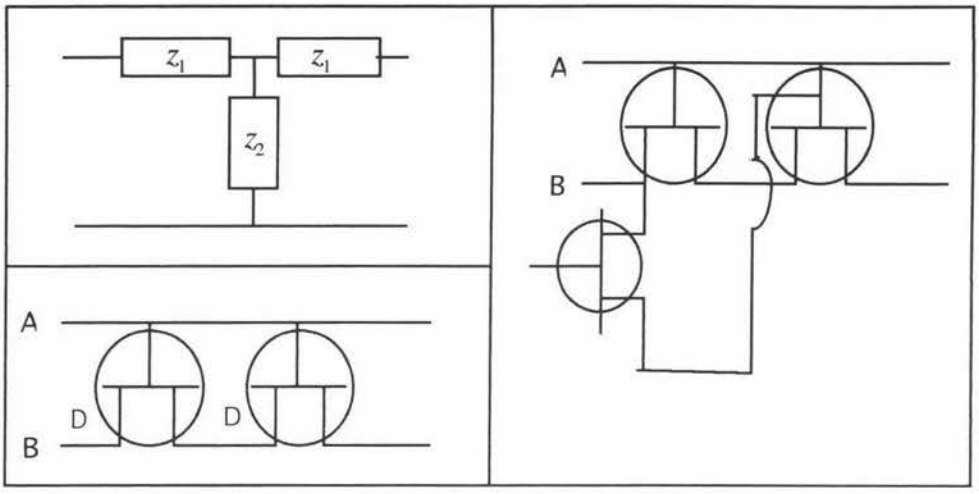

Figure 2.3a. (Top left) An artificial transmission line consisting of shunt capacitors and serial inductors.
Figure 2.3b. (Bottom left) A distributed amplifier phase shifter consisting of two artificial transmission lines, A and B, coupled through two MESFET amplifiers. This system will phase shift but it has a gain much less than unity.
Figure 2.3c. (Top right) A distributed amplifier phase shifter with gain greater than unity.

2.5. R - C Circuit Phase Shifters.

It is well known that a passive resistor - capacitor (R-C) network will phase shift a signal depending on the signal frequency, and the network impedance. Variable capacitors (PIN diodes) were tried as phase shifters but interest waned after it was discovered that the PIN diode suffered disappointingly large insertion losses[3]. Since then PIN diodes have been improved and are now used to tune television receivers.

This type of circuit is lossy by its very nature because the R-C network is a voltage divider. The impedance of the PIN diode changes with changing capacitance and hence produces a phase shift (see figure 2.4a). At the same time the change in capacitance effects the relative amplitude (figure 2.4b). The optimum phase shift occurs when the attenuation is most severe This limits the maximum phase shift of any single phase shifter to about 60°. However, the idea is simple and therefore an attractive option for a demonstration model. An R-C phase shifter is simply a cascaded network of high pass filters (see fig 2.5).

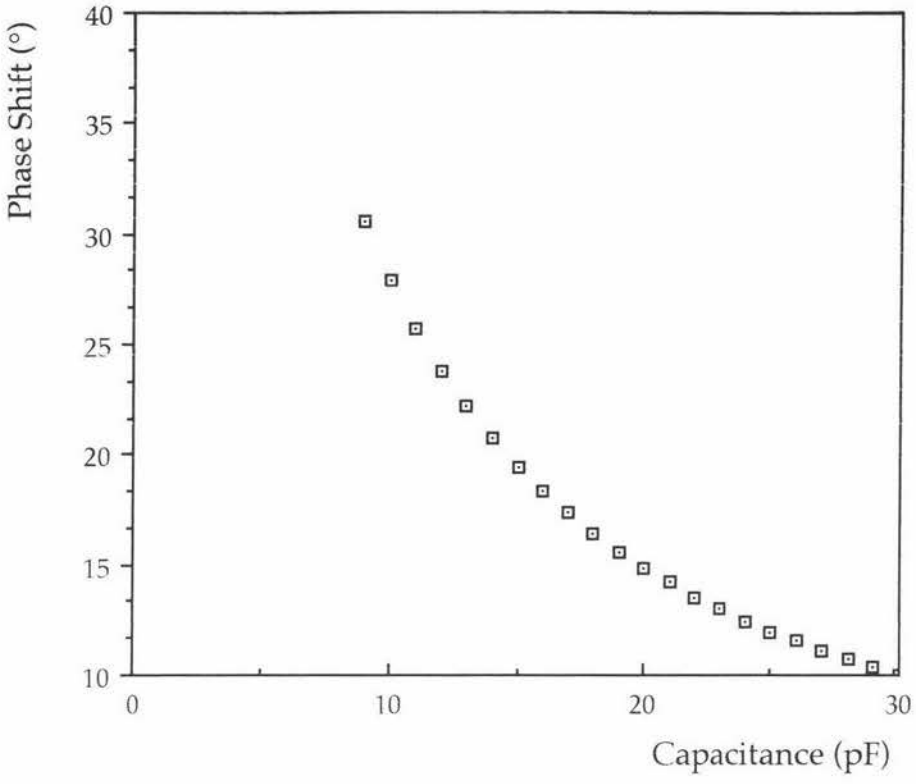

Figure 2.4a. The calculated phase shift for a simple R - C network is shown here. As stated before the phase shift is not linear with changing capacitance.

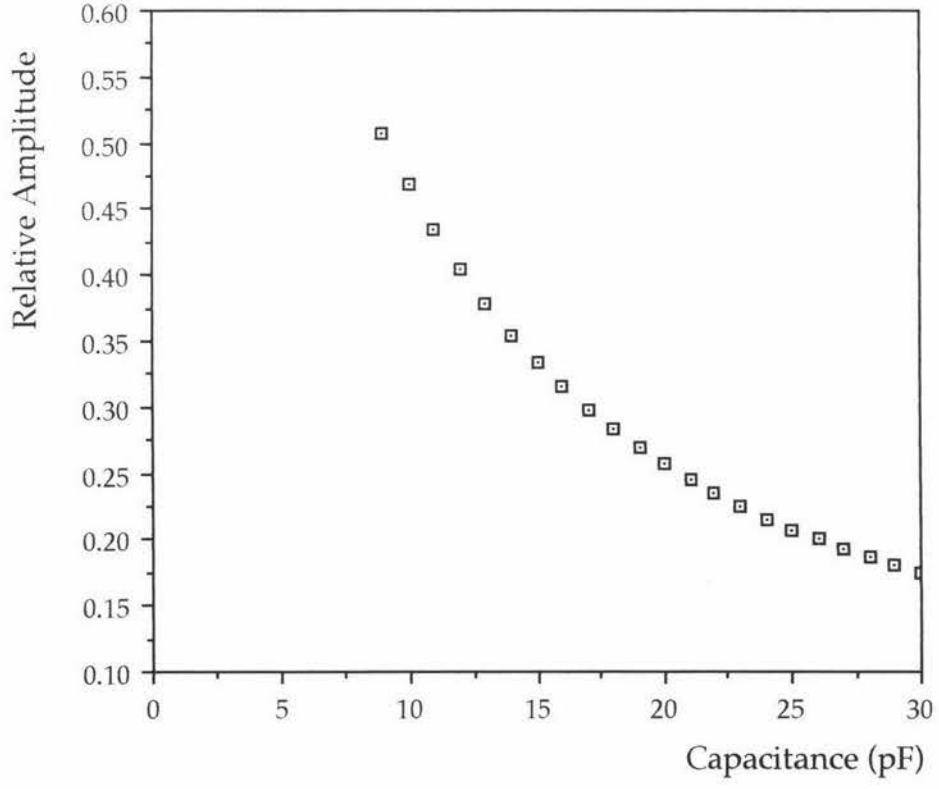

Figure 2.4b. The calculated relative amplitude from the output of a simple R - C network. Imposing a phase shift severely attenuates the signal.

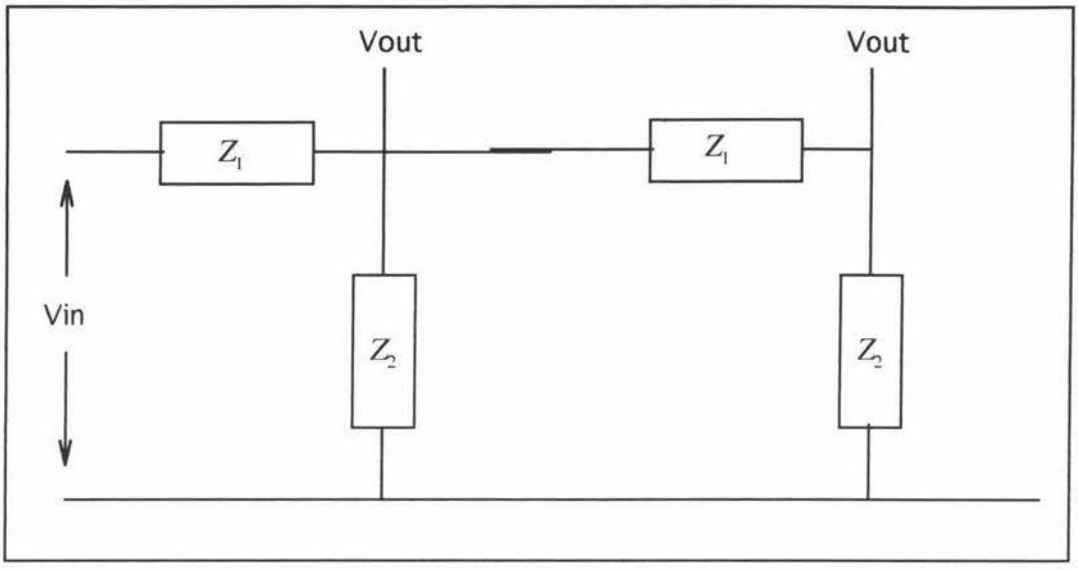

Figure 2.5. A cascaded network of impedances can be used as a phase shifting device. The simplest method is to replace Z_1 with a resistor and Z_2 with a variable capacitor. The phase between adjacent outputs will vary in a nonlinear fashion with respect to the capacitor. The amplitude of the signal will vary with the applied phase shift as well.

2.6. Wave Guide Phase Shifter.

This is a variant of the transmission line phase shifter in that the line capacitance is varied by changing the permittivity of a dielectric. Recent advances in ferroelectric materials have offered an alternative approach to rf phase shifting. Certain barium strontium titanium oxide ceramics (BST) have a permittivity that varies with an applied dc electric field. As the permittivity changes so does the phase of the signal. This is an apparently simple solution to the problem. All one need do is fill a wave guide with the ceramic, match the input and output of the wave guide and apply a dc electric field[3], [10], [11] (see figure 2.6). BST is not yet commercially available, but it is relatively easy to synthesise BST in the powder form.

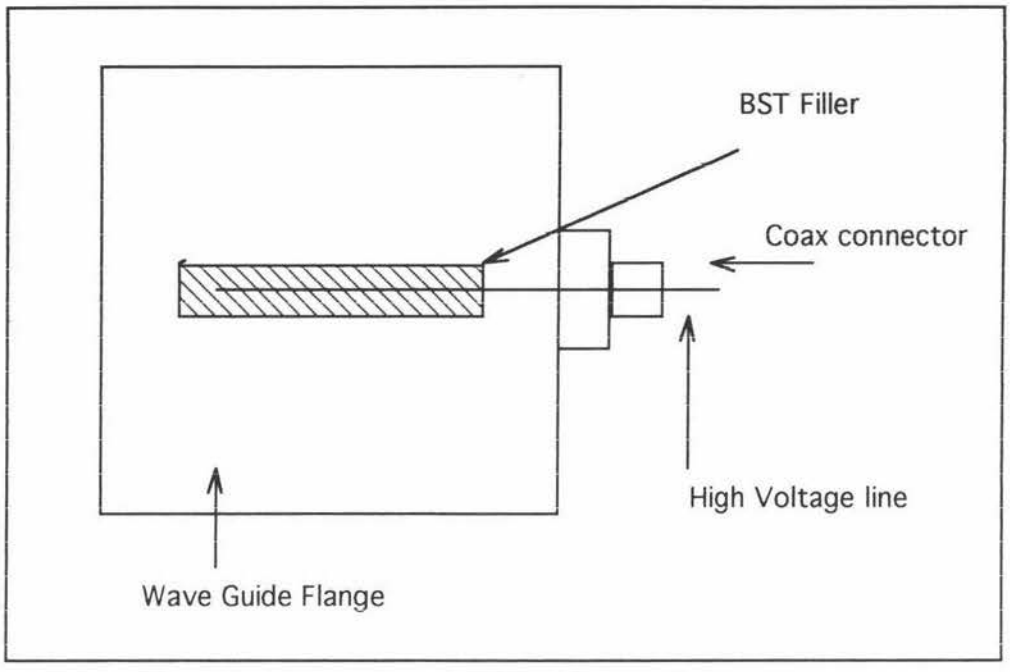

Figure 2.6. View of ceramic filled Ku band wave guide, looking down the guide. The dc voltage across the dielectric can be varied to phase shift the signal as it passes through the guide. To obtain the optimum performance the wave guide is tapered until the shown aspect ratio is attained. This wave guide must be matched at the input and the output.

Chapter 3
The Phase Shifter.

3.1. Design of a Phase Shifter.

As stated in the introduction, the phase shifter determines the direction of propagation of the antennas major radiation lobe. This makes the design of a phase shifting device top priority. Chapter 2 gave an overview of some phase shifters currently in use or under development. As no single method stands out it was decided to pursue a two pronged attack. Viz. construction of a ceramic phase shifter would be attempted and If this method failed PIN diodes would be used as it is well known that PIN diode phase shifter can be produced although they do not have ideal practical characteristics.

BST is a ceramic that changes its permittivity when a transverse (to the direction of propagation) electric field is applied. This in turn introduces a phase change to the radiation. The constant phase point of a wave is given by

$$f\lambda = \frac{1}{\sqrt{\mu\varepsilon}} \qquad \text{Equation 3.a.}$$

where f is the frequency of the radiation, λ is the wavelength, μ is the magnetic permeability and ε is the permittivity. At a given frequency the wavelength of an electromagnetic wave is inversely proportional to the square root of the permittivity of the medium. A change in permittivity by a factor of 4 is sufficient to double the phase speed and so introduce a 360 degree phase change over one wavelength.

The operating frequency was chosen to be 200 MHz, high enough to be challenging and low enough for easy amplification. At 200 MHz half wave dipoles are of manageable length (75 cm). If the frequency is 200 MHz a ceramic filled wave guide is not practical as the dimensions of the wave guide would be too large. Coaxial cable could be employed but the length of cable necessary would be too long. A more subtle approach would be to create an artificial transmission line.

A transmission line (see Fig 3.1a) always has some inductance distributed along its length (inductance per meter) and capacitance between the transmission line and ground (capacitance per meter). An artificial transmission line is a block of capacitors and inductors (Fig 3.1b). The value of the inductance and capacitance

determines the optical length of the transmission line. If variable capacitors are used then the optical length can be varied and hence a path difference between two transmission lines can be introduced. Several artificial transmission lines contain-

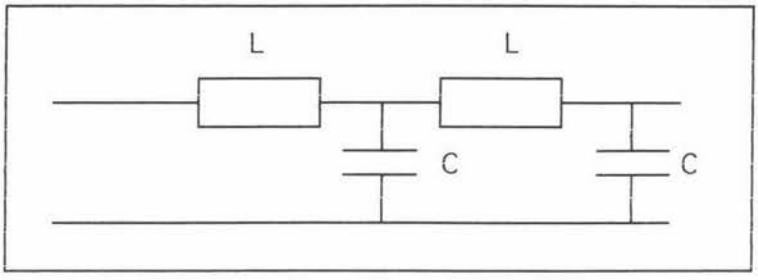

Figure 3.1a. A real transmission line has serial inductance and shunt capacitance along its length. The Phase speed is given by $v = \frac{1}{\sqrt{LC}}$.

ing variable capacitors can be used to make a phase shifter (see figure 3.2).

A variable capacitor can be produced by separating two metal plates with a disk of BST. BST materials have been shown to change their permittivity as much as 50%. This can be equated to a 30° phase change in a simple R-C circuit.

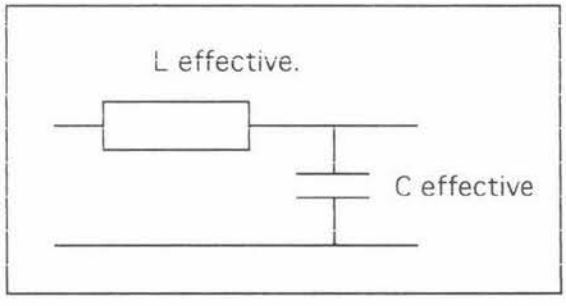

Figure 3.1b. An artificial transmission line can be manufactured by using a large block capacitor and an inductor. By changing C or L the phase speed of the transmission line is varied. This variation can be used to introduce time delays between transmission lines.

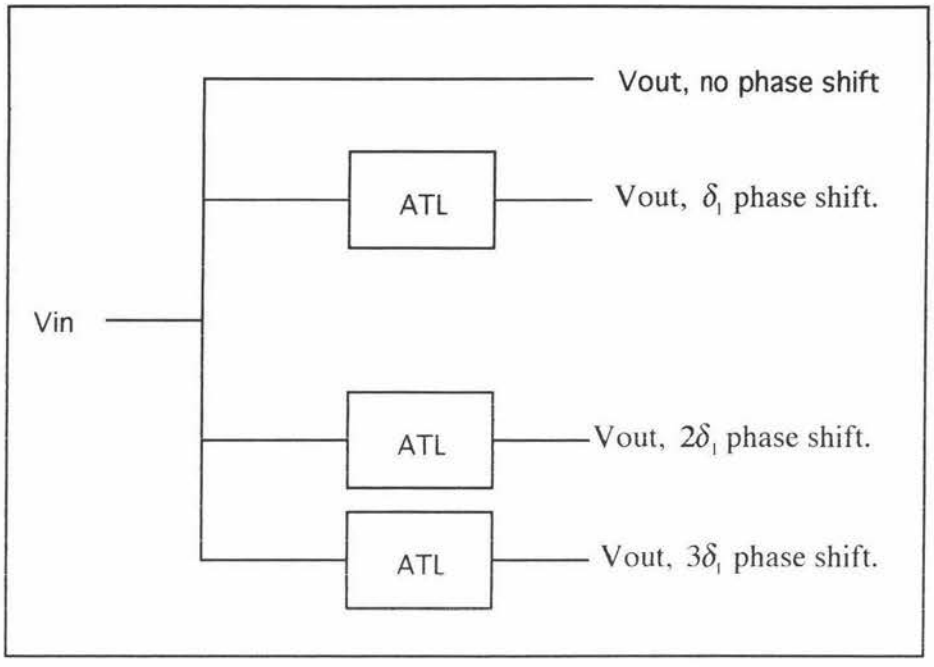

Figure 3.2. Artificial transmission lines (ATL) are used to introduce path differences to different elements of the antenna.

3.2. Producing a BST Phase Shifter.

To make BST filled capacitors Barium Carbonate, Strontium Carbonate and Titanium Oxide powders must be mixed in the correct ratio. There are several methods available. One such method is to mix the powders in the desired ratio. The powder is then calcined at an extremely high temperature (>1200°C), milled until the powder is fine and finally sintered to form the ceramic. This method of BST production has two delicate steps. First, the calcined product has a large grain size and must be milled for long periods of time before a small (~1 μm) grain sized is attained. second, during the milling process impurities are introduced (because the mill itself wears away and powders previously used in the mill may be present)[12].

In view of the high calcination temperature and problems with the grain size, a wet chemical route was chosen. The wet chemical route is outlined in the schematic diagram (figure 3.3). The lower calcination temperature (<800°C) is not the only advantage of the wet chemical route. After calcination the powder is very fine (~.1μm) and no milling is necessary. The purity of the powder is increased (provided glassware is cleaned properly). However, the very fine powder is 'fluffy', and so difficult to put into molds for pressing and sintering. Also, the required relative abundance of 65% barium complex to 35% Strontium complex (by mass)

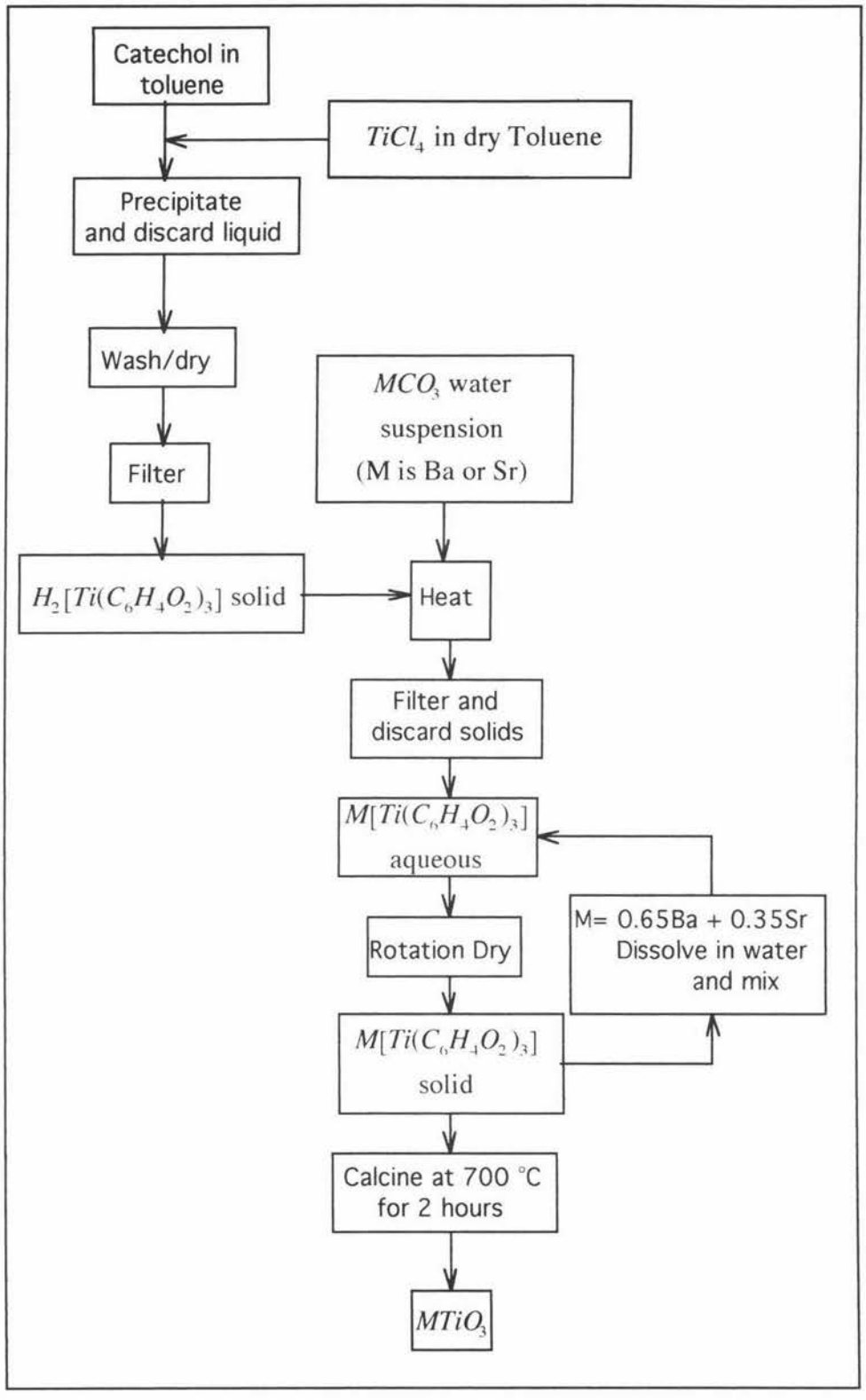

Figure 3.3. Flow diagram of the procedure for the preparation of BST powder by a wet chemical route[12].

can only be approximated because each complex contains an unknown quantity of water which cannot be taken into account during the weighing and mixing process. See appendix 2 for details on production of the powder. The exact composition can be determined after calcination by any of a number of standard procedures (ie mass spectroscopy)†.

The final step in the synthesis of a BST filled capacitor is pressing and sintering the BST powder. The ceramic must be sintered at 1200°C for approximately 4 hours at a pressure of 20 MPa. The ceramic can be produced at atmospheric pressure but the low pressure promotes the growth of large grains within the ceramic. Large grains are undesirable because they decrease the sensitivity of the permittivity value to applied voltage[12].

An iron - constantan thermocouple was used to monitor the temperature during the process. The calibration chart for the thermocouple is below (fig 3.4).

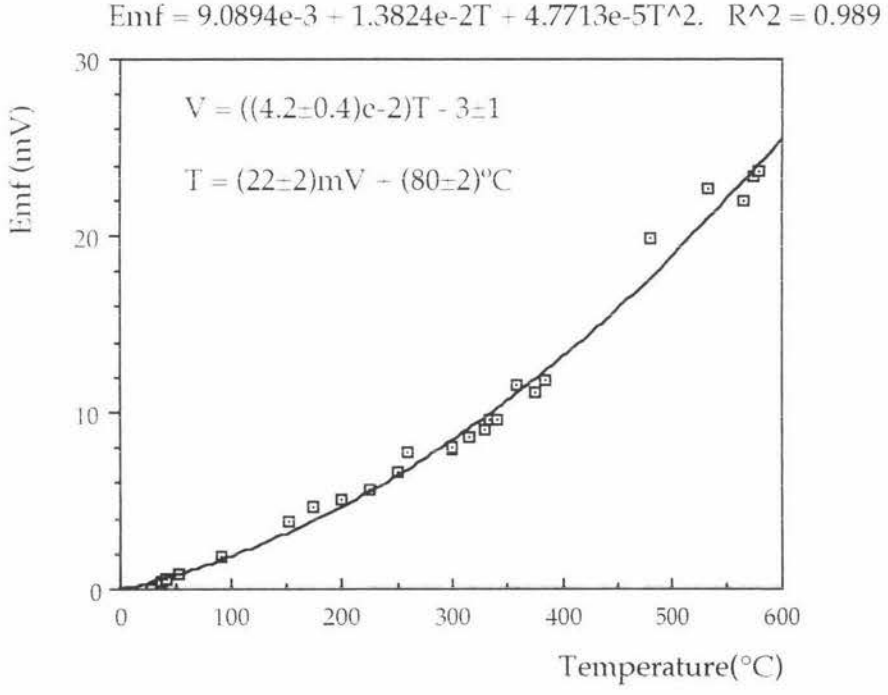

Figure 3.4. Calibration curve for the thermocouple. Higher temperature calibration was achieved by heating the bead of a known thermocouple and the new thermocouple over a bunsen flame.

Taken individually the requirement for 1200°C for 4 hours and 20 MPa pressure are not difficult to achieve. An acetylene torch can produce a flame at 3300°C and a G-Clamp can be made to produce 20 MPa on a small area. Stainless steel with a

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† The author wishes to thank Dr M. Daglish and Dr A.K. Burrell for their assistance.

large current passing through it will reach a temperature of 1600°C before melting. The steel heating element would only be needed to heat a small volume to 1200°C. With this in mind a hot press was designed (see Fig 3.5).

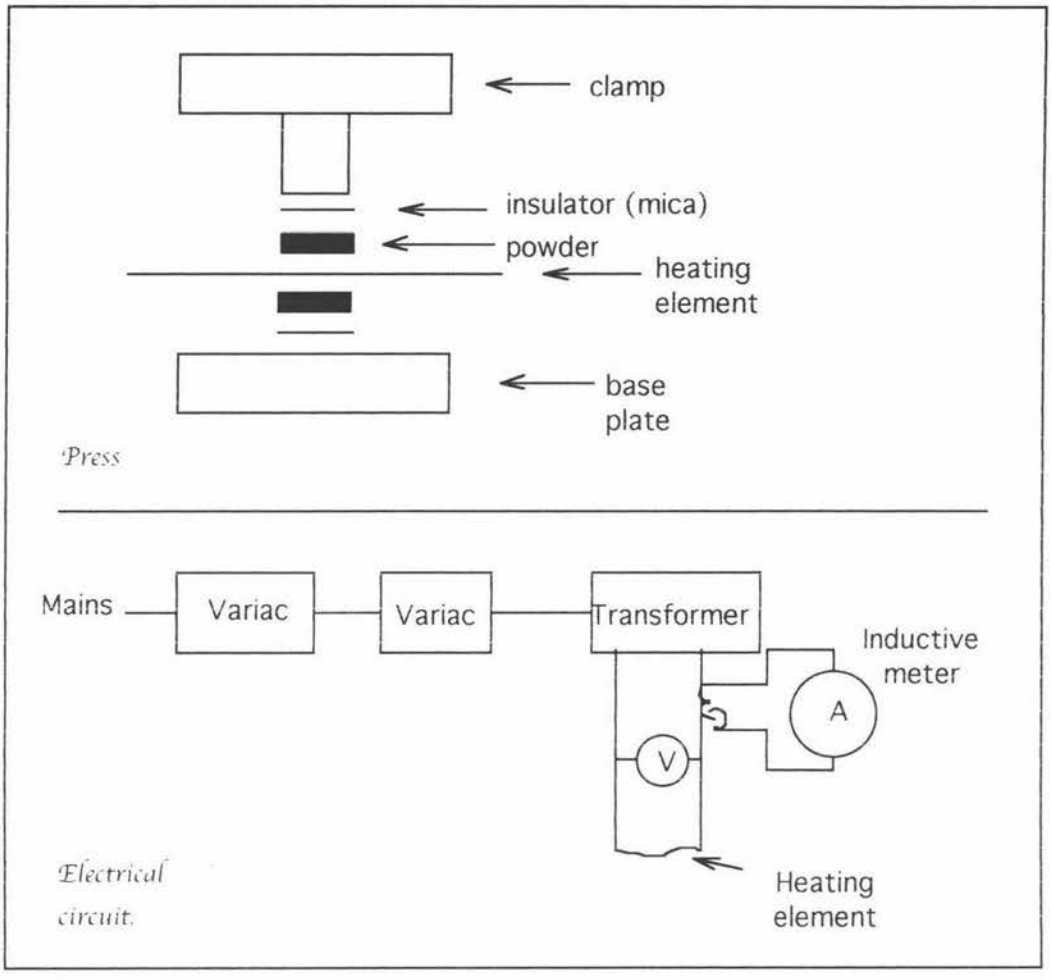


Figure 3.5. Hot press Mk. 1. The base plate and clamp were attached VIA 4 bolts which could easily apply 20 MPa of pressure. Expansion due to high temperature was not expected to be a problem as the extremities of the hot press were not expected to get very hot.

In the first attempt the hot press was found to have several disadvantages. First, the heat losses were so great that equilibrium was established at about 600°C (see fig 3.6). The press had no container for the powder to be pressed into so any ceramic produced would have been very "ragged" around the edges. The surface of the heating element did reach the required temperature and a thin layer of ceramic was sintered in such a way as to adhere to the surface of the heating element. The second attempt (figure 3.7) used a fire brick to limit heat losses. The

heating element was continuously operating for 6 hours before the it melted. The ceramic reached a temperature of approximately 1000°C (see fig 3.8). The sample was allowed to cool for 4 hours before examination. No sintering had occurred.

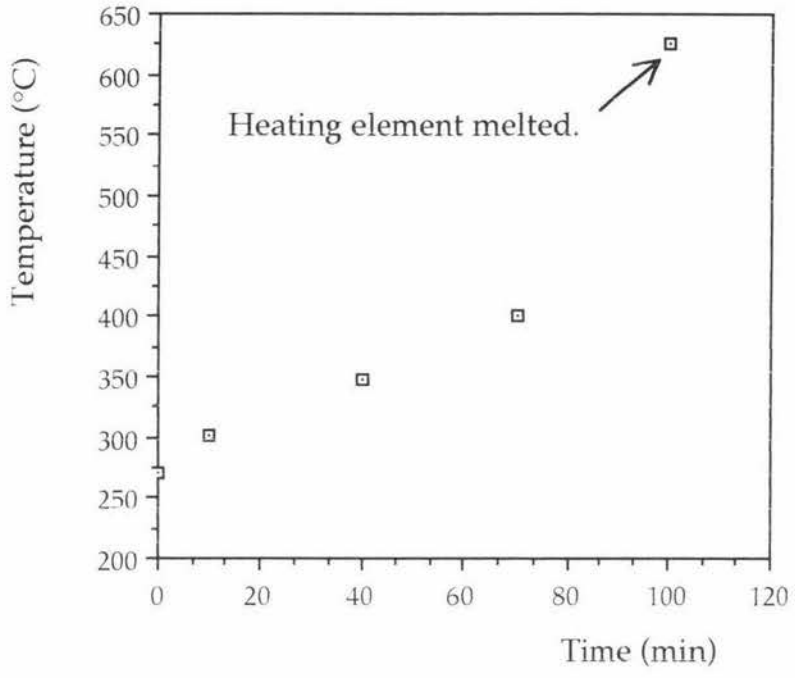


Figure 3.6. First attempt at sintering. The heating element melted when the power was increased. A small amount of ceramic was sintered and had adhered to the heating element.

This could be further developed, perhaps by using an acetylene torch or automating the control of the heating element so that longer heating times could be arranged. However instead of pursuing these approaches it was decided to build a PIN diode phase shifter. The BST phase shifter could be developed at a later date.

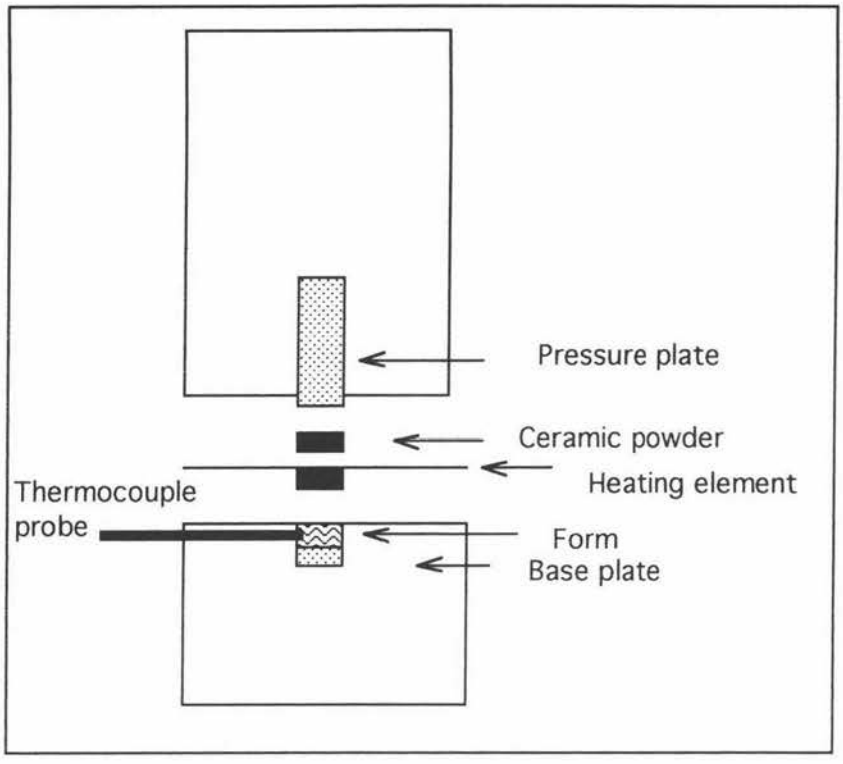


Figure 3.7. Hot press Mk. 2. The press had better mechanical properties but it was difficult to estimate the temperature of the ceramic.

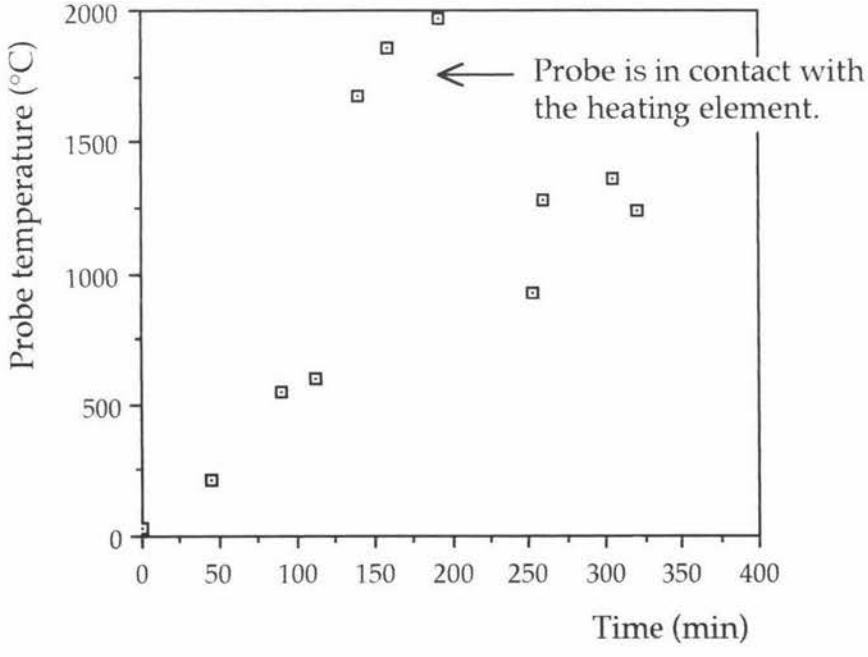


Figure 3.8. The second attempt at sintering BST ceramic. Although the required temperature was reached at the heater, the ceramic did not sinter because the temperature decreased sharply as the probe was moved away from the heating element.

3.3 PIN Diode Phase Shifter.

The PIN diode can act as a variable capacitor. Any diode can be thought of as two 'charged plates' separated by a distance, d (see fig 3.9). The depletion region in a diode lengthens and contracts depending on the size and direction of an applied electric field. Thus by varying the voltage across the diode the capacitance can be changed. As the reverse bias voltage is increased, the width of the depletion region also increases and the capacitance decreases. If a varying electric field is applied then the depletion region will contract and expand as the electric field varies. The speed at which the depletion region can expand and contract is determined by the drift velocity of the holes and electrons. At VHF, UHF and radio frequencies the inertia of the holes and free electrons is so great that the width of the depletion

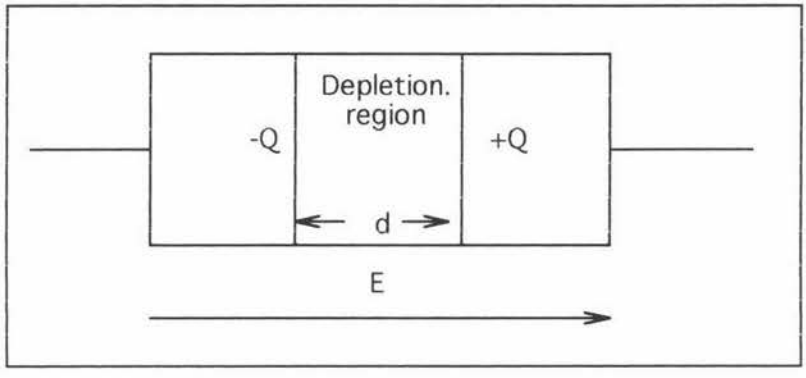


Figure 3.9. Schematic diagram of a diode. In a PIN diode, the depletion region will contract and expand substantially to give a highly variable capacitance. The cross section of a PIN diode is larger to increase the capacitance.

region remains constant. An external dc electric field can be applied and the value of the capacitance seen by the high frequency fields is determined by the applied dc electric field.

The phase shifter can be designed in two different ways. The first relies on artificial transmission lines as described on page 20. The second makes use of passive filter characteristics as described on page 14. This idea is very simple but has one major disadvantage. As the phase change is increased the signal amplitude is reduced. This limits the maximum phase change to under 60°. Two phase shifters were designed. The first (fig 3.10) is based on a naïve idea which failed to take into account the attenuation due to each phase shifter. It also ignored the geometry of the array.

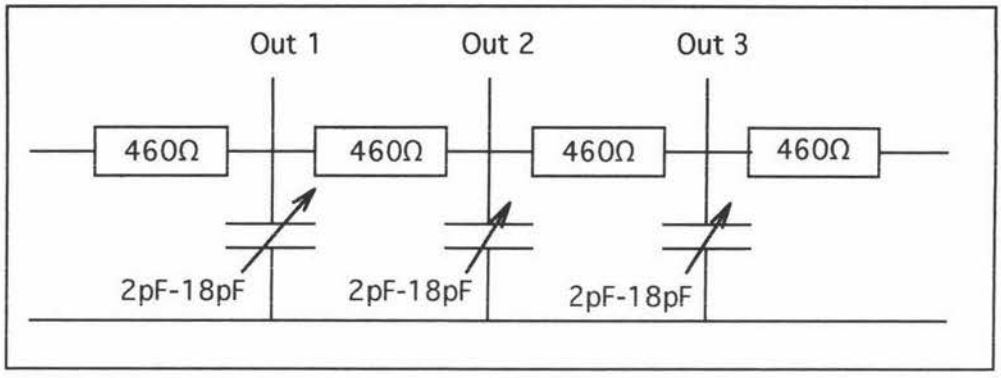


Figure 3.10. Phase shifter Mk. 1. A cascaded network of 16 R - C circuits. No amplification is included so signal levels are severely attenuated by the sixth output.

Although the antenna will be described in detail later, it is necessary for some basic information to be presented now. The array is a regular 4 by 4 grid as in Fig 3.11. To direct the major lobe of the antenna in a particular direction (ignoring any coupling) only two phase differences are necessary. The phase shifter design shown in Fig 3.10 makes it impossible to take advantage of this. The phase shifter in figure 3.12 is laid out in a series of columns each with a phase difference of δ_1. The signal is then amplified before the second δ_2 phase shift is imposed on each

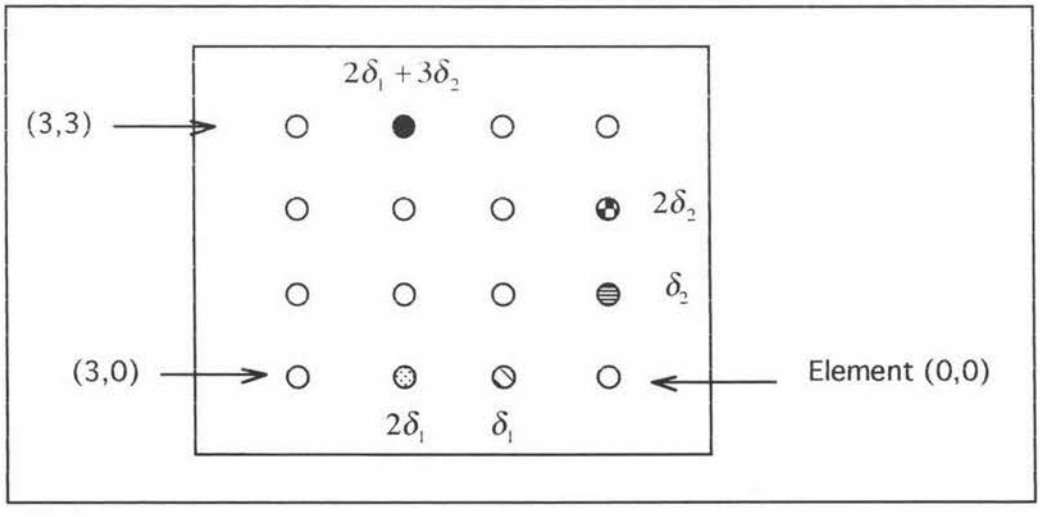


Figure 3.11. Geometry of the antenna. The phase difference between adjacent elements are multiples of δ_1 and δ_2 (as determined by Equation 1.a.). This can be used to simplify the design of the phase shifter.

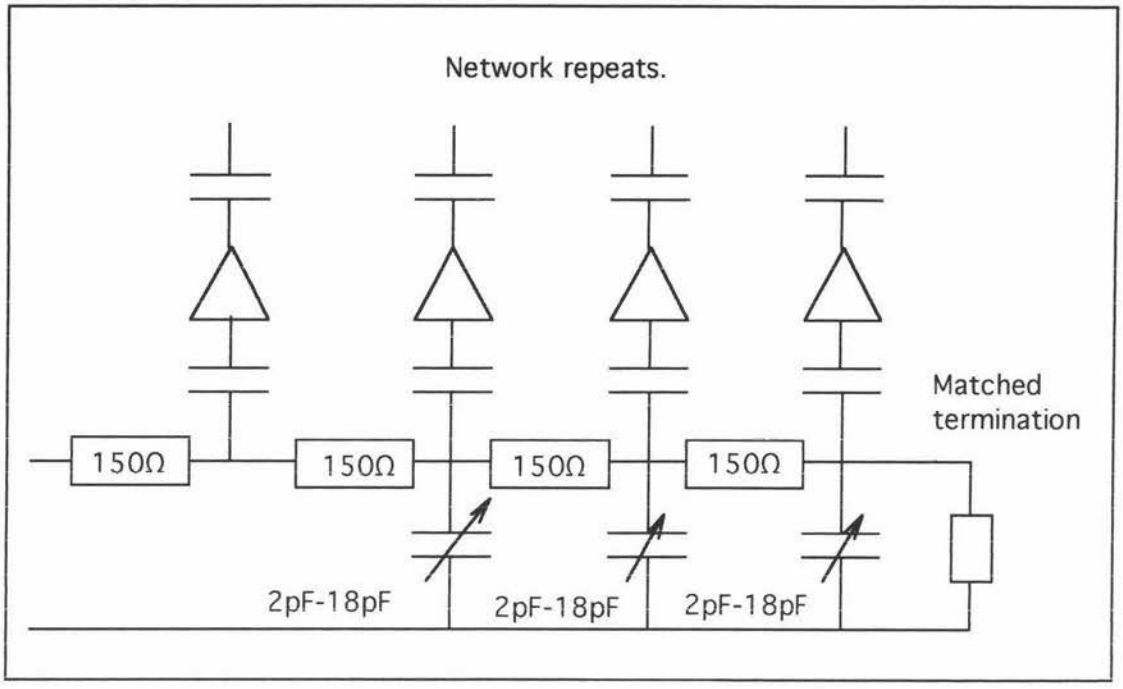


Figure 3.12. Phase shifter Mk. 2. This phase shifter is designed to take advantage of the geometry of the array. The $\delta 1$ phase shift is applied in multiples by a short cascaded network of R - C circuits. The 4 outputs are amplified and pass through an identical network to apply the $\delta 2$ phase shift in multiples.

row. This phase shifter cannot be used in an array with different geometry. The phase shifts, δ_1 and δ_2, must be less than 60° which limits the range of directions the array can orientate the major radiation lobe.

The PIN diodes capacitance varies between 2 and 18pF. A resistance value must be chosen so that a large phase change (>40°) occurs with a small amplitude variation. To choose a resistance value the circuit was modelled using the Electronics Work Bench Package with a range of resistance values (10Ω to 500Ω). The results were plotted (fig 3.13a) and the optimum region of the graph was chosen. This region was retested with smaller resistance intervals (see figure 3.13b). 150Ω was chosen as the R-C circuit did not cause excessive attenuation. The maximum phase shift between adjacent elements was predicted to be approximately 40°. This is too small for a phased array to be used in a practical situation but is suitable for demonstration purposes. The phase shifter employed in the array gives a much larger phase shift than that predicted by Electronics Work Bench (~80°) (see figure 3.14). This is probably because the real phase shifting device is effected by spurious capacitance. The amplitude of the phase shifted signal was smaller than predicted. This is expected as the amplitude variation increases with an increasing phase variation and the phase change was greater than predicted.

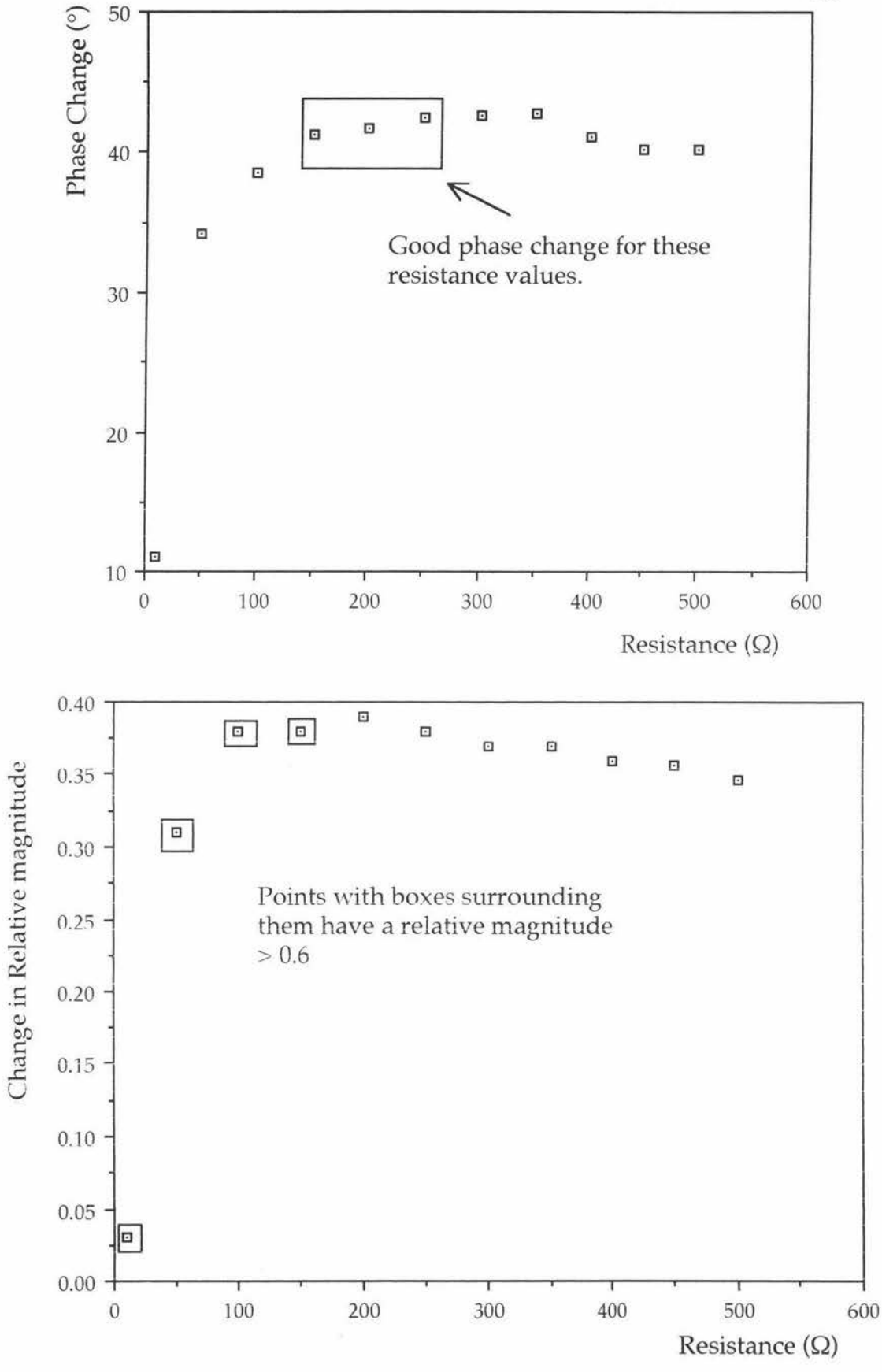


Figure 3.13a. The expected phase variation (top) is compared for different resistance values. The optimum region is between 100Ω and 200Ω. The variation in amplitude (bottom) is large in this region also. Thus we expect the signal to be severely attenuated at the output of the phase shifter.

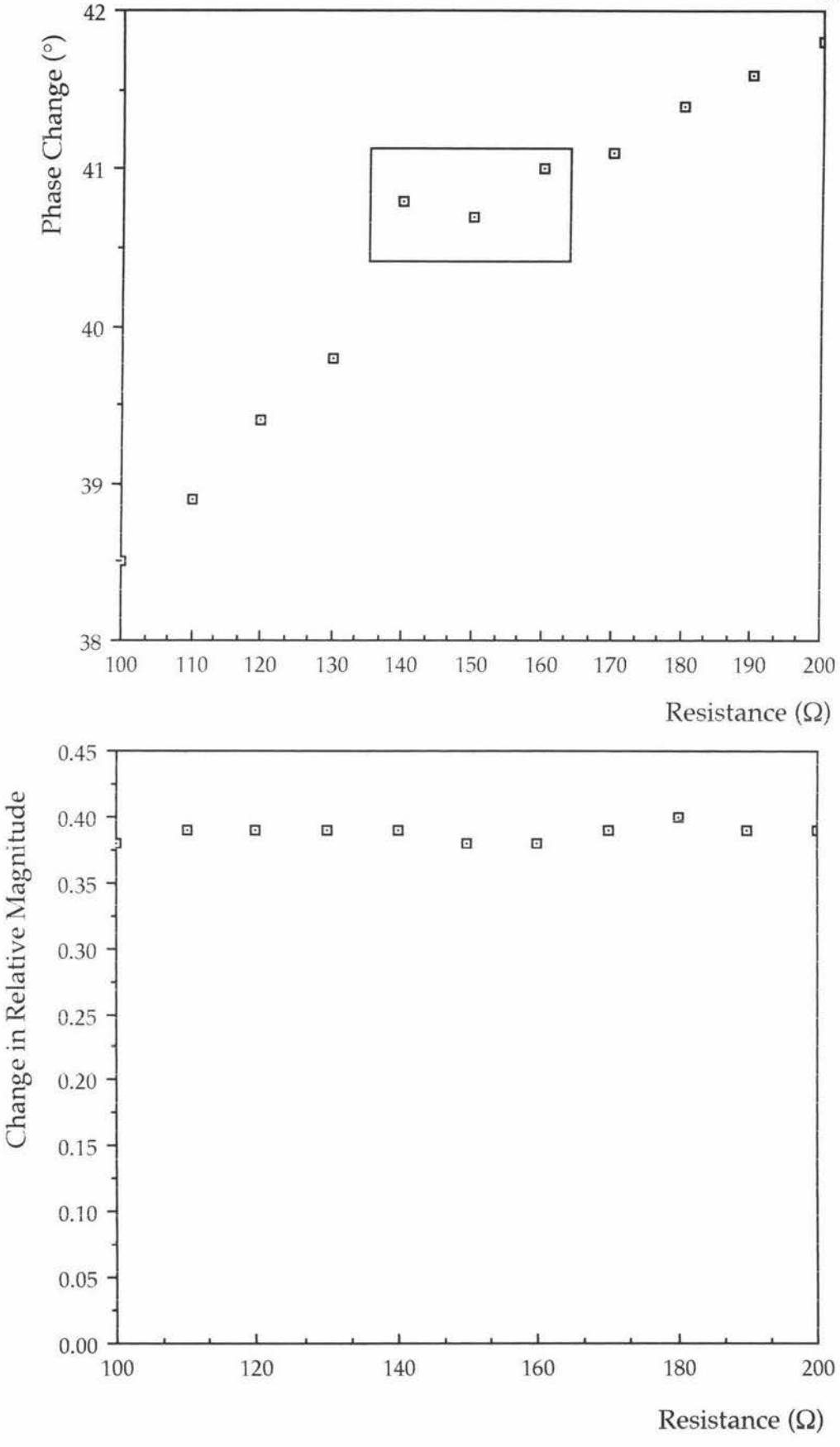


Figure 3.13b. The expected phase variation (top) is compared for different resistance values, within the region selected from figure 3.13a. The optimum region is within the box. The variation in amplitude (bottom) is essentially constant over the range of resistance values.

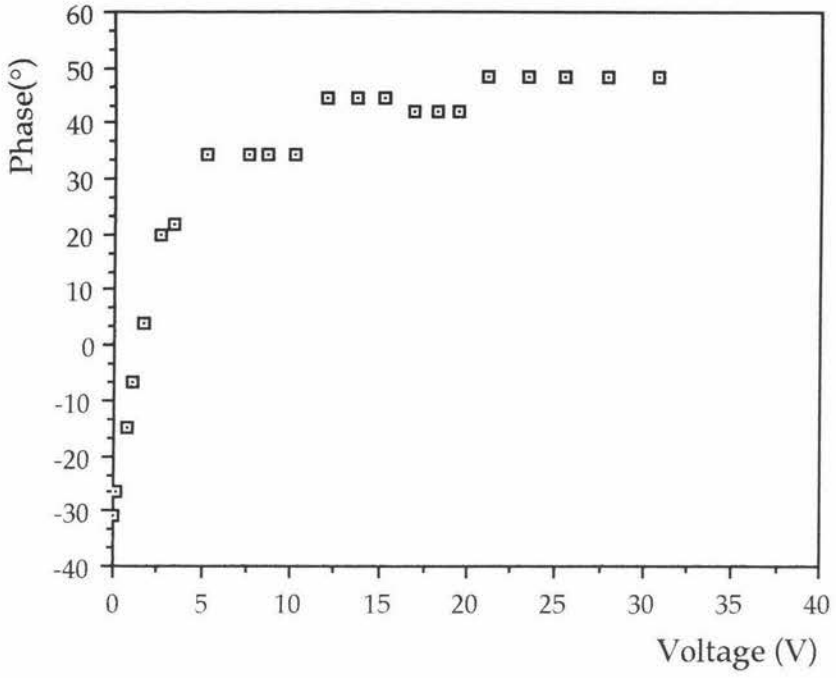


Figure 3.14. The measured phase shift between adjacent elements due to changing the voltage across the PIN diodes. The phase change is steep initially as the change in capacitance is very sensitive at low voltages. The measurements at higher voltages appear quantised. This is an effect of using a digital oscilloscope to measure small phase variations near the upper cut off frequency.

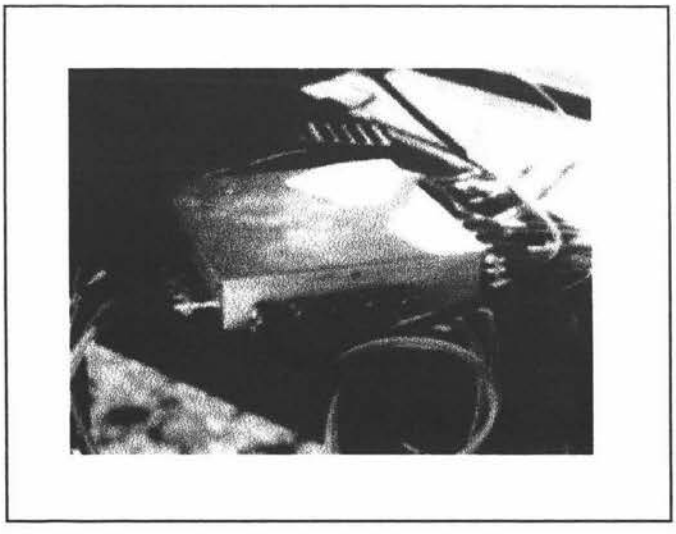


Figure 3.15. The phase shifter within its box. All the high frequency circuits are contained within seperate boxes to reduce cross talk and interference from background noise.

Chapter 4
The Attenuator.

4.1 Amplitude Control.

The signals emanating from the phase shifting unit are small and unequal. That is, each feed from the phase shifter has a different amplitude. If the amplitude from each element is different it will reduce the directivity of the antenna. The position and shape of the main lobe (the direction the antenna is pointing) will change as will those of the minor lobes. Therefore, it is important to be able to control the output of each element in the antenna.

The output amplitude of each element is controlled VIA an attenuator circuit. Assume (for the moment) that it is desirable for each element to have the same output amplitude. Element (0,0), having gone through the shortest path of the phase shifter, will have the strongest signal. Element (3,3) will have the weakest signal because it has the longest path through the phase shifter. This means the signal to the elements can be ranked from strongest to weakest depending only on the phase shift and the element position. The stronger elements will have their signal reduced to the same level as that of the weakest signal and then all the signals will be amplified by identical amplifiers. This system will give a uniform output, indeed, any amplitude distribution can be imposed on the elements of the antenna.

An attenuator can be produced from three PIN diodes (see figure 4.1). A practical PIN diode attenuator is shown in figure 4.2. This design comes from an rf amateur handbook[4] with only one modification. The attenuated signal must be amplified directly afterwards so an amplifier was built into the attenuator. The PIN diode attenuator is a fairly simple device. When the control voltage is close to, or above, the reference voltage the impedance of the diodes across the attenuator drops. The diode in series acts as a very large resistor so very little voltage appears across the amplifier terminals. When the control voltage is much less than the reference voltage the diodes across the attenuator are open circuits while the diode in series is a short circuit and hence all the voltage appears across the amplifier.

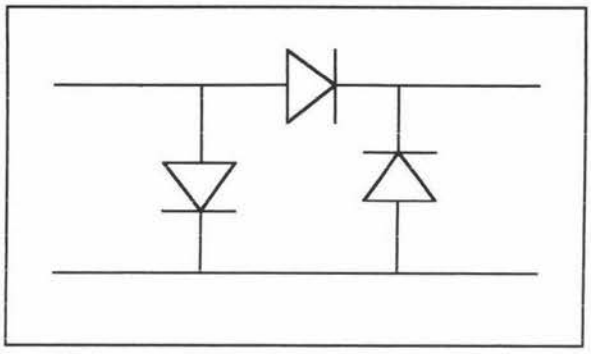


Figure 4.1. Basic PIN diode attenuator.

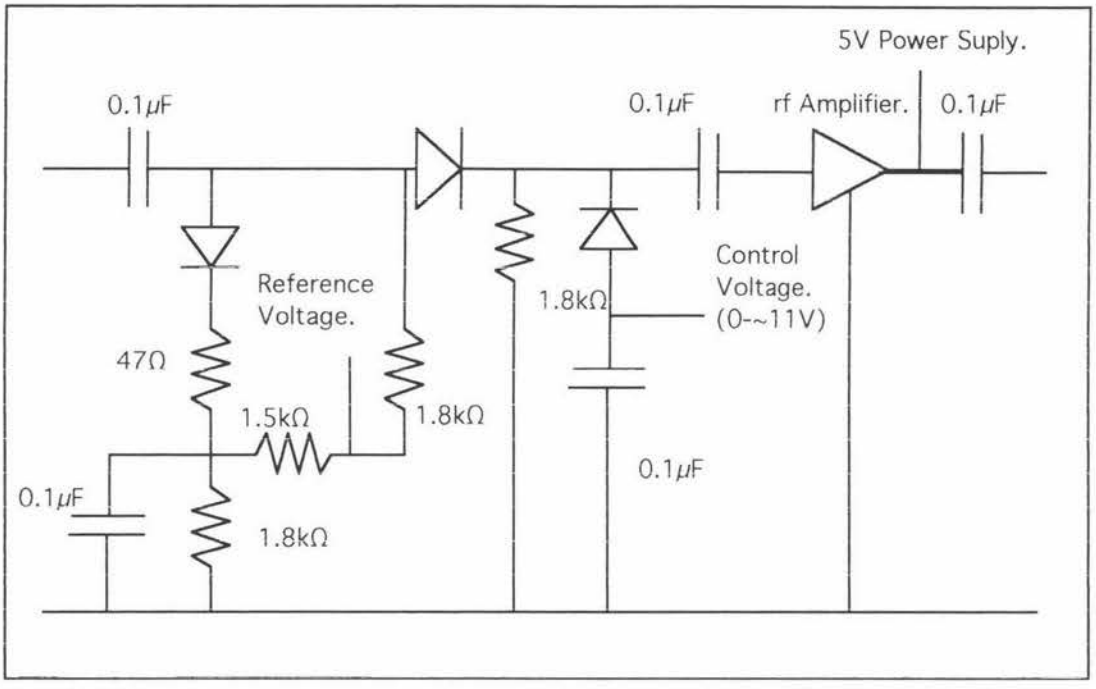


Figure 4.2. A practical PIN diode attenuator. The diodes are 5082 schottky barrier diodes.

4.2. Attenuator Performance.

The attenuators were tested individually by measuring the output from a known input signal. The input signal was 200 MHz (the carrier frequency of the antenna) with an amplitude of 100 mv (rms). The reference voltage was set to 12V and the control voltage was increased from 0V until the signal was indistinguishable from the noise. The characteristic curves of the 16 attenuators are shown in figure 4.3.

All of these curves show a sharp cut off as the control voltage approaches the reference voltage. To investigate this, a 'typical' attenuator was tested. The reference voltage was varied from 12V down to ground. For each reference voltage the cutoff voltage and the maximum output was noted. The cut off voltage was plotted as a function of the reference voltage (figure 4.4). This information was used to standardise all the attenuators.

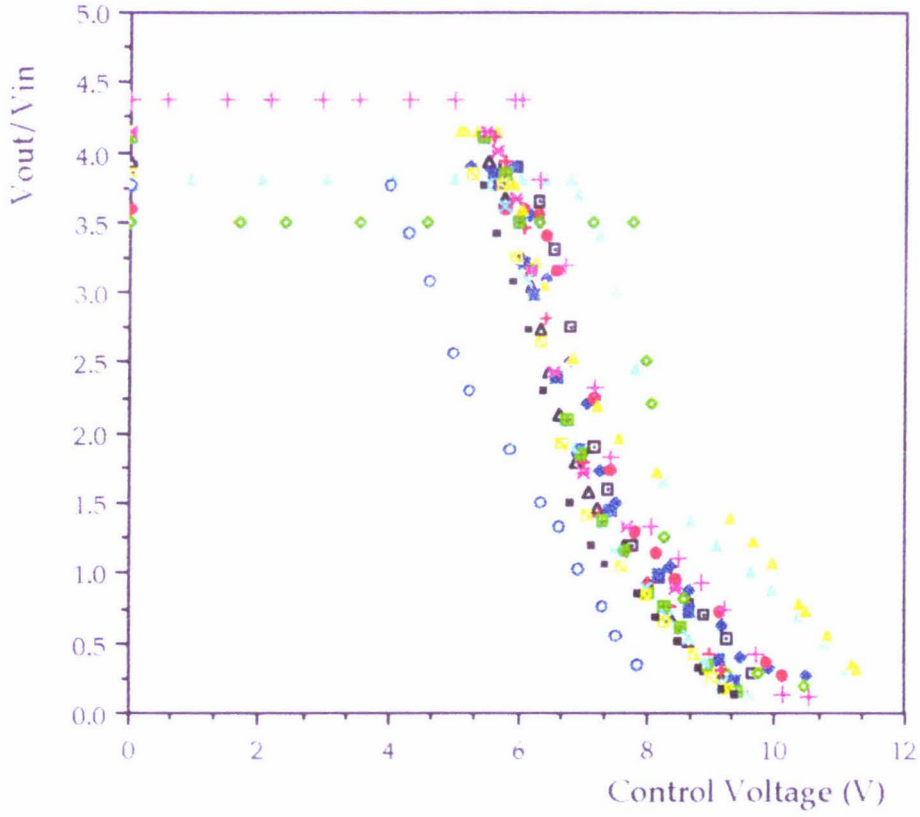


Figure 4.3. The attenuator profiles. All of the attenuators perform in the same manner but the cutoff voltage varies between attenuators. The cutoff voltage could be made the same by varying the reference voltage.

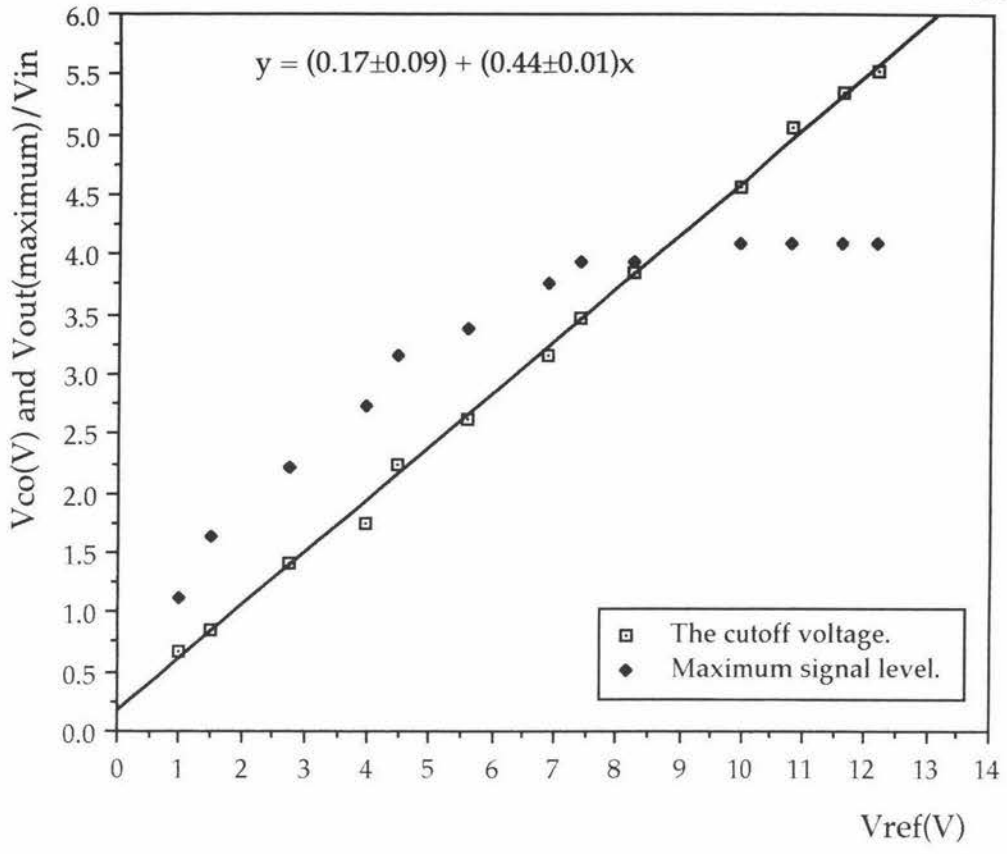


Figure 4.4. The cutoff voltage and the maximum output vary with reference voltage. The output decreases with a decreasing reference voltage so the reference voltage must remain fixed at 12 volts.

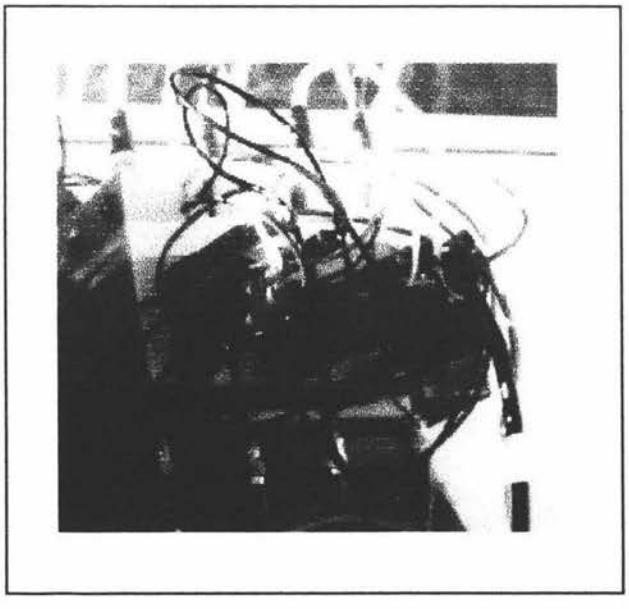


Figure 4.5. A group of 4 attenuators. The attenuators are obscured by cables as each must have three power supplies (reference voltage, control voltage and amplifier power supply) and ground as well as input and output.

Chapter 5.
Control Software.

5.1. Introduction.

The design and performance of the phase shifters and attenuators have been discussed. They operate at 200 MHz although their operation is controlled by dc voltages. The system that controls the attenuators and phase shifters has only two tasks. First, given a direction to orientate the main lobe, the control system must command the appropriate phase shift and attenuation for each element. Secondly, it must convert the phase shifts and attenuations into a voltage and deliver the voltage to the appropriate terminal.

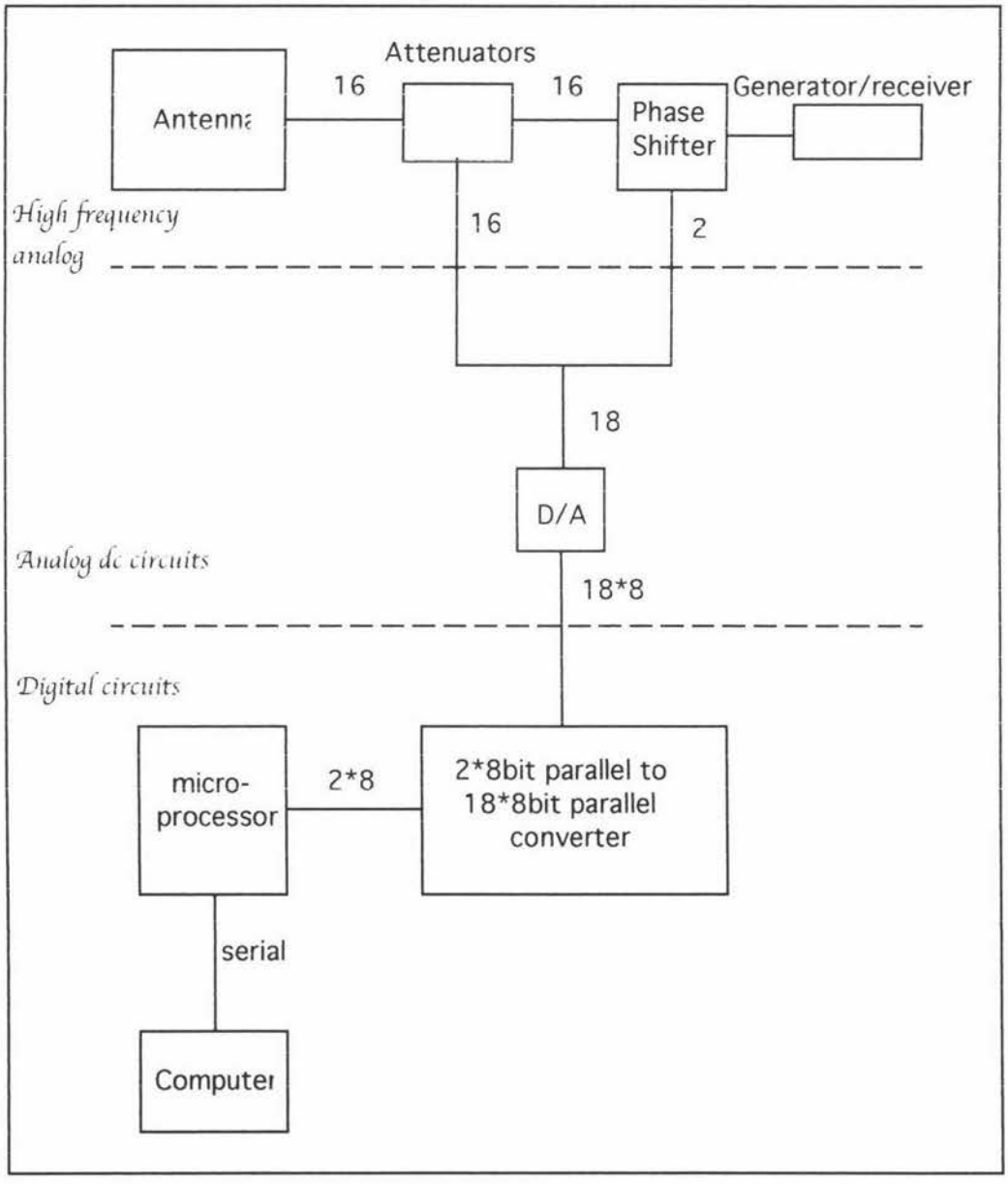


Figure 5.1. Schematic layout of the antenna control circuitry. The number of parallel data lines are indicated by the number alongside each control line. This indicates some of the hardware and software requirements of the antenna. The nature of the circuits are indicated in italics.

The first task the control system must complete is a software problem while the second part is only partially so. To determine the software requirements of the control system, some decisions regarding the hardware must be made.

1) An Apple Macintosh computer is used. The serial port is the only port available, but the control system requires 18, 8 bit wide parallel data. This means the data must go from the computer to the control system via a microprocessor.

2) The 6809 microprocessor trainer receives the serial data from the computer and converts it to parallel data. The microprocessor has 2 parallel ports so a hardware "sample and hold" system must be used to further expand the parallel network.

The software must calculate the phase and amplitude information. These data must be converted into a form acceptable to a microprocessor. The microprocessor receives the data and uses its parallel port to make the data fully parallel. The hardware must contain a sample and hold system to receive the data from the microprocessor and remember the data until the microprocessor updates it. The output from the sample and hold system must be converted into the analogue voltage used to control the attenuators and phase shifters.

5.2. Computer Control Program.

The control system starts in the computer. It is here that the phase and amplitude of each element is calculated and converted to a number between 1 and 255. It is this number that is sent to the microprocessor. Figure 5.2 shows a flow chart of the program. The source code (included here) is written in C using the Symantec Think C Program manager.

The phase is simple to calculate given the required direction of the major radiation lobe and the spacing between the elements (see equation 1.a).

```
float pathdiffx( float hormax, float dx)
{
float phi1,a;
a= -2*pi*dx;
```

a is the phase difference due to the spacing of the elements (dx).

```
phi1 = a*cos(hormax);
```

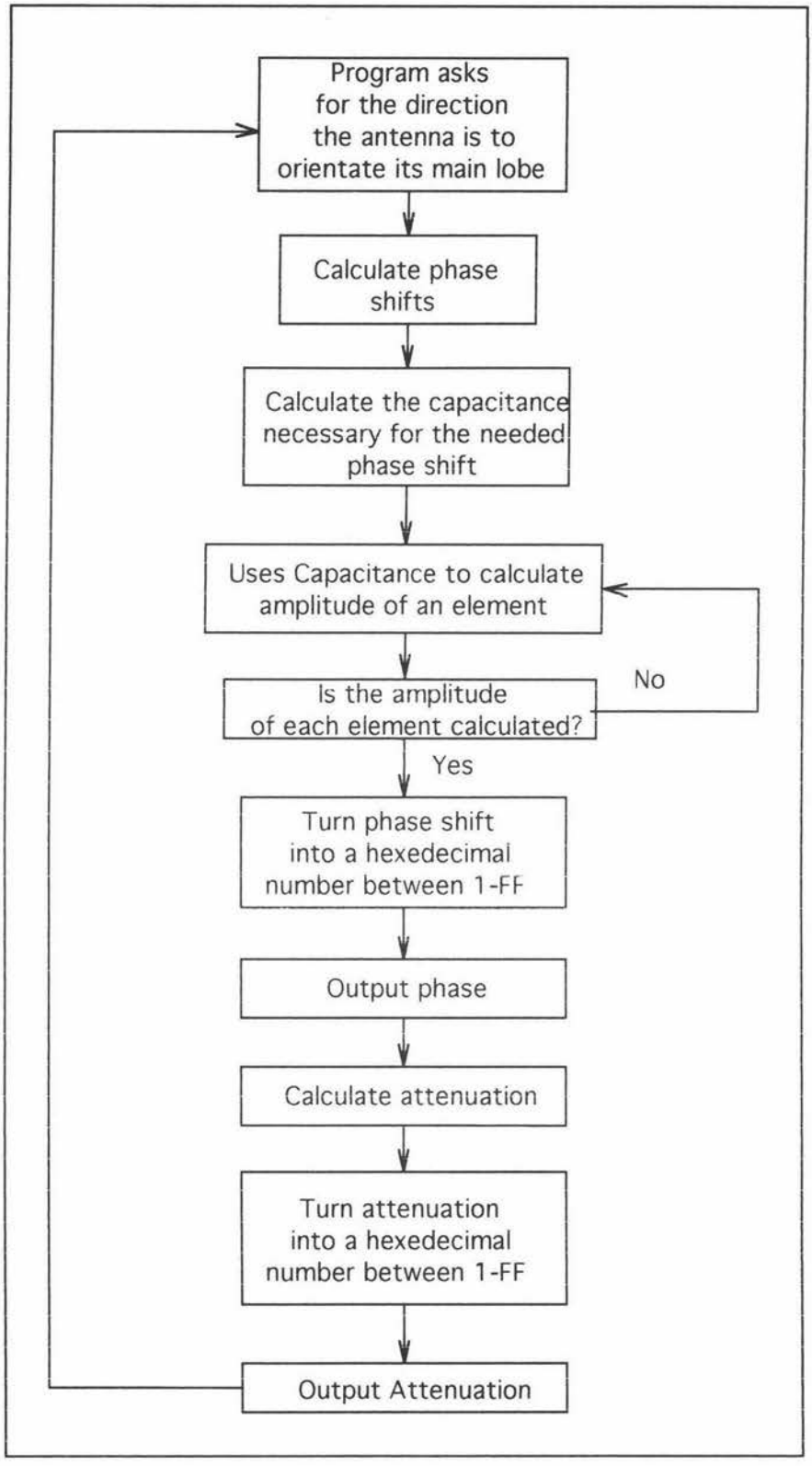


Figure 5.2. Flow chart of the program to calculate and output the phase and amplitude information to the microprocessor.

phi1 is the necessary phase adjustment to ensure the major radiation lobe is in the direction *hormax*.

```
return(phi1);
}
```

This part of the program calculates one of the two phase differences needed. The variable, *a*, is merely the effective phase difference between adjacent elements. The total phase difference must add to an integral number of wavelengths. Hence, *phi1* is the phase difference necessary for a maxima to occur in the direction of *hormax*. See figure 5.3 for the coordinate system employed. The second phase difference is similar but the phase difference is calculated for the direction of the maximum in the azimuthal direction (*vertmax*).

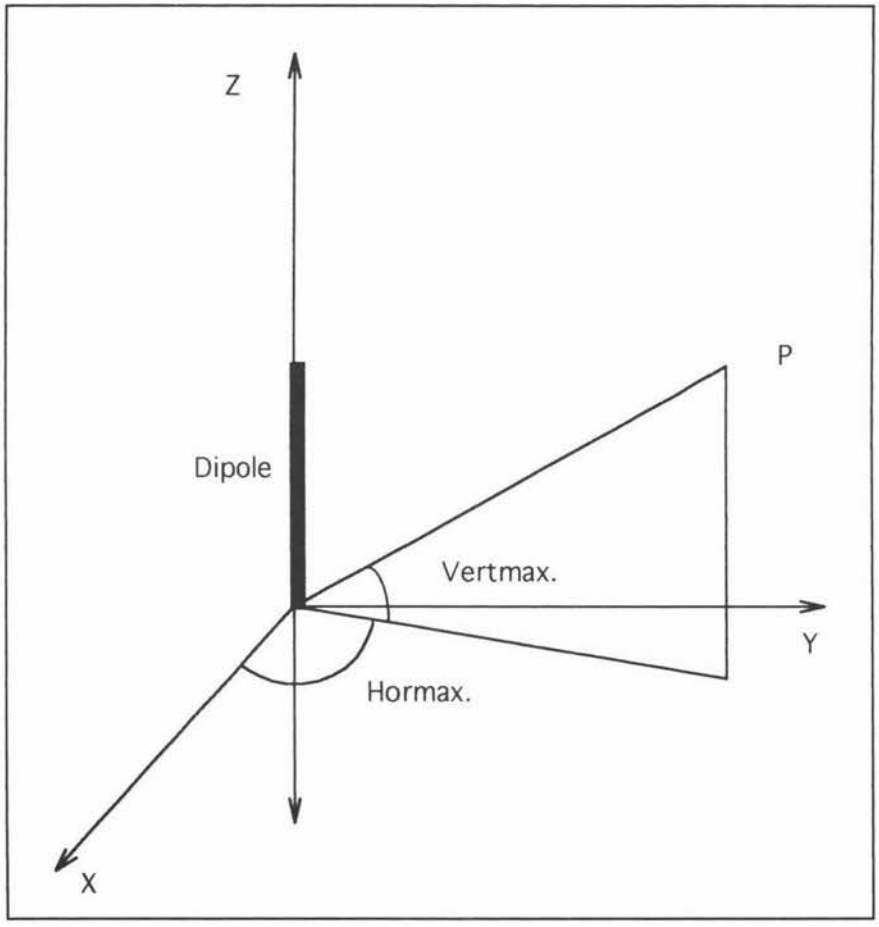


Figure 5.3. Coordinate system used by the software to calculate the data necessary for the main lobe to point in the direction of P. The antenna lies in the x - y plane as shown by the dipole.

The next part of the program calculates the capacitance necessary to produce the required phase shift.

```
float find_c1(float phasex)
{
float f,r,c1,cap;

r = 150;  The resistance of the network resistors
f = 200e6;  The operating frequency of the antenna

c1 = 2*pi*r*f*tan(-phasex);
The capacitance using simple R-C circuit theory
cap = 1/c1;
return cap;
}
```

The capacitance is found so that the attenuation of the circuit can be found. The circuit is a voltage divider so it is simple to calculate the attenuation at each element feed.

```
float amp_det2(float cap2)
{
float r, vo, vi,f,x2,atten2,temp2;

r = 150;
vi = 100;  The input voltage.
f = 200e6;

x2 = 1/(2*pi*f*cap2);  The reactance of the circuit.
temp2 = sqrt(r*r + x2*x2);  The total impedance of the circuit.
vo = (r/temp2)*vi;
atten2 = vo/vi;  The attenuation of the circuit.

return(atten2);
}
```

The attenuation of a single step down one of the networks has been found. The attenuation of element *i,j* is simply

$A_{ij} = i * (\text{step attenuation of the first network}) * j * (\text{step attenuation of the second network})$

The next step is to calculate the attenuation required for each element and use this to ensure that the output at each element is the same.

```
OSErr outamp(float atten1, float atten2, short ain, short aout)
{
float atten[5][5],attenmax,outat;
int i,j;
short x;
long *z,k;
OSErr err;
unsigned char b;
attenmax = 0;
k = 2;
for(i=1;i<=4;i++)
        {
        for(j=1;j<=4;j++)
                {
                atten[i][j] = 1/(i*atten1*j*atten2);
```

The maximum attenuation necessary is found in this loop.

```
                if(atten[i][j]>attenmax)
                        {
                        attenmax = atten[i][j];
                        }
                }
        }
for(i=1;i<=4;i++)
        {
        for(j=1;j<=4;j++)
                {
                outat = atten[i][j]/attenmax;
```

The actual attenuation is turned into a function of the maximum attenuation (normalised).

```
            x = outat*255;  The normalised attenuation is turned into an integer
                            between 1 and 255 for output to the microprocessor.
            b = x;
            if(b==0)
                    {
                    b=1;
                    }
            printf("output amplitude is %X\n",b);
            err = FSWrite(aout, &k, &b);par
            wait(0.1);
            }
        }

return(err);
}
```

The entire listing is on a diskette in the pocket on the inside of the the back cover. This program does not take into account the coupling between elements. Simulation programs are developed later to show the effect of this on the performance of the array.

5.3 Data Reception Program.

The microprocessor has only 2 tasks. The first is to receive the computer output. The second task involves emitting the data in a parallel form to the appropriate device. The first task is trivial. The computer sends a serial data stream to the microprocessor. The serial port on the microprocessor simply accepts a byte of information and shuts down until the microprocessor reads the byte from the port (and stores it in memory). The port then resets and starts receiving again. As the computer is so much faster than the microprocessor the computer delays for half a second between bytes.

```
WAIT    LDA     0,Y         READ SERIAL PORT STATUS REGIS-
TER
        ANDA    #$01  IF DATA HAS NOT BEING RECEIVED WAIT
        BEQ     WAIT
        LDA     1,Y                         DATA IS RECEIVED
        CMPA    #$00  IS DATA ZERO? IF SO WAIT FOR SOME
MORE
        BEQ     WAIT
```

The wait routine simply loads accumulator A with the information at the address of the status register of the serial port. If the status register tells the microprocessor that the serial port has been written to then the microprocessor will read the byte at the serial port's address. The information contained at the serial port (from the computer) is read into accumulator A. If the byte is zero then it is rejected and the microprocessor begins the cycle again.

```
STA     ,X      STORE DATA IN ITS DESIGNATED AREA
JSR     UPDATE          UPDATE DISPLAY REGISTER
STB     BSTOR                   STORE B TEMPORARILY
LDB     #$FF    LOAD B WITH 255 SO DISPLAY WILL LAST
JSR     DISPL           DISPLAY DATA
```

If the byte is accepted as valid data it is stored at the X pointer location. The microprocessor then jumps to a display routine (so the operator can check the validity of the data) and increments the X pointer. The B accumulator is loaded with 255 so that the display will last long enough for the operator to read it.

```
LDB     BSTOR                   RETRIEVE B
INCB                    ADD 1 TO B
CMPB    #DMAX
BEQ     OUTP    ALL DATA RECEIVED GO OUTPUT DIS-
PLAY
BRA     WAIT    IF NOT RETURN TO GET NEXT CHARAC-
TER
```

The program now checks how many bytes of data have been received. If all the data are received the program branches to the second microprocessor program to output the data. If the data are not complete then the microprocessor will return to wait for more data from the computer.

5.4. Hardware Interface Program.

The second program is a little more complex. The program must determine what each byte of data is destined to control. All of the control data must be output in parallel. The microprocessor has only 2 parallel ports so a direct approach is impossible.

Each byte of data must be output along with a second byte controlling the destination of the data. This is possible through the use of latches and AND gates.

At this point a small aside is necessary. A latch is a device which ignores the current input until a high signal is applied to the control pin. The device will then output the input and continue to do so when the control pin goes low. While the control pin is low the input is ignored and the output will continue unchanged. See figure 5.4 for schematic and truth table.

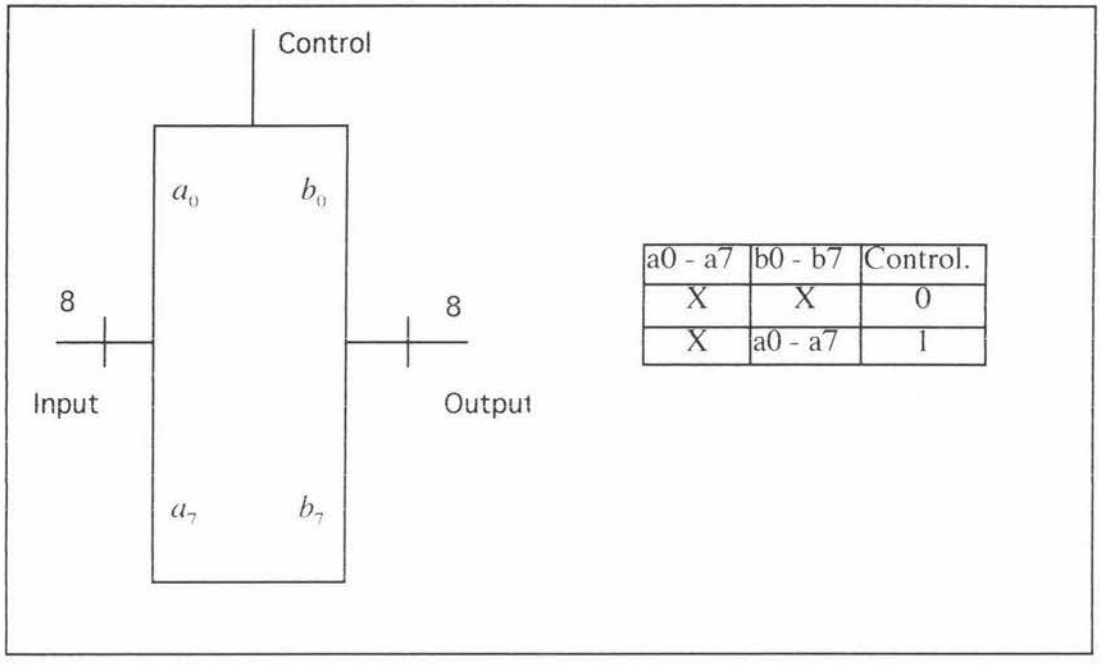


Figure 5.4. Schematic view of a latch with its truth table.

The microprocessor can use one port to output data and the second port can control the final destination of the data byte. The control byte is fed into 18 AND gates in such away that only 1 AND gate is high for any control byte. The AND gates are connected to the control lines on the latches. Thus the data destination is controlled.

All that remains is to determine some form for the control byte. The control byte can have only two high bits at any one time and each pairing must be unique. If each bit in the second port is paired up as in Table 5.1. Then there are 18 unique 2 bit signals. Each 2 bit signal can be fed into a logical AND gate to make 18 control lines.

0o000011
0o000101
0o001001
0o010001
0o010001
0o100001
o1000001
1o000001
1o000010
1o000100
1o001000
1o010000
1o100000
11o00000
0o000110
0o001010
0o010010
0o100010

Table 5.1. 18, 8 bit binary numbers containing only 2 high bits.

Below is the heart of the output routine. The lines in bold represent where the data is sent to the hardware. The rest of the routine is spent manipulating bits to produce control bit patterns similar to those shown in table 5.1. Producing the bit routines involves using the two accumulators. Each is loaded with a single bit and rotated (that is the accumulator shifts its bits along to the left or right) in turn to produce the needed patterns. The contents of each accumulator must, periodically be stored so the output can be loaded and sent to the outport.

```
        LDB     #$02
        STB     BSTOR2
        *
CONT    LDA     #$01        LOAD A
        ADDA    BSTOR2          ADD A AND B
        STA     ASTOR
        STA     2,Y             OUTPUT CONTROL BITS
        LDB     ,-X             GET REAL DATA
        STB     0,Y             OUTPUT DATA
```

The above block of code works as follows. The A and B accumulators are given one bit numbers (1 and 2). Accumulator B stores its number at the memory location BSTOR2. Accumulator A adds the number from BSTOR2 to the value it already contains making a one byte number containing only 2 high bits. This number is sent to the B parallel port and from there to the hardware. Accumulator B retrieves the

data byte from the X pointer and sends it to the A parallel port and from there to the hardware.

```
LDB     BSTOR2
CMPB    #$80
BEQ     CONT2
LSLB
STB     BSTOR2
CLRA
STA     2,Y
BRA     CONT
```

Accumulator B loads the one bit number from BSTOR2 and compares it to hexadecimal 80 (binary 10000000). This happens to be the highest one bit number available in a byte. If accumulator B is equal to $80 then the microprocessor branches to the next control routine CONT2. If accumulator B is not equal to $80 then accumulator B is rotated left one bit (ie from 00000010 to 00000100 etc) and stores it at BSTOR2. The control port is cleared to prevent any of the latches from changing their output and the program branches back to CONT. When the program branches to CONT2, it has sent 7 of the 18 data bytes.

```
CONT2   LDA     #$02    AGAIN WITH A ACCUM BIT ROTATED ONE
        LDB     BSTOR2
        ADDA    BSTOR2
        STA     ASTOR
        STA     2,Y             OUTPUT CONTROL DATA
        LDB     ,-X
        STB     0,Y             OUTPUT DATA TO ARRAY
```

When the program reaches CONT2, BSTOR2 contains $80 and accumulator A is loaded with 2 (00000010) and the process reverses itself. Accumulator A and BSTOR2 add to make a byte with a unique combination of high bits. This control byte is sent to the control port and the data are sent to the data port.

```
LDB     BSTOR2
CMPB    #$04    GOTO CONT3 IF CONT OUT = 01000001
BEQ     CONT3
LSRB
STB     BSTOR2
```

```
        CLRA
        STA     2,Y
        BRA     CONT2
```

Now accumulator B is compared to $4 (00000100), if it is not equal the accumulator B rotates to the right and stores the result in BSTOR2. The control port is cleared and the microprocessor branches back to CONT2 to continue sending the data. When accumulator B is $4 the program has sent 13 of 18 bytes of data and branches to CONT3.

```
CONT3   LDA     #$04    AGAIN WITH BITS ROTATED EVEN FUR-
THER
        LSLB
        STB     BSTOR2
        ADDA    BSTOR2
        STA     ASTOR
        STA     2,Y             OUTPUT CONTROL DATA
        LDB     ,-X
        STB     0,Y             OUTPUT DATA TO ARRAY
```

CONT3 is, essentially, a continuation of the previous two routines. At this point BSTOR2 has $4 and accumulator A has $4. The two added together will not make a byte with two high bits. To prevent this accumulator B is shifted left once (from 00000100 to 00001000). Accumulator A and BSTOR2 are added together and sent to the control port. The data byte is sent to the data port.

```
        LDB     BSTOR2
        CMPB    #$80            OUTPUT CONTROL = 10000100
        BEQ     RETURN
        LDB     BSTOR2
        CLRA
        STA     2,Y
        BRA     CONT3
```

Now BSTOR2 is compared to $80, if it is not equal to $80 the program branches back to CONT3 after clearing the control port. When BSTOR2 is equal to $80, the process of data output is complete. The program then goes into an infinite loop keeping both the data and the control ports clear.

Chapter 6
Hardware.

6.1. The Digital Board.

The hardware is required to receive 18 bytes of data from the computer. The digital data must be delivered to the appropriate device as an analogue voltage. In many respects the form the hardware has taken was determined by the choice of software and computer.

The basic layout is shown in figure 6.1. It consists of 18 latches connected to a data bus. The latches are controlled by a series of AND gates which are operated by the control bus. The output of the latches goes into an almost binary weighted network[1]. The output from the resistor network is fed into an amplifier with unity gain. This is fed into a second amplifier with the gain determined by the needs of the device to be controlled.

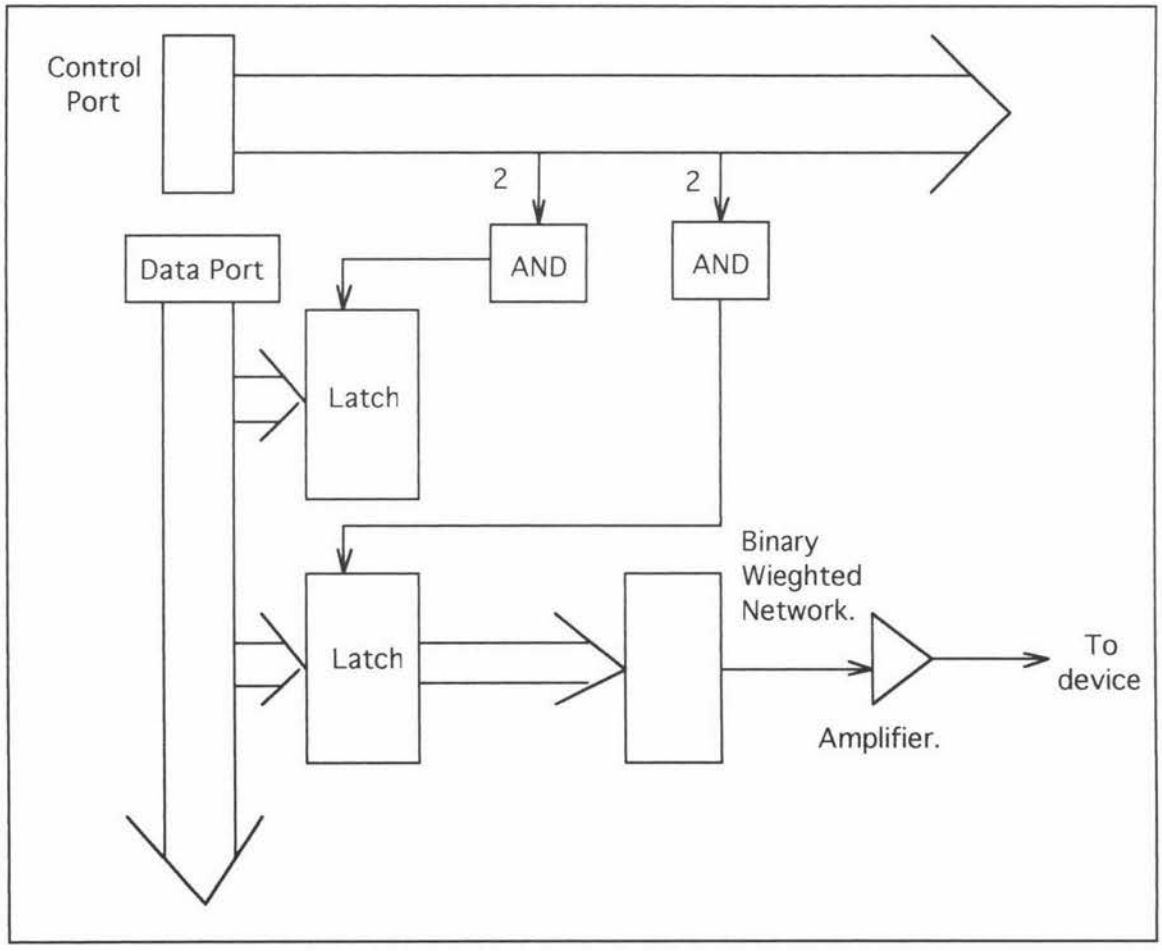


Figure 6.1. Schematic diagram of the control hardware. The binary weighted network combined with the amplifiers make up the D/A converters.

1. The reason the resistor network is not quite binary is that resistor values follow the series $R_{new} = R_{old} + 0.2R_{old}$. Thus we get values such as 1kΩ, 1k2Ω, 1k5Ω, 1k8Ω, 2k2Ω. If the base value of the resistor network is 1kΩ, then the next 8 values are 2kΩ, 4kΩ, 8kΩ, 16kΩ, 32kΩ, 64kΩ, 128kΩ, 256kΩ. None of these values (apart from 1kΩ) are available so the values closest to ideal were chosen.

6.2. The analogue Board.

The output of the digital circuit goes into a binary weighted network and from there to two amplifiers. The gain of the amplifiers will determine the range of the analogue voltage. An additional voltage applied between the first and second amplifier will provide an offset to the output of the D/A converter (see figure 6.2). The attenuators do not respond to control voltages below the "knee" voltage (see figure 6.3a). Thus the amplifiers have an offset close to that of the "knee" voltage. After this offset is applied the D/A only needs to vary through about 5V so no gain is needed. The phase shifter (see figure 6.3b) control voltage must vary from 0V through to 12V. Thus no offset is needed but a gain of 2 is necessary.

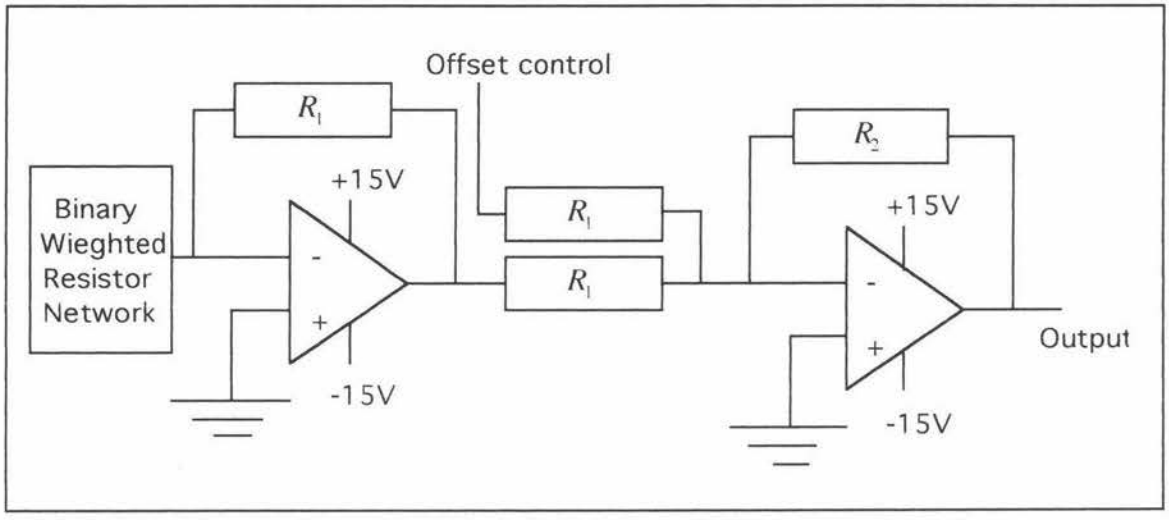


Figure 6.2. Schematic diagram of the D/A converter. R1 is 1 kΩ and R2 is determined by the device to be controlled.

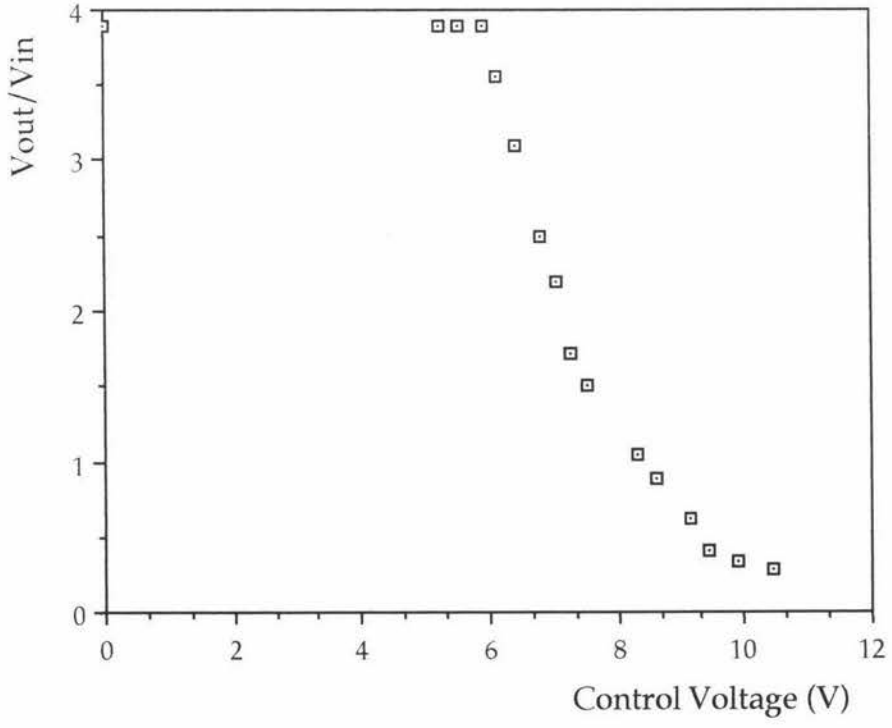


Figure 6.3a. A "typical" attenuator calibration curve. Note the attenuation starts at about 6V.

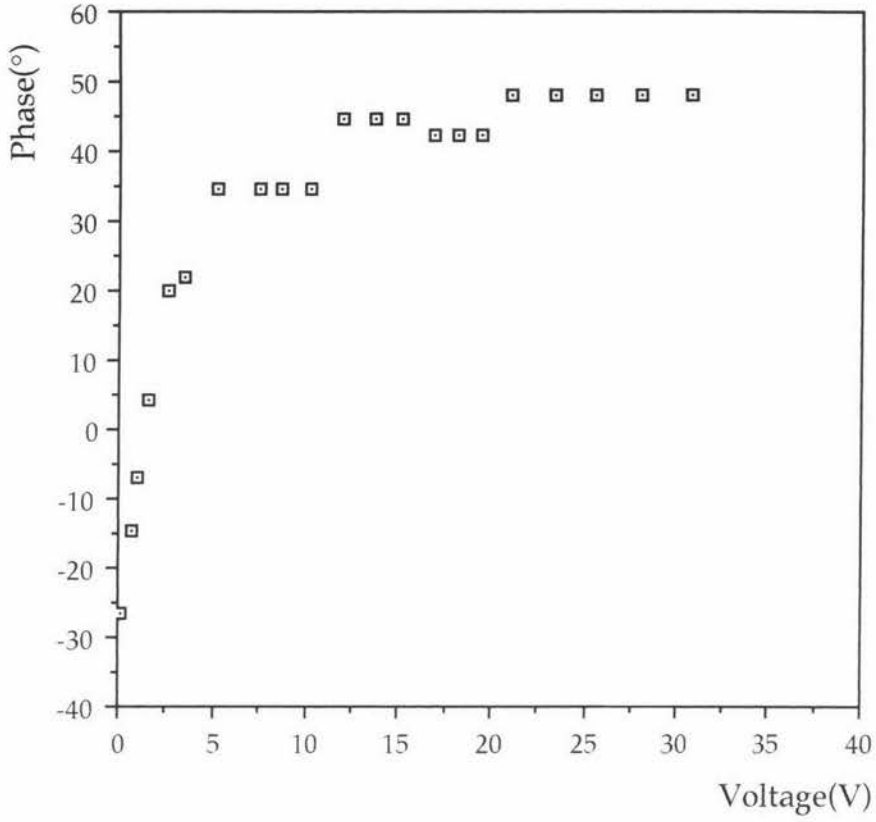


Figure 6.3b. Shows the phase shift changing with applied voltage. Note that the phase shift is close to its maximum value by 12V.

6.3. Hardware Performance.

After some teething problems (like mistakes in printed circuit boards). The control system was tested. The microprocessor was made to output numbers between 0 and 255. The response of the control system was measured and the average results were plotted (see figure 6.4a and b). The average step size of the D/A converters without gain is 0.02±0.03V. The uncertainty in the step size is larger than the least significant bit but for this application it does not matter. The D/A converters with gain have a step size 0.04±0.01V.

The control system is now set up and will only require fine tuning. Adjustments to the software will achieve most of this. The method for converting the attenuation and phase shift to a number between 1 and 255 can be changed to take into account the calibration data.

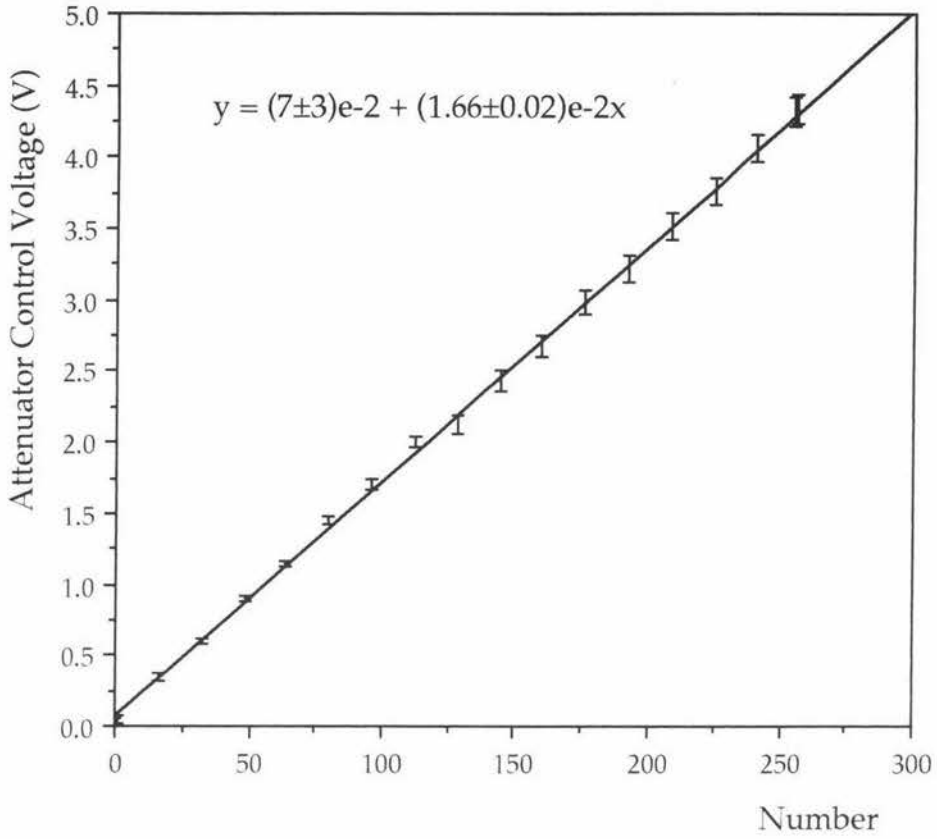


Figure 6.4a. The calibration curve for the D/A converters used to control the attenuators. The output is linear but the minimum step size is smaller than the error in any one value.

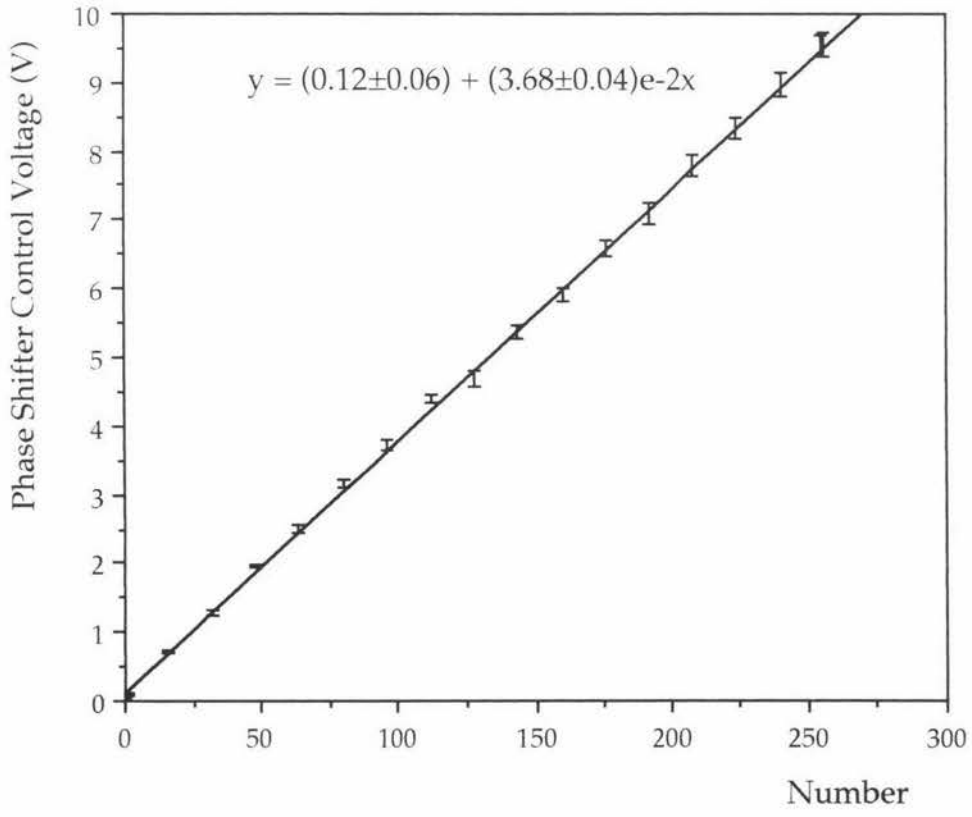


Figure 6.4b. The calibration curve for the D/A converters controlling the phase shifter. The output is linear and the error is smaller than the minimum step size.

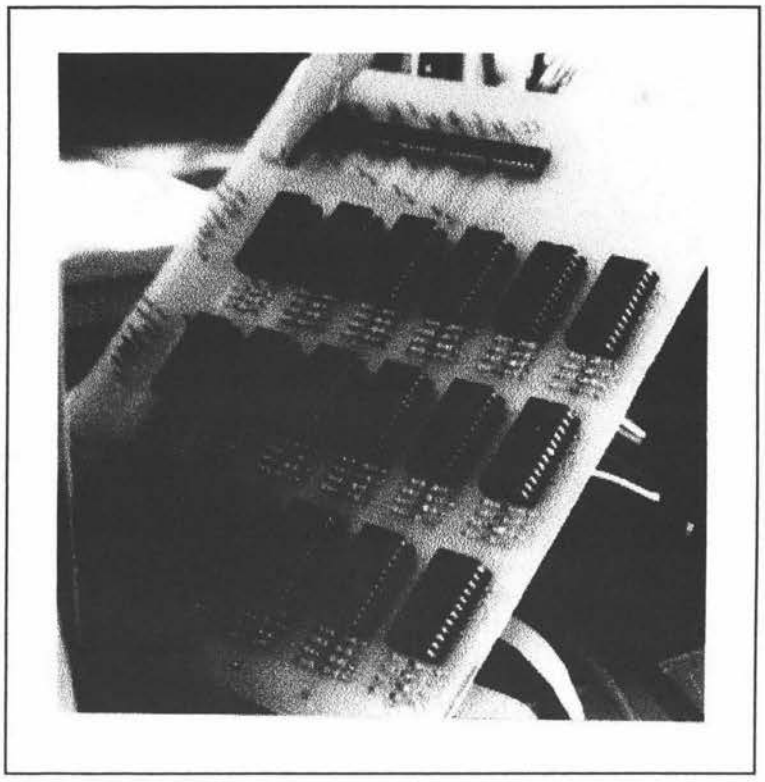


Figure 6.5. The digital board consisting of 18 latches connected to a bus. The latches are controlled by AND gates.

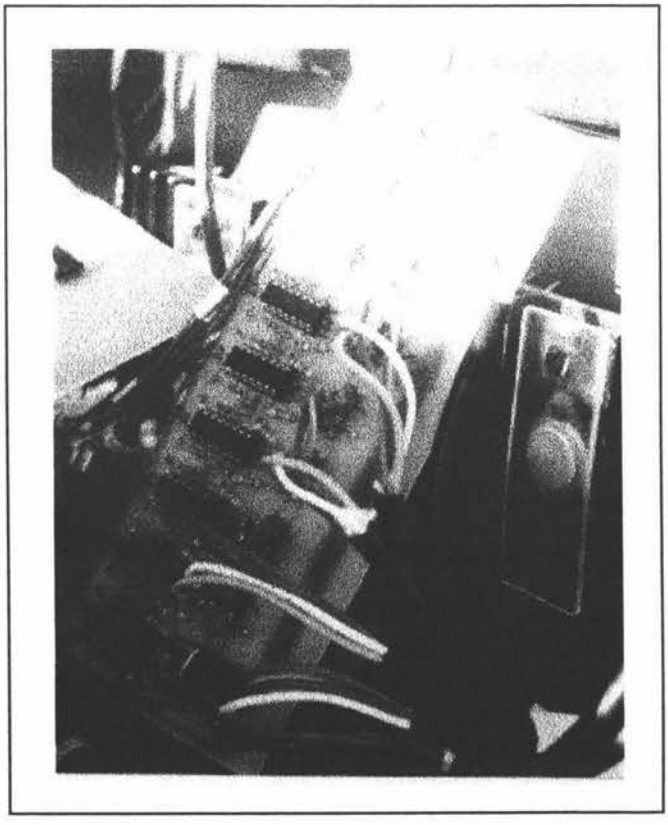


Figure 6.6. The analogue board. 18 D/A converters composed of a binary weighted network and amplifiers.

Chapter 7
Antenna Design.

The antenna is of a very simple design. 16 quarter wave monopoles are arrayed on a 4X4 grid with even $\lambda/9$, rectangular, spacing between the elements. The elements are mounted on sheet aluminium acting as a ground plane. The quarter wave monopoles can be considered half wave dipoles because of the ground plane. The spacing and choice of the type of element were selected after Kraus (ref. 2) was extensively consulted. The choice was made on the basis of two considerations. The antenna had to be portable and therefore small. The antenna should be constructed of the simplest components so that it can be simulated. See figures 7.1 and 7.2 for details of the design. The antenna elements were soldered directly onto BNC connectors. The solder will change the impedance of each element depending on the quantity of solder applied and its location on the element. This impedance mismatch will effect the elements performance but there is little (short of redesigning the antenna) that can be done to prevent this.

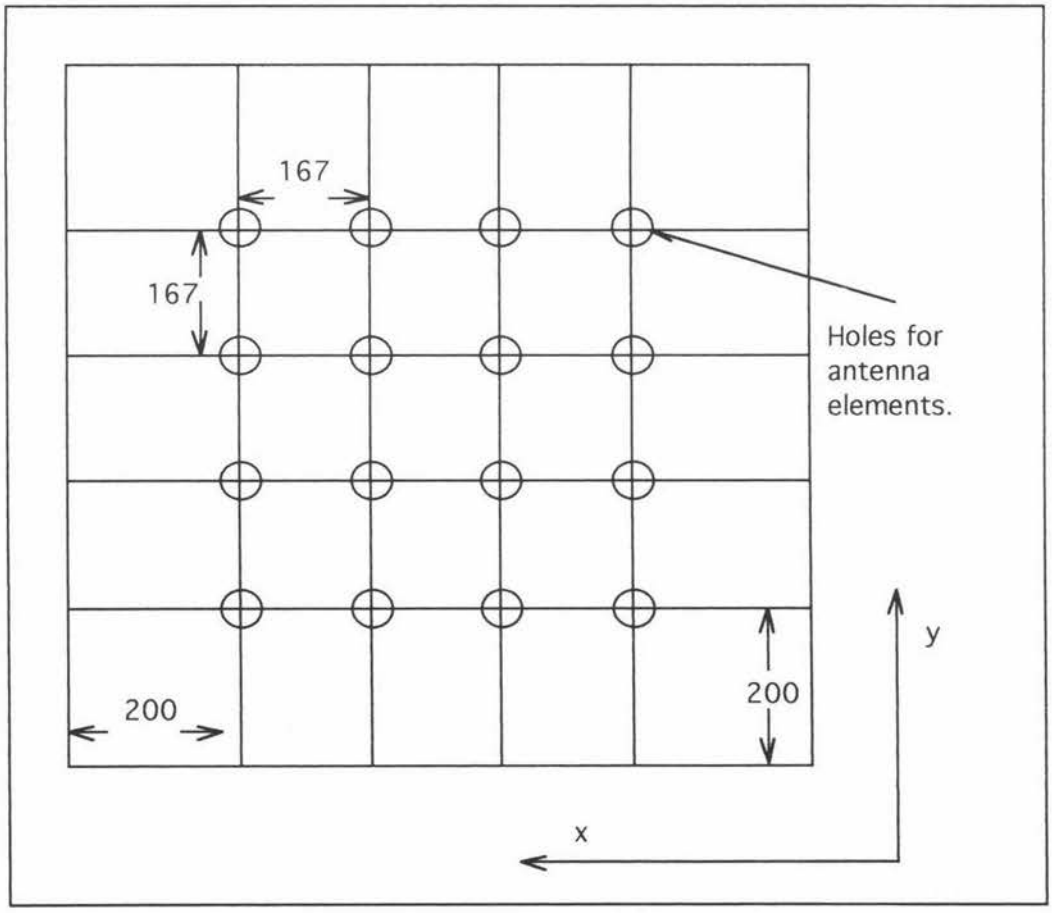


Figure 7.1. Earth plane of the antenna. The elements are spaced $\lambda/9$ apart. The distances are shown in mm.

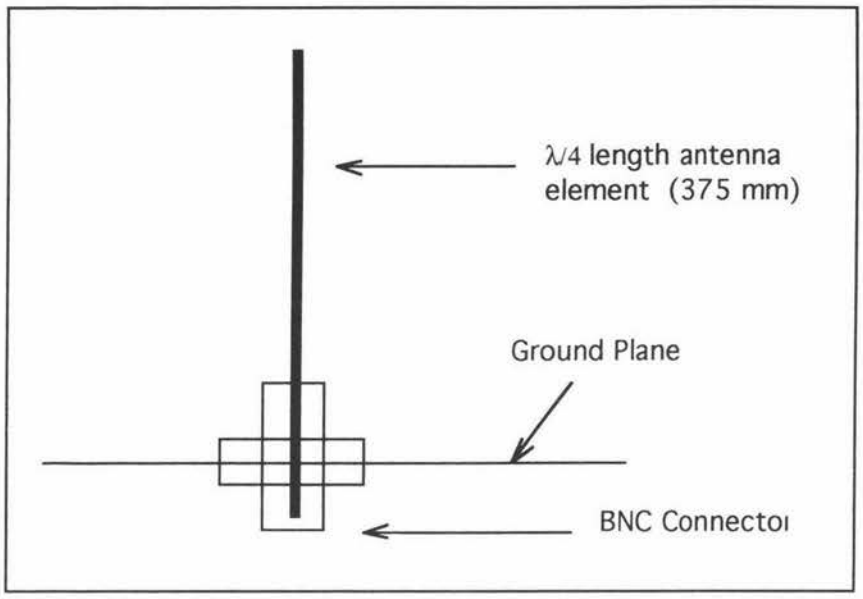


Figure 7.2. Shows the monopole attachment to the ground plane.

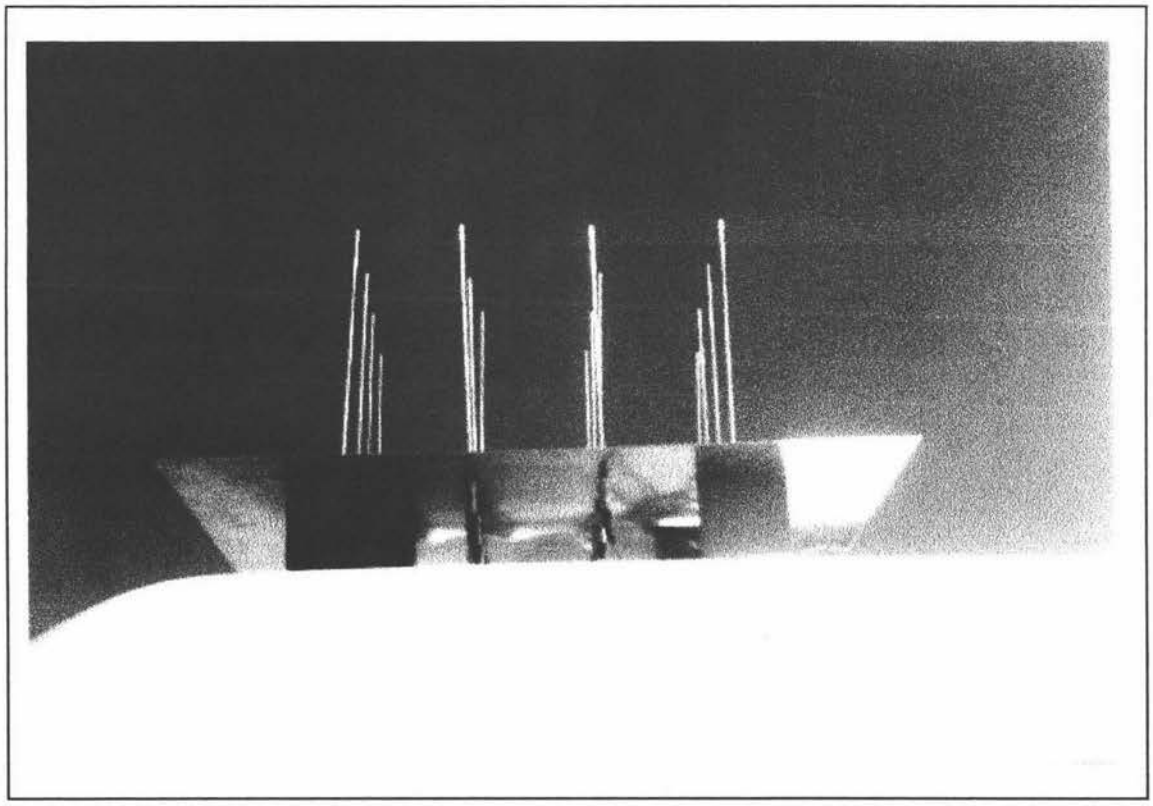


Figure 7.3. Photograph of the antenna during tests. It is shown mounted on top of the van used in the field observations.

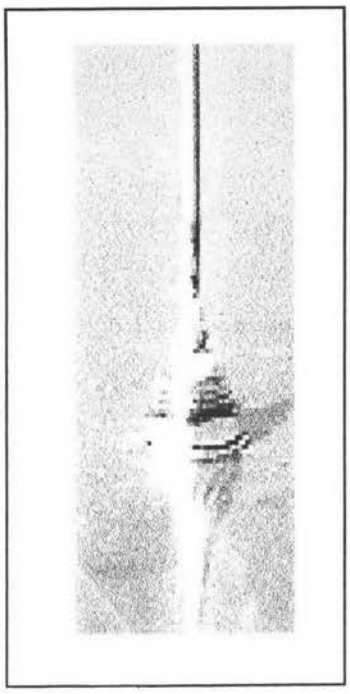


Figure 7.4. Photograph of the attachment of a monopole to the ground plane of the antenna.

Chapter 8
Signal Detection.

With the antenna and the supporting equipment constructed a method for detecting the received signal was needed. The carrier frequency is 200 MHz. This is well within the bandwidth of many modern oscilloscopes and indeed a high frequency oscilloscope was used initially to ensure that the antenna system was working. An oscilloscope is unsuitable for use in field tests as it is bulky and, more importantly, does not filter the input signal. As the transmitting antenna is moved away from the receiver the background interference (public radio stations) begins to dominate and it is no longer possible to measure the signal strength from the transmitter. It was clear that any detection system must act as a filter also.

There are two solutions to this problem. The carrier could be rectified and amplified to provide a small dc voltage that is proportional to the signal amplitude. This is problematical, as the diodes would require characteristic times much less than 5ns. The diode employed must also have a low threshold voltage so that small signals are rectified. However the question is largely academic when one considers the number of high quality detectors available on a single chip.

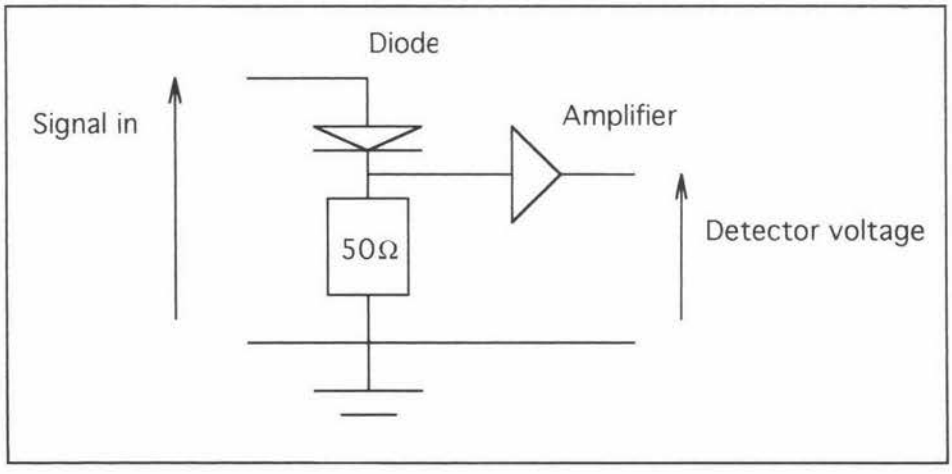


Figure 8.1. General method behind the detection of amplitude modulated signals. Modern methods use lock in amplifiers.

All the detectors available with a bandwidth including 200 MHz are purpose built to demodulate an FM signal. FM signals cannot be used when testing the antenna because the detector output depends on variation of frequency and is largely independent of signal strength. The solution lay in a radio designed to receive signals from the entire public broadcasting spectrum (including 200 MHz). The

detector employed by the radio demodulated AM and FM signals across the entire spectrum. The built in antenna was disconnected and the antenna under investigation was attached. The output from the ear phone jack was sent to a Macquisition unit (a signal acquisition system that can be directly connected to a computer). The signal acquisition software performed a fast fourier transform on the data thus producing the power spectral density function of the received signal. If the signal is amplitude modulated, the value of the power spectral density function at the modulation frequency is directly proportional to the signal strength

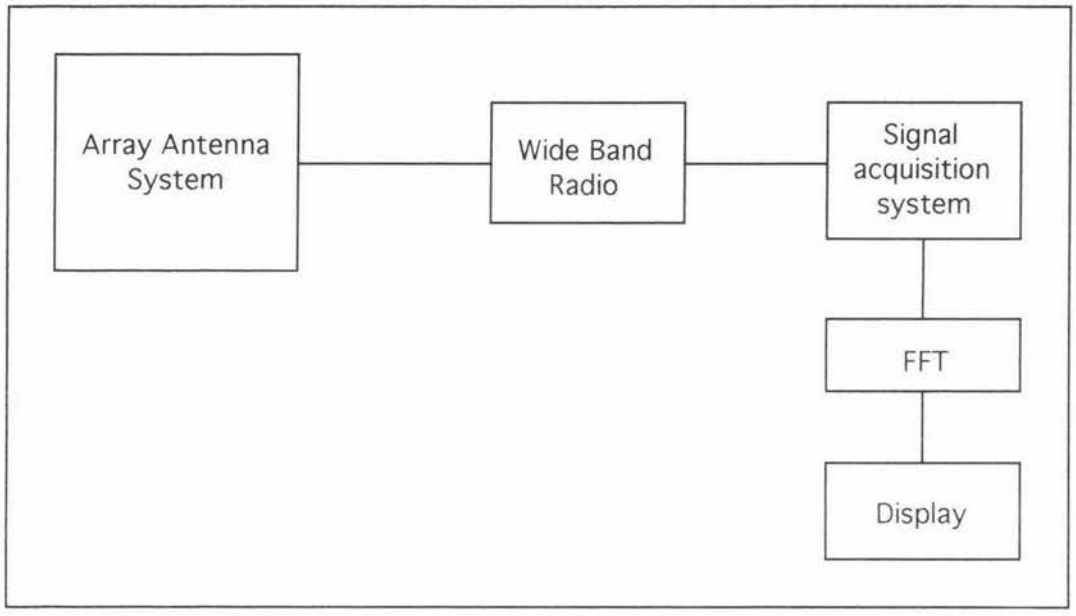


Figure 8.2. Schematic diagram of the detection system used to investigate the array antenna.

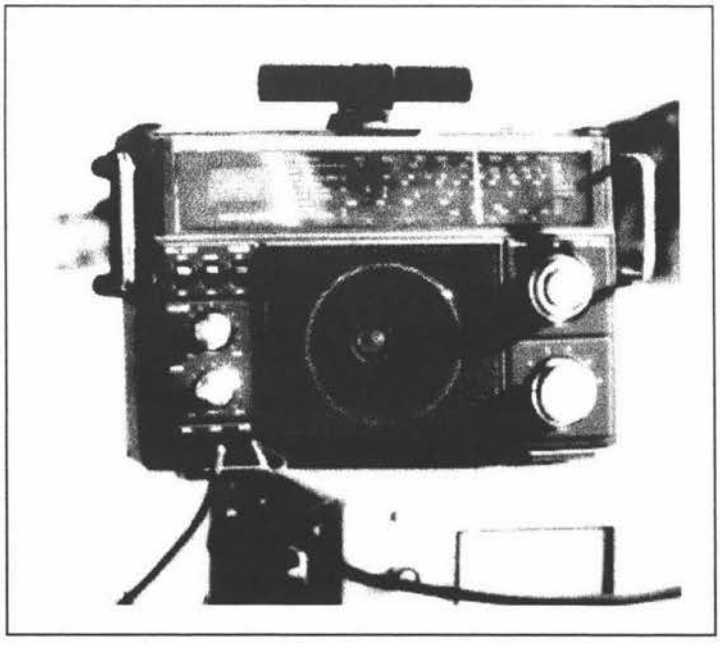


Figure 8.3. "Dick Smith Multi band radio receiver/direction finder" used as the signal detector. The antenna signal is connected to the radio through the antenna jack. The ear phone jack is connected to the Macquisition unit.

Chapter 9
Testing Methodology.

9.1. The Testing Range.

The wavelength was too long for the antenna to be tested inside so all testing was done on a cricket oval during two consecutive fine days (24/25 September). The antenna radiation pattern was measured by using the antenna as a receiver. A quarter wave monopole was used as the transmitter. The transmitter power was 10 watt. The transmitter was moved in 7.8m steps around a circle with a radius of approximately 50m. Both the transmitting and receiving antenna were about 2m above the ground see figure 9.1, 9.2 and 9.3. Despite being in a paddock there were still a number of bodies that could cause disturbances. The worst of these was a lamp post about 5m within the perimeter of the circle (see figure 9.1). Overall the conditions made for relatively interference free measurements.

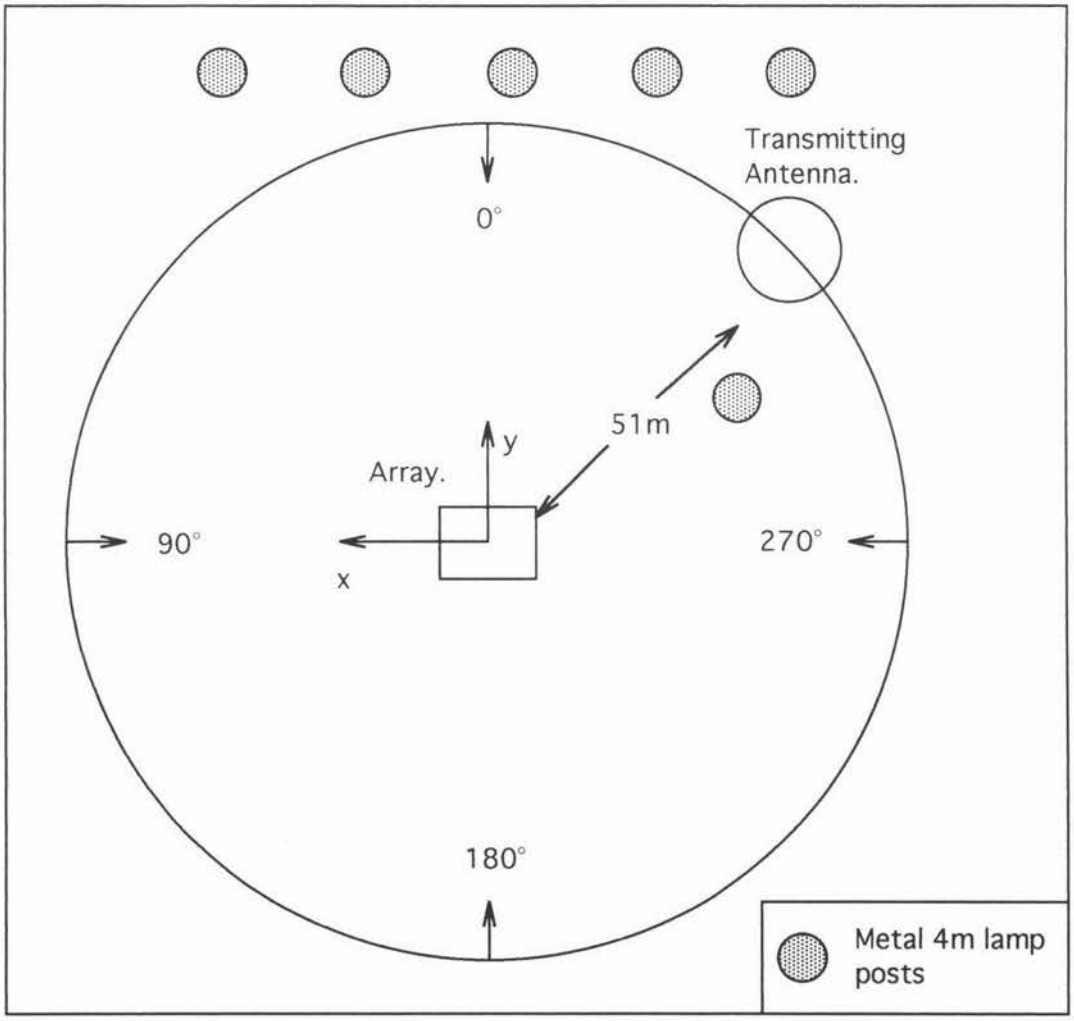


Figure 9.1. Plan view of the testing range. After the phases are set the transmitting antenna was stepped around the circle to measure the power pattern. The phases were then changed and the process repeated.

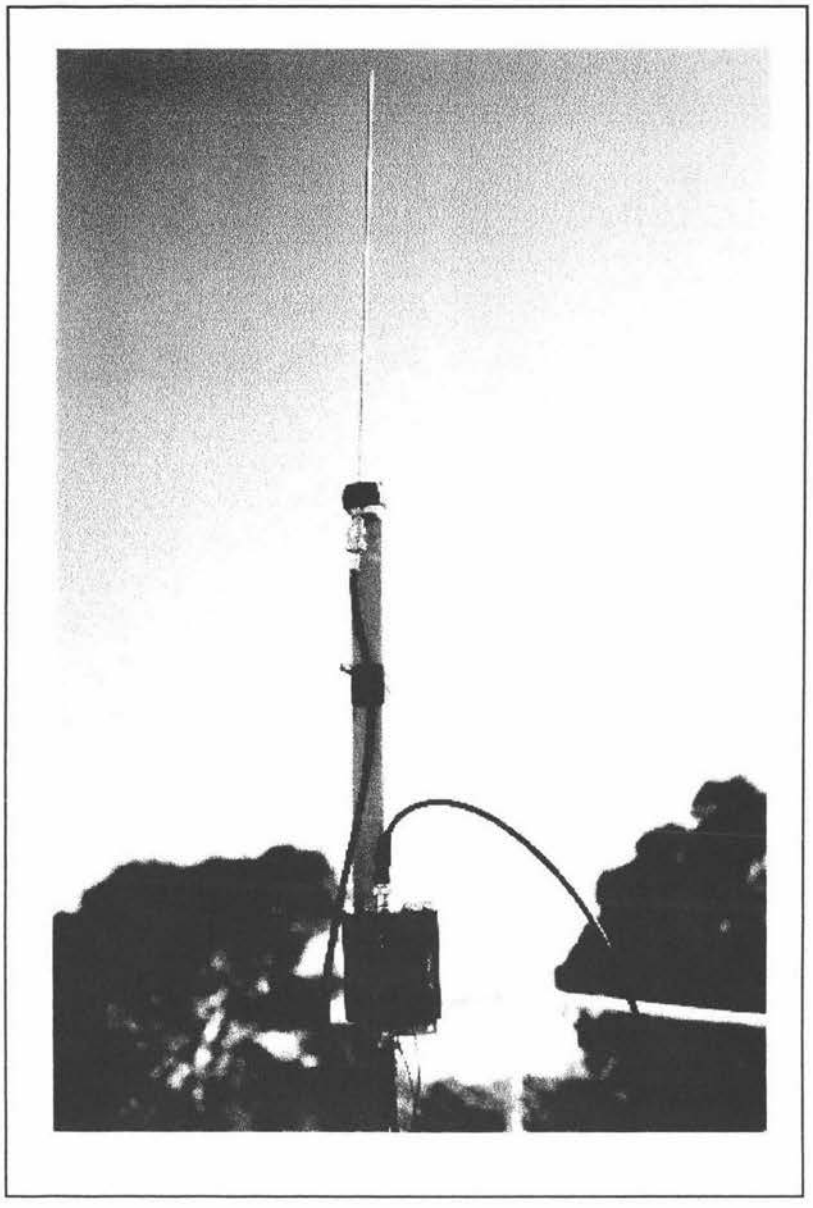


Figure 9.2. The 10W transmitting antenna. This was moved around the circle in 7.8m steps.

9.2. Data Collection.

The control program developed previously was designed for operating a working antenna but it is not suited to testing an antenna. To test the antenna, a second very simple program was implemented. This program required the user to input a 'phase step'. The program initially sets all the phase control voltages to zero. When the antenna's power pattern is measured the program increments the phase by the phase step, the process was then repeated (the program is included on the diskette on the inside of the back cover).

To measure the power pattern the carrier was modulated at 5.8 kHz. The strength of the signal was measured by noting the value of the power spectral density function at 5.8 kHz. The power spectral density function is found using a Macquisition unit and supporting software. Macquisition is a commercial data

acquisition system for Macintosh computers. The software will display time based data and, through the use of fast fourier transforms, the power spectral density function. Automated data collection was not possible as the Macquisition application does not save all the data it receives. When Macquisition saves, transient data (or sharp peaks in this case) are often omitted.

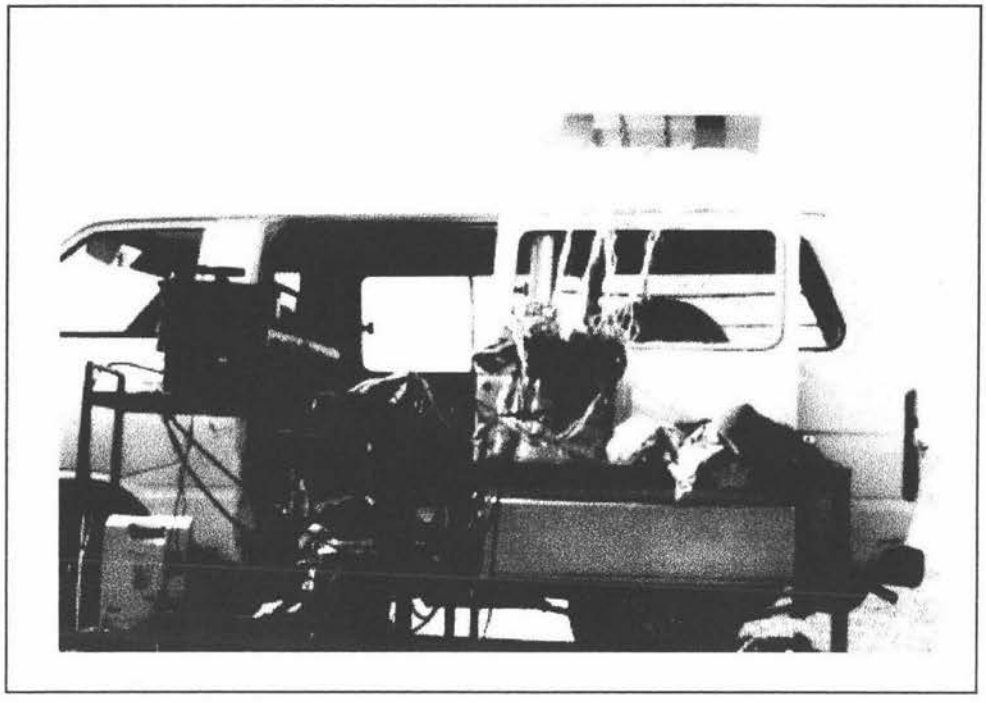


Figure 9.3. The receiving array and the receiving station. The electronic equipment is on the trolley. A portable generator was used to supply power.

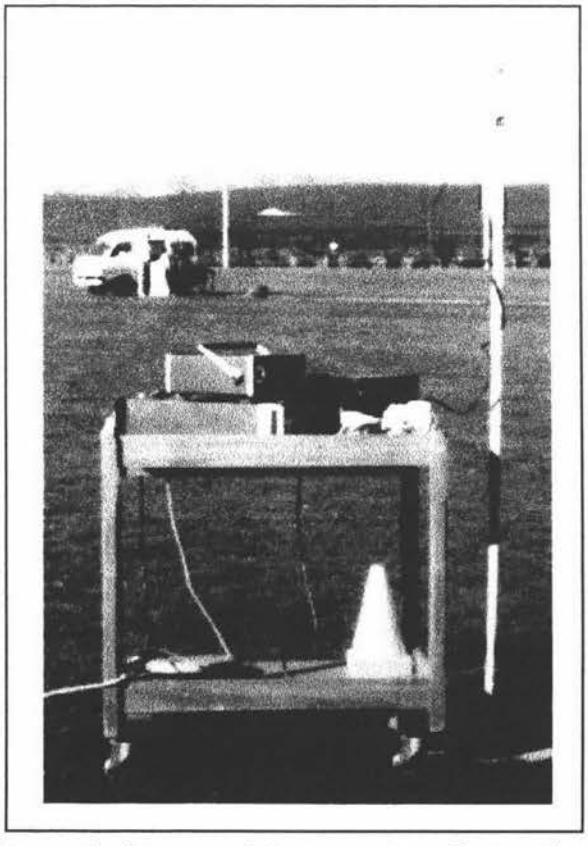


Figure 9.4. View of the receiving station from the transmitter, illustrating the scale involved.

Chapter 10
Observations.

10.1 Field Observations.

The antenna power pattern was measured for 6 phase combinations. The first measurement was made with 0V across the PIN diodes (see figure 3.12). According to figure 3.14 this establishes a phase shift of -30° between adjacent elements. The phase shift along the x axis (see figure 7.1) of the array was then decreased to 0° and finally increased 25°. The phase shift along the y axis was held constant. The phase shift on the x axis was returned to -30° while the phase shift on the y axis was varied through the same steps. Finally the antenna power pattern was measured for zero phase shift along each axis (see table 10.1). The results from these tests are shown in figures 10.1 through 10.6.

y \ x	-30°	0°	-25°
-30°	✓	✓	✓
0°	✓	✓	X
25°	✓	X	X

Table 10.1. This table indicates the different phase combinations for which the field pattern was measured. The boxes marked with an X are phase combinations that were excluded

As expected the radiation pattern changes significantly as the phase shift between adjacent elements is changed. In order to understand what is happening the radiation pattern was simulated using a Macintosh computer. Three simulation programs have been written and each simulates the antenna with a varying degree of sophistication. The programs are written in Pascal and C using Think Pascal V4.0 and Think C V6.0 for Macintosh. Two languages were used as some of the C functions were corrupted while writing the programs. The program listings and comments are included on the diskette located on the inside of the back cover.

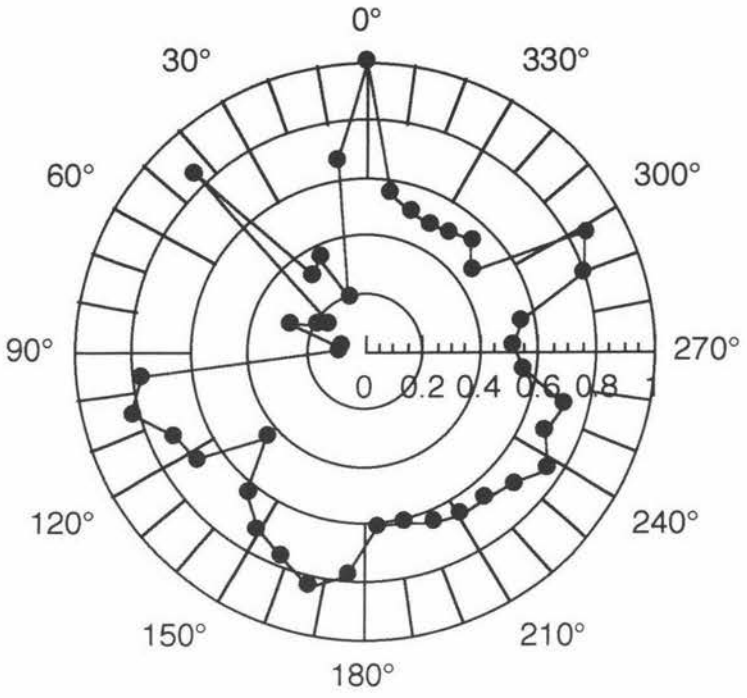


Figure 10.1. Power received indicated by the length of the radius on a linear scale. The antenna has a phase shift of -30° between adjacent elements along each axis (figure 10.2 shows how the x and y axis relate to these patterns). The pattern is "pseudo planar isotropic" that is the major lobe has no marked orientation in the plane.

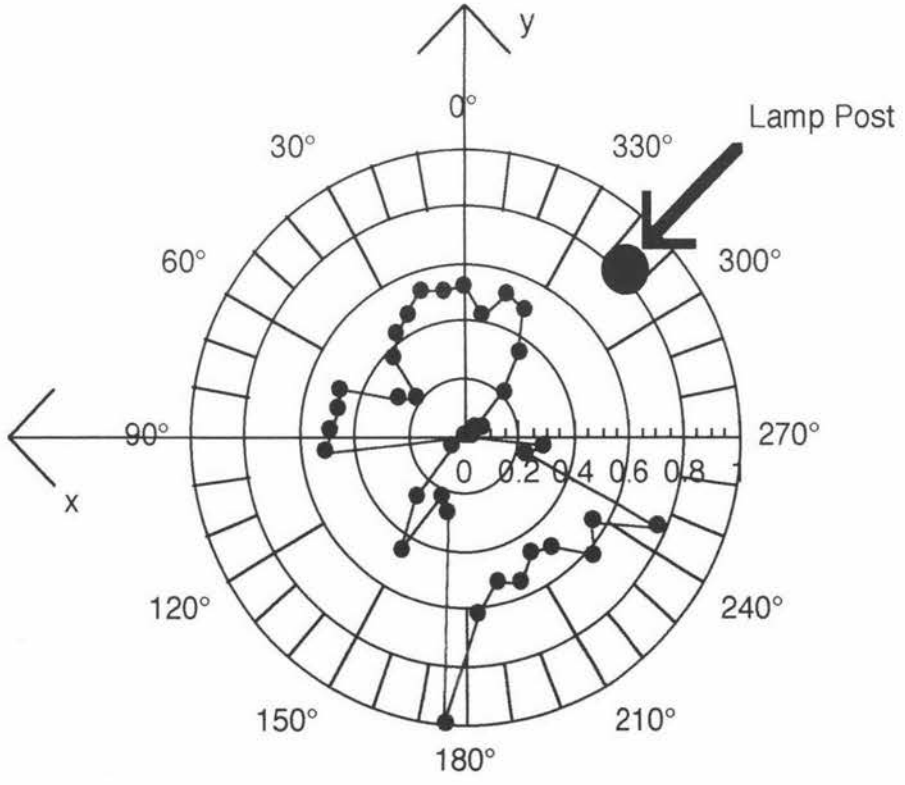


Figure 10.2. The antenna has no phase shift along the x axis and a -30° phase shift imposed along the y axis. The pattern is "pseudo broadside". Overlaid are the x and y axis. The position of the lamp post is shown also. Although the lamp post is not shown in the other power patterns it affected all the power patterns

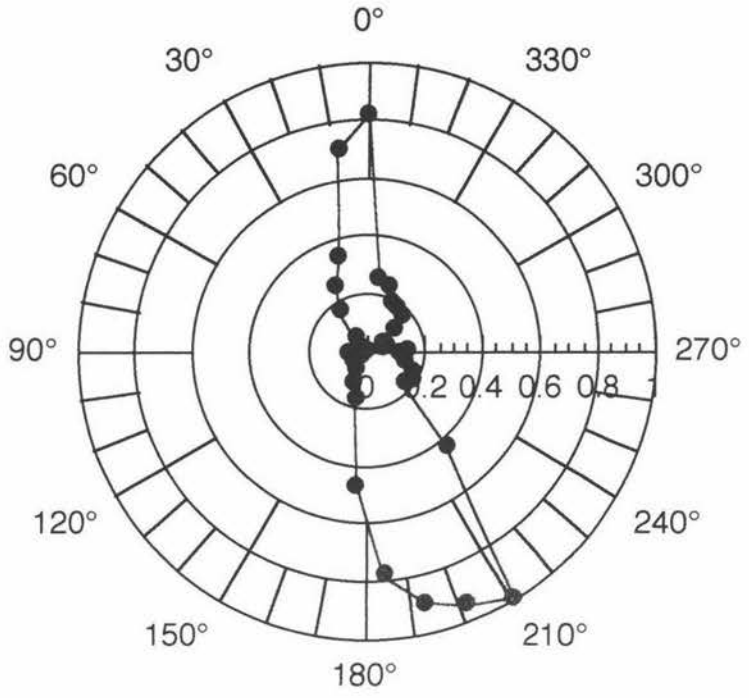


Figure 10.3. The elements along the x axis have a 25° phase shift between them while the y axis elements have a -30° phase shift imposed. The antenna pattern is similar to that of figure 10.2 but the major lobes are narrower.

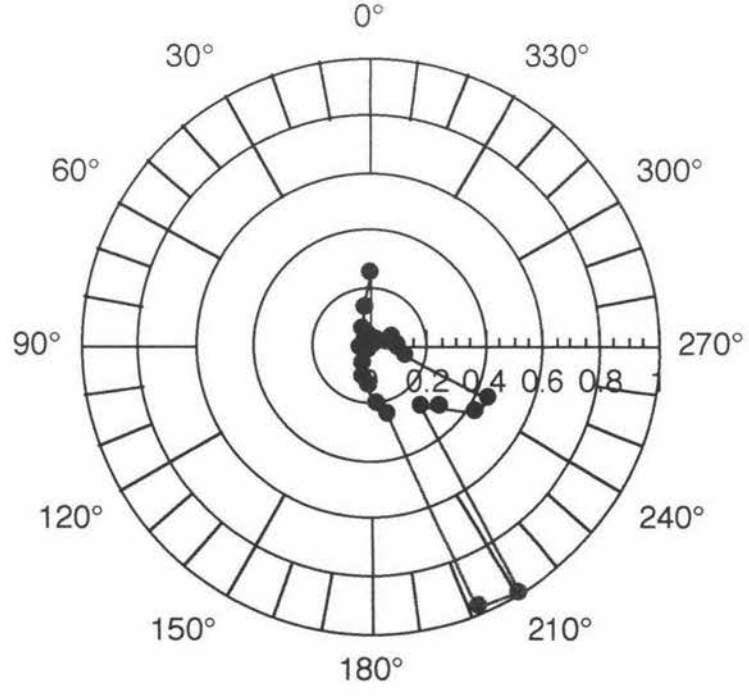


Figure 10.4. The elements have a -30° phase shift along the x axis and no phase shift along the y axis. The pattern is now "pseudo end fire" with a narrow major lobe.

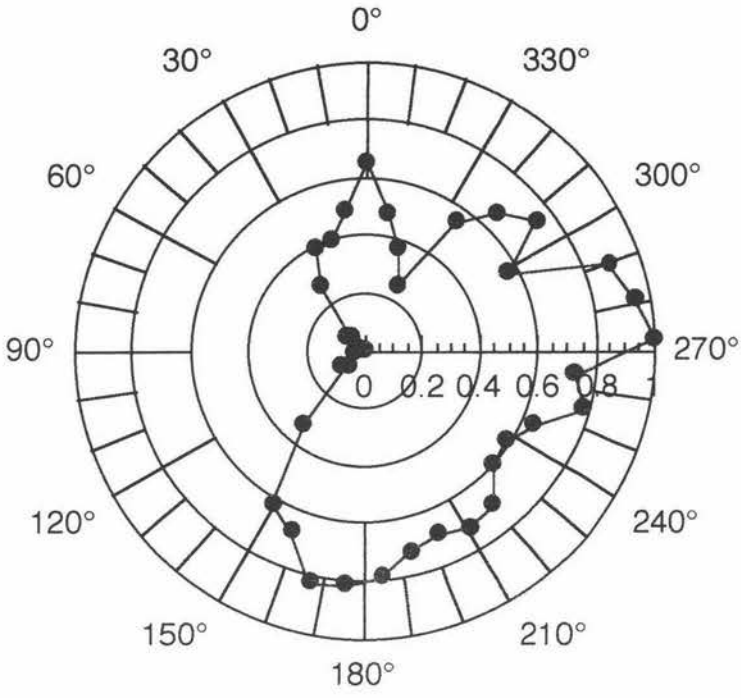


Figure 10.5. The elements have a -30° phase shift imposed along the x axis and a 25° phase shift imposed along the y axis. The pattern is wide "pseudo end fire".

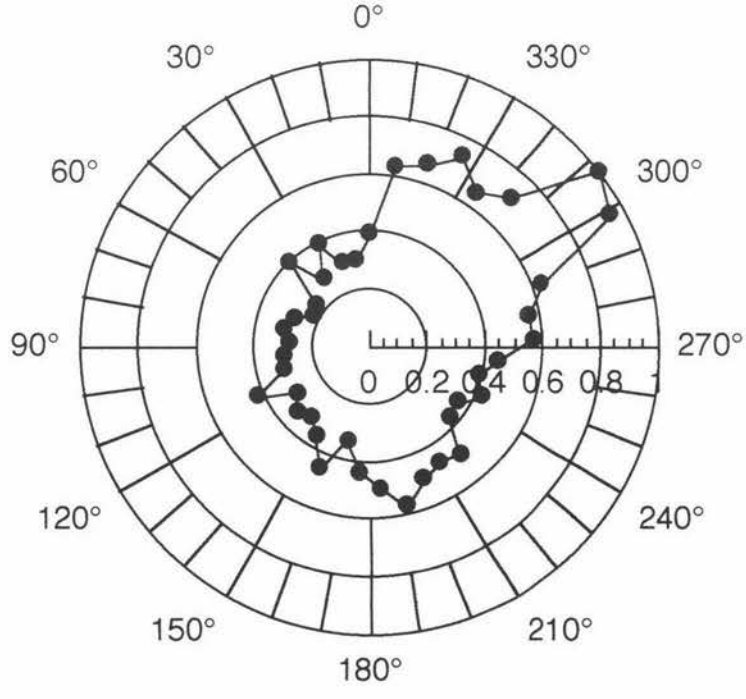


Figure 10.6. The elements have no phase shift imposed along either axis. The result is a "pseudo end fire" pattern along a substantially different axis from that of any of the other patterns.

10.2. A Simple Array Simulation: "The Standard Simulation".

This simulation assumes that the elements all contribute equally. The elements are isotropic and there is no coupling between them. The resulting power pattern can be found in any textbook on electromagnetism, see for example Kraus (ref. 2). The results from the standard simulation are shown in figures 10.7 and 10.8. In all the figures the simulation data is plotted in red against the field observations in blue. The standard simulation does not predict the antenna power patterns correctly because important assumptions made earlier are incorrect. A more sophisticated simulation is necessary.

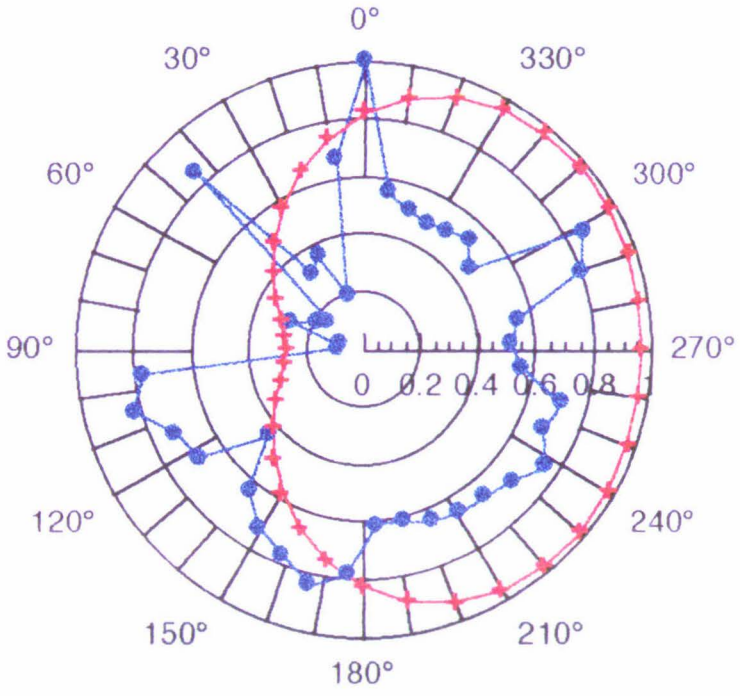


Figure 10.7. The result of a "text book" simulation (red) overlaid the field observations (blue). The imposed phase shift is -30° along both axis.

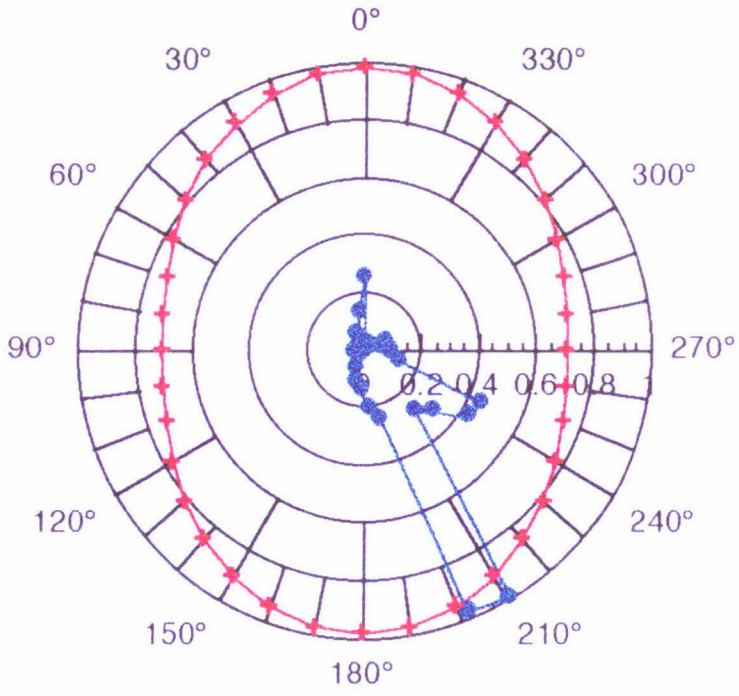


Figure 10.8. The result of a "text book" simulation (red) overlaid the field observations (blue). There is no phase shift along the x axis and a -30° phase shift between adjacent elements along the y axis.

10.3. Uncoupled Half Wave Dipole Simulation.

In this simulation the antenna elements are assumed to be half wave dipoles with unequal contributions. The relative output of an element is determined by the attenuation it suffers while passing through the phase shifter. Coupling is not considered in this simulation. The results from this simulation are shown in figures 10.9 through 10.14. There is better qualitative agreement between the field observations and the simulation. The lobes do not point in the correct direction and the side lobes are very different. To correctly predict the antenna pattern we must take into account the mutual coupling between the antenna elements. The effect of mutual coupling is to change the elements amplitude and phase. Once these phase and amplitude changes are calculated then the algorithm to calculate the antenna power pattern is the same as for the uncoupled simulation.

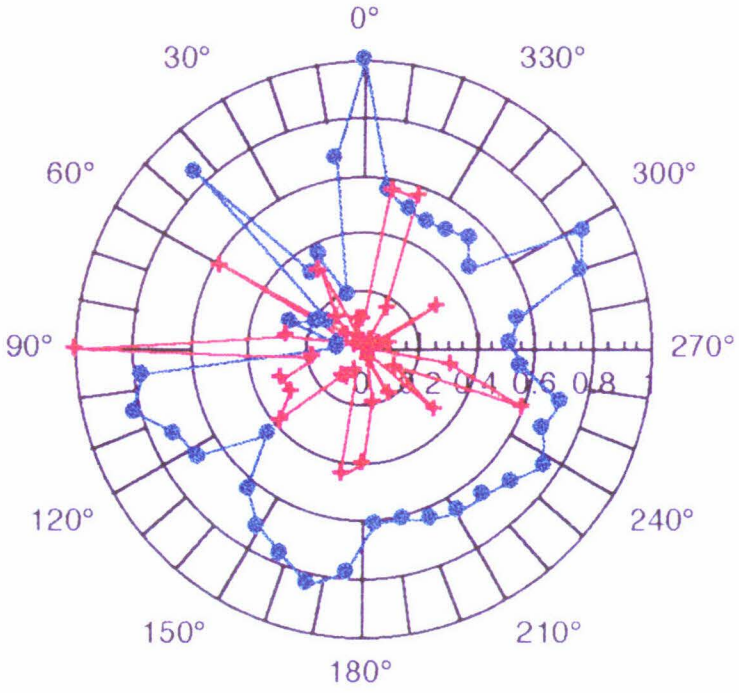


Figure 10.9. Simulation of non interacting dipoles (red) against the field observations (blue). The imposed phase shift is -30° along both axis.

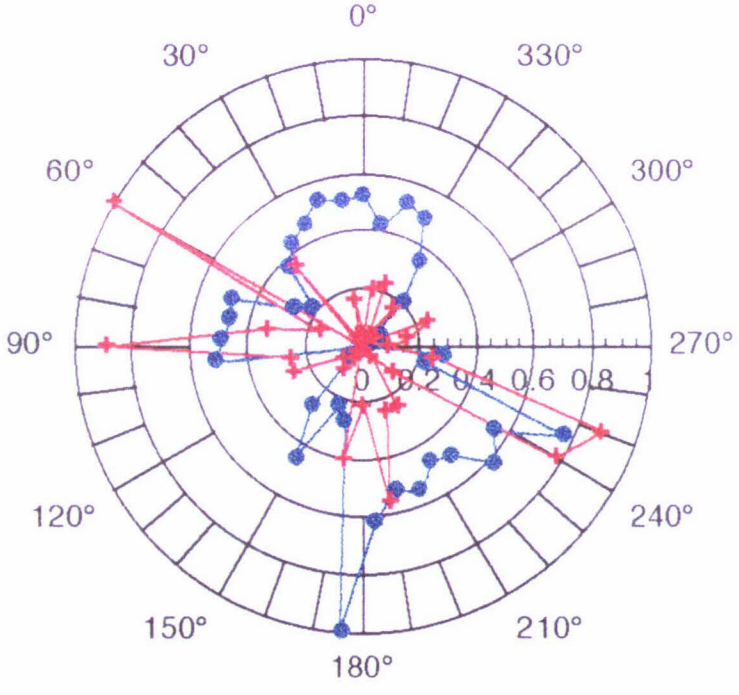


Figure 10.10. Simulation of non interacting dipoles (red) against the field observations (blue). There is no phase shift along the x axis and a phase shift of -30° imposed between adjacent elements along the y axis.

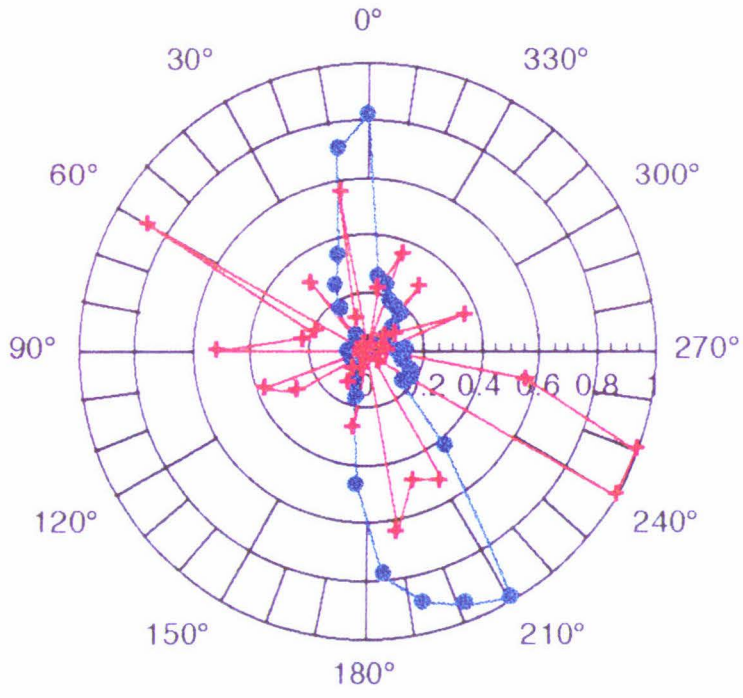


Figure 10.11. Simulation of non interacting dipoles (red) against the field observations (blue). There is a 25° phase shift imposed between adjacent elements along the x axis and a phase shift of -30° imposed between adjacent elements along the y axis.

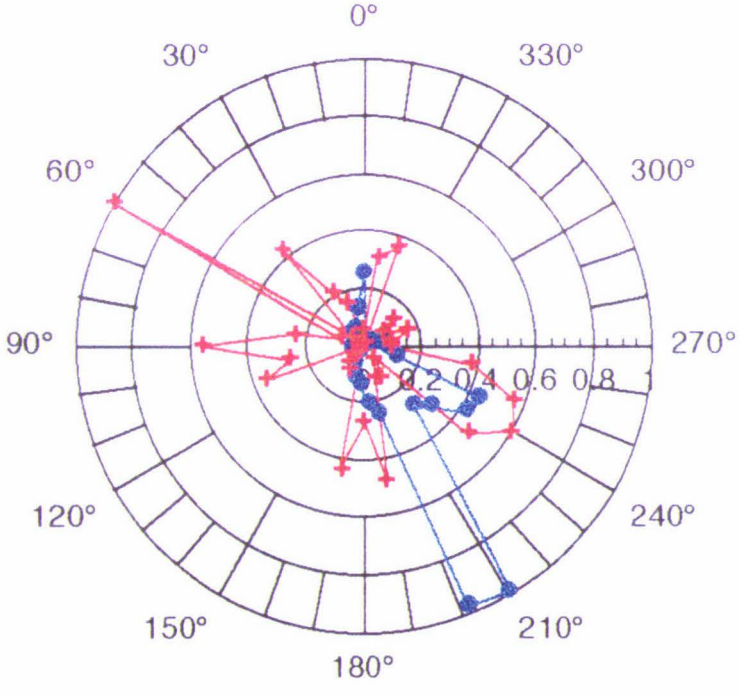


Figure 10.12. Simulation of non interacting dipoles (red) against the field observations (blue). There is a -30° phase shift imposed between adjacent elements along the x axis and a no phase shift along the y axis.

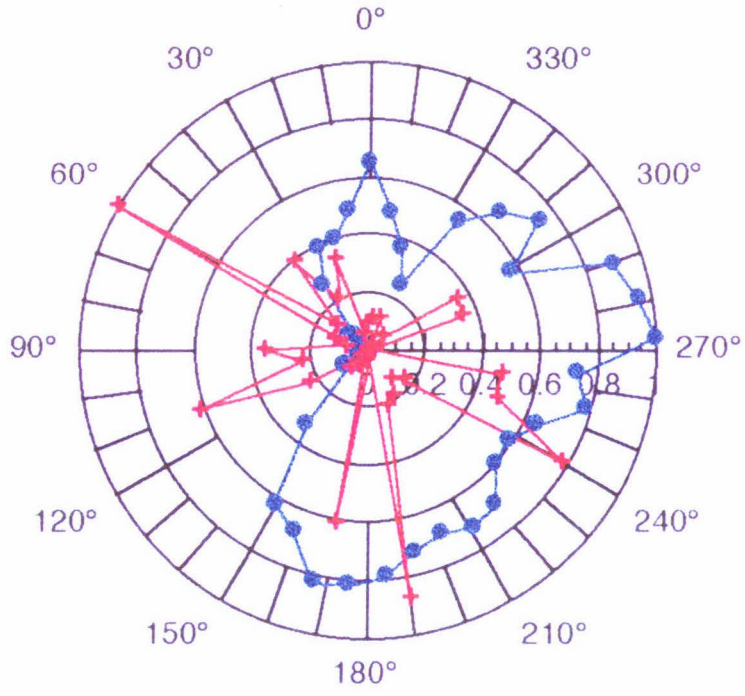


Figure 10.13. Simulation of non interacting dipoles (red) against the field observations (blue). There is a -30° phase shift imposed between adjacent elements along the x axis and a phase shift of 25° imposed between adjacent elements along the y axis.

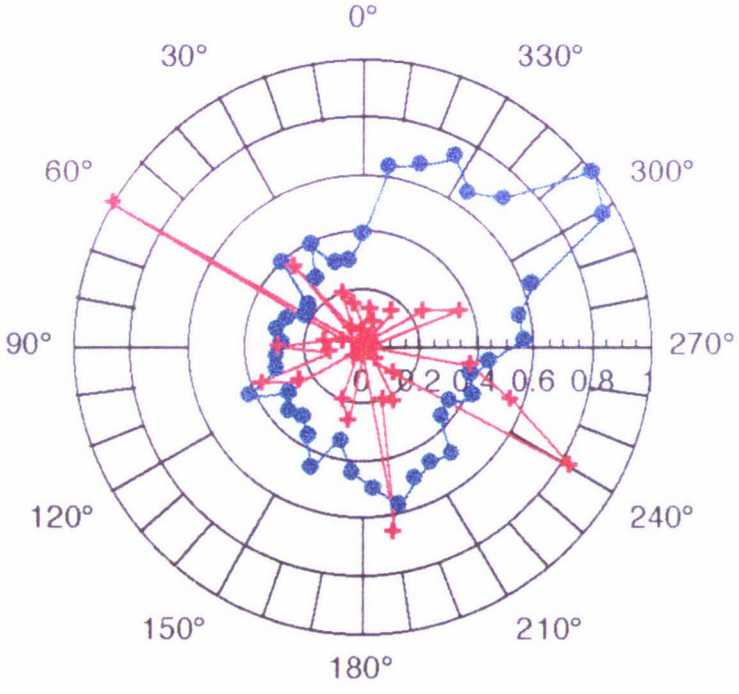


Figure 10.14. Simulation of non interacting dipoles (red) against the field observations (blue). There is no phase shift along either axis.

10.4. Fully Coupled Dipole Simulation.

The final simulation makes very few assumptions about the antenna. The elements are half wave dipoles with unequal contributions, they are also coupled together. The phase shifter is assumed to be unaffected by the coupling between the elements (it is buffered by the attenuators). The program is given initial phases and amplitudes, the program then uses the known mutual impedance (see equations 1.h, j and k) between the elements to calculate the phase and amplitude of all the elements. With the new phase and amplitudes calculated the uncoupled algorithm can be used to calculate the antenna power pattern.

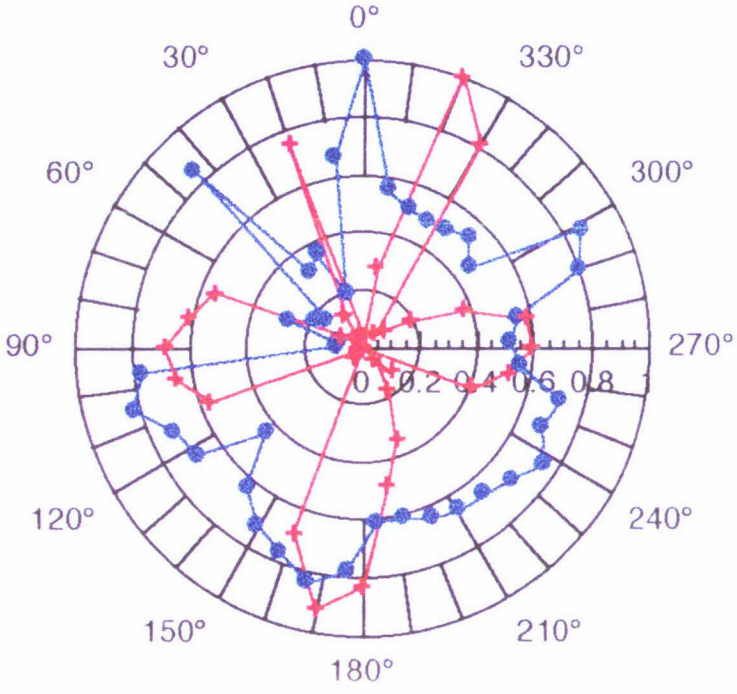


Figure 10.15. Simulation of fully coupled dipoles (red) and the field observations (blue). The imposed phase shift is -30° between adjacent elements along both axis. Notice that, although the minima are greatly exaggerated, the maxima are orientated in the correct direction. The maxima also have approximately the correct relative power.

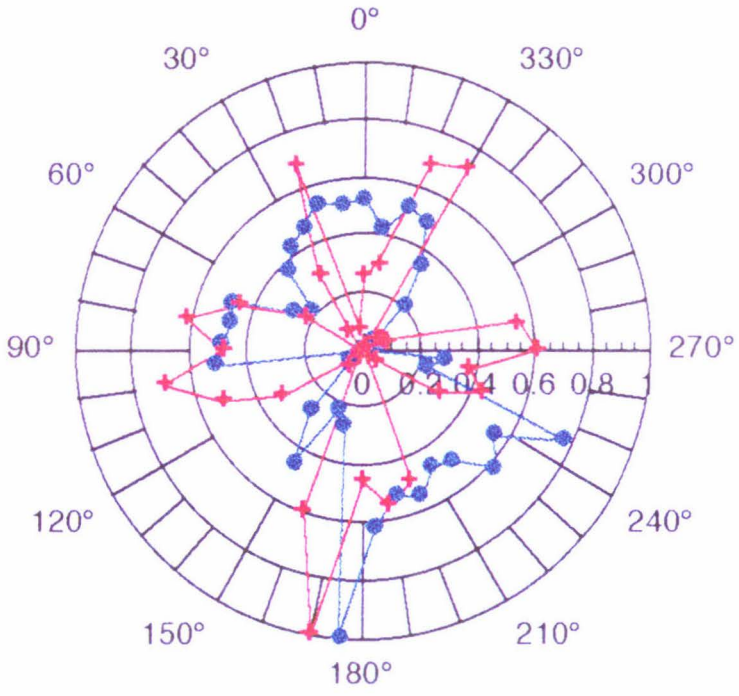


Figure 10.16. Simulation of fully coupled dipoles (red) and the field observations (blue). There is no phase shift imposed between adjacent elements along the x axis and a -30° phase shift imposed between adjacent elements along the y axis. The two patterns agree well, although the minima are exaggerated. There is a 10° systematic error between the field observations and the simulation.

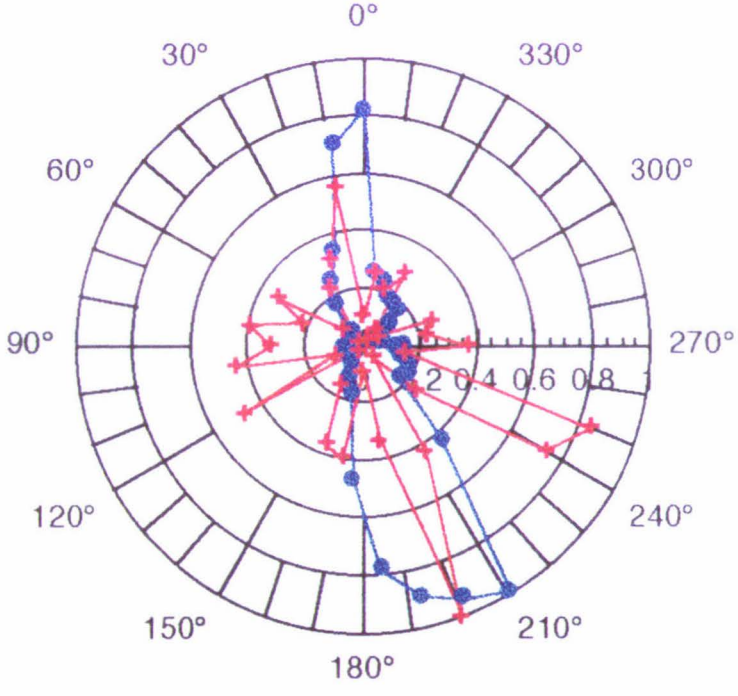


Figure 10.17. Simulation of fully coupled dipoles (red) and the field observations (blue). There is a 25° phase shift imposed between adjacent elements along the x axis and a -30° phase shift imposed between adjacent elements along the y axis. The agreement between the simulated pattern and the field observations is unremarkable.

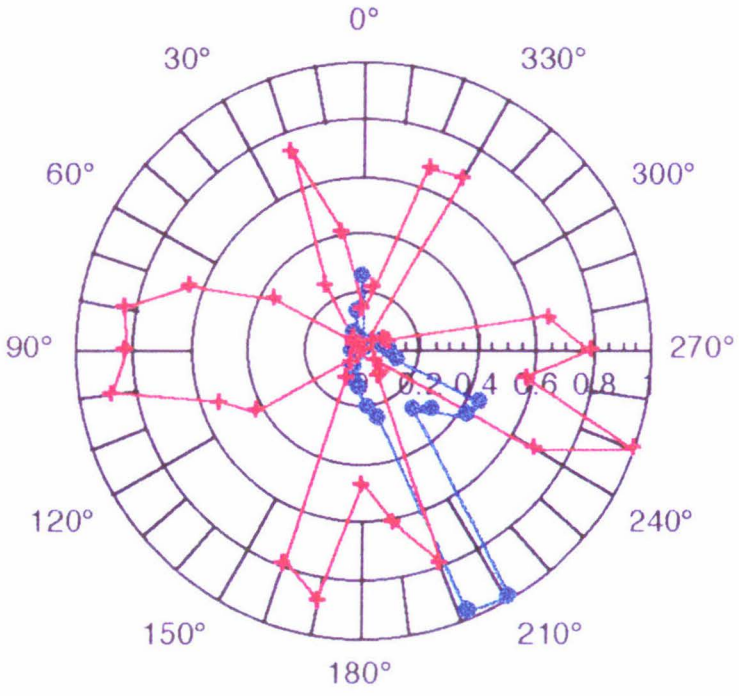


Figure 10.18. Simulation of fully coupled dipoles (red) and the field observations (blue). There is a -30° phase shift imposed between adjacent elements along the x axis and no phase shift imposed between adjacent elements along the y axis. The simulated results predict a number of side lobes that were not found in the field observations. This may be because the antenna dipoles were not perfectly parallel.

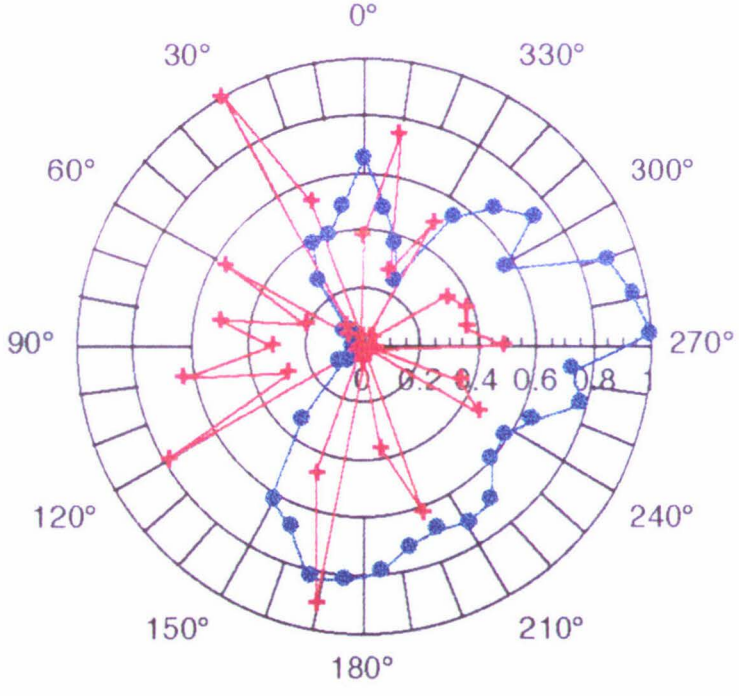


Figure 10.19. Simulation of fully coupled dipoles (red) and the field observations (blue). There is a -30° phase shift imposed between adjacent elements along the x axis and a 25° phase shift imposed between adjacent elements the y axis. The predicted fine structure was not observed and poor overall agreement.

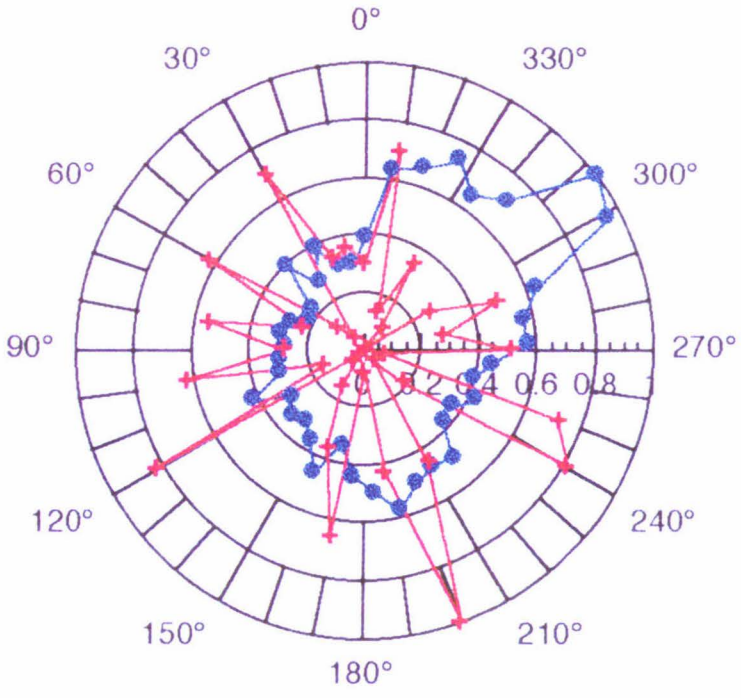


Figure 10.20. Simulation of fully coupled dipoles (red) and the field observations (blue). There is no phase shift imposed between adjacent elements. The simulation results are very different from the field observations. This may be due to the 0° degree phase shift. The major radiation lobe would propagate directly overhead but the dipoles cannot radiate in that direction (because of their polarization) hence only side lobes are shown.

Chapter 11
Conclusion.

11.1. Conclusion.

A phased array antenna with limited phase control and very good amplitude control has been designed. This is not an electronically beam steered antenna as intended but is instead an antenna whose power pattern can be "shaped."

The antenna can not be steered as the phase control unit was only partially effective because it did not allow the phase of each element to be individually set. However one could work backwards to discover the appropriate phase shift and then impose them.

The production of an electronically beam steered array antenna would require direct phase control of each element. An iterative program to calculate the phase and amplitude for every element would be needed. The complexity of such a program would relate directly to the number of elements in the array. The computational power necessary would increase as the array increased in size.

11.2. Future Work.

The simulation programs and the program used to calculate applied phase shifts can be combined to produce predictions for the necessary phase shifts of each element. This information can be used to design a more effective phase shifter. Ferroelectric phase shifters should be pursued along with the distributed amplifier phase shifter. As digital technology becomes faster, shift registers and SAW tap lines would be worth considering.

Each of the phase shifters can be improved using the current software but to make an effective antenna both the software and interface must be redesigned. In itself this development process is a very large undertaking. However, the basic system is already functional and each development of the phase shifter can be produced with little or no change to the remaining hardware. When an effective phase shifter is constructed then the entire antenna system can be redesigned around it. All the phase shifters employed should be either frequency independent (not very likely) or adaptable to higher frequencies as this type of antenna is suited for microwave frequency operations (GHz frequency range).

The antenna itself is not a design likely to be employed in any practical phased array antenna. Development of different elements to enable steering in the azimuthal plane would be necessary. The final antenna must be physically robust and should employ a number of different element types.

Overall there is room for development at every stage of this project. An incremental development by Masters or Honours students would be ideal as any one project could be adjusted in size to meet the students requirements. Development should be pursued in such a way that well known electronic components are employed wherever possible. This will challenge the student without ranging too far outside the experience within the department.

Appendicies

A.1. Mutual Coupling.

In this section the mutual impedance between two parallel half wave dipoles will be derived. Much of this derivation can be found in Kraus (ref. 2).

The mutual impedance between two elements is defined as

$$Z_{ij} = -\frac{V_{ij}}{I_i}$$ Equation a.1

By the reciprocity theorem (see ref. 1 pg 410 - 413)

$$Z_{ij} = Z_{ji} = -\frac{V_{ij}}{I_i} = -\frac{V_{ji}}{I_j}$$ Equation a.2

The antennas are arranged as in figure a.1. Antenna, *i*, is driven by a sinusoidal current, I_i. Antenna j is an open circuit. Thus the electric field at antenna *j* is the value of the electric field due to antenna *i* at *j*, E_{ji}. The induced voltage $V_{ji} = V_{ij}$ and current $I_j = I_i$. V_{ij} is the voltage due to the self impedance of antenna *i*. The expression for this is equation 1.d. Substituting in the values for antenna j equation 1.d becomes

$$V_{ji} = \frac{1}{I_i}\int I_z E_{ji} dz$$ Equation a.3

I_j is the maximum current if the terminals are short circuited. E_{ji} is the electric field at antenna *j* due to antenna *i*. As in the case of self impedance, the current distribution along the antennas is

$$I_z = I_j \sin(\beta z)$$ Equation a.4

so equation a.3 becomes

$$V_{ji} = \int E_{ji} \sin(\beta z) dz$$ Equation a.5

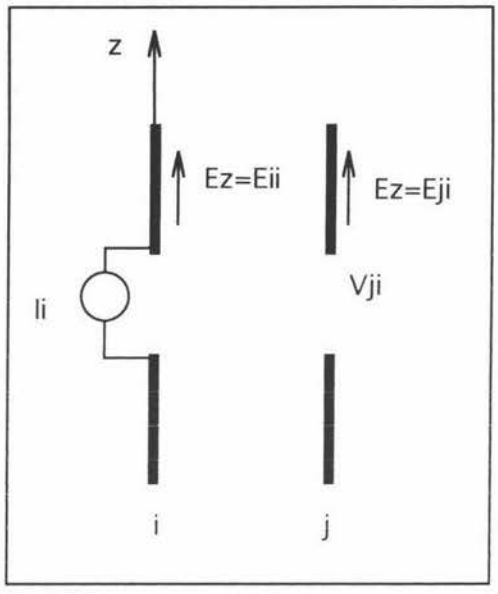


Figure a.1. Antenna, i, produces an electric field, E_{ji}, at antenna j. The voltage, V_{ji}, at the terminals of antenna j is due to E_{ji}. This can be used to find the mutual impedance.

then

$$Z_{ji} = -\frac{1}{I_i}\int_0^L E_{ji}\sin(\beta z)dz \qquad \text{Equation a.6}$$

This is a general expression for the mutual impedance due to two thin linear parallel, centre-fed antennas with a sinusoidal current distribution. We are interested in the case where both antenna are of length λ/2, parallel and separated by a distance, d (see figure a.2).

E_{ji} is given by equation 1.f, where

$$r_1 = \sqrt{d^2 + z^2} \qquad \text{Equation a.7}$$

$$r_2 = \sqrt{d^2 + (L-z)^2} \qquad \text{Equation a.8}$$

Substituting equations a.7 and a.8 into equation 1.f, the mutual impedance becomes

$$Z_{ji} = j30\int_0^L \left\{ \frac{e^{-j\beta\sqrt{d^2+z^2}}}{\sqrt{d^2+z^2}} + \frac{e^{-j\beta\sqrt{d^2+(L-z)^2}}}{\sqrt{d^2+(L-z)^2}} \right\}$$

Equation a.9

It has been shown[1] upon integration, that equation a.9. becomes

$$Z_{ji} = 30\left\{2Ei(-j\beta d) - Ei\left[-j\beta(\sqrt{d^2+L^2}+L\right] - Ei\left[-j\beta(\sqrt{d^2+L^2}-L\right]\right\}$$

Equation a.10

where

$$Ei(\pm jy) = Ci(y) \pm jSi(y)$$

Equation a.11

ie

$$R_{ji} = 30\left\{2Ci(\beta d) - Ci\left[\beta(\sqrt{d^2+L^2}+L\right] - Ci\left[\beta(\sqrt{d^2+L^2}-L\right]\right\}$$

Equation a.12

$$X_{ji} = -30\left\{2Si(\beta d) - Si\left[\beta(\sqrt{d^2+L^2}+L\right] - Si\left[\beta(\sqrt{d^2+L^2}-L\right]\right\}$$

Equation a.13

Ci(x) and Si(x) are

$$Ci(x) = \int_0^x \frac{\cos v\,dv}{v}$$

Equation a.14

$$Si(x) = \int_0^x \frac{\sin v\,dv}{v}$$

Equation a.15

Instead of numerically integrating these some simplifications can be made[1].

When x is small (x<0.2),

$$Ci(x) \approx 0.557 + \ln x$$

Equation a.16

When x is large ($x>1$),

$$Ci(x) \approx \frac{\sin x}{x}$$ Equation a.17

For Si(x) similar simplifications can be made.

When x is small ($x<0.5$),

$$Si(x) \approx x$$ Equation a.18

When x is large ($x>1$),

$$Si(x) \approx \frac{\pi}{2} - \frac{\cos x}{x}$$ Equation a.19

These simplifications can be used to shorten the algorithm used to calculate the mutual impedance of each element. If they are not used then a numerical method such as Eulers' or Gaussian integration must be employed.

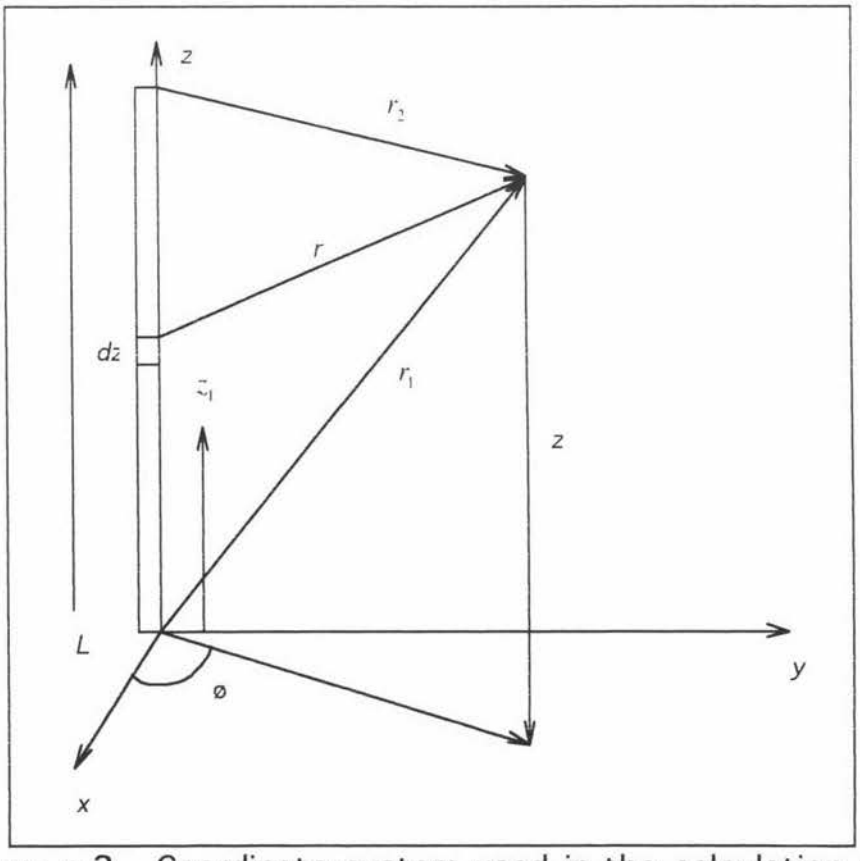
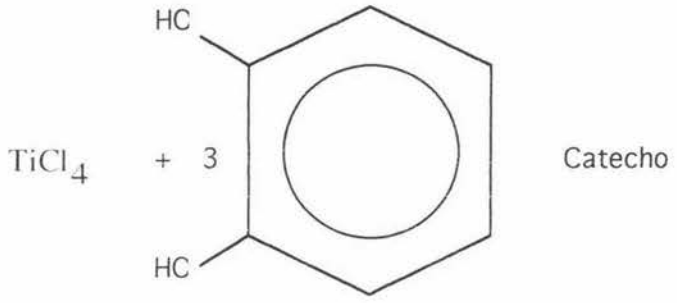


Figure a.2. Coordinate system used in the calculation of the mutual impedance.

A.2 Production of BST Powder.

The production of BST powders VIA a wet chemical route was outlined briefly in Chapter 2. The details of this method come from M. Daglish (ref. 12).

Catechol reagent (0.6 moles) was dissolved in boiling toluene (500 ml). Titanium chloride (0.2 moles) in toluene (30 ml) was added dropwise to the catechol solution whilst stirring in a reflux apparatus. A dark red precipitate formed. Heating was continued for 45 minutes after all the titanium chloride had been added. The solution was filtered under suction and washed thoroughly with hot toluene. The precipitate was then dried in a vacuum oven. The chemical process is summarised below.



refluxing in dry toluene

$$\longrightarrow \quad H_2Ti(C_6H_4O_2)_3\downarrow + 4HCl$$

Barium carbonate was suspended in distilled water and heated until it boiled. The titanium complex formed in the previous reaction was added in small batches (~1g). The reaction yielded an aqueous solution of $MTi(C_6H_4O_2)_3$.

$$H_2Ti(C_6H_4O_2)_3 + MCO_3$$

$$\longrightarrow \quad MTi(C_6H_4O_2)_3 + H_2O + CO_2$$

rotation - dry

$$MTi(C_6H_4O_2)_3.xH_2O$$

The solution was allowed to cool. The liquid was filtered to remove the excess barium carbonate. The liquid was dried by rotation drying. The resultant contains an unknown amount of water but nothing can be done about this.

The process above is repeated using strontium carbonate in place of barium carbonate. The two powders were then mixed in the desired molar ratio as aqueous solutions. The aqueous solution was rotation dried. The dried product was then heated to 700°C for 2 hours to calcine the powder.

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