Integrated Power Amplifier and Antenna-on-Chip for 5G Communication Applications

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ABSTRACT

With the advent of 5G cellular networks, there is a crucial requirement for wireless hardware operable at microwave and millimeter-wave (mmW) frequencies. Two significant elements of wireless hardware are Power Amplifier (PA) and Antenna. An integrated power amplifier designed for 5G communications is expected to offer maximum performance in terms of efficiency, output power, and/or gain. An On-Chip Antenna design would require features like simple geometry, a small form factor, free from the risk of micro-fracture, and cost-effectiveness.

Among different classes of PAs, the Class-F^{-1} amplifier is selected because it offers relatively better output power and efficiency. Different techniques are utilized in this work to enhance the performance parameters of the Class-F^{-1} PA, designed at the 5G-millimeterwave frequency of 38-GHz. In order to achieve high gain, a two-stage topology of Class-F^{-1} PA is employed. For the purpose of obtaining high output power, a stacking structure is established in the final stage of the two-stage topology. Class-F^{-1}-based parasitic-aware harmonic-control loading is employed to improve the efficiency of the power amplifier. Therefore, a two-stage Class-F^{-1} power amplifier with a double-stacked configuration is designed and fabricated. GlobalFoundries 8HP 130nm SiGe-BiCMOS process technology is utilized for realizing the integrated mmW power amplifier. A Figure of Merit (FoM) is calculated for comparing the performance of the designed power amplifier with other mmW amplifiers reported in the literature. It is observed that the proposed two-stage double-stacked Class-F^{-1} PA shows comparatively the highest FoM (69.68) achieved so far in state-of-the-art silicon-based Class F/F^{-1} power amplifiers.

Another integrated Class-F^{-1} power amplifier is proposed at a new unlicensed 5G-microwave frequency of 6-GHz. The PA is designed to achieve very high power-efficiency. The amplifier employs a "single-transistor" design in 65-nm standard CMOS process technology. The PA is loaded with a Class-F^{-1} harmonic-control network, employing a new parasitic-aware topology deduced using a novel iterative-algorithm. The proposed algorithm starts from a specific reference value and quickly converges towards the solution. A dual-purpose output-matching circuit is employed in the design. The output-matching circuit not only matches the output impedance to 50-Ω but also reinforces the Class-F^{-1} harmonic network in controlling the harmonics efficiently. The proposed amplifier offers a peak power-added-efficiency (PAE) of 47.8% which is one of the

highest when compared with previously reported microwave/millimeterwave PAs in CMOS and SiGe process technologies.

Besides power-amplifiers, another essential part of this research is On-Chip Antenna (OCA). As millimeterwave frequencies exhibit relatively smaller wavelengths, it becomes feasible to design an antenna on a microchip using standard CMOS processes. As compared to Off-Chip Antennas, the On-Chip Antennas offer a high level of integration with RF-front-end circuitry, as well as an external interconnect-free interface and low fabrication cost. An On-Chip Planar-Inverted-F Antenna (PIFA) in TSMC 180-nm CMOS is designed to radiate at the 5G-millimeterwave frequency of 38-GHz. A PIFA is selected because it offers simple geometry, small form factor, design flexibility, and robustness. An Ultra-Thick Metal (UTM) layer in 180-nm CMOS is utilized to implement the antenna structure on the chip. To achieve better radiation performance, the OCA is positioned close to the edge of the microchip. The measurements are conducted after placing the fabricated OCA over a 3D-printed plastic-slab to minimize the reflections from the metallic-chuck of the probe-station. The fabricated OCA delivered an antenna-gain of 0.7-dBi at the millimeterwave center-frequency of 38-GHz.

Keywords: Integrated power amplifier, microwave integrated circuits, millimeterwave integrated circuits, class-F/F^{-1}, stacking, 5G, microwave / millimeterwave frequency, on-chip antenna, planar inverted-F antenna (PIFA), cellular communications.

AUTHOR’S DECLARATION

This thesis is produced with three research articles according to Massey University’s “Ph.D. thesis by publication” guidelines. The thesis is based on research that has been published. One research article is published in *IEEE Transactions on Microwave Theory and Techniques,* the second article is published in *Electronics,* and the third article is published in the *International Journal of Antennas and Propagation*. IEEE does not require individuals working on a thesis to obtain a formal reuse license and the other two journals are open-access journals. The presented content is identical to the published version of the articles however, the thesis-version has formatting differences for maintaining the uniformity in the thesis.

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LIST OF ACRONYMS

AM	Amplitude Modulation
AMC	Artificial Magnetic Conductor
AUT	Antenna Under Test
BEOL	Back End Of Line
BiCMOS	Bipolar Complementary Metal Oxide Semiconductor
BV	Breakdown Voltage
CBEBC	Collector Base Emitter Base Collector
CMOS	Complementary Metal Oxide Semiconductor
CPW	Co-Planar Waveguide
DE	Drain Efficiency
DRC	Design Rule Check
FET	Field Effect Transistor
FCC	Federal Communications Commission
FOM	Figure Of Merit
GDS	Graphic Design System
GF	Global Foundries
GaAs	Gallium Arsenide
GaN	Gallium Nitride
GSG	Ground Signal Ground

HBT	Heterojunction Bipolar Transistor
IEEE	Institute of Electrical and Electronics Engineers
InP	Indium Phosphide
ITRS	International Technology Roadmap for Semiconductors
LVS	Layout versus Schematic
mmW	Millimeterwave
MMIC	Monolithic Microwave Integrated Circuit
NMOS	N-channel Metal Oxide Semiconductor
OCA	On Chip Antenna
PA	Power Amplifier
PAE	Power Added Efficiency
PDK	Process Design Kit
PIFA	Planar Inverted F Antenna
PLA	Poly Lactic Acid
PM	Phase Modulation
RF	Radio Frequency
SiGe	Silicon Germanium
TSMC	Taiwan Semiconductor Manufacturing Company
UTM	Ultra Thick Metal
WPAN	Wireless Personal Area Network

CHAPTER NO.1

THESIS OVERVIEW

1.1 Motivation

In recent years, demand for high data rate in next-era cellular communication (5G) is increasing exponentially and the current systems seem unable to cope with this upcoming level of throughput requirements. In order to deal with this challenge, "New unlicensed 6-GHz band and Millimeterwave frequencies" in the electromagnetic spectrum have been offered to academic and commercial sectors for research and system production. The Federal Communications Commission (FCC) has recently opened an unlicensed 6-GHz band ranging from 5.925 GHz to 7.125 GHz [1]. This new 6-GHz band resides in the realm of "Microwave-frequencies" focused on establishing 5G communications. Whereas millimeterwave frequencies start from 30 GHz and rise up to 300 GHz. From the perspective of wireless communication, the term "Millimeterwave" (mmW) corresponds to a few bands of the electromagnetic spectrum that includes Ka-band (27−40 GHz), V-band (59−64GHz), and E-band (71−76 GHz and 81−86 GHz). As far as 5G-communication is considered the frequencies of interest are 28-GHz ([2], [3]), 38-GHz [4] and 60-GHz ([5], [6]).

Traditionally, microwave and millimeterwave integrated circuits have been designed in III-V compound semiconductor technologies like GaAs and InP because these technologies offer superior performance in comparison with silicon-based technologies. The III-V compound semiconductor devices offer higher mobility and higher breakdown voltage than silicon devices thereby yielding higher output power. However, the main drawback of these compound semiconductor technologies is their extremely high cost. As microwave/millimeterwave integrated circuits or systems designed for 5G communication applications have to be produced in bulk quantity, therefore, the cost is a key factor in avoiding these fabrication technologies. In contrast, silicon-based fabrication technologies like CMOS and SiGe (Silicon-Germanium) offer high yield, high levels of integration, and low fabrication/end-user cost.

In order to realize 5G cellular communication, there is a crucial demand for high-performance microwave/millimeterwave hardware. The analog section of the communication hardware includes an oscillator, mixer, power amplifier and antenna. Among all of these hardware modules, the power amplifier is the most power-hungry module, which consumes power from the system's battery. Hence, in order to design efficient communication hardware, it is necessary to focus on improving the efficiency of the power amplifier. Moreover, the battery life in portable devices can be extended by designing a power amplifier that demonstrates a high power-efficiency ([1], [7]). Furthermore, designing an antenna on the CMOS platform is necessary for realizing a fully integrated RF system. An integrated RF system does not exhibit circuit-to-antenna interface losses and hence is more efficient. Moreover, as such a system is fabricated on the same CMOS platform, therefore, it is cost-effective as well. Hence, compared to Off-Chip Antenna, an On-Chip Antenna offers a high level of integration with RF-front-end circuitry, as well as an external interconnect-free interface and low fabrication cost [8]. This work specifically investigates Power-Amplifiers operable at microwave and millimeterwave frequencies of 6-GHz and 38-GHz respectively and Antenna-on-Chip radiating at 5G millimeterwave frequency band of 38-GHz.

1.2. Research Goals

The research goals of this thesis are described as follows:

- ***Integrated Millimeterwave Power Amplifier:*** The main aim of this research section is to investigate, design and implement a switching power amplifier showing optimum performance in terms of gain, output power and efficiency by utilizing 130-nm SiGe BiCMOS 8HP technology. The goal specifically is to obtain the highest Figure-of-Merit (FoM – a performance evaluation metric) as compared to previously reported FoMs of the power-amplifiers in CMOS and SiGe process technologies. Moreover, the focus is on developing generalized methods/techniques to increase the FoM of a power amplifier.

- ***Integrated Microwave Power Amplifier:*** The main objective of this part of the research is to investigate, design and implement a very high-efficiency CMOS-based power amplifier. While attempting to considerably enhance the Power-Added-Efficiency (PAE), it is imperative to make sure that the amplifier's other parameters like output power, etc. are

not significantly compromised and reside within the practically acceptable limits. Once again, the focus is on developing generalized methods/techniques to increase the PAE of a power amplifier.

- ***Millimeterwave On-Chip Antenna (OCA):*** The main aim of this segment of the research is to investigate an On-Chip Antenna (OCA) that is best-suited for 5G communication at the millimeterwave center-frequency of 38-GHz. The essential tasks are to seek the appropriate antenna type offering a small form-factor and to propose a geometrically simple antenna structure. Moreover, some techniques to reduce the absorption of electromagnetic radiation within the silicon substrate can also be investigated.

1.3 Thesis Organization

The thesis is organized as follows:

- **Chapter 2:** This chapter initially presents an introduction to power amplifiers and their classifications, especially emphasizing Class F/F^{-1} power amplifiers. Then, the chapter illustrates SiGe BiCMOS technology and the stacking mechanism of Heterojunction Bipolar Transistors (HBTs). Afterwards, this chapter introduces antennas, their types and the fundamental parameters of antennas. The last section of the chapter presents a literature review of millimeterwave power amplifiers, microwave power amplifiers and millimeterwave on-chip antennas.

- **Chapter 3:** This chapter reports a 38-GHz millimeterwave double-stacked HBT Class-F^{-1} power amplifier in 130-nm SiGe-BiCMOS process technology. The chapter describes in detail the new parasitic-aware Class-F^{-1} topology and the techniques employed to achieve the highest Figure-of-Merit (FoM).

- **Chapter 4:** This chapter reports a 6-GHz integrated high-efficiency Class-F^{-1} power amplifier in 65-nm CMOS process node. The chapter explains in detail the 'single-

transistor' approach and novel iterative algorithm-based Class-F^{-1} circuitry employed to design the high-efficiency power amplifier at 5G-microwave frequency.

- **Chapter 5:** This chapter reports an on-chip planar inverted-F antenna in 180-nm CMOS for 5G communication applications. The contents of the chapter describe the details of the implemented CMOS technology and the design of the proposed on-chip antenna along with the layout challenges.

- **Chapter 6:** The chapter concludes the PhD-research-work and outlines directions for future work.

References:

[1] Federal Communications Commission, (2020, Apr. 2), *FCC Fact Sheet: Unlicensed use of the 6-GHz band*. [Online], Available: https://docs.fcc.gov/public/attachments/DOC-363490A1.pdf (accessed on Apr. 06, 2020).

[2] D. Shakya, D. Chizhik, J. Du, R. A. Valenzuela and T. S. Rappaport, "Dense Urban Outdoor-Indoor Coverage from 3.5 to 28 GHz," *ICC 2022 - IEEE International Conference on Communications*, Seoul, Korea, Republic of, 2022, pp. 932-937.

[3] S. Ito and T. Hayashi, "Measurement and Evaluation of 28 GHz Propagation Characteristics in Specific Environments," in *IEEE Access*, vol. 10, pp. 26242-26256, 2022.

[4] Y. Xing and T. S. Rappaport, "Millimeter Wave and Terahertz Urban Microcell Propagation Measurements and Models," in *IEEE Communications Letters*, vol. 25, no. 12, pp. 3755-3759, Dec. 2021.

[5] S. Lagen et al., "New Radio Beam-Based Access to Unlicensed Spectrum: Design Challenges and Solutions," in *IEEE Communications Surveys & Tutorials*, vol. 22, no. 1, pp. 8-37, Firstquarter 2020.

[6] F. Liu and Y. Yang, “Spectrum Efficient Coexistence Between 5G NR Unlicensed and WiGig in 60 GHz Band,” *2022 IEEE 22nd International Conference on Communication Technology (ICCT)*, Nanjing, China, 2022, pp. 1421-1425.

[7] A. Vasjanov and V. Barzdenas, “A review of advanced CMOS RF power amplifier architecture trends for low power 5G wireless networks,” *Electronics*, vol. 7, no. 271, Oct. 2018.

[8] H. M. Cheema and A. Shamim, “The last barrier: on-chip antennas,” *IEEE Mirowave Magazine*, vol. 14, no. 1, pp.79–91, Jan. 2013.

CHAPTER NO. 2

POWER AMPLIFIER AND ANTENNA: INTRODUCTION AND LITERATURE REVIEW

2.1 Introduction to Power Amplifier

Power Amplifier magnifies both the voltage and current of the input signal. It converts a weak or low-power signal into a high-power signal intended to drive specific loads like loudspeakers or transmitting antennas etc. Power-Gain and Power-Efficiency are the two important performance parameters of a power amplifier. Power-Gain of an amplifier is the ratio of output power delivered to the load to the input power fed to the amplifier. It can be represented as follows:

$$G_P = \frac{P_L}{P_{in}} \tag{2.1}$$

Where, G_P is power-gain, P_L is signal power delivered to the load and P_{in} is input power supplied to the amplifier.

Efficiency (η) of an amplifier is the ratio of output power (P_{out}) to the total power drawn from the DC supply (P_{dc}).

$$\eta = \frac{P_{out}}{P_{dc}} \tag{2.2}$$

A better figure of merit with regards to efficiency is Power-Added-Efficiency (PAE). PAE is the difference between output power and input power divided by the total power fetched from the dc supply.

$$PAE = \frac{(P_{out} - P_{in})}{P_{dc}} \tag{2.3}$$

PAE represents the ability of a PA to convert DC power into RF power. If efficiency is low, it means the power in an amplifier is not sufficiently converting into a useful signal and is being dissipated as heat.

2.2 Classification of Power Amplifiers

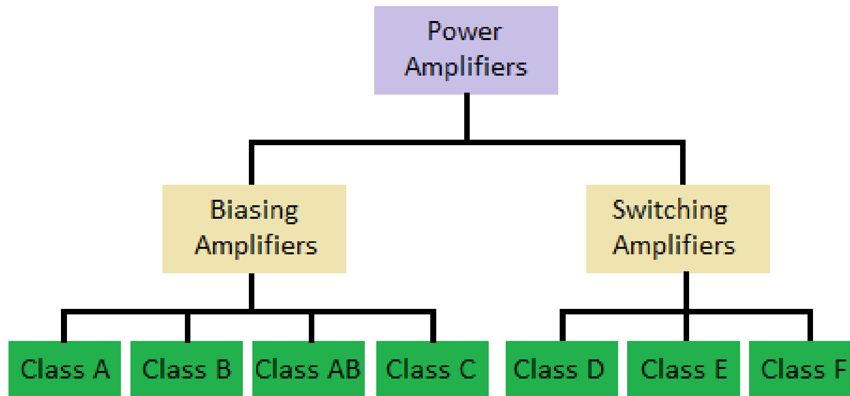


Fig. 2.1. Classification of power amplifiers.

Power Amplifiers (PAs) are classified into two major groups i.e., Linear PAs and Non-Linear PAs. If the output power produced by an amplifier is proportional to the input power, then it falls in the category of Linear Power-Amplifiers. Whereas if an amplifier's output power is not proportional to its input power then it lies within the realm of Non-Linear Power-Amplifiers.

The design of a power amplifier is based on trade-offs. There exist trade-offs between linearity, efficiency, output power and gain. Some proportion of these performance parameters are traded-off to obtain better values of some other parameters. For example, linearity is traded-off to achieve better efficiency.

Power Amplifiers are also categorized as Biasing-PAs (Linear) and Switching-PAs (Non-Linear) [1], [2]. Transistor in Biasing-PAs works as a current source but in switching-PAs, it acts as a switch. Class A, B, AB and C are examples of Biasing-Class and Class D, E and F fall in the category of Switching-Class PAs (Fig. 2.1).

Switching power amplifiers offer high Power-Added-Efficiency (PAE) as compared to biasing-PAs and therefore, are preferred over biasing class amplifiers. Among switching power amplifiers, Class F is preferred over Class D and Class E PAs. In contrast to Class F, Class D and Class E amplifiers need a square-wave input signal which demands an additional circuit to realize it. Moreover, a square-wave input signal is a fast drive signal which also increases the stress on the active device. Furthermore, as compared to Class F amplifiers, Class E amplifiers require relatively higher breakdown voltage and higher current handling of the active device. All of the above-mentioned reasons make Class F amplifiers more attractive to researchers than Class D or E power amplifiers.

2.2.1 Class F

Class F amplifier is also a member of Switching-Class amplifiers. Class F PA enhances both the output power and the efficiency with the help of a harmonic control network or harmonic resonators connected at the output of the amplifier. The harmonic network configuration of Class F amplifier shapes the voltage and current waveform at the drain / collector terminal of the active device in such a way that it short circuit even harmonics and open circuit odd harmonics. Drain voltage waveform incorporates one or more odd harmonics and transforms nearly into a square wave whereas drain current waveform includes one or more even harmonics and establishes a half-sinusoidal wave. In the case of Class F^{-1} power amplifier, the harmonic network is configured in such a way that the shapes of voltage and current waveforms are exchanged i.e., drain-voltage waveform approximates itself as a half-sinusoidal wave by open circuiting the 2nd harmonic whereas drain-current waveform approximates itself as a square wave by short-circuiting the 3rd harmonic. As there exists no overlapping of voltage and current waveforms at the drain (or collector) terminal hence, ideally Class F/F^{-1} amplifier offers 100 % efficiency.

Perfect square-wave and half-sinusoidal wave can be achieved by controlling an infinite number of even and odd harmonics and hence is impractical. Practically the most influential harmonics i.e., 2nd harmonic and 3rd harmonic are controlled. Sometimes, researchers reach up to controlling 5th harmonic, but it is not reasonable as the number of components and level of complexity increases considerably and the attempt becomes less fruitful than the efforts done.

Figure 2.3 shows a Class F amplifier in which 2nd and 3rd harmonics are controlled. Such a network configuration is called "third harmonic peaking topology". The output network consists of a parallel resonant tank (L_3C_3) which resonates at a frequency of $3f_0$ (f_0 is operating frequency). This tank is connected in series with the drain (or collector) output. It provides a short-circuit at 2nd harmonic ($2f_0$) and an open-circuit at 3rd harmonic ($3f_0$). Another parallel-tuned L_0C_0 output tank, tuned to resonate at the fundamental frequency, is connected in parallel with the load resistance. This tank only allows the fundamental frequency to pass through and stops all other frequencies. Figure 2.4 shows the ideal voltage and current waveforms at the drain terminal of the Class-F amplifier. At load resistance, the output voltage and current waveforms acquire a pure sinusoidal shape, which also remains in-phase with each other [3]-[9]. Apart from the output network shown in Fig. 2.3, many other network schemes are designed to shape the waveforms at the drain / collector terminal of the Class-F/F^{-1} amplifiers [3].

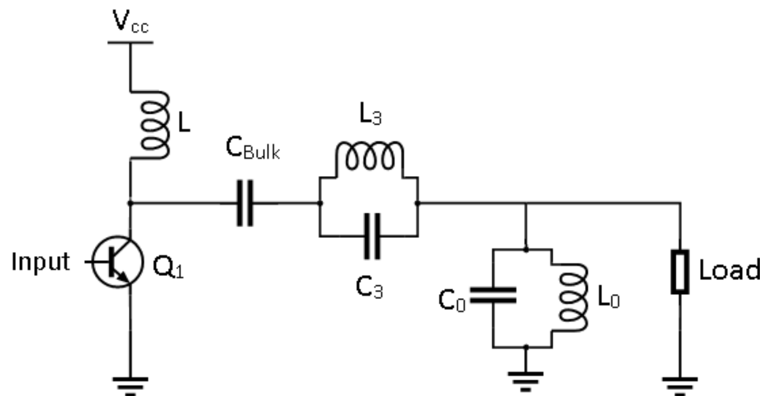


Fig. 2.2. Class F PA with third harmonic peaking topology.

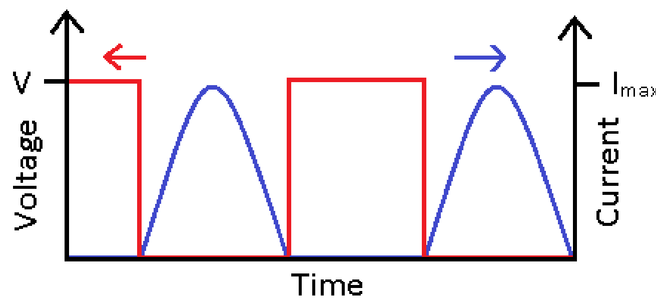


Fig. 2.3. Voltage and current waveforms at the drain terminal.

2.3 8HP SiGe-BiCMOS: An Advanced Technology

Lately, silicon-based technologies have made significant advancements. The Microelectronics industry offers SiGe-BiCMOS technology as a competitor of other semiconductor technologies like expensive III-V compound semiconductor processes. As millimeterwave-based commercial applications will be in demand in the future, therefore, due to the core advantages of cost-effectiveness and high level of RF & Digital-circuit integration the SiGe-BiCMOS technology is being viewed as the key candidate for realizing 5G-millimeterwave systems.

The core of Silicon-Germanium (SiGe) BiCMOS Technology resides in its ability to integrate analog and digital circuitry on a single chip using existing CMOS fabrication facilities. The essential element in SiGe Technology is a *SiGe Heterojunction Bipolar Transistor (HBT)* which provides considerable benefits over both conventional Si-bipolar plus Si-CMOS for realization of RF circuits on-chip [10]. SiGe HBT's performance advantages like extremely high transition and oscillation frequencies (f_T and f_{max} respectively), high-speed operation, higher breakdown voltage, high output drive capability and improved power-added efficiency (PAE) make SiGe HBTs an excellent choice for Power Amplifier applications [11].

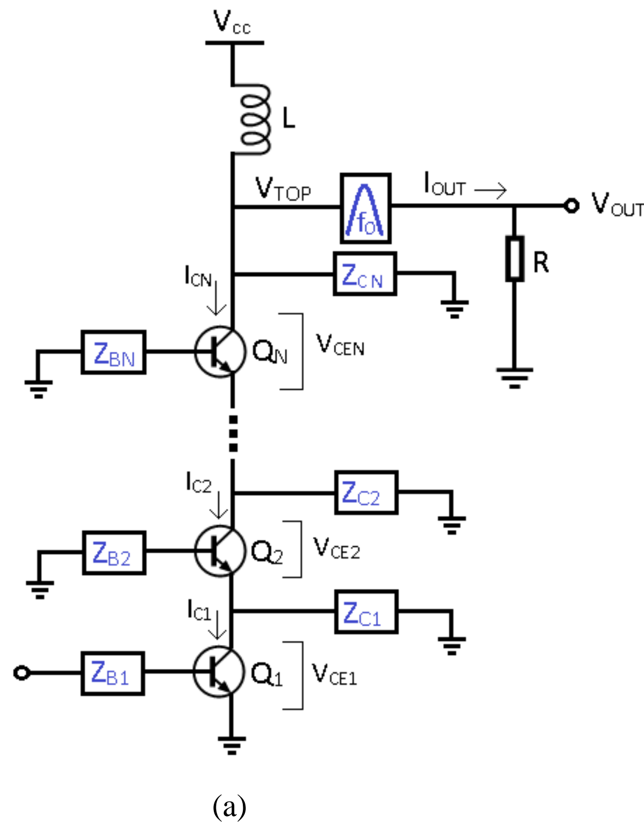
Therefore, the benefits of the SiGe-BiCMOS technology, especially the features being offered in ***130nm SiGe 8HP*** [12], motivated us to utilize this technology for our Millimeterwave Power Amplifier design. The 8HP technology offers f_T / f_{max} of 200 GHz / 265 GHz with a maximum breakdown voltage BV_{CES} of 5.9 V for SiGe bipolar device. Moreover, this process is comprised of 7 metallization layers of which 5 are copper layers (M1-M4, MQ) and 2 are aluminum metal layers (LY and AM).

2.4 Transistor Stacking

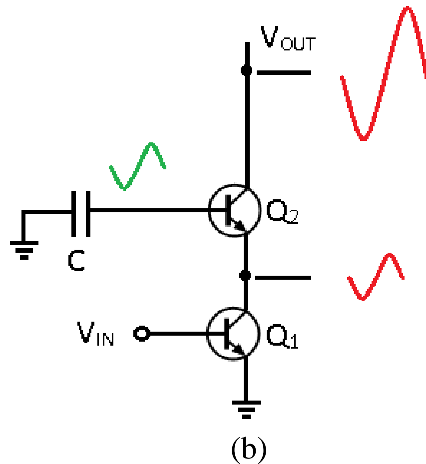
The stacking of transistors is a very effective mechanism for achieving high output power by increasing the voltage swing across the load. Stacking also offers to improve the efficiency of a power amplifier by allowing waveform shaping at the output terminal of its active device. The stacking structure is made up of 'N' number of active devices (FETs or BJTs) stacked on top of each other as shown in Fig. 2.5a below. If 'BV' is the breakdown voltage of each of the 'N'

identically stacked transistors then the voltage swing at the drain / collector of the topmost stacked transistor 'V_{TOP}' can reach N x BV. So, the higher the voltage swing at the load higher will be the output power. Stacking requires a finite signal swing at the gate (or base) of the individual transistors. Such a signal swing can be achieved by connecting finite-sized capacitors at the gate or base of the transistors as shown in Fig. 2.5b ([13]-[16]). Stacking operation is ensured when the voltage at the collector / drain terminal of each stacked transistor adds up linearly to produce the resultant output voltage swing.

Transistors present in stacked configuration may be made to operate in linear or switched mode. In a general stacked structure, the size, type, voltage and current waveform of a transistor are not needed to be similar. Moreover, the current and voltage waveforms of each transistor in stacking can be engineered [13].



(a)



(b)

Fig. 2.4. a) General schematic of stacked-transistors b) BJT stacking with voltage swing depiction.

2.5 Planar Inverted-F Antenna (PIFA)

The proposed On-Chip Antenna (OCA) in this research work is Planar Inverted-F Antenna (PIFA). PIFA is a standing wave antenna. It has a feeding stripe, a shorting stripe and a longitudinal open-ended stripe as shown in Fig. 2.11. It also has a ground plane to reflect the radiation. The antenna-structure resembles an "inverted-F" which explains the name PIFA [17], [18].

The shorting stripe acts as an inductor (a short-circuited stub) and the open-ended longitudinal stripe acts as a capacitor at resonant frequency thereby conforming a tank circuit. This tank circuit resonates at the resonant frequency for which the antenna is designed to radiate.

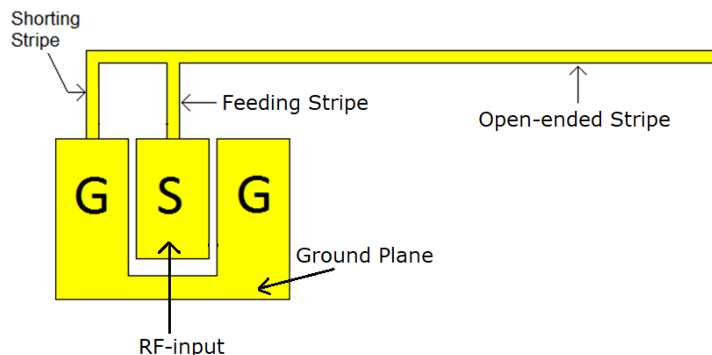


Fig. 2.5. Planar Inverted-F Antenna Structure.

2.6 Literature Review

2.6.1 Millimeterwave Power Amplifiers

The Class-F power amplifier was introduced in the 1950s and since then numerous designs were presented by the researchers. In order to realize a Class-F/F^{-1} amplifier, there are a few general schemes for deploying a Class-F/F^{-1} harmonic circuit in the vicinity of its active device [6]. These schemes are shown in Fig. 2.8. The first scheme as shown in Fig. 2.8a is the conventional one in which the harmonic-network is employed only at the output side of the amplifier whereas the input side consists of a simple matching network designed at the fundamental frequency. A similar scheme was shown in Fig. 2.3 (section 2.2.7) where a third harmonic peaking network was connected at the output of the active device.

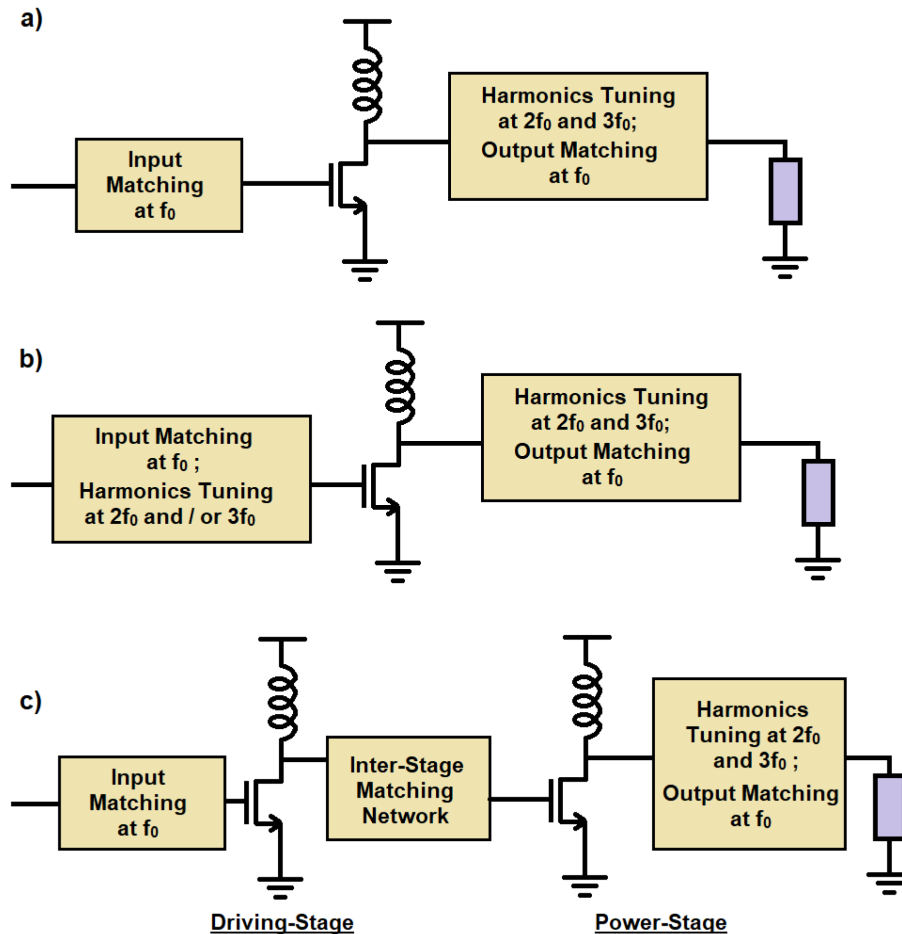


Fig. 2.6. a) Scheme-1: Harmonics tuned at the output. b) Scheme-2: Harmonics tuned both at the input and the output. c) Scheme-3: Two-stage amplifier.

The second scheme (Fig. 2.8b) proposes to shape or tune the harmonics not only at the output side of the active device but also at its input side. The third scheme is shown in Fig. 2.8c, which is a two-stage amplifier. The first stage is called the driving-stage and the second one is the main/power-stage. Driving-stage feeds sufficient power to the main stage and hence drives the main stage into a power-saturation state. The output of the driving-stage and the power-stage may employ a Class-F or a Class-F^{-1} harmonic-network. The third scheme also contains an intermediate stage called as Inter-stage. Inter-stage consists of an impedance-matching network that matches the output impedance of the driving-stage with the input impedance of the power-stage. The third scheme offers higher gain and output power whereas its efficiency may decline as compared to the other two schemes. It is to be noted that Fig 2.8 shows MOSFETs however, the depicted active devices could be BJTs as well.

Research work on integrated millimeterwave Class F/F^{-1} PAs began just a few years back so, there is less work reported regarding it up till now. Most of the latest research work on Class F/F^{-1} PAs is done by S. Y. Mortazavi. Mortazavi presented a Class F^{-1}/F PA in [19]. This amplifier employed a specific wave-shaping network connected at the collector terminal of the SiGe-HBT that enabled it to transform from Class-F^{-1} to Class-F when the frequency changes from 24-GHz to 31-GHz. The amplifier delivered 40.7% PAE along with a gain of 10.3 dB and an output-power of 17.1 dBm. Subsequently, the same author proposed a two-stage Class-F^{-1} power-amplifier in SiGe-BiCMOS [20] which was operable at a center-frequency of 38-GHz. It consisted of a Class-AB driving-stage cascaded with a Class-F^{-1} output-stage. Voltage and current waveforms at the output were shaped by employing a multi-resonant parallel-series load network that also transformed the load impedance to present 50 ohms at the signal output. This amplifier rendered 38.5% peak PAE, an output power of around 16.5 dBm along with a power gain of 16.5 dB. Another PA operable at 28 GHz was reported by Mortazavi in [21]. The amplifier used a coupled-inductor-based harmonic impedance modulator to resonate out 2nd and 3rd harmonic load impedances appropriately for Class F^{-1} operation. The amplifier yielded 42% PAE along with 21.2 dB gain and 17.1 dBm output power. Furthermore, another millimeterwave Class-F^{-1} power amplifier design was proposed by him in [22]. The design was a two-stage amplifier that utilized a quarter-wave transformer at the output side of the driving and the main stage. The PA offered 43% PAE, a power gain of around 18 dB and an output power of 17 dBm at the frequency of 40.5 GHz. A two-stage transformer-based continuous-mode Class F^{-1} PA was reported in [23]. The

amplifier offered a power gain of 20 dB, a peak PAE of 43.5% and a saturated output power of 17 dBm at the operational center-frequency of 28.5 GHz.

As SiGe-BiCMOS is the technology of our interest, therefore, HBT-based stacking structures designed using this technology are essential to be reported. K. Dutta *et al.* reported a Q-band SiGe HBT double-stacked Class E PA in [24]. It consisted of a Class E driving-stage amplifier along with a Class-E-based stacking structure in the main-amplifier. The fabricated chip showed 23.4 dBm maximum saturated power, 34.9 % peak PAE and 14.5 dB power gain at 41 GHz of operating frequency. The same author also proposed a tripled-stacked Class E amplifier in [25] yielding 22.2 dBm output power, 20.8 % PAE and a gain of 15.4 dB at 40 GHz.

Investigations into integrated millimeter-wave (mmW) Class-F^{-1} power amplifiers (PA) in stacked configuration have not been reported previously. This work presents a new two-stage 38-GHz Class-F^{-1} power amplifier with a double-stacked HBT structure in 130-nm SiGe BiCMOS. The proposed design employs Class-F and Class-F^{-1} parasitic-aware harmonic control networks in the driving-stage and the power-stage respectively along with HBT stacking in the power-stage of the amplifier. The proposed amplifier yields a saturated output-power of 21.2 dBm along with an overall gain of 22.1 dB and a peak power-added-efficiency (PAE) of 30.1%. A Figure-of-Merit (FoM) of 69.68 was achieved which is the highest so far when compared with various previously reported integrated millimeter-wave Class F^{-1}/F PAs fabricated in CMOS and SiGe technologies.

2.6.2 Microwave Power Amplifiers

There are several power-amplifier designs operating at the microwave frequency of 6-GHz. Those designs are comprised of cascode, differential and push-pull architectures. An integrated Class-AB power amplifier operating at the center-frequency of 6-GHz was reported in [26]. The amplifier is implemented in 250-nm SiGe-HBT technology. The PA employed an on-chip transformer to combine the output power of two SiGe-HBT push-pull pairs. The amplifier yielded a power-gain of 12 dB, PAE of 24.7% and saturated output-power of 24 dBm. A transformer-based Class-E/F power amplifier in 65-nm CMOS technology was proposed in [27]. The PA incorporated a Single-Pole Triple-Throw (SP3T) switch to select between the outputs of three sub-amplifiers, each operating at a specific range of frequencies from 0.5 to 6 GHz. The amplifier delivered a peak drain efficiency of 34% and an output power of 25.6 dBm. The work did not

report any information regarding values of gain and Power-Added-Efficiency (PAE). A 6-GHz Class-AB power amplifier designed in 65-nm was reported in [28]. The amplifier proposed an output-matching network based on differential architecture and the PA obtained a peak PAE of 28.4%. The PA offered a saturated output power of 22.4 dBm and a gain of 23.6 dB. A Class-F^{-1} power amplifier implemented in 180-nm CMOS technology was proposed in [29]. The amplifier was operated at a frequency of 4.6 GHz. Cascode architecture was incorporated into the design to achieve a high output power of 27.8 dBm. Class-F^{-1} based harmonic tuning technique was employed to obtain a peak PAE of 32%. Moreover, the amplifier provided a gain of 11.6 dB. Very recently a 65-nm differential-cascode based power amplifier operable at the decade frequency range from 600-MHz to 6-GHz was presented in [30]. The amplifier was not fully integrated (off-chip) as its output matching network was fabricated on FR-4 PCB. The PA rendered a PAE of 27.9%, a gain of 19.4 dB and output power of 18.9 dBm.

"Single-transistor" integrated Class-F/F^{-1} power-amplifiers operable at "5G-millimeter-wave frequencies" have been investigated for the last few years. "Single-Transistor" PAs are desirable for 5G-mobile communications as they offer low-voltage operation, a small form factor, and especially a high power-added efficiency (PAE) if the PA is harmonically tuned. A single-transistor millimeterwave Class F^{-1}/F power amplifier in SiGe-BiCMOS was reported in [19] and has been already discussed in the previous section. Very recently another single-transistor Class-F power amplifier in 65nm-CMOS operable at 5G-millimeterwave frequencies is reported in [31]. The PA proposed a tunable-transformer to neutralize the gate-drain capacitance (C_{gd}) and incorporated a parasitic-aware harmonic-network at the drain terminal of the active device. The 1.1 V driven power amplifier rendered 46.4% peak PAE, an output-power of around 14.75 dBm along with a power gain of 10 dB.

A "single-transistor" PA architecture along with Class F/F^{-1} harmonic network operable at a new unlicensed "5G-microwave frequency" of 6-GHz has not been investigated so far in the literature. This work reports a "single-transistor" Class-F^{-1} power amplifier operable at a "5G-microwave frequency" of 6 GHz. The amplifier is designed with 65-nm CMOS technology. The proposed design employs a "parasitic-aware" class-F^{-1} harmonic network connected at the drain terminal of the NMOS device. There are several Class-F^{-1} circuit-topologies based on the LC network however, the proposed Class-F^{-1} LC-network is a new topology deduced using a novel

iterative algorithm. A dual-purpose output matching network is incorporated in the design which reinforces the waveform-shaping capability of the class-F^{-1} harmonic-network along with performing the typical task of output impedance matching. The fabricated PA shows a power gain of 13.8 dB and 14.4 dBm saturated output power. The proposed amplifier offers one of the highest PAEs (47.8%) compared to many other monolithic microwave/millimeter-wave CMOS and SiGe power-amplifiers reported so far.

2.6.3 Millimeterwave On-Chip Antennas

While realizing a truly integrated RF system, designing an antenna on chip is considered to be the last barrier. Several designs of antennas in standard CMOS technologies have been investigated by researchers. Designing an On-Chip Antenna (OCA) is not only challenging from the perspective of appropriate selection of antenna structure but also from the viewpoint of stringent requirements related to the fabrication of the antenna on a microchip-platform.

A straight-line Planar Inverted-F Antenna (PIFA) fabricated in standard CMOS process technology was proposed in [32]. The OCA was operable at the millimeter-wave frequency band of 60-GHz. The antenna was excited at the fourth-order mode resulting in an increased antenna footprint. The measurement results showed that the OCA yielded an absolute-gain of -19 dBi. A PIFA has a very strong dependence on the ground-plane and the OCA in [32] was designed without a ground-plane resulting in significant deterioration in antenna-gain. In [33], a meander-line PIFA was fabricated in 180-nm TSMC CMOS process node. This OCA was excited at the 5G millimeter-wave frequency of 60-GHz and produced an absolute-gain value of -15.7 dBi. The OCA's meandered section, residing at the edge of the microchip, helped to reduce the overall antenna length however, a considerable part of the antenna body remained away from the edge of the microchip causing reduction in radiation efficiency. Moreover, the work did not show the dimensions of the antenna thereby providing no information on the width and length of the fabricated OCA. Apart from positioning the OCA close to the edge of the microchip another effective technique to minimize the radiation absorption within the silicon substrate is to establish arrays/grid of Artificial Magnetic Conductor ([34]−[37]) underneath the antenna body. A 60-GHz On-Chip patch antenna in 180-nm CMOS technology was proposed in [38]. The gain of the antenna was attempted to be improved by employing artificial magnetic conductors. Two parasitic

elements (square metallic regions) were positioned on either side of the patch antenna for the purpose of obtaining a broad bandwidth. The measurement results indicated that the antenna offered a gain performance of around -2.2 dBi in the frequency range of 50 to 70 GHz. The OCA is comprised of large metallic sections in the form of patch antenna and rectangular parasitic elements. Such large metallic areas or similar structure drawn by the top-most metal layer of CMOS technology has the potential to cause micro-fracture to the silicon substrate. Hence such a design is not appreciated for fabrication in CMOS technology, especially for bulk production. Moreover, the work did not discuss and showed metal-fill areas essential to satisfy the microchip's pattern-density requirements.

Recently a monopole on-chip antenna was designed for 77-GHz automotive radar application [39]. This OCA employed a layer of AMC underneath the monopole antenna to improve radiation efficiency. The on-chip monopole was fabricated in 180-nm CMOS and yielded a gain of around -4 dBi. The OCA was positioned in the center of the microchip and the metal-exclusion-area was not drawn to cover the entire antenna-design (OCA plus AMC) and hence introduced a barrier in the path of antenna radiation resulting in lower antenna-gain than expected. Very recently a meander-line on-chip monopole fabricated in Standard 65-nm CMOS was proposed in [40]. The antenna yielded a gain of 0-dBi while operating at the millimeter-wave frequency of 60-GHz. The OCA did not incorporate an AMC grid however, the design employed an additional substrate under the silicon die to improve the radiation efficiency. Such an OCA-design urges additional post-processing treatment and demands to fulfill a certain criterion in terms of thickness and permittivity values of that substrate.

Besides the above-mentioned fabricated On-Chip Antennas (OCAs) there are numerous simulation-based OCA-structures proposed in the literature. A circular disk monopole OCA designed at 60-GHz in standard CMOS process technology was proposed in [41]. Simulation results showed that the antenna produced a gain of -4.9 dBi at 60-GHz frequency. An AMC-based triangular monopole antenna-on-chip at 60-GHz in 180-nm process technology was designed in [42]. Simulation results demonstrated that the antenna produced a gain of 2.5 dBi. In [43], an on-chip slot-based patch antenna was proposed for indoor wireless communications. The OCA offered circular polarization when excited at 60-GHz and yields an antenna-gain of 1-dBi. Apart from the above-mentioned OCAs, there were various other simulation-based OCA structures excited at the

millimeterwave frequencies ([44]-[46]). The above-referred work on simulation-based OCAs did not discuss the requirements of the metal-fill density and practical feasibility of a large exclusion area essential for the proper operation of the antenna on microchip.

Most of the work regarding the On-Chip Antennas has been performed at 5G frequency of 60-GHz whereas, less work has been reported on OCAs operating at 5G frequencies that are lower than 60-GHz. An OCA referred and discussed above [40] was designed to radiate not only at 60-GHz but also at 5G millimeterwave frequency of 28-GHz. The antenna was fabricated in 65-nm CMOS process node and yielded a gain of -10 dBi at 28-GHz. Other than 60-GHz and 28-GHz, a potential candidate for 5G cellular communications at millimeterwave frequencies is 38-GHz [47]-[49]. A 38-GHz AMC-based on-chip triangular monopole antenna designed in 28-nm CMOS technology was reported in [50]. The work presented simulation results only. The OCA offered an antenna-gain of -1.75 dBi and occupied a considerably huge area of more than 4 mm^2 on the microchip. The simulation-based OCA did not discuss the requirements of the metal-fill density and the practical feasibility of such a large (more than 4-mm^2) exclusion area.

As limited work has been conducted on OCA operating at a 5G millimeterwave frequency of 38-GHz and the frequency also exhibits minimum atmospheric absorption characteristics therefore, in this work, 38-GHz of 5G-frequency is selected for designing an on-chip antenna. The work presents an On-Chip Planar Inverted-F Antenna (PIFA) in 180-nm CMOS process technology. A PIFA is selected because of its features which make it the best-suited candidate for on-chip deployment. PIFA offers simple geometry, a small form factor, design flexibility and robustness. Moreover, the input impedance of a PIFA can be set by adjusting the distance between the shorting stripe and the feeding stripe. Additionally, PIFA is only a quarter-wavelength long and therefore, it can easily fit inside an already space-constraint environment of a microchip. An Ultra-Thick Metal (UTM) layer in 180-nm CMOS process node is utilized to implement the proposed PIFA structure on the chip. To achieve better radiation performance, the OCA body is positioned close to the edge of the microchip. The measurement results show that the on-chip PIFA achieves a minimum return loss of 14.8 dB and a gain of 0.7 dBi at the center-frequency of 38-GHz. To the best of the authors' knowledge, the presented OCA is the first *On-Chip PIFA* designed, fabricated and tested at the *5G millimeterwave frequency 38-GHz.*

References

[1] D. M. Pozar, “Microwave amplifier design,” in *Microwave Engineering*, 2nd ed., John Wiley & Sons, 1998, Chapter 11, pp. 536-572.

[2] Thomas L. Floyd, “Power amplifiers,” in *Electronic Devices*, 7th ed., Prentice Hall, 2004, Chapter 9, pp. 426-457.

[3] A.V. Grebennikov, “Circuit design technique for high efficiency class F amplifiers,” *IEEE MTT-S Int. Symp. Dig.*, Boston, MA, USA, June 11–16, 2000, pp. 771–774.

[4] S. Gao, “High efficiency class F RF/microwave power amplifiers,” *IEEE Microwave Magazine*, pp. 40–48, Feb 2006.

[5] Y. Woo, Y. Yang and B. Kim, “Analysis and experiments for high efficiency class F and inverse class F power amplifiers,” *IEEE Transactions on Microwave Theory and Techniques*, vol. 54, no. 5, pp. 1969-1974, May 2006.

[6] D. Wang, W. Chen, X. Liu, X. Li, F. M. Ghannouchi and Z. Feng, "A 24–44 GHz Broadband Transmit–Receive Front End in 0.13-μm SiGe BiCMOS for Multistandard 5G Applications," in *IEEE Transactions on Microwave Theory and Techniques*, vol. 69, no. 7, pp. 3463-3474, July 2021.

[7] Z. Wang et al., "A Linearity-enhanced 28-GHz Class-F−1 SiGe Power Amplifier," *2022 IEEE MTT-S International Wireless Symposium (IWS)*, Harbin, China, 2022, pp. 1-3.

[8] M. Osama, H. F. Ragai and M. El-Nozahi, "A 28GHz High Efficiency Inverse Class-F Series Doherty Power Amplifier," *2023 11th International Conference on Internet of Everything, Microwave Engineering, Communication and Networks (IEMECON)*, Jaipur, India, 2023, pp. 1-6.

[9] V. Manouras and I. Papananos, “A Ka-Band SiGe BiCMOS Quasi-F^{-1} Power Amplifier Using a Parasitic Capacitance Cancellation Technique,” *Journal of Low Power Electronics and Applications*, vol. 13, no. 2, p. 23, Mar. 2023.

[10] M. Schroter, T. Rosenbaum *et al.*, “SiGe HBT Technology: Future trends and TCAD-based roadmap,” *Proceedings of IEEE*, vol. 105, no. 6, pp. 1068–1086, June 2017.

[11] J. B. Johnson,A. J. Joseph *et al.,* “Silicon Germaninum BiCMOS HBT technology for wireless power amplifier applications,” *IEEE Journal of Solid State Circuits*, vol. 39, no. 10, pp. 1605-1614, Oct. 2004.

[12] Globalfoundaries, https://www.globalfoundries.com/sites/default/files/product-briefs/130nm- sige-performance-brief.pdf (accessed on Sep. 1, 2017).

[13] H. Hashemi, “Millimeterwave power amplifiers and transmitters,” *2017 IEEE Custom Integrated Circuit Conference*, Austin, TX, USA, 3 May, 2017.

[14] C. Zhang, Z. Li, G. Cheng, H. Wang and Z. Li, "A 26.5-40 GHz Stacked Power Amplifier in 130 nm SiGe BiCMOS Technology," *2018 IEEE International Conference on Integrated Circuits, Technologies and Applications (ICTA)*, Beijing, China, 2018, pp. 36-37.

[15] N. L. K. Nguyen et al., "A Wideband SiGe Power Amplifier Using Modified Triple Stacked-HBT Cell," in *IEEE Microwave and Wireless Components Letters*, vol. 31, no. 1, pp. 52-55, Jan. 2021.

[16] Z. Liu, E. A. Karahan and K. Sengupta, "A Compact SiGe Stacked Common-Base Dual-Band PA With 20/18.8 dBm Psat at 36/64 GHz Supporting Concurrent Modulation," in *IEEE Microwave and Wireless Components Letters*, vol. 32, no. 6, pp. 720-723, June 2022.

[17] A. Balanis, “Linear wire antennas,” in *Antenna Theory: Analysis and Design*, 3rd ed., John Wiley & Sons, 2005, Chapter 4, pp. 151-218.

[18] P. J. Bevelacqua, “Antenna basics.” *Antenna-Theory.com*. https://www.antenna-theory.com/antennas/patches/pifa.php (accessed on Feb. 7, 2021).

[19] S. Y. Mortazavi and K.-J. Koh, “A Class F^{-1}/F 24-to-31GHz power amplifier with 40.7% peak PAE, 15dBm OP_{1dB}, and 50mW P_{sat} in 0.13μm SiGe BiCMOS,” in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, San Francisco, CA, USA, Feb. 2014, pp. 254–255.

[20] S. Y. Mortazavi and K.-J. Koh, “Integrated inverse class-F silicon power amplifiers for high power efficiency at microwave and mm-Wave,” *IEEE Journal of Solid State Circuits*, vol. 51, no. 10, pp. 2420–2434, Oct. 2016.

[21] S. Y. Mortazavi and K.-J. Koh, "A 28-GHz inverse class-F power amplifier with coupled-inductor based harmonic impedance modulator," in *IEEE Custom Integrated Circuits Conference*, San Jose, CA, USA, Sep. 2015.

[22] S. Y. Mortazavi and K.-J. Koh, "A 43% PAE inverse class F power amplifier at 39-42 GHz with a λ/4 transformer based harmonic filter in 0.13-um SiGe BiCMOS," in *IEEE MTT-S International Microwave Symposium (IMS)*, San Francisco, CA, USA, 22-27 May 2016.

[23] T-W. Li, M-Y. Huang, and H. Wang, "Millimeter-Wave continuous-mode power amplifier for 5G MIMO applications," *IEEE Transactions on Microwave Theory and Techniques*, vol. 67, no. 7, pp. 3088–3098, Jul. 2019.

[24] K. Datta *et al.*, "Analysis, design and implementation of mm-wave SiGe stacked class-E power amplifiers," in *IEEE RFIC Symp. Dig. Papers*, Seattle, WA, USA, Jun. 2013, pp. 275–278.

[25] K. Datta and H. Hashemi, "Performance limits, design, and implementation of mm-wave SiGe HBE class-E and stacked class- E power amplifiers," *IEEE Journal of Solid State Circuits*, vol. 49, no. 10, pp. 2150 – 2171, Oct. 2014.

[26] D. Gruner and G. Boeck, "Fully integrated 5.6–6.4 GHz power amplifier using transformer combining," in *Ph.D. Research in Microelectronics and Electronics*, pp. 160–163, Aug. 2009.

[27] H. Wang and H. Hashemi, "A 0.5–6GHz 25.6 dBm fully integrated digital power amplifier in 65-nm CMOS," in *Proc. IEEE Radio Freq. Integr. Circuits Symp. (RFIC)*, Jul. 2014, pp. 409–412.

[28] W. Ye, K. Ma and K. S. Yeo, "A 2-to-6 GHz class-AB power amplifier with 28.4% PAE in 65nm CMOS supporting 256 QAM," in *IEEE Int. Solid-State Circuits Conf. (ISSCC)*, Mar. 2015, pp. 38–39.

[29] F. Chen, Y. Wang, Y.-H. Hsiao, J.-L. Lin. Y.-C. Chen and H. Wang, "A 4.6-GHz class-F^{-1} high power CMOS power amplifier," in *IEEE Int. Symp. on Radio-Freq. Integr. Tech.(RFIT)*, Sep. 2017, pp. 183–185.

[30] J. Lindstrand, M. Tormanen and H. Sjoland, "A decade frequency range CMOS power amplifier for sub-6-GHz cellular terminals," *IEEE Microwave and Wireless Component Letters*, vol. 30, no. 1, pp. 54–57, Jan. 2020.

[31] S. N. Ali, P. Agarwal, S. Gopal S. Mirabbasi and D. Heo, "A 25-35 GHz neutralized continuous class-F power amplifier for 5G mobile communications achieving 26% modulation PAE at 1.5 Gb/s and 46.4% peak PAE," *IEEE Transactions on Circuits* and *Systems-I, Reg. Papers*, vol. 66, no. 2, pp. 834–847, Feb. 2019.

[32] Y. P. Zhang, M. Sun and L. H. Guo, "On-chip antennas for 60-GHz radios in silicon technology," *IEEE Transactions on Electronic Devices*, vol. 52, no. 7, pp. 1664 – 1668, Jun. 2005.

[33] P. J. Guo *et al.*, "60-GHz millimeter-wave CMOS RFIC on-chip meander-line planar inverted-F antenna for WPAN applications," in *IEEE Antennas and Propagation Society International Symposium*, Sep. 2008.

[34] D. Sievenpiper, L. Zhang, R. F. Broas, N. G. Alexopolous, and E. Yablonovitch, "High-impedance electromagnetic surfaces with a forbidden frequency band," *IEEE Transactions on Microwave Theory and Techniques*, vol. 47, no. 11, pp. 2059–2074, Nov. 1999.

[35] A. P. Feresidis, G. Goussetis, S. Wang, and J. C. Vardaxoglou, "Artificial magnetic conductor surfaces and their application to low profile high-gain planar antennas," *IEEE Transactions on Antennas and Propagation*, vol. 53, no. 1, pp. 209–215, Jan. 2005.

[36] R. Dewan, M. K. A. Rahim, M. R. Hamid, M. F. M. Yusoff, N. A. Samsuri, N. A. Murad, and K. Kamardin. "Artificial magnetic conductor for various antenna applications: An overview." *International Journal of RF and Microwave Computer-Aided Engineering*, vol. 27, no. 6, pp. 1–18, Feb. 2017.

[37] A. Kumar *et al.*, "Studies of Various Artificial Magnetic Conductor for 5G Applications." in *Optical and Wireless Technologies*, Singapore, Springer, 2020, pp. 523–530.

[38] H. Chu *et al.*, "60-GHz broadband CMOS on-chip antenna with an artificial magnetic conductor," in *IEEE International Microwave workshop Series on Advanced Materials and Processes for RF and THz Application (IMWS-AMP)*, July. 2016.

[39] H. Zhang and A. Shamim, “Tackling the issues of millimeter-wave on-chip antenna measurements,” in *13th European Conference on Antennas and Propagation (EuCAP)*, June 2019.

[40] P. Burasa, T.Djerafi and Ke Wu, “A 28 GHz and 60 GHz dual-band on-chip antenna for 5G-compatible IoT-served sensors in standard CMOS process,” *IEEE Transactions on Antennas and Propagation*, vol. 69, no. 5, pp. 2940–2945, May 2021.

[41] S. Upadhyay and S. Srivastava, “A 60-GHz on-chip monopole antenna using silicon technology,” in *IEEE Applied Electromagnetics Conference (AEMC)*, pp. 1–2, Dec. 2013.

[42] D. Gang, H. M. Yang and Y. Y. Tang, “Wideband 60-GHz on-chip triangular monopole antenna in CMOS,” in *Proc. 3rd Asia-Pacific Conference on Antennas and Propagation*, pp. 623–626, Jul. 2014.

[43] A. Masrouri and N. Amiri, “Circularly Polarized On-Chip Antenna for 60GHz Indoor Wireless Communications,” in *IEEE 18th Mediterranean Microwave Symposium (MMS)*, pp. 264–267, Nov. 2018.

[44] F. Gutierrez *et al.*, “On-chip integrated antenna strucutres in CMOS for 60 GHz WPAN systems,” *IEEE Journal on Selected Areas in Communications*, vol. 27, Iss. 8, pp. 1367–1378, Sep. 2009.

[45] W. Yang, Wanlan, K. Ma, K. S. Yeo, and W. M. Lim, “A 60GHz on-chip antenna in standard CMOS silicon Technology,” in *2012 IEEE Asia Pacific Conference on Circuits and Systems*, pp. 252–255, Dec. 2012.

[46] K. S. Sultan, H. H. Abdullah, E. A. Abdallah, M. A. Basha, and H. H. El-Hennawy, "A 60-GHz gain enhanced vivaldi antenna on-chip," *IEEE International Symposium on Antennas and Propagation & USNC/URSI National Radio Science Meeting*, pp. 1821–1822, Jul. 2018.

[47] T. S. Rappaport, S. Sun, R. Mayzus, H. Zhao, Y. Azar, K. Wang, G. N. Wong, J. K. Schulz, M. Samimi and F. Gutierrez, “Millimeter-wave mobile communications for 5G cellular: It will work!,” *IEEE Access*, vol. 1, pp. 335–349, May 2013.

[48] Y. Huo *et al.*, “5G cellular user equipment: From theory to practical hardware design,” *IEEE Access*, vol. 5, pp. 13992–14010, Jul. 2017.

[49] A. Ghosh, T. A. Thomas, M. C. Cudak, R. Ratasuk, P. Moorut, F. W. Vook, T. S. Rappaport, G. R. MacCartney, S. Sun, and S. Nie, "Millimeter-wave enhanced local area systems: A high-data-rate approach for future wireless networks," *IEEE Journal on Selected Areas in Communications*, vol. 32, no. 6, pp. 1152–1163, Jun. 2014.

[50] M. K. Hedayati *et al.*, "A 38 GHz on-chip antenna in 28-nm CMOS using artificial magnetic conductor for 5G wireless systems," in *4th International Conference on Millimeter-waves and Terahertz Technologies (MMWaTT)*, pp. 29–32, Dec. 2016.

CHAPTER NO. 3

INTEGRATED MILLIMETERWAVE POWER AMPLIFIER

Chapter 3 includes the research article, "A 38-GHz Millimeter-wave Double-Stacked HBT Class-F^{-1} High-Gain Power-Amplifier in 130-nm SiGe-BiCMOS", published in *IEEE Transactions on Microwave Theory and Techniques*, vol. 68, no. 7, pp. 3039–3044, May 2020. DOI: 10.1109/TMTT.2020.2988874.

The full text of the publication is included in this chapter without any modifications. However, there are formatting differences to keep the format the same for the thesis. The formatting modifications involve page setup, line spacing, and font size.

A 38-GHz Millimeter-wave Double-Stacked HBT Class-F^{-1} High-Gain Power-Amplifier in 130-nm SiGe-BiCMOS

3.1 Abstract

Investigations into integrated millimeter-wave (mmW) Class-F^{-1} power amplifier (PA) in stacked configuration have not been reported previously. This article presents a novel two-stage double-stacked heterojunction bipolar transistor (HBT) Class-F^{-1} PA in the 130-nm SiGe-BiCMOS technology. The proposed amplifier operates at the mmW center frequency of 38 GHz. The driving stage of the amplifier is loaded with a Class-F harmonic network and the double-stacked power stage incorporates Class-F^{-1} loading. An interstage matching network is designed to deliver maximum power from the driving stage to the power stage. The proposed new HBT amplifier yields a saturated output power of 21.2 dBm along with an overall gain of 22.1 dB and a peak power-added efficiency (PAE) of 30.1%. A figure-of-merit (FoM) of 69.68 was achieved for this amplifier which is the highest so far when compared with various recently reported integrated mmW Class-F^{-1}/F PAs.

3.2 Introduction

In recent years, demand for high data-rate in cellular communication is increasing exponentially and the current systems appear unable to cope with this upcoming level of throughput requirements. In an effort to deal with this challenge "millimeter-wave (mmW) frequencies" in the electromagnetic spectrum have been offered to academic and commercial sectors for research and system production. One of the millimeter-wave frequencies of interest for the next era cellular communication (5G) is 38-GHz [1]. To realize 5G, there is a crucial requirement of wireless circuits operable at the specified millimeter-wave frequency. One of the significant circuit modules in wireless hardware implementation is the power-amplifier (PA).

Integrated Class-F PAs operable at millimeter-wave frequencies have been investigated for the past few years. A Class F^{-1}/F PA was reported in [2]. This amplifier employed a specific wave-

shaping network connected at the collector terminal of the SiGe-HBT that enables it to transform from Class-F^{-1} to Class-F when the frequency changes from 24-GHz to 31-GHz. The amplifier delivered 40.7% power-added-efficiency (PAE) along-with a gain of 10.3 dB and an output-power of 17.1 dBm. Subsequently, Mortazavi and Koh [2] proposed a two-stage Class-F^{-1} PA in SiGe-BiCMOS [3] which was operable at a center-frequency of 38-GHz. It consisted of a Class-AB driving-stage cascaded with a Class-F^{-1} output-stage. The voltage and current waveforms at the output were shaped using a multi-resonant parallel-series load network that also transforms the load impedance to present 50 Ω at the signal output. This amplifier rendered 38.5% peak PAE, an output power of around 16.5 dBm along-with a power gain of 16.5 dB. Very recently a two-stage continuous-mode Class F^{-1} PA was reported in [4]. The amplifier offered a power gain of 20 dB, a peak PAE of 43.5% and a saturated output power of 17 dBm at the operational center-frequency of 28.5 GHz. The work reported in this article describes a new two-stage Class-F^{-1} power amplifier with a double-stacked HBT structure in 130-nm SiGe BiCMOS. The proposed design employs Class-F and Class-F^{-1} harmonic networks in the driving-stage and the power-stage (output-stage), respectively, along-with HBT stacking in the power-stage of the amplifier. The proposed design offers the highest Figure-of-Merit compared to many other monolithic Class F/F^{-1} SiGe-BiCMOS power-amplifiers reported so far.

3.3 Two-Staged Double-Stacked Class-F^{-1} PA

Fig. 3.1 shows the proposed new two-stage double-stacked HBT Class-F^{-1} PA consisting of a Class-F driving-stage and a Class-F^{-1} power-stage. Input and output matching provides around 50 Ω characteristic impedance on both ports of the PA. An inter-stage matching network is designed to transfer maximum power from the output of the driving-stage to the input of the stacked HBT power-stage. The harmonic control networks (circuits) in the driving-stage and the stacking power-stage are *parasitic aware networks* which take into account the parasitic capacitances in generating the required voltage and current waveform shapes. The matching networks are implemented by including these parasitic capacitances as components of the harmonic control network. The details of the proposed amplifier are further elaborated in the sections below.

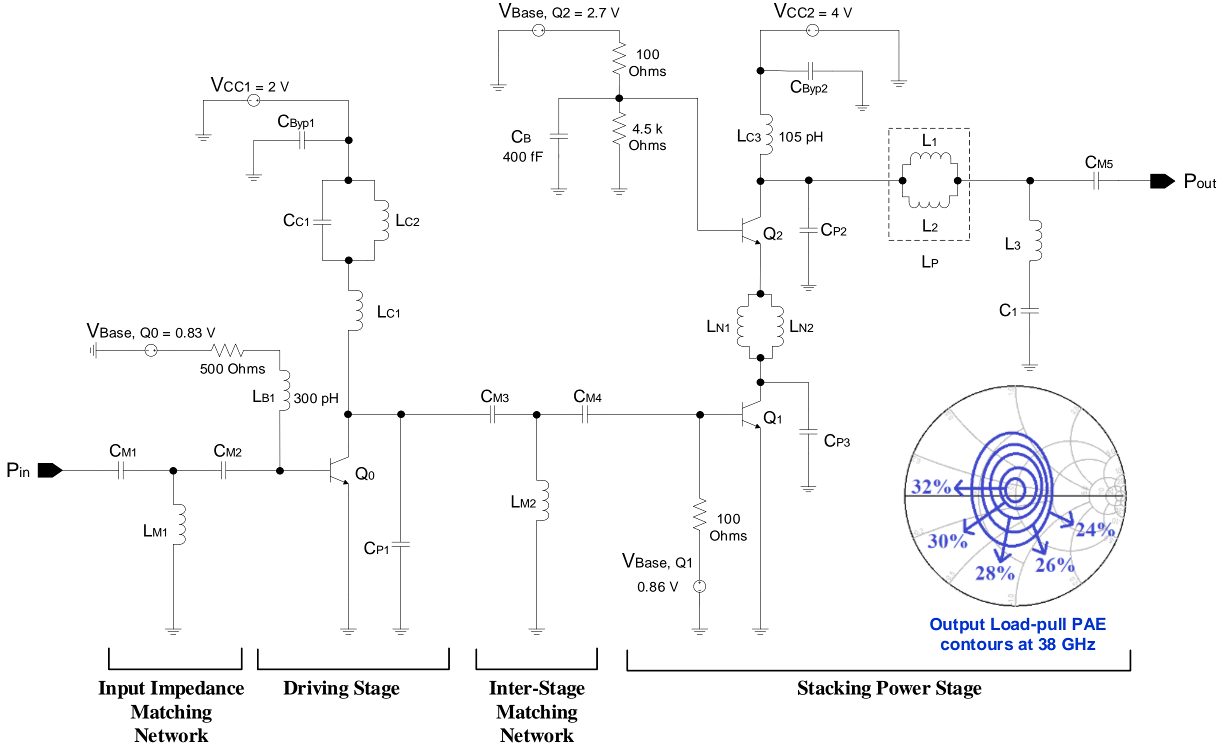


Fig. 3.1. The proposed new 2-stage double stacked class-F^{-1} power amplifier in Global-Foundries 130 nm SiGe-BiCMOS technology.

3.3.1 Class-F Driving Stage

The driving-stage HBT Q_0 has an emitter-area of 2×12×0.12 μm^2 and is biased through chokes employing a DC collector-voltage V_{CC1} of 2 V along with a DC base-voltage $V_{Base,Q0}$ = 0.83 V. This combination of transistor-size and bias-voltages enables the driving-stage to produce 13 dBm of saturated output-power. Moreover, it drags the power-stage to deliver the saturated output-power when the driving-stage output-power reaches the vicinity of its 1-dB compression-point, OP_{-1dB} of 10.7 dBm. The collector node of the HBT Q_0 is loaded with a Class-F harmonic-network and the collector-to-substrate parasitic capacitance C_{P1} (55 fF) is harvested as a component of this network as shown in the Fig. 3.1. Other components of this Class-F circuitry consist of an LC-tank (L_{C2}, C_{C1}) and an inductor L_{C1}. The required values of these passive reactive components are calculated employing the following formulas [5].

$$L_{C1} = 1 / 6\omega_0^2 C_{P1} = 53.2 \text{ pH} \tag{3.1}$$

$$L_{C2} = (5 / 3)\ L_{C1} = 88.7\ \text{pH} \quad (3.2)$$

$$C_{C1} = (12 / 5)\ C_{P1} = 132\ \text{fF} \quad (3.3)$$

The parallel resonant tank (L_{C2}, C_{C1}) is tuned to resonate at a frequency higher than the fundamental, f_0 but lower than the second harmonic, $2f_0$. Consequently, it behaves as an overall inductor (with overall inductive reactance) at the fundamental frequency and combines its inductance with L_{C1} to resonate out the parasitic capacitance C_{P1}. At the second harmonic frequency, $2f_0$, the tank circuit becomes overall capacitive (with overall capacitive reactance) and constitutes a series LC resonant circuit with the inductor L_{C1} resulting in the creation of a short circuit path to AC ground. Whereas, at $3f_0$, the tank (L_{C2}, C_{C1}) becomes capacitive, but along-with L_{C1} appears as an overall inductor (with overall composite inductive reactance). This apparent inductor resonates with the capacitance C_{P1} to produce an open-circuit looking into the load at the 3rd harmonic. The composite LC-tuned harmonic-network at the collector of the driving-stage HBT performs a wave-shaping operation at the driving-stage output so that the voltage waveform and the current waveform appear approximately as square-wave and half-sinusoidal-wave respectively as shown in the Fig. 3.2. The voltage spectrum in Fig. 3.3 shows an odd harmonic rich spectrum as the composite tank behaves like an open-circuit at $3f_0$, whereas, the figure shows the current spectrum containing higher 2nd harmonic level as the load appears to be short circuited at $2f_0$. In Fig. 3.3 the normalization references for the voltage and current levels are respectively the DC-bias voltage and the DC-bias current associated with the collector terminal of the HBT Q_0.

The driving stage is followed by an inter-stage impedance matching network. The T-match circuit consists of a grounded RF-Line (a transmission line structure) inductor L_{M2} (104 pH) along-with two floating capacitors C_{M3} (45 fF) and C_{M4} (150 fF). As the contribution of the pre-power (driving) stage's efficiency in the overall efficiency of the power-amplifier is relatively small, the inter-stage matching network is designed for maximum power transfer from the driving-stage to the stacked power-stage rather than for maximum efficiency, as a trade-off, thereby achieving higher overall gain. It is to be noted that the composite LC-tuned network connected at the output of the stacked power-stage along with the bulk capacitance C_{M5} (500 fF) approximately matches the circuit's output impedance to 50-Ω load. This eliminates the need for an additional output matching circuit and prevents any consequent PAE deterioration associated with losses in the matching-circuit components. An input matching network to match 50-Ω source is provided at the

input of the driving-stage and it consists of another T-match circuit employing the grounded RF-Line inductor L_{M1} (90 pH) and two floating MIM capacitors C_{M1} (124 fF) and C_{M2} (350 fF).

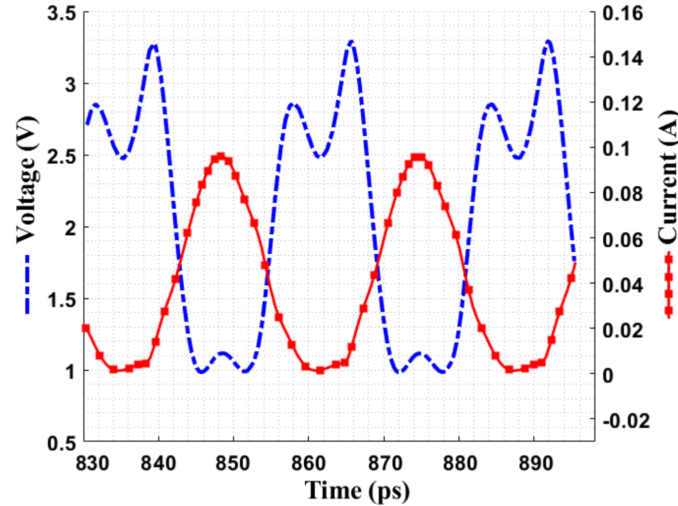


Fig. 3.2. Voltage and current waveforms at the collector terminal of the driving stage HBT(Q_0).

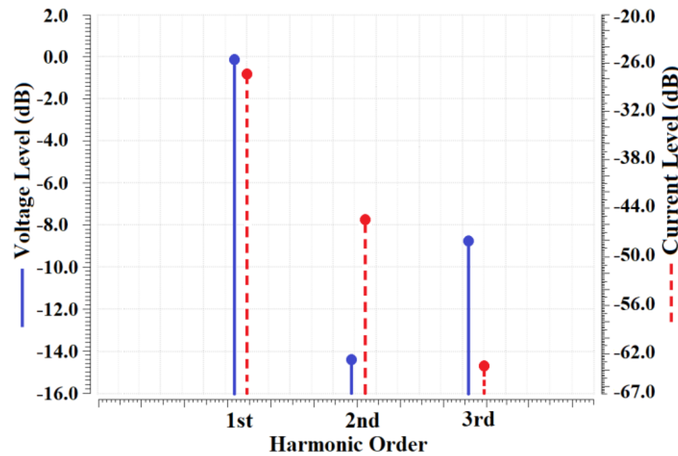


Fig. 3.3. Voltage and current spectrum up to the 3rd harmonic at the collector of the HBT (Q_0).

3.3.2 Stacked Class-F^{-1} Power-Stage Amplifier

Two composite HBTs are stacked in series ("cascode" like topology) in the power-stage of the amplifier as shown in the Fig. 3.1. Stacking enables high output-power at low V_{CE} swing for each HBT device thus ensuring linear operation of each device in the stack in the forward-active-region.

In general, a stacking structure with many stacked devices can be operated at a higher V_{DC} compared to a cascode structure since there is a voltage-swing controlling mechanism in the stacking structure. Stacking also allows the exploration of efficiency improvement by allowing current and voltage waveform shaping at the output (collector) terminal of each device in the stack. The technique requires finite signal swing at the base terminal of the stacked device in distinction from a cascoding device. Such a signal swing can be achieved through capacitive voltage-division employing a finite-sized capacitor (C_B = 400 fF, as shown in the Fig. 3.1) at the base in conjunction with the C_{BE} [base-emitter (B-E) diffusion capacitance] of the forward-biased B-E junction. Compared to a cascoding device in a cascode whose base is at AC ground, the base of a stacked device is thus not at AC ground. The cascoding device in a cascode operates in the common-base configuration, whereas the stacked device in a stacking structure operates as a superposition of the common-base and the common-emitter configurations. The small-signal variations at the collector of the stacked device can thus be smaller compared with that at the collector of the cascoding device. This results in higher collector efficiency for each device in the stacking structure compared to each device in a cascode [6]. The voltages across the collector-emitter terminals of stacked HBTs add up linearly to produce the resultant output voltage-swing. Overall, the trade-off with the topologically similar cascode structure is thus higher linearity and efficiency for the stacking implementation at the expense of somewhat reduced gain.

In Fig. 3.1, the lower active device (Q_1) is implemented using six HBTs connected in parallel each having an emitter-length of 16 µm. On the other hand, the upper stacked device (Q_2) also consists of six parallel HBTs but each of these has an emitter-length of 12 µm. These HBT devices are formed employing the available CBEBC (Collector-Base-Emitter-Base-Collector) layout-cells of the 8HP technology to enable enhanced collector current handling reliability (reduce current crowding). The DC-bias voltages are selected considering the break-down voltages, BV_{CBO} = BV_{CES} = 5.9V. A supply voltage V_{CC2} of 4 V along-with the base-voltages $V_{Base,Q2}$ of 2.7 V and $V_{Base,Q1}$ of 0.86 V are employed. In addition, the DC bias base resistances of Q_1 and Q_2 are set to be around ~100 Ω so that the overall DC operating-point is well-defined and away from the breakdown I-V region. A saturated output-power, P_{out} of 21.3 dBm is produced, and is delivered to the 50-Ω load with around 32% PAE in the load-pull simulations at 38 GHz as indicated by the contours on the Smith-chart in Fig. 3.1.

The stacking structure is loaded with a Class-F^{-1} harmonic control network which also harvests the parasitic capacitance C_{P2} (165 fF) in its implementation. The Class F^{-1} harmonic control network was implemented from a circuit theoretic approach rather than an impedance transformation approach that uses rotations on the smith-chart. It was designed using a carefully chosen network configuration and lumped reactive components to satisfy the parallel and series resonance conditions for various frequencies to achieve the necessary matching for the overall Class-F^{-1} voltage and current wave-form shapes. The insight into the harmonic control network design procedure begins from the first step of tuning out the parasitic capacitance C_{P2}. The fundamental frequency along-with the harmonic frequencies have to tune out this parasitic capacitance in order to realize an open or a short circuit path depending on the wave-shaping requirement.

Fig. 3.4 shows the behavior of the harmonic control network at different frequencies of interest. At the fundamental, f_0 [Fig. 3.4(a)], the LC-tuned circuits become dual-f_0 resonator. The inductor L_{C3} at the collector of Q_2 resonates with the parallel parasitic capacitor C_{P2} and produces an open-circuit at f_0. Whereas, the inductor L_P constitutes a series resonant LC short-circuit at f_0 with the bulk capacitance C_{M5} and allows only the fundamental to reach the load. Here L_P (=35.5 pH) consists of two equal parallel inductors (L_1 and L_2, 71 pH each). This enables an accurate implementation of a smaller inductance value employing two larger inductors. The series branch of (L_3, C_1) with L_3 = 73 pH and C_1 = 60 fF constitutes a high impedance path to ground at the fundamental. At the 2nd harmonic, the series resonant branch of (L_3, C_1) creates a short-circuit to the AC-ground. Hence, the resulting circuit as shown in the Fig. 3.4(b) consists of a parallel resonant tank circuit comprising the composite inductor $L_{C3} \parallel L_P$ in parallel with the parasitic capacitance C_{P2}, thus generating an open-circuit at $2f_0$. On the other hand, the 3rd harmonic is short-circuited by the parasitic capacitance C_{P2} as shown in the Fig. 3.4(c). Hence, through this passive frequency steering the implemented harmonic-control network fulfills the requirement of Class-F^{-1} loading. The loadpull simulation is carried out at the output of the power-stage which includes the effect of the harmonic control circuitry.

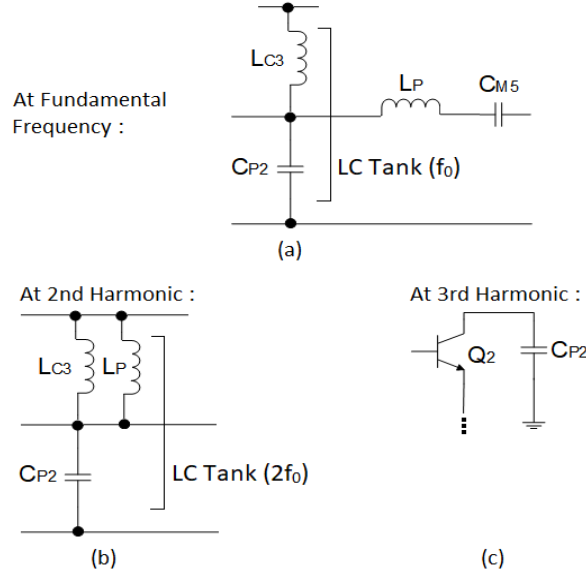


Fig. 3.4. Depiction of passive frequency steering by the Class-F^{-1} harmonic control network at the collector of Q_2 (stacked stage output node) for (a) fundamental, (b) 2nd harmonic, and (c) 3rd harmonic.

The current and voltage waveforms at the collector of Q_2, the output node of the stacked structure are shown in the Fig. 3.5 and their respective spectrums are depicted in the Fig. 3.6. The current waveform in the Fig. 3.5 is approximating itself as a square-wave and hence reducing the overlap with the voltage waveform resulting in reduced power loss. The voltage waveform is basically a linear algebraic addition of the voltage swings across the HBTs Q_1 and Q_2. These voltage swings are depicted separately in the Fig. 3.7. It can be easily observed from the figure that the voltage waveform across the HBT Q_2 is half-sinusoidal thus satisfying the definition of Class-F^{-1} behavior. Current spectrum in the Fig. 3.6 is odd harmonic rich as the 3rd harmonic content is prominent due to the short-circuit loading at the collector of Q_2 at this frequency. Whereas, voltage spectrum shows higher 2nd harmonic content since the load appears to be open-circuited at this harmonic.

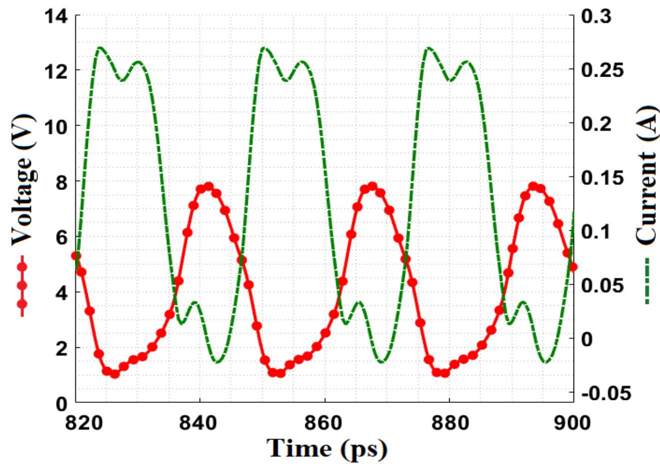


Fig. 3.5. Voltage and current waveforms at the collector terminal of power stage HBT (Q_2).

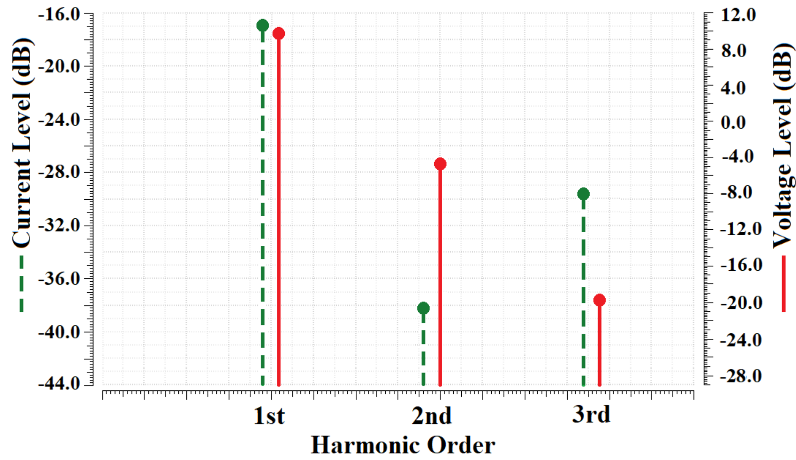


Fig. 3.6. Current and voltage spectrum up to the 3rd harmonic at the collector terminal of the power stage HBT (Q_2).

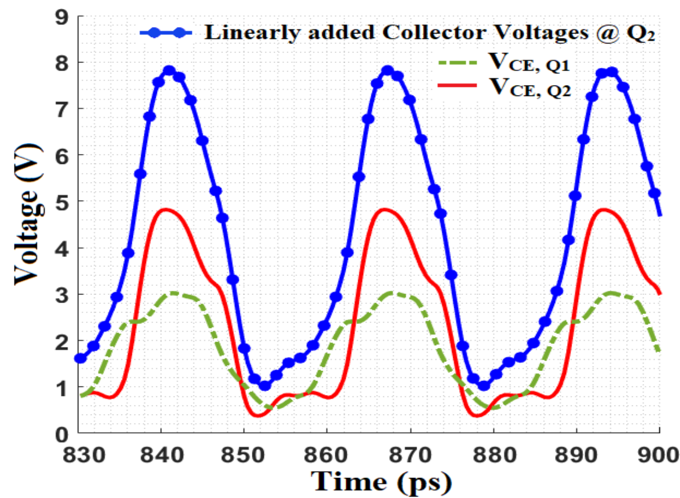
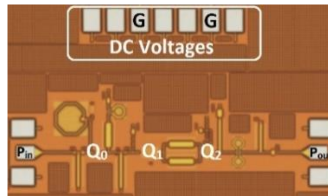


Fig. 3.7. V_{CE} voltage swings across the stacked HBTs Q_1 and Q_2 indicating algebraic sum at the stacked-stage output.

To mitigate the effect of the parasitic capacitances associated with the intermediate node of the stacked structure, inductive tuning technique [6] is utilized as shown in the Fig. 3.1. Inductive-tuning is accomplished by employing twin parallel-connected inductors (L_{N1} and L_{N2}) at the intermediate node with an equivalent inductance of 24 pH in order to neutralize the reactance of the parasitic capacitances, especially C_{P3} (~205 fF). Due to the large value of C_{P3} it is difficult to introduce a harmonic-control network at the collector node of the HBT Q_1. Moreover, if any such network is employed, it accrues component losses which negates the benefit of minor efficiency improvements (if any).

3.4 Measurement Results

Fig. 3.8(a) shows the photomicrograph of the implemented power amplifier chip fabricated in Global-Foundries (GF) 8HP 130 nm SiGe-BiCMOS process (f_T/f_{MAX}=200/265 GHz). The size of the PA is 1110 µm × 684 µm (excluding the pads). A Cascade Microtech Summit 11K probe station was used for on-wafer testing as shown in the Fig. 3.8(b). The On-wafer small-signal S-parameter measurements were made after performing standard SOLT calibration. Fig. 3.9 shows the measured S-parameter results for the bias-voltages of V_{CC1} (2 V) and V_{CC2} (4 V).



(a)

(b)

Fig. 3.8. (a) Chip photomicrograph of the fabricated SiGe-BiCMOS stacked Class-F^{-1} PA, (b) Cascade Microtech Summit 11000 Probe-Station test set-up for the on-wafer probing of the fabricated PA.

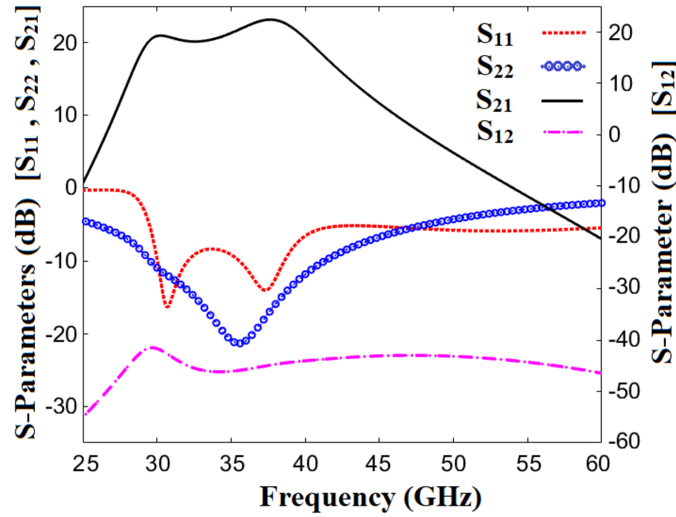


Fig. 3.9. Measured traces of S-parameters for the fabricated PA.

The measured S_{11} (input reflection co-efficient) and S_{22} (output reflection co-efficient) are less than −10 dB for a reasonable span of mm-wave frequencies indicating sufficient input and output matching behavior. In addition, a S_{21} (forward power–gain) of 20 – 23 dB in the range 29.5 – 40.3 GHz indicate high signal amplification. The center-frequency S-parameter values specifically at 38 GHz are S_{11}= −12.4 dB, S_{22}= −15.9 dB, S_{21}= 23 dB and S_{12}= −44.7 dB. The stability analysis indicates that the PA's stability factor (k) for the complete configuration is greater than 1 for the defined range of operating frequencies. For the purpose of large-signal measurements, the input and output power of the PA were measured employing a power-meter and power-sensors. Careful characterization and de-embedding of RF measurement path traces (cabling) was performed for the entire frequency range of interest. Large signal measurement results at 38 GHz operating-frequency are shown in the Fig. 3.10. The amplifier displays a power gain of 22.1 dB, saturated output-power, P_{SAT} of 21.2 dBm and, peak PAE of 30.1%. Output power at 1-dB compression point, OP_{-1dB} is 17.5 dBm. The PAE suffers some reduction due to several factors, such as lossy passive components associated with the matching circuits whose Q-factors are not very high. Moreover, the voltage and current waveforms at the collector terminal of the HBTs are not perfectly square or half-sinusoid and as a consequence there exists some voltage and current overlap resulting in power loss. The traces of P_{out} and PAE versus frequency are shown in the Fig. 3.11. P_{out} remains above 18 dBm from 33 to 42 GHz whereas PAE stays higher than 20 % from 34 to 42 GHz. Table 3.1 compares the Figure-of-Merit (FoM) of the proposed PA with recent

previously reported PAs in SiGe-BiCMOS process. The FoM is calculated using the International Technology Roadmap for Semiconductors (ITRS – now called as IRDS – International Roadmap for Devices and Systems) [10] formula shown below:

$$\text{FoM} = \text{P}_{\text{SAT}}(\text{dBm}) + \text{Gain}\ (\text{dB}) + 10.\log_{10}(\text{PAE}) + 20.\log_{10}(\text{Freq._GHz}) \tag{3.4}$$

It can be easily observed from the table that the proposed two-stage double-stacked Class-F^{-1} PA offers the highest FoM (69.68) achieved so far among integrated Class-F^{-1}/F PAs.

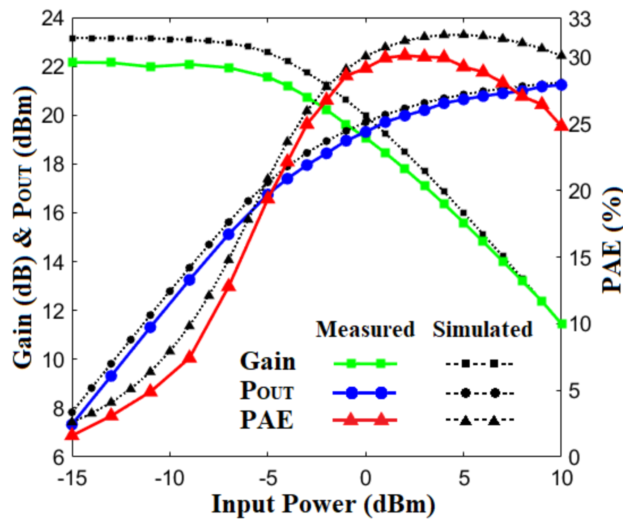


Fig.3.10. Simulated and measured performance parameter curves for the SiGe-BiCMOS stacked Class-F^{-1} PA: Gain, output power and PAE versus input power.

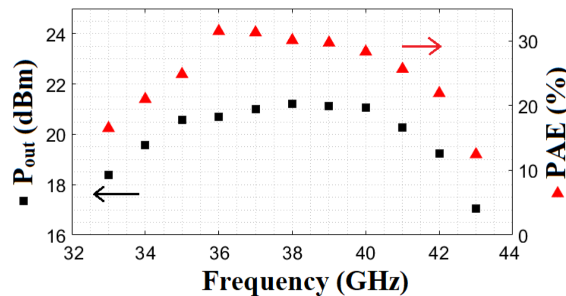


Fig. 3.11. Measured output power and PAE traces with respect to frequency for the fabricated PA.

TABLE 3.1
COMPARISON OF RECENTLY REPORTED SIGE-BICMOS PAS AND EVALUATION OF FIGURE-OF-MERIT (FOM)

Referenced Work	Technology	Amplifier's Class	Power Gain, G_p [dB]	Output Power, P_{SAT} [dBm]	PAE (%)	10.log [PAE]	Frequency (GHz)	20.log [Freq.]	ITRS Figure of Merit [FoM]
This Work	**0.13 µm SiGe**	**Double Stacked Class F^{-1}**	**22.1**	**21.2**	**30.1**	**14.78**	**38**	**11.6**	**69.68**
[2]	0.13 µm SiGe	Class F^{-1}/F	10.3	17.1	40.7	16.1	31	9.83	53.33
[3]	0.13 µm SiGe	Class F^{-1}	16.5	16.5	38.5	15.85	38	11.6	60.45
[4]	0.13 µm SiGe	Class F^{-1}	20	17	43.5	16.38	28.5	9.1	62.48
[7]	0.13 µm SiGe	Class F^{-1}	21.2	17.1	42	16.23	28	8.94	63.47
[8]	0.13 µm SiGe	Double Stacked Class E	14.5	23.6	34.9	15.43	41	12.26	65.79
[9]	0.13 µm SiGe	Triple Stacked Class E	15.4	22.5	20.8	13.18	40	12.04	63.12

3.5 Conclusion

A two-stage 38 GHz bipolar PA consisting of a Class-F driving-stage followed by a double-stacked Class-F^{-1} power-stage in GF 130-nm SiGe-BiCMOS (8HP) process is presented. The proposed PA achieves high gain through the two-stage implementation as well as sufficient PAE by incorporating suitable harmonic control network. In addition, double stacking was used in the power stage to achieve high output-power. This is a new result since transistor stacking has not been investigated/reported before for Class-F amplifiers. The considerable increase in gain and output-power of the fabricated double-stacked PA results in the highest ITRS FoM (69.68) achieved so far in state-of-the-art silicon-based Class-F Power Amplifiers. Considering frequencies of up to the 3rd harmonic, the stacked Class-F^{-1} design concept could be "suitably" implemented up to a center-frequency of 66 GHz using this GF SiGe technology with f_T/f_{MAX}=200/265 GHz.

References

[1] T. S. Rappaport, S. Sun, R. Mayzus, H. Zhao, Y. Azar, K. Wang, G. N. Wong, J. K. Schulz, M. Samimi and F. Gutierrez, "Millimeter-wave mobile communications for 5G cellular: It will work!," *IEEE Access*, vol. 1, pp. 335–349, May 2013.

[2] S. Y. Mortazavi and K.-J. Koh, "A class F^{-1}/F 24-to-31GHz power amplifier with 40.7% peak PAE, 15dBm OP_{1dB}, and 50mW P_{sat} in 0.13µm SiGe BiCMOS," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2014, pp. 254–255.

[3] S. Y. Mortazavi and K.-J. Koh, "Integrated inverse class-F silicon power amplifiers for high power efficiency at microwave and mm-Wave," *IEEE Journal of Solid State Circuits*, vol. 51, no. 10, pp. 2420–2434, Oct. 2016.

[4] T-W. Li, M-Y. Huang, and H. Wang, "Millimeter-Wave continuous-mode power amplifier for 5G MIMO applications," *IEEE Transactions on Microwave Theory and Techniques*, vol. 67, no. 7, pp. 3088–3098, Jul. 2019.

[5] A. V. Grebennikov, "Circuit design technique for high efficiency class F amplifiers," in *2000 IEEE MTT-S Int. Microwave Symp. Dig*., vol. 2, Jun. 2000, pp. 771-774

[6] H-T. Dabag, B. Hanafi, F. Golcuk, A. Agah, J. F. Buckwalter, and P. M. Asbeck, "Analysis and design of stacked-FET millimeter-wave power amplifiers," *IEEE Transactions on Microwave Theory and Techniques*, vol. 61, no. 4, pp. 1543–1556, Apr. 2013.

[7] S. Y. Mortazavi and K.-J. Koh, "A 28-GHz inverse class-F Power amplifier with coupled-inductor based harmonic impedance modulator," in *IEEE Custom Integr. Circuits Conf. (CICC)*, Sep. 2015, pp. 1–4.

[8] K. Datta, J. Roderick, and H. Hashemi, "Analysis, design and implementation of mm-wave SiGe stacked class-E power amplifiers," in *IEEE Radio Freq. Integr. Circuits Symp. (RFIC)*, Jun. 2013, pp. 275–278

[9] K. Datta and H. Hashemi, "Performance limits, design and implementation of mm-wave SiGe HBT class-E and stacked class-E power amplifiers," *IEEE Journal of Solid State Circuits*, vol. 49, no. 10, pp. 2150–2171, Oct. 2014.

[10] A. Chakrabarti and H. Krishnaswamy, "Multi-output stacked class-E millimetre-wave power amplifiers in 45 nm silicon-on-insulator metal–oxide–semiconductor: theory and implementation," *IET Microwaves, Antennas and Propagation,* vol. 9, no. 13, pp. 1425–1435, Oct. 2015.

CHAPTER NO. 4

INTEGRATED MICROWAVE POWER AMPLIFIER

Chapter 4 includes the research article, “A 6-GHz Integrated High-Efficiency Class-F^{-1} Power-Amplifier in 65-nm CMOS Achieving 47.8% Peak PAE”, published in *Electronics,* vol. 10, no. 20: 2450, Oct. 2021. DOI: 10.3390/electronics10202450.

The full text of the publication is included in this chapter without any modifications. However, there are formatting differences to keep the format the same for the thesis. The formatting modifications involve page setup, line spacing and font size.

A 6 GHz Integrated High-Efficiency Class-F^{-1} Power Amplifier in 65 nm CMOS Achieving 47.8% Peak PAE

4.1 Abstract

This paper reports a "single-transistor" Class-F^{-1} power amplifier (PA) in 65 nm CMOS, which operates at the microwave center frequency of 6 GHz. The PA is loaded with a Class-F^{-1} harmonic control network, employing a new "parasitic-aware" topology deduced using a novel iterative algorithm. A dual-purpose output matching network is designed, which not only serves the purpose of output impedance matching, but also reinforces the harmonic control of the Class-F^{-1} harmonic network. This proposed PA yields a peak power-added efficiency (PAE) of 47.8%, which is one of the highest when compared to previously reported integrated microwave/millimeter-wave PAs in CMOS and SiGe technologies. The amplifier shows a saturated output power of 14.4 dBm along with an overall gain of 13.8 dB.

4.2 Introduction

The exponential rise in the demand for a high data rate in cellular and WLAN communications requires the current systems to demonstrate their capability to handle the upcoming throughput requirements. In order to deal with this challenge, shifting the systems to higher frequency bands in the spectrum is the only viable solution. A significant module in wireless systems is the power amplifier (PA). Integrated power amplifiers operable at microwave/millimeter-wave frequencies focusing 5G-communications are expected to demonstrate high efficiency and wideband operation within a small form factor. In a transceiver system, the power amplifier is the most dissipative module, which consumes power from the system's battery. Hence, in order to extend the battery life in portable devices, it is imperative to design a power amplifier that demonstrates a high power efficiency [1–5]. Moreover, recently, the Federal Communications Commission (FCC) has also emphasized maximizing the battery life of the client device operating at the new unlicensed 6 GHz band (5.925 GHz to 7.125 GHz) [5]. Therefore, there is a crucial need for a 6 GHz power amplifier that exhibits high efficiency and thereby improves the battery life of the client device.

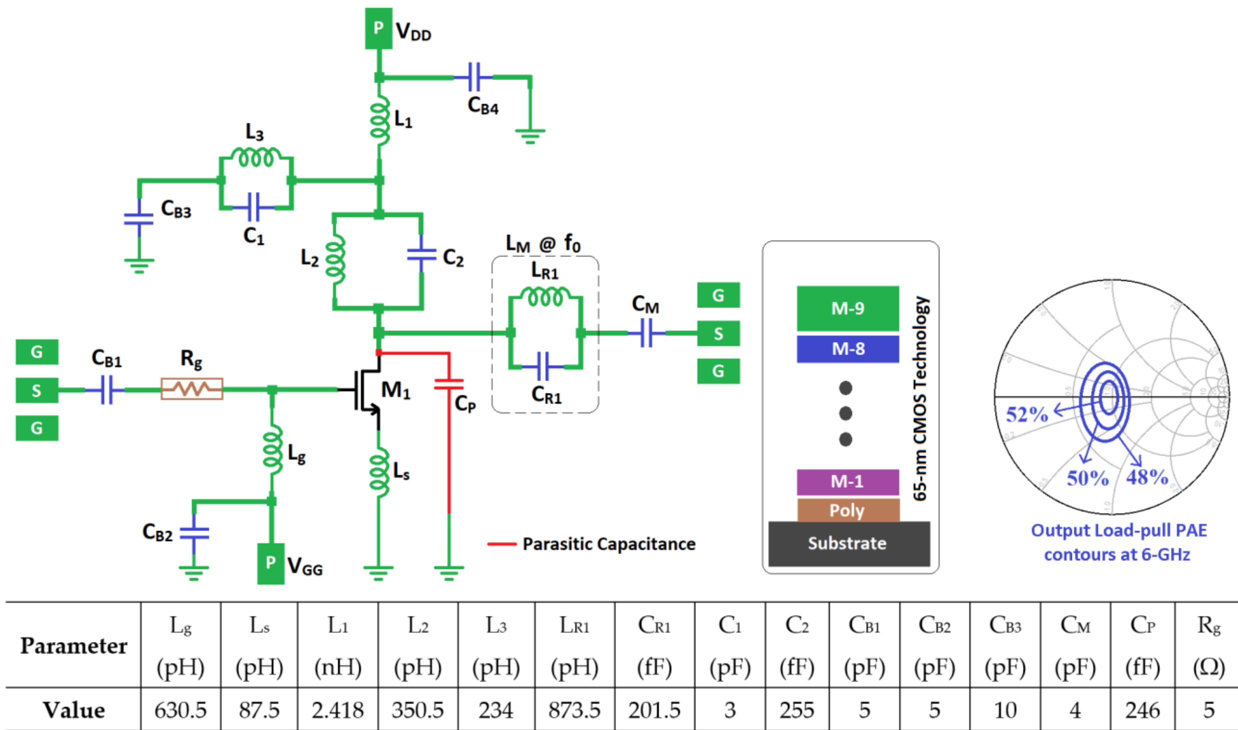
"Single-Transistor" PAs are desirable for 5G-mobile communications as they offer low-voltage operation, a small form factor, and a high power-added efficiency (PAE) if the PA is harmonically tuned. Moreover, the "single-transistor" approach incurs lower power consumption and, hence, naturally exhibits superior power efficiency over the multi-transistor approach (e.g., cascode or stacked, etc.). The term "single-transistor" means transistors are merged (shunted) in a parallel combination but are represented as one device in the circuit. "Single-transistor" integrated Class-F/F^{-1} power amplifiers operable at "5G-millimeter-wave frequencies" have been investigated in recent years. However, an integrated "single-transistor" Class-F/F^{-1} power amplifier operable at a "5G-microwave frequency" of 6 GHz has not been reported so far in the literature. A single-transistor millimeter-wave Class-F/F^{-1} power amplifier in SiGe-BiCMOS was reported in [6]. This power amplifier employed a wave-shaping network connected at the collector node of the active device, which allows it to transform from Class-F^{-1} to Class-F when the frequency shifts from 24 GHz to 31 GHz. The amplifier was operating at 2.2 V and delivered 40.7% PAE along with a gain of 10.3 dB and an output power of 17.1 dBm. Very recently, a 65 nm CMOS single-transistor Class-F power amplifier operable at 5G-millimeter-wave frequencies was reported in [7]. The 1.1 V driven power amplifier rendered 46.4% peak PAE, a power gain of 10 dB along with an output power of around 14.75 dBm. To the best of the author's knowledge, this paper reports the first "single-transistor" integrated Class-F^{-1} power amplifier operable at a "5G-microwave frequency" of 6 GHz. The amplifier is designed in 65 nm CMOS technology. The proposed design employs a "parasitic-aware" Class-F^{-1} harmonic control network connected at the drain terminal of the NMOS device. There are several Class-F^{-1} circuit topologies based on the LC network [6–10]; however, the proposed Class-F^{-1} LC-network is a new topology deduced using a novel iterative algorithm. A dual-purpose output matching network is incorporated in the design, which reinforces the waveform-shaping capability of the Class-F^{-1} harmonic network along with performing the typical task of output impedance matching. The proposed amplifier offers one of the highest PAEs (47.8%) compared to many other monolithic microwave/millimeter-wave CMOS and SiGe power amplifiers reported so far.

This paper is organized as follows. Section 4.3 describes the details of the Class-F^{-1} amplifier's circuit topology, which includes a harmonic control network and dual-purpose output matching circuit. Moreover, the section also explains in detail the iterative algorithm employed to extract

the component values of the harmonic network. Measurement results and a comparison table are reported in Section 4.4. Finally, Section 4.5 concludes the work presented in this paper.

4.3 Single-Transistor Class-F^{-1} Power Amplifier

Figure 4.1 shows the proposed Class-F^{-1} PA using a “single-transistor” approach, implemented in 65 nm TSMC CMOS technology. The active device in the design employs an NMOS transistor M_1. The total width of the device (W_T) is 384 µm, which is divided into six power-cell units. Each power-cell unit contains 32 fingers (N_f), and each finger is 2 µm wide (W_f). The amplifier is biased, with a drain supply V_{DD} of 1.1 V and gate supply V_{GG} of 480 mV. A 5 Ω resistor (R_g) and a small inductor (L_s) are incorporated, respectively, at the gate and at the source of the transistor for the purpose of establishing unconditional stability for the power amplifier.



Parameter	L_g (pH)	L_s (pH)	L_1 (nH)	L_2 (pH)	L_3 (pH)	L_{R1} (pH)	C_{R1} (fF)	C_1 (pF)	C_2 (fF)	C_{B1} (pF)	C_{B2} (pF)	C_{B3} (pF)	C_M (pF)	C_P (fF)	R_g (Ω)
Value	630.5	87.5	2.418	350.5	234	873.5	201.5	3	255	5	5	10	4	246	5

Fig. 4.1. Circuit diagram of the proposed single-transistor class-F^{-1} PA in TSMC 65-nm CMOS and its load-pull PAE contours at 6-GHz. The figure also shows the BEOL stacked metal layers of the technology with color-coded-scheme (reflecting the corresponding components in the schematic), as well as the values of the component parameters.

The drain terminal is loaded with a novel "parasitic-aware" Class-F^{-1} harmonic control network, which harvests the parasitic capacitance C_P (246 fF) in its implementation. The parallel resonant tank (L_2, C_2) behaves as an inductor at the fundamental frequency f_0, and combines its inductance with L_1 to tune out the parasitic capacitance C_P. However, the tank circuit (L_3, C_1) resonates at f_0 to create an open circuit, and, hence, does not interrupt the fundamental frequency's path to resonate out the C_P. At the second harmonic frequency $2f_0$, the resonant tank (L_2, C_2) acts again as an inductor, which resonates out the parasitic capacitance C_P. However, the tank circuit (L_3, C_1) becomes overall capacitive at $2f_0$ and constitutes a low impedance path to the ground, thereby discarding the presence of the inductor L_1 and leaving the second harmonic to resonate with the remaining circuit, whereas at $3f_0$, the tank (L_2, C_2) becomes capacitive and constitutes a series LC resonant circuit with the inductor L_1 resulting in the formation of a short circuit path to the AC ground. A second short circuit path for the third harmonic is also established by the tank circuit (L_3, C_1), which behaves as an overall capacitor, thus dumping $3f_0$ into ground. Hence, with the help of this passive frequency-steering the employed harmonic network accomplishes the requirements for Class-F^{-1} loading.

In order to determine the values of the inductors (L_1, L_2) and the capacitor C_2, a novel "educated" and deterministic iterative technique is employed. It begins by inserting an incremental capacitance value, ΔC in (4.1) in each kth iteration step of contiguous steps and then executing and validating a sequence of equations in a loop to finally extract the required reactive component values. The following equations are loaded in MATLAB in a routine and then the values of the components C_2, L_1, and L_2 are extracted instantly at the end of the iterative search.

$$C_2 = [\Delta C]_k + C_P \tag{4.1}$$

where $[\Delta C]_k$ is an incremental value in fF (such as 1fF, 3fF, 7fF, etc.) at the kth step, with k = 1, 2, 3….n. Additionally, in the equations below, f_{1o}, f_{2o}, and f_{3o} are the fundamental, 2nd and 3rd harmonics of the 6 GHz microwave center frequency, while f_{0R}, f_{2R}, and f_{3R} are the calculated resonance frequencies in each iteration. In addition, $L_{eq@2fo}$ and $X_{Leq@2fo}$ are, respectively, the required equivalent inductance and the corresponding inductive reactance of the parallel resonant tank (L_2, C_2) to tune out C_P at the 2nd harmonic. Further, $X_{Ceq@3fo}$ and $C_{eq@3fo}$ are, respectively, the equivalent capacitive reactance and the corresponding equivalent capacitance of the tank (L_2,

C_2) at the 3rd harmonic. Finally, $X_{Leq@fo}$ and $L_{eq@fo}$ are, respectively, the equivalent inductive reactance and the corresponding equivalent inductance of the tank (L_2, C_2) at the fundamental frequency. The parasitic "C_P" thus provides the starting "educated" search reference for C_2, while L_1 and L_2 are found deterministically using C_2. It is thus different from any "brute force" algorithm, which may employ roughly estimated trial values. Now, for this proposed iterative technique:

$$L_{eq@2fo} = \frac{1}{\left(2\pi f_{2o}\right)^2 C_P} \tag{4.2}$$

$$X_{Leq@2fo} = 2\pi f_{2o} L_{eq@2fo} \tag{4.3}$$

$$X_{C2@2fo} = \frac{1}{2\pi f_{2o} C_2} \tag{4.4}$$

$$X_{L2@2fo} = \frac{\left(X_{Leq@2fo} X_{C2@2fo}\right)}{\left(X_{C2@2fo} + X_{Leq@2fo}\right)} \tag{4.5}$$

$$L_2 = \frac{X_{L2@2fo}}{2\pi f_{2o}} \tag{4.6}$$

$$f_{2R} = \frac{1}{2\pi\sqrt{L_{eq@2fo} C_P}} \tag{4.7}$$

$$X_{L2@3fo} = 2\pi f_{3o} L_2 \tag{4.8}$$

$$X_{C2@3fo} = \frac{1}{2\pi f_{3o} C_2} \tag{4.9}$$

$$X_{Ceq@3fo} = \frac{\left(X_{L2@3fo}\ X_{C2@3fo}\right)}{\left(X_{L2@3fo} - X_{C2@3fo}\right)} \tag{4.10}$$

$$C_{eq@3fo} = \frac{1}{\left(2\pi f_{3o} X_{Ceq@3fo}\right)} \tag{4.11}$$

$$L_1 = \frac{1}{\left(2\pi f_{3o}\right)^2 C_{eq@3fo}} \tag{4.12}$$

$$f_{3R} = \frac{1}{2\pi\sqrt{L_1 C_{eq@3fo}}} \tag{4.13}$$

$$X_{L2@fo} = 2\pi f_o L_2 \tag{4.14}$$

$$X_{C2@fo} = \frac{1}{2\pi f_o C_2} \tag{4.15}$$

$$X_{Leq@fo} = \frac{\left(X_{L2@fo}\ X_{C2@fo}\right)}{\left(X_{C2@fo} - X_{L2@fo}\right)} \tag{4.16}$$

$$L_{eq@fo} = \frac{X_{Leq@fo}}{2\pi f_o} \tag{4.17}$$

$$L_T = L_1 + L_{eq@fo} \tag{4.18}$$

$$f_{0R} = \frac{1}{2\pi\sqrt{L_T C_P}} \tag{4.19}$$

Since the parameters C_P = 246 fF (captured through parasitic extraction incorporating the transistor's parasitic capacitance (C_{ds}) plus parasitics associated with the layout interconnects), f_{1o} = 6 GHz, f_{2o} = 12 GHz, and f_{3o} = 18 GHz are known, they are used to extract the required component values by employing the above iterative technique.

It can be seen from the above equations and Table 4.1 that the required resonance conditions at the 2nd and 3rd harmonics (f_{2R} and f_{3R}) are automatically in agreement, and satisfaction of the resonance condition at the fundamental harmonic, f_{0R}, is the validating parameter in this iterative component extraction method. For the first three iteration values of ΔC, the deduced reactive components resonate close to f_{0R}, but for the last iteration value of ΔC (=9fF), f_{0R} comes exactly to 6 GHz thereby completing the component search. It can be noted that the proposed algorithm starts from a specific reference value and quickly converges to the solution, as shown in the table. It is judiciously designed around a single parameter, i.e., a parasitic capacitance, and, hence, is different from other optimization algorithms, which perform a search based on arbitrary values of the various parameters.

TABLE 4.1
COMPARISON OF RESULTS EXTRACTED BY THE ITERATIVE TECHNIQUE

ΔC (fF)	C_2 (fF)	L_1 (nH)	L_2 (pH)	f_{3R} (GHz)	f_{2R} (GHz)	f_{0R} (GHz)
1	247	2.80	357	18	12	5.66
2	248	2.75	356	18	12	5.7
5	251	2.59	354	18	12	5.8
9	255	2.42	351	18	12	**6.0**

Determining the component values of the tank circuit (L_3, C_1) constitutes a separate sub-problem and have been evaluated for resonance at f_0 and for equivalent capacitive AC-bypass to ground at $2f_0$ and $3f_0$. Hence, setting C_1 to a suitable value of 3 pF, L_3 can be easily deduced as follows:

$$L_3 = \frac{1}{(2\pi f_o)^2 C_1} = 234 \text{ pH} \tag{4.20}$$

For the purpose of satisfying the Class-F^{-1} condition, the output-matching network also has to present an open-circuit to the second harmonic so that this harmonic would reflect back towards the drain of the active device. A simple output-impedance matching can be established by just using the two components, inductor L_M and capacitor C_M; however, in order to stop the second harmonic from propagating towards the load, a simple technique is employed. In this technique, the inductor L_M (1.165 nH) is judiciously decomposed into a $2f_0$-tank circuit by employing the design equations below:

$$L_{R1} = \frac{3}{4} L_M = 873.75 \text{ pH} \tag{4.21}$$

$$C_{R1} = \frac{1}{4\omega_0^2 L_{R1}} = 201.5 \text{ fF} \tag{4.22}$$

The above-mentioned design equations can be used to convert any inductor into a $2f_0$-tank-circuit. The tank-circuit (L_{R1}, C_{R1}) offers an open-circuit to the second-harmonic and behaves as the inductor L_M at the fundamental. Hence, the proposed output-matching network adds the second harmonic content at the NMOS drain terminal. This causes further refinement in the voltage

waveform, resulting in a reduction in the current–voltage overlap and hence, improving the power-added efficiency.

The proposed Class-F^{-1} harmonic control network, along with the dual-purpose output-matching network connected at the drain of the NMOS transistor, performs the desired wave-shaping operation as shown in Fig. 4.2. The voltage waveform approximates itself as a half-sinusoidal wave as the second harmonic content is dominant, whereas the current waveform is approximating itself as a square wave due to the higher third harmonic content (Fig. 4.3). Load impedance observed from the drain terminal of the NMOS device (Fig. 4.4) maintains a constant impedance close to the optimum value of 50 Ω at the fundamental frequency (f_0). The impedance trace depicts a high impedance at the second harmonic frequency ($2f_0$) and low impedance at the third harmonic frequency ($3f_0$). The input impedance matching is realized with the help of a DC-blocking capacitor, C_{B1}, as shown in Fig. 4.1. The output load-pull simulations of the power amplifier offer around 52% peak PAE at 6 GHz, as indicated by the contours on the Smith chart in Fig. 4.1.

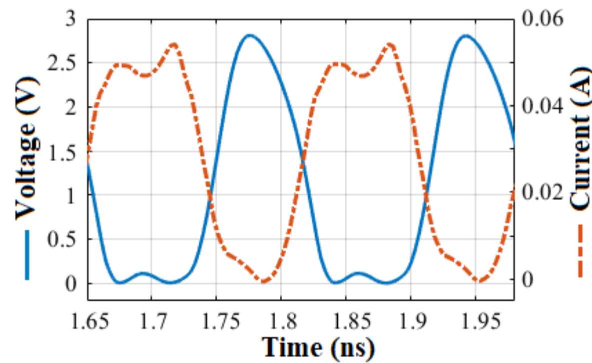


Fig. 4.2. Voltage and current waveforms at the drain of the NMOS device.

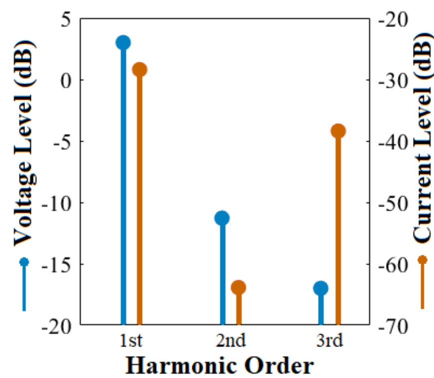


Fig. 4.3. Voltage and current Spectrum up to the 3rd harmonic frequency.

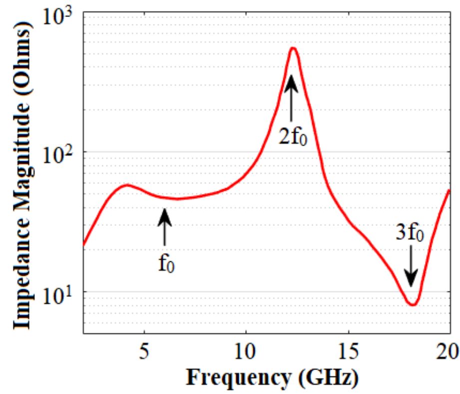


Fig. 4.4. Impedance trace as a function of frequency.

4.4 Measurement Results

Figure 4.5 shows the photomicrograph of the implemented power amplifier employing the 65 nm TSMC CMOS process with a PA size of 753 µm × 927 µm. A Cascade Micro-Tech Summit 11K probe-station along with infinity-quad-probe (50 GHz RF and 100-µm pitch) and a Rohde & Schwarz ZVA50 Vector Network Analyzer were employed for on-wafer testing, as shown in Fig. 5. Standard SOLT calibration was performed for the purpose of on-wafer small-signal S-parameter measurements with the results shown in Fig. 4.6. The measured S_{11} and S_{22} values are under −10 dB for a considerable range of frequencies of interest. The measured maximum S_{21} was 14.1 dB along with a −3dB range of 3.67–7.4 GHz, thus offering a 3.7 GHz wide small-signal bandwidth (BW_{3dB} = 67.4%). Stability analysis reveals that the amplifier's stability factor (k) is greater than 1, as shown in Fig. 4.7, ensuring unconditional stability of the proposed power amplifier.

Large signal measurements were conducted with the help of a power meter and power sensors. The measured results captured at the operating frequency of 6 GHz are shown in Fig. 4.8. The amplifier exhibits a peak power-added efficiency (PAE) of 47.8%, saturated output power, P_{SAT}, of 14.4 dBm and, a power gain of 13.8 dB. The output power at the 1 dB compression point, OP_{-1dB}, is 12.9 dBm. Fig. 4.9 shows the measured PAE traces from 5 GHz to 7 GHz with respect to the input power. P_{OUT} stays above 12 dBm from 3.5 GHz to 7.5 GHz, whereas PAE remains higher than 30% from 4 GHz to 7.5 GHz, as shown in Fig. 4.10. Normalized AM–AM and AM–PM distortion curves are depicted in Fig. 4.11. The measured AM–PM distortion at $P_{in, -1dB}$ (6 dBm) is less than 2°, indicating good linearity performance.

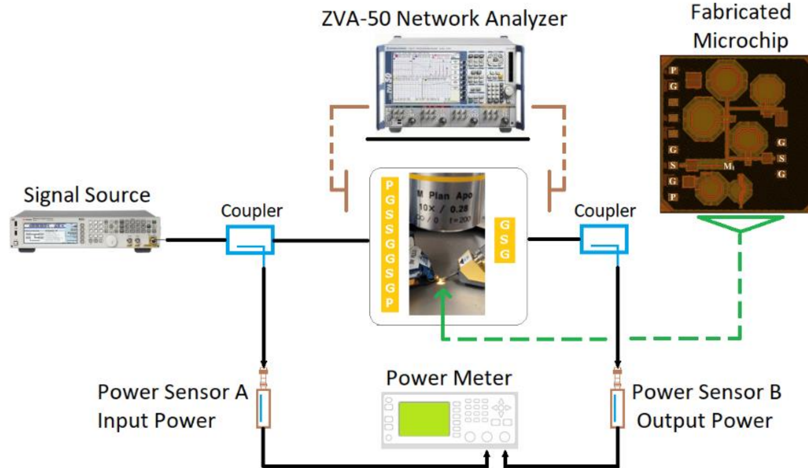


Fig. 4.5. Chip photomicrograph of the fabricated 65 nm CMOS class-F^{-1} PA and Cascade Microtech Summit 11K probe-station test set-up.

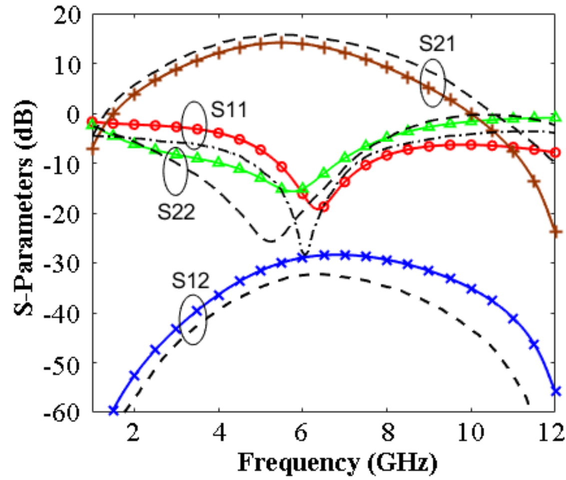


Fig. 4.6. Simulated (black dotted) and measured (colored solid) traces of S-parameters for the fabricated PA.

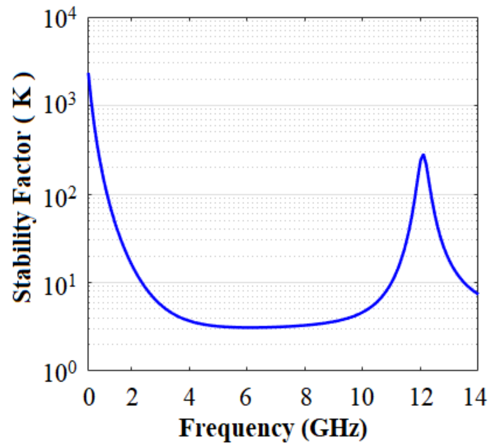


Fig. 4.7. Stability curve.

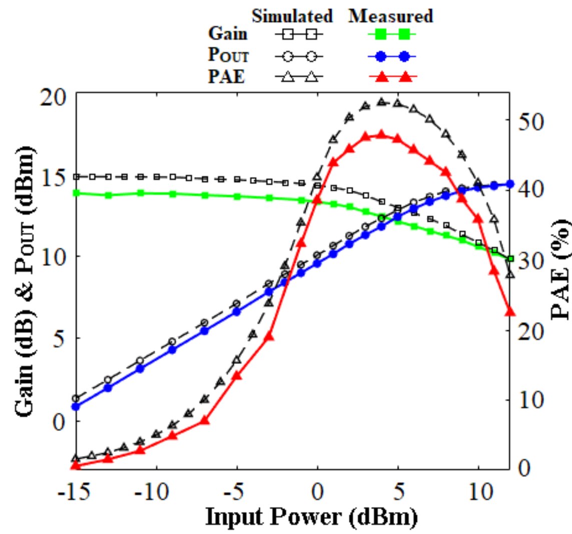


Fig. 4.8. Simulated and measured performance parameter traces for the proposed PA: output power, gain, and PAE versus input power.

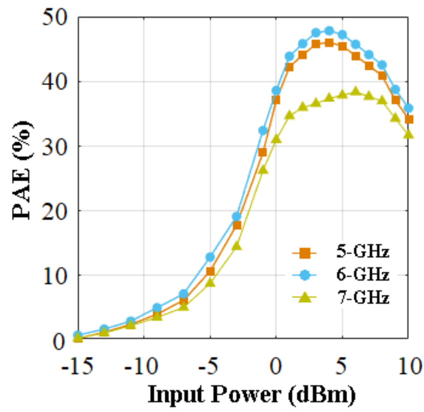


Fig. 4.9. Measured PAE traces at different frequencies.

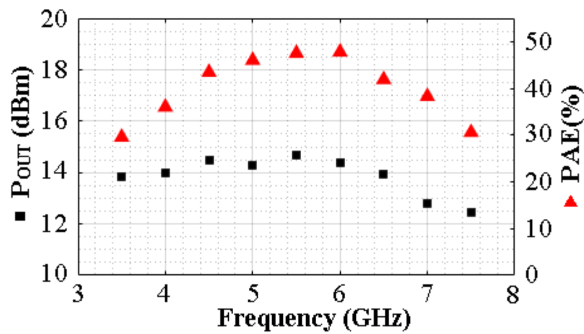


Fig. 4.10. Measured PAE and output power traces versus frequency for the fabricated class-F^{-1} PA.

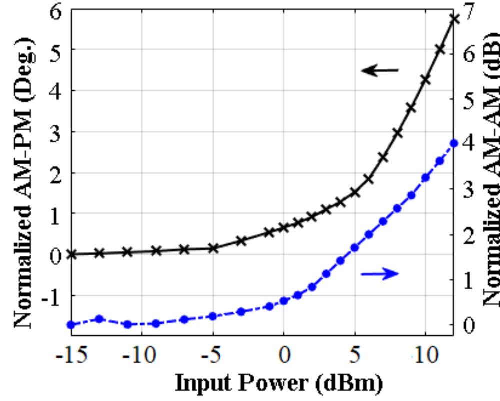


Fig. 4.11. Measured AM–AM and AM–PM distortion across input power.

TABLE 4.2
COMPARISON OF RECENTLY REPORTED CMOS AND SIGE-BICMOS PAS

Referenced Work	Process Technology	Architecture	Amplifier's Class	Freq. (GHz)	Gain [dB]	P_{SAT} [dBm]	Peak PAE (%)	Supply Voltage (V)	Area on-chip (mm^2)
This Work	**65-nm CMOS**	**Single Transistor**	**Class F^{-1}**	**6**	**13.8**	**14.4**	**47.8**	**1.1**	**0.69**
[6]	130-nm SiGe	Single Transistor	Class F^{-1}/F	31	10.3	17.1	40.7	2.2	0.27
[7]	65-nm CMOS	Single Transistor	Class F	29	10	14.75	46.4	1.1	0.12*1
[11]	180nm CMOS	Cascode Stages	Class F^{-1}	4.6	11.6	27.8	32	3.6	2.32
[12]	65-nm CMOS	Differential	Class E/F	6	N/A	25.6	34*2	1.8	9.03
[13]	250-nm SiGe	Push-pull Stages	Class AB	6	12	24	24.7	1.8	2.08
[14]	65-nm CMOS	Differential	Class AB	6	23.6	22.4	28.4	3.3	0.89
[15]	65-nm CMOS	Differential Cascode	Class AB	6	19.4	18.9	27.9	3	0.73*3

*1 Area without pads (Active area). *2 Drain Efficiency. *3 Circuit is not fully integrated (Output matching network is off-chip). Green Shading: mm-Wave PAs. Blue Shading: Single-Transistor.

Table 4.2 compares the proposed PA with several previously reported PAs in CMOS and SiGe. It can be easily inferred from Table 4.2 that the proposed amplifier yields the highest peak PAE (47.8%) as compared to the referenced papers. According to the author's knowledge, there are no

“single-transistor” integrated microwave Class-F/F^{-1} PAs that have been reported so far; however, two millimeter-wave Class-F/F^{-1} PAs with similar “single-transistor architecture” have been reported, and these have been included in the table, although they are in a totally different RF spectrum compared to the other PAs in the table. The proposed PA offers a very high efficiency and operationwise reasonable output power. The saturated output power of 14.4 dBm resides within the designated power limits outlined by the FCC [5] for establishing 5G communications at 6 GHz. Moreover, this power level helps to extend the client device battery life as well. Table 4.2 also shows that when compared to other 6 GHz power amplifiers, the proposed PA offers low-voltage operation (1.1 V) and small form factor.

4.5 Conclusion

A highly power-efficient Class-F^{-1} PA for 5G communications at 6 GHz, employing a “single-transistor” design implemented in 65nm CMOS, is proposed. The amplifier employs an iterative algorithm-based parasitic-aware harmonic control network along with a dual-purpose output-matching network. The amplifier offers a low-cost, low-voltage driven, area-constrained, wideband, and a highly power-efficient PA for establishing 5G communications at 6 GHz.

References

[1] A. Grebennikov and F. H. Raab, “History of class-F and inverse class-F techniques,” *IEEE Microwave Mag*, vol. 19, no. 7, pp. 99–115, Dec. 2018.

[2] A. Vasjanov and V. Barzdenas, “A review of advanced CMOS RF power amplifier architecture trends for low power 5G wireless networks,” *Electronics*, vol. 7, no. 271, Oct. 2018.

[3] L. Kouhalvandi, O. Ceylan and S. Ozoguz, “A review on optimization methods for designing RF power amplifiers,” *IEEE Int. Conf. on Electrical & Electronics Engineering (ELECO)*, Busa, Turkey, Nov. 28–30, 2019, pp. 375–378.

[4] S. Gao, “High-efficiency class F RF/microwave power amplifiers,” *IEEE Microwave Mag*, vol. 7, no. 1, pp. 40–48, Feb. 2006.

[5] Federal Communications Commission, (2020, Apr. 2), *FCC Fact Sheet: Unlicensed use of the 6-GHz band*. [Online], Available: https://docs.fcc.gov/public/attachments/DOC-363490A1.pdf (accessed on Apr. 06, 2020).

[6] S. Y. Mortazavi and K.-J. Koh, "A class F^{-1}/F 24-to-31GHz Power Amplifier with 40.7% Peak PAE, 15dBm OP_{1dB}, and 50mW P_{sat} in 0.13μm SiGe BiCMOS," in *IEEE Int. Solid-State Circuits Conf. (ISSCC)*, San Francisco, CA, USA, Feb. 9–13, 2014, pp. 254–255.

[7] S. N. Ali, P. Agarwal, S. Gopal S. Mirabbasi and D. Heo, "A 25-35 GHz neutralized continuous class-F power amplifier for 5G mobile communications achieving 26% modulation PAE at 1.5 Gb/s and 46.4% peak PAE," *IEEE Transactions on Circuits* and *Systems-I, Reg. Papers*, vol. 66, no. 2, pp. 834–847, Feb. 2019.

[8] S. Y. Mortazavi and K.-J. Koh, "Integrated inverse class-F silicon power amplifiers for high power efficiency at microwave and mm-wave," *IEEE J. Solid-State Circuits*, vol. 51, no. 10, pp. 2420–2434, Oct. 2016.

[9] S. Y. Mortazavi and K.-J. Koh, "A 28-GHz inverse class-F power amplifier with coupled-inductor based harmonic impedance modulator," in *Proc. IEEE Custom Integr. Circuits Conf. (CICC)*, San Jose, CA, USA, Sep. 28–30, 2015, pp. 1–4.

[10] S. M. A. Ali, S. M. R. Hasan, "A 38-GHz Millimeter-Wave Double-Stacked HBT class-F^{-1} High-Gain Power Amplifier in 130-nm SiGe-BiCMOS." *IEEE Transactions on Microwave Theory and Techniques*, vol. 68, no. 7, pp. 3039–3044, May 2020

[11] F. Chen, Y. Wang, Y.-H. Hsiao, J.-L. Lin. Y.-C. Chen and H. Wang, "A 4.6-GHz class-F^{-1} high power CMOS power amplifier," in *IEEE Int. Symp. on Radio-Freq. Integr. Tech.(RFIT)*, Seoul, Korea, Sep. 2017, pp. 183–185.

[12] H. Wang and H. Hashemi, "A 0.5–6GHz 25.6 dBm fully integrated digital power amplifier in 65-nm CMOS," in *Proc. IEEE Radio Freq. Integr. Circuits Symp. (RFIC)*, Tampa, FL, USA, Jun. 1–3, 2014, pp. 409–412.

[13] D. Gruner and G. Boeck, "Fully integrated 5.6–6.4 GHz power amplifier using transformer combining," in *Ph.D. Research in Microelectronics and Electronics*, Cork, Ireland, Jul. 12–17, 2009, pp. 160–163.

[14] W. Ye, K. Ma and K. S. Yeo, “A 2-to-6 GHz class-AB power amplifier with 28.4% PAE in 65nm CMOS supporting 256 QAM,” in *IEEE Int. Solid-State Circuits Conf. (ISSCC)*, San Francisco, CA, USA, Feb. 22–26, 2015, pp. 38–39.

[15] J. Lindstrand, M. Tormanen and H. Sjoland, “A decade frequency range CMOS power amplifier for sub-6-GHz cellular terminals,” *IEEE Microwave and Wireless Component Letters*, vol. 30, no. 1, pp. 54–57, Jan. 2020.

CHAPTER NO. 5

MILLIMETERWAVE ON-CHIP ANTENNA

Chapter 5 includes the research article, "An On-Chip Planar Inverted-F Antenna at 38-GHz for 5G Communication Applications", published in *International Journal of Antennas and Propagation,* vol. 2022, Article ID 1017816, 7 pages, 2022. DOI: 10.1155/2022/1017816

The full text of the publication is included in this chapter without any modifications. However, there are formatting differences to keep the format the same for the thesis. The formatting modifications involve page setup, line spacing and font size.

An On-Chip Planar Inverted-F Antenna at 38-GHz for 5G Communication Applications

5.1 Abstract

This thesis presents an On-Chip Planar Inverted-F Antenna (PIFA) implemented in TSMC 180-nm CMOS process technology. The antenna operates at 5G millimeterwave center-frequency of 38-GHz. Ultra-Thick Metal (UTM) layer of the technology is utilized to implement the on-chip antenna. The OCA is positioned close to the edge of the microchip for improving the gain-performance. The open end of the antenna is folded to develop a top-loaded PIFA structure yielding better 50-Ω impedance matching and wider bandwidth. On-wafer measurements are conducted through the Cascade Microtech Summit 11K probe-station and ZVA-50 vector network analyzer to measure the return loss and gain of the fabricated on-chip antenna. The measurements are performed after placing the fabricated OCA over a 3D-printed plastic slab to minimize the reflections from the metallic-chuck of the probe-station. The measurement results show that the fabricated on-chip PIFA achieves a minimum return loss of 14.8 dB and a gain of 0.7 dBi at the center-frequency of 38-GHz. To the best of the authors' knowledge, the presented OCA is the first On-Chip PIFA designed, fabricated and tested at the 5G millimeterwave frequency of 38-GHz.

5.2 Introduction

The millimeterwave frequencies have recently gained enormous attention among research circles because of their capability of providing high data rate for 5G communication systems. As millimeterwave (mmW) frequencies exhibit relatively smaller wavelengths therefore, it becomes feasible to design antennas on microchips using standard CMOS processes. Millimeterwave on-chip antennas (OCAs) offer a high-level of integration with RF-front-end circuitry, external interconnect-free interface and low fabrication cost. The on-chip antenna (OCA) can overcome the last barrier to realize a truly integrated RF system [1]. A potential candidate for next-era cellular communications at millimeterwave frequencies is 38-GHz due to its minimum atmospheric absorption characteristics [2]. Therefore, in this work, 5G millimeterwave frequency of 38-GHz is selected for designing an on-chip antenna.

Several on-chip antenna structures have been reported in the literature and most of these OCAs were designed to operate at the millimeterwave frequency of 60-GHz. In [3], a straight-line PIFA fabricated in Standard CMOS process technology was proposed. The OCA was operable at the millimeter-wave frequency of 60-GHz. The antenna was excited at the fourth-order mode resulting in an increased antenna footprint. The measurement results showed that the OCA yielded an absolute gain of -19 dBi. A PIFA has a very strong dependence on the ground-plane and the OCA in [3] was designed without a ground-plane thereby causing significant deterioration in antenna-gain. A meander-line On-Chip PIFA fabricated in TSMC 180-nm CMOS process technology was proposed in [4]. The OCA was excited at a 5G millimeterwave frequency of 60-GHz and produced an absolute-gain value of -15.7 dBi. The OCA's meandered section, residing at the edge of the microchip, helped to reduce the overall antenna length however, a considerable part of the antenna body remained away from the edge of the microchip causing reduction in radiation efficiency. Moreover, the work did not show the dimensions of the antenna thereby providing no information on the width and length of the fabricated OCA. A 60-GHz triangular monopole antenna-on-chip in 180-nm process technology was designed in [5]. Gain of the antenna was attempted to be improved with the help of artificial magnetic conductors (AMCs). Simulation results showed that the antenna produced a gain of 2.5 dBi. A 60-GHz On-Chip patch antenna in 180-nm CMOS technology was presented in [6]. The measurement results indicated that the antenna offered a gain performance of around -2.2 dBi in the frequency range between 50 to 70 GHz. Very recently a monopole on-chip antenna fabricated in 65-nm CMOS technology was proposed in [7]. The OCA reported an antenna-gain of 0-dBi at 60-GHz. Apart from the above-mentioned OCAs, there were several other OCAs excited at the millimeterwave frequency of 60-GHz [8]−[10] however, a 38-GHz triangular monopole on-chip antenna was reported in [11]. The OCA was designed with AMCs in 28-nm CMOS process technology. The work presented simulation results only. The OCA showed an antenna-gain of -1.75 dBi and occupied a considerably huge area of more than 4 mm^2 on microchip. The metal width of the OCA was 8µm which is very narrow and thus contributed to constraining the antenna-gain. Moreover, the simulation-based OCA did not discuss the requirements of the metal-fill density and the practical feasibility of such a large (more than 4-mm^2) exclusion-area, essential for proper operation of the antenna on microchip. In simulations related to on-chip antennas, a designer can ignore the exclusion area limitation but practically the scenario appears to be quite different.

A large metallic area like a patch or similar structure constructed using the top-most metal layer of CMOS technology has the potential to suffer micro-fracture, hence, in this work, a planar inverted-F antenna comprising of a few metallic-lines is selected to avoid such a risk. Moreover, a favorable feature of PIFA with regards to on-chip integration is its small vertical dimension. It enables the antenna to be implemented at one of the chip's edges thereby facilitating the antenna to radiate readily in the free space and hence minimizing the absorption of electromagnetic radiation within the silicon substrate. As PIFA has both horizontal and vertical elements therefore, it can perform in both horizontal and vertical polarizations. The performance of PIFA with two-polarizations helps to improve the reception in WPAN environments. The input impedance of a PIFA can be set by adjusting the distance between the shorting stripe and the feeding stripe. The input impedance can be tuned to an appropriate value to match the source impedance without making use of an additional circuit between the source and the antenna. PIFA offers a small form factor as it is only quarter-wavelength long and therefore, it can easily fit inside an already space-constraint environment of a microchip. Moreover, a PIFA has a strong connection with the ground plane through its shorting stripe therefore, as compared to other antennas, it naturally behaves in a very robust manner when operating close to metallic objects, which have the tendency to affect the radiation capabilities of an antenna. This fact is particularly important in microchip environment where a Design Rule Check (DRC) called as "pattern density" is a ritual that needs to be satisfied. Therefore, a PIFA can better tolerate the presence of the metal-fill chunks in its vicinity as compared to the other OCA designs. After taking all of the above-mentioned facts into account it can be inferred that a PIFA is the best-suited OCA-candidate for indoor 5G-wireless applications. Moreover, due to PIFA's proven edge over other antennas, it is practically being widely used as a mobile-communication antenna. However, such an antenna has not been investigated/ implemented on-chip at 38-GHz, which is one of the potential 5G frequencies. This work presents a top-loaded On-Chip Planar Inverted-F Antenna (PIFA) operable at the millimeterwave frequency of 38-GHz. The proposed antenna shows a reflection co-efficient $|S_{11}|$ value of -14.8 dB and offers an antenna-gain of 0.7 dBi at the center-frequency of 38 GHz. To the best of the authors' knowledge, this thesis reports the ***first On-Chip PIFA*** designed, fabricated and tested at the ***5G millimeterwave frequency of 38-GHz.***

This chapter is organized as follows. Section 5.3 describes the details of the CMOS technology and the design of the proposed on-chip PIFA along with the layout challenges. Measurement

results are reported in Section 5.4 and finally, Section 5.5 concludes the work presented in this chapter.

5.3 On-Chip Planar Inverted-F Antenna Design

The proposed On-Chip Planar Inverted-F Antenna (PIFA) is implemented in TSMC 180-nm CMOS process technology. Fig. 5.1 shows the stacked back-end-of-line (BEOL) metal layers of the technology which offers 6 metallization levels. The top-most metal layer M-6 is utilized to implement the On-Chip Antenna (OCA). There is a passivation layer of silicon nitride which is deposited at the top of the microchip for protection purposes. Silicon substrate is 300 μm thick with permittivity of 11.9 and resistivity of 10 Ω-cm. The region between the metal layer M-6 and the substrate is filled with silicon dioxide having a dielectric constant of 3.9.

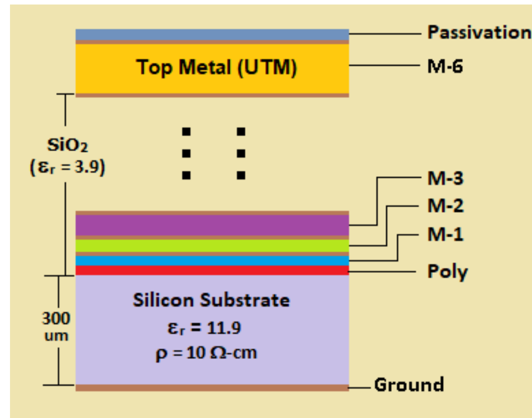


Fig. 5.1. Stacked BEOL metal layers of the standard 180-nm TSMC CMOS process technology.

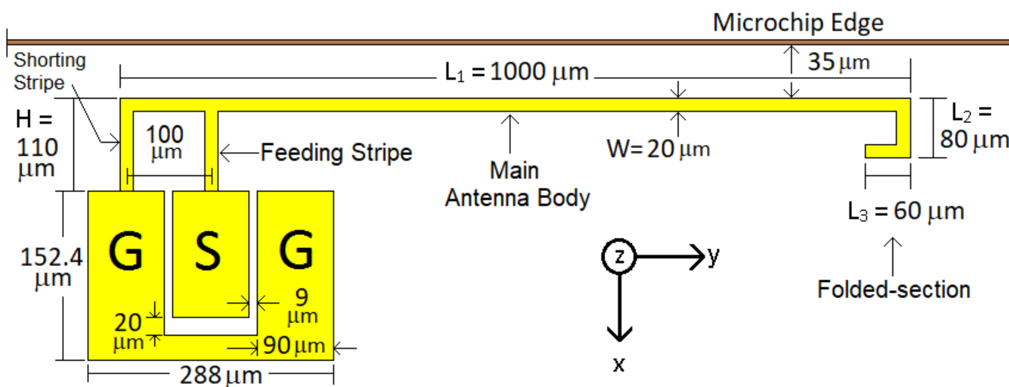


Fig. 5.2. Design and dimensions of the proposed on-chip PIFA.

The proposed On-Chip PIFA design is shown in the Fig. 5.2. The antenna consists of a feeding stripe, a shorting stripe, main antenna body and a folded-stripe section. The antenna structure is positioned very close to the edge of the microchip enabling the OCA to radiate readily into the free-space and hence minimizing the absorption of radiation within the silicon substrate. The placement of the OCA close to the chip's edge improves the gain-performance of the antenna. By varying the effective length (L_1+L_2+L_3+H) of the PIFA the resonant frequency can be tuned. The input impedance of the antenna can be matched to 50 Ω by adjusting the spacing between the feeding and the shorting stripes. The open end of the PIFA is folded to achieve a top-loaded structure. The folded section provides an additional capacitance effect. This capacitance helps to achieve wide bandwidth and improved 50 Ω matching.

As a PIFA is quarter-wavelength antenna therefore, the approximate length of the proposed antenna can be evaluated by the help of the following formula:

$$L \approx \frac{\lambda_g}{4} = \frac{1}{4} \cdot \frac{c}{f\sqrt{\varepsilon_r}} \tag{5.1}$$

$$L \approx 1000\ \mu\text{m}$$

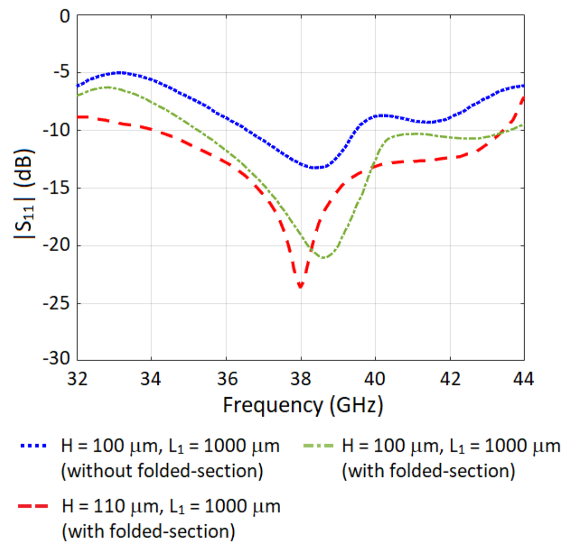


Fig. 5.3 Reflection co-efficient traces showing selection of the optimized dimensions of the proposed OCA.

Where, 'λ_g' is guided wavelength. The dimensions of the PIFA were optimized as shown in the Fig. 5.3. The blue-colored trace in the figure was captured when the height of the antenna was 100

µm and the open-end of the PIFA was not folded. Whereas the green-colored trace was obtained along with the folded-section of the antenna. A clear improvement in terms of reflection co-efficient values and bandwidth can be observed in the green-trace as compared to the blue-trace. However, the green-colored trace was still off-set from the desired resonant frequency of 38-GHz. A slight increase of 10-µm in the height of the PIFA centered the resonance dip (red-colored trace) at exactly 38-GHz along with relatively providing an increase of around 1-GHz in the bandwidth of the antenna.

The antenna is fed with the help of a co-planar waveguide (CPW) incorporating 100 µm pitch Ground-Signal-Ground (GSG) pads as shown in the Fig. 5.2. As co-planar waveguide is part of the overall antenna structure therefore, its effect is involved in the impedance matching characteristics of the antenna. Fig. 5.4 shows the top-view of the optimized on-chip antenna. The On-Chip PIFA is printed by the topmost metal layer M-6 and the ground plane is deployed on metal layer M-1. In 180-nm CMOS process node, the top-most metal layer M-6 comes with a few options with regards to the layer thickness. The first one is the general option providing a thickness of 0.99 µm and the second option is relatively a thicker metal layer with a thickness of 2.34 µm. Whereas the third option offers the thickest layer called as Ultra Thick Metal (UTM) layer with 4.6 µm of thickness. In this work, the 4.6-µm UTM is used to implement the antenna-structure. The 20 µm wide metal width of the OCA-stripes along with the maximum thickness (4.6 µm) contribute to enhancing the gain performance of the antenna. The ground pads of the proposed antenna are connected to the ground plane at metal layer M-1 with the help of vias. The optimized ground plane covers an area of 1645 µm × 897 µm as shown in Fig. 5.4. The ground plane reflects the electromagnetic radiation and thereby improves the antenna-gain.

There is an important practical consideration regarding standard foundry fabrication rules which needs to be taken into account while designing an integrated antenna in standard CMOS processes. Fabrication rules also termed as; “Design Rule Check” (DRC) is imperative to be satisfied for deploying any structure on the silicon substrate for manufacturability. The DRC of utmost concern for the OCA is “Pattern Density”. Pattern density means that all the metal layers of that process technology need to satisfy a specific percentage (20% to 80%) of the metal-fill in the total area of the microchip. However, these small chunks of every metal layer spread all around the microchip will cause disturbance in the electromagnetic radiation from the integrated antenna.

Therefore, in order to avoid the metal-fill interference, an exclusion area (0.439 mm^2) in the layout is designed surrounding the PIFA structure as shown in the Fig. 5.4.

Mostly On-Chip Antennas (OCAs) designed at 60-GHz have deployed Artificial Magnetic Conductors (AMCs) underneath the antenna structure however, AMCs at 38 GHz are practically non-feasible on chip due to the constraint of large exclusion area. At high millimeterwave frequencies (like 60-GHz) the dimensions of the AMC unit-cell are small whereas at relatively low millimeterwave frequencies (like 38-GHz) these dimensions become comparatively large. Therefore, the overall AMC-grid designed at the millimeterwave frequency of 38-GHz will occupy a huge area on microchip and hence, for the purpose of ensuring effective operation, will demand all its occupied region to be excluded from the dummy metal-fill. However, at the fabrication end, the microchip foundries do not allow a large exclusion area due to the high possibility of microfractures in the chip and/or deformation of the microchip structure. In fact, a large exclusion area jeopardizes the mechanical stability of the microchip and hence, is not approved by the foundry.

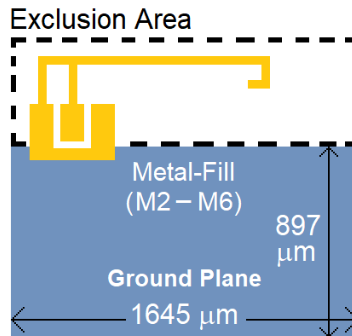


Fig. 5.4. Top-view of the proposed OCA depicting designated exclusion area along with dummy metal-fill region and the ground-plane.

5.4 Antenna Measurement Results

The photomicrograph of the On-Chip Planar Inverted-F Antenna (PIFA) implemented in TSMC 180-nm CMOS process technology is shown in the Fig. 5.5. The area occupied by the antenna on microchip is 1645 μm × 1164 μm. Cascade Micro-tech Summit 11K probe-station and Rohde & Schwarz (ZVA-50) Vector Network Analyzer (VNA) is used to perform the on-wafer measurements. The Cascade Microtech co-planar probes are landed on 100 μm-pitch GSG (Ground-Signal-Ground) pads for the purpose of exciting the antenna. The reflection co-efficient

$|S_{11}|$ of the proposed OCA is shown in the Fig. 5.6. Simulated and measured reflection coefficient values are -23.76 dB and -14.8 dB respectively, at the center-frequency of 38-GHz. The figure shows that the measured reflection co-efficient trace stays below -10 dB for a considerable range of frequencies. It can also be observed from the Fig. 5.6 that the measured resonance dip has shifted to about 2-GHz from the simulated resonance dip. The reason of this shift could be that the introduced signal has perceived the longitudinal dimension of the antenna slightly smaller than the realized stripe.

Fig. 5.5 depicts the test setup for antenna gain and radiation pattern measurements. Antenna Under Test (AUT) senses the radiation from the WR-28 standard gain horn antenna (26.5 – 40 GHz) with a gain of 15 dBi. The aperture dimensions of the horn antenna are 19.03×13.64 mm^2. The rotating shaft is steered at different angles to trace the radiation pattern of the AUT. For radiation-gain calculation through Friis transmission expression, the transmission coefficient $|S_{21}|$ is measured between the horn antenna and the AUT with the help of vector network analyzer. The distance between the AUT and the horn antenna is kept as 40 cm to ensure the far-field criteria, expressed by the following formula:

$$R \geq \frac{2D^2}{\lambda_0} \tag{5.2}$$

Where, D is the largest aperture dimension of the horn antenna and λ_0 is free-space wavelength.

The antenna-gain is calculated by the help of the following formula:

$$[G_{AUT}]_{dB} = [S_{21}]_{dB} - [G_{Horn}]_{dB} + [L_{Probe}]_{dB} + [L_{Adapter}]_{dB} - \left[\left(\frac{\lambda}{4\pi R}\right)^2\right]_{dB} \tag{5.3}$$

where S_{21} is transmission coefficient, G_{Horn} is gain of the horn antenna (15 dBi), L_{Probe} is probe loss (2.0 dB), $L_{Adapter}$ is waveguide to coax adapter loss (0.35 dB), λ is free-space wavelength (7.89 mm) and 'R' is the distance between the horn-antenna and the AUT (40 cm). The above-mentioned calculations are related to 38-GHz of frequency.

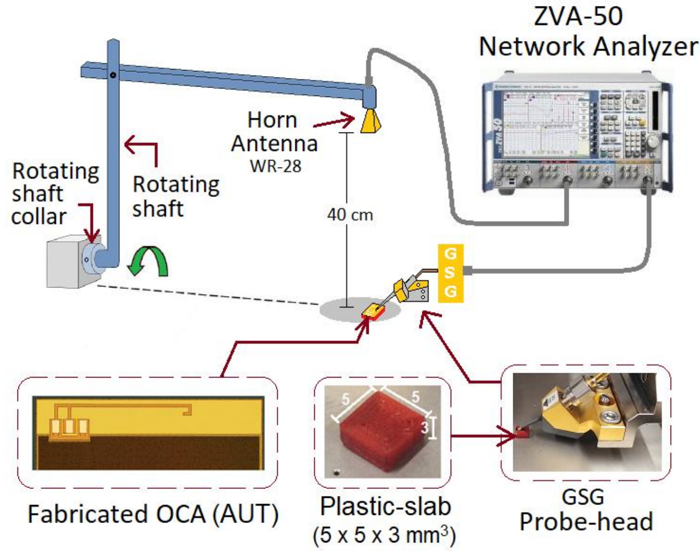


Fig. 5.5. Radiation pattern measurement setup of the Antenna Under Test (AUT) employing Cascade Microtech GSG co-planar probe, WR-28 horn antenna and Rohde & Schwarz ZVA-50 Vector Network Analyzer.

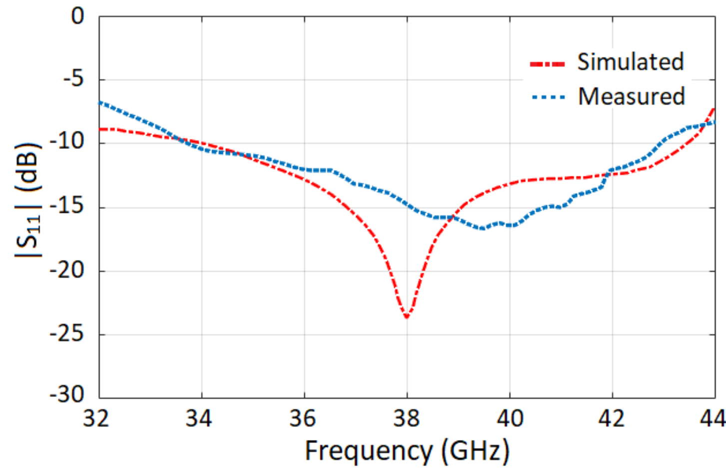
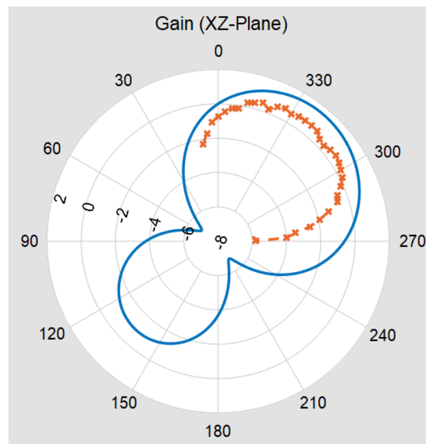


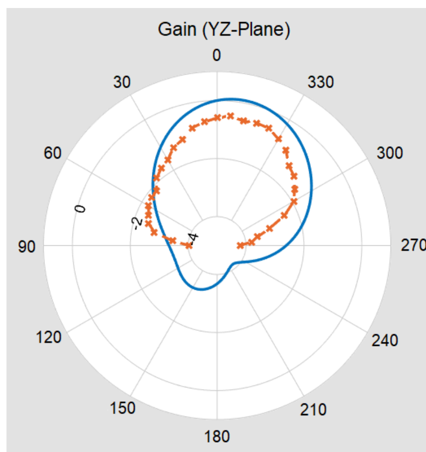
Fig. 5.6. Simulated and measured reflection co-efficient $|S_{11}|$ of the on-chip PIFA.

The measurements are conducted after placing the fabricated on-chip antenna over a miniature plastic-slab ($5 \times 5 \times 3$ mm^3) for the purpose of minimizing the reflections from the metallic chuck of the probe-station. 3-D printed plastic-slab, shown in the Fig. 5.5, is made up of Poly-Lactic-Acid (PLA) material. Fig. 5.7 depicts the simulated and measured radiation patterns of the proposed OCA captured at the center-frequency of 38-GHz. In XZ plane, the simulated radiation pattern shows a peak antenna gain of 1.6 dBi and the measured radiation trace exhibits the peak gain of 0.7 dBi. Whereas in YZ plane, the simulated and measured radiation traces show the peak

gain values of 0.09 dBi and -0.52 dBi respectively. It is important to note here that the proximity of the probe-head to AUT limits the scanning zone of the horn antenna in XZ-plane as shown in the Fig. 5.8. The radiation pattern is scanned up to a safe limit of 10^0 and the reading is not captured beyond this point. However, in YZ-plane the entire angular sector from 90^0 to 270^0 is scanned for acquiring the radiation pattern. The tilt in the antenna beam of radiation (Fig. 5.7(a)) confirms that the positioning of the OCA-structure close to the edge of the microchip facilitates the antenna to radiate readily into free-space and hence minimizes the absorption of radiation within the silicon substrate. The minor discrepancy in the simulated and measured results could be due to the reason that the OCA experienced slightly higher dielectric and conductor losses than expected.



(a)



(b)

Fig.5.7. Simulated (blue) and measured (orange) radiation patterns in XZ-Plane (a) and YZ-Plane (b) at the center-frequency of 38-GHz.

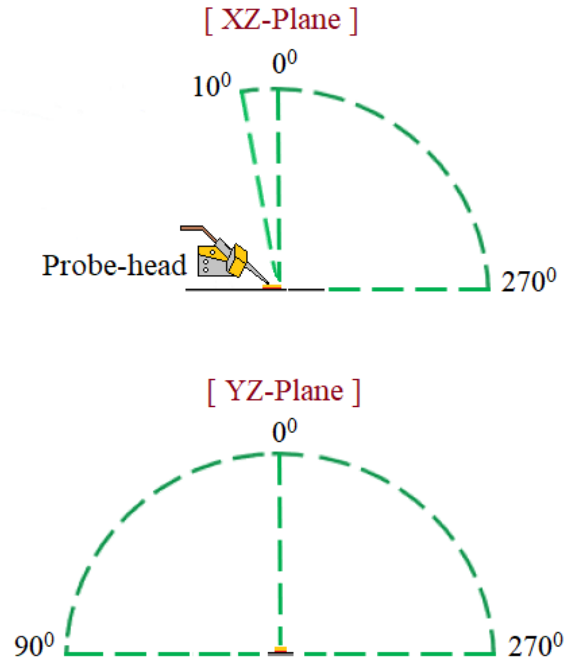


Fig. 5.8 Scannable angular sectors for XZ-Plane and YZ-Plane.

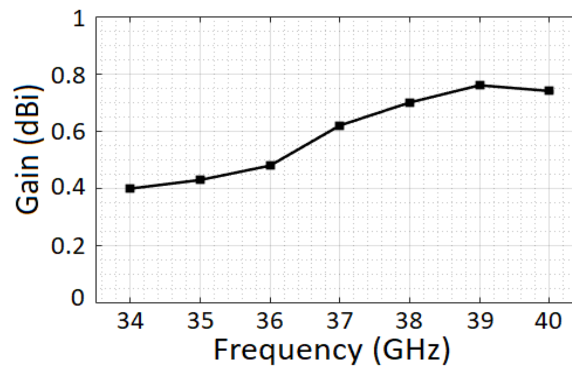


Fig. 5.9 Measured peak gain values of the fabricated OCA at different frequencies.

Fig. 5.9 depicts the measured peak gain of the fabricated OCA at different frequencies in the vicinity of 38 GHz. It can be observed from Fig. 5.9 that the gain values are slightly higher at 39-GHz and 40-GHz as compared to 38-GHz of frequency. This can easily be explained by observing the measured reflection co-efficient trace in Fig. 5.6. The measured S_{11} trace in Fig. 5.6 touches -15 dB at 38-GHz and continues to follow the downward trend up till 40-GHz. Better reflection co-efficient value means there exists less mismatch and more power is being transferred to the OCA. This is the reason that at 39-GHz and 40-GHz the measured gain of the antenna is coming better

than at 38-GHz of frequency. Whereas, for frequencies below 38-GHz, as the measured reflection co-efficient trace shows upward trend (moving from 38-GHz to 32-GHz) in Fig. 5.6 therefore, the corresponding gain values in Fig. 5.9 are lower than that at 38-GHz of frequency.

5.5 Conclusion

The chapter presents a 38-GHz On-Chip Planar Inverted-F Antenna (PIFA) implemented in TSMC 180-nm CMOS process node. The OCA structure is deployed with the help of Ultra-Thick Metal (UTM) layer. For improving the gain-performance, the OCA is positioned close to the edge of the microchip. The open end of the antenna is bent to develop a top-loaded PIFA structure resulting in better 50-Ω impedance matching and wider bandwidth. Measurements are conducted after placing the OCA over a 3D-printed plastic slab to reduce the reflections from the metallic chuck of the probe-station. The proposed antenna showed the return loss of 14.8 dB and a gain of 0.7 dBi at the center-frequency of 38-GHz. The implemented CMOS-PIFA offered a simple geometrical structure, small form-factor and cost-effective antenna-solution. Therefore, it is one of the most suitable on-chip antennas for applications related to 5G cellular communications at 38-GHz band.

References

[1] H. M. Cheema and A. Shamim, "The last barrier: on-chip antennas," IEEE Mirowave Magazine, vol. 14, no. 1, pp.79–91, Jan. 2013.

[2] T. S. Rappaport *et al.*, "Millimeter wave mobile communications for 5G cellular: It will work!," IEEE Access, vol. 1, pp. 335–349, 2013.

[3] Y.P. Zhang, M. Sun and L. H. Guo, "On-chip antennas for 60-GHz radios in silicon technology," *IEEE Transactions on Electronic Devices*, vol. 52, no. 7, pp. 1664 – 1668, Jun. 2005.

[4] P. J. Guo *et al.*, “60-GHz millimeter-wave CMOS RFIC on-chip meander-line planar inverted-F antenna for WPAN applications,” *IEEE Antennas and Propagation Society International Symposium*, pp.1–4, Sep. 2008.

[5] D. Gang, H. M. Yang and Y. Y. Tang, “Wideband 60-GHz on-chip triangular monopole antenna in CMOS,” in *Proc. 3rd Asia-Pacific Conference on Antennas and Propagation*, pp. 623–626, Jul. 2014.

[6] H. Chu *et al.*, “60-GHz broadband CMOS on-chip antenna with an artificial magnetic conductor,” in *IEEE International Microwave workshop Series on Advanced Materials and Processes for RF and THz Application (IMWS-AMP)*, Jul. 2016.

[7] P. Burasa, T. Djerafi and Ke Wu, “A 28 GHz and 60 GHz dual-band on-chip antenna for 5G-compatible IoT-served sensors in standard CMOS process,” *IEEE Transactions on Antennas and Propagation*, vol. 69, no. 5, pp. 2940–2945, May 2021.

[8] P. J. Guo *et al.*, “60-GHz millimeter- wave CMOS RFIC on-chip triangular monopole antenna for WPAN applications,” *IEEE Antennas and Propagation Society International Symposium*, pp.1–4, June 2007.

[9] A. Masrouri and N. Amiri. "Circularly Polarized On-Chip Antenna for 60GHz Indoor Wireless Communications," IEEE *18th Mediterranean Microwave Symposium (MMS)*, pp. 264–267, Nov. 2018.

[10] K. S. Sultan, H. H. Abdullah, E. A. Abdallah, M. A. Basha, and H. H. El-Hennawy, "A 60-GHz gain enhanced vivaldi antenna on-chip," *IEEE International Symposium on Antennas and Propagation & USNC/URSI National Radio Science Meeting*, pp. 1821-1822, Jul. 2018.

[11] M. K. Hedayati *et al.*, “A 38 GHz on-chip antenna in 28-nm CMOS using artificial magnetic conductor for 5G wireless systems,” in *4th International Conference on Millimeter-waves and Terahertz Technologies (MMWaTT)*, pp. 29–32, Dec. 2016.

CHAPTER NO. 6

CONCLUSION

6.1 Summary

This research work aimed to design integrated 5G microwave and millimeterwave power amplifiers, as well as a millimeterwave On-Chip Antenna. Different techniques were employed to design a high-performance millimeterwave switching amplifier. The main technique was "*Transistors-Stacking*", which helped to achieve high output power and also provided the opportunity to incorporate Class-F^{-1} circuitry for considerably improving the power-added efficiency (PAE). The Class-F^{-1} harmonic-network enhanced the PAE by shaping the voltage and current waveforms at the collector terminal of the active device. The amplifier design proposed a novel "*parasitic-aware*" Class-F^{-1} harmonic network that employed a circuit-theoretic approach to open-circuit the second harmonic and short-circuit the third harmonic frequency. The power-gain parameter was attempted to be enhanced by making the amplifier a two-stage design comprised of a driving-stage followed by the final power-stage. Moreover, the interstage-matching network was designed for maximum power-transfer resulting in further enhancement in the power-gain of the amplifier. The entire circuit was designed in 130-nm *SiGe-BiCMOS 8HP technology* which offers higher breakdown voltage and higher values of f_T & f_{max}. The stacking of transistors had not been investigated for integrated Class-F/F^{-1} amplifiers and this work is the first in the literature to report such an investigation. The performance-metric of a power amplifier is called Figure-of-Merit (FoM). The FoM of the proposed amplifier was calculated and it was found that the amplifier achieved the highest value of FoM i.e., 69.68 among previously reported millimeterwave integrated Class-F/F^{-1} PAs. Hence, the research goal of designing a high-performance integrated millimeterwave power amplifier was successfully accomplished.

This research work also proposed a 5G-microwave power-amplifier that was designed to achieve the highest performance in only one of the main parameters i.e., Power-Added-Efficiency (PAE). In order to achieve the goal, a "*Single-Transistor*" design approach with "*parasitic-aware*" Class-F^{-1} harmonic-control topology was employed. Single-transistor design consumes less power

as compared to multi-transistor designs and therefore provides efficiency enhancement. Furthermore, the Class-F^{-1} harmonic-control network connected at the drain terminal of the active device well-shaped the voltage and current waveforms and played its role in achieving the highest possible PAE value. For the purpose of designing a Class-F^{-1} harmonic-network, a new topology derived from a novel iterative algorithm was incorporated in the design. The key advantage of the algorithm as compared to other optimization algorithms was that it started from an educated reference value and quickly converged towards the solution. A dual-purpose output matching network was designed which not only served the purpose of output-impedance-matching but also supplemented the harmonic-control of the Class F^{-1} harmonic-network, thereby further improving the PAE value. The amplifier was fabricated in TSMC 65-nm CMOS process node and it is the first "single-transistor" integrated Class-F^{-1} power amplifier operable at "5G-microwave frequency" of 6 GHz. The amplifier yielded a gain of 13.8 dB and a saturated output-power of 14.4 dBm. The proposed PA offered a peak power-added-efficiency (PAE) of 47.8% which is one of the highest when compared with previously reported integrated microwave/millimeterwave PAs in CMOS and SiGe technologies. Hence, the research goal of designing a high-efficiency integrated microwave power amplifier was successfully attained.

Furthermore, this research work proposed an On-Chip Planar Inverted-F Antenna (PIFA) radiating at 5G millimeterwave frequency of 38-GHz. The antenna is designed in TSMC 180-nm CMOS process node comprising of 6 metallization levels. The OCA was deployed on chip by utilizing the Ultra-Thick Metal (UTM) layer at the M-6 level of the technology whereas the ground plane was deployed with the help of the bottom-most metal layer (M-1). To achieve better radiation performance, the OCA was positioned close to the edge of the microchip. The open-end of the PIFA was folded to obtain a top-loaded structure for improved 50-Ω impedance matching and bandwidth. The reflection coefficient and radiation patterns of the OCA were acquired using a ZVA-50 vector network analyzer, standard gain WR-28 horn antenna, and Cascade Microtech Summit 11K probe station. Measurements were performed after placing the fabricated OCA over a 3D-printed plastic slab to minimize the electromagnetic reflections from the metallic-chuck of the probe-station. The measurement results showed that the fabricated OCA yielded a return loss of 14.8 dB and a peak gain of 0.7-dBi at the center-frequency of 38-GHz. This work presented the first On-Chip Planar Inverted-F Antenna designed at the 5G millimeterwave center-frequency of 38-GHz. The proposed On-Chip Antenna offered desired features like simple geometrical

architecture, small form factor, and cost-effective CMOS design for 5G communication applications.

Recent work related to MMIC (Monolithic Microwave Integrated Circuits) PAs is reported as follows. A continuous-mode wideband Class-F^{-1} power amplifier designed in 130-nm SiGe BiCMOS technology was proposed in [1]. The amplifier yielded an output power of 19 dBm, a gain of 17.8 dB, 26.8% peak PAE and an FoM of 64.7. Another Class-F^{-1} power amplifier fabricated in 130-nm SiGe process node was reported in [2]. The PA used common-emitter topology with a transformer-based harmonic control network. The amplifier delivered an output power of 16.5 dBm, 37.2% PAE, a gain of 20 dB and an FoM of 61.14 at an operating frequency of 28-GHz. A simulation-based Class-F^{-1} differential-series Doherty power amplifier was recently proposed in [3]. Both main and auxiliary amplifiers were tuned using Class-F^{-1} harmonic control networks operable at 28 GHz of center frequency. The PA was employed in 45-nm CMOS process technology. The amplifier was not fabricated. However, simulations results showed that the proposed architecture offered a saturated output power of 25.9 dBm, a gain of 11.1 dB, peak power added efficiency of 38.8% and an FoM of 61.82. Very recently a single-stage quasi-Class-F^{-1} power amplifier implemented in 130-nm SiGe BiCMOS process node is reported in [4]. The amplifier achieves a gain of 14.7 dB, saturated output power of 18.8 dBm, peak PAE of 33% and an FoM of 60.28 at the operating frequency of 38 GHz.

A triple-stacked power amplifier designed in 130 nm SiGe BiCMOS technology was reported in [5]. The amplifier employed reactive tuning between the active devices. The power of the two triple-stacked PAs was combined using Wilkinson power combiners. The PA was not fabricated on-chip and only the layout simulation results were presented. Simulation results showed that the PA offered a saturated output power of 23.4 dBm, a gain of 15.9 dB, 19.2% PAE and an FoM of 62.5 at 33 GHz center frequency. It can be easily inferred from the results presented in [5] that increasing the number of stacked devices in a stacked configuration may provide an increase in output power however, such a structure suffers from PAE deterioration. Therefore, the stacking tower should be increased judiciously. In our proposed millimeterwave PA design, the double-stacked structure is employed as the triple-stacked structure was not beneficial in terms of achieving a higher PAE. Moreover, our output power was already considerably high. Therefore, decision was made to not trade-off our PAE for further increase in output power, which could have

been achieved by implementing a triple-stacked structure. A wideband SiGe BiCMOS power amplifier implemented in 90-nm process node was proposed in [6]. The amplifier employed a triple-stacked HBT structure with emitter degeneration. A gain of 13.2 dB is offered by the PA in the frequency range of 0 to 40 GHz. It is to be noted that the amplifier's output power and PAE was not mentioned and hence its FoM cannot be calculated. Very recently a double-stacked power amplifier fabricated in 90-nm SiGe BiCMOS process technology was reported in [7]. The dual-band amplifier employed a common base (CB) configuration. The PA achieved a saturated output power of 20/18.8 dBm, power gain of 9.5/16 dB, peak PAE of 25/22.5% and FoM of 54.1/64.44 at 36/64 GHz frequency.

TABLE 6.1
BENCHMARKING OF THE DEVELOPED INTEGRATED MILLIMETERWAVE POWER AMPLIFIER WITH RECENTLY REPORTED PAS AND EVALUATION OF FIGURE-OF-MERIT (FOM)

Referenced Work	Technology	Amplifier's Class	Chip's Status	Power Gain, G_p [dB]	Output Power, P_{SAT} [dBm]	PAE (%)	Frequency (GHz)	Figure of Merit [FoM]
This Work	**0.13 µm SiGe**	**Double Stacked Class F^{-1}**	**Fabricated**	**22.1**	**21.2**	**30.1**	**38**	**69.68**
[1]	0.13 µm SiGe	Class F^{-1}	Fabricated	17.8	19	26.8	44	64.7
[2]	0.13 µm SiGe	Class F^{-1}	Fabricated	20	16.5	37.2	28	61.14
[3]	45-nm CMOS	Class F^{-1}	Simulated	11.1	25.9	38.8	28	61.82
[4]	0.13 µm SiGe	Class F^{-1}	Fabricated	14.7	18.8	33	38	60.28
[5]	0.13 µm SiGe	Triple Stacked	Simulated	15.9	23.4	19.2	33	62.5
[6]	90-nm SiGe	Triple Stacked	Fabricated	13.2	-	-	40	-
[7]	90-nm SiGe	Double Stacked	Fabricated	9.5 / 16	20 / 18.8	25 / 22.5	36 / 64	54.1 / 64.44

Table 6.1 summarizes the above-mentioned discussion, and the proposed work has been benchmarked against the most recently published work. It shows the three key performance parameters of the referenced PAs along with their respective Figure of Merit (FoM) values. It can be easily inferred from the Table that the FoM of the power amplifiers reported in recent literature

is less than our proposed amplifier's FoM (69.68). Therefore, the performance of the proposed PA design is superior as compared to the recently published state-of-the-art PA designs. It is to be noted that Table 6.1 is an updated version of a similar benchmarking Table (Table 3.1) presented in Chapter 3. Furthermore, a similar comparative Table had also been presented in Chapter 4 (Table 4.2) for our second PA design i.e., Microwave Power Amplifier.

The 38-GHz of 5G/6G communication frequency has not yet been regulated. In the absence of rules from the regulatory body, the limitations/recommendations regarding the output power, gain and efficiency are unknown. Hence, it becomes difficult to evaluate and benchmark the performance of components like PA at that released frequency. Therefore, researchers have to select a judicious performance evaluation. Literature shows that the researchers have used Figure of Merit (FoM) as a benchmark for evaluating the performance of their PA designs. FoM was initially introduced by ITRS [8]. It is to be noted that the ITRS no longer exists. However, another similar body named IRDS (International Roadmap for Devices and Systems) has taken its place [9] and it is currently carrying the legacy of ITRS.

After conducting the literature review, it was noted that a maximum FoM of around 66 (Table 3.1) was achieved by the PA designers. Therefore, for the design of the proposed millimeterwave power amplifier, the target FoM was higher than this value.

FoM is comprised of three key parameters:

- Gain,
- Output Power,
- PAE.

Therefore, it was decided to focus on all three of these key performance parameters for achieving the targeted FoM (i.e., > 66). The flow chart depicted in Fig. 6.1 shows the proposed schemes/techniques employed to achieve the targeted performance. The value of the gain parameter was increased considerably by employing a two-stage PA design. The first stage is the driving stage, with the second one being the power-stage. A two-stage design obviously yields more gain as compared to a single-stage design. The Power-Added-Efficiency (PAE) value was enhanced by incorporating Class-F/F^{-1} harmonic control networks at the output terminals of the active devices in both the driving and the power stage of the PA. Finally, the output power was

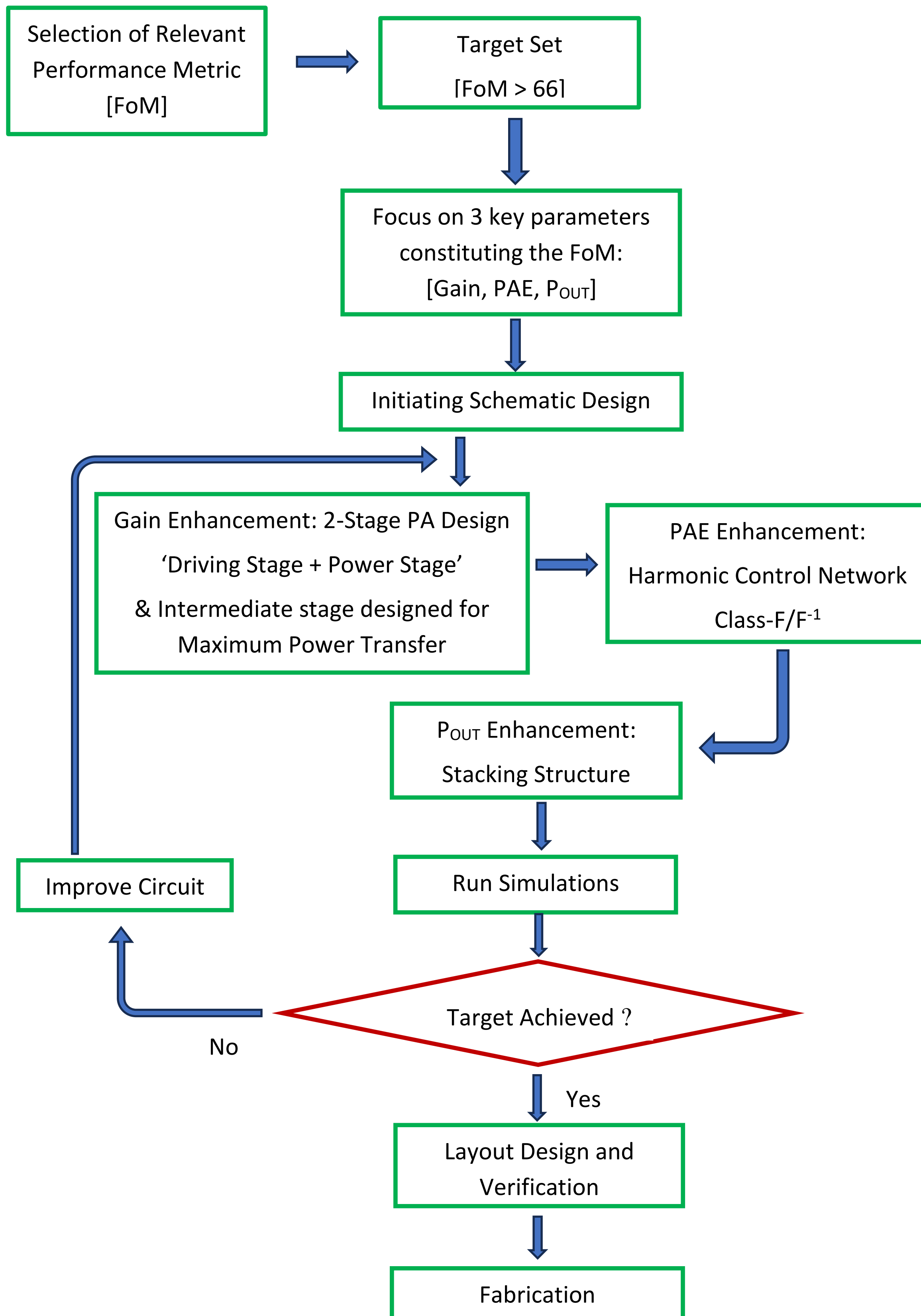

Selection of Relevant Performance Metric [FoM]
Target Set [FoM > 66]
Focus on 3 key parameters constituting the FoM: [Gain, PAE, P_{OUT}]
Initiating Schematic Design
Gain Enhancement: 2-Stage PA Design
‘Driving Stage + Power Stage’
& Intermediate stage designed for Maximum Power Transfer
PAE Enhancement:
Harmonic Control Network
Class-F/F^{-1}
P_{OUT} Enhancement:
Stacking Structure
Run Simulations
Improve Circuit
Target Achieved ?
No
Yes
Layout Design and Verification
Fabrication

Fig. 6.1 Flow Chart depicting the proposed schemes/techniques to achieve the targeted performance of Integrated Millimeterwave Power Amplifier.

improved significantly by employing a 'double-stacked' structure in the PA design. Simulations were then run, and results were observed. Further improvement in the gain and PAE values was achieved by designing the intermediate stage (circuit connecting the driving stage and the power stage) for maximum power transfer and inductive tuning technique respectively. This is an iterative process comprised of running the simulations, checking the results, and making further improvements in the circuit unless the targeted FoM is achieved. After achieving the desired value of FoM (i.e., > 66) the microchip layout was designed, and design verification steps were conducted. As a last step, the final design file (GDSII format) was then sent to the microchip foundry for fabrication. It is to be noted that the above-mentioned proposed schemes/techniques can be used to meet the target design specifications (e.g., improve the FoM) of Millimeterwave Power Amplifiers and therefore is a major contribution of this thesis.

Microwave frequency of 6-GHz is regulated by the Federal Communication Commission (FCC). The FCC emphasized maximizing the battery-life of the client device (mobile, tablets, etc.). The power amplifier in communication hardware is the most dissipative module that consumes power from the system's battery. Therefore, in order to extend the battery life in portable devices, it is imperative to design a power amplifier that provides high power-efficiency. The performance metric for this work is, therefore, Power Added Efficiency (PAE).

After conducting the literature review, it was noted that a maximum PAE of around 35% (Table 4.2) was achieved by the PA-designers. Therefore, the target PAE for the proposed microwave power amplifier needs to be higher than this value. The flow chart depicted in Fig. 6.2 shows the proposed schemes/techniques to achieve the targeted performance. Multiple techniques to enhance the PAE were investigated. It was observed that a "single-transistor" PA-design approach was considerably more power-efficient than a "multi-transistor" approach as it incurs lower power consumption and thereby exhibits superior power efficiency. Another method of PAE improvement was incorporating a harmonic control network at the output terminal of the active device. A class-F^{-1} harmonic control circuit was employed for shaping the current and voltage waveforms at the drain terminal of the active device. Furthermore, a dual-purpose output matching

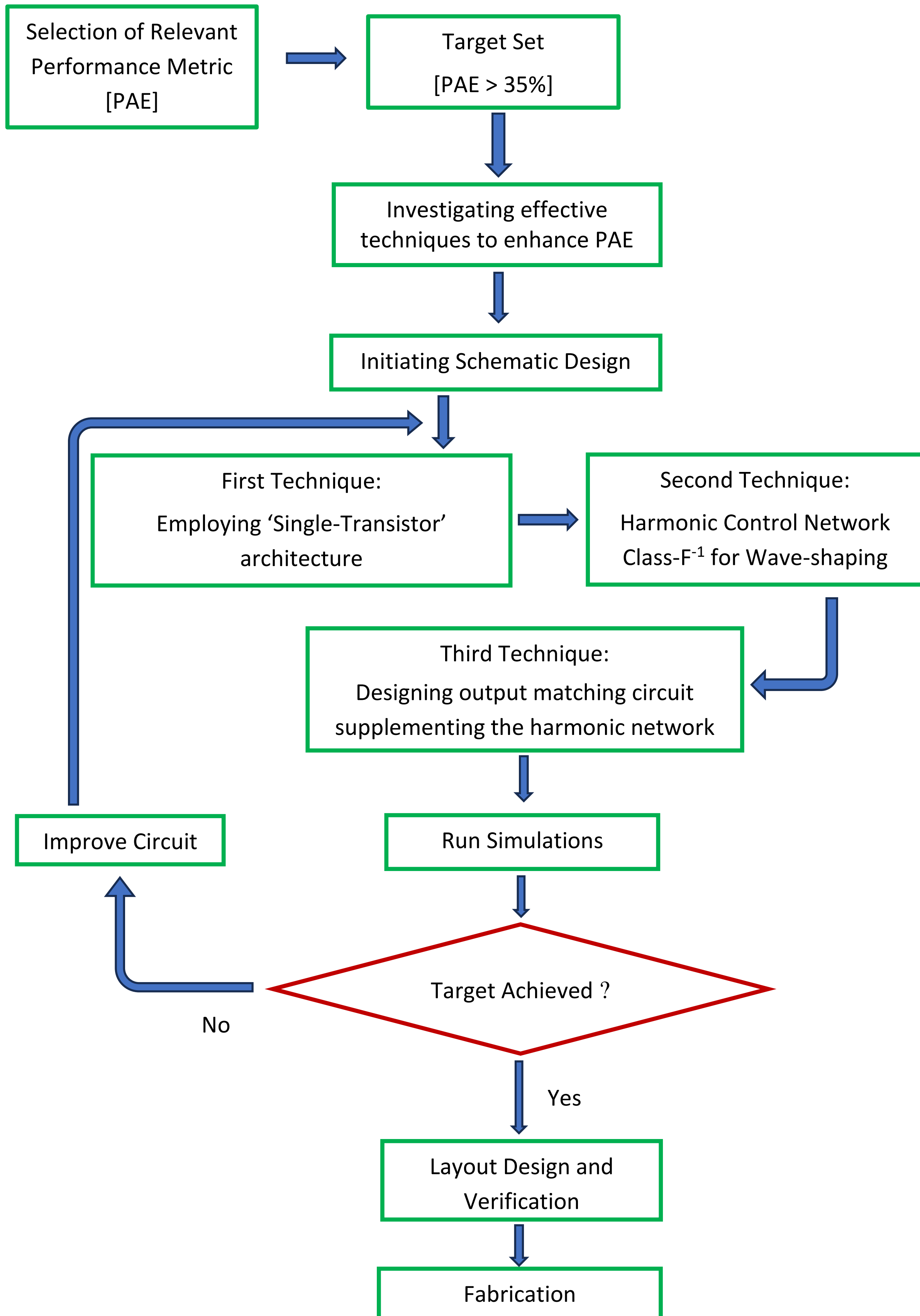

Selection of Relevant Performance Metric [PAE]
Target Set
[PAE > 35%]
Investigating effective techniques to enhance PAE
Initiating Schematic Design
First Technique:
Employing 'Single-Transistor' architecture
Second Technique:
Harmonic Control Network Class-F-1 for Wave-shaping
Third Technique:
Designing output matching circuit supplementing the harmonic network
Improve Circuit
Run Simulations
Target Achieved ?
No
Yes
Layout Design and Verification
Fabrication

Fig. 6.2 Flow Chart depicting the proposed schemes/techniques to achieve the targeted performance of Integrated Microwave Power Amplifier.

network was incorporated in the design, which not only performed the typical task of impedance matching but also reinforced the waveform-shaping capability of the Class-F^{-1} harmonic network resulting in further efficiency enhancement. This entire process is iterative consisting of running the simulations, checking the results, and making any possible improvements in the circuit until the targeted value of PAE is achieved. After achieving the desired value of PAE (i.e., $> 35\%$) the microchip layout was designed followed by design verification steps. As a last step, the final design file (GDSII format) was then sent to the microchip foundry for chip fabrication. It is to be noted that the above-mentioned proposed schemes/techniques can be used to meet the target design specifications (e.g., improve the PAE) of Microwave Power Amplifiers and therefore is a major contribution of this thesis.

A high-level description of the microchip design/fabrication process is outlined to explain the design stages a microchip must undergo before reaching the foundry. It should be noted that a microchip must be designed with a specific fabrication technology e.g., 130-nm SiGe Technology, 65-nm CMOS Technology etc. Therefore, the schematic models must be in the same technology in which the microchip is intended to be fabricated. In order to realize this requirement, the foundries provide foundry-specific component models to microchip designers. All these proprietary models comprising of inductors, transistors, capacitors, etc. are packed by the foundry in a Process Design Kit (PDK). The PDK not only contains the schematic models but also the layout models of the components. The circuit is designed in the schematic window by employing these proprietary components. Simulations are run and results are then observed after each iterative run. After completing the schematic, the layout of the schematic circuitry is designed in the layout window. First of all, the size of the microchip is defined in the layout environment so that the circuit would remain inside the microchip's boundary. Afterwards, the respective layout components are connected appropriately with the help of metal layers of that technology (as depicted in Fig. 4.1 and Fig. 5.1). In the end, Pads are connected at the required ends of the layout circuit. When the layout design of the chip is complete, it is checked for the design rules provided by the foundry. This step is called Design Rule Check (DRC). Once the layout satisfies the DRC

then another check called Layout Versus Schematic (LVS) check is performed. LVS guarantees that the fabricated circuit will functionally match the designed schematic. Layout simulation results can be checked by performing the Post-Layout Simulation. In order to provide the chip-design to the foundry, synthesis steps are required that would produce the GDSII (Graphic Design System) file needed by the foundry for fabricating the microchip.

Several implementation technologies [10] are available for fabricating a microchip design. A comparison of different semiconductor technologies is presented in Table 6.2.

TABLE 6.2
COMPARISON OF SEMICONDUCTOR TECHNOLOGIES FOR 5G & BEYOND COMMUNICATIONS

	Gallium Nitride (GaN)	**Gallium Arsenide (GaAs)**	**Silicon Germanium (SiGe)**	**CMOS**
Affordability	✗	✗	✓	✓
Technology Accessibility	✗	✓	✓	✓
Integration (RF + Digital circuits)	✗	✗	✓	✓
Bulk production	✗	✗	✓	✓

It can be easily observed from Table 6.2 that SiGe and CMOS technologies are the most appropriate choices for implementing 5G & Beyond microwave/millimeterwave hardware. These cost-effective technologies have the potential to integrate digital and RF circuitry on the same chip platform. The resulting product can be produced in bulk quantity for consumer grade products for 5G and beyond communications.

As far as MMIC (Monolithic Microwave Integrated Circuits) Power Amplifiers are considered, there are some products available in the market. However, these products are fabricated in expensive semiconductor technologies i.e., Gallium Arsenide (GaAs) and Gallium Nitride (GaN) process nodes and not in cheaper SiGe BiCMOS and Standard CMOS process technologies. Two of the main IC design companies offering such MMIC PAs are MACOM and Qorvo. Products offered by them are Qorvo's TGA2222 (GaN), TGA2224 (GaN), QPA2640T (GaN), QPA4346D

(GaN) and MACOM's MAAP-015016-DIE (GaAs), XP1080-QU (GaAs), MAAP-011170 (GaAs) etc. Please note that these MMIC PAs are used for specific applications like microwave/ millimeterwave instruments and defense electronics and not used for volume applications like consumer products (e.g., cellphones, Wi-Fi).

The applications of the power amplifier designs proposed in this work are for handheld communication devices like mobile phones, tablets, etc. The designs presented in this thesis not only provide a solution to realize the next era 5G/6G communication but also can be employed in ANY circuitry requiring Class-F^{-1} operation. A novel topology of Class-F^{-1} network has been proposed in millimeterwave power amplifier. This topology is simple and easy to design as it requires only a few components to exhibit an effective Class-F^{-1} behavior. The presented topology not only works at the operating frequency of 38 GHz at which it is designed but also can be employed to design the same Class-F^{-1} network at any frequency of interest, which means the topology offers a generic Class-F^{-1} structure. Moreover, the proposed iterative method depicted in Fig. 6.1 (Flow Chart) is a generalized method focused on achieving a higher FoM value. PA designers can use these proposed generic techniques to improve the circuit topology and FoM of their amplifier. *The novel Class-F^{-1} topology and the iterative design method are major generalized contributions of this research work conducted on Millimeterwave Power Amplifier.*

Similarly, the microwave power amplifier proposed in this work is comprised of a novel Class-F^{-1} network deduced using a novel iterative algorithm. Both the proposed topology and the algorithm can be employed to design a Class-F^{-1} network at ANY desired frequency and hence present a generic design for employing a Class-F^{-1} harmonic control network. Moreover, the design presents two equations (4.21 and 4.22) that can convert any inductor into a $2f_0$ tank circuit. This simple technique is very effective. It not only provides output impedance matching but also prevents the second harmonic from reaching the load. This technique is also generic and can be employed in ANY circuitry that requires an inductor to transform into a tank circuit and satisfy harmonic matching requirements. Moreover, the proposed iterative method depicted in Fig. 6.2 (Flow Chart) is a generalized method focused on achieving a higher PAE value. PA designers can use these proposed generic techniques to improve the circuit topology and PAE of their amplifier. *The novel Class-F^{-1} network deduced using a novel iterative algorithm, and the iterative design*

method are major generalized contributions of this research work conducted on Microwave Power Amplifier.

6.2 Future Directions

Future research can be conducted to design a dual 5G-band power amplifier and On-Chip Antenna. As an example, a power amplifier capable of operating at dual 5G-bands like 28-GHz and 38-GHz, or 38-GHz and 60-GHz can be investigated. Similarly, an OCA can also be investigated which could be excited at more than one 5G frequency.

In contrast to individual dual-band designs of PA or OCA, a co-design of a power amplifier and On-Chip Antenna operable at dual 5G millimeterwave frequencies can also be investigated. A double or triple-stacked structure along with Class-F/F^{-1} harmonic control network can be introduced in the power-amplifier design so that it could feed its output-power to the OCA. One interesting aspect of such a co-design would be that it will no longer require the output-impedance of the power amplifier to be terminated to 50-ohms load. This is because the output-impedance of the amplifier could be directly matched to the input impedance of the OCA. Consequently, a well-integrated RF system can be realized on-chip. Such a co-design based dual band system will be beneficial as it can offer more degrees of freedom or flexibility. For example, if there is a circuit operable at both 38-GHz and 60-GHz, the communication system can use 60-GHz frequency for indoor communication while switching to 38-GHz for outdoor communication.

Another attractive direction can be reconfigurable power-amplifiers and reconfigurable On-Chip-Antennas. Reconfigurability in terms of the selection of values/levels of a parameter like output-power (for OCA: antenna-gain etc.) or choosing a frequency of interest among multi-frequencies etc. can be investigated. A reconfigurable system will be able to operate at different power, frequency or efficiency levels that are best suited to the conditions of the surroundings. For example, different power levels (or antenna-gain values) can allow the handheld terminal to establish device to device, device to access point or device to base-station communications.

References

[1] D. Wang, W. Chen, X. Liu, X. Li, F. M. Ghannouchi and Z. Feng, "A 24–44 GHz Broadband Transmit–Receive Front End in 0.13-μm SiGe BiCMOS for Multistandard 5G Applications," in *IEEE Transactions on Microwave Theory and Techniques*, vol. 69, no. 7, pp. 3463-3474, July 2021.

[2] Z. Wang et al., "A Linearity-enhanced 28-GHz Class-F^{-1} SiGe Power Amplifier," *2022 IEEE MTT-S International Wireless Symposium (IWS)*, Harbin, China, 2022, pp. 1-3.

[3] M. Osama, H. F. Ragai and M. El-Nozahi, "A 28GHz High Efficiency Inverse Class-F Series Doherty Power Amplifier," *2023 11th International Conference on Internet of Everything, Microwave Engineering, Communication and Networks (IEMECON)*, Jaipur, India, 2023, pp. 1-6.

[4] V. Manouras and I. Papananos, "A Ka-Band SiGe BiCMOS Quasi-F^{-1} Power Amplifier Using a Parasitic Capacitance Cancellation Technique," *Journal of Low Power Electronics and Applications*, vol. 13, no. 2, p. 23, Mar. 2023.

[5] C. Zhang, Z. Li, G. Cheng, H. Wang and Z. Li, "A 26.5-40 GHz Stacked Power Amplifier in 130 nm SiGe BiCMOS Technology," *2018 IEEE International Conference on Integrated Circuits, Technologies and Applications (ICTA)*, Beijing, China, 2018, pp. 36-37.

[6] N. L. K. Nguyen et al., "A Wideband SiGe Power Amplifier Using Modified Triple Stacked-HBT Cell," in *IEEE Microwave and Wireless Components Letters*, vol. 31, no. 1, pp. 52-55, Jan. 2021.

[7] Z. Liu, E. A. Karahan and K. Sengupta, "A Compact SiGe Stacked Common-Base Dual-Band PA With 20/18.8 dBm Psat at 36/64 GHz Supporting Concurrent Modulation," in *IEEE Microwave and Wireless Components Letters*, vol. 32, no. 6, pp. 720-723, June 2022.

[8] International Technology Roadmap for Semiconductors (ITRS), http://www.itrs2.net/ (accessed on Sep. 21, 2023).

[9] International Roadmap for Devices and Systems (IRDS), https://irds.ieee.org/ (accessed on Sep. 21, 2023).

[10] P. M. Asbeck, N. Rostomyan, M. Özen, B. Rabet and J. A. Jayamon, "Power Amplifiers for mm-Wave 5G Applications: Technology Comparisons and CMOS-SOI Demonstration Circuits," in *IEEE Transactions on Microwave Theory and Techniques,* vol. 67, no. 7, pp. 3099-3109, July 2019.

APPENDIX A

The derivation of (4.5) at the 2nd harmonic ($2f_0$) is as follows:

$$Z = R \pm jX \tag{A-1}$$

As Z_{L2} is in parallel with Z_{C2},

$$Z_{Leq} = Z_{L2} || Z_{C2} \tag{A-2}$$

Hence, the equivalent impedance Z_{Leq} is given by,

$$\frac{1}{Z_{Leq}} = \frac{1}{Z_{L2}} + \frac{1}{Z_{C2}} \tag{A-3}$$

Or, $$Z_{Leq} = \frac{Z_{L2}Z_{C2}}{Z_{L2} + Z_{C2}} \tag{A-4}$$

Or, $$Z_{Leq}(Z_{L2} + Z_{C2}) = Z_{L2}Z_{C2} \tag{A-5}$$

Or, $$Z_{Leq}Z_{L2} - Z_{L2}Z_{C2} = -Z_{Leq}Z_{C2} \tag{A-6}$$

Or, $$Z_{L2}Z_{C2} - Z_{Leq}Z_{L2} = Z_{Leq}Z_{C2} \tag{A-7}$$

Or, $$Z_{L2}(Z_{C2} - Z_{Leq}) = Z_{Leq}Z_{C2} \tag{A-8}$$

Or, $$Z_{L2} = \frac{Z_{Leq}Z_{C2}}{Z_{C2} - Z_{Leq}} \tag{A-9}$$

Now, as,

$$Z = R \pm jX, \text{ and, } \because R = 0 \tag{A-10}$$

$$Z = \pm jX \tag{A-11}$$

Hence,

$$Z_{Leq} = +jX_{Leq} \quad \text{(A-12)}$$

And, $$Z_{C2} = -jX_{C2} \quad \text{(A-13)}$$

After inserting Z_{Leq} and Z_{C2} in (A-9),

$$Z_{L2} = \frac{(+jX_{Leq})(-jX_{C2})}{(-jX_{C2} - jX_{Leq})} \quad \text{(A-14)}$$

Or, $$Z_{L2} = \frac{(+jX_{Leq})(-jX_{C2})}{(-j)(X_{C2} + X_{Leq})} \quad \text{(A-15)}$$

Or, $$Z_{L2} = +j\left[\frac{X_{Leq}\ X_{C2}}{X_{C2} + X_{Leq}}\right] \quad \text{(A-16)}$$

With $$Z_{L2} = +jX_{L2} \quad \text{(A-17)}$$

$$+jX_{L2} = +j\left[\frac{X_{Leq}\ X_{C2}}{X_{C2} + X_{Leq}}\right] \quad \text{(A-18)}$$

And, finally, $$X_{L2} = \frac{X_{Leq}\ X_{C2}}{X_{C2} + X_{Leq}} \quad \text{(A-19)}$$

Similarly, the derivation of (4.10) at the 3rd harmonic (@$3f_0$) is as follows:

$$Z_{Ceq} = \frac{Z_{L2}Z_{C2}}{Z_{L2} + Z_{C2}} \quad \text{(A-20)}$$

Or, $$-jX_{Ceq} = \frac{(jX_{L2})(-jX_{C2})}{(jX_{L2}) + (-jX_{C2})} \quad \text{(A-21)}$$

Or, $$X_{Ceq} = \frac{X_{L2}X_{C2}}{X_{L2} - X_{C2}} \quad \text{(A-22)}$$

And, finally, the derivation of (4.16) at the fundamental (@f_0) is as follows:

$$Z_{Leq} = \frac{Z_{L2} Z_{C2}}{Z_{L2} + Z_{C2}} \tag{A-23}$$

Or,

$$jX_{Leq} = \frac{(jX_{L2})(-jX_{C2})}{(jX_{L2}) + (-jX_{C2})} \tag{A-24}$$

Or,

$$X_{Leq} = \frac{X_{L2} X_{C2}}{X_{C2} - X_{L2}} \tag{A-25}$$

APPENDIX B

The following is a derivation of (4.21) and (4.22),

X_{LM} the reactance of L_M,

X_{CR1} the reactance of C_{R1}, and,

X_{LR1} the reactance of L_{R1}.

As X_{CR1} and X_{LR1} are in parallel, X_{LM} is given by:

$$\frac{1}{X_{LM}} = \frac{1}{X_{LR1}} + \frac{1}{X_{CR1}} \tag{B-1}$$

With,

$$X_{LR1} = j\omega L_{R1} \tag{B-2}$$

And,

$$X_{CR1} = \frac{1}{j\omega C_{R1}} \tag{B-3}$$

Applying (B-2) and (B-3) in (B-1),

$$\frac{1}{X_{LM}} = \frac{1}{j\omega L_{R1}} + j\omega C_{R1} \tag{B-4}$$

Or,

$$\frac{1}{X_{LM}} = \frac{1 + j^2\omega^2 L_{R1} C_{R1}}{j\omega L_{R1}} \tag{B-5}$$

Or,

$$\frac{1}{X_{LM}} = \frac{1 - \omega^2 L_{R1} C_{R1}}{j\omega L_{R1}} \tag{B-6}$$

Next, evaluating for fundamental frequency (ω_0) in (B-6),

$$\frac{1}{j\omega_0 L_M} = \frac{1 - \omega_0^2 L_{R1} C_{R1}}{j\omega_0 L_{R1}} \tag{B-7}$$

Or, $$L_M = \frac{L_{R1}}{1-\omega_0^2 L_{R1} C_{R1}} \tag{B-8}$$

The reactance X_{LM} is required to be infinite at 2nd harmonic in order to create an open-circuit at 2nd harmonic, and hence, setting $\omega = 2\omega_0$ and $X_{LM} = \infty$ in (B-6),

$$0 = 1-(2\omega_0)^2\ L_{R1} C_{R1} \tag{B-9}$$

Which deduces to,

$$C_{R1} = \frac{1}{4\omega_0^2 L_{R1}} \tag{B-10}$$

Applying (B-10) in (B-8),

$$L_M = \frac{L_{R1}}{1-\omega_0^2 L_{R1}\left(\frac{1}{4\omega_0^2 L_{R1}}\right)} \tag{B-11}$$

Or, $$L_M = \frac{L_{R1}}{1-\frac{1}{4}} \tag{B-12}$$

And finally, $$L_{R1} = \frac{3}{4} L_M \tag{B-13}$$

APPENDIX C

The Appendix C includes three DRC-16 forms (Statement of Contribution) attached below.

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