VLSI Design, Fabrication and Testing of an Ultra-Wideband Low Noise Amplifier Microchip using Nanometric CMOS Technology

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ABSTRACT

The wide operating bandwidth of the ultra-wideband (UWB) signal leads to new circuit design challenges and methodologies. Similar to any other RF system, the most critical component of the UWB receiver is the low noise amplifier (LNA). Contrary to the narrow-band LNAs, the single-tone assumption is not valid for defining the SNR of an UWB LNA where the input signal encompasses several GHz. Defining the UWB LNA system's SNR as the matched filter bound (MFB) is an appropriate approach to deduce its noise figure (NF). Using this approach, a mathematical model is proposed to achieve optimal NF, employing the g_m-boosted common gate (CG) LNA topology along with a passive noise matching input network. Besides the low noise performance, the other challenges in the design of the UWB LNA include adequate input match and forward power gain with low power dissipation. Considering the superior performance of the g_m-boosted CG amplifier topology for UWB, a new single-ended (SE) g_m-boosted CG UWB LNA architecture is proposed in this research. In the SE LNA architecture, the power dissipation is further minimized by sharing the bias current between the g_m-boosted CG and the active g_m-boosting amplifier stages in a current-reuse fashion ("*piggyback*" g_m-boosting). The proposed *piggyback* g_m-boosted CG LNA, operating in 3-5 GHz range, is fabricated using 130nm RFCMOS process with adequate results. The noise optimization mathematical model proposed in this thesis is applied to the new *piggyback* g_m-boosted CG LNA architecture by including an intervening noise matching passive network at the input of the LNA. The bandwidth of the noise matched *piggyback* g_m-boosted CG LNA is extended using series peaking technique to the complete UWB band from 3.1 to 10.6 GHz. The proposed full-band noise matched UWB LNA is fabricated in a differential manner using 130nm RFCMOS process and exhibited excellent performance improvements with figure of merit (FOM) of 2.86.

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I am indebted to my parents for their love for me and continuous prayers for my success. My success belongs to them as much as it belongs to me. Many thanks to my lovely wife Ayesha and delightful daughters Asma and Hafsa for their tremendous patience, understanding and support.

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CHAPTER 1

INTRODUCTION

1.1 Motivation

The demand for high performance, small size and low power wireless communication systems has increased immensely in the last decade. The urge to remain connected to share the information network and the multi-media is growing as the advancements in the wirele2ss technologies are made. Ultra-wideband (UWB) radio is a rapidly emerging wireless technology to provide a more reliable, faster and low-power short-range access to the data communication equipment. The short range radio technology is playing a key role in the modern information age to provide robust wireless access in the indoor home and office environments. The increased demand of wireless video transfer and positioning applications is observed at personal and industrial levels. Keeping in view these needs, UWB radios are highly anticipated to take over the personal area networks (PANs). It can be predicted that UWB technology will have a great impact on the home networking and the entertainment market relying on high-speed short-range wireless links.

By definition, an UWB radio signal is meant to have a fractional bandwidth larger than 20% (or 0.2) [1]. The fractional bandwidth is defined as the ratio of -10dB transmission bandwidth and the center frequency of the transmitted signal. The Federal Communications Commission (FCC), in 2002, authorized the unlicensed use of specific frequency bands and defined the spectral mask for the UWB communication equipment [1]-[5]. The frequency bands allocated for UWB communication are below 960 MHz and 3.1-10.6 GHz depending on the type of wireless application. Fig. 1.1 shows the FCC spectral mask for indoor UWB erective isotropic radiated power (EIRP) emission level.

The importance of UWB radios can be highlighted using the Shannon's channel capacity theorem [6]-[8]. Expanding bandwidth (if possible and feasible) is the preferred cost-effective technique to achieve higher data rates without the need of increasing the transmit power or resorting to the sophisticated error control coding and higher order modulation schemes. The Shannon's channel capacity theorem is given by [8],

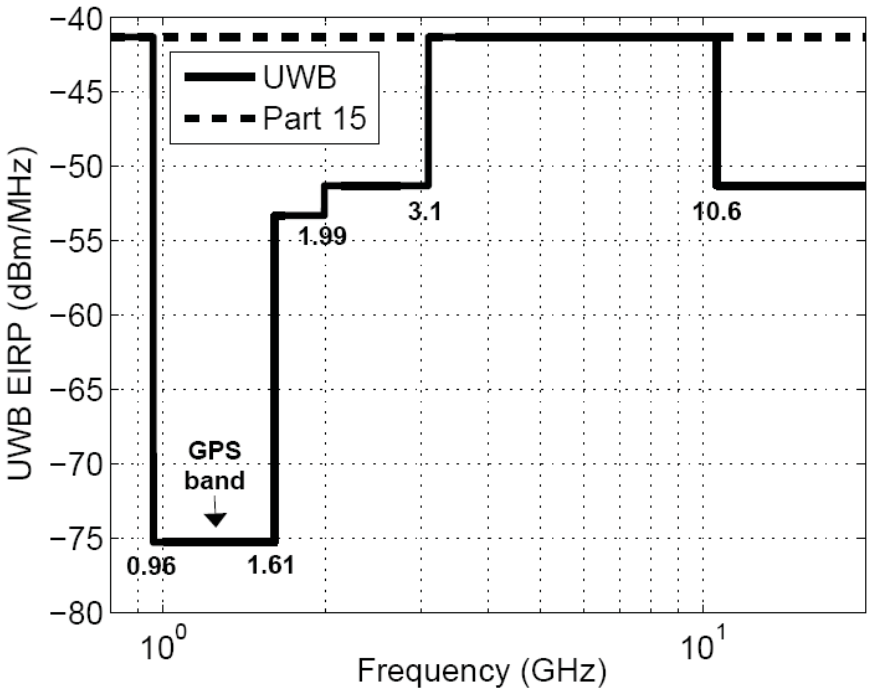

Fig-1.1. FCC spectral mask for indoor UWB communications [1].

$$C = B \log(1+SNR) \qquad (1\text{-}1)$$

Where, '*C*' is the channel capacity to transmit the data, *B* is the bandwidth of the signal being transmitted. It can be observed from (1-1) that for a particular signal-to-noise ratio (SNR), more bandwidth will be required to transmit the data at higher speed. Therefore, when bandwidth is large, very small radiation power is needed to achieve higher data rate.

Owing to the fact that the UWB signal emissions are kept very low power, these signals degrade rapidly with increased distance as compared to the narrow band signals [22]. Hence, UWB systems can co-exist with each other and with other already existing narrow band systems. The potential applications of the UWB technology are wireless PANs, wireless sensory and measurement networks, vehicular radar systems, and imaging and positioning systems [1]-[4], [21], [22].

Due to its high data rate, low transmit power and unlicensed operation, UWB technologies have attracted immense interest by the academia and the industry. With the advancements made in the solid-state integrated circuits in the recent past, implementing the wide bandwidth radio circuits is more realizable and achievable than it was ever before. UWB devices are being feverishly designed and developed by the researchers within the

technical community [8]-[17]. In 2005, WiMedia Alliance proposed the UWB communication standard that divides the 3.1-10.6 GHz frequency range into five Band-Groups (BGs). Each BG is further divided into three sub-bands of 528MHz with the exception of BG-5 which is divided into two sub-bands, as shown in Fig. 1.2 [17], [18].

Although UWB technology has many advantages over the traditional narrowband systems, its success in the future depends heavily on the ability to provide high performance UWB radio frontends at low cost with low power consumption. It thus imposes various design challenges from the theory to its implementation that have never been researched before in the narrowband systems' era. The technical challenges include:

- ✓ the development of efficient and effective modulation and coding techniques for UWB,
- ✓ UWB multiple-input multiple-output (MIMO) systems,
- ✓ robustness to interference and noise at UWB receiver,
- ✓ design of high speed circuits with low power consumption (wideband low noise amplifiers, power amplifiers, and analog-to-digital converters),
- ✓ UWB antenna design, etc.

Due to the advancements made in CMOS RF technologies in the last decade, science community has been showing enormous interest in utilizing CMOS circuits to realize UWB systems. The design of RF CMOS UWB frontend is still posing a great challenge. The transmit power for UWB systems, authorized by FCC, is very low and the power consumption of UWB frontend is not dominated by the radiation power. Optimization of the UWB RF frontend can only be achieved by carefully crafting and optimizing every sub-circuit of the UWB frontend. Design of UWB antenna is also a challenge as the modeling of antenna as a 50Ω resistor is not valid for a very wide bandwidth.

Similar to the narrow band receiver, UWB receiver also requires a band selection and pre-amplification stage comprising of a band-pass low noise amplifier (LNA). The UWB LNA should provide flat gain, low noise performance with wideband input match to the UWB antenna. Low power dissipation, linearity and stability are the noted issues in the RF CMOS UWB LNA design [19], [20]. To deal with these challenges in realizing UWB LNA, new circuit configurations and topologies are needed [21].

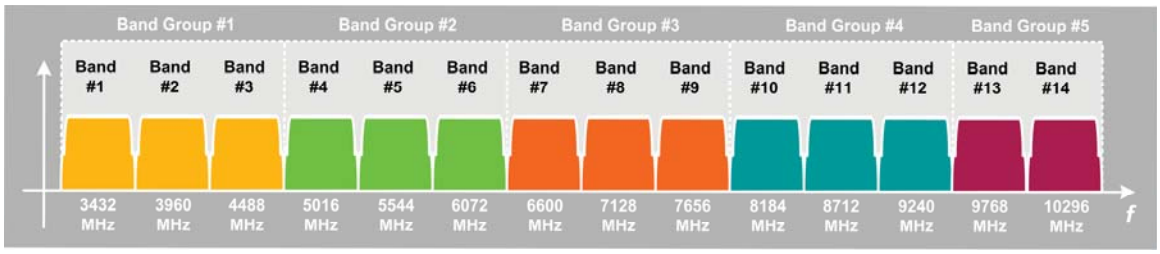

Fig. 1.2. WiMedia frequency plan [18], [43].

1.2 Research Goal

The goal of this research is to investigate the design trade-offs and propose a novel circuit design technique to realize the optimum RF CMOS LNA for UWB frontend. The research thus follows the steps as:

1. Investigate traditional CMOS UWB LNA architectures and devise an appropriate circuit topology suitable for the corresponding frequency band of interest.
2. Find a methodology to optimize and enhance the performance of the UWB LNA in the frequency band of operation.
3. Design and fabricate the circuits using the advanced nanometric CMOS technology to test and verify the circuit design.

1.3 Thesis Organization

This thesis provides insight into the developing CMOS ultra-wideband LNA technology and the contribution of the author in this field of research.

Chapter 2 provides an overview of the basic UWB CMOS LNA architecture and draws a comparison among different competing topologies for the UWB LNA circuit design. The same chapter very briefly presents the work done by different researchers in this field. In Chapter 3 of this thesis, the g_m-boosted common gate (CG) LNA architecture is discussed in detail with the help of the short-channel MOS device model. Mathematical derivations related to the power gain and noise performance of the short-channel g_m-boosted CG LNA architecture are performed in this chapter. The same chapter further demonstrates a new noise model and proposes a novel technique to design the g_m-boosted

CG UWB LNA for optimal noise performance with the help of an example circuit. In Chapter 4, a new circuit topology is proposed which enables the circuit designer to minimize the power dissipation of the g_m-boosted CG UWB LNA using an active g_m-boosting amplifier. In the proposed design, the DC bias current is *reused* or shared between the active g_m-boosting amplifier and the g_m-boosted CG amplifier stages ("*piggyback*" g_m-boosting) to reduce the power consumption overheard. The design and fabrication of the proposed g_m-boosted CG LNA, and the measurement results under the power-matched condition are presented in this chapter. The power-matched g_m-boosted CG LNA operates in 3 to 5 GHz frequency range. In the light of the noise optimization technique presented in Chapter 3 and using the improved version of the circuit topology proposed in Chapter 4, the design and fabrication of a full-band g_m-boosted CG UWB LNA is investigated in Chapter 5. The full-band UWB LNA operates in 3.1 to 10.6 GHz UWB range and is designed to achieve optimal low noise performance (noise-match) by combining the approaches proposed in Chapters 3 and 4. In the same chapter, the measurement results are presented. The next chapter draws comparisons among the power-matched and the noise-matched g_m-boosted CG UWB LNAs and the published state-of-the-art works. Chapter 7 concludes the thesis with the summary of the contributions made by the author in the research. Future work suggestions are also included in the end of the last chapter.

CHAPTER 2

LOW NOISE AMPLIFIER ARCHITECTURES FOR UWB

2.1 Introduction

The advancements made in the down-scaling of the CMOS transistor size have been a great driving force for the academic and industrial communities to investigate new and efficient ultra-wideband (UWB) RF CMOS circuits. The FCC has opened up the unlicensed frequency band from 3.1 to 10.6 GHz for low power and multi-megabit per second RF UWB communication. Since then, different comparative UWB RF frontend designs and the UWB circuits have been proposed in the published research. The low noise amplifier (LNA) is an imperative part of the UWB RF frontend and is required to amplify all in-band signals received at the UWB antenna. Low noise performance, good gain flatness with sharp out-of-band roll-off, adequate power gain, input matched to the antenna, sufficient linearity and low power dissipation are the well-known issues in the UWB LNA design.

2.2 UWB LNA Architectures

The LNA is the pre-amplification stage of an UWB RF frontend. It must provide input-matching as close to 50Ω as possible over the entire UWB spectrum with increasing the noise content of the UWB signal within bounds. LNA must possess sharp out-of-band roll-off at upper and lower -3dB cutoff frequencies to suppress the nearby interferer signals like GSM, Bluetooth, 802.11b and Zigbee etc. High enough linearity, good reverse isolation for stable operation and low power dissipation are the important figures of merit for an UWB LNA. Keeping these characteristics in view, the UWB LNA architectures can be divided into two broad categories, namely the common source (CS) LNA and the common gate (CG) LNA [20]. These architectures are described in detail in this chapter and their general circuit topologies are shown in Fig. 2.1.

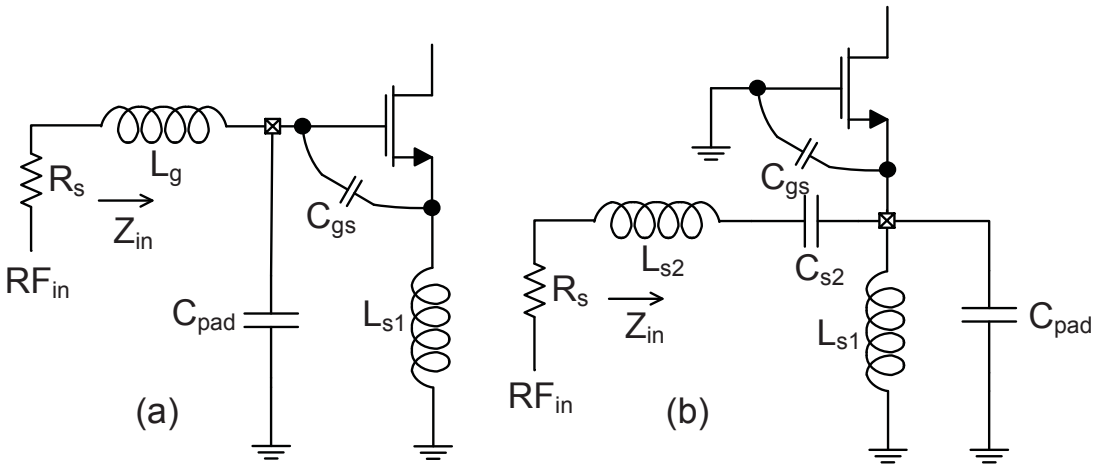

Fig. 2.1. UWB LNA architectures, (a) common source LNA and (b) common gate LNA.

2.2.1 Common Source UWB LNA

The circuit topology shown in Fig. 2.1(a) is commonly known as inductive-degenerated CS LNA. In literature, several works have been published by the researchers to optimize the inductive-degenerated CS LNA topology for narrow-band applications [19]. The same techniques to design CS LNA for narrow-band RF frontend have been adopted by the circuit designers and are extended to realize UWB LNAs. In [23], an improved LNA design technique, possessing 3-5 GHz bandwidth, is presented to yield simultaneous noise and power-match using the inductive degenerated CS topology. Looking at the RLC network shown at the input of the CS LNA in Fig. 2.1(a), ignoring the parasitic pad capacitance C_{pad}, the input impedance $Z_{in}(\omega)$ faced by the source resistance R_s(antenna) is given by [24],

$$Z_{in}(\omega) = j\omega(L_g + L_{s1}) + \frac{1}{j\omega C_{gs}} + \omega_T L_{s1} \tag{2-1}$$

Where, L_g and L_{s1} are the gate terminal and the source terminal inductances respectively and C_{gs} denotes the gate-to-source capacitance of the CS stage. ω_T is the unity gain frequency and loosely defined as the ratio of the transconductance (g_m) of the CS stage and the gate-to-source capacitance C_{gs}. In (2-1), it is clear that $\omega_T L_s$ is purely resistive at resonance and can be matched to R_s=50Ω for adequate power-match. In the presence of a

wideband signal, the CS transistor's DC operating point and the size of L_g and L_s can be chosen to resonate at the center frequency of the operating frequency spectrum to provide wideband input-match.

The Q factor of the input matching network of the inductive-degenerated CS LNA is given by [27],

$$Q_{match_{CS}} = \frac{1}{2\omega C_{gs} R_s} \tag{2-2}$$

From the above equation, it is apparent that $Q_{match_{CS}}$ is inversely proportional to C_{gs}. The CMOS technology has shrunk to nanometer scale resulting in smaller C_{gs} values. This causes $Q_{match_{CS}}$ to increase and the effective bandwidth of the matching network to decrease. Although the matching network in this topology is ideally noiseless and increases the over-all gain of the amplifier, its higher $Q_{match_{CS}}$ makes it unsuitable for UWB circuits.

The noise figure (NF) of the CS LNA has a linear relationship with the operating frequency, and can increase considerably at higher frequencies. The CS LNA also suffers from the parasitic pad capacitance C_{pad} which affects the gain and the matching characteristics of the UWB LNA. The gate-to-drain capacitance C_{gd} of the CS stage reduces the reverse isolation and causes stability issues. Therefore, advance circuit design techniques are required to design the UWB LNA using the CS amplifier configuration [25]-[28].

In literature, many UWB LNA circuits have been reported using the CS transistor as the input stage. To increase the bandwidth of the LNA for wideband operation, active or passive feedback techniques are commonly employed [22], [29]-[32]. In the feedback configuration, a tradeoff exists between the circuit noise and the input matching characteristics. This tradeoff can be alleviated using a common drain device (source follower) in the feedback path as demonstrated in [32]. Fig. 2.2 shows different CS feedback wideband LNA architectures published in the literature.

Several wideband current-reuse LNA architectures have also been reported for UWB, employing a matching network with a CS input stage and a cascaded CS stage sharing the bias current [33]-[39]. In this case, a structure of passive components is used

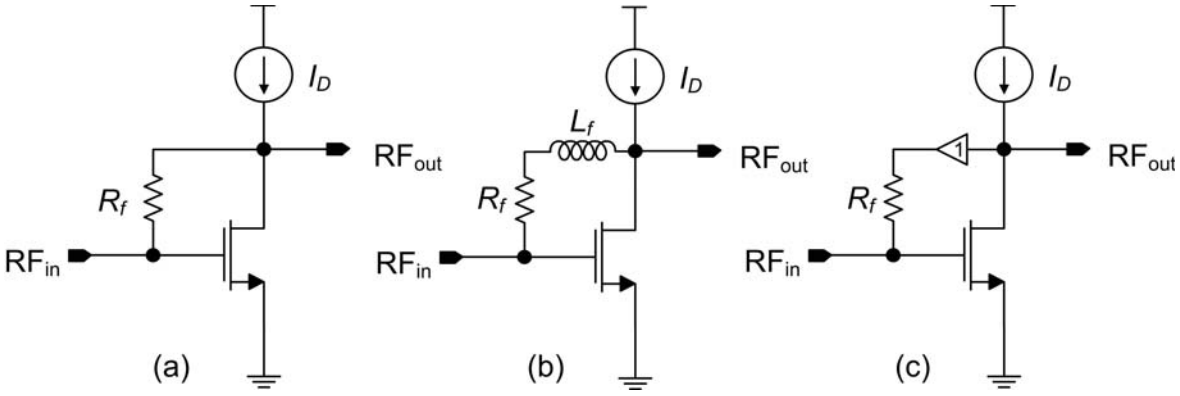

Fig. 2.2. CS feedback UWB LNAs, (a) resistive feedback, (b) inductive feedback and (c) resistive feedback with unity-gain buffer [32].

between the two cascaded CS stages to provide isolation at in-band frequencies and share the bias current at DC. Besides lower power dissipation due to current reusing, this technique provides wider bandwidth and better reverse isolation as compared to the single stage CS amplifier. A current-reuse CS UWB LNA is demonstrated in [37], where a inductive-degenerated CS stage in cascade with a CS cascode stage is employed, as illustrated in Fig. 2.3(a). The inductor L_D decouples the input CS and cascode stages at AC frequencies and shares the DC bias current between CS transistors M_1 and M_2 of the respective amplifying stages. The series LC tank circuit comprising inductor L_G and capacitor C_G, provides an in-band low impedance path and increases the overall power gain of the LNA. L_L and L_B are the peaking inductors for bandwidth extension and transistor M_4 acts as the low-impedance wideband output matching buffer for testing purposes.

The bandwidth of the CMOS LNA is mainly limited by the parasitic capacitances of the active devices. To over-come these capacitances, inductive-peaking techniques are employed by the circuit designers. The parasitics of the MOS devices with short-channel length have also reduced considerably. In this case, the lower parasitic capacitances have pushed ω_T high enough to permit inductorless LNA designs. On the other hand, the short-channel length of the MOS device reduces its intrinsic gain and multiple stages are required to extract sufficient forward power gain from the amplifier circuit. In Fig. 2.3(b) the basic cell (CMOS push-pull inverter amplifier) of the inductorless LNA is shown. Six of these inductorless basic cells were used in cascade to implement the UWB LNA [17].

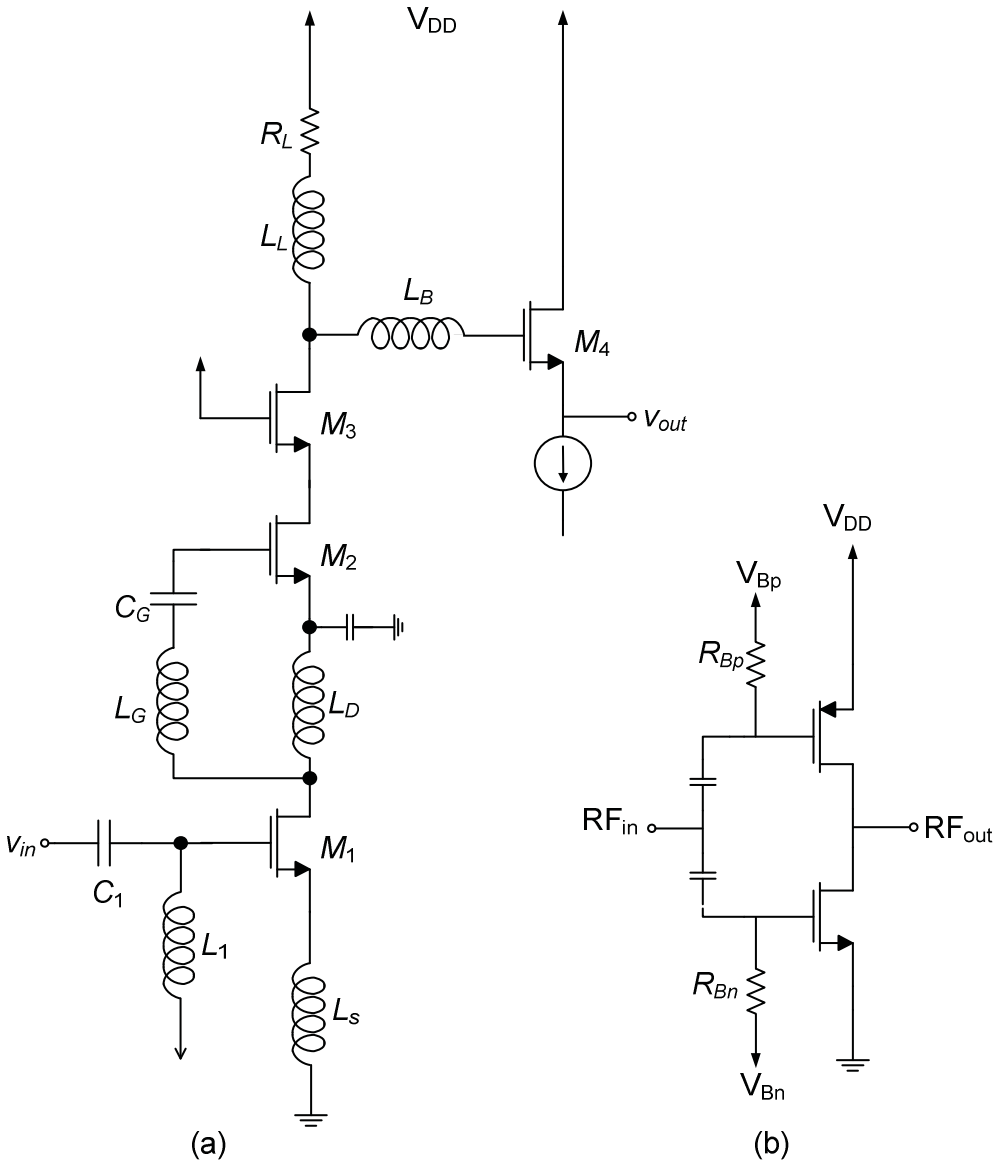

Fig. 2.3. (a) Current resuse CS UWB LNA [37] and (b) inductorless inverter amplifier [17].

2.2.2 Common Gate UWB LNA

Several researchers have adopted different variations of the CG LNA shown in Fig. 2.1(b), to achieve high performance UWB LNAs. Although the NF of the CG LNA is higher compared to its counter part at low frequency, it is almost independent of the operating frequency and the signal bandwidth. The CG LNA topology has better input matching characteristics as compared to the CS LNA and it is easier to absorb the parasitic capacitances (like C_{pad}) into the matching network. It also exhibits better reverse isolation as C_{gd} is not present in the RF signal path.

The impedance looking into the matching network shown in Fig. 2.1(b) collapses to $1/g_m$ at resonance, where g_m is purely resistive and denotes the CG device transconductance. Properly setting the DC bias point of the CG device ($\frac{1}{g_m} = R_s$) can easily achieve good matching to the source resistance R_s (power-match). Besides, the CG LNA input matching network exhibits lower $Q_{match_{CG}}$ as compared to that of the inductive-degenerated CS LNA. Hence it is easier and more feasible to design a wideband amplifier using this topology. The $Q_{match_{CG}}$ of the CG LNA is given by [27],

$$Q_{match_{CG}} = \frac{\omega C_{gs} R_s}{2} \tag{2-3}$$

In contrast to the CS LNA, $Q_{match_{CG}}$ reduces as per (2-3) with the down-scaling CMOS technology (smaller C_{gs}) hence it is easier to achieve wider bandwidth using the short-channel CG LNA topology without using many extra components. These attributes of the CG LNA topology make it popular among the wideband circuit designers [27].

Besides several advantages of the CG LNA, this topology suffers from noisy channel conductance. The noise factor of the CG LNA, denoted by F_{CG}, under the input matched condition, is given by [24], [85],

$$F_{CG} = 1 + \left.\frac{\gamma}{\alpha}\right|_{g_m R_s = 1} \tag{2-4}$$

In (2-4), γ and α are the bias dependent noise parameters and are not a function of operating frequency [24]. It makes the NF of the CG LNA constant at all frequencies. It is noted that as per (2-4), F_{CG} has a strong coupling with the g_m (and input matching condition ($\frac{1}{g_m} = R_s$)). The NF of the CG LNA can not be reduced further without sacrificing the power-match condition. To decouple the NF from the g_m of the CG device, the g_m-boosting technique is proposed [20]. A general g_m-boosted CG LNA architecture is shown in Fig. 2.4 where an inverting gain using a passive or active element is introduced

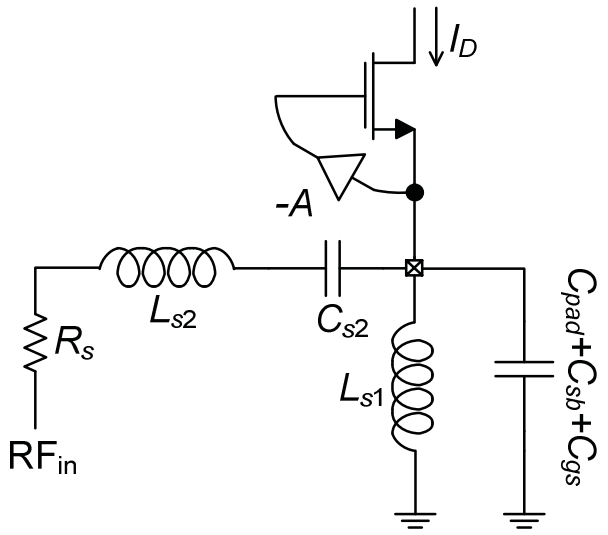

Fig. 2.4. The g_m-boosted CG UWB LNA.

between the source and the gate terminals of the CG device. As a result, the effective g_m of the CG device is *boosted* by a factor (1+A) where A is the gain magnitude of the (inverting) g_m-boosting gain amplifier. The noise factor of the g_m-boosted CG LNA is given by [85],

$$F_{CG} = 1 + \frac{\gamma}{\alpha(1+A)}\bigg|_{(1+A)g_m R_s = 1} \tag{2-5}$$

Using this technique, power-match can be achieved at lower g_m values (low power dissipation) and NF can be reduced by increasing the g_m-boosting gain A. A detailed noise analysis of the g_m-boosted CG LNA and important noise contributing entities in MOS devices are discussed in detail in the next chapter.

Due to the popularity of the CG amplifier topology to implement the UWB LNA, several designs have been proposed based on this topology to achieve wideband input match, better reverse isolation, linearity, low power consumption and low noise operation [40]-[45]. To reduce power consumption, current-reuse technique is adopted in recent topologies with CG input stage [40], [46], [47]. With regard to the g_m-boosted CG LNA architecture, several active and passive methodologies have been reported to introduce the inverting gain between the source and the gate terminals of the CG stage. Capacitive and transformer coupling are two important solutions to provide the inverting gain to boost the

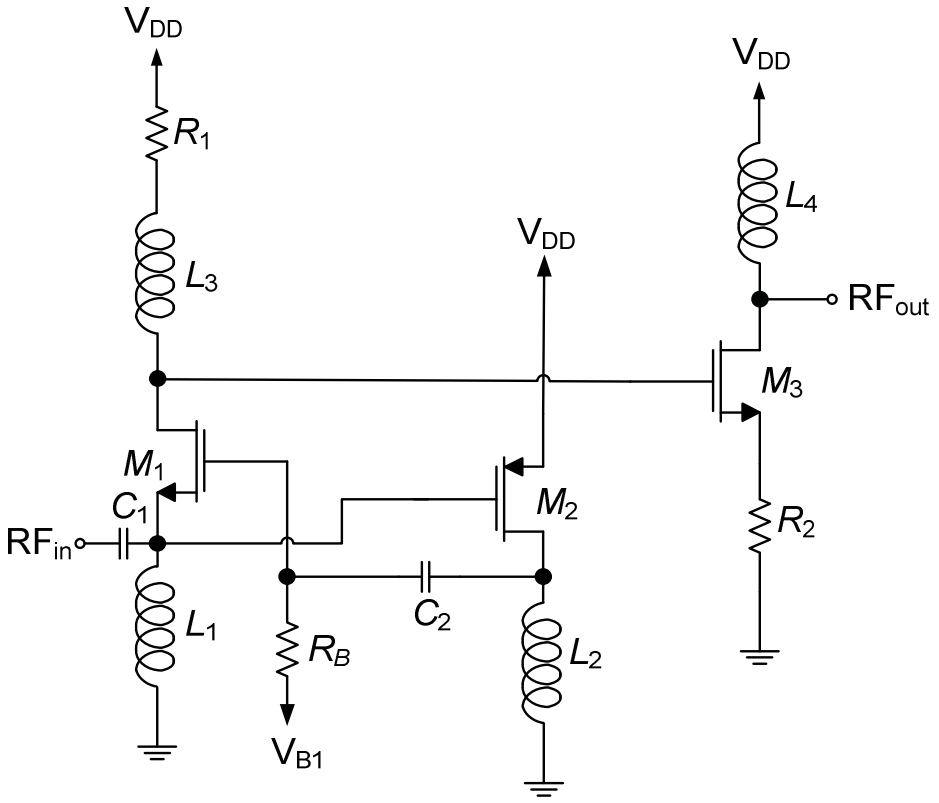

Fig. 2.5. The g_m-boosted CG UWB LNA with pMOS g_m-boosting amplifier [48].

g_m of the CG transistor. In [48], an pMOS CS amplifier is introduced as the g_m-boosting stage in the CG UWB LNA. This UWB LNA circuit is reproduced in Fig. 2.5. In this circuit, the DC power consumption is relatively large as all the three transistors M_1, M_2 and M_3, are biased separately. Here, M_1 and M_2 constitute the CG g_m-boosted and the CS g_m-boosting stages, while M_3 is a CS cascaded stage to extend the gain and bandwidth of the UWB LNA. A similar approach to introduce the inverting gain between the source and the gate terminals of the CG stage is adopted in [45] as well. Using the MOS device as the g_m-boosting stage, A can be set higher than unity and considerable reduction in the system noise is achieved on the expense of higher power dissipation due to the active g_m-boosting stage.

2.3 Conclusion

Based on the brief discussion presented in this chapter, the g_m-boosted CG topology is found suitable for UWB LNA design due to its low power and low noise performance.

The active g_m-boosting technique to implement the UWB LNA could be an attractive solution if the power dissipation due to the active g_m-boosting amplifier could be minimized.

In the next chapter, a new noise optimization mathematical model of the g_m-boosted CG UWB LNA is presented that employs a passive noise matching network at its input to maximize the over-all signal-to-noise ratio (SNR) of the CG UWB LNA. In the same chapter, a practical example of the CMOS g_m-boosted CG UWB LNA is considered using the CS stage as the active g_m-boosting amplifier. This mathematical model and the noise optimization technique are also published in [85]. The published manuscript is included in the 'Appendices' section of this thesis.

One of the techniques to reduce the power dissipation is to employ '*current-reuse*' technique. Sharing the DC bias current of the g_m-boosting amplifier with the input CG stage can be fruitful in reducing the power consumption overhead. Current sharing between the two active stages can be made possible by stacking up the g_m-boosted CG stage and the g_m-boosting amplifier. This current-reuse architecture is proposed and investigated in detail in Chapter 4 and has been accepted for publication as indicated in [96]. The accepted manuscript reporting this new current-reuse architecture is included in the 'Appendices' section of this thesis. In the published literature, no author in our knowledge has reported such circuit topology to *reuse* the bias current and share it between the two stages of a g_m-boosted CG UWB LNA.

CHAPTER 3

ANALYSIS AND DESIGN OF g_m-BOOSTED CG UWB LNA

3.1 Introduction

The need for low power and high throughput wireless communication systems has grown exponentially in the last few years. Ultra-wideband (UWB) technology has attracted immense interest from the research and industry communities because of its high data rate, robustness against multipath fading and low power dissipation. This technology provides high-bandwidth wireless link for the transmission of audio, video and high speed data. Frequency bands from 0 to 960 MHz (sub-gigahertz band) and 3.1 to 10.6 GHz are allocated by FCC for UWB communication, respectively, for medium range (<100m) low throughput, and, short range (<10m) high throughput (1 GBPS) data [49], [50]. By definition, an UWB radio signal is expected to have a fractional bandwidth greater than 20% or a bandwidth of at least 500MHz. This ultra-wide channel bandwidth *B* allows high channel capacity *C*, enabling data transfer at a very high rate, while, keeping the transmitted signal-to-noise ratio (SNR) to a minimum. This phenomenon is based on the well-known Shannon's channel capacity theorem [8], [51], and is expressed as,

$$C = B\log(1+SNR) \qquad (3\text{-}1)$$

An UWB radio stretches the transmit signal power, very sparsely, over an ultra-wide bandwidth from 500MHz to few GHz. Within the UWB operating band, the transmit signal power is kept very small to allow its coexistence with other already present co-habiting narrowband systems, and, by the same token, an UWB radio must also contend with these narrowband systems' interference [52].

A typical digital radio system consists of two parts: a transmitter and a receiver. In the transmitter, after the source coding and channel coding, the information signal is then modulated. After necessary pulse shaping and power amplification, the modulated signal is finally radiated through the antenna into the unguided channel medium. The channel

degrades, distorts and adds noise to the transmitted waveforms. At the receiver, reverse operation takes place where the received signal is captured at the antenna, filtered and amplified in the analog frontend. After digitization, it is then demodulated and error corrected to recover the actual information data bits. The crucial part of a receiver is its analog frontend that conditions and refines the received signal for digitization to achieve highest performance after demodulation and decoding in the back-end digital signal processor. The performance of the analog frontend is critically reliant on the low noise amplifier (LNA). Its role is to improve the quality of reception by amplifying the received signal and inducing as little noise and distortion as possible. In the realization of an UWB front-end, it is an enormous challenge to design and optimize the UWB LNA using standard CMOS technology. An UWB LNA must exhibit low noise performance, broadband input match and reasonably flat pass-band gain [53]. The most important performance metric of an LNA is the noise factor, which is the ratio between the total output noise power and the output noise power due to the input source. In other words, it is a metric of the input SNR degradation by the circuit or the increase in Wehrl's entropy [54] caused by the LNA.

Based on the noise performance, CMOS UWB LNA architectures can be divided into two major groups; namely the Common Source (CS) and the Common Gate (CG) LNA. General topologies of these architectures are shown in the previous chapter and are reproduced in Fig. 3.1. The noise figure (NF), i.e. noise factor in dB, of the CS LNA with inductive source degeneration is linear with the operating frequency f and can be large in the range of GHz. This architecture is inherently narrowband and achieving wideband input match to the signal source, in the presence of the parasitic capacitances (e.g. bond pad, etc) is very difficult. On the other hand, the NF of the CG LNA, although slightly higher as compared to its counter part, is independent of f. Achieving wideband input match and absorbing parasitic capacitances is relatively simple and less affected by process variations in the case of the CG topology. To optimize the noise performance of the CG LNA for UWB, several techniques have been published in literature [55]-[59]. It is also proposed to use g_m-boosting technique to reduce the noise of the UWB CG LNA and to provide input matching at lower device transconductance, g_m [60]. Wideband input matching employing higher-order input filter is also proposed in other publications [61][62].

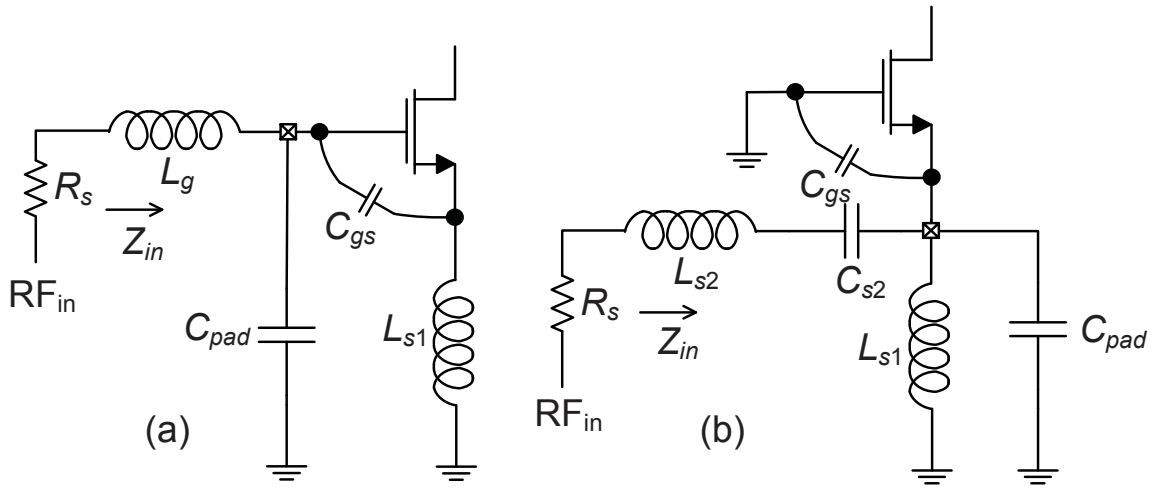

Fig. 3.1. UWB LNA architectures, (a) common source LNA and (b) common gate LNA.

Enormous amount of work has been reported for the noise optimization of the narrowband LNA systems; however, it is not appropriate to apply the same techniques to the UWB radios. The operating bandwidth of the UWB system is several orders of magnitude greater than that of the narrowband systems. Due to this fact the narrowband LNA implementation techniques can not be directly adopted for the UWB LNA design. The most relevant metric to optimize an UWB LNA is the relationship between the SNR at its input and its output and, the measure of the performance after the final digital decoding process. A design technique presented in [63] defines SNR as the matched filter bound (MFB) in order to derive and optimize a basic CS UWB LNA's noise performance in an UWB radio. In this chapter, a solution to the design of an optimum matching network is demonstrated for a g_m-boosted short-channel CG UWB LNA that minimizes the NF by applying this definition of the SNR as the MFB. This chapter also exhibits in detail, how the short-channel output conductance g_{ds} (=1/r_{ds}) and the g_m-boosting technique can be utilized to reduce the noise floor of the UWB CG LNA.

This chapter is organized as follows: The MOS device model used in this analysis is explained in section 3.2. In the same section, a general short-channel g_m-boosted CG LNA architecture and its preliminary noise analysis is also presented. In the next section, matching related circuit and system models of the UWB short-channel g_m-boosted CG LNA are explained and its different noise-related expressions using the MFB definition of SNR are derived. Sections 3.4 and 3.5 of this chapter elaborate the analysis to optimize the noise performance of the LNA by designing the appropriate matching network at the input

of the amplifier. Section 3.6 discusses the performance results including the practical circuit simulation of CMOS process related non-idealities, and, conclusions are drawn in Section 3.7 of this chapter. With regard to notations in this chapter, mathematical entities in the frequency domain are represented by capital letters [e.g., $Z(\omega)$] and the inverse Fourier transforms of these entities in the time domain are represented by corresponding lower case letters [e.g., $z(t)$]. Sometimes, if it is not necessary to be mentioned, the terms ω and t are understood to be present.

3.2 Short-Channel g_m-boosted CG LNA and Preliminaries

3.2.1 Short-channel MOS Device Model with Finite g_{ds} Effect

A simplified small signal model, with relevant noise sources, of the g_m-boosted CG LNA is shown in Fig. 3.2. Unlike the conventional CG amplifier, here, the gate terminal of the MOS device is not an AC ground and there is an inverting gain stage between it and the source terminal [64]. This inverting gain stage is assumed to be an ideal, noiseless operational amplifier with infinite input impedance and very low output impedance. As the CMOS device channel length is rapidly decreasing with technology advancements, the short-channel device output resistance r_{ds} can not be ignored, and is therefore included in the small signal model for the analysis. For the short-channel MOS device, the channel (drain-to-source) resistance is defined by [65],

$$r_{ds} = \frac{2L}{1-\frac{\Delta L}{L}} \times \frac{1}{I_D}\sqrt{\frac{qN_{sub}}{2\varepsilon_{si}}\left(V_{DS}-V_{DS,sat}\right)} \tag{3-2}$$

Where, L is the channel length, N_{sub} is the substrate doping level, ε_{si} is the silicon dielectric constant, q is the unit electronic charge, V_{DS} is the drain-to-source voltage, I_D is the drain-current and $V_{DS,sat}$ is the drain-to-source voltage at the onset of pinch-off. By applying quasi-static MOS transistor model [24], [63], [66], these terms are given by,

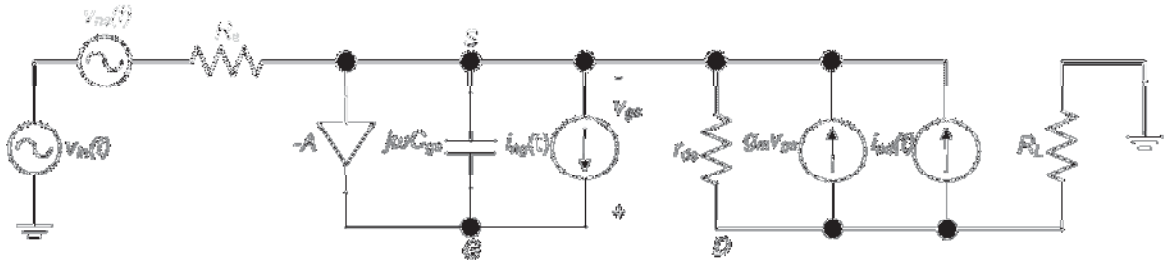

Fig. 3.2. Small signal model of the short-channel g_m-boosted CG LNA.

$$I_D = \begin{cases} 2v_{sat}C_{ox}W\dfrac{(V_{OD}-V_{DS}/2)V_{DS}}{V_{OD}+L\xi_{sat}} & V_{DS} \le V_{DS,sat} \\ v_{sat}C_{ox}W\dfrac{V_{OD}^2}{V_{OD}+L\xi_{sat}} & V_{DS} \ge V_{DS,sat} \end{cases} \tag{3-3}$$

$$V_{DS,sat} = \frac{V_{OD}}{V_{OD}+L\xi_{sat}} \tag{3-4}$$

Where, W is the width of the MOS gate and C_{ox} is the MOS gate-oxide capacitance per unit area. The gate overdrive voltage V_{OD} and the carrier saturation velocity v_{sat} are given by,

$$V_{OD} = V_{GS} - V_{TH} \tag{3-5}$$

$$v_{sat} = \frac{\mu_n \xi_{sat}}{2} \tag{3-6}$$

In addition, in (3-5) and (3-6), V_{GS} is the gate-to-source voltage, V_{TH} is the threshold voltage of the MOS device, μ_n is the electron mobility in silicon, and ξ_{sat} is the saturation electric field intensity. Also, in (3-2), ΔL is the change in the effective channel length of the MOS device due to the body effect and can be represented by,

$$\Delta L = \sqrt{\frac{2\varepsilon_{si}}{qN_{sub}}\left[\phi_B + \left(V_{DS} - V_{DS,sat}\right)\right]} \tag{3-7}$$

Where, Φ_B denotes the S/D-to-body junction built-in potential.

After inspection of the circuit in Fig. 3.2, the input resistance R_{in} looking into the source terminal of the short-channel CG LNA is given by,

$$R_{in} = \frac{r_{ds} + R_L}{1 + (1 + A) g_m r_{ds}} \tag{3-8}$$

Where, the device transconductance g_m can be expressed in terms of the normalized gate overdrive $\rho = V_{OD}/L\xi_{sat}$ and the DC power dissipation $P_D = I_D V_{DD}$ (V_{DD} is the supply voltage) by,

$$g_m = \frac{2P_D}{V_{DD} L \xi_{sat}} \left[\frac{1 + \rho/2}{\rho + \rho^2} \right] \tag{3-9}$$

By inspecting (3-8), it is clear that the effective transconductance G_m is increased to $(1+A)g_m$ due to the g_m-boosting gain between the source and the drain terminals of the MOS device. The effect of r_{ds} on the input resistance of the amplifier can also be seen from (3-8). When r_{ds} is very large in case of long-channel devices, and, in the absence of gain A, (3-8) reduces to $1/g_m$ which is the input resistance of the conventional CG amplifier.

3.2.2 LNA Noise Analysis

In Fig. 3.2, there are three noise sources: The thermal noise voltage $v_{ns}(t)$ of the RF source resistance R_s(i.e. the antenna resistance), the MOS drain current noise $i_{nd}(t)$ and the induced gate current noise $i_{ng}(t)$ [24], [65]-[67]. The power spectral densities (PSDs) of these noise sources are given by,

$$S_{v_{ns}}(\omega) = 4kTR_s \tag{3-10}$$

$$S_{i_{nd}}(\omega) = 4kT\gamma g_{d0} \tag{3-11}$$

$$S_{i_{ng}}(\omega) = 4kT\delta \frac{(\omega C_{gs})^2}{5 g_{d0}} \tag{3-12}$$

The noise sources $i_{nd}(t)$ and $i_{ng}(t)$ are random processes and are correlated with the correlation coefficient c given by,

$$c = \frac{\sqrt{S_{i_{ng}}(\omega).S_{i_{nd}}^{*}(\omega)}}{\sqrt{S_{i_{ng}}(\omega)}\sqrt{S_{i_{nd}}(\omega)}} \tag{3-13}$$

Where k is the Boltzmann constant, T is the absolute temperature, and ω is the angular frequency of operation. γ and δ are respectively the coefficients of channel and induced gate noise and are technology and bias dependent parameters. For long-channel devices, $\gamma \approx 2/3$, $\delta \approx 4/3$, and, c is complex with a value $\approx j0.394$. The constants γ and δ have higher values for short-channel MOS devices, while, the value of c reduces with deep nanometric scaling. The zero-bias drain-to-source (channel) conductance g_{d0} and the gate-to-source capacitance C_{gs}, are given by,

$$g_{d0} = \frac{2P_D}{V_{DD}L\xi_{sat}}\left[\frac{1+\rho}{\rho}\right] \tag{3-14}$$

$$C_{gs} = \frac{2}{3}\frac{P_D}{V_{DD}v_{sat}\xi_{sat}}\left[\frac{1+\rho}{\rho^2}\right] \tag{3-15}$$

At this point, for simplicity in the initial analysis of the noise in Fig. 3.2, the gate current noise $i_{ng}(t)$ is neglected, since in the case of the CG amplifier topology, it is usually considered to be very small compared to the drain current noise $i_{nd}(t)$ [68]. The susceptance $j\omega C_{gs}$ is also neglected at this stage for ease of intuitive understanding. After applying KVL and KCL to form and solve the voltage and current equations, the voltage gain A_v and output noise voltage $v_{on,ind}$ due to i_{nd} are derived as:

$$A_v = \frac{\{1+(1+A)g_m r_{ds}\}R_L}{R_s + r_{ds} + R_L + (1+A)g_m r_{ds}R_s} \tag{3-16}$$

$$v_{on,ind} = \frac{-r_{ds}R_L}{R_s + r_{ds} + R_L + (1+A)g_m r_{ds}R_s}\cdot i_{nd} \tag{3-17}$$

From the basic definition, the noise factor F of the LNA is given by,

$$F = \frac{SNR_{in}}{SNR_{out}} = \frac{S_{in}(\omega)/S_{v_{ns}}(\omega)}{S_{out}(\omega)/S_{nout}(\omega)} = \frac{S_{nout}(\omega)/S_{v_{ns}}(\omega)}{S_{out}(\omega)/S_{in}(\omega)} = \frac{S_{nout}(\omega)}{A_v^2 S_{v_{ns}}(\omega)} \tag{3-18}$$

Where $S_{nout}(\omega)$, the total noise PSD at the output of the amplifier, is given by,

$$S_{nout}(\omega) = A_v^2 S_{v_{ns}}(\omega) + \left(\frac{v_{on,ind}}{i_{nd}}\right)^2 S_{i_{nd}}(\omega) \tag{3-19}$$

For the derivation of the noise factor, the constant α is defined as the ratio between the device transconductace g_m and the zero-bias channel conductance g_{d0}. By using the equations (3-10) to (3-19), noise factor of the short-channel g_m-boosted CG LNA is then derived and given by,

$$F = 1 + \frac{\gamma}{\alpha}\left(\frac{g_m}{R_s}\right)\left[\frac{r_{ds}^2}{\{1+(1+A)g_m r_{ds}\}^2}\right] \tag{3-20}$$

For long-channel MOS device, r_{ds} is very high and (3-20) reduces to the noise factor of the *input matched* long-channel g_m-boosted CG amplifier, given by,

$$F = 1 + \frac{\gamma}{\alpha(1+A)}\bigg|_{(1+A)g_m R_s = 1} \tag{3-21}$$

Another variation of the noise factor expression can be derived for the short-channel g_m-boosted CG amplifier by including the effect of finite g_{ds} (=1/r_{ds}), which shows that, by carefully setting the device channel resistance of the amplifier, further reduction in the noise can be achieved [56]. By substituting R_s with R_{in} from (8) into (3-20) (for matched input port), F is derived and given by,

$$F \approx 1 + \frac{\gamma}{\alpha(1+A)}\left(\frac{r_{ds}}{r_{ds}+R_L}\right) \tag{3-22}$$

$$F \approx 1 + \frac{\gamma}{\alpha(1+A)}\frac{1}{2}\bigg|_{r_{ds}=R_L} \tag{3-23}$$

(3-23) clarifies the role of finite g_{ds} (=1/r_{ds}) in reducing the noise factor of the short-channel g_m-boosted CG amplifier. By setting the real part of the load impedance equal to r_{ds}, the channel current noise is reduced to half, as compared to its long-channel counter part.

3.3 Modeling Noise Matched g_m-Boosted CG UWB LNA and Noise Analysis using the MFB Definition

3.3.1 Circuit Model of the LNA

A block diagram of the *noise matched* UWB g_m-boosted CG LNA is shown in Fig. 3.3(a). The LNA comprises of three basic components: a passive matching network, an active device and a load. The active device consists of the inverting gain stage and the short-channel CG CMOS transistor stage. The inverting gain stage is at this point considered an ideal operational amplifier sinking no current at its input and not inducing any noise in the circuit. Fig. 3.3(b) is the small signal *noise matched* circuit model of the LNA indicating matching components and relevant noise sources. $Z_s(\omega)=R_s+jX_s(\omega)$ is the complex source impedance of the UWB input signal generator $v_{in}(t)$. The noise matching network consists of a series reactance $X_1(\omega)$, and a susceptance $B_2(\omega)$ parallel to the MOS input; and are assumed to be noiseless.

In a typical g_m-boosted CG LNA, the gate terminal of the MOS device is not an AC ground but connected to the DC bias voltage source V_{bias} through bias resistance R_G (as shown in Fig. 3.4). Thus, the susceptance looking into the source terminal is the effective susceptance $B_{s,eff}(\omega)$ of the sub-circuit in Fig. 3.4, due to the Miller multiplication, and is given by,

$$B_{s,eff}(\omega) = (1 + A)\omega C_{gs} \tag{3-24}$$

For better understandability and clarity, the source reactance $X_s(\omega)$ is combined with $X_1(\omega)$ and in the analysis, it is referred to as $X_a(\omega)$. Similarly, $B_b(\omega)$ is the combination of $B_{s,eff}(\omega)$ and $B_2(\omega)$.

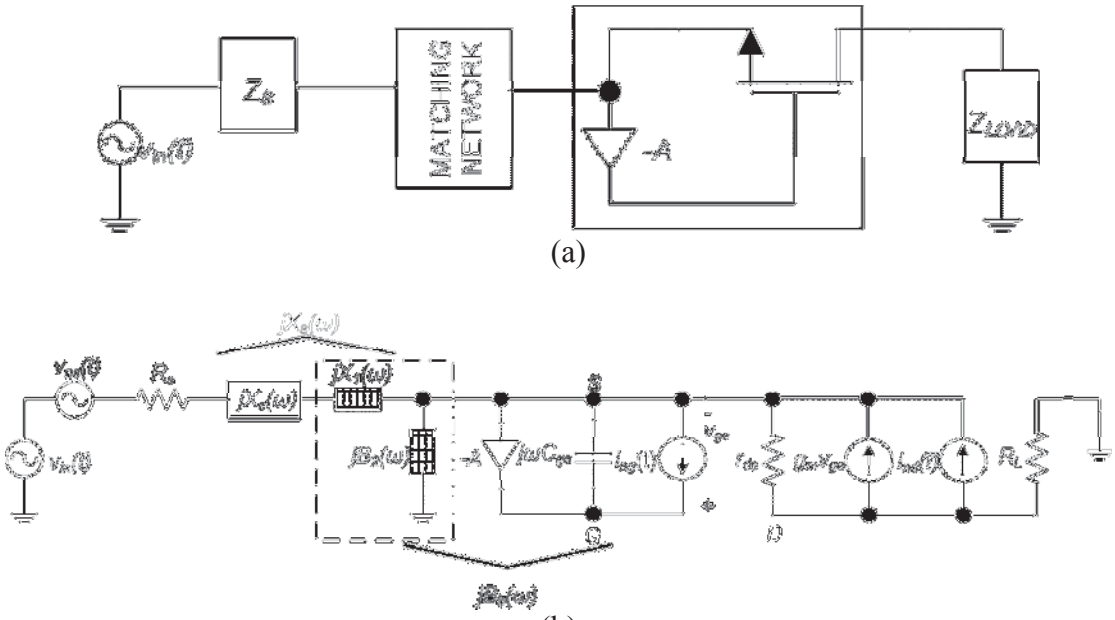

Fig. 3.3. General model of the g_m-boosted CG LNA for UWB, (a) block diagram of the LNA, and, (b) the circuit Model of the LNA.

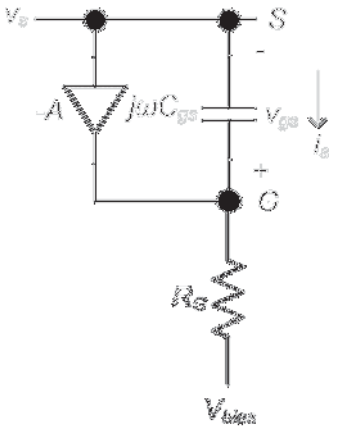

Fig. 4. Susceptance looking into the source terminal.

3.3.2 System Model of the LNA

The system model corresponding to the circuit model of Fig. 3.3(b) is shown in Fig. 3.5. The Appendix-A provides details of all the derivations leading to Fig. 3.5. If the gate current noise is ignored, it is evident that the g_m-boosting by the factor (1+A) has increased the system SNR considerably. It can be shown that a passive matching network can increase the SNR by providing minimum gain at resonance. It can be achieved by setting

$X_a(\omega) = 1/B_b(\omega)$ and making $|X_a(\omega)|$ as large as possible. But this would not be true if the gate current noise were not negligible. As shown in the system model, increasing $|X_a(\omega)|$, would amplify the gate noise and, unlike the drain current noise, there is no effect of the g_m-boosting gain stage on it. Effect of the short-channel resistance can also be appreciated by looking at the system model of the LNA. Reducing r_{ds} can reduce the drain current noise without bound and theoretically at zero channel resistance, the drain current noise completely disappears. Practically, this is not feasible as r_{ds} cannot be technologically controlled to such a limiting value.

To reduce the noise in the system, optimal values of the reactance $X_a(\omega)$ and the susceptance $B_b(\omega)$ needs to be determined. The matching network should also exploit the correlation between the noise sources to optimize the noise performance of the amplifier. For the noise analysis, the gate current noise is decomposed into two orthogonal components. The PSD due to $i_{ng,u}(t)$, the uncorrelated component *of* $i_{ng}(t)$ with $i_{nd}(t)$, is given by,

$$S_{i_{ng,u}}(\omega) = 4kT\delta \frac{(\omega C_{gs})^2}{5g_{d0}}\left(1-|c|^2\right) \tag{3-25}$$

On the other hand, $i_{ng,c}(t)$ is the in-phase component of $i_{ng}(t)$ with $i_{nd}(t)$. For the g_m-boosted CG amplifier, this is given by,

$$i_{ng,c}(t) = \left\{\frac{r_{ds}}{1+(1+A)g_m r_{ds}}\right\}.i_{nd}(t) \otimes y_c(t) \tag{3-26}$$

Where $y_c(t)$ is the correlation admittance between $i_{ng}(t)$ and the input referred noise voltage due to $i_{nd}(t)$ while, $\otimes$ indicates convolution. After some derivations (shown in Appendix-B), the correlation admittance $Y_c(\omega)$ is found and is given by,

$$Y_c(\omega) = j\frac{B_{s,eff}(\omega)}{(1+A)}\left\{\frac{1+(1+A)g_m r_{ds}}{r_{ds}g_{d0}}|c|\sqrt{\frac{\delta}{5\gamma}}\right\} = jB_c(\omega) \tag{3-27}$$

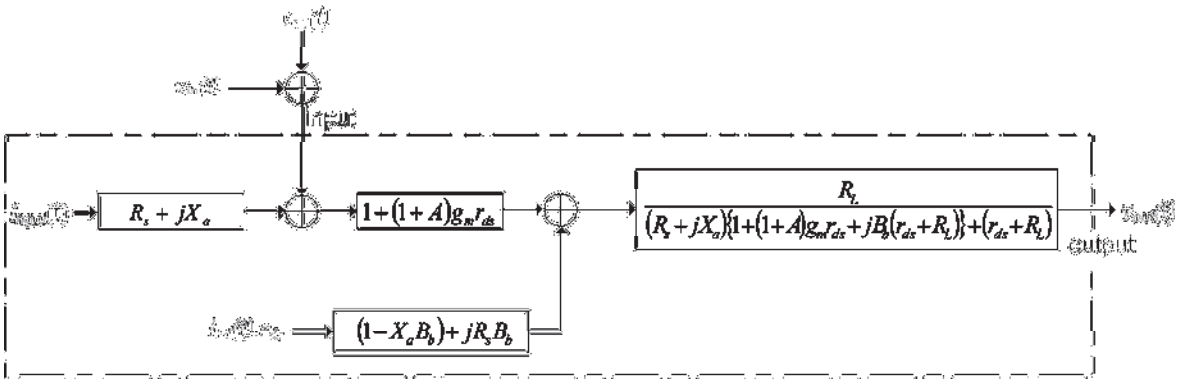

Fig. 3.5. Equivalent system model of the g_m-boosted CG LNA for UWB.

3.3.3 MFB and Noise Analysis

Using the MFB definition of the SNR [63], [69], the SNR of the received input signal at the LNA is given by,

$$SNR_{in} = \int_{-\infty}^{\infty} \frac{|P(\omega)|^2}{S_{v_{ns}}(\omega)} d\omega \tag{3-28}$$

Where, $P(\omega)$ is the transmitted signal collected at the input of the LNA corrupted by the source noise $v_{ns}(t)$. Similarly, the SNR at the output of the LNA is given by,

$$SNR_{out} = \int_{-\infty}^{\infty} \frac{|P(\omega)|^2}{S_{v_{ns}}(\omega) + S_{v_{irn}}(\omega)} d\omega \tag{3-29}$$

In (3-29), $S_{v_{irn}}(\omega)$ is the total noise PSD at the input of the LNA due to the internal noise sources of the MOS device, and is given by,

$$S_{v_{irn}} = S_{i_{nd}} \left[\frac{r_{ds}^2}{\{1+(1+A)g_m r_{ds}\}^2} \right] \left[\{1 - X_a(B_b + B_c)\}^2 + R_s^2 (B_b + B_c)^2 \right] + S_{i_{ng,u}} \left(R_s^2 + X_a^2 \right) \tag{3-30}$$

The first term in (3-30) is the input referred noise PSD due to $i_{nd}(t)$, and, the second term in this expression is the PSD due to $i_{ng,u}(t)$ at the input of the LNA.

By inspection of the system model in Fig. 3.5, it is clear that there is no effect of the matching network on the SNR_{in} and the noise factor can only be minimized by maximizing the SNR_{out} given in (3-29). Hence, the main design goal is to find optimal values of $X_a(\omega)$ and $B_b(\omega)$ in order to maximize SNR_{out}.

3.4 Optimizing the Matching Network

Based on (3-30), the drain current noise can be minimized considerably by setting the device transconductance or the gain of the g_m-boosting stage appropriately. These parameters do not have any effect on the uncorrelated gate current noise. Where as, the input referred noise spectral density, due to both the internal noise sources is affected by the matching network. A frequency dependant parameter $\pi(\omega)$ is defined with the dimensions of $1/\Omega^2$. It is the ratio of the uncorrelated gate current noise power and the input referred drain current noise power for the short-channel CG amplifier and is given by,

$$\pi(\omega) = \frac{S_{i_{ng,u}}(\omega)}{S_{i_{nd}}(\omega)\dfrac{r_{ds}^2}{\{1+(1+A)g_m r_{ds}\}^2}} \tag{3-31}$$

To find the optimal reactance $X_a(\omega)$and susceptance $B_b(\omega)$ to maximize SNR_{out}, the infinite integral in (3-29) is differentiated partially with respect to $X_a(\omega)$ and $B_b(\omega)$, solving for $X_a(\omega)$ and $B_b(\omega)$ respectively, after setting the differentiation result to zero. Two possible results are obtained depending on the target of optimization and the operating conditions. If $\pi(\omega)\geq 1$ and the input $S_{i_{ng,u}}$ minimization is the main objective, the optimum $X_a(\omega)$ and $B_b(\omega)$, denoted by $X_{a,opt}(\omega)$ and $B_{b,opt}(\omega)$, are then given by,

$$X_{a,opt}(\omega) = 0 \tag{3-32}$$

$$B_{b,opt}(\omega) = -B_c(\omega) \tag{3-33}$$

In this case, the input-referred $S_{i_{nd}}$ can be reduced by utilizing the g_m-boosted technique. In the second case, $S_{v_{irn}}$ minimization, as a whole, is the main design goal, independent of the

device transconductance and the g_m-boosting gain (effective transconductance G_m). Here, $\pi(\omega)<1$ and the input-referred drain current noise is minimized by decreasing the gain in the matching network without increasing the corresponding gate current noise and $X_{a,opt}(\omega)$ and $B_{b,opt}(\omega)$ are derived as,

$$X_{a,opt}(\omega) = \pm\sqrt{R_s\left(\sqrt{1/\pi(\omega)} - R_s\right)} \tag{3-34}$$

$$B_{b,opt}(\omega) = \pm\sqrt{\frac{\pi(\omega)}{R_s}\left(\sqrt{1/\pi(\omega)} - R_s\right)} - B_c(\omega) \tag{3-35}$$

Although (3-32) to (3-35) are similar to those derived for the CS UWB LNA [63], they imply quite different implementation aspects of the matching network design for the g_m-boosted CG LNA. It is quite evident from the system model of the LNA in Fig. 5, that the uncorrelated gate current noise PSD $S_{i_{ng,u}}(\omega)$ can be the dominant noise component in the total noise PSD $S_{v_{irn}}$, over the input referred drain current noise power, due to, (a) the short-channel length effect in nanometric CMOS (which results in finite g_{ds} values and reduced noise correlation coefficient magnitude, $|c| < 0.3$ [70]-[72], and (b) the g_m-boosting gain. In this scenario $\pi(\omega)\geq 1$ is true, otherwise, for long-channel amplifier devices (with $r_{ds} \to \infty$ and $|c|$ close to 0.4) and without g_m-boosting, $\pi(\omega)<1$.

As in this case of nanometric g_m-boosted design $\pi(\omega)\geq 1$, the optimal reactance and susceptance, as given by (3-32) and (3-33), represents almost a second order circuit at resonance, where the floating series reactive part of the network is cancelled out, while, its grounded parallel susceptive part remains equal but opposite to the correlation susceptance that optimizes the noise performance. By substituting (3-32) to (3-35) into (3-29), the optimal noise factor F_{opt} of the UWB g_m-boosted CG LNA is derived and is given by (3-36); and, the corresponding power gain G_{opt} (V^2/V^2) of this LNA, with the optimal matching network is given by (3-37).

$$F_{opt} = \frac{1}{\int_{\theta_1} \frac{1}{1+\frac{\gamma}{\alpha R_s}\left[\frac{g_m r_{ds}^2}{\{1+(1+A)g_m r_{ds}\}^2}\right]+\frac{\delta R_s \omega^2 C_{gs}^2\left(1-|c|^2\right)}{5g_{d0}}}\left(\frac{|P(\omega)|^2}{P_T}\right)d\omega + \int_{\theta_2} \frac{1}{1+\left[\frac{g_m r_{ds}}{1+(1+A)g_m r_{ds}}\right]\frac{\omega}{\omega_T}\sqrt{\frac{4\gamma\delta}{5}\left(1-|c|^2\right)}}\left(\frac{|P(\omega)|^2}{P_T}\right)d\omega} \tag{3-36}$$

$$G_{opt} = (1+(1+A)g_m r_{ds})^2 R_L{}^2 \times \int_{-\infty}^{\infty} \frac{1}{\{R_s(1+(1+A)g_m r_{ds})+(r_{ds}+R_L)(1-X_{a,opt}B_{b,opt})\}^2 + \{R_s B_{b,opt}(r_{ds}+R_L)+X_{a,opt}(1+(1+A)g_m r_{ds})\}^2} \left(\frac{|P(\omega)|^2}{P_T}\right) d\omega \quad (3\text{-}37)$$

In (3-36) and (3-37), $P_T = \int |P(\omega)|^2 d(\omega)$, and,

$$\theta_1 = \omega : \pi(\omega) \geq 1, \; for \; \forall \, \omega \quad (3\text{-}38)$$

$$\theta_2 = \omega : \pi(\omega) < 1, \; for \; \forall \, \omega \quad (3\text{-}39)$$

Also, ω_T is the unity gain angular frequency given by,

$$\omega_T \approx \frac{g_m}{C_{gs}} \quad (3\text{-}40)$$

3.4.1 Noise Factor of the LNA for Narrowband Assumption

If the input signal is a single tone, as in the case of a narrow band LNA, such that, the input signal power is non-zero only at the tone angular frequency ω_0, then, assuming $|\omega| = \omega_0$ and $\pi(\omega) \geq 1$, (3-36) collapses to,

$$F_{opt} = 1 + \frac{\gamma}{\alpha R_s}\left[\frac{g_m r_{ds}^2}{\{1+(1+A)g_m r_{ds}\}^2}\right] + \frac{\delta R_s \omega^2 C_{gs}^2 \left(1-|c|^2\right)}{5 g_{d0}} \quad (3\text{-}41)$$

(3-41) proves that when narrow-band assumption is made, neglecting the last term, the above equation simplifies to (3-20) which is the noise factor of the g_m-boosted narrowband short-channel CG LNA. This deduction also validates the consideration of the case $\pi(\omega) \geq 1$ for (3-31).

3.4.2 Effect of UWB Bandwidth on Noise Factor

The effect of the ultra-wide bandwidth of the input signal on the noise factor of the UWB CG LNA discussed in the previous sections, is now studied by assuming the input

signal power to be constant within the pass-band [$|\omega|$ ε (ω_1, ω_2)] and zero out of it, for simplicity. Assuming $\pi(\omega)\geq 1$, the optimum noise factor given in (3-36) then reduces to,

$$F_{opt} = \frac{1}{\frac{1}{\Delta\omega\sqrt{\psi_1\psi_2}}\left[Tan^{-1}\left(\omega_2\sqrt{\frac{\psi_2}{\psi_1}}\right) - Tan^{-1}\left(\omega_1\sqrt{\frac{\psi_2}{\psi_1}}\right)\right]} \tag{3-42}$$

Where $\Delta\omega=(\omega_2-\omega_1)$, ψ_1 is the noise factor as given in (3-20) and,

$$\psi_2 = \frac{\delta \cdot R_s C_{gs}^2\left(1-|c|^2\right)}{5g_{d0}} \tag{3-43}$$

Next, using the trigonometric infinite series $Tan^{-1}z=z-z^3/3+z^5/5\ldots\ldots$ to expand (3-42) and, ignoring the higher order terms of the expanded series, F_{opt} is given by,

$$F_{opt} \approx \psi_1 = 1+\frac{\gamma}{\alpha}\left(\frac{g_m}{R_s}\right)\left[\frac{r_{ds}^2}{\{1+(1+A)g_m r_{ds}\}^2}\right] \tag{3-44}$$

F_{opt} given by (3-44) is now the same as (3-20), and is independent of the input signal bandwidth, which is an important new result. This analysis thus proves the advantage of the CG LNA over the CS LNA [63] whose noise performance degrades with increasing bandwidth. Hence, the CG LNA is a better alternative for UWB LNA design, where the signal bandwidth can reach up to a few GHz.

3.4.3 Trade-off between Power Match and Noise Match

For maximum power transfer between the ultra-wideband signal source (e.g. antenna) and the UWB LNA, the input impedance $Z_{in}(\omega)$ of the LNA should be equal to the complex conjugate of the UWB signal source. This is accomplished by setting up the operating point of the UWB LNA such that the real part of $Z_{in}(\omega)$ would approximate R_s and the imaginary part would be cancelled out using noiseless resonant circuits, over the UWB input signal bandwidth. $Z_{in}(\omega)$ of the LNA circuit model in Fig. 3(b) is given by,

$$Z_{in}(\omega) = jX_1(\omega) + \frac{1}{\frac{1+(1+A)g_m r_{ds}}{r_{ds}+R_L} + jB_b(\omega)} \tag{3-45}$$

If the imaginary terms in (3-45) are cancelled out through resonant elements, $Z_{in}(\omega)$ coincides with $R_{in}(\omega)$ in (3-8), which is purely resistive. $X_1(\omega)$, in (3-45), can be resonated out with source reactance $X_s(\omega)$ such that $X_a(\omega)= X_s(\omega)+X_1(\omega)=0$; which is one of the conditions for optimal noise matching as well. However, there is a tradeoff between noise match and power match in setting $B_b(\omega)= B_{s,eff}(\omega) +B_2(\omega)=0$ which is contrary to the condition for optimal noise match in (3-33). It is also clear from (3-45) that matching the real part of $Z_{in}(\omega)$ to R_s becomes possible at lower g_m (hence consuming less DC power) due to the effect of the g_m-boosting gain A.

3.5 Practical Matching Network Implementation

To illustrate the g_m-boosted CG UWB LNA design approach presented in this chapter, a practical design example is now considered. To achieve optimal noise performance, structures of the matching network are selected based on (3-32) and (3-33) as shown in Fig. 3.6. In this design example, the UWB signal source impedance is assumed to be purely resistive with R_s=50Ω. A large susceptance, $B_1(\omega)=1/X_1(\omega)$ is used, making $X_a(\omega)\approx X_{a,opt}(\omega)=0$. The susceptance $B_1(\omega)$ is implemented using a large capacitor in series such that it provides perfect short-circuit at AC frequencies. Next, as $B_2(\omega)+B_{s,eff}(\omega)=B_b(\omega)$ and, based on (3-33) $B_{b,opt}(\omega)=-B_c(\omega)$, $B_{2,opt}(\omega)$ is replaced by the reactance $X_{2,opt}(\omega)=1/B_{2,opt}(\omega)$ which is realized as a grounded inductor L_2 in parallel. Its optimal reactance $X_{2,opt}(\omega)$ is thus given by,

$$X_{2,opt}(\omega) = \frac{1}{B_{s,eff}(\omega) + B_c(\omega)} \tag{3-46}$$

If the parasitic (bottom-plate) capacitance of C_1 is included in the analysis, it will appear in parallel with the $C_{gs,eff}$ and L_2, and, in the process of calculating $L_{2,opt}$, it can be

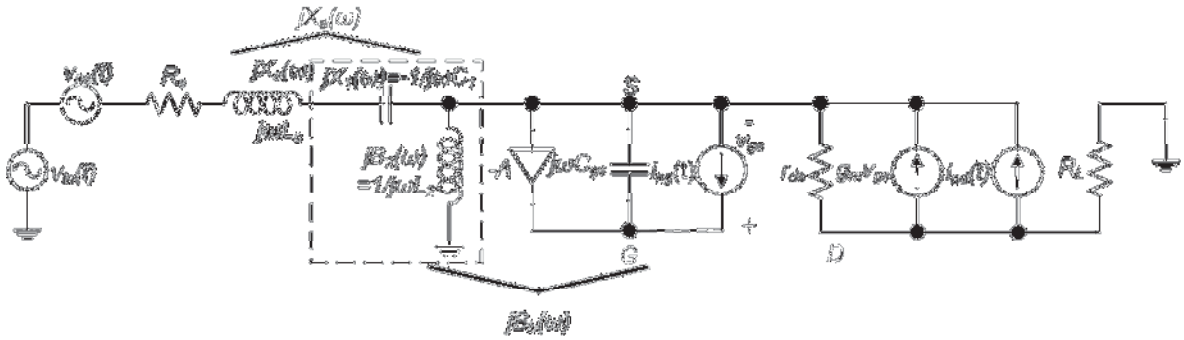

Fig. 3.6. Optimal LNA matching network implementation.

considered as a part of $C_{gs,eff}$ and merged (added) into it. This can be an advantage as the size of $L_{2,opt}$ would be smaller in that case with the larger composite $C_{gs,eff}$.

Next, the noise factor and the voltage power gain of the LNA circuit in Fig. 6 are derived as (3-47) and (3-48) at the bottom of this page. To find the value of L_2 that minimizes the noise generated by this LNA, numerical iterative search technique is applied by approximating the integral in (3-47) by finite summation, using *MATLAB*. For numerical optimization of (3-47) for the UWB signal with 7.5 GHz bandwidth with center frequency of 6.85 GHz; operating parameters are extracted from the 130nm IBM CMOS process, using the MOS device model described in Section II and the *Cadence SpectreRF* simulator. For W=15μm and V_{DS}=1V the following transistor parameters are extracted: g_m=8.215mS, C_{gs}=6.25fF, g_{d0}=12.3mS and r_{ds}=1.6KΩ. The noise parameters γ, δ and c for the short-channel MOS device are assumed to be 2/3, 4/3 and j0.395 respectively [70]-[72]. Also, in order to evaluate the developed mathematical model of the g_m-boosted CG LNA with regard to the noise and bandwidth non-idealities of the CS g_m boosting amplifier, a CMOS g_m-boosted CG LNA as shown in Fig. 3.7 is designed and simulated in *Cadence SpectreRF* using the IBM 130nm CMOS process parameters. Thermal noise perturbations are inserted in the circuit diagram to indicate the inclusion of contributions to SNR degradation due to the gate current noise and the uncorrelated drain current noise in both the CS gain boosting amplifier and the CG LNA. The DC bias points for the CS gain boosting amplifier (M_2) and the CG LNA (M_1) are set using a bias voltage of 0.5V feed via separate bias resistors R_{B1} and R_{B2} (similar to the Fig. 3.4 in the earlier discussion). A load resistance R_L of 1K (comparable to MOS finite r_{ds}) is used for the CG stage, while, the CS amplifier is implemented with a load resistance R_D of 250Ω which yields an average g_m-

boosting gain of approximately 1.8 over the UWB. Both the devices M_1 and M_2 have a *W/L* ratio of 15um/0.13um. For the above given operating parameters and the g_m-boosting gain of 1.8, the theoretically optimal inductance (based on the introduced model) $L_{2,opt}$ is found to be 27.8 nH. To take into account the contribution of the correlated gate current noise due to the drain current noise, the correlation capacitances are C_{c1}=10fF for M_1, and, C_{c2}=3.75fF for M_2 calculated respectively using (3-27) for the CG device M_1, and the correlation admittance derivation in [63] for the CS device M_2. These capacitances are included in the circuit simulation of the composite LNA.

$$F = \frac{1}{\int_{-\infty}^{\infty} \frac{1}{1+\frac{\gamma}{\alpha R_s}\left\{\frac{g_m r_{ds}^2}{(1+(1+A)g_m r_{ds})^2}\right\}\left[1+R_s^2\left\{\frac{(1+A)\omega^2 L_2 C_{gs}-1}{\omega L_2}+\omega C_{gs}\left(\frac{1+(1+A)g_m r_{ds}}{r_{ds}g_{d0}}|c|\sqrt{\frac{\delta}{5\gamma}}\right)\right\}^2\right]+\frac{\delta R_s \omega^2 C_{gs}^2\left(1-|c|^2\right)}{5g_{d0}}}\left(\frac{|P(\omega)|^2}{P_T}\right)d\omega} \tag{3-47}$$

$$G_{opt} = (1+(1+A)g_m r_{ds})^2 R_L{}^2 \times \int_{-\infty}^{\infty} \frac{1}{\{R_s(1+(1+A)g_m r_{ds})+(r_{ds}+R_L)\}^2+\left[\frac{R_s\{1-\omega^2(1+A)C_{gs}L_{2,opt}\}(r_{ds}+R_L)}{\omega L_{2,opt}}\right]^2}\left(\frac{|P(\omega)|^2}{P_T}\right)d\omega \tag{3-48}$$

3.6 Analytical and Circuit Simulation Results

The performance results are now obtained using the parameters described in the previous section. The received signal is assumed to be a 3.1 to 10.6 GHz UWB band-pass signal. The optimal inductance $L_{2,opt}$ that maximizes the output SNR of the g_m-boosted LNA circuit model in Fig. 3.6, is determined by solving (3-47) numerically. This solution indicates an inverse relationship between the g_m-boosting gain A and $L_{2,opt}$ which is plotted in Fig. 3.8. It is also found that the LNA exhibits minimum NF at a frequency of around 5.7 GHz. At this frequency, the theoretical value of $L_{2,opt}$, using (3-46) and that using the numerical analysis of (3-47) are found to be almost the same. The variation of the difference between these two entities, $\Delta L_{2,opt}$ with A, is also plotted in Fig. 3.8. Plots of the optimal parallel susceptance $B_{b,opt}(\omega)$ and the optimal parallel reactance $X_{2,opt}(\omega)$ are shown in the Fig. 3.9 and the Fig. 3.10 respectively. In these figures, the gain A is varied between 0.6 and 3.0 in 0.6 steps. The plot of the optimal NF (NF_{opt}=$10log_{10}F_{opt}$) is shown

in the Fig. 3.11, while, Fig. 3.12 shows the plots of the *dB* voltage power gain G_{opt} for the same set of operating parameters and g_m-boosting gain values. The noise figure and the voltage power gain curves are obtained using respectively (3-47) and (3-48) of the introduced g_m-boosting LNA model. NF_{opt} and G_{opt} are found to be almost independent of the frequency of operation at lower values of A. NF_{opt} becomes slightly frequency dependent at higher values of A with the increase in the gate current noise at higher frequencies owing to higher correlation admittance. Over all, considerable reduction in the NF_{opt} is achieved with increasing g_m-boosting gain A using the optimized matching network, as per (3-44) of the g_m-boosting LNA. To investigate the sensitivity of the noise-matched g_m-boosted CG UWB LNA circuit model of Fig. 3.6 with process related variations in the g_m-boosting gain, A, noise and impedance analysis are carried out for small gain perturbations around A=1.8 (chosen at random). For the operating conditions given in section V, the optimal NF of the LNA for A=1.8 is around 1.6dB as shown in Fig. 11. The NF of the LNA, with up to ±0.2 variation in A in the vicinity of A=1.8, is plotted in Fig. 3.13 indicating a variation of ±0.2dB in the NF of the LNA. Similarly, the corresponding variations in the real and the reactive parts of $Z_{in}(\omega)$ of the LNA are also plotted in the Fig. 13. Variations of ±9Ω and ±3Ω in the real and the reactive part respectively of $Z_{in}(\omega)$ are observed.

Circuit simulation results are next discussed to compare the analytical performance of the presented optimization model with the actual performance of practical CMOS LNA circuit. The effect of the non-idealities of the CS g_m- boosting stage on the composite noise optimized g_m-boosted CG UWB LNA design are also investigated. In this regard, the simulated noise performance (at room temperature of 298K) of the CMOS UWB LNA circuit shown in Fig. 3.7 and discussed in the previous section, is now explored. Ignoring the noise contribution of the CS stage initially, the simulated NF of the composite g_m-boosted CG LNA, $NF_{CG\text{-}sim}$, is almost same as the analytical NF_{opt} for A=1.8. All the analytical and simulated gain and NF of the g_m-boosted CG UWB LNA are plotted in the Fig. 3.14 for comparison. There is a slight increase in the $NF_{CG\text{-}sim}$ at higher UWB signal frequencies, which is due to the loss of the over-all simulated gain, G_{sim}, of the LNA at higher frequencies. The loss in G_{sim} at higher frequencies is due to the substrate leakage and other parasitics. This can be prevented by using advanced bandwidth extension techniques such as shunt peaking. The simulated total NF of the LNA including the noise

contribution of the CS g_m-boosting stage, $NF_{t\text{-}sim}$ is also shown in the Fig. 3.14. It is found to be within an acceptable range for the CG UWB LNAs being mostly under 4 dB. The noise contribution of the CS g_m-boosting stage ($= NF_{t-sim} - NF_{CG-sim}$) is almost constant at around 1.8dB across the UWB band as shown in Fig. 14.

To study the tradeoff between input power matching and noise matching, for the same set of operating parameters described above, and assuming that the imaginary component of the input impedance of the LNA, Im[$Z_{in}(\omega)$], can be reduced to zero (tuned out) if needed; A is calculated using (3-45) to be 2.88 if the real component of the input impedance of the LNA, Re[$Z_{in}(\omega)$] is matched to R_s. For optimal noise matching at this value of the g_m-boosting gain, $L_{2,opt}$ is found to be 20.1nH using (3-24), (3-33) and (3-46) in sections 3.3, 3.4 and 3.5 respectively. In that case, switched varactor tuning option may be introduced at the source terminal for optional impedance matching (power matching) with co-incident *sub-optimal* noise matching, if desirable. Fig. 3.15 plots the NF and the rectangular components of $Z_{in}(\omega)$ for this noise match using (3-45) to (3-47). In this regard, a process technology related variation of A of ±0.1 in the vicinity of A=2.88 is also investigated to evaluate its effect on the NF and $Z_{in}(\omega)$ of the g_m-boosted CG UWB LNA as shown in the Fig. 3.15.

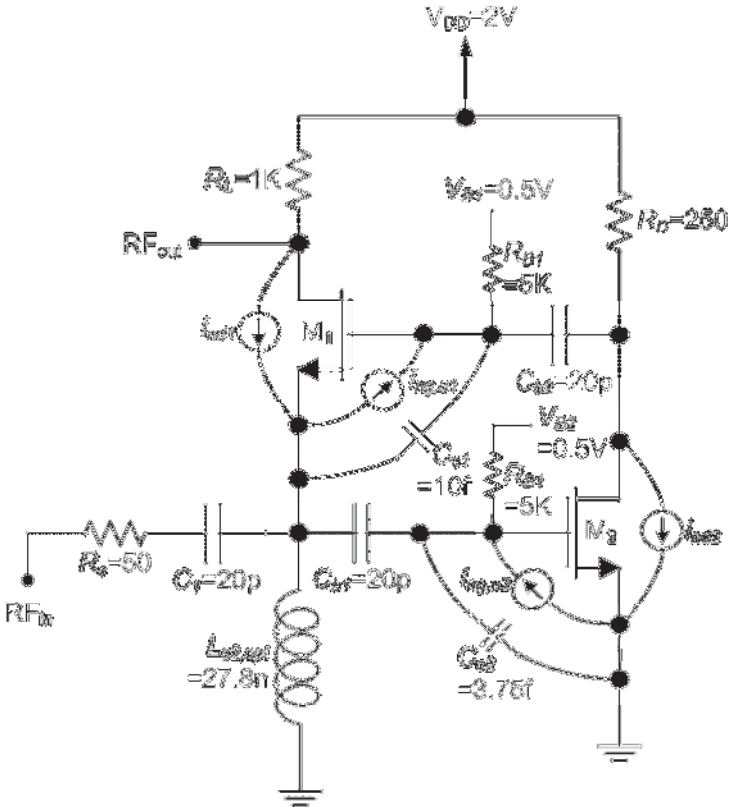

Fig. 3.7. Practical CMOS g_m-boosted CG LNA implementation circuit with noise optimization matching circuit.

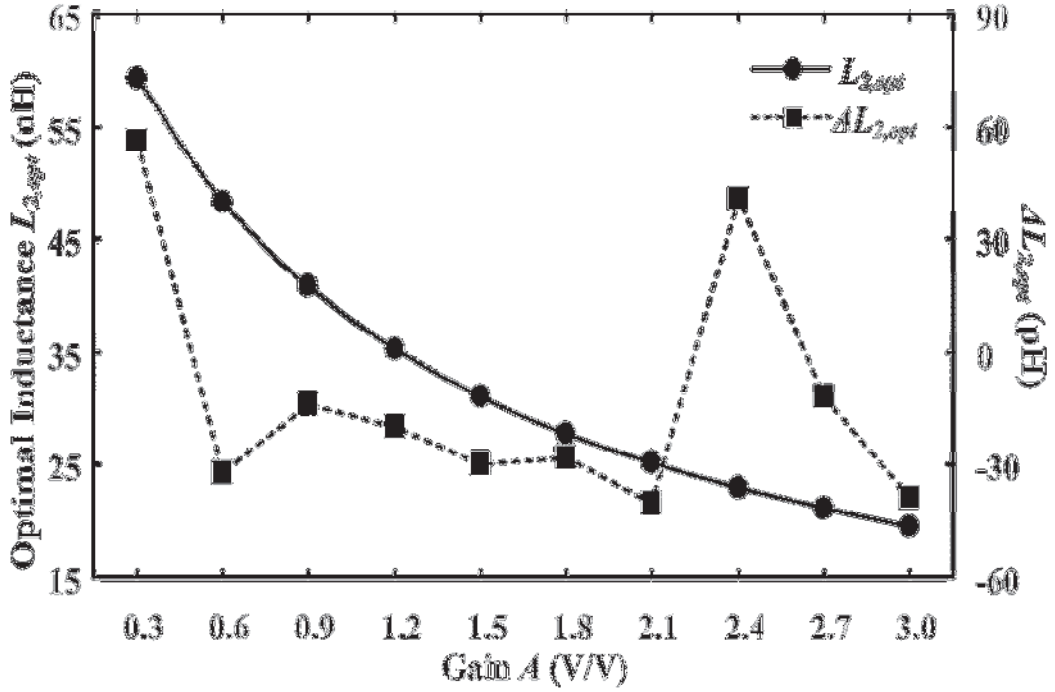

Fig. 3.8. Optimal inductance for the matching network.

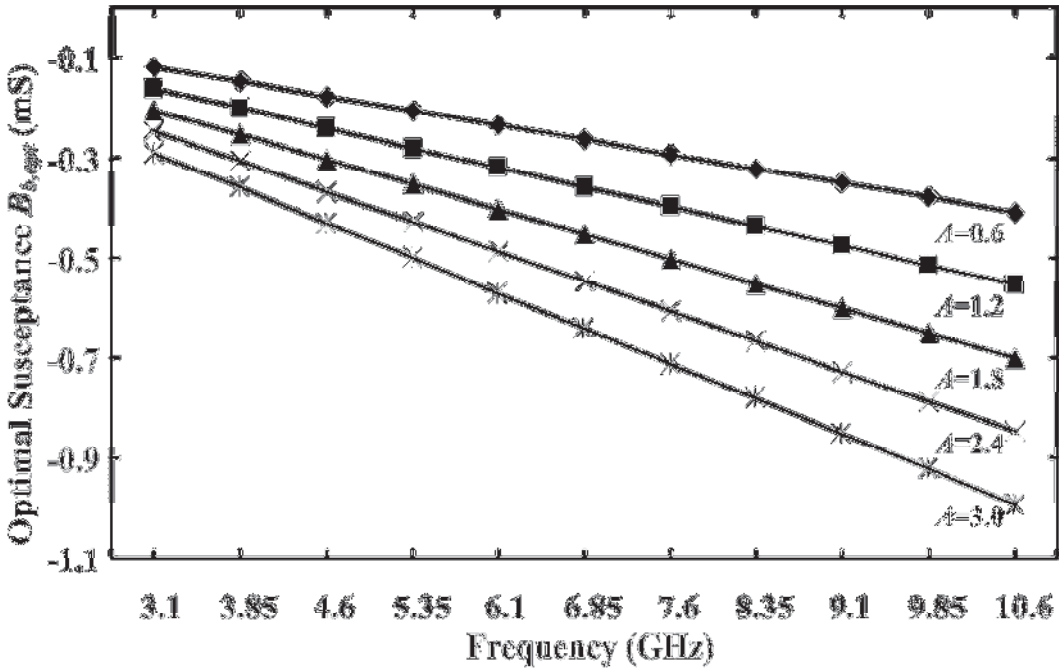

Fig. 3.9. Optimal parallel susceptance $B_{b,opt}$ with varying g_m-boosting gain A (when C_{gs}=6.25fF and g_m=8.215mS).

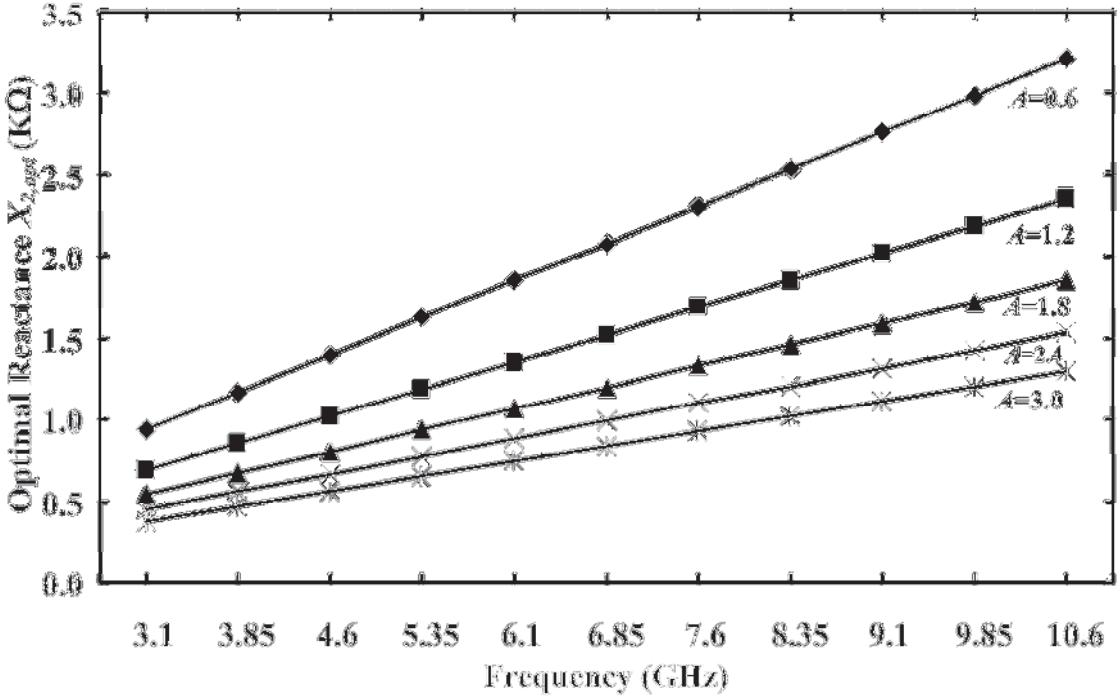

Fig. 3.10. Optimal reactance $X_{2,opt}$ for noise matching with varying g_m-boosting gain A (when C_{gs}=6.25fF and g_m=8.215mS).

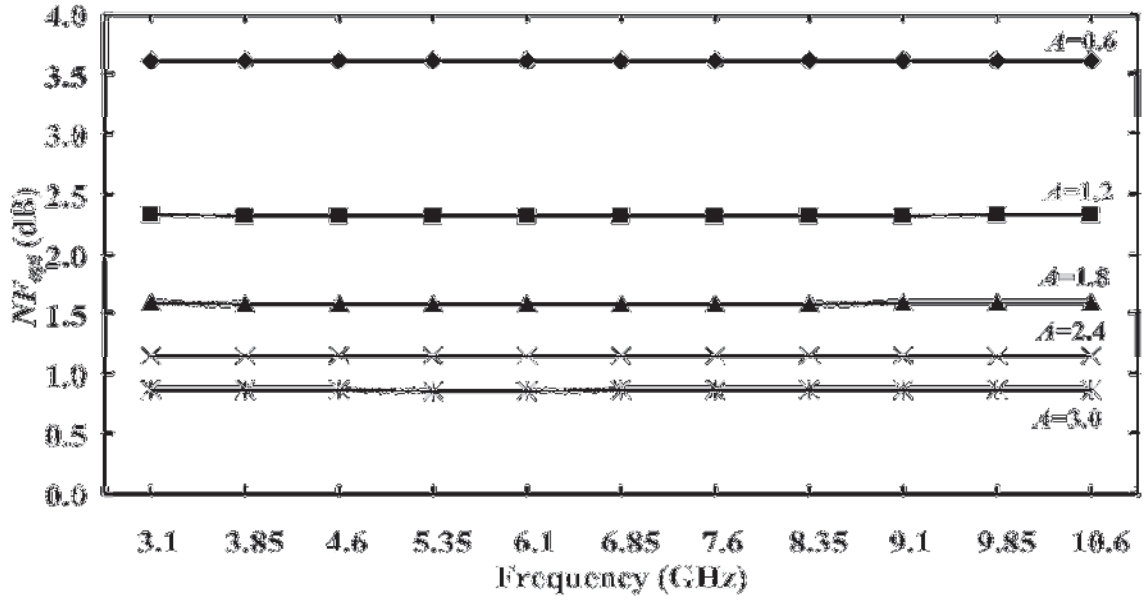

Fig. 3.11. Optimal noise figure curves with varying g_m-boosting gain A (when C_{gs}=6.25fF and g_m=8.215mS).

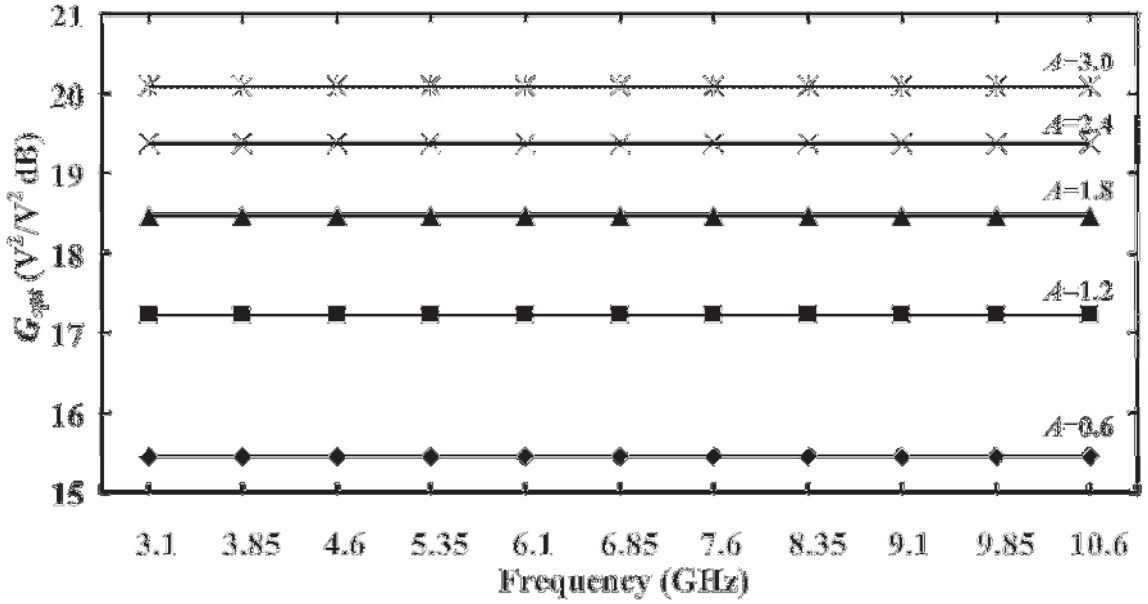

Fig. 3.12. Optimal voltage power gain with varying g_m-boosting gain, A (when C_{gs}=6.25fF and g_m=8.215mS).

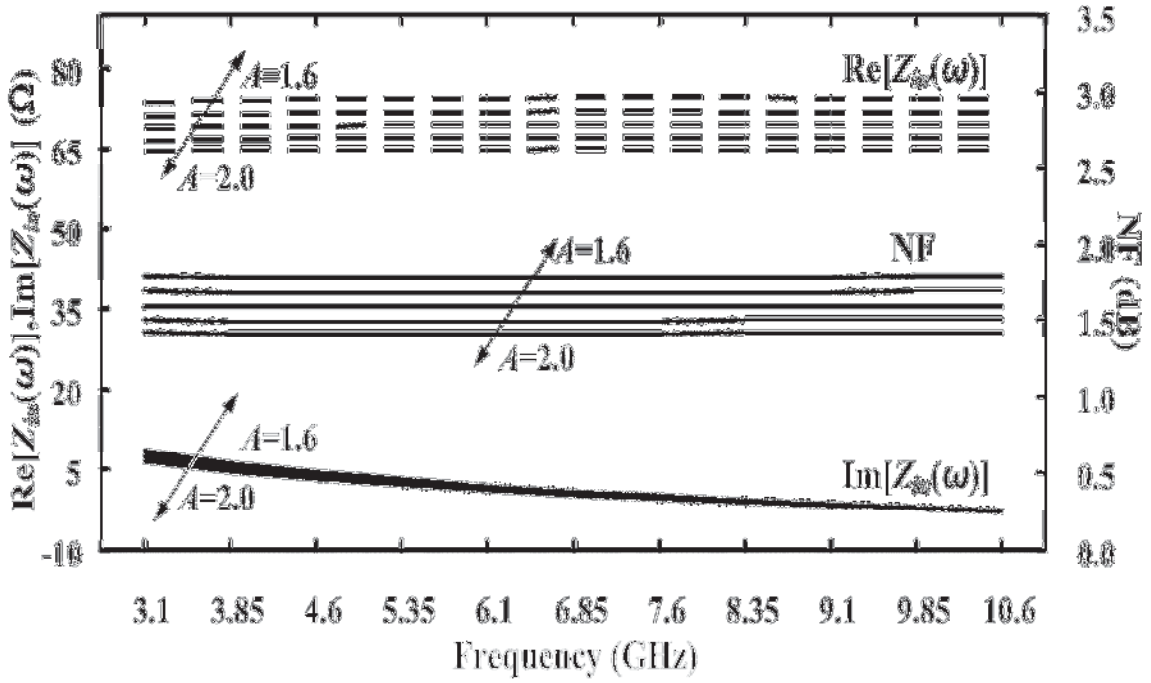

Fig. 3.13. Variations in the input impedance $Z_{in}(\omega)$ and the noise figure (NF) of the g_m-boosted CG UWB LNA, with $L_{2,opt}$=27.8nH, and, A varying between 1.6 and 2.0 in 0.1 steps.

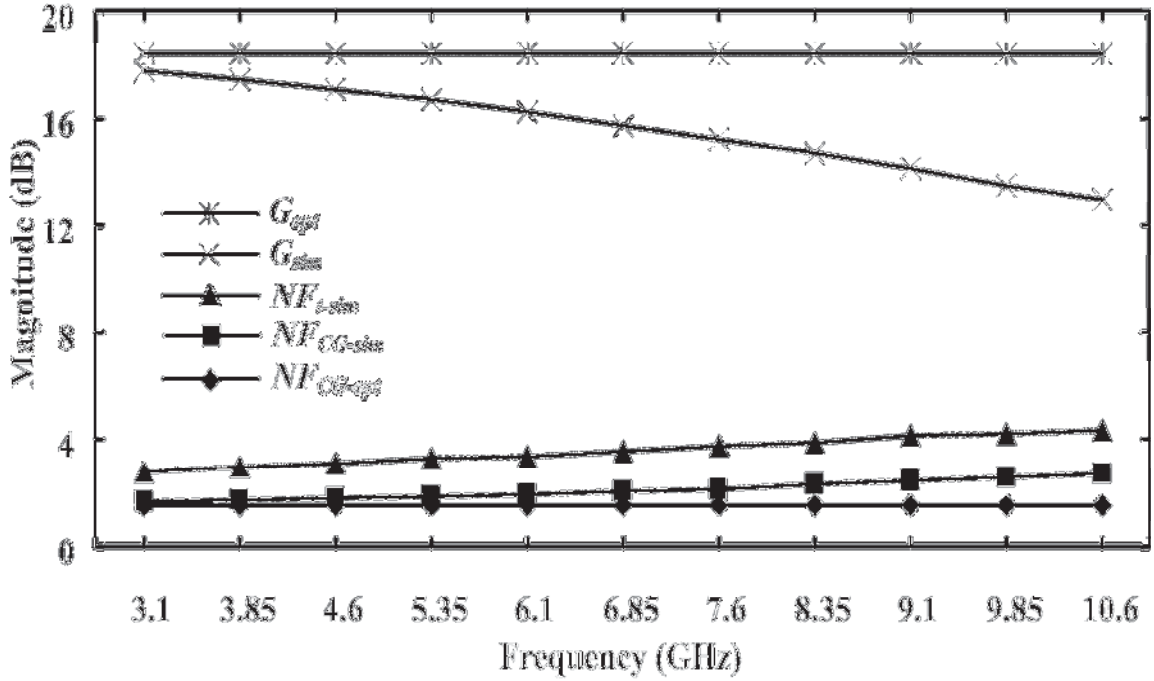

Fig. 3.14. Comparison between the optimal (analytical) and the simulated overall gain of the LNA, and, curves showing the optimal $NF_{CG\text{-}opt}$, the simulated $NF_{CG\text{-}sim}$ (ignoring noise

contribution by the CS stage), and, the overall (total) simulated $NF_{t\text{-}sim}$ (including the noise contribution by the CS stage).

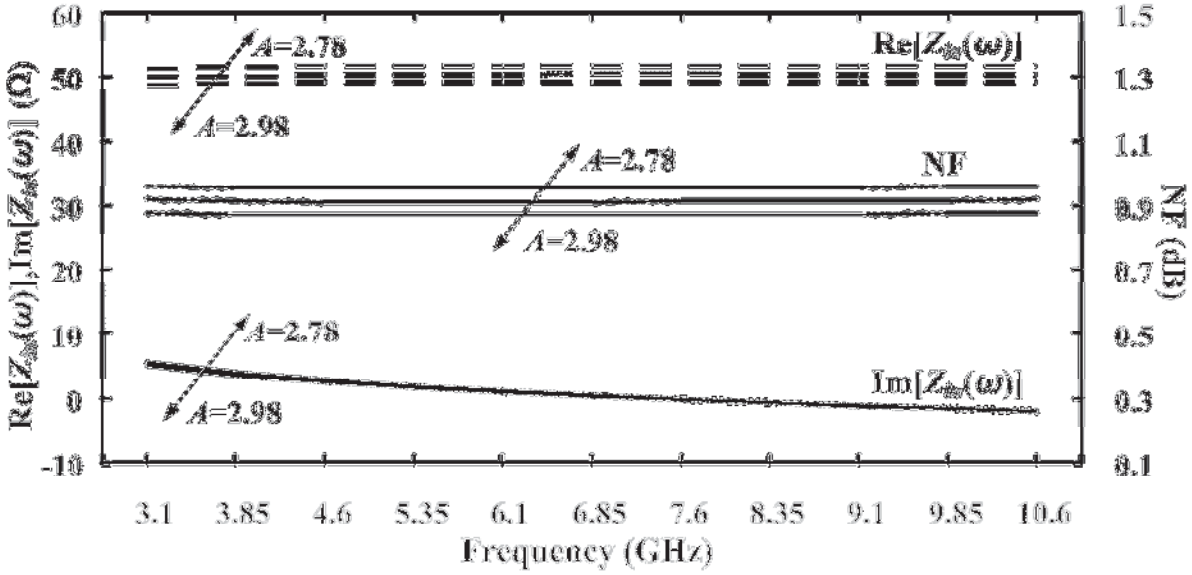

Fig. 3.15. Values and variations in the input impedance $Z_{in}(\omega)$ and the NF of the UWB g_m-boosted CG LNA for process related variation of A by ±0.1 in the vicinity of A=2.88 for input power match (with sub-optimal noise match) using $L_{2,opt}$=20.1nH.

3.7 Conclusion

A general analysis of the g_m-boosted CG LNA for UWB is presented in this chapter. It is proven that, in contrast to the UWB CS LNA, the noise performance of the UWB CG LNA with the g_m-boosting technique is independent of the bandwidth of the input signal and is almost constant. It is found that the NF of the UWB CG system can be considerably improved by increasing the g_m-boosting gain. The noise analysis presented in this chapter, defines the SNR of the system as MFB, which represents the upper limit on the performance of digital RF systems. Using this definition of SNR, the noise matching network for the g_m-boosted CG LNA architecture is optimized for the short-channel MOS devices taking into consideration the finite g_{ds}(=1/r_{ds}) effect. Reduction in the NF is achieved by, (a) improving the output SNR of the system, (b) reducing the gate current

noise as much as possible, and, (c) keeping the drain current noise to a minimum. Depending on the chip area and other constraints, the g_m-boosting gain can be specifically set to optimize the noise, provide input power matching to the UWB signal source, and, determine the size of the parallel inductor. The noise analysis also shows the trade-off between noise matching and input impedance matching. Following the analysis, a design example is considered, whereby a noise matching network is designed and the effect of the g_m-boosting gain on the matching network is studied. Also, through the circuit simulation of a practical CMOS g_m-boosted CG UWB LNA design example, the dependence of the NF on the noise and the non-ideal effects of the g_m-boosting CS device have also been explored.

In the next chapter, a novel single-ended (SE) current-reuse CMOS g_m-boosted CG LNA architecture is investigated. The SE UWB LNA utilizes a CS stage to provide the g_m-boosting gain and is fabricated using 130nm IBM CMOS process. The power consumption of the proposed circuit is optimized by '*re-using*' the bias current and sharing it between the 'g_m-boosted' CG and the 'g_m-boosting' CS stages of the UWB LNA. The new current-reuse g_m-boosted CG UWB LNA design has been accepted for publication as mentioned in [96]. The manuscript of the accepted paper is attached in the 'Appendices' section of this thesis.

CHAPTER 4

DESIGN, FABRICATION AND TESTING OF CURRENT-REUSE g_m-BOOSTED CG UWB LNA FOR 3-5GHz BAND

4.1 Introduction

The overwhelming technological advancements have pushed the CMOS device dimensions to the low nanometer scale. For the futuristic system-on-chip (SOC) designs, the ability to integrate digital and basic analog and RF building blocks with low power consumption is an acute necessity. Also, scaling to nanometric dimensions have resulted in CMOS devices achieving transit frequencies (f_T) comparable to those of bipolar junction transistors (BJTs) [73]-[75]. Since the Federal Communications Commission (FCC) defined the frequency spectral mask for the ultra-wideband (UWB) radios, and authorized this technology for commercial use in 2002 [76], [77], Ultra-Wideband (UWB) has been the emerging broadband wireless technology that promises the connectivity within 3.1 to 10.6 GHz UWB. It has been of great significance for the academic and industrial communities to investigate better techniques to realize UWB transceiver using the 'continually shrinking' CMOS technologies (e.g., [78]-[84]). Various methods of pulse shaping and pulse modulation can be adopted to utilize the vast UWB spectrum. WiMedia Alliance proposes multiband orthogonal frequency division multiplexing (MB-OFDM) for the future UWB systems and divides the UWB spectrum between 3.1 to 10.6 GHz into 14 sub-bands, each of which is 528 MHz wide [73]. The 14 sub-bands are further combined into 5 band-groups as shown in Fig. 4.1 [74], [75].

The UWB LNA is required to provide adequate forward gain, matching to 50Ω antenna source, low power consumption and low noise figure (NF). It also must possess high linearity with high input referred third order intercept point (IIP3). In published literature, several techniques have been reported to impart high performance in the design of the UWB LNA. Based on the input matching characteristics and noise performance, the published CMOS UWB LNA architectures can be divided into two major groups, the

common source (CS) and the common gate (CG) LNA. General topology of these architectures is shown in Fig. 4.2. The noise factor of the CS LNA with inductive source degeneration is linear with the operating angular frequency and can be large in the GHz range as its output gate current noise increases with the increase in ω. This architecture is inherently narrowband and achieving wideband input match to the signal source, in the presence of the parasitic capacitances (e.g. bond pad, package and board traces) is quite difficult [19], [67]. In this case, advanced design techniques are required to provide wideband input match to meet UWB matching requirements. On the other hand, the CG LNA noise factor, although slightly higher as compared to its counter part, is almost independent of ω and remains nearly constant irrespective of the bandwidth and the frequency of operation. Also, achieving wideband input match and absorbing parasitic capacitances is relatively simple and is less effected by process variations in the case of the CG topology. The CG UWB LNA, shown in Fig. 4.2(b), has a parallel resonant RLC-network with the quality factor ($Q = \frac{\omega C_{gs} R_s}{2}$) ignoring other parasitics and the body effect. As the Q is proportional to the gate-to-source capacitance C_{gs}, it would decrease with shrinking technology and hence, the bandwidth would demonstrate a broad-band behavior. Therefore, the CG LNA can easily be adopted for broadband impedance matching without many extra components [27]. Although, the NF of the CG LNA ($\approx 1+[\gamma/\alpha]$) depends on the device size and process parameters, it remains almost constant with $\boldsymbol{\omega}$. Also, the NF of the CG LNA has a strong coupling with the bias point, or, in other words, the $1/g_m$ input matching resistance looking into the source. Reduction in the output noise floor of the CG LNA is achieved by using the g_m-boosting technique that de-couples the input matching and the NF of the CG LNA [68].

Current-reuse technique has been used in many recent LNA topologies [33]-[39], [76]-[79] to reduce power consumption in mobile devices. In this chapter, a new current-reuse g_m-boosted CG LNA architecture with a passive LC-band-pass filter for broadband input matching with sharp out-of-band roll-off is reported. The circuit operates in the UWB band between 3.1 and 4.8 GHz and utilizes an active g_m-boosting CS gain stage that shares the bias current with the CG amplifying stage to drastically reduce the power dissipation.

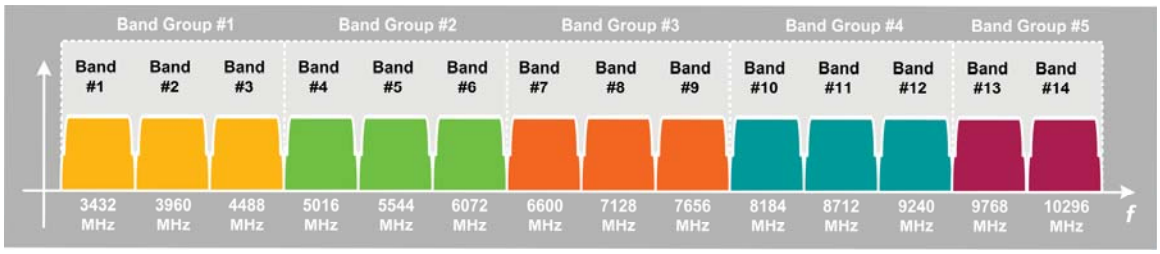

Fig. 4.1. Frequency plan of WiMedia multiband orthogonal frequency multiplexing for UWB [18], [43].

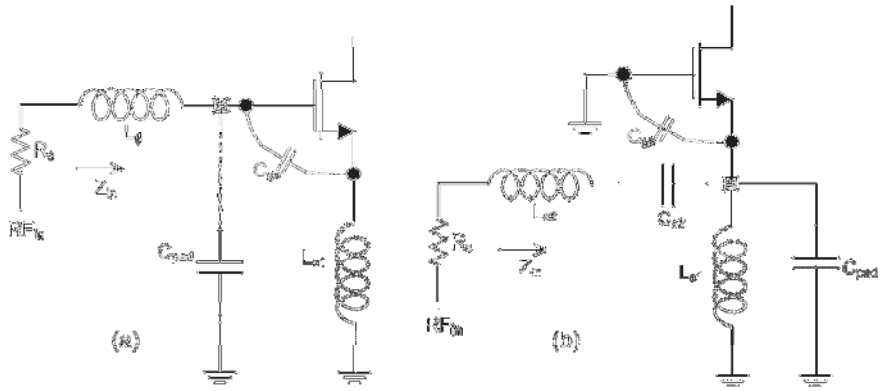

Fig. 4.2. UWB LNAs, (a) common source LNA, (b) common gate LNA.

The organization of this chapter is as follows: The basic principle of operation of the current-reuse g_m-boosted CG configuration is explained in section 4.2. In the same section, the circuit topology of the proposed short-channel g_m-boosted CG LNA architecture is presented. In the next section, the small signal model and noise analysis of the proposed architecture is explained and its various mathematical expressions are derived. Sections 4.4 and 4.5 provide respectively the circuit design and simulation, and, the fabrication and experimental results of the proposed optimized UWB LNA. Finally, conclusions are drawn in the Section 4.6 of the chapter, based on the performance of the proposed LNA. With regard to the notations in this chapter, similar approach is used as in the previous chapter. Here, mathematical entities in the frequency domain are represented by capital letters [e.g., $Z(\omega)$] and the inverse Fourier transforms of these entities in the time domain are represented by the corresponding lower case letters [e.g., $z(t)$]. Sometimes, if it is not necessary to be mentioned, the terms ω and t are understood to be present.

4.2 Current-Reuse g_m-Boosted CG UWB LNA

4.2.1 Current-Reuse Technique

In literature, several narrowband and broadband current-reuse architectures have been proposed and majority of them are based on a cascade of CS stages (CS-CS) sharing the bias current [33]-[39]. To adequately isolate the cascading stages, a single inductor is used. For better isolation, in [33], LC T-network is used to provide third order isolation in the operating band along with improved noise performance. In [77], a narrowband g_m-boosted CG LNA with current-reuse technique is introduced that uses a CS amplifier as the cascaded stage (CG-CS) to boost the gain. In this design, the g_m-boosting gain is provided using the transformer coils connected across the source and the gate terminals of the input device. Despite the transformer being a passive device consuming no electrical power, it is not suitable for adoption in UWB applications due to process non-linearities, and, the presence of low parasitic resistance that can cause pronounced noise at the output of the amplifier.

A g_m-boosted CG UWB LNA is designed in [48], which utilizes an active pMOS CS device to provide the inverting g_m-boosting gain. The circuit diagram of the proposed UWB LNA in [48] is reproduced in Chapter 2 in Fig. 2.5. This design does not utilize the current-reuse technique, and the bias currents through the CG amplifying stage and the CS g_m-boosting stage are not shared. It also utilizes another CS stage in cascade which is separately biased as well and causes more power dissipation. The UWB LNA circuit, proposed in this chapter, takes advantage of the current-reuse technique by 'stacking' the active pMOS stage (that provides the inverting g_m-boosting gain between the source and the gate terminals of the input CG stage) on top of the input CG stage ("*piggyback* g_m-boosting"). Thus the new approach, proposed here, is to reduce the power dissipation by implementing current-reuse technique with the g_m-boosting, while the current is shared between the g_m-boosting (CS) and amplifier (CG) stages. An appropriate isolation circuit is designed to separate out the CG and the CS stages at in-band AC-frequencies and for sharing the DC bias current. The isolation circuit also provides the loading on the drain terminals of the CG and the CS stages for adequate gain.

4.2.2 Circuit Topology

The circuit topology of the proposed UWB LNA is shown in Fig. 4.3. A CG amplifying device M_1 is used at the input. The CG stage with low input impedance characteristic and broadband behavior provides NF that is almost independent of the frequency of operation. The CG stage also eliminates the Miller effect and hence provides better isolation from the output return signal. To decouple the NF from the input matching condition and to reduce the noise floor, the pMOS CS stage M_2 is used as the g_m-boosting inverting amplifier. The CS stage M_2, in conjunction with the low impedance path of the series resonant LC tank with inductor L_t and capacitor C_t, provides the inverting gain $A(\omega)$ between the source and the gate terminals of M_1. The gain $A(\omega)$ boosts the g_m of M_1 by a factor of $[1+A(\omega)]$, without having to increase its device size or the bias current [20]. As a result, better UWB noise performance and input matching is accomplished without increasing power dissipation.

While the series resonant L_t and C_t provides a low impedance path between the drain of M_2 and the gate of M_1, the isolation circuit has an impedance which is adequately large to provide a high impedance path between the drains of the two MOS devices, and to provide loading for reasonable gain for the g_m-boosting and amplification stages. Since the 2nd order resonant circuit composed of L_t and C_t presents a narrowband characteristic, it is tuned at a frequency that is nearer to the upper end of the desired band [37] instead of a mid-band frequency. In this way, the increasing impedance of this tank circuit, as the signal frequency deviates from the resonant frequency at the lower end of the desired band, is compensated by the higher intrinsic gain of the devices at lower frequencies.

An LC T-network is chosen as the isolation circuit between the amplifying and the g_m-boosting stages considering its advantages over the simple single inductor circuits [33]. The 3rd order low pass LC T-network with series inductor coils L_n and L_p, and a large shunt capacitor C_{sh}, provides adequate isolation between the drain terminals of M_1 and M_2, in the frequency band of operation which is necessary for the amplification. L_n and L_p also carry the common DC bias current through M_1 and M_2 making the current-reuse possible and thus reducing the power consumption. In addition, the large capacitor C_{sh} acts as a bypass capacitor for AC-frequencies with the inductors acting as loads for the corresponding MOS devices.

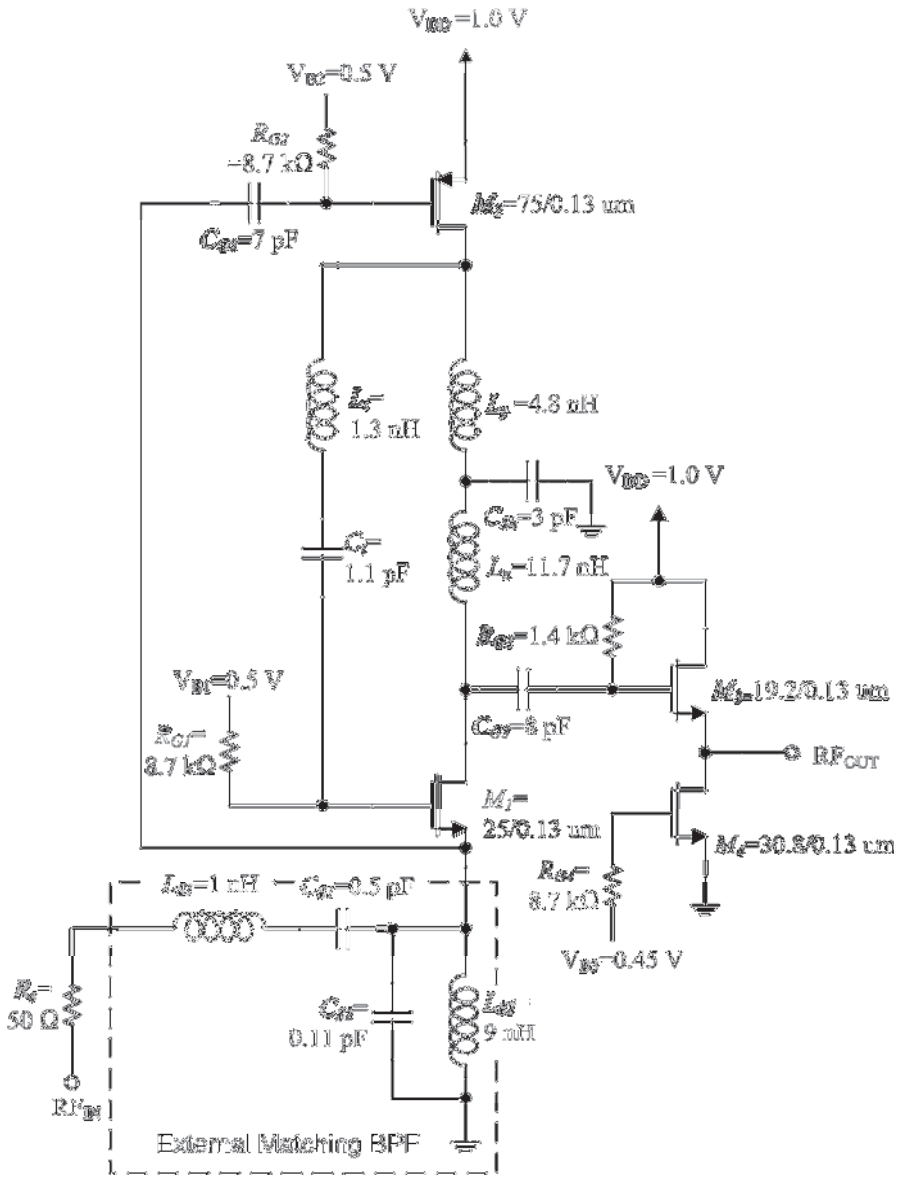

Fig. 4.3. Schematic of the proposed g_m-boosted current-reuse CG LNA operating in band group#1 of UWB.

In order to achieve wideband input match, an off-chip 4th order LC band-pass filter (BPF) is used at the amplifier input. The BPF starts with a series branch and ends with a shunt branch, where L_{s1} and L_{s2} are the series and shunt branch inductors respectively. C_{s1} and C_{s2} are the corresponding series and shunt capacitors. This filter architecture is chosen in order to provide sharp out-of-band roll-off and to absorb the CG stage parasitics into the filter. The shunt branch inductor L_{s2} also facilitates the DC biasing by sinking the common

drain current of M_1(and M_2) to the circuit ground. The impedance-matched band-pass LC section is obtained using *automatic filter generation software* [80].

The devices M_3 and M_4 constitute an output buffer to provide 50Ω match for testing purpose. The capacitors C_{G2} and C_{G3} are AC-coupling capacitors while R_{G1}, R_{G2}, R_{G3} and R_{G4}, are biasing resistances. The bias voltages to setup the DC operating point of the amplifier are generated by on-chip current mirror circuits that are not shown in the schematic diagram of Fig. 4.3.

4.3 LNA Architectural Analysis and Design Methodology

Fig. 4.4. represents the equivalent small signal model of the proposed g_m-boosted current-reuse CG UWB LNA excluding the output buffer. For simplicity of the analysis, the large bypass and AC-coupling capacitors are replaced by short circuits in the small signal model. The UWB small signal input source $v_{in}(t)$, with source resistance R_s, is assumed to have constant power within the pass-band [$|\omega| \varepsilon (\omega_L, \omega_H)$] and zero outside it. Hence, the BPF at the input of the amplifier is acting as a lossless matched filter within the UWB pass-band. It is assumed that the BPF is not inducing any noise into the circuit; hence, it is replaced by a short circuit path in the model. Similarly, the LC tank circuit composed of L_t and C_t is also replaced by a short circuit. The bulk terminals of the MOS devices M_1 and M_2 are shorted to the circuit ground and V_{DD}, respectively to remove the back-gate or body effect. Hence, the body effect of the MOS devices is ignored in the analysis of the UWB LNA. C_{gs1} and C_{gs2} are the gate-to-source capacitances of M_1 and M_2 respectively, while, v_{gs1} and v_{gs2} are the gate-to-source small signal voltages of the respective MOS devices. Although, C_{gs2} is shown in the small signal model for clarity, it can be open-circuited by absorbing its susceptance, $B_2(\omega)=\omega C_{gs2}$, into the shunt branch of the BPF. g_{m1} and g_{m2} are the transconductances of M_1 and M_2 respectively. In order to study the effect of the finite short-channel resistance (due to the nanometric shrinking of the MOS devices) on the performance of the proposed UWB LNA, the short-channel resistances, r_{ds1} and r_{ds2} of the corresponding MOS devices are also included in the model for analysis.

In today's nanometric processes short-channel devices posses very small gate-to-source capacitances (of the order of *fF*) and small channel resistance. Looking at the small

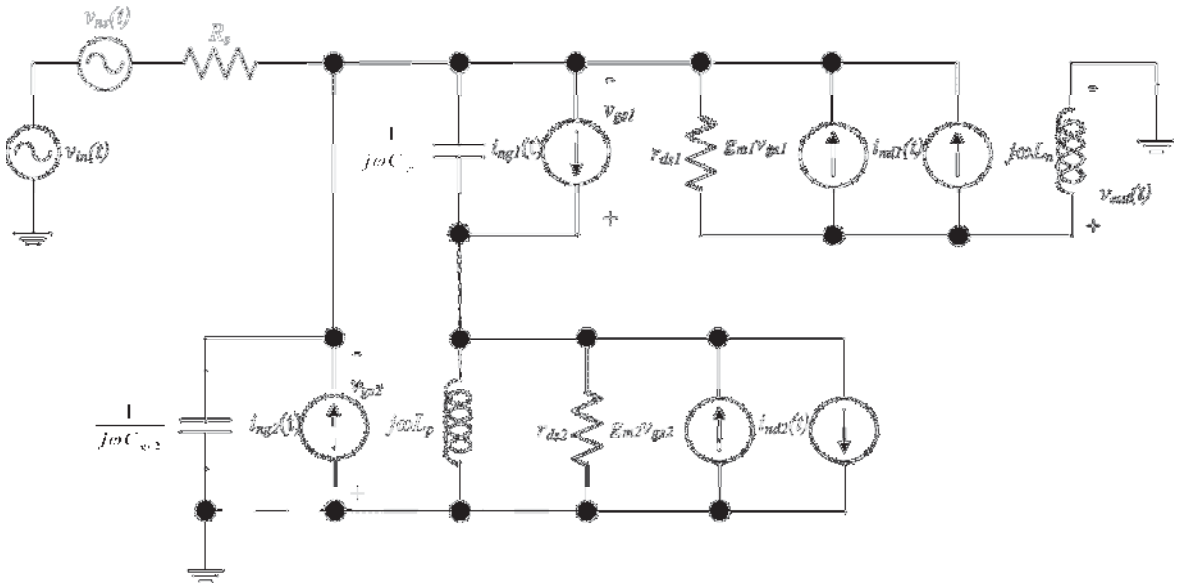

Fig. 4.4. Small signal equivalent representation of the proposed UWB LNA with relevant noise sources.

signal model of the LNA, it is clear that for in-band frequencies, the impedance looking into the gate of M_1, i.e., $\frac{1}{j\omega C_{gs1}}$ in series with R_S, is quite large, and it is in parallel with $(r_{ds2}\|jX_p(\omega))$, where, $X_p(\omega)=\omega L_p$. Hence, the g_m-boosting gain '$A(\omega)$' provided by M_2, when the impedance looking into its drain terminal is dominated by $(r_{ds2}\|jX_p)$, can be approximated by,

$$A(\omega) \approx -g_{m2}\{r_{ds2} \parallel jX_p(\omega)\} \tag{4-1}$$

With reactance $X_n(\omega)=\omega L_n$, the overall gain $A_O(\omega)$ of the proposed CG UWB LNA is then given by,

$$A_o(\omega) = \frac{\{1+(1+A)g_{m1}r_{ds1}\}.jX_n}{(R_s)\{1+(1+A)g_{m1}r_{ds1}+jB_1(r_{ds1}+jX_n)\}+(r_{ds1}+jX_n)} \tag{4-2}$$

In Fig. 4.4, $i_{nd1}(t)$ and $i_{nd2}(t)$ are the drain current noise sources of the devices M_1 and M_2 respectively, and, $i_{ng1}(t)$ and $i_{ng2}(t)$ are the corresponding gate current noise sources, while, $v_{ns}(t)$ is the noise generator for the source resistance R_s. A comprehensive analysis of

different types of noise in MOS devices and definitions of different noise parameters can be found in [34].

4.3.1 Noise Analysis of UWB LNA

Having established the form of the UWB LNA small signal model, the noise analysis is presented in this sub-section. If the input referred noise power spectral density (PSD) due to $v_{ns}(t)$ is represented as $S_{v_{ns}}$, the noise factor F is then given by,

$$F = 1 + \frac{S_{v_{irn1}} + S_{v_{irn2}}}{S_{v_{ns}}} \tag{4-3}$$

In (4-3), $S_{v_{irn1}}$ and $S_{v_{irn2}}$ are the input-referred noise PSDs due to the internal noise sources of M_1 and M_2, respectively. Now, by inspecting Fig. 4.4, it can be proven mathematically, that the input referred noise power spectral density (PSD) due to the internal noise sources of the device M_1 , is given by,

$$S_{v_{irn1}} = S_{i_{nd1}} \left[\frac{r_{ds1}^2}{\left\{1 + (1+A) g_{m1} r_{ds1}\right\}^2} \right] \left\{1 + R_s^2 \left(B_1 + B_{c1}\right)^2\right\} + S_{i_{ng1,u}} R_s^2 \tag{4-4}$$

Where, $S_{i_{nd1}}$ is the PSD of M_1's internal noise source $i_{nd1}(t)$, and $S_{i_{ng1,u}}$ is the PSD of the orthogonal component of $i_{ng1}(t)$ to $i_{nd1}(t)$ [34] and $B_1(\omega)$ is the effective susceptance looking into the gate terminal of M_1. In (4-4), the correlation admittance $B_{c1}(\omega)$ is included to account for the effect of correlation between the two noise sources of the device M_1. The correlation admittance $B_{c1}(\omega)$ for the CG stage in (4-4) found after some simple derivations, and is given by,

$$B_{c1}(\omega) = \frac{B_1(\omega)}{(1+A)} \left\{ \frac{1 + (1+A) g_{m1} r_{ds1}}{r_{ds1} g_{d01}} |c| \sqrt{\frac{\delta}{5\gamma}} \right\} \tag{4-5}$$

In (4-5), the correlation coefficient c, the constants γ and δ, and M_1's zero-bias channel conductance g_{d01} are technology and bias dependent parameters [24].

Calculation of input referred noise PSD $S_{v_{irn2}}$, due to the noise sources of the device M_2, as shown in Fig. 4.4, is done by dividing $i_{ng2}(t)$ into two orthogonal components: $i_{ng2,u}(t)$ (with PSD $S_{i_{ng2,u}}$) which is completely uncorrelated, and $i_{ng2,c}(t)$ (with PSD $S_{i_{ng2,c}}$)which is fully correlated and in phase with $i_{nd2}(t)$ (with PSD $S_{i_{nd2}}$) [34]. The input-referred noise PSD due to all the noise sources of M_2 can then be derived to be given by,

$$S_{v_{irn2}} = S_{i_{nd2}} \frac{\left[\{1+(1+A)g_{m1}r_{ds1}\}R_s + r_{ds1} - B_1R_sX_n\right]^2 + \left(X_n + B_1R_sr_{ds1}\right)^2}{g_{m2}^2\left(r_{ds1}^2 + X_n^2\right)} + S_{i_{ng2,c}}R_s^2$$
$$+ 2\sqrt{S_{i_{ng2,c}}S_{i_{nd2}}R_s^2 \frac{\left[\{1+(1+A)g_{m1}r_{ds1}\}R_s + r_{ds1} - B_1R_sX_n\right]^2 + \left(X_n + B_1R_sr_{ds1}\right)^2}{g_{m2}^2\left(r_{ds1}^2 + X_n^2\right)}} + S_{i_{ng2,u}}R_s^2 \quad (4\text{-}6)$$

In this composite PSD expression, the first term is contributed by the drain current noise of M_2, the second term by the correlated part of the induced gate current noise, the third term arises from the cross-correlation of these two noise sources, and the final term is the contribution of the uncorrelated induced gate current noise of M_2.

Inspecting (4-3) and (4-4), it is evident that the g_m-boosting by the factor (1+A) has increased the system SNR considerably. It can be proven that the casual matching BPF network at the input of the LNA can increase the SNR by setting $B_1(\omega)$=- $B_{c1}(\omega)$. This can be achieved by setting the reactive components of the BPF in accordance with the size of $B_1(\omega)$. Effect of the short-channel resistance can also be appreciated by analyzing (4-4). Reducing r_{ds1} can reduce the channel current noise without bound and theoretically at zero channel resistance, the channel current noise completely disappears. Practically, this is not feasible as r_{ds} cannot be technologically controlled to such a limiting value.

From (4-6), it is apparent that increasing the g_m-boosting gain $A(\omega)$ can increase the noise PSD due to M_2, resulting in a reduction of the system SNR, which is highly undesirable. It can be appreciated that the noise contribution by M_2 can be minimized by keeping high device transconductance, g_{m2}, as it appears in the denominator of two noise terms. However, an increase in g_{m2} would also increase the g_m-boosting gain $A(\omega)$ that can degrade the SNR due to M_2's noise sources. As a compromise, $A(\omega)$ can be kept within an

acceptable limit by maintaining low effective load ($r_{ds2}||jX_p$) at the drain terminal of M_2 while still designing for higher g_{m2}.

The total noise factor of the proposed g_m-boosted UWB CG LNA is then computed by substituting (4-4) and (4-6) into (4-3) and solving for F, which is then given by,

$$F = \frac{\gamma g_{d01}}{R_s}\left[\frac{r_{ds1}^2}{\{1+(1+A)g_{m1}r_{ds1}\}^2}\right]\{1+R_s^2(B_1+B_{c1})^2\}+\frac{\delta B_1^2 R_s}{5g_{d01}}+\frac{\gamma g_{d02}}{R_s}\beta^2+\frac{\delta B_2^2 R_s}{5g_{d02}}+2\beta B_2\sqrt{\frac{\delta\gamma}{5}} \quad (7)$$

Where $\beta(\omega)$ is a frequency dependent parameter of the dimension Ω (ohms) and is given by,

$$\beta(\omega)=\frac{1}{g_{m2}}\sqrt{\frac{[\{1+(1+A)g_{m1}r_{ds1}\}R_s+r_{ds1}-B_1R_sX_n]^2+(X_n+B_1R_sr_{ds1})^2}{(r_{ds1}^2+X_n^2)}} \quad (8)$$

In addition, γ and δ are assumed to be the same for M_1 and M_2 , while, g_{d01} and g_{d02} are zero-bias channel conductances for M_1 and M_2 respectively [24].

4.3.2 Input Matching and Noise

In the previous subsections, detailed noise analysis of the proposed UWB LNA was carried out. From (4-7), it can be seen that the g_m-boosting gain $A(\omega)$ has an inverse relationship with the input referred noise due to M_1, and, on the other hand, a direct relationship with the input referred noise due to M_2. It is now necessary to observe the effect of the short-channel finite resistance and the g_m-boosting gain $A(\omega)$ on the input matching characteristics of the proposed UWB LNA. Revisiting the small signal model of the LNA in Fig. 4.4, the frequency domain representation of the input admittance of the proposed circuit, as seen by the UWB source, is given by,

$$Y_{in}(\omega)=\frac{1+\{1+A(\omega)\}g_{m1}r_{ds1}}{r_{ds1}+jX_n(\omega)}+jB_1(\omega)+jB_2(\omega) \quad (4\text{-}9)$$

If $B_1(\omega)$ and $B_2(\omega)$ are relatively small and absorbed by the L_{s2}-C_{s2} shunt branch of the BPF at the source terminal of M_1, the admittance can be separated into its real and imaginary parts that are given by,

$$Y_{in}(\omega) = \frac{\{1+(1+A)g_{m1}r_{ds1}\}.r_{ds1}}{r_{ds1}^2 + X_n^2} - j\frac{\{1+(1+A)g_{m1}r_{ds1}\}.X_n}{r_{ds1}^2 + X_n^2} \quad (4\text{-}10)$$

The effect of the g_m-boosting can be appreciated from (4-10) where g_{m1} is increased by a factor $\{1+A(\omega)\}$ resulting in higher effective transconductance of M_1 and better input matching without the expense of more power supply drain. $Y_{in}(\omega)$ reduces to $(1+A)g_{m1}$ when long-channel assumption is made ($r_{ds1} \to \infty$) which is the published input admittance of long-channel g_m-boosted CG LNA[68]. It is clear from (4-10) that the imaginary part of $Y_{in}(\omega)$ represents a grounded inductor in parallel with the shunt branch of the BPF and can be absorbed into it. Due to the short-channel (finite r_{ds1}), the effect of the load at the drain of M_1 also appears at its source and causes a reduction in the input admittance of the CG stage (which is not desirable). It indicates a tradeoff between the gain of the LNA, its input matching and the power consumption. This is because, for higher gain a larger $X_n(\omega)$ would be required, which would force setting a higher value for g_{m1} (higher power dissipation), in order to bound the real part of $Y_{in}(\omega)$ for impedance matching to 50 ohms. Hence, the effective transcoductance of the short-channel CG stage should be set higher than 20mS for better input match.

As a concluding remark in this section with regard to design methodology, the g_m-boosting gain $A(\omega)$ must be set carefully so that the reduction in the drain current noise due to M_1 on the system SNR, is not offset by the deterioration of the input referred noise due to M_2 (comparing (4-4) and (4-6)). As discussed in the previous subsection, g_{m2} can be increased while maintaining low effective load at the drain of M_2, so as to keep the input referred noise component in the system SNR due to M_2 to a minimum.

4.4 UWB LNA Circuit Design and Simulation

The design of the proposed CMOS UWB LNA, as shown in Fig. 4.3, is based on the IBM 130nm RF CMOS process. For better performance at high frequencies and lower parasitics, a minimum channel length of 130nm is chosen for all the transistors in the circuit. The extensive circuit simulations, optimization and chip layout of the proposed design was carried out using *Cadence* tools. Following the analysis and the design methodology in section-4-3, g_{m1} and g_{m2} are set at 11.5mS and 10.5mS respectively. For these transconductance values, the widths of M_1 and M_2 are set at 25μm and 75μm respectively, that gives a reused bias current of around 1.25mA. The resulting approximate unity gain frequencies of f_{T1}=180 GHz (for M_1) and f_{T2}=55 GHz (for M_2) are more than 5 times the maximum frequency of the band of operation and hence provides sufficient intrinsic bandwidth for achieving the specified performance of the UWB LNA. After iterative simulations, keeping in view the tradeoffs explained in the previous section, L_n and L_p are designed as 11.7nH and 4.8nH inductors, respectively, to provide adequate UWB gain and noise performance. L_p in conjunction with g_{m2} gives a gain magnitude ($|A(\omega)|$) of around 1.33 peak at 4.2 GHz, which is chosen to be within the upper-half frequencies of the band of operation, through rigorous simulations to optimize the noise within the band. This makes the effective transconductance of M_1 around 27mS at this frequency. The effective transconductance is set higher than 20mS to take into account the effect of the short-channel finite resistance as per (4-10). As mentioned earlier, the UWB LNA gain and noise is optimized at a frequency, nearer to the upper cut-off frequency of the operating band with the realization that, at lower frequencies these can be compensated by the higher intrinsic gain of the devices. For the same reason, the resonant frequency of the L_t-C_t tank is chosen as 4.2 GHz using a 1.3nH inductor and a 1.1pF capacitor. For low power consumption, the DC supply voltage is kept at 1.0V and the gate terminals of M_1 and M_2 are biased at 500mV with the drain to source voltage drops for each of the MOS devices set at 500mV. The gate-bias voltages are generated by current mirror circuits so as to minimize power consumption. A source-follower is added as an output buffer to provide 50Ω output match for testing purposes. The external BPF components are chosen considering the presence and the absorption of the front-end (pad, bonding wire and

package) parasitic reactances including the inductive susceptance of the UWB LNA's input admittance, in order to provide better broadband input match with sharp out-of-band signal rejection. For effective BPF design, the *Cadence Spectre-RF* simulator is used to extract device operating parameters for both M_1 and M_2. The important extracted parameters were: C_{gs1}=9.5fF, C_{gs2}=30.1fF, r_{ds1}=932Ω and r_{ds2}=1250Ω. Fig. 4.5 shows the composite circuit topology of the RF signal input interconnect path showing a cascaded network of the input impedance of the UWB LNA, wire-bond, package parasitics, and the external band-pass filter. Here, $R_{in}(\omega)$ and $L_{in}(\omega)$ are the equivalent resistance and inductance at the source terminal of M_1 and are computed using (10). $C_{in}(\omega)$ is the equivalent capacitance at the source terminal of M_1 and is a parallel combination of $B_1(\omega)$, $B_2(\omega)$ and the bonding-pad capacitance (C_{pad}≈0.2pF). Here, as a trade-off the effective admittance at the input of the LNA is absorbed in the input matching network (*power-match*) instead of matching with the correlation admittance as per (4-4) and (4-5) (*noise-match*), which is compensated by the g_m-boosted lowering of the overall noise figure. The over-all input impedance of the amplifier in the operating band, is plotted using the smith-chart, as shown in Fig. 4.6. The smith chart trace depicts the variation of the impedance looking into the RF signal input interconnect path, indicating a close match with 50 Ω source resistance at 4.1 GHz and the amount of mismatch (radial distance from the origin to a point on the trace) at the other frequencies within the pass-band ranging between the corner frequencies (3.1 GHz at the bottom terminus of the trace and 4.8 GHz at the top terminus of the trace).

4.5 Fabrication and Experimental Results

The UWB LNA was fabricated using the IBM 130nm RF CMOS process. The photomicrograph of the fabricated die is shown in Fig. 4.7 with chip area of 640µm×325µm (0.208 sq. mm) excluding the bonding pads. All the on-chip active devices are fabricated with fingered gate terminals to reduce the gate-resistance so that the intrinsic f_T of the devices are maximized and their gate-resistance noise PSDs are minimized. All the on-chip inductors were fabricated as octagonal spirals with central cavity (for high Q) using 5um wide traces of top thick aluminum layer MA with copper layer E1 as underpass

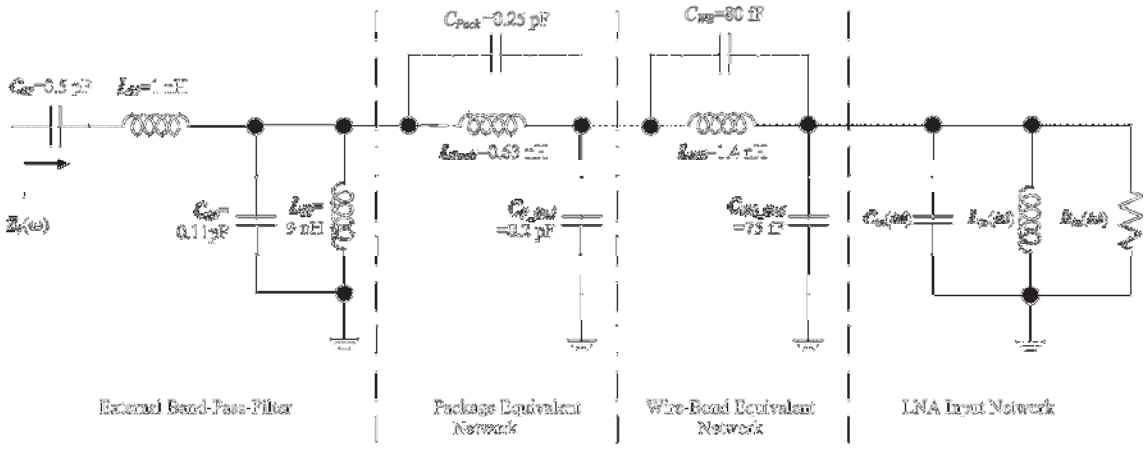

Fig. 4.5. Composite circuit topology of the RF signal input interconnect path showing a cascaded network of the input impedance of the UWB LNA, wire-bond, package and the external band-pass filter.

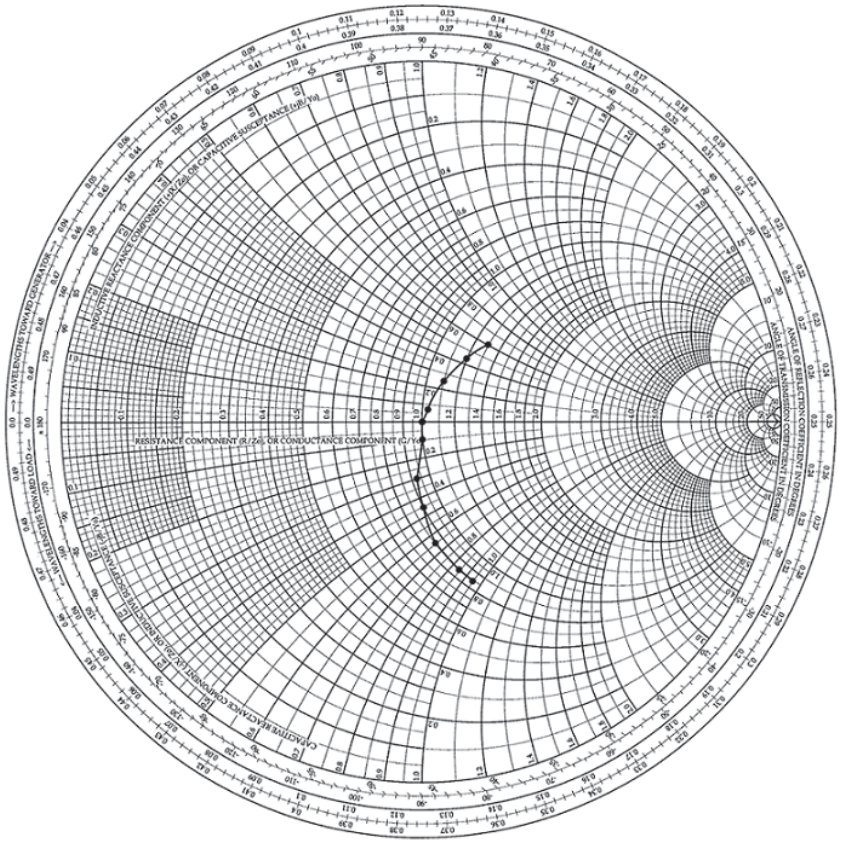

Fig. 4.6. A smith chart trace depicting the variation of the impedance looking into the RF signal input interconnect path, indicating a match with 50Ω source resistance at 4.1 GHz and the amount of mismatch (radial distance from the origin to the trace) at the corner frequencies (3.1GHz at the bottom terminus of the trace and 4.8 GHz at the top terminus of the trace).

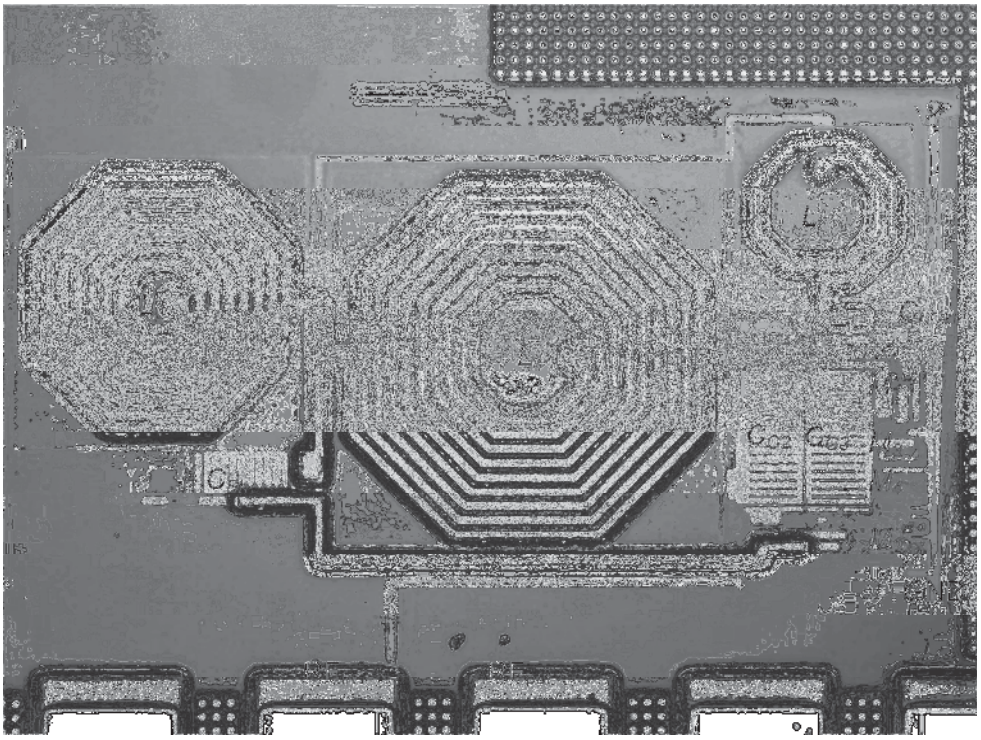

Fig. 4.7. Microphotograph of proposed LNA with labels showing all the active and passive components.

contact to the spiral center. The outer diameters of the on-chip inductors are respectively 250µm, 180µm and 100µm for L_n, L_p and L_t. The shunt capacitor C_{sh}, the bypass capacitors C_{G3} and C_{G2}, and the series tank capacitor C_t are fabricated as MIM capacitors using the thin metal layers QY and HY with thin dielectric aluminum nitride sandwiches, interconnected with the enclosing layers E1 and LY. All the resistors providing DC biasing, and, the current mirror and AC blocking terminations are fabricated using the high sheet resistance shallow p^+ poly layer. All the active and passive components are labeled on the chip photo. Transient and AC measurements were carried out using the Agilent DCA J 86100C and Agilent E4428C ESG signal generator. Network-level characterization was carried out by power wave measurements in the TDR/TDT mode [83]. All measurements include trace and connector losses. Fig. 4.8 shows the simulated and measured input reflection coefficient S_{11}. In the simulation phase, S_{11} is kept in the range <-10dB. The degradation in the measured result is mainly due to the presence of the CG input susceptances, bonding-pad parasitics, bonding wire, packaging traces, and the inaccuracies in the external BPF components. Despite these intervening terminations

causing signal reflection, the LNA S_{11} is below -8dB over the entire frequency band of operation which indicates reasonably acceptable input matching. The S_{11} plot is also found to be roughly close to its theoretical estimate in the smith chart of Fig. 4.6. Fig. 4.9 shows the forward power-gain curve and its comparison with the simulation. The forward-gain, S_{21}, is measured to be around 13dB with the dc power consumption of around 3.4 mW (which includes the power dissipation and the 6 dB gain loss at the source-follower output buffer). The gain is almost flat with some degradation at the upper UWB frequencies. This gain erosion is mainly due to the increase in the substrate leakage at higher frequencies. Fig. 4.10 presents the achieved noise figure for the proposed LNA. The measured noise figure of the LNA is below 4.5 dB in the pass-band with an NF_{min} of around 3.5 dB, which is acceptable for an UWB LNA [25], [81]. This noise performance is achieved in power-match condition and can be further optimized by designing the matching circuit for noise-match (setting B_1=- B_{c1}), as per (4). The g_m-boosting CS stage noise contribution can also be optimized by employing inductive source degeneration technique. Using this technique, with reducing the overall system noise, input matching characteristics of the LNA can be further enhanced, as the inductive degenerated CS stage would contribute a resistive component in parallel to the input impedance of the LNA given in (10). Figs. 4.11 and 4.12 show the remaining measured S-parameters and their comparison with the simulation. The LNA provides very good reverse isolation as the use of the CG topology removes the miller effect. Hence, the measured S_{12} is less than -40dB within the pass-band. The reverse isolation deteriorates at higher frequencies due to increased parasitic feed back at higher frequencies. The measured S_{12} is higher than the simulated value due to the effect of the additional stray feedback paths not accounted for by the parasitic extraction simulator. The measured output matching coefficient S_{22} is less than -14dB throughout the operating band and is almost constant largely due to the broadband behavior of the output impedance of the output source-follower buffer. In order to determine the spurious free dynamic range ceiling, the IIP3 and the 1-dB compression point were evaluated. Accordingly, a two-tone test was carried out at the mid-band frequency of 3.9 GHz with a 500MHz tone separation. The measurements indicate an input-referred IP3 of -6.1 dBm and an input-referred 1-dB compression point (ICP_{1dB}) of -15.4dBm, as shown in the Fig. 4.13. Finally, Table I summarizes the measured performance of the proposed current-reuse g_m-boosting CG UWB LNA and provides a comparison of the circuit with recently reported designs. The

improvements attained by the proposed current-reuse g_m-boosted architecture is clearly evident when compared to these other UWB LNA circuits.

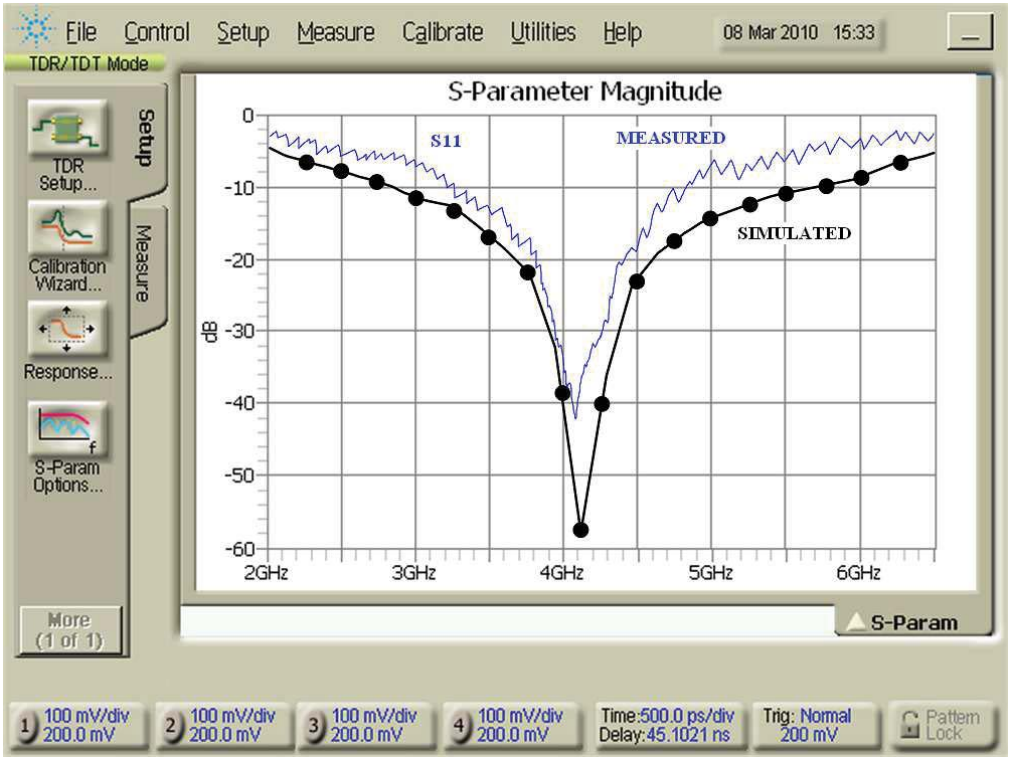

Fig. 4.8. The input reflection coefficient (S_{11}).

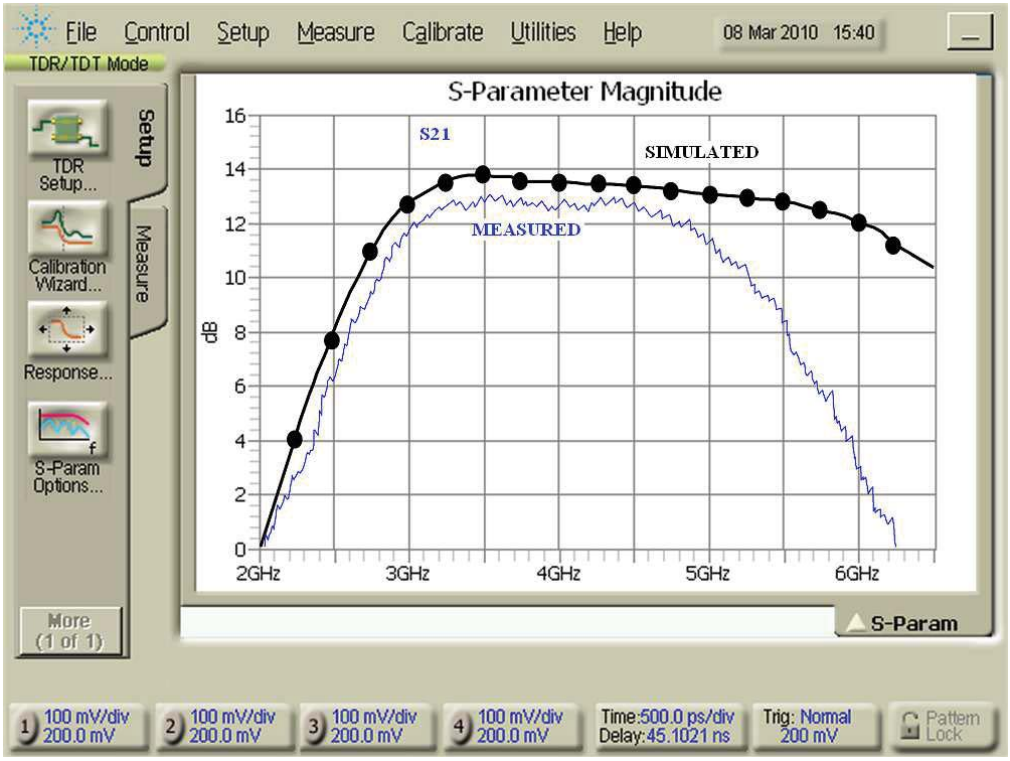

Fig. 4.9. The forward gain (S_{21}).

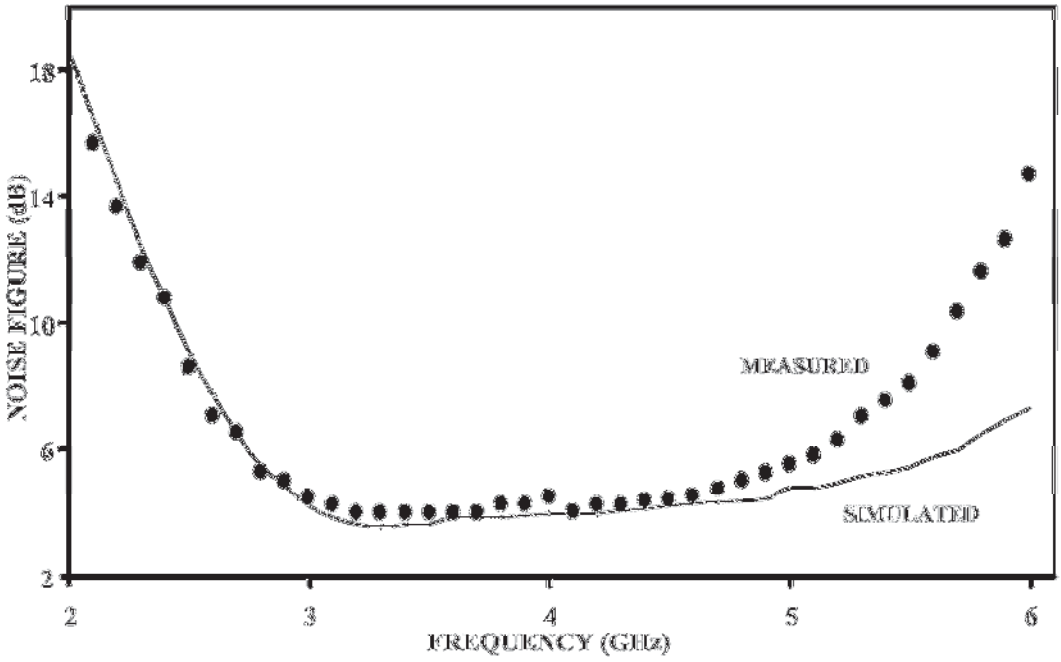

Fig. 4.10. The noise figure (NF).

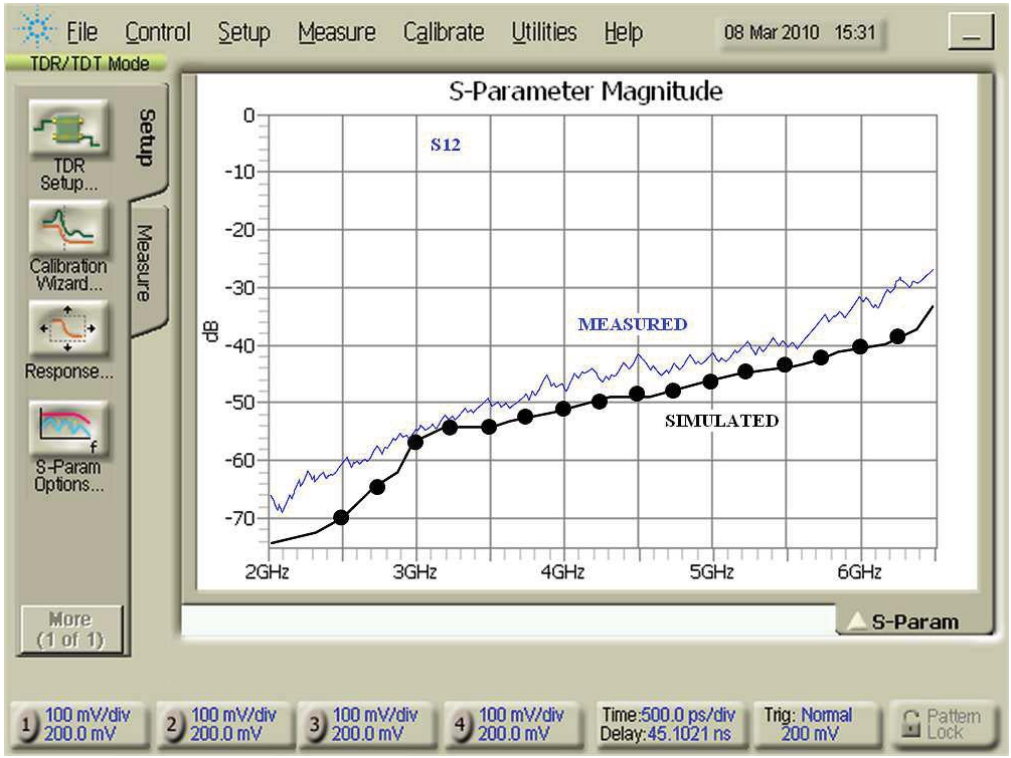

Fig. 4.11. The reverse isolation (S_{12}).

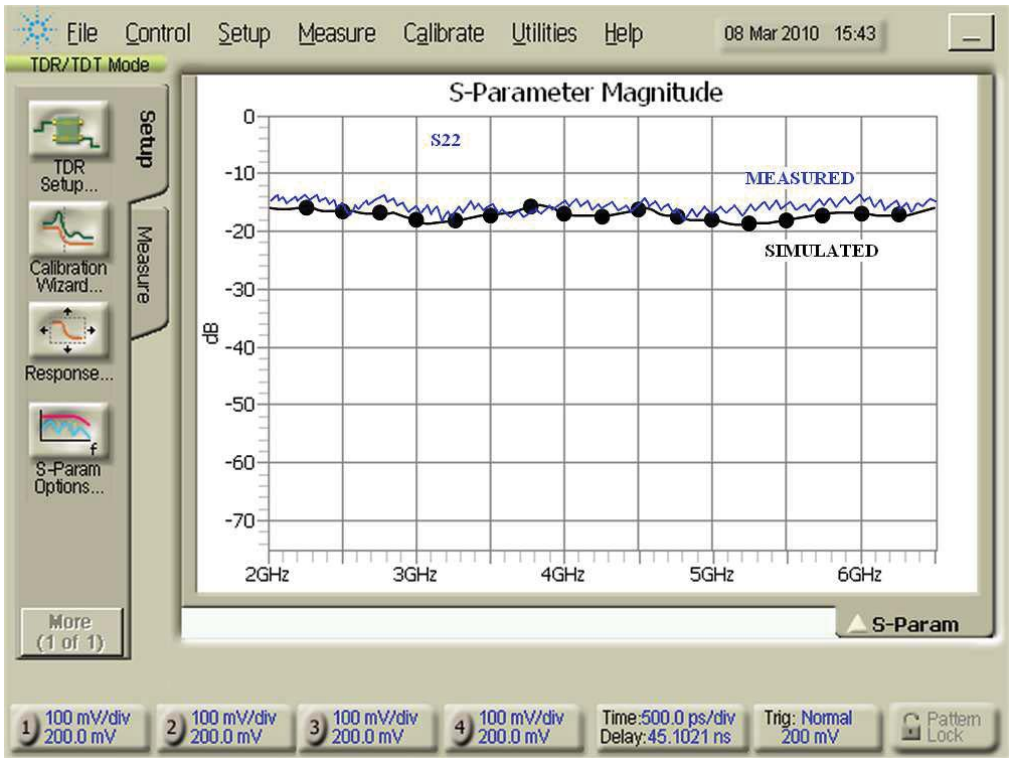

Fig. 4.12. The output reflection coefficient (S_{22}).

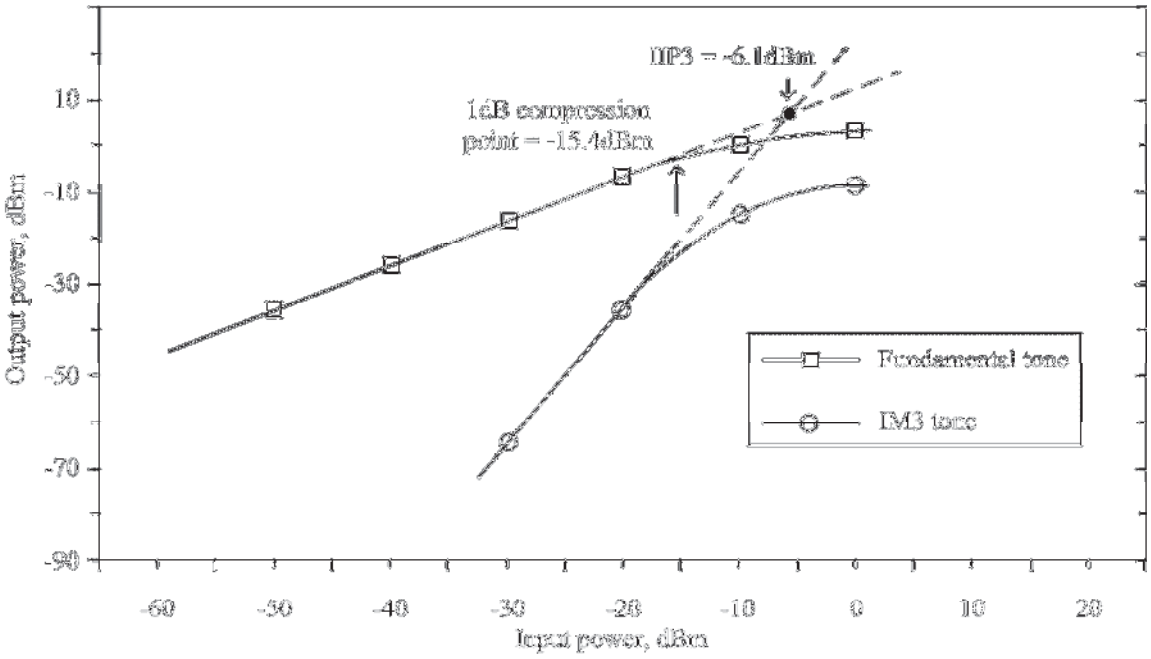

Fig. 4.13. The IIP3 and 1dB compression point for the UWB LNA at 3.9 GHz.

TABLE I. Summary of the power matched g_m-boosted CG UWB LNA performance, and comparison with previous recently published designs.

	This work	[83]	[92]	[60]#%	[95]	[87]*%
Technology (nm)	130	180	180	45	180	130
Year	2010	2010	2010	2009	2008	2006
$Bandwidth_{3\text{-}dB}$ (GHz)	3.1-4.8	3.4-11	3-4.8	2.5-9.6	3.1-4.8	2-4.6
Input return loss S_{11}(dB)	<-8	<-10	<-10	<-15	<-10	<-10
Reverse isolation S_{12}(dB)	<-40	<-65	N/A	N/A	N/A	N/A
Forward gain S_{21} (dB)	13	14	15	12.5	13.9	9.5
Output return loss S_{22}(dB)	<-14	N/A	N/A	N/A	<-8.2	N/A
Minimum noise figure, NF_{min} (dB)	3.5	4.7	3.5	5.5	4.68	3.5
Power dissipation P_{diss} (mW)	3.4	30	5.0	5.3	14.6	16.5
Supply voltage (V)	1.0	2.5	1.8	1.2	1.8	1.5
Chip-area (mm^2)	0.4^	1.11	0.76	0.441	0.945	1.08
I/R compression point ICP_{1dB} (dBm)	-15.4	-14.5	-18.0	N/A	N/A	-6.0
I/R third order intercept point IIP_3 (dBm)	-6.1	-5.3	N/A	N/A	0.12	-0.8
#: Simulation only %: Differential *: CS input stage N/A: Not available I/R: Input referred ^: Estimated, including bonding pads and external filter						

4.6 Conclusion

This chapter demonstrated the design of low power LNA architecture, operating in the 3.1-4.8 GHz UWB range, fabricated using the IBM 130nm CMOS process. Here, a new approach is presented to boost the g_m ("*piggyback* g_m-boosting") of the CG LNA by adopting a current-reuse technique to reduce the power dissipation by sharing the bias current between the g_m-boosting gain and the UWB signal amplifying stages. The system's expressions for the LNA to represent and optimize the noise factor have been derived.

Various design tradeoffs between the g_m-boosting gain, input matching, gain of the amplifying stage and noise contributions by the active devices constituting the complete g_m-boosted CG UWB LNA are also explained and analyzed. Measured results show satisfactory performance of the proposed LNA with a power consumption of only 3.4 mW. This technique thus provides an avenue for achieving broadband low noise performance using the CG topology.

In the next chapter, the same technique with the enhancements of the differential structure, the series peaking bandwidth extension and noise matching input filter is demonstrated. The UWB LNA presented in the next chapter operates in 3.1-10.6 GHz (full-band) range and designed to achieve optimal noise performance following the technique presented in Chapter 3. The new differential UWB LNA design investigated in the next chapter is accepted for publication as mentioned in [97] and its manuscript is included in the 'Appendices' section of this thesis.

CHAPTER 5

DESIGN, FABRICATION AND TESTING OF NOISE MATCHED UWB LNA FOR 3.1-10.6 GHz

5.1 Introduction

In the previous chapter, a single-ended (SE) ultra-wideband (UWB) low noise amplifier (LNA) architecture is proposed that utilizes a new variation of the current-reuse technique to reduce the power consumption and operates in 3-5 GHz frequency band. The g_m-boosting technique is employed to minimize the noise figure (NF) of the proposed SE LNA while wideband power match is achieved by using an off-chip input band pass filter. In this chapter, an improved version of the current-reuse g_m-boosted CG UWB LNA is investigated where the matching network at the input of the CG stage is configured following the noise optimization methodology presented in Chapter 3. The UWB LNA design, presented in this chapter employs inductive series peaking technique to widen the operating bandwidth up to 10.6 GHz.

The availability of the unlicensed spectrum between 3.1-10.6 GHz for UWB wireless communication has been a great source of interest for the academic and the industrial researchers for almost a decade. Advancements in the cost effective RF CMOS system-on-chip (SOC) circuit design has also pushed the designers to utilize the features of this state-of-the-art technology to realize the UWB circuits. In a WiMedia UWB frontend, the LNA, preferably operating in the full 3.1-10.6 GHz spectrum, is critical to the on-the-whole system performance. Being the first subsystem in the RF signal receiving chain, the signal at the input of the LNA is of the order of a few micro volts. Besides providing adequate power gain and inducing minimum noise, the LNA should provide good input matching characteristic to the UWB antenna. Many studies of the RF CMOS circuits have been reported in the published literature with good results [78]-[84]. Commonly used techniques to extend the bandwidth of the CMOS LNAs to the UWB range are the inductive peaking techniques and the distributed amplifier (DA) topology [32]. Both of

these techniques use a number of onchip spiral inductors for bandwidth extension but later topology dissipates more power due to its distributed nature. Recently, inductorless wideband CMOS LNAs gained interest due to their smaller chip area [17]. Resistive feedback technique is used in some of the inductorless designs to extend the bandwidth which requires large input transconductance to acquire enough forward power gain and low NF. In these designs, large input transconductance usually results in high power consumption. In [32], the concept of resistive feedback is employed with use of one small onchip spiral inductor and achieved good results with smaller chip area.

The input stage of the UWB LNA is critical to achieve low noise performance with almost flat forward power gain and input matching over the entire extent of the UWB frequencies. The well-known common source (CS) and the common gate (CG) topologies are rigorously employed by the designers to serve the purpose of an UWB LNA input stage. Studies show that the later topology exhibits better wideband matching, frequency independent NF and better reverse isolation among the two [27], [42]. The Q factor of this topology ($Q_{CG} = \frac{\omega R_s C_{gs}}{2}$) is directly proportional to the gate-to-source capacitance C_{gs}, opposite to the CS LNA topology (with $Q_{CS} = \frac{1}{2\omega R_s C_{gs}}$) which has inverse relationship. With technology scaling (as the C_{gs} is reducing), the Q reduces and hence the bandwidth of the circuit increases. The CG topology, as shown in Fig. 5.1(a), has an inherent capability to absorb the parasitic capacitances associated with the CG device. As the C_{gs}, the source-to-bulk capacitance C_{sb} and the pad capacitance C_{pad} can be easily absorbed into the parallel input RLC tank. Sharp out-of-band roll-off is required for the UWB LNA to reject the nearby out-of-band RF signals including GSM-1800/1900, Bluetooth and 802.11b/g. This can be achieved by using a multi-order passive band pass filter (BPF) at the input of the UWB LNA. Several designs of the CG UWB LNA with matching BPF at the input have been published [80], [83]. The NF of the CG LNA is dominated by the noisy channel conductance in the signal path. It is strongly coupled with the DC operating point and the power match to the signal source (R_s). Transconductance 'g_m' boosting, shown in Fig. 5.1(b), is a reported technique to decouple the NF of the CG LNA from the mentioned entities. This technique provides better input matching and signal-to-noise ratio (SNR) with lower power consumption as compared to a traditional CG LNA [68].

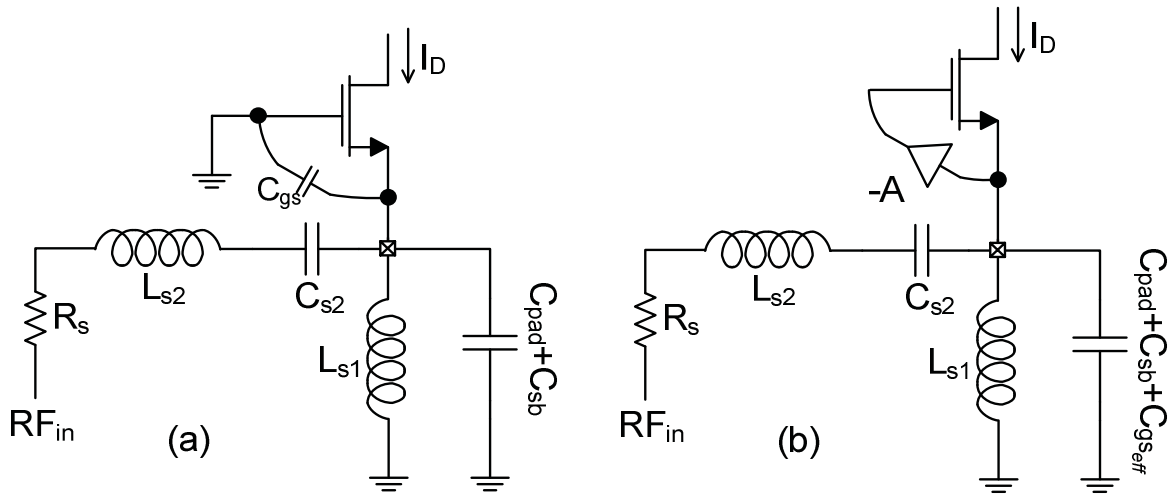

Fig. 5.1. (a) CG UWB LNA and (b) CG UWB LNA with g_m-boosting.

In Chapter 3 of this thesis, a new noise optimization technique for the g_m-boosted CG UWB LNA is presented. It is a suitable option to practically implement the noise matching network to minimize the in-system noise contributed by the g_m-boosted CG input device. This UWB LNA design technique to realize optimal noise matching network is also published in [85]. In this chapter, a two-stage fully-differential noise matched g_m-boosted CMOS UWB LNA is presented encompassing the whole of the UWB spectrum from 3.1-10.6GHz. The proposed full-band UWB LNA employs the noise optimization technique presented in Chapter 3. The 1st stage of the LNA utilizes an onchip passive network for wideband noise match. It comprises of a differential current-reuse g_m-boosted CG structure where the g_m-boosting gain is provided by a current sharing differential CS active structure to reduce the power consumption. The 2nd stage comprises of a differential common drain device with inductive peaking to enhance the bandwidth of the LNA and provides wideband output matching to the test load.

This chapter is organized as follows. The section 5.2 describes the conceptual circuit diagram of the proposed two-stage UWB LNA with the help of its small signal model. In the same section, the noise model of the conceptual circuit is derived to optimize the noise performance of the proposed UWB LNA. The next two sections encompass the design of the differential UWB LNA including the optimal noise matching network. Here, different design tradeoffs are also discussed related to the noise matched and the power matched conditions. In section 5.5, the chip layout and the measurement results are presented and

compared with recently published research works. Conclusions are drawn in section 5.6 of this chapter. With regard to the mathematical notations used in the derivations and expressions in this chapter (analogous to the previous two chapters), the frequency domain entities are represented by capital letters (e.g., $Z(\omega)$) and the corresponding time domain entities are represented by respective lower case letters (e.g., $z(t)$). Sometimes, the terms ω and t are omitted from the expressions for clarity and are understood to be present.

5.2 Proposed g_m-boosted CG UWB LNA

The conceptual circuit diagram of the proposed noise matched g_m-boosted series peaked CG UWB LNA topology is depicted in Fig. 5.2(a). The LNA circuit comprises of two cascaded stages. The input RF voltage is applied to the first stage of the LNA which is further divided into three basic components: a passive noise matching network at the input, a CG device M_1 with an inductor L_n as the inductive load and a g_m-boosting amplifier. The g_m-boosting amplifier is an active device M_2, proposed to be a traditional CS stage providing frequency dependent inverting gain of magnitude $A(\omega)$. The g_m-boosting amplifier circuit diagram is depicted in Fig. 5.2(b). The capacitive input susceptance of the g_m-boosting amplifier is given by $B_2(\omega)=\omega C_{gs2}$ and its output impedance is denoted by $Z_A(\omega)$. The amplified UWB RF signal at the drain terminal of M_1, is then fed through the large coupling capacitor C_{G3}, to the second cascaded stage of the LNA. The second stage contributes in extending the bandwidth of the UWB LNA to the required upper corner frequency. The series peaking inductor L_{ser}, in combination with the nMOS device M_3 (common drain configuration) constitutes a buffer stage to extend the bandwidth and match to the test load. In the conceptual circuit, I_{D1}, I_{D2}, and I_{D3} are the frequency independent DC current sources exhibiting infinite ouput impedances. A large resistor R_{G1} is added to block the AC signal and set the DC bias point of M_1 in combination with the bias voltage V_{B1}. Similar to this manner, R_{G3} is used to set the DC bias point of M_3. Moreover, C_{sh} is acting as the AC shunt capacitor that is large enough to sink the AC current to the global circuit ground.

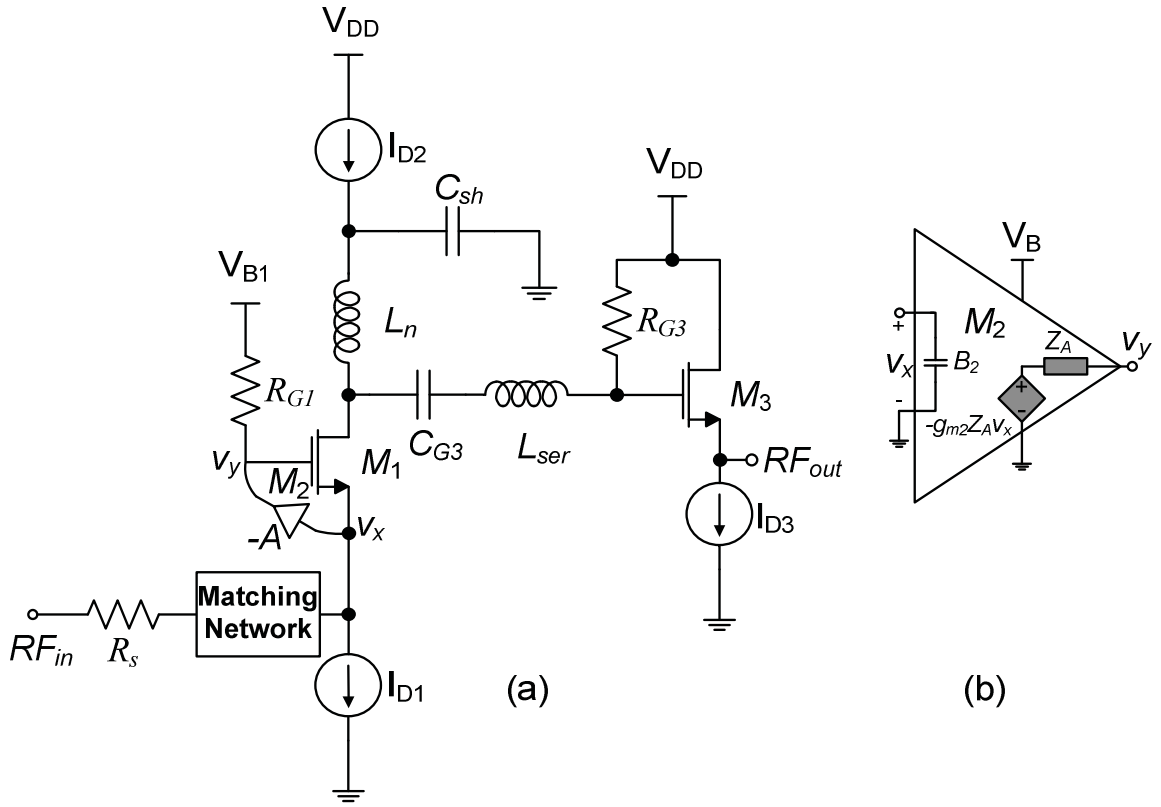

Fig. 5.2. (a) Conceptual circuit diagram of the proposed noise matched searies-peaked g_m-boosted CG UWB LNA, and (b) the CS g_m-boosting amplifier.

5.2.1 Small Signal Model of the proposed LNA

The noise matched small signal model corresponding to the circuit shown in Fig. 5.2(a), is diagrammed in Fig. 5.3 indicating the relevant noise sources and the elements of the noise matching network. '$v_{in}(t)$' is assumed to be purely resistive UWB signal source with output resistance R_s, exhibiting constant power within the operating band and zero out of it. The noise matching network is divided into a series reactance $X_a(\omega)$ and a susceptance $B_b(\omega)$ parallel to the CG MOS input, and are assumed to be noiseless. In the equivalent small signal model, the g_m-boosting amplifier is represented as a combination of a CS stage M_2 and the inductor L_p connected as the load, which results in $Z_A(\omega)=(r_{ds2}\|j\omega L_p)$. C_{gs1} and C_{gs2} are the gate-to-source capacitances of M_1 and M_2, respectively, and $v_{gs1}(t)$ and $v_{gs2}(t)$ are the gate-to-source small signal voltages of the corresponding devices. To study the effect of the finite short-channel resistance due to the very small MOS dimensions, the corresponding short-channel resistances r_{ds1} and r_{ds2} are included in the small signal model. The effect of the source-to-bulk voltages is ignored for the ease of understanding.

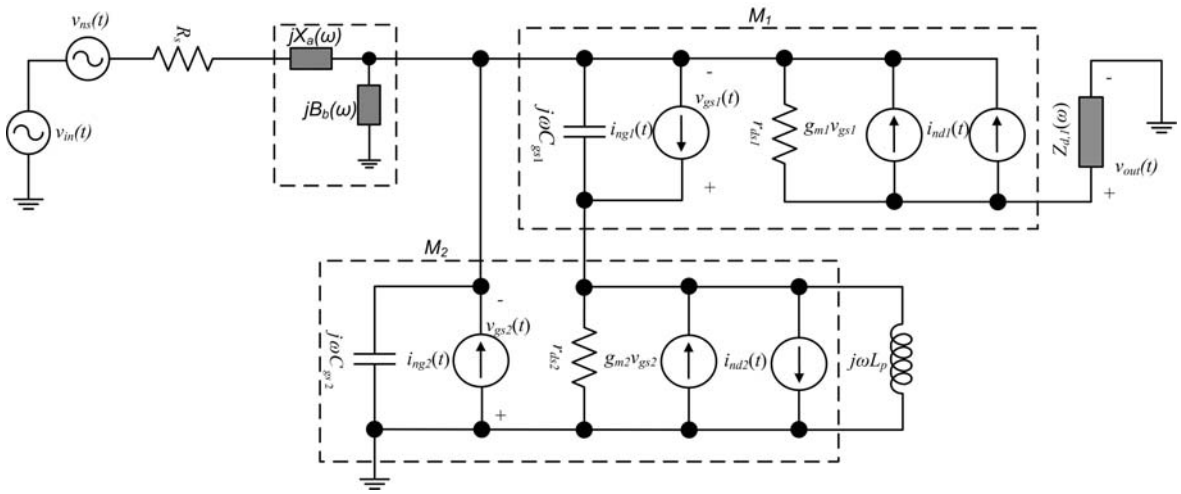

Fig. 5.3. Small signal model of the proposed g_m-boosted CG UWB LNA with the passive noise matching network.

g_{m1} and g_{m2} are the transconductances of M_1 and M_2 respectively and C_{sh} is replaced by a short circuit for simplicity of the analysis. It should be noted that M_1 and M_2 are not noiseless and the respective noise sources of the active devices are also considered while examining the noise performance of the proposed circuit. The sources, $i_{nd1}(t)$ and $i_{nd2}(t)$, represent the root-mean-square (RMS) channel thermal noise current for the devices M_1 and M_2 respectively. $i_{ng1}(t)$ and $i_{ng2}(t)$ denote the corresponding RMS gate current noise sources. While $v_{ns}(t)$ is the voltage source representing the RMS white-noise generator for the resistance R_s. A detailed investigation of the origins of different types of noise in the MOS transistor and definitions of the noise parameters can be found in [24], [67], [85].

As the 2nd stage in cascade with the g_m-boosted CG stage of the proposed UWB LNA is acting as a wideband source-follower, within the operating frequency band, its voltage gain is close to unity. Therefore, the voltage gain of the proposed LNA is found out at the drain terminal of the 1st stage (the CG stage) which is given by,

$$A_v(\omega) = \frac{\{1 + (1 + A)g_{m1}r_{ds1}\}.Z_{d,1}}{(R_s + jX_a)\{1 + (1 + A)g_{m1}r_{ds1} + jB_{in}(r_{ds1} + Z_{d,1})\} + (r_{ds1} + Z_{d,1})} \tag{5-1}$$

Here, $B_{in}(\omega)$ is the effective susceptance at the source terminal of M_1 and given by,

$$B_{in}(\omega) = B_b(\omega) + [1 + A(\omega)]B_1(\omega) + B_2(\omega) \tag{5-2}$$

$A(\omega)$ and the equivalent impedance at the drain terminals of M_1 and M_2, denoted by $Z_{d,1}(\omega)$ and $Z_{d,2}(\omega)$ respectively, are given by following equations:

$$A(\omega) = -g_{m2} Z_{d,2}(\omega) \tag{5-3}$$

$$Z_{d,1}(\omega) = j\omega L_n \,\|\left[j\omega L_{ser} + \frac{1}{j\omega C_{G3}} + \frac{1}{j\omega C_{gs3}} + \frac{g_{m3} R_L}{j\omega C_{gs3}} + R_L \right] \tag{5-4}$$

$$Z_{d,2}(\omega) = Z_A \,\|\left[\frac{1}{jB_1} + \left\{ \frac{(R_s + jX_a)}{1 + (Y_{in} + jB_b + jB_2)(R_s + jX_a)} \right\} \right] \tag{5-5}$$

In (5-4), g_{m3} is the device transconductance and C_{gs3} is the gate-to-source capacitance for the transistor M_3, and R_L denotes the load at the output of the LNA. In (5-5), $Y_{in}(\omega)$ is the input admittance looking into the source terminal of M_1, excluding the gate-to-source susceptance $B_1(\omega)=\omega C_{gs1}$ of the CG device. $B_2(\omega)=\omega C_{gs2}$ is the gate-to-source susceptance of the CS device M_2. Here, the term within the brackets is dominated by $\frac{1}{jB_1(\omega)}$ due to the smaller size of the MOS devices and being $B_1(\omega)$ very small, (5-5) is dominated by $Z_A(\omega)$ (the output impedance of the g_m-boosting amplifier).

5.2.2 System Model of the LNA and Noise Analysis

Following the analysis, presented in Chapter 3, after making suitable modifications and adding the effect of the noisy g_m-boosting CS amplifier, the system model of the proposed noise matched g_m-boosted series peaked CG UWB LNA is derived. In the system model shown in Fig. 5.4, $i_{ng_u}(t)$ and $\kappa(\omega)$ (a dimensionless complex frequency dependent entity) are given by,

$$i_{ng_u}(t) = i_{ng1_u}(t) + i_{ng2_u}(t) \tag{5-6}$$

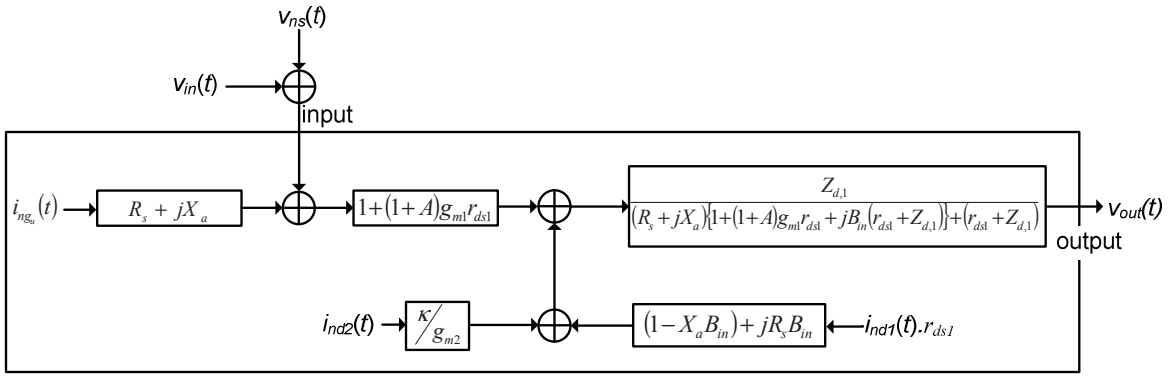

Fig. 5.4. System model of the proposed UWB LNA.

$$\kappa(\omega) = (g_{m1}r_{ds1}A)\left[\frac{(R_s + jX_a)\{1 + (1 + A)g_{m1}r_{ds1} + jB_{in}(r_{ds1} + Z_{d,1})\} + (r_{ds1} + Z_{d,1})}{r_{ds1} + Z_{d,1}}\right] \tag{5-7}$$

In (5-6), $i_{ng1_u}(t)$ and $i_{ng2_u}(t)$ are the uncorrelated components of $i_{ng1}(t)$ and $i_{ng2}(t)$ with $i_{nd1}(t)$ and $i_{nd2}(t)$, respectively.

Looking at the derived system model, it is evident that the SNR degradation caused by $i_{ng_u}(t)$ remains unaffected by the g_m-boosting gain. Contrary to the inverse relationship between the g_m-boosting by a factor of (1+A) and the noise contribution to the SNR by $i_{nd1}(t)$; the input referred noise voltage due to $i_{nd2}(t)$ has a direct relation with (1+A). This correlation between $i_{nd1}(t)$ and $i_{nd2}(t)$ must be carefully examined to optimize the SNR of the system.

Referring back to the noise factor derivations, performed in Chapter 3, from 3-18, 3-28 and 3-29, the noise factor F of the proposed g_m-boosted CG UWB LNA is given by,

$$F = \frac{\int_{-\infty}^{\infty} \frac{|P(\omega)|^2}{S_{v_{ns}}(\omega)} d\omega}{\int_{-\infty}^{\infty} \frac{|P(\omega)|^2}{S_{v_{ns}}(\omega) + S_{v_{irg_u}}(\omega) + S_{v_{irn1}}(\omega) + S_{v_{irn2}}(\omega)} d\omega} \tag{5-8}$$

Where, $S_{v_{ns}}$ is the noise power spectral density (PSD) due to $v_{ns}(t)$ and, $S_{v_{irg_u}}$, $S_{v_{irn1}}$ and $S_{v_{irn2}}$ are the input referred noise voltage PSDs due to $i_{ng_u}(t)$, $i_{nd1}(t)$ and $i_{nd2}(t)$, respectively. In (5-8), $|P(\omega)|^2$ represents the received UWB signal power at the input of the LNA.

By inspecting Fig. 5.3 and Fig. 5.4, it can be proven that the input referred noise PSDs due to the internal noise sources of M_1 and M_2 are given by following equations:

$$S_{v_{irg_u}} = \left(R_s^2 + X_a^2\right) \times S_{i_{ng_u}} \tag{5-9}$$

$$S_{v_{irn1}} = S_{ind1}\left[\frac{r_{ds1}^2}{\left\{1+(1+A)g_{m1}r_{ds1}\right\}^2}\right]\left[\left\{1 - X_a\left(B_{in}+B_{c1}\right)\right\}^2 + R_s^2\left(B_{in}+B_{c1}\right)^2\right] \tag{5-10}$$

$$S_{v_{irn2}} = S_{ind2}\frac{\left|\kappa_c\right|^2}{g_{m2}^2} + 2\frac{R_s\left|\kappa_c\right|}{g_{m2}}\sqrt{S_{ing2_c}S_{ind2}} \tag{5-11}$$

In (5-9), $S_{i_{ng_u}}$ is the noise current PSD of the composite of the uncorrelated gate current noise sources ($i_{ng_u}(t)$) as defined in (5-6). S_{ind1} and S_{ind2}, in (5-10) and (5-11), are the corresponding noise current PSDs of $i_{nd1}(t)$ and $i_{nd2}(t)$, respectively. S_{ing2_c} is the noise current PSD of $i_{ng2_c}(t)$ which is the inphase and correlated component of $i_{ng2}(t)$ to $i_{nd2}(t)$. While calculating $S_{v_{irn1}}$; the correlation admittance $B_{c1}(\omega)$, is added to $B_{in}(\omega)$ to take into account the effect of correlation between the gate current noise and the channel thermal noise sources of M_1. Similarly, the effect of correlation between the internal noise sources of M_2 is also modeled while calculating $S_{v_{irn2}}$. The 2nd term in (5-11) appears due to the correlation between the two internal noise current sources of M_2.

The correlation admittance, $B_{c1}(\omega)$, for the g_m-boosted CG stage (M_1 in this case) is derived in Chapter 3 and given by [85],

$$B_{c1}(\omega) = B_1(\omega)\left\{\frac{1+(1+A)g_{m1}r_{ds1}}{r_{ds1}g_{d01}}\left|c_1\right|\sqrt{\frac{\delta_1}{5\gamma_1}}\right\} \tag{5-12}$$

In the above equation, the noise constants γ_1 and δ_1, the correlation coefficient c_1 and the channel conductance (at zero drain-to-source bias voltage) g_{d01} for the device M_1 are the technology and bias dependent parameters [85].

5.2.3 Optimal Noise Matching Network Design

To find the optimal values, $X_{a,opt}(\omega)$ and $B_{b,opt}(\omega)$, for noise matching, (5-8) is partially differentiated, keeping the assumptions that $S_{ind1}(\omega) \approx S_{ind2}(\omega)$ and $g_{m1} \approx g_{m2}$, for obtaining a meaningful result. After setting the differentiation result to zero and simultaneously solving the equations, two sets of optimal results are obtained. When minimizing the gate current noise of the g_m-boosted CG stage is the design goal as it is not affected by the g_m-boosting gain which mainly reduces the drain current noise considerably, the optimal values are given by,

$$X_{a,opt}(\omega) = 0 \tag{5-13}$$

$$B_{b,opt}(\omega) = -B_{c1}(\omega) - \left[\{1 + A(\omega)\}B_1(\omega) + B_2(\omega)\right] \tag{5-14}$$

This result is useful at high frequencies when the gate current noise increases quadratically as compared to the drain current noise which is constant with respect to the operating frequency. In the second case, when the noise minimization as a whole is the main design goal, then the optimal solution is given by,

$$X_{a,opt}(\omega) = \pm\sqrt{R_s(\omega)\left(\sqrt{1/\pi(\omega)} - R_s(\omega)\right)} \tag{5-15}$$

$$B_{b,opt}(\omega) = \pm\sqrt{\frac{\pi(\omega)}{R_s(\omega)}\left(\sqrt{1/\pi(\omega)} - R_s(\omega)\right)} - B_c(\omega) - \left[\{1 + A(\omega)\}B_1(\omega) + B_2(\omega)\right] \tag{5-16}$$

Where, the parameter $\pi(\omega)$ with the dimensions of $\left(\frac{1}{\Omega^2}\right)$ is given by,

$$\pi(\omega) = \frac{1}{2} \times \left[\frac{S_{ing_u}(\omega)}{S_{ind1}(\omega) \times \dfrac{r_{ds}^2}{\{1 + (1 + A)g_m r_{ds}\}^2}} + \left\{ \frac{1 + (1 + A)g_{m1} r_{ds1}}{r_{ds1} + Z_{d,1}} \right\}^2 \right] \tag{5-17}$$

The optimal values of the noise matching network components, derived in this subsection in the presence of a noisy g_m-boosting amplifier, are consistent with the results obtained in Chapter 3, with the exception of $\pi(\omega)$ as given in (5-17).

Revisiting the system model of the UWB LNA in Fig. 5.4, it is noted that the equivalent gate current noise PSD $S_{i_{ngu}}$, can be the dominant noise component in the combined noise power when referred to the input of the LNA. Due to the technology scaling and shrinking channel length, smaller r_{ds1} values and the g_m-boosting gain $A(\omega)$ yields reduced $S_{v_{irn1}}$; and $S_{v_{irn2}}$ can be reduced by setting a higher g_{m2}. From (5-9), it is clear that $S_{i_{ngu}}$ is not effected by the g_m-boosting gain or the smaller channel length. It can only be minimized by choosing the appropriate noise matching network. In this situation, it is quite evident that the solution depicted in (5-13) and (5-14) is appropriate in this case. The noise factor of the proposed g_m-boosted UWB CG LNA is then computed by substituting (5-13) and (5-14) into (5-8) and solving for optimal noise factor, F_{opt}, which is then given by,

$$F_{opt} = \frac{1}{\int_{\infty} \frac{1}{1+\frac{\gamma_1 g_{d01}}{R_s}\left[\frac{r_{ds1}^2}{\{1+(1+A)g_{m1}r_{ds1}\}^2}\right]+\frac{\delta_1 B_1^2 R_s\left(1-|c|^2\right)}{5g_{d01}}+\frac{\delta_2 B_2^2 R_s}{5g_{d02}}+\frac{\gamma_2 g_{d02}}{R_s}|\beta|^2+2|\beta||c|B_2\sqrt{\frac{\delta_2\gamma_2}{5}}}\left\{\frac{|P(\omega)|^2}{P_T}\right\}d\omega} \tag{5-18}$$

In (5-18), $P_T=\int|P(\omega)|^2 d(\omega)$ and $\beta(\omega)$ is a frequency dependent parameter of the dimension Ω (ohms) and is given by,

$$\beta(\omega) = \frac{g_{m1} r_{ds1} A}{g_{m2}}\left[\frac{\{1+(1+A)g_{m1}r_{ds1}\}R_s + r_{ds1} + R_{d,1} + jX_{d,1}}{\{1+(1+A)g_{m1}r_{ds1}\}(r_{ds1} + R_{d,1} + jX_{d,1})}\right] \tag{5-19}$$

In the above equation, $R_{d,1}(\omega)$ and $X_{d,1}(\omega)$, respectively, represents the real and imaginary parts of $Z_{d,1}(\omega)$. In addition, γ_1 and δ_1 for M_1 and, γ_2 and δ_2 for M_1, are bias dependent noise parameters. Similarly, g_{d01} and g_{d02} are the zero-bias channel conductances for the respective MOS devices.

5.3 Differential UWB LNA Design and Simulation

To illustrate the full-band noise matching network design approach presented in this chapter, a fully-differential noise matched series peaked CG UWB LNA with the active g_m-boosting technique is considered and diagrammed in Fig. 5.5. A Fully-differential topology is adopted to minimize the effects of parasitic ground inductance and process variations. An important attribute of the differential configuration is its rejection to the common-mode (CM) noise in the presence of the noisy supply and substrate voltages. This is a normal case in a mixed signal design. Specially, in the case of WiMedia UWB communication, where the local oscillator (LO) is needed to '*hop*' over multiple bands and the CM switching noise is generated during the band transition [86]. Besides, the differential LNA can be directly interfaced with the onchip differential UWB mixer when integrated on a single chip transceiver.

In this section of the chapter, the design approach is discussed with the help of the half circuit of the proposed UWB LNA. The UWB LNA is designed using IBM 130nm RF CMOS process. For low parasitics, reducing noise of the CG input stage by exploiting the smaller drain-to-source resistance, a minimum channel length of 130nm was chosen for all the circuit transistors. Rigorous simulations and optimization of the proposed design and extraction of the small signal device parameters were carried out using *Cadence Spectre*.

5.3.1 Half circuit of the Differential UWB LNA

In Fig. 5.6, the half circuit of the proposed differential series peaked CG UWB LNA is shown. It is noted that the half circuit of the UWB LNA is the equivalent practical circuit of the proposed CG UWB LNA architecture presented in Fig. 5.2. Here, the nMOS transistor M_1 with the drain inductor L_n constitutes the g_m-boosted CG stage. The pMOS transistor M_2 in combination with the load inductor L_p provides the g_m-boosting gain between the source and the drain terminals of M_1. To minimize the power dissipation, current-reuse technique is employed by stacking up the CG nMOS and the CS pMOS amplifiers. A large capacitor C_{sh} provides the ac ground and decouples both amplifiers at the in-band frequencies. The source terminal of M_1 is coupled to the gate terminal of M_2 through the large capacitor C_{G2}. The drain terminal of M_2 is shorted to the gate terminal of M_1 to complete the g_m-boosting loop and supply the gate bias voltage (diode-connected

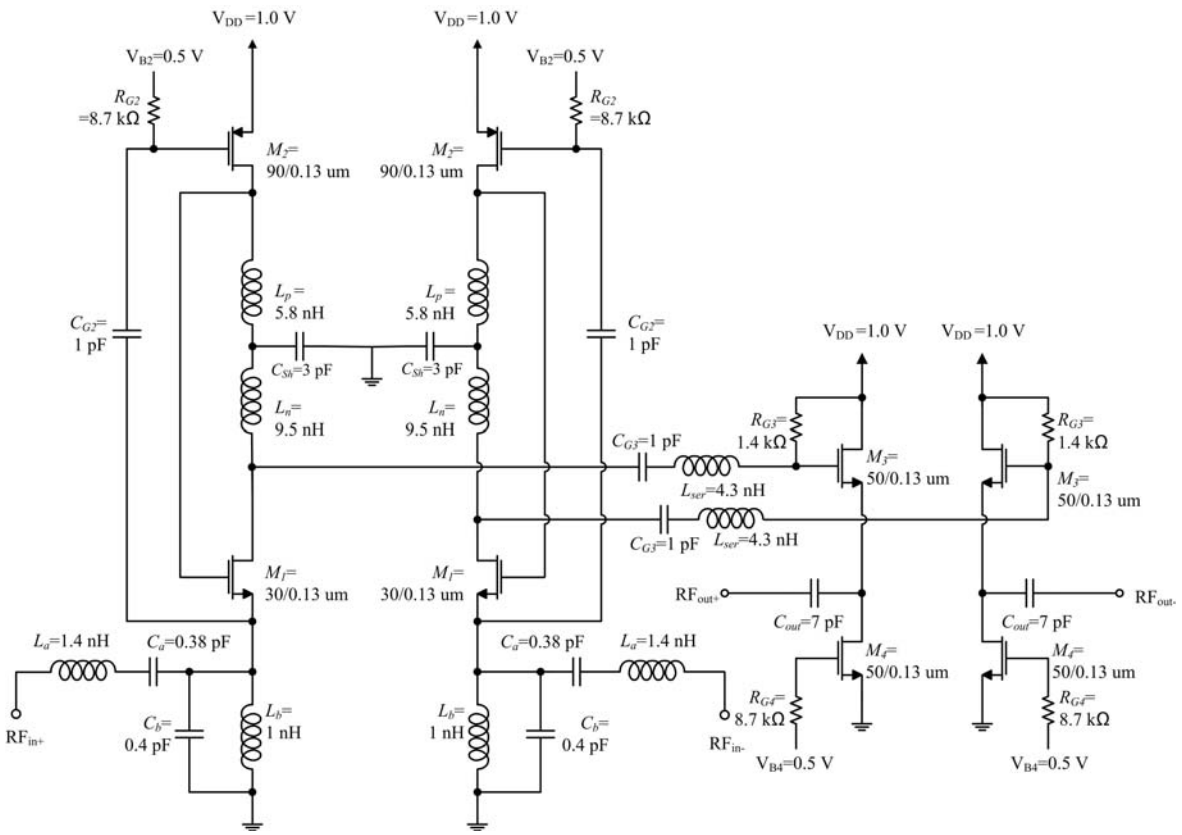

Fig. 5.5. Fully-differential series peaked CG UWB LNA with current-reuse g_m-boosting CS amplifier and 2nd order noise matching network.

configuration). The UWB RF signal is applied at the source terminal of M_1 through an intervening second order passive noise matching network. The reactance $X_a(\omega)$ of the noise matching network is constituted by a series LC tank, comprising of the inductor L_a and the capacitor C_a. The susceptance $B_b(\omega)$ of the noise matching network at the source terminal of M_1 is implemented as a parallel LC tank, comprising of the inductor and the capacitor L_b and C_b, respectively. The inductor L_b also shunts the shared DC bias current of M_1 and M_2 to the circuit ground. To broaden the operating bandwidth of the UWB LNA, a series peaking inductor L_{ser} is connected between the drain terminal of M_1 and the output buffer comprising the common drain device M_3 and the current source device M_4.

In accordance with the design methodology, presented in section 5.2, g_{m1} and g_{m2} are set as 7.6mS and 7.5mS. The corresponding channel widths to achieve these g_m values are set at 15 um and 53 um, for M_1 and M_2, respectively. After numerous simulations, L_n and L_p are designed as 9.5 nH and 5.8 nH, respectively. To set the DC operating point of the MOS devices, with V_{DD}=1.0 V DC, the gate terminal of M_2 is biased at 0.5 V which

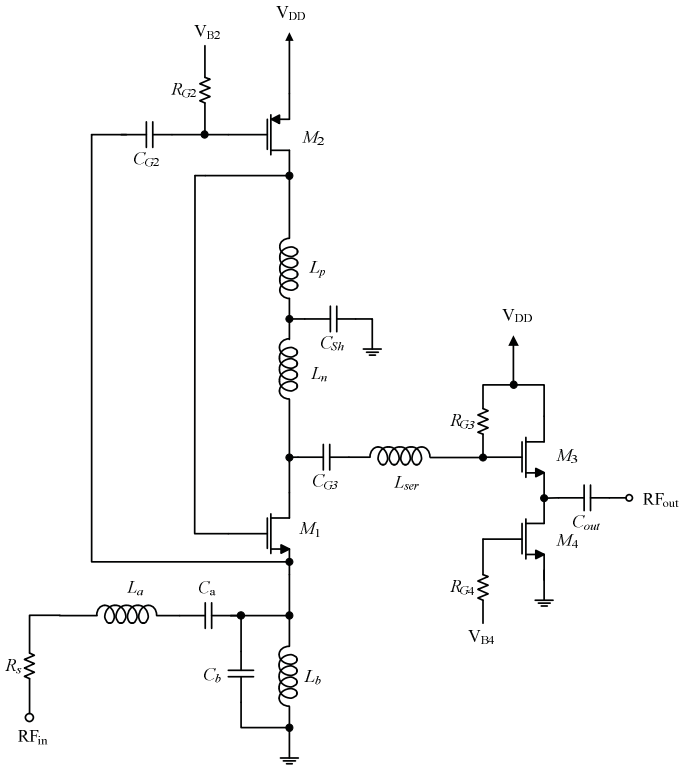

Fig. 5.6. Half circuit of the proposed noise matched g_m-boosted CG UWB LNA.

sets the drain-to-source voltage drop at 0.5 V for both of the devices. To enhance the bandwidth of the LNA, the series peaking inductor L_{ser} is sized to be 4.3 nH. M_3 and M_4 devices are sized at 50 um each to provide 50 Ω match to the test equipment, where, M_3 is biased through R_{G3}=1.4 kΩ, pulled-up to V_{DD} and the current source device M_4 is biased at the gate voltage of 0.5 V. To minimize the power consumption, the bias voltages for the devices M_2 and M_4 are generated through the current mirror circuits with large series resistances R_{G2} and R_{G4} of 8.7 kΩ that serve the purpose of blocking the ac signal.

5.3.2 Noise Match and SNR Degradation due to the g_m-Boosting Amplifier

In a traditional CG LNA, the input matching characteristic is very closely coupled with its noise factor. The circuit noise, which is dominated by the channel thermal noise current of the CG device, is inversely proportional to its transconductance (g_m). For power match, $1/g_m$ should be matched to the source resistance R_s and hence can not be controlled independently. Using the g_m-boosted CG LNA design technique with the noiseless g_m-boosting amplifier, this relationship between the power and the noise match can be decoupled. As a result, considerable noise reduction can be achieved by setting appropriate

g_m-boosting gain.. In the presence of a noisy g_m-boosting amplifier (in the proposed LNA circuit), $A(\omega)$ imply quite different implementation aspects.

As in (5-10), input referred drain current noise PSD of M_1 can be considerably reduced by increasing $A(\omega)$. On the other hand, the terms related to the noisy g_m-boosting amplifier in (5-11) are in direct relation with $A(\omega)$. In this scenario, the g_m-boosting gain should be set taking into account the increase in the input referred PSD due to the g_m-boosting amplifier drain current noise. The reduction in the noise factor due to the g_m-boosted CG stage must not be offset by the deterioration in the SNR due to the g_m-boosting CS stage. By inspecting (5-11), for a given value of $A(\omega)$, g_{m2} can be increased keeping low effective load at the CS drain terminal to keep the SNR degradation caused by M_2 to be a minimum.

5.4 Noise Optimization of the Proposed UWB CG LNA

As in long-channel devices ($r_{ds}\rightarrow\infty$), the input admittance at the source terminal of the g_m-boosted CG device is multiplied by $\{1+A(\omega)\}$, resulting in higher effective transconductance without the expense of more power dissipation. While considering the short-channel MOS device, the effect of the finite channel resistance should also be explored. After taking into account the effect of the g_m-boosting and the finite drain-to-source resistance, the resultant admittance looking into the source terminal of M_1 is given by,

$$Y_{in}(\omega)=\frac{\{1+(1+A)g_{m1}r_{ds1}\}(r_{ds1}-X_{d,1})}{(r_{ds1}-X_{d,1})^2+R_{d,1}^2}-j\frac{\{1+(1+A)g_{m1}r_{ds1}\}(R_{d,1})}{(r_{ds1}-X_{d,1})^2+R_{d,1}^2}+j(1+A)B_1 \qquad (5\text{-}20)$$

The first term in (5-20) shows the increase in the transconductance of M_1 by a factor of $\{1+A(\omega)\}$ as a result of the g_m-boosting technique. The second term represents a grounded inductor and should be taken into account while designing the noise matching network. The effect of smaller channel resistance can also be seen in (5-20) as the load at the drain terminal of M_1 affects the source admittance and causes the reduction in the effective transconductance.

Fig. 5.7 depicts the RF input interconnect path showing cascaded network of the

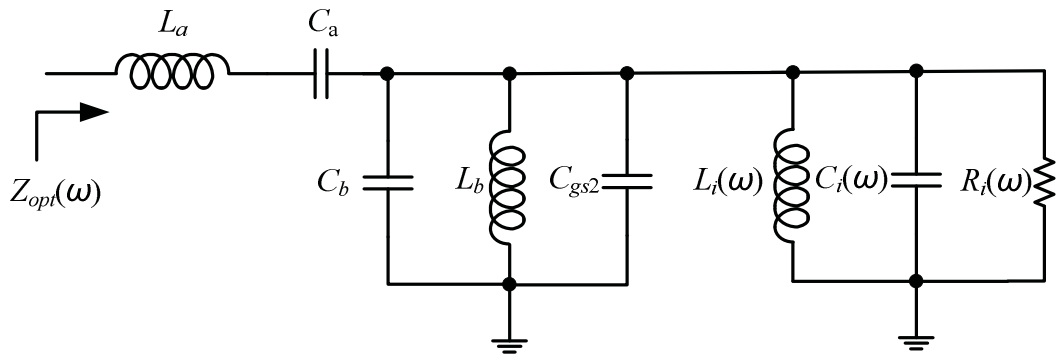

Fig. 5.7. Equivalent RF interconnect path at the input of the proposed UWB LNA.

noise matching network and the input admittance at the source terminal of the single-ended CG UWB LNA (half circuit). Here, $C_i(\omega)$ is the effective gate-to-source capacitance of the device M_1. $R_i(\omega)$ and $L_i(\omega)$ are the equivalent resistance and inductance looking into the source terminal of M_1 and can be computed using (5-20). The parallel grounded inductor $L_i(\omega)$ can effect the noise matching characteristics of the UWB LNA and must be absorbed into the shunt branch of the noise matching network.

Using 130 nm IBM RF CMOS technology, at the DC operating point of the circuit (V_{gs}=V_{ds}= 0.5 V and the details mentioned in the previous subsection), the device parameters were extracted using *Cadence*. The extracted parameters for M_1 are given as: g_{m1}=7.6mS, r_{ds1}=1.4 kΩ, C_{gs1}=6 fF and g_{d01}=11 mS. For M_2, the extracted parameters are: g_{m2}=7.5mS, r_{ds2}=1.7 kΩ and C_{gs2}=23 fF and g_{d02}=18 mS. Under these circuit conditions, the CS stage provides an average gain magnitude of 1.5 within the operating band. The noise parameters γ, δ and c are assumed to be same for both of the MOS devices and are chosen to be 2/3, 4/3 and j0.395, respectively [85]. To achieve better noise performance throughout the UWB frequency band in the presence of the noisy CS g_m-boosting amplifier, the matching network is optimized at the center frequency ω_{opt} of 6.85 GHz. The design of the matching network to optimize the circuit noise, using the technique presented in this chapter, is elaborated in the next subsection.

5.4.1 Realizing Matching Network Components

The input referred noise voltage PSD $S_{v_{irg_u}}$ is a foremost part in the degradation of the SNR in the presence of the g_m-boosting gain and the finite channel length of the CG device. In this case, the solution depicted in (5-13) represents a short circuit and

implemented as a 2nd order series LC tank as shown in Fig. 5.7. Where, the inductive and capacitive reactances of L_a and C_a cancel out each other within the operating band. At ω_{opt}, the series branch of the matching network is implemented by selecting L_a=1.4 nH and C_a=0.38 pF. From (5-14), $B_{b,opt}(\omega)$ can be realized as a grounded parallel network of noiseless passive components connected to the source terminal of M_1. The parallel circuit network at the source terminal of M_1 is a combination of the inductive and capacitive reactances as shown in Fig. 5.7. It is noted that these entities do not cancel each other (which is the case of power match) but results in an over-all inductive reactance (as per 5-14). It is also noted that the load reactance that appears at the source terminal of M_1 due to the finite r_{ds1}, denoted by L_i (ω) should be absorbed into the parallel LC tank circuit (L_b-C_b) for optimized noise performance. Keeping in view these limitations, the system model of the LNA is reproduced in *MATLAB* and (at $|A(\omega)|_{av}$=1.5) $|B_{b,opt}(\omega)|$ is found corresponding to the extracted parameters. Using the numerical iterative search technique to minimize (5-8), L_b and C_b are calculated as 1 nH and 0.4 pF, respectively at ω_{opt}. Here, the use of 2nd order LC tank circuits to implement the noise matching network should be appreciated. If the 1st order inductive circuit structure (an inductor) to realize $B_b(\omega)$ would be used, its size could be very large in the presence of very small gate-to-source capacitances of M_1 and M_2. Using a parallel capacitor C_b considerably reduces the size of the inductor L_b. Besides making the onchip implementation feasible, it results in lower parasitic series resistance and reduced loss due to the substrate leakage.

It should be noted that the matching network at the input of the proposed UWB LNA is designed to maximize the over-all SNR of the system. In this connection, the matching network is designed to be inductive in nature following (5-13) and (5-14). In this case, a compromise is made with regard to larger input reflection coefficient. This shows the tradeoff between the noise match and power match conditions for the proposed UWB LNA. To show this tradeoff, the over-all input impedance of the amplifier within the operating band, is plotted in Fig. 5.8 using the smith chart. The Smith chart depicts the degradation of the power match characteristics at the frequencies nearer to the cutoff frequencies of the pass-band due to the band pass nature of the noise matching network. This mismatch can be avoided if the antenna is placed in close proximity of the input trace of the UWB LNA.

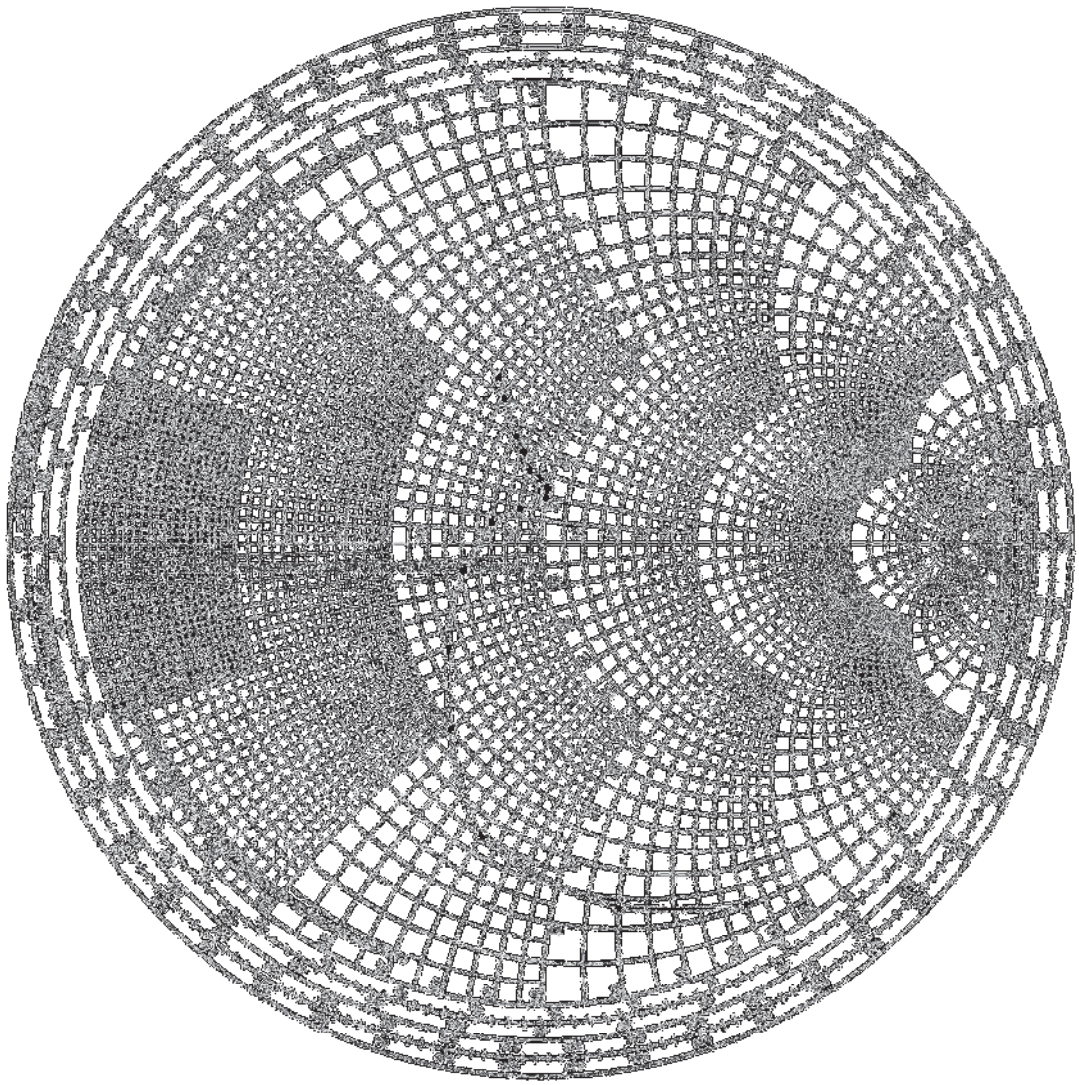

Fig. 5.8. Smith chart trace depicting the variation in the input impedance of the proposed UWB LNA within the operating band.

5.5 Fabrication and Experimental Results

The chip micrograph of the fully-differential fabricated die including the wafer probe pads is shown in Fig. 5.9 with chip area of 1.25mm×0.8mm (1 sq. mm). The die was fabricated in a 130nm IBM RF CMOS process. Using the DC power supply of 1V, based on the analysis presented in the previous sections, the sizes of transistors M_1 and M_2 were chosen to be 15 um and 53 um, respectively. At the minimum channel length of 130nm, these device sizes yielded a bias current of 1mA flowing through the 1st stage of the proposed UWB LNA. Both of the buffer stage devices M_3 and M_4 were sized at 50 um

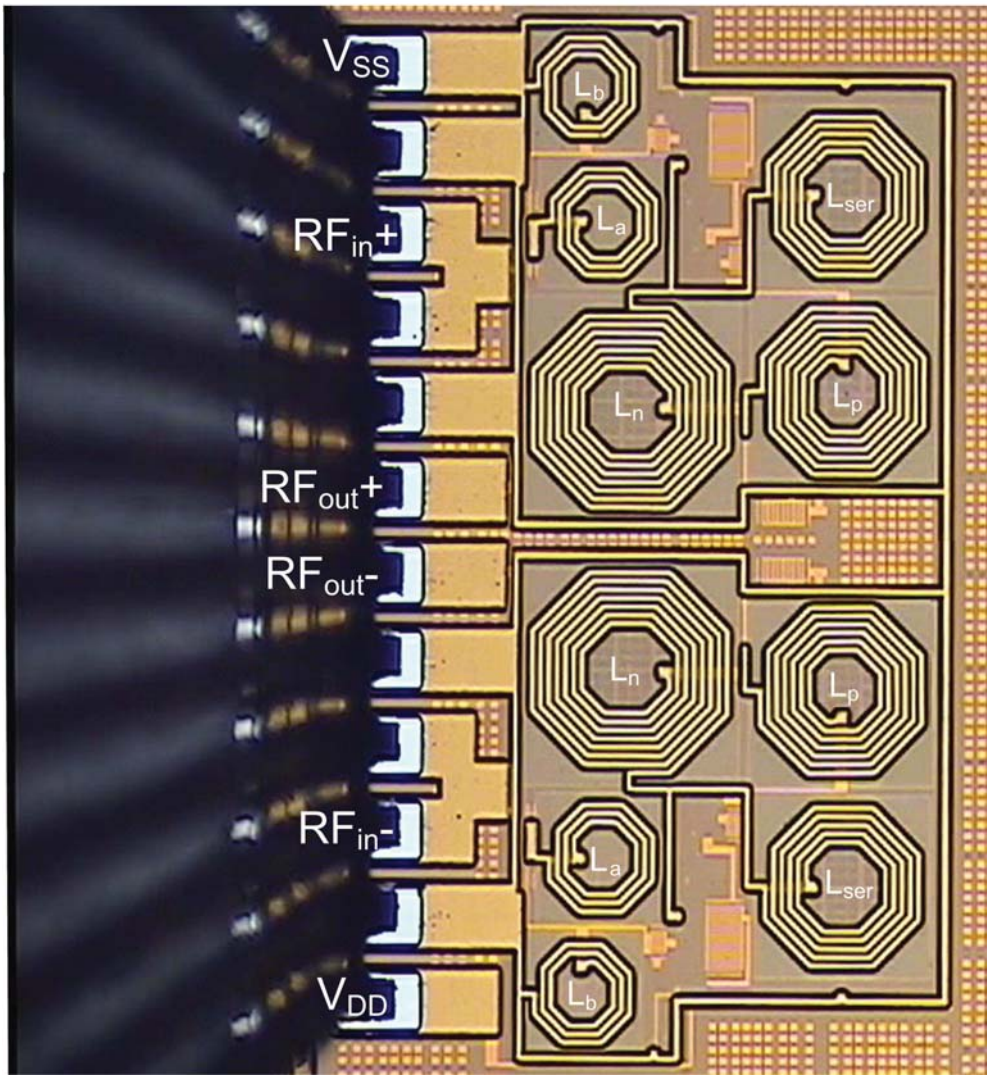

Fig. 5.9. Chip micrograph of the fabricated differential UWB g_m-boosted CG LNA showing the RF test probe touched down onto the probe pads.

with a bias current of 2.5mA to match to the 50Ω load for testing purposes. To maximize the intrinsic f_T of the onchip MOS devices and minimize their thermal gate-resistance noise PSDs, fingered poly-silicon gate terminals were laid out. All the reactive devices in the circuit were implemented as onchip spiral inductors using 5 um wide traces of top thick aluminum layer MA with copper layer E1 as underpass contact to the spiral center. The outer diameters of the inductors associated with the noise matching network, L_a and L_b, were sized as 130 um and 120 um, respectively. Where as the outer diameters of L_n, L_p and L_{ser} were set as 240 um, 200 um and 190 um, respectively. The bottom most metal layer M1 was used underneath the inductors as the ground shield to minimize the current

leakage and mutual inductance among these devices. All the capacitors in the circuit of the UWB CG LNA were fabricated as MIM capacitors using the thin metal layers QY and HY with thin dielectric aluminum nitride sandwiches. Thick metal layers E1 and LY were used to connect to the parallel plates of the MIM capacitors formed by QY and HY layers. The onchip resistive devices providing DC biasing and AC blocking terminations were laid out using the high sheet resistance shallow p^+ poly layer. M1 layer was used as the contact to the poly resistor terminals. To minimize the interconnect losses, thick metal layers MA, E1 and LY were used to lay out the interconnection lines. Transient and AC measurements were carried out using the Agilent DCA J 86100C and Agilent E4428C ESG signal generator. Network-level characterization was carried out by power wave measurements in the TDR/TDT mode [83], [96]. Wafer probing station from *Cascade Microtech* was used to probe the die using *Cascade Microtech* 12-pin *Unity Probe*. For this purpose, probe pads measuring 100 um × 70 um with 100 um pitch (micrometer distance between the center of the two adjacent probe pads) were placed on the die. Fig. 5.10 shows the measured and simulated forward power gain (S_{21}) under operating conditions of V_{DD}=1V and DC current consumption of 7mA. The proposed UWB LNA exhibited S_{21} of 14.5 dB in the pass-band with NF varying between 4.5 dB and 5 dB. The NF of the UWB LNA is diagrammed in Fig. 5.11. Fig. 5.12 exhibits the simulated and measured input reflection coefficient (S_{11}) which is less than -10 dB on frequencies between 4.5 GHz and 10.6 GHz but deteriorates at lower frequencies with worst case S_{11} of -8 dB. These measurements conform to the power matching characteristics of the proposed LNA diagrammed using the Smith chart in Fig. 5.8. The reverse power gain (S_{12}) is measured as less than -35 dB throughout the operating band and shown in Fig. 5.13. The two-tone test measurement was carried out at the center frequency of 6.85 GHz and the results are plotted in Fig. 5.14 showing the input-referred 1 dB compression point (ICP_{1dB}) of 12.1 dBm and input-referred 3rd order intercept point (IIP3) of -4.8 dBm.

The proposed UWB LNA exhibited adequately flat gain and acceptable input/output return losses with low NF within the whole operating UWB band. It also showed good linearity characteristics and low power dissipation. Table II compares the proposed LNA performance with some recently published UWB LNAs.

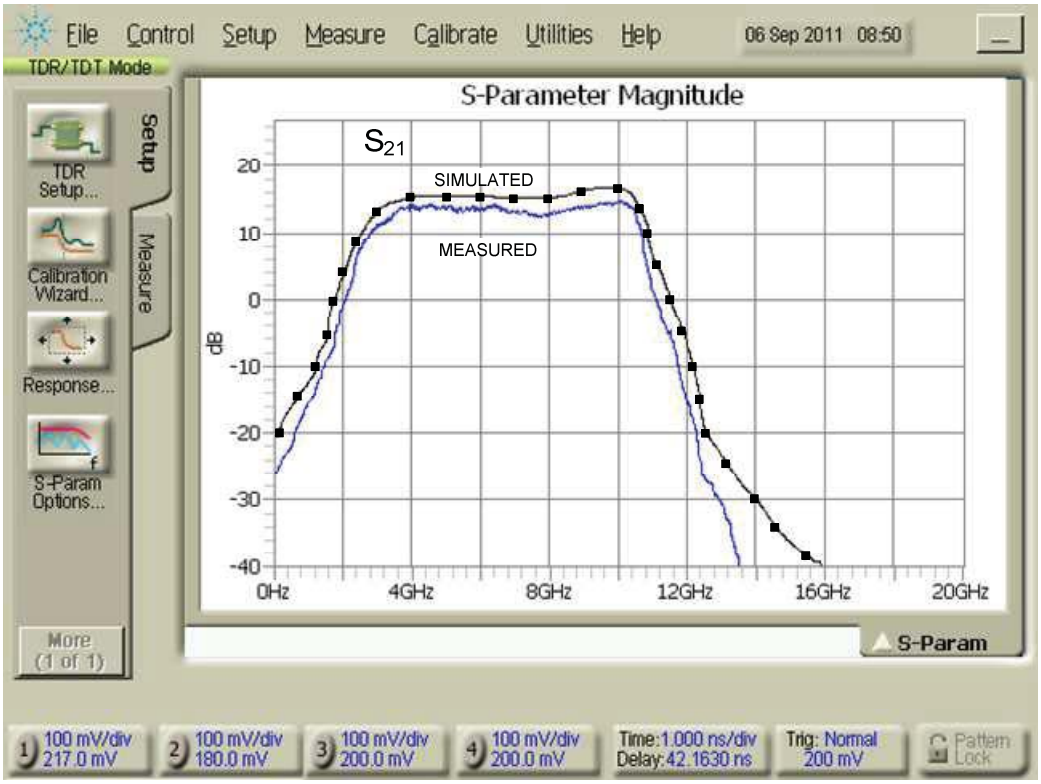

Fig. 5.10. Measured and simulated forward power gain in dB of the fabricated UWB LNA.

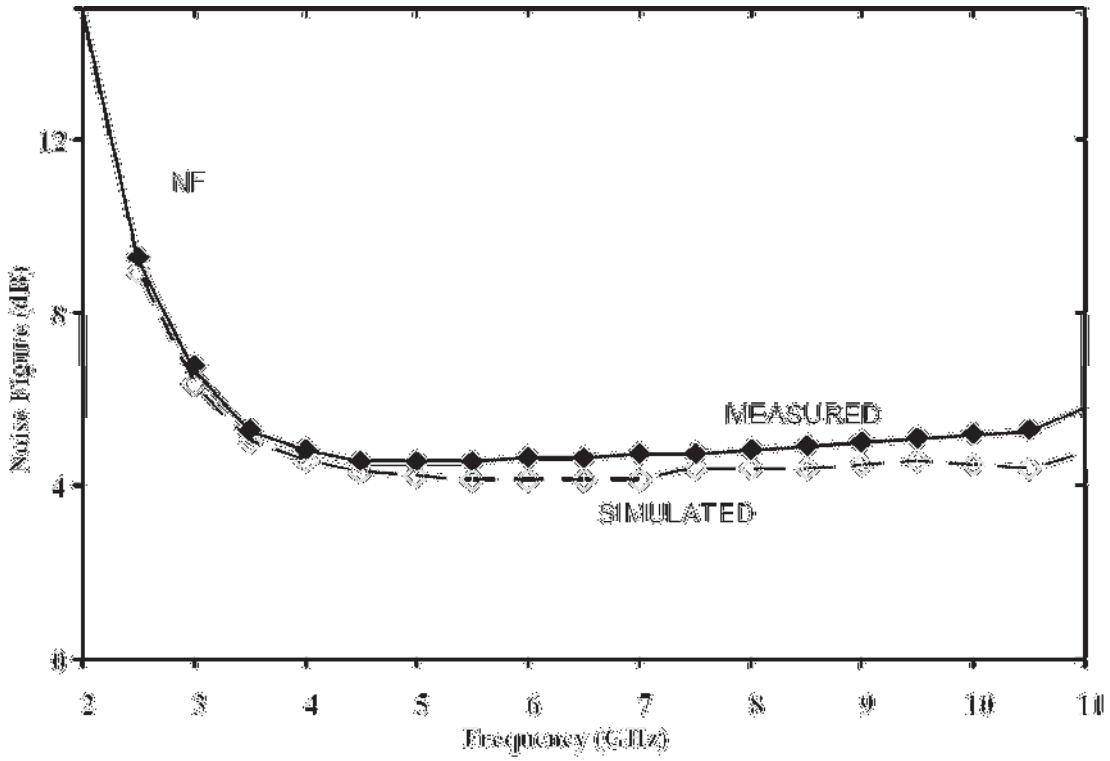

Fig. 5.11. Measured and simulated NF of the fabricated UWB LNA.

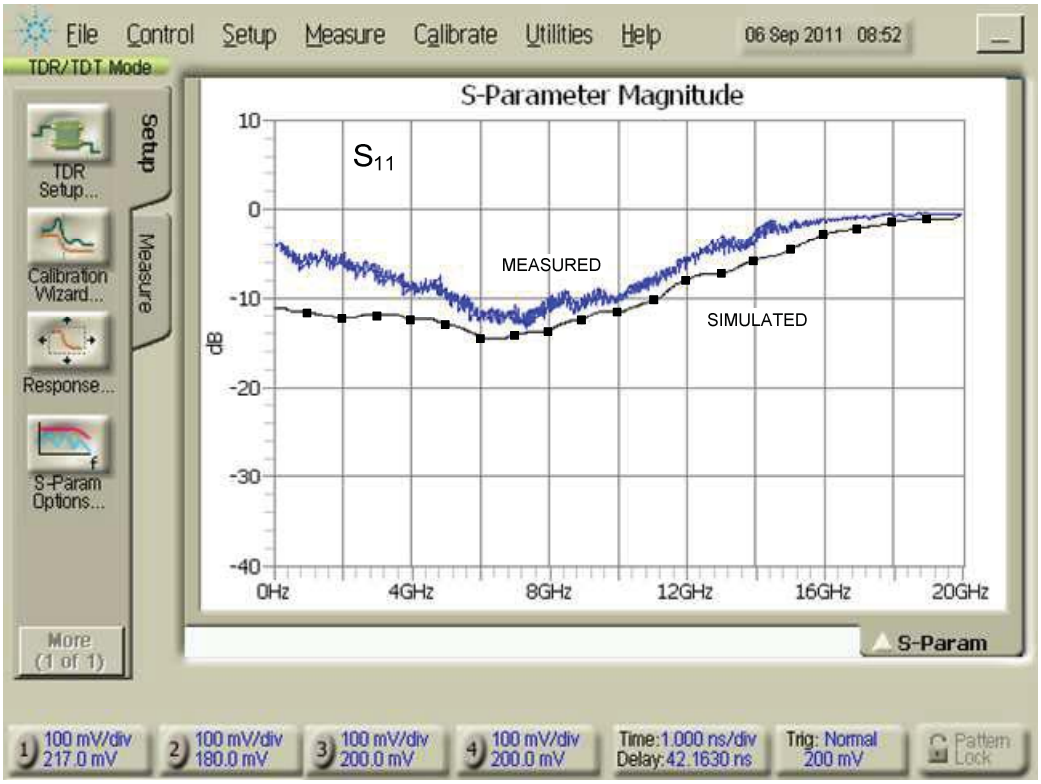

Fig. 5.12. Measured and simulated input reflection coefficient of the fabricated LNA.

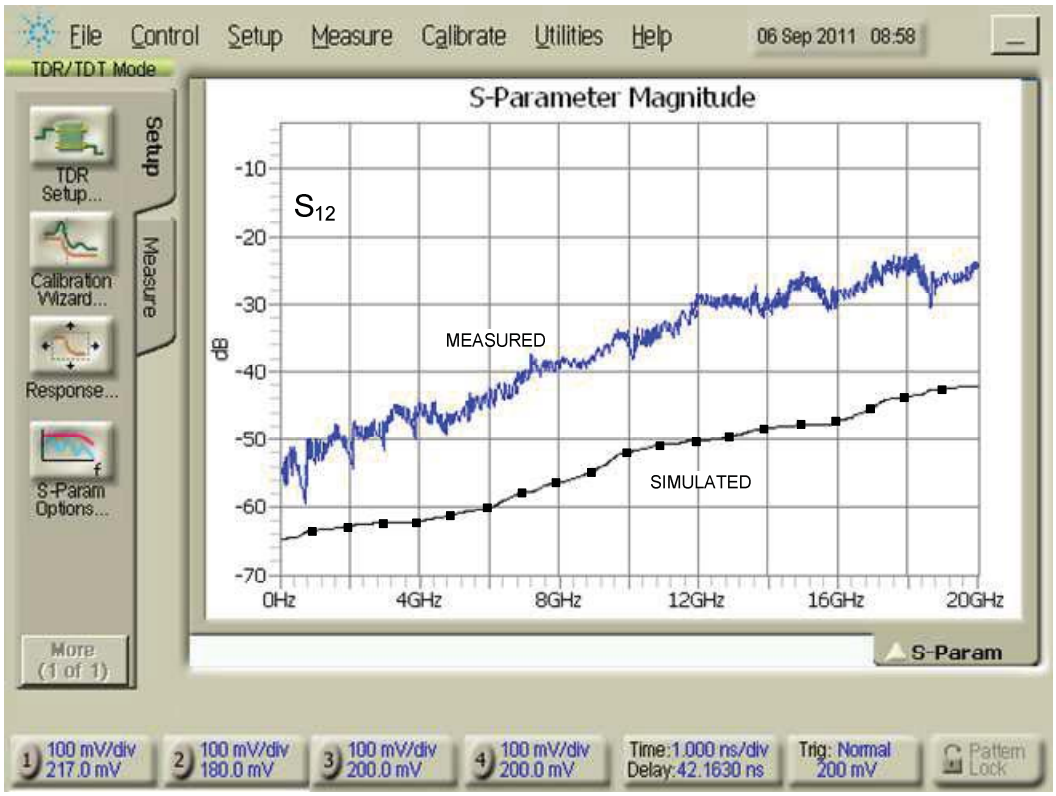

Fig. 5.13. Measured and simulated reverse power gain of the fabricated UWB LNA.

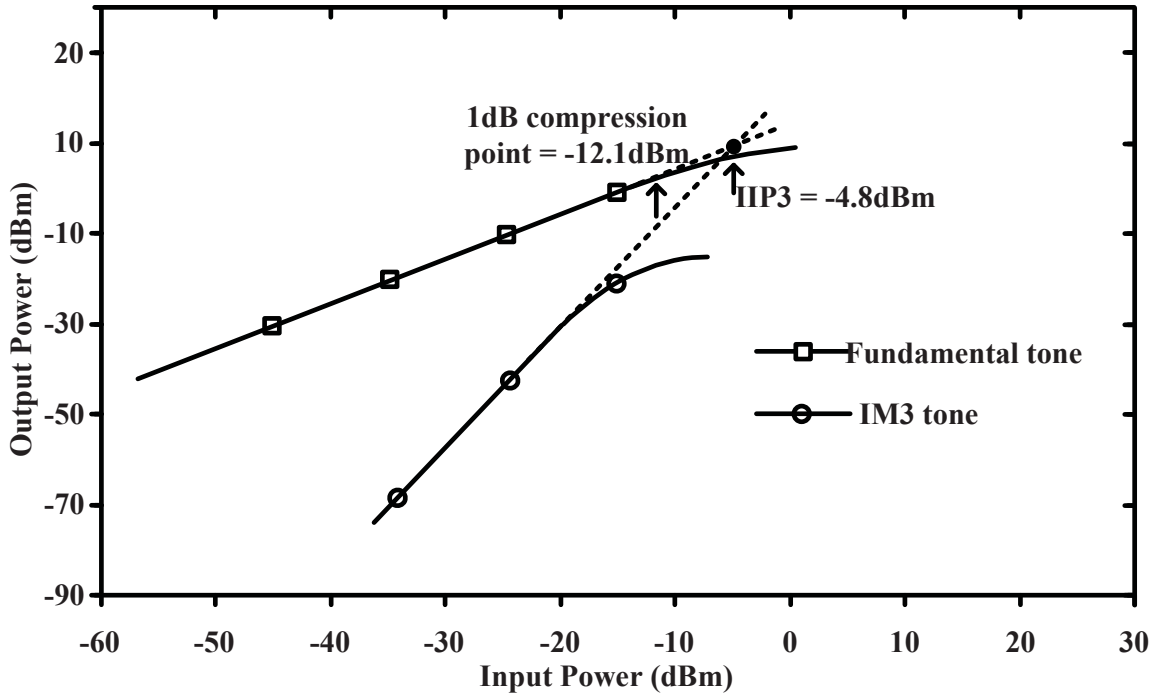

Fig. 5.14. Measured ICP_{1dB} and IIP3 of the fabricated UWB LNA at 6.85GHz.

5.6 Conclusion

The design analysis and experimental results presented in this chapter exhibit the capacity of the proposed circuit to operate in the full UWB spectrum from 3.1 to 10.6 GHz and to comply with the critical requirements of low noise performance with adequate power gain and linearity, effective input matching within the operating band and low power dissipation. Furthermore, the proposed UWB LNA is embedded with an intervening noise matching network at its input, designed to achieve optimal noise performance within the UWB band. This chapter presents the practical implementation of a second order noise matching network to maximize the SNR of the g_m-boosted CG LNA and derives the necessary mathematical expressions to enhance the noise performance. The fully-differential UWB LNA architecture presented in this chapter achieved an NF_{min} of 4.5dB with power dissipation of only 7mW using 1V power supply.

TABLE II. Summary of the noise matched series-peacked g_m-boosted noise matched CG UWB LNA performance, and comparison with previous recently published designs.

Specification	This Work [%]	[41]	[83]	[93]	[45]	[88][%]	[47]
Technology (nm)	130	180	180	180	130	90	90
Year	2011	2011	2010	2010	2009	2009	2011
$Bandwidth_{3\text{-}dB}$ (GHz)	3.1-10.6	2.8-10.4	3.4-11	3.1-10.6	3-10.35	3.1-10.6	2.6-10.2
Input return loss, S_{11}(dB)	<-8	<-10.1	<-10	<-9.5	<-8.3	<-9.3	<-9
Forward Gain, S_{21} (dB)	14.5	10.4	14	13.2	12.5	22.6	12.5
$Noise\ Figure_{min}$ (dB)	4.5	4.58	4.7	4.5	3.3	5.5	3
P_{diss} (mW)	7	2.15	30	28	7.2	34.8	7.2
Supply Voltage (V)	1.0	1.2	2.5	1.8	1.2	1.2	1.2
ICP_{1dB}(dBm)	-12.1	-15.4	-14.5	-11	-14	-19.7	-12
IIP3(dBm)	-4.8	-5.4	-5.3	-1.4	-	-	-

[a]%: Differential

CHAPTER 6

DISCUSSION

In an ultra-wideband (UWB) receiver, the goal of an analog frontend is to process the received signal prior to the digitization process. The low noise amplifier (LNA) is the most critical component of the analog frontend being the first subsystem in the receiver chain. The main function of the LNA is to amplify the received signal adequately with adding as little distortion and circuit noise as possible. To optimize the UWB LNA performance where the operating bandwidth can encompass several GHz, techniques developed to design the narrow band LNAs with fundamental assumption of *single-tone* input signal are inappropriate.

A technique to design the noise matched UWB LNA by defining the signal-to-noise ratio (SNR) of the system as the matched filter bound (MFB) was proposed in [63]. In the proposed design, the common source (CS) topology was employed to realize a practical LNA circuit ignoring the need of 50Ω input match. The optimal noise factor of the noise matched CS LNA was derived and found proportional to both the input signal frequency and the UWB operating bandwidth. The achievable optimum noise factor of the noise matched CS LNA was given by the following equation,

$$F_{opt\,CS} \approx \frac{\lambda.\Delta\omega}{\ln\left(1+\frac{\Delta\omega}{\omega_1}\right)} \tag{6.1}$$

Where $\Delta\omega=(\omega_2-\omega_1)$ is the UWB bandwidth with ω_1 and ω_2 being the lower and the upper cutoff frequencies of the pass-band, respectively. From (6.1), it is evident that the optimal noise factor of the noise matched CS UWB LNA worsens as the bandwidth of the input signal increases.

In Chapter 3 of this thesis, the g_m-boosted common gate (CG) LNA topology was exploited for its high input admittance, frequency independent noise factor and low power dissipation. It has been proven mathematically that in the presence of a noise matching

network, the optimal noise factor of the g_m-boosted CG UWB LNA topology is independent of the input signal frequency as well as the operating bandwidth and given by,

$$F_{opt_{CG}} \approx 1 + \frac{\gamma}{\alpha}\left(\frac{g_m}{R_s}\right)\left[\frac{r_{ds}^2}{\{1+(1+A)g_m r_{ds}\}^2}\right] \tag{6.2}$$

Here, $F_{opt_{CG}}$ is independent of the operating frequency ω and the UWB signal bandwidth $\Delta\omega$. The analysis presented in Chapter 3 established the advantage of the CG UWB LNA over the CS UWB LNA. The g_m-boosted CG topology with noise matching input network is found to be a better alternative for UWB LNA design, where the signal bandwidth can reach up to several GHz. The definitions of the different parameters in (6.1) and (6.2) can be found in [63] and Chapter 3, respectively.

Chapter 3 further explained in detail, the passive noise matching network design technique to realize a practical noise matched UWB LNA using the g_m-boosted CG topology. The analysis showed that under the noise matched condition; the passive network can be implemented as a single grounded inductor parallel to the g_m-boosted CG amplifier input with a series AC coupling capacitor to the UWB source.

Keeping in view the superior noise performance of the g_m-boosted CG amplifier topology for UWB, a new single-ended (SE) g_m-boosted CG UWB LNA architecture, operating in 3-5 GHz range, was proposed in Chapter 4. In the SE LNA, the bias current was shared between the g_m-boosted CG and the g_m-boosting CS stages in a current-reuse fashion. The active g_m-boosting amplifier stage was employed to provide the gain magnitude of larger than unity to enhance the SNR of the system considerably with less power dissipation. To demonstrate the feasibility of the proposed current-reuse structure, the design was fabricated using 130nm process and the measured results were found satisfactory for UWB LNA implementation. To improve the noise performance of the SE current-reuse g_m-boosted CG structure over the complete UWB frequency range, the 2nd LNA was fabricated employing the series peaking technique for bandwidth enhancement with an intervening noise matching filter. To design the noise matching filter for this UWB LNA, the technique presented in Chapter 3 was followed. Furthermore, to exploit the advantages of the differential topology, the UWB LNA was fabricated using 130nm process with a fully-differential structure. The design and fabrication methodologies and

the measurement results of the series peaked current-reuse g_m-boosted differential CG UWB LNA operating in 3.1-10.6 GHz range were reported in Chapter 5. It is noted that the noise contribution due to the CS g_m-boosting stage was also taken into account during the noise calculation and optimization of the full-band UWB LNA. The results show that the optimal values of the matching network components remain consistent as derived in Chapter 3 when the noise contribution of the CS g_m-boosting stage was ignored.

The earlier SE version of the LNA topology presented in Chapter 4, was aimed to deliver a low power and low noise solution in the 3-5 GHz frequency range. The mathematical analysis and experimental results presented in Chapter 5 exhibited the capacity of the current-reuse circuit to operate in the full UWB spectrum from 3.1 to 10.6 GHz. The noise matched differential UWB LNA complies with the critical requirements of low noise performance with adequate power gain and linearity, effective input matching within the operating band and low power dissipation. Although the input network was designed to maximize the SNR (noise match) but due to the higher input admittance of the g_m-boosted CG device, the proposed full-band differential LNA exhibited satisfactory power match within the complete UWB band. Slight deterioration of the input reflection coefficient at the frequencies nearer to the upper and lower cutoff was noted. This worsening of the input reflection coefficient at lower and higher frequencies was expected due to the band pass nature of the input passive network. It can be ignored if the antenna is placed in the close proximity of the UWB LNA chip.

In Table 6.1, the summary of the two fabricated current-reuse g_m-boosted CG UWB LNAs is presented and compared with other recently published wideband CMOS LNAs. A figure of merit (FOM) suitable for comparing the performance of the UWB LNA is also enlisted in Table III which is defined as [41], [94],

$$FOM[GHz/mW] = \frac{|S_{21}|_{abs}(BW)}{(|NF|_{abs} - 1) \times P_D} \tag{6.3}$$

Where (*abs*) stands for absolute value, S_{21} is the average forward power gain, BW is the -3dB bandwidth in GHz, NF is the average noise figure and P_D is the total power dissipation in mW.

TABLE III. Summary of the measured results for the two fabricated CG UWB LNAs and recently reported state-of-the-art CMOS UWB LNAs.

Work	Year	CMOS Technology	BW (GHz)	S_{11} (dB)	S_{21}dB)	P_D (mW)	Average NF (dB)	Minimum NF (dB)	IIP3 (dBm)	ICP_{1dB} (dBm)	Die Area (mm^2)	FOM (GHz/mW)	SE/Diff
LNA1	2010	130	1.7	<-8	13	3.4	3.7	3.5	-6.1	-15.4	0.4	1.66	SE
LNA2	2011	130	7.5	<-8	14.5	7.0	4.75	4	-4.8	-12.1	1	2.86	Diff
[41]	2011	180	7.6	<-10.1	10.4	2.15	4.9	4.58	-5.4	--	0.73	5.60	SE
[83]	2010	180	7.6	<-10	14	30	5.15	4.7	-5.3	-14.5	1.11	0.56	SE
[87]	2006	130	2.6	<-10	9.5	16.5	3.8	3.5	-0.8	-6	1.08	0.34	Diff
[88]	2009	90	7.5	<-9.3	22.6	34.8	6	5.5	--	-19.7	0.69	0.98	Diff
[89]	2008	90	7.9	<-10	16	16	4.6	3.4	-9	--	0.14	1.65	Diff
[90]	2008	90	8.8	<-10	10	20	6.1	4.2	-8	--	0.13	0.45	Diff
[91]	2006	130	0.83	<-10	13	3.6	4	4	-10.2	-18	0.3	0.68	Diff
[92]	2010	180	1.8	<-10	15	5	3.6	3.5		-18	0.76	1.57	SE
[93]	2010	180	7.5	<-9.5	13.2	28	5.35	4.5	-1.4	-11	1.42	0.50	SE

LNA1: SE g_m-boosted CG UWB LNA operating in 3-5 GHz range.

LNA2: Differential (Diff) full-band g_m-boosted CG UWB LNA.

Table III shows better performance of the proposed circuit (LNA2) with the largest FOM among the published differential UWB amplifiers. It is evident by the state-of-the-art measured results of the proposed UWB LNA, that the design is suitable for the full-band UWB operation. The noise model developed and employed for the fabrication of the full-band UWB LNA takes the channel resistance (r_{ds}) into account. This makes the noise model relevant when an advanced process with smaller channel length would be targeted for the implementation of the UWB LNA circuit.

CHAPTER 7

CONCLUSION

7.1 Summary

Ultra-wideBand (UWB) radio technology is considered to be a compelling solution for short range communications. It is characterized by high data-rates, low-power consumption devices robustness to multi-path fading, and low-power emission that allows it to coexist with other indoor wireless technologies. The doctoral research targeted the design, fabrication and testing of the low noise amplifier (LNA) for UWB receiver frontend.

This thesis very briefly describes the basics of UWB technology and frequency spectral mask approved by FCC. After carefully studying the UWB LNA architectures, the common gate (CG) amplifier topology is chosen to design the UWB LNA. To optimize the noise performance of the CG UWB LNA, the well-known g_m-boosting technique is adopted. To enhance the signal-to-noise ratio (SNR) of the LNA system, an intervening passive noise matching network is introduced. In the research, a new mathematical model is developed to optimize the size of the noise matching network components based on the DC operating of the LNA circuit and the operating bandwidth. The novel noise optimization mathematical model also takes into account the effect of the finite drain-to-source admittance of the CG amplifying device and describes its effect on the system SNR. Furthermore, the mathematical model is verified using simulation of an example test circuit where a common source (CS) stage is employed to provide the g_m-boosting gain. To study the tradeoff between the noise-match and power-match conditions, a power-matched single-ended (SE) g_m-boosted CG LNA is fabricated using 130nm IBM process operating in the 3-5 GHz range. The fabricated SE LNA circuit uses a new variation of the current-reuse technique to optimize the power dissipation by sharing the bias current between multiple amplifiers. In the SE LNA design, the bias current is shared between the CG amplifying stage and the CS g_m-boosting stage ("*piggyback g_m-boosting*"). A 2nd order band pass filter is used at the input of the power-matched SE LNA to provide sharp out-of-

band roll-off. An improved fully-differential version of this current-reuse g_m-boosted CG LNA is also fabricated using 130nm IBM process exploiting the series peaking technique to enhance the bandwidth of the UWB LNA. The series peaked current-reuse g_m-boosted CG fully-differential UWB LNA is designed to attain noise-match by employing the mathematical noise model developed in this research. In this connection, a noise matching network is employed at the input of the fabricated UWB circuit. The thesis presents the simulation and the measurement results of the fabricated circuits in detail with necessary derivations and mathematical expressions to optimize the noise of the UWB LNAs.

The measured results of the fully-differential series peaked noise matched g_m-boosted CG UWB LNA validate the noise optimization technique proposed in this thesis. It is also proven that the current-reuse technique can be adopted successfully by sharing the DC current between the UWB g_m-boosted CG amplifier and the g_m-boosting CS amplifier stages ("*noise-matched piggyback g_m-boosting*") to realize a fully-differential UWB LNA with highest FOM as indicated in the Table III in the previous chapter.

7.2 Future Work

7.2.1 Noise Optimization of the CS g_m-Boosting Amplifier

The noise model developed in this thesis does not address the optimization of the CS g_m-boosting amplifier in detail. Further work can be done by employing inductive degenerated CS amplifier in the circuit and its effect on the input matching and noise matching characteristics of the UWB LNA can be studied. The inductive degeneration of the CS stage can increase the effective input admittance at the source terminal of the CG stage making effective power match possible with lower power dissipation. It can also result in enhancement of the over-all system SNR as the noiseless inductive network will boost the UWB signal prior to entering the CS stage.

7.2.2 Modeling a Noisy Matching Network at the UWB LNA Input

The noise optimization technique presented in this thesis assumes noiseless noise matching network components. Advanced inductor and capacitor models can be used with embedded relevant noise sources to model the effects of non-idealities. This can enhance the accuracy of the noise optimization technique presented in this thesis.

7.2.3 System Integration

The proposed noise-matched UWB LNA is designed using fully-differential circuit configuration keeping in view the requirements of a complete system-on-chip (SOC) design. Further work can be done by integrating the proposed UWB LNA with the UWB RF receiver subsystems on the same die including differential mixers, frequency hopping local oscillators (LOs), analog filters and analog-to-digital converters (ADCs). Many challenging issues can arise when it is integrated with other RF and mixed signal subsystems of UWB frontend.

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APPENDICES

I) Appendix A – Derivation of UWB LNA System Model

II) Appendix B – Derivation of Correlation Susceptance for g_m-boosted CG Device

APPENDIX A

Derivation of UWB LNA System Model

The general model of the g_m-boosted CG LNA for UWB is given in Fig. 3. For ease in mathematical derivation, current sources in parallel with r_{ds} are converted into the corresponding voltage sources in series and the resulting equivalent circuit model is shown in the Fig. A-1.

To find the output voltage $v_{out}(t)$ across the load resistance R_L in Fig. A-1, due to the UWB signal source $v_{in}(t)$, all the noise sources are suppressed. Using the voltage divider rule, $v_s(t)$ (i.e. the voltage between the source terminal of the MOS device and the circuit ground) is given by,

$$v_s = \frac{Z_{s1}}{(R_s + jX_a) + Z_{s1}} \cdot v_{in} \tag{A-1}$$

Where, $Z_{s1}(\omega)$ is the impedance looking into the source terminal of the MOS device as shown in Fig. A-1, and is given by,

$$Z_{s1} = \frac{(r_{ds} + R_L)}{1 + \beta g_m r_{ds} + jB_b(r_{ds} + R_L)} \tag{A-2}$$

Where, β=A+1. Hence, (A-1) can be reorganized as,

$$v_s = \frac{(r_{ds} + R_L)}{(R_s + jX_a)\{1 + \beta g_m r_{ds} + jB_b(r_{ds} + R_L)\} + (r_{ds} + R_L)} \cdot v_{in} \tag{A-3}$$

By applying KVL to determine $i_L(t)$ (i.e. the loop current through R_L) the voltage loop equation is given by,

$$v_s = i_L(r_{ds} + R_L) + g_m v_{gs} r_{ds}$$

$$\text{Or,} \qquad v_s = i_L(r_{ds} + R_L) - \beta g_m r_{ds} v_s \tag{A-4}$$

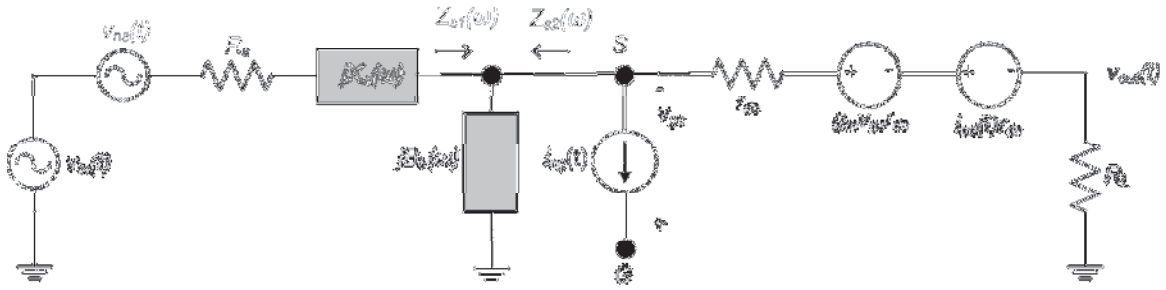

Fig. A-1. Equivalent circuit model of the CG UWB LNA.

Solving (A-3) and (A-4) simultaneously, $i_L(t)$ is given by,

$$i_L = \frac{(1+\beta g_m r_{ds})v_{in}}{(R_s + jX_a)\{1+\beta g_m r_{ds} + jB_b(r_{ds}+R_L)\} + (r_{ds}+R_L)} \tag{A-5}$$

and since, $v_{out}(t)=i_L(t)R_L$, the output voltage is given by,

$$v_{out} = \frac{(1+\beta g_m r_{ds})R_L}{(R_s + jX_a)\{1+\beta g_m r_{ds} + jB_b(r_{ds}+R_L)\} + (r_{ds}+R_L)} \cdot v_{in} \tag{A-6}$$

To find the output voltage $v_{nd,out}(t)$ across load R_L in Fig. A-1 due to the drain current noise source $i_{nd}(t)$, all the other noise sources and the input voltage source are suppressed. Then, applying KVL (with i_{nd,R_L} being the loop current through the load due to the drain current noise), the voltage loop equation is given by,

$$\begin{aligned} &(Z_{s2} + r_{ds} + R_L)\cdot i_{nd,R_L} + g_m v_{gs} r_{ds} + i_{nd} r_{ds} = 0 \\ \text{Or, } &(Z_{s2} + r_{ds} + R_L)\cdot i_{nd,R_L} + \beta g_m v_s r_{ds} + i_{nd} r_{ds} = 0 \\ \text{Or, } &(Z_{s2} + r_{ds} + R_L)\cdot i_{nd,R_L} + \beta g_m i_{nd,R_L} Z_{s2} r_{ds} + i_{nd} r_{ds} = 0 \\ \text{Or, } &(Z_{s2} + \beta g_m Z_{s2} r_{ds} + r_{ds} + R_L)\cdot i_{nd,R_L} + i_{nd} r_{ds} = 0 \end{aligned} \tag{A-7}$$

After re-arranging and multiplying by R_L, $v_{nd,out}(t)$ is given by,

$$v_{nd,out} = i_{nd,R_L}\cdot R_L = \frac{-r_{ds}R_L}{Z_{s2}(1+\beta g_m r_{ds}) + r_{ds} + R_L}\cdot i_{nd} \tag{A-8}$$

Where, $Z_{s2}(\omega)$ is the equivalent impedance looking out of the source terminal of the MOS device, as shown in the Fig. A-1, and is given by,

$$Z_{s2} = \frac{R_s + jX_a}{1 - X_a B_b + jR_s B_b} \tag{A-9}$$

Putting $Z_{s2}(\omega)$ from (A-9) into (A-8), output noise voltage due to the drain current noise source is then given by,

$$v_{nd,out} = \frac{-(1 - X_a B_b + jR_s B_b) r_{ds} R_L}{(R_s + jX_a)\{1 + \beta g_m r_{ds} + jB_b(r_{ds} + R_L)\} + (r_{ds} + R_L)} \cdot i_{nd} \tag{A-10}$$

Next, to find the output voltage $v_{ng,out}(t)$ across R_L in Fig. A-1, due to the gate current noise source $i_{ng}(t)$, all the other noise sources and the input voltage source are suppressed. By inspection, it can be easily determined that the voltage $v_s(t)$, in this case, is given by,

$$v_s = i_{ng} \{Z_{s1} \parallel (R_s + jX_s)\}$$

$$\text{Or,} \quad v_s = \frac{(R_s + jX_a) \cdot (r_{ds} + R_L) \cdot i_{ng}}{(R_s + jX_a) \cdot \{1 + \beta g_m r_{ds} + jB_b(r_{ds} + R_L)\} + (r_{ds} + R_L)} \tag{A-11}$$

Using (A-4), $v_s(t)$ (with i_{ng,R_L} being the loop current through the load R_L due to the gate current noise) is then given by,

$$v_s = i_{ng,R_L} \cdot \frac{(r_{ds} + R_L)}{(1 + \beta g_m r_{ds})} \tag{A-12}$$

Equating (A-11) and (A-12), and multiplying both sides by R_L, $v_{ng,out}(t)$ is given by,

$$v_{ng,out} = \frac{(R_s + jX_a)(1 + \beta g_m r_{ds}) R_L}{(R_s + jX_a)\{1 + \beta g_m r_{ds} + jB_b(r_{ds} + R_L)\} + (r_{ds} + R_L)} \cdot i_{ng} \tag{A-13}$$

APPENDIX B

Derivation of Correlation Susceptance for g_m-boosted CG Device

The general model of the short-channel g_m-boosted CG LNA is given in Fig. 2. From (16) and (17), the voltage $v_{in,ind}(t)$ at the input of the CG amplifier (i.e. the source terminal), due to the drain current noise $i_{nd}(t)$ is given by,

$$v_{in,ind}(t) = \frac{r_{ds}}{1 + \beta g_m r_{ds}} . i_{nd}(t) \tag{B-1}$$

The above equation shows that the noise voltage $v_{in,ind}(t)$ is completely inphase with $i_{nd}(t)$. Taking the Fourier transform on both sides, (B-1) can be written as,

$$V_{in,ind}(\omega) = \left(\frac{r_{ds}}{1 + \beta g_m r_{ds}} \right) I_{nd}(\omega) \tag{B-2}$$

By virtue of its definition, the correlation admittance $Y_c(\omega)$ is given by,

$$Y_c(\omega) = \frac{I_{ng,c}(\omega)}{V_{in,ind}(\omega)} \tag{B-3}$$

Where, $I_{ng,c}(\omega)$ is the frequency domain representation of the gate current noise that is correlated with the drain current noise and represented as $i_{ng,c}(t)$ in the time domain. From (B-2) and (B-3), $Y_c(\omega)$ is given by,

$$Y_c = \left(\frac{1 + \beta g_m r_{ds}}{r_{ds}} \right) \frac{I_{ng,c}}{I_{nd}}$$

$$\text{Or,} \qquad Y_c = \left(\frac{1 + \beta g_m r_{ds}}{r_{ds}} \right) \frac{\overline{I_{ng,c} I_{nd}^*}}{\overline{I_{nd} I_{nd}^*}}$$

$$\text{Or,} \qquad Y_c = \left(\frac{1 + \beta g_m r_{ds}}{r_{ds}} \right) \frac{\overline{I_{ng} I_{nd}^*}}{\overline{I_{nd}^2}} \tag{B-4}$$

As the uncorrelated component of the gate current noise $I_{ng}(\omega)$ does not contribute to the cross-correlation [18], $I_{ng,c}(\omega)$ is replaced by $I_{ng}(\omega)$ in (B-4). Next, (B-4) can be re-written as,

$$Y_c = \left(\frac{1 + \beta g_m r_{ds}}{r_{ds}} \right) \frac{\overline{I_{ng} I_{nd}^*}}{\sqrt{\overline{I_{nd}^2}} \sqrt{\overline{I_{nd}^2}}} \sqrt{\frac{\overline{I_{ng}^2}}{\overline{I_{ng}^2}}}$$

$$\text{Or,} \qquad Y_c = \left(\frac{1 + \beta g_m r_{ds}}{r_{ds}} \right) \frac{\overline{I_{ng} I_{nd}^*}}{\sqrt{\overline{I_{ng}^2}} \sqrt{\overline{I_{nd}^2}}} \sqrt{\frac{\overline{I_{ng}^2}}{\overline{I_{nd}^2}}} \tag{B-5}$$

(B-5) can be re-written in terms of the corresponding PSDs of the noise currents as,

$$Y_c = \left(\frac{1 + \beta g_m r_{ds}}{r_{ds}} \right) \frac{\sqrt{S_{i_{ng}}(\omega) \cdot S_{i_{nd}}^*(\omega)}}{\sqrt{S_{i_{ng}}(\omega)} \cdot \sqrt{S_{i_{nd}}(\omega)}} \sqrt{\frac{S_{i_{ng}}(\omega)}{S_{i_{nd}}(\omega)}} \tag{B-6}$$

By substituting suitable values from (11), (12) and (13) into (B-6), $Y_c(\omega)$ is given by,

$$Y_c(\omega) = jB_{gs}(\omega) \left\{ \frac{1 + (1 + A) g_m r_{ds}}{r_{ds} g_{d0}} |c| \sqrt{\frac{\delta}{5\gamma}} \right\}$$

$$\text{Or,} \quad Y_c(\omega) = j \frac{B_{s,eff}(\omega)}{\beta} \left\{ \frac{1 + \beta g_m r_{ds}}{r_{ds} g_{d0}} |c| \sqrt{\frac{\delta}{5\gamma}} \right\} = jB_c(\omega) \tag{B-7}$$

LIST OF PUBLICATIONS

I) Journal paper titled "Novel analysis and optimization of g_m-boosted common-gate UWB LNA" in *Microelectronics Journal*, vol. 42, issue 2, Feb. 2011, pp. 253-264.

II) Journal paper titled "A 3-5 GHz current-reuse g_m-boosted CG LNA for ultrawideband in 130 nm CMOS" in *IEEE Trans. Very Large Scale Integration Systems*, (Accepted for publication) available online, URL: http://ieeexplore.ieee.org/stamp/stam p.jsp?arnumber=05720541, accessed 08 Nov. 2011.

III) Journal paper titled "A series peaked noise matched g_m-boosted 3.1-10.6 GHz CG CMOS differential LNA for UWB WiMedia" in *Electronic Letters*, (Accepted for publication), 2011.

IV) Journal paper titled "A series peaked g_m-boosted 3.1-10.6 GHz CMOS CG UWB LNA for WiMedia" in *Microwave and Optical Technology Letters*, Wiley Inter-Science, (Accepted for publication), 2011.

V) Journal paper titled "A 4mW 3-5 GHz current reuse g_m-boosted short channel common-gate CMOS UWB LNA" in *Analog Integrated Circuit and Signal Processing, Express Letters*, Kluwer Academic Publishers (Springer), vol. 65, pp. 415-418, 2010.

VI) Conference paper titled "Design of a sub-gigahertz complementary cascode LNA with active input matching" in *Proceedings of 15th Electronics New Zealand Conference*, Nov. 24-25, Auckland, New Zealand, pp. 39-44, 2008.

VII) Conference paper titled "Design of a full-band g_m-boosted current reused UWB LNA" in *Proceedings of 15th Electronics New Zealand Conference*, Nov. 24-25, Auckland, New Zealand, pp. 25-28, 2008.

VIII) Conference paper titled "Design of a low-power narrowband amplifier for HF radio applications using CMOS FETs" in *Proceedings of 16th Electronics New Zealand Conference*, Nov. 18-20, Dunedin, New Zealand, pp. 131-136, 2009.