CMOS Radiation Sensor Design in 130nm CMOS Technology

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by

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Abstract

This research work deals with a CMOS radiation sensor design, which covers a new open source floating-gate MOSFET (FGMOSFET) device model for analog circuit design, Floating Gate Radiation Field Effect Transistor (FGRADFET) design, FGRADFET sensor output circuit design and their layout implementation using the 130nm IBM CMOS process.

At first, a new FGMOSFET device model to facilitate circuit design is presented. In this model, the floating gate is charged by the Fowler-Nordheim tunneling effect. The equations representing the new device model were explored and verified on MATLAB. Verilog-A script was employed to transfer the equations and build the complete device model. The new FGMOSFET circuit model was plugged-in as a pop-up menu component in a standard 130 nm CMOS technology design library so that it can be instanced directly on a schematic editor palette for analog circuit simulation and design in a similar fashion as the standard MOSFET devices. Furthermore, the thesis describes the radiation sensor of FGRADFET that has an extra silicon area ($125\mu m \times 200\mu m$) as an antenna to sense the radiation from the environment. There are 16 PMOS transistors ($1\mu m \times 2\mu m$ *each*) beneath the edge of the antenna to charge the floating gate. A radiation sensor readout circuit is also designed for this sensor. This circuit includes differentiator, pre-amplify buffer, chopper amplifier, low-pass filter and single-ended output amplifier. This integrated dosimeter has a 3.205mW power consumption and 2.33mGy -23mGy measuring range (The single-ended output voltage changes from 226mV to 967mV), which could be used for tremendous radiation exposure applications such as radiation therapy.

Acknowledgements

I wish to express my utmost appreciation and special thanks to my supervisor Dr. Rezaul Hasan for providing me with exciting research project and for his glowing advice, patient guidance, inspiring encouragement and endless support throughout my studies and research. He has a broad knowledge of VLSI and integrated circuit design. The spirit of his hard work and attitude of patience impress me deeply. I still remember the first time that I visited him in his office. That day, there was no one working in that building because it was the day just before Christmas. He was the only one working in his office. It is Dr. Rezaul Hasan tought me how to treat my work with a thorough and patient attitude. I thank him, and all his help and valuable advice would be kept in my mind forever. He has always been my constant source of motivation. Without his guidance and persistent help, this work would not have been possible.

Special thanks go to my great colleagues Mr. Stepan Lapshev, Ms. Meera Kumari and Ms. Sara Han. It is a fantastic experience to stay and work with them. I thank Mr. Stepan Lapshev who gives me a lot of useful guidance and good advice on how to use CAD software. Thanks to Ms. Meera Kumari and Ms. Sara Han for their generous suggestions and patient discussion with me on my research.

At last but not least, I would like to appreciate my family for their unconditional support and constant motivation throughout my studies. They invested their blessings and entire resources in helping me to grow and accomplish my goal. There is no doubt that I would never arrive at this point without their substantial help, which I will always remember.

Declaration

The author declares that this is his own work except where due acknowledgment has been given. It is being submitted for Master in Engineering to Massey University, New Zealand.

This thesis describes the research carried out by the author at the Scool of Engineering and Advanced Technology, Massey University, New Zealand from February 2017 to November 2017, supervised by Dr. Rezaul Hasan.

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List of Symbols and Abbreviations

ADE	Analog Design Environment
BPS	Boro-Phosphoro-Silicate
BSIM	Berkeley Short-channel IGFET Model
CM	Common Model
CAD	Computer-Aided Design
CMOS	Complementary Metal Oxide Semiconductor
DRC	Design Rule Check
EPROM	Erasable Programmable Read-Only Memory
EEPROM	Electrically Erasable Programmable Read-Only Memory
FGMOSFET	Floating-gate Metal Oxide Semiconductor Field Effect Transistor
FGRADFET	Floating Gate Radiation Field Effect Transistor
GM	Geiger Muller
IBM	International Business Machines Corporation
ICs	Integrated Circuits
LVS	Layout vs Schematic
LPF	Low-Pass Filter
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
NMOS	N-Type Metal-Oxide-Semiconductor
PMOS	P-Type Metal-Oxide-Semiconductor
PEX	Practices Extraction
PSD	Power Spectral Density
PLL	Phase Locked Loop

RADFET	Radiation Field Effect Transistor
SEAT	School of Engineering and Advanced Technology
SiO_2	Silicon Dioxide
TID	Total Ionizing Dose
VLSI	Very-Large-Scale Integration
VCO	Voltage Control Oscillator
V_{th}	Threshold Voltage

Chapter 1 Introduction

This chapter delivers a brief background and motivation for this research work. The objectives of this thesis, its contributions to knowledge and its organization are also presented.

1.1 Thesis Background

Radiation is a normal phenomenon in nature. For example, the night pearl that some people like has different levels of radiation. The luminous that night pearl produced comes from the effect of the rays produced by its radioactive material impacting with other substances. Radioactivity in our lives is more common derived from air and drinking water, which usually caused by radioactive radon. Generally, radon enters the atmosphere from soil and rock. In lower basements and lower floors, the concentration of radon is higher, and radioactivity is stronger in this case. People only suffer from radiation that from the natural environment in the past. Today, some medical devices, such as computed tomography (CT) and x-ray, would cause more radiation to human bodies.

However, radiation cannot be seen and touched. We can only infer the radiation by its effect on some other material. This material can act as the radiation sensor to help us sense and measure the radiation. The radiation sensor with its readout circuit is called radiation dosimeter.

Radiation dosimeter has been used widely for a broad range of applications in the society, such as radiation therapy [1][2] in the hospital, security check in the airport [3] and radiation analysis in spacecraft [4]. As an important component of nuclear radiation detection, dosimeter has been significantly improved with the development of science, technology and the expansion of nuclear technology applications. The size of radiation dosimeter is becoming smaller and smaller. Micro radiation dosimeter also becomes more and more popular and is prefered in some special situations like radiation therapy in hospital and radiation detection in spacecraft.

Currently, there are many types of radiation dosimeters, such as ionization chamber, GM counter tube and scintillator detector. However, they have common drawbacks: low energy resolution, long time resolution, big size and GM counter tube also need high voltage to work. However, semiconductor detectors overcome these limitations and have the advantages of high energy resolution, short time resolution, small volume, lightweight, simple structure, anti-magnetic field interference and so on. Even if there are so many advantages about semiconductor detectors, the strict limitation of spread and universal IC technology, the difficulty to process the small ionizing radiation signal and lack of

FGMOSFET model make it less accessible for general people to design integrated CMOS radiation sensor.

1.2 Motivation

In the investigation of radiation therapy, which is one of the most common treatments for cancer. The radiation therapy uses high-energy waves or particles likes γ-rays and x-rays to damage or destroy cancer cells with as little harm as possible to nearby healthy cells. The radiation therapy can be given in three different ways [5].

First one is external radiation, which utilizes a machine that guides high-energy rays from outside the body into a tumor. Currently, this guidance data comes normally from the imaging scans that are done before every treatment with three-dimensional conformal radiation therapy (3D-CRT). Therefore, there is no indication whether the high-energy rays arrived at the tumor exactly and how much radiation received in there. Considering this, the integrated wireless radiation dosimeter that can be designed as small as 2mm square package size can be employed and placed exactly around the tumor to enhance the guidance of the high-energy particles and measure the total dose that the tumor has received. This radiation dose data received by the dosimeters around the tumor can be calculated by computers and helps to adjust the position of the high-energy particles machine and re-focus the radiation, which could provide more accurate local radiation treatment and lower the damage for other healthy cells.

The second method to carry out the radiation therapy is called internal radiation. A radioactive source is placed inside the body into or very near the tumor, which is normally a painless procedure and has a lower radiation harms for few normal cells than external radiation. In this process, the integrated wireless radiation sensor still can be utilized to real-time monitor the situation of radiation source by tied them together. Since the radiation coming from radiation source will become weaker and weaker as time goes by, we can know how much the radiation dose rate is left and working by the real-time monitoring from the dosimeter and make the decision to change the radiation source.

The third method of radiation therapy is systemic radiation, which is carried out on radioactive drugs that are put into a vein or given through mouth. These radioactive drugs then flow through in the body. In this case, the radiation dosimeter can be used to test the radiation dose rate of blood extracting from this body.

Another important application for integrated dosimeter is blood transfusion [6], in which γ-rays and x-rays are required to sterilize the blood to prevent patient infection. Currently, the procedures of blood

sterilization rely on a machinist's assessment of the color variation of rad labels located on each blood bag. This controlling mechanisms and operator's mistakes could cause the uncertainties in the operation of the blood-irradiator machine, which will subsequently cause blood over irradiated or under irradiated and eventually waste the blood. This whole procedure should be updated by replacing the rad labels with a dosimeter that can be read automatically by computer avoiding the operating errors. Prevent day, accessible radiation dosimeters cannot be integrated into integrated circuits (ICs) for the automatic record. Therefore, lots of blood are over irradiated or under irradiated when the operators are tired and make mistakes. Furthermore, these rad labels are not recyclable, which will increase the cost of blood sterilization when massive amounts are involved.

Since most of equipment in the spacecraft should be designed as small as possible and as light as possible to make sure a higher acceleration and lasting flight, radiation detection in spacecraft have a higher demand in integrated dosimeter.

In conclusion, it is necessary to do research about integrated dosimeter that could contribute to the development of medical and some other applications.

1.3 Thesis Objectives

The overall objective is to design an integrated CMOS radiation sensor. This research work also involves these specific objectives:

1) Conduct a wide-ranging review of the up-to-date state of the radiation dosimeters to find the better way to design FGMOSFET sensor devices.
2) Design a FGMOSFET device model for FGRADFET simulation and design with Verilog-A language in Cadence, and in MATLAB.
3) Perform an experimental analysis of FGMOSFET device to understand how it works and what the difference between FGMOSFET and MOSFET is.
4) Design the structure of FGRADFET sensor that can be embedded in the same chip with readout circuit.
5) Design the floating-gate voltage readout circuit and Fowler-Nordheim tunneling charging circuit.
6) Design an appropriate readout circuit to process the small ionizing radiation signal.
7) Design and layout IC arrangements of floating-gate dosimeters in 130nm IBM-CMOS technology, and test these layout in DRC, LVS and PEX simulations.
8) Conduct a series of simulation and experiment analysis to assess and verify the validity of the dosimeter designs.

1.4 Thesis Contributions to Knowledge

The main contribution of this thesis is design and development of the FGMOSFET model, small signal process. This research illustrated in the following chapters of this thesis makes fundamental contributions to knowledge around CMOS dosimeter design by:

1) Presenting a design for a fully-integrated novel Floating-gate MOSFET radiation sensor on a recent 130nm manufacturing process.
2) Enhancing the understanding of FGMOSFET device model.
3) Enhancing the understanding of the single-poly FGRADFET's geometry structure.
4) Enhancing the understanding of current mirror, differentiator, chopper amplifier, buffer, low-pass filter and a single-end output circuit.
5) Developing the ability to calculate the transistors' size to obtain an optimized output signal.
6) Improving the ability to analysis circuit, draw energy band diagram, design and layout analog circuit.
7) Improving the ability to analyze and solve IC circuit design problem.

1.5 Thesis Organization

This thesis is arranged as follows: Chapter 2 evaluates the literature related to the objectives and details through an overview of the dosimeter applications, the nature of several rays, different approaches to measure rays, and floating gate dosimeter. In Chapter 3, the geometry and theory of FGMOSFET, FGMOSFET mathematical model, simulation and verification results of FGMOSFET simulation model and the design of single polysilicon FGRADFET will be presented. Chapter 4 describes radiation sensor's front-end readout circuit design including block diagram for the whole dosimeter circuit, floating gate voltage readout circuit design, differentiator circuit design, source-follower preamplifier buffer design, modulation and demodulation chopper circuit design and two-stage differential amplifier design. This is followed by a Chapter 5 on the radiation sensor output circuit design, which is composed of pre-filter circuit design, four order low-pass filter circuit design, single-ended output circuit design, an overall circuit diagram of the dosimeter and the overall layout for the dosimeter. Chapter 6 illustrates the transient analysis for the whole circuit, DRC and LVS analysis for the whole layout, and PEX analysis for the whole layout. Finally, Chapter 7 summarizes all results from the research, the issues and challenges emerging from this research, and provides possible directions for future work.

Chapter 2 System Overview and Literature review

2.1 Dosimeter Applications

The main applications of the dosimeter are:

(1) Environmental, air quality monitoring

(2) Nuclear power plants, hospitals and other radioactive real-time monitoring

(3) Radioactive detection of building materials

(4) Petroleum industry, scientific investigation, archaeological exploration, geology

(5) To measure the content of radioactive elements in natural minerals and jewelry

2.2 The Nature of Several Radiation

In our living space, there are a variety of radioactive rays, mainly including α-ray, β-ray and γ-ray owing to the decay of nuclei, and X-ray producing by electron evolution from the atomic shell [7].

α-ray is a charged particle flow, the most prone to ionization. But its ability to penetrate is the worst compared with other rays. A piece of paper or the body's skin can block it, so it does not constitute a greater harm to the human body.

β-ray is a charged, high-speed running particle. Its ionization ability is slightly less than α-ray. But its penetrating ability is stronger than α ray. A piece of paper, the clothes or skin of the human body can only make the radiation weaker and cannot completely block it. But a piece of foil can block it.

γ-ray is a kind of electromagnetic wave with a very short wavelength. Its ionization ability is the worst. But its penetration ability is stronger than both of α-ray and β-ray. It can penetrate the body's skin into the body's cells, and destroy the cells within the organization. In a serious case, normal cells will be converted to cancer cells due to the ionizing radiation of γ-ray. Therefore, the monitoring and preventing of γ-ray are particularly crucial. Since γ-ray generally does not present separately and is often accompanied by the ionization processes of α-ray and β-ray, the presence of γ-ray generally indicates the presence of other rays.

X-ray is a kind of photon generated by electron transitions outside the nucleus. Because of its strong penetrating ability, it can penetrate the body's tissues and organs, and often is used for hospital chest X-ray and so on. But long-term exposure to X-ray on the human body can also cause great harm, for example, it not only reduces the number of body's white blood cells, but also causes the decreased of body immunity and even lead to cancer cells.

2.3 Different Approaches to Measure Radiation.

Ionizing radiation refers to the above-described α-ray, β-ray, γ-ray and so on. To measure a variety of radiation, there are three main types of dosimeters: gas ionization chamber, GM counter tube, scintillation counter and semiconductor detector.

1) Gas ionization chamber [8]: There is noble gas storing in the chamber. The high voltage source is connected between anode and cathode as shown in Fig. 2.1. When it works, the incident ionizing radiation impacts rare gas and produce electrons and positive ions. Under the strong electric field, these charges will move to positive and negative poles separately and form a small current which can be detected by an electrical current measuring device. The magnitude of the current is proportional to the dose rate. The gas ionization chamber has the advantages of simple structure and good energy response. But it needs to apply high voltage and quite a complex signal processing circuit. In addition, it has a low sensitivity and is difficult to be integrated into a chip.

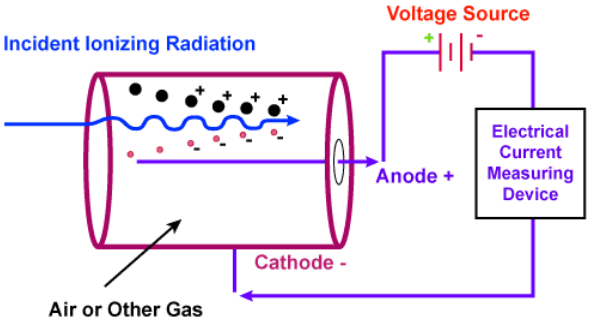


Fig. 2. 1 Gas ionization chamber [8].

2) Geiger Muller (GM) counter tube: GM counter tube has the same structure with the gas ionization chamber as shown in Fig. 2.2. But there is a stronger electric field around the anode wire. At this point, the ionization caused by the incident particle forms an avalanche along the entire anode wire, while the amplitude of the output voltage pulse is independent of the energy and nature of the incident particle. Besides, it cannot count quickly and requires

additional high voltage. The energy and species of particles cannot be identified. It's hard to scale down.

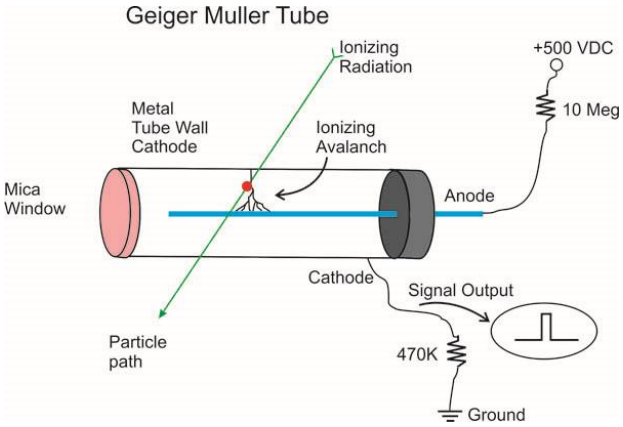


Fig. 2. 2 GM counter tube [9].

3) Scintillation counter: Scintillator counter detects ionizing radiation through the flash of ionizing radiation in some special materials such as sodium-lodide crystal as shown in Fig. 2.3. It is also one of the most widely used detectors for measuring ionizing radiation. The energy resolution is still lower than the semiconductor detector.

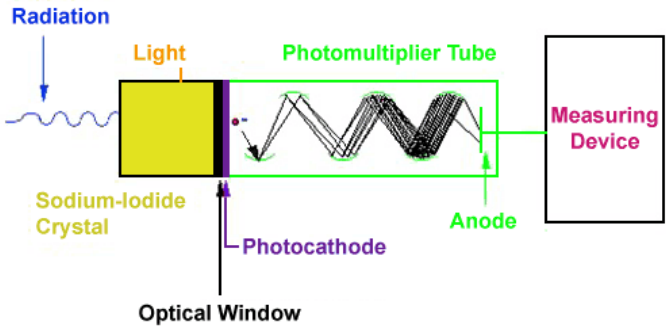


Fig. 2. 3 Scintillation counter [10].

4) Semiconductor detector: Most of silicon particle detectors work, in principle, by doping narrow (usually around 100 micrometers wide) strips of silicon to turn them into diodes, which are then reverse biased. As charged particles pass through these strips, they cause small ionization currents that can be detected and measured.

Most semiconductor detectors are doped into a *p-n* diode, which are then reverse biased as shown in Fig. 2.4. When the charged particles come into this depleted layer, they will produce electron-hole pairs in the sensitive volume of the semiconductor detector. The electron-hole pairs drift under the influence of the external electric field, which will create small current signals. It seems like gas ionization chamber. But it does not need high voltage supply and can be integrated into a chip.

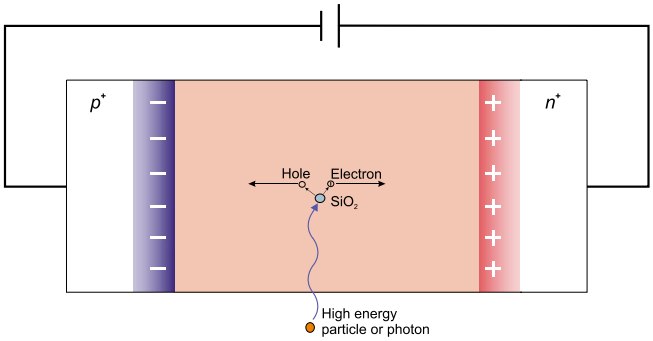


Fig. 2. 4 Semiconductor detector

2.4 MOSFET Dosimeter Design Approaches

In this part, different MOSFET dosimeters approaches are presented. They are classified into single-poly gate devices: RADFET dosimeter with thick oxide devices. Double-poly devices: FGRADFET dosimeter. Single-poly FGRADFET dosimeter.

1. Single-poly RADFET dosimeter: A single-poly *n*-type RADFET sensor structure shows in Fig. 2.5. The gray layer is a SiO_2 layer, which can sense the ionizing radiation as described in Fig. 2.4. The electron-hole pair induced by ionizing radiation will move towards bulk and gate separately, which will cause the variation of source current and threshold voltage. Therefore, the dose rate can be inferred by two methods. The first one is for detecting the change of source current. The second one is to measure threshold voltage variation. The first method is the simplest way but is independent of temperature. The read circuit of second way is shown in Fig. 2.6. Gate and Drain are connected to Ground. Source and bulk are connected to the ideal current source, the threshold voltage is the voltage drop between Source and ground (Gate voltage). The principle of detecting radiation for Single-poly RADFET dosimeter is to measure the variation of threshold voltage (V_{th}) as described in [11]. Electron-holes pair will be produced in silicon dioxide (SiO_2) under

Fig. 2. 5 The structure of single-poly *p*-type RADFET sensor [12].

Fig. 2. 6 A read circuit of single-poly *p*-type RADFET [13].

the gate when incident particles impact the oxide layer. The electrons are very flexible in SiO_2 and quickly move to the anode interface. In contrast, holes may be trapped within the SiO_2. Therefore, the change of V_{th} is relevant to the increase of trapped positive charges in the oxide layer Q_{ot} and the interface Q_{it}:

$$\nabla V_{th} = -\frac{\nabla Q_{ot} + \nabla Q_{it}}{C_{ox}} \tag{2.1}$$

C_{ox} is the oxide capacitor below the gate and it is inversely proportional to the thickness of the oxide layer. As the development of IC technology, the dimension of devices quickly shrinks. The thickness of the oxide layer also becomes smaller and smaller, which cause the increase of C_{ox} value. Therefore, the variation of the threshold is smaller for both of NMOS and PMOS, which leads to the lower of the sensitivity of single-poly RADFET.

2. Double-poly FGRADFET dosimeter: The theory of FGRADFET to sense radiation is same with the gas ionization chamber. Its structure is shown in Fig. 2.7 [36]. Before it works, it is charged by Fowler-Nordheim tunneling process through injector gate, which makes charges storing in the floating gate. When ionizing radiation comes in and impacts the field oxide, the electron-hole pairs will be produced likes the theory of RADFET dosimeter. The electrons quickly move to the floating gate and combine with positive charges in there. The decrease of positive charge Q_{fg} in floating gate will lead to the drop of the floating gate voltage V_{fg}:

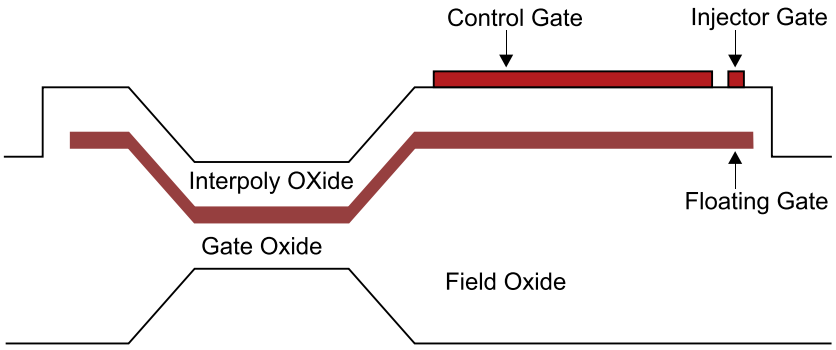


Fig. 2. 7 Structure of FGRADFET in cross-section.

$$\nabla V_{fg} = \frac{\nabla Q_{fg}}{C_T} \tag{2.2}$$

C_T is the total capacitor around the floating gate. The radiation dose rate can be detected by measuring the variation of floating gate voltage. This would be considered as a better way than singly-poly RADFET to detect ionizing radiation because it is not affected by the shrink of transistor's size. However, there is nearly no double-poly technology for present small size transistors.

1) Single-poly FGRADFET dosimeter: The structure of Single-poly FGRADFET is modified by removing the second gate of Double-poly FGRADFET depicted in Fig. 2. 8. The principle for single-poly FGRADFET to detect rays is similar with double-poly FGRADFET. The only difference is the structure of this dosimeter as it is presented in Fig. 2. 9.

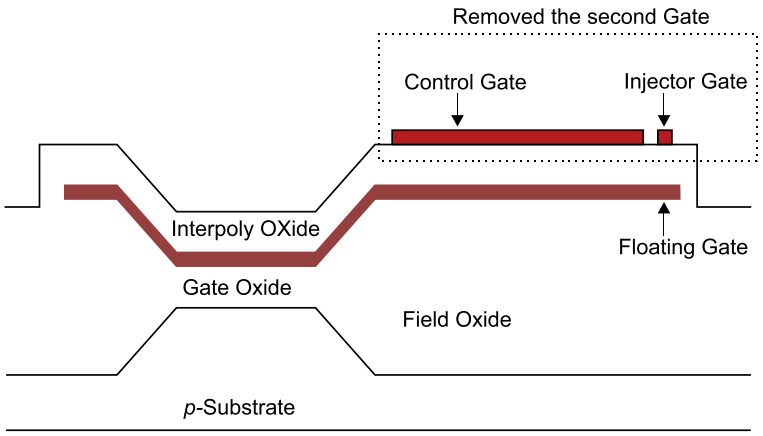


Fig. 2. 8 Cross section of modified FGRADFET structure [14].

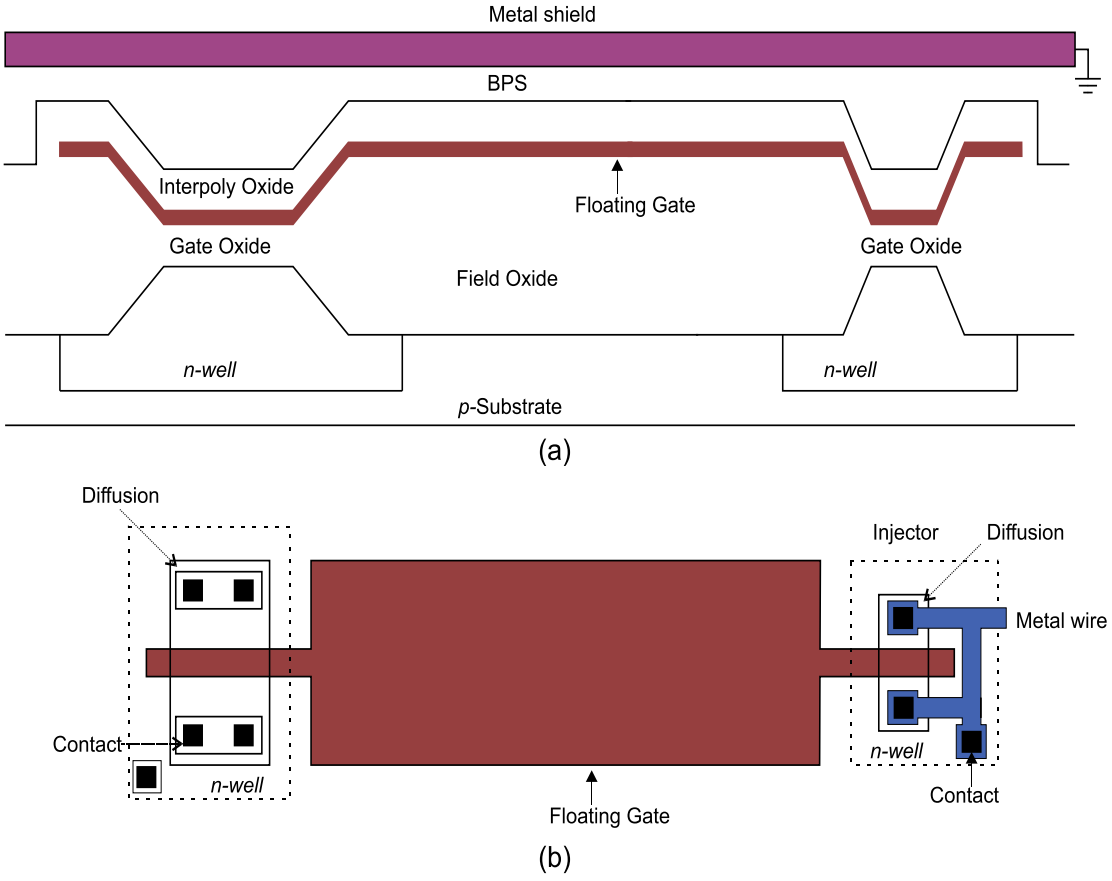


Fig. 2. 9 Single-poly FGRADFET

(a) Cross section view of the basic structure. The left one is a p-type FGRADFET transistor, and the right one is a shorted PMOS transistor to work as an injector. This FGRADFET is covered by a Boro-phosphoro-silicate (BPS) layer and a metal to protect the FGRADFET sensor and reduce noise from the environment. (b) Top view showing the injection electrode. The left part is a p-type FGRADFET transistor, and the right part is an injector simple layout. The drain, source and body of the injector are shorted together, and connect to a pulse voltage to get a positive charge.

The single-poly FGRADFET has a big floating gate (Polysilicon) area as an antenna to sense the incident rays. The relationship between ionizing radiation and the floating gate voltage is same with double-poly FGRADFET dosimeter as shown in equation 2.2. Since the control

gate is removed and total capacitance will reduce, the sensitivity of single-poly FGRADFET is higher than double-poly FGRADFET. In this research, single-poly FGRADFET is chosen to work as the radiation sensor.

Chapter 3 Floating Gate Radiation Field Effect Transistor (FGRADFET) Design

To simulate floating gate transistor in Cadence software, the simulation model of FGMOST is needed. This Chapter will show the whole process for designing FGMOSFET model.

3.1 FGMOSFET

FGMOSFET has been used as non-volatile storage devices such as EEPROM and EPROM in digital circuit design for many years [16]. The primary distinction in geometry between the FGMOSFET and MOSFET is the floating gate beneath the control gate. Fig. 3. 3(a) shows the top mask layout view of the FGMOSFET device fabricated on a lowly-doped p-type substrate. The floating gate (n-poly1) is fully surrounded (insulated) by silicon dioxide (SiO2) and there are no resistive connections to the gate (n+-poly2) and substrate (body) as shown in the cross-section view in Fig. 3. 3(b) [17]. However, the charge can be stored and modified in the floating gate by trapping electrons and holes through Hot-Electron Injection and Fowler-Nordheim Tunneling process respectively [18]- [23].

The characteristics of the FGMOSFET are similar to those of the MOSFET before it is charged. Once the process of charging is completed, the electric field produced by the stored holes or electrons on the floating gate has the same properties as those of the electric field produced by the gate voltage. It can force the majority carriers in the substrate away from the nearby oxide-silicon interface of the substrate under the SiO2 and attract minority carriers to form an inversion layer [24]. As a result, the FGMOS can still operate in the strong inversion saturation region by relying on floating gate charge even though the gate voltage is tiny or zero.

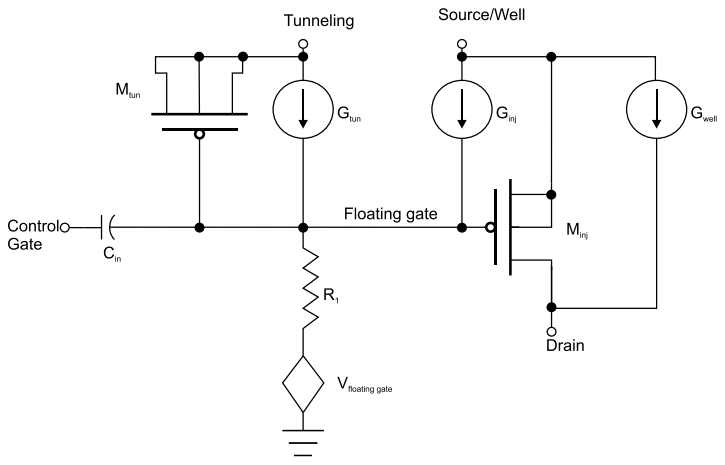


Fig. 3. 1 FGMOSFET macro model.

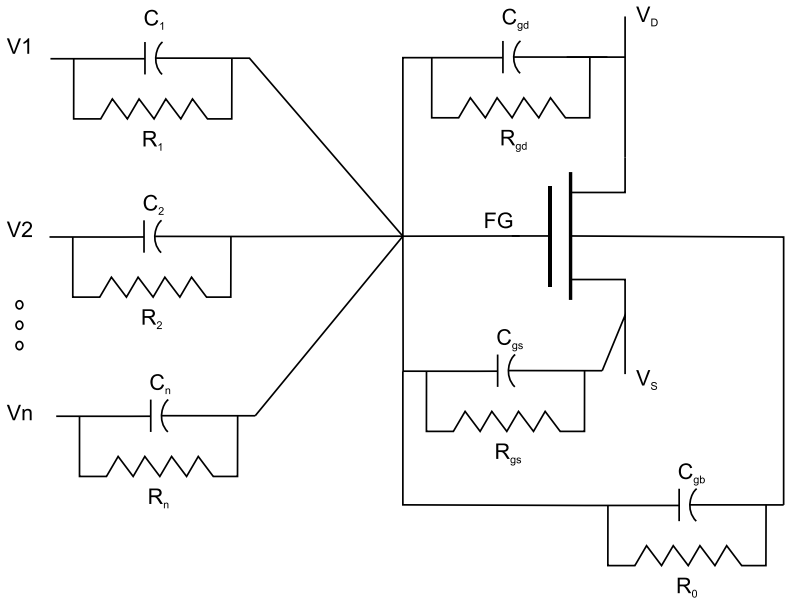
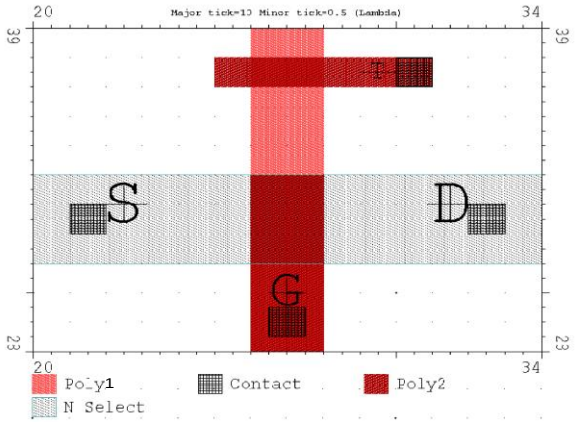


Fig. 3. 2 FGMOSFET simulation model.

In the literature review, there are lots of modeling methods for simulation FGMOSFET. But most of these models use macro models which are not suitable for simulation with other components in IC design environment. For example, a FGMOSFET macro model described in [30] is shown in Fig. 3. 1. G_{tun} and G_{inj} model the tunneling current and injecting current, respectively; G_{well} models impact ionizing current. M_{tun} is a shorted PMOS which is used to charge the Floating gate. $V_{floating\ gate}$ is a voltage source that acts as the voltage source stored in the floating gate. Another popular FGMOSFET model is shown in Fig. 3. 2 [24][25]. C1 to C_n are the gate to floating gate capacitances. C_{gd}, C_{gs} and C_{gb} are the gate to drain, gate to source and gate to bulk capacitances. R1 to Rn is used here to avoid convergence. The value of R1 to Rn is very large so that the current does not flow through these resistances. This model can be placed directly into the simulation. However, we cannot get the accurate simulation result match the floating gate transistor with these macro models. The FGMOSFET model should be built with equations.

At present, there are no precise FGMOSFET models in the analog simulation library of most IC design CAD environments [23] [27]. Hence, it is necessary to create a suitable FGMOSFET circuit model that can be instanced directly in commercial VLSI CAD software tools like Cadence. This will provide a seamless analog circuit simulation and design platform employing the floating gate transistors just like normal MOSFETs and other circuit components.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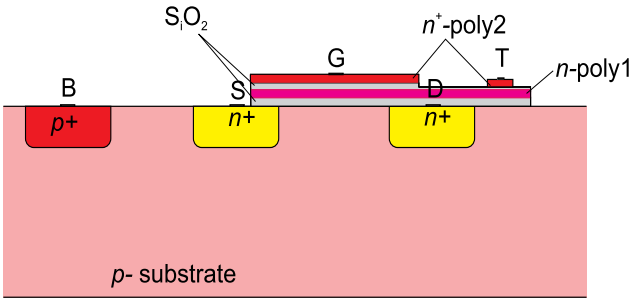
(a)


S_iO_2
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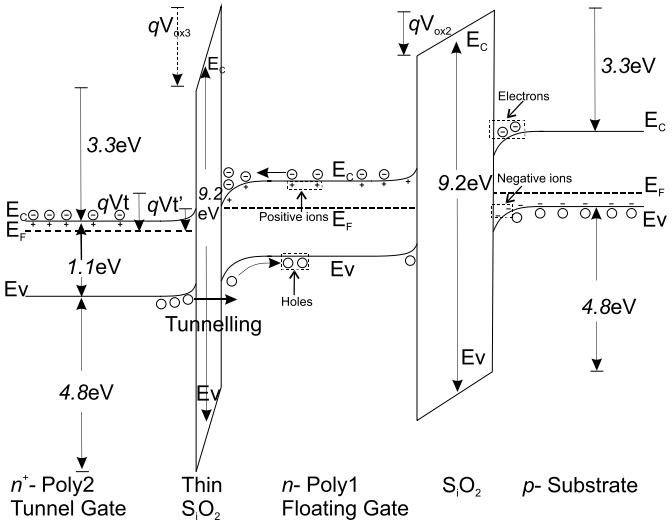
(b)


qV_{ox3}
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E_c
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Electrons
E_c
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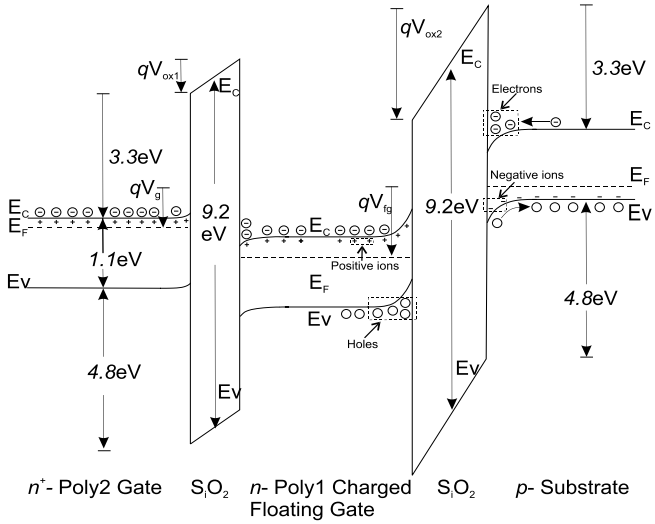
E_c
qVt
qVt'
9.2 eV
Positive ions
E_F
9.2eV
Negative ions
E_F
E_F
Ev
1.1eV
Ev
Holes
Ev
Tunnelling
4.8eV
Ev
Ev
4.8eV
n^+- Poly2
Tunnel Gate
Thin
S_iO_2
n- Poly1
Floating Gate
S_iO_2
p- Substrate

(c)

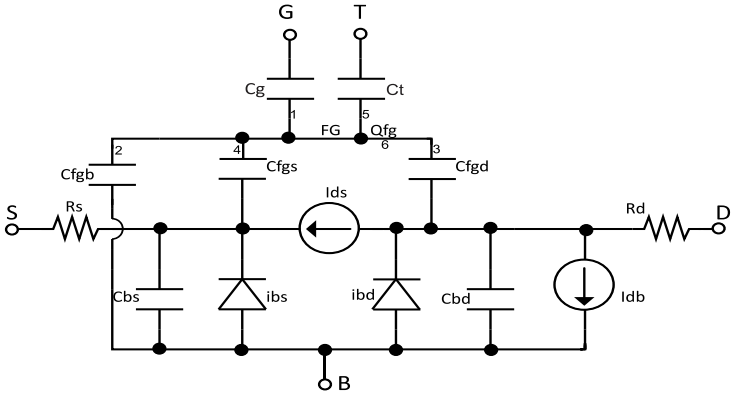


(d)

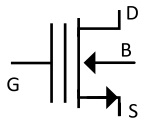
Fig. 3. 3 An n-type FGMOSFET's layout, cross-section and energy band diagram.

(a) Layout. (b) Cross-section. (c) Energy band diagram for Fowler-Nordheim tunneling process. The tunneling voltage (Vt) is applied from n+-poly2 tunnel gate to the p-substrate. The voltage drop across the oxide between poly2 and n-poly1(the floating gate) is the tunneling voltage (Vt'=Vt-Vfg), which can force the holes to tunnel through the thin dioxide to the floating gate (or valence electrons move to poly2 tunnel-gate). (d) Energy band diagram for charged FGMOSFET in the vertical cross-sectional direction (from gate to substrate) with a small gate voltage (Vg) applied from poly2 gate to the substrate. In the floating gate, a relatively large floating gate voltage (Vfg) is obtained. It is constituted by stored (trapped) hole charge and part of Vg.

In this presented model, FGMOSFET has five terminals, which are gate, tunnel-gate, drain, source and bulk. The layout, cross-section, and energy-band diagrams of an n-type FGMOSFET are depicted in Fig. 3. 3 [20] [30] [31]. The gate and the tunnel-gate are fabricated using highly-doped n+-type polysilicon (Poly2). On the other hand, moderately doped n-type polysilicon (Poly1) forms the floating gate. An 8-10 V potential is applied to the tunnel-gate with respect to the substrate (bulk) for about 1ms to charge the floating-gate through Fowler-Nordheim hole tunneling from tunnel-gate to floating gate. The consequent net stored (trapped) positive charge on the floating-gate creates the



(a)



(b)

Fig. 3. 4 FGMOSFET equivalent circuit and its symbol.

(a) An n-channel FGMOSFET equivalent circuit, where, Idb is the drain-to-bulk (body) impact ionization current, while, ibd and ibs are respectively bulk-to-drain and bulk-to-source reverse-biased n-p junction diode currents. Also, Ids is the drain-to-source channel current, Rs and Rd are respectively source and drain area resistances, while, Cbs and Cbd are source and drain diffusion junction capacitances. Finally, Cg, Ct, Cfgb, Cfgs and Cfgd are floating-gate to gate, tunnel-gate, bulk (body), source and drain parallel-plate capacitances respectively. (b) The n-channel FGMOSFET symbol. The T-gate is assumed to be an internal pre-setting terminal to apply tunnel voltage and pre-charge floating gate by the desired amount before being employed in the simulation. Hence the T terminal is made externally invisible in the device symbol.

same channel carrier mechanism as that due to a gate-voltage (and hence gate-charge). Both phenomena produce an electric field, which attracts carriers of opposite charge to the substrate-oxide interface, providing a conductive channel between the source and the drain. Normally, the stored (trapped) charge on the floating gate can be retained for a nominal period of around 10 years (≈ 88K hours). However, the quantity of the stored charge will reduce with time due to leakage and other environmental effects caused by temperature, electrostatic-fields and small-dose radiation. Thus, it is important to fabricate a tunneling terminal that can be employed to charge (rejuvenate) the floating gate as shown in Fig. 3. 3(b). The energy-band diagram during the Fowler-Nordheim tunneling process is shown in Fig. 3. 3(c) for the applied tunneling voltage Vt between the tunnel-gate (terminal) and the substrate. The voltage drop between the poly2 tunnel-gate and the poly1 floating-gate (with voltage Vfg) is the tunneling voltage (Vt'=Vt-Vfg) which can force holes to tunnel through the thin-oxide to the floating-gate (by virtue of valence electrons traveling into the poly2 tunnel-gate). Fig. 3. 3(d) depicts the energy-band diagram for the floating-gate charged FGMOSFET for an applied voltage between the poly2 gate (normal MOS gate) and the substrate. A small gate-voltage (Vg) is applied between the poly2 gate and the substrate. As a result, a relatively large poly1 floating-gate voltage (Vfg) can be obtained as a consequence of the stored net positive charge on the floating gate. It is constituted by the net charge due to trans-located holes (during tunneling) and a part of the applied gate-voltage Vg. According to Shichman-Hodges MOSFET Model [29], the n-type FGMOSFET equivalent circuit can be drawn as shown in Fig. 3. 4 (a) with its symbol depicted in Fig. 3. 4 (b). The gate and the tunnel-gate voltages are capacitively coupled to the floating gate.

3.2 FGMOSFET Mathematical Model

3.21 Floating-gate Voltage

In Fig. 3. 4(a), at the FG node, in accordance with the superposition of electrostatically induced voltages at the floating-gate, the expression [32] for the floating-gate voltage can be extracted in general as:

$$V_{fg} = V_1 + V_2 + V_3 + V_4 + V_5 + V_6 \tag{3.1}$$

Where the numbers marked adjacent to the top capacitor plates connecting to the floating-gate indicate the induced voltages corresponding to the parallel-plate capacitances that intervene the respective node voltages surrounding the floating-gate. The number 6 labeled on the floating-gate attributes to the contribution due to pre-stored tunnelling charge on the floating-gate. Hence, V_6 corresponds to the induced voltage due to the pre-set stored (trapped) charge Q_{fg} on the floating-gate with respect to the total capacitance C_T looking from the floating-gate. The electrostatically induced voltage contributions in (3.1) are thus:

$$V_1 = \frac{C_g}{C_T} V_g,\ V_2 = \frac{C_{fgb}}{C_T} V_b,\ V_3 = \frac{C_{fgd}}{C_T} V_d,\ V_4 = \frac{C_{fgs}}{C_T} V_s,\quad V_5 = \frac{C_t}{C_T} V_t \qquad \text{and, } V_6 = \frac{Q_{fg}}{C_T}.$$

Where, V_g, V_b, V_d, V_s and V_t refer to voltages at the gate (terminal G), bulk (body), drain, source and tunnel-gate surrounding the floating gate with respect to ground. Also,

$$C_T = C_g + C_{fgb} + C_{fgd} + C_{fgs} + C_t \tag{3.2}$$

Where C_g, C_{fgb}, C_{fgd}, C_{fgs} and C_t are respectively the gate-to-floating-gate, floating-gate-to-body, floating-gate-to-drain, floating-gate-to-source and tunnel-gate-to-floating-gate parallel-plate capacitances respectively.

Next, expanding (3.1):

$$V_{fg} = \frac{C_g}{C_T} V_g + \frac{C_{fgb}}{C_T} V_b + \frac{C_{fgd}}{C_T} V_d + \frac{C_{fgs}}{C_T} V_s + \frac{C_t}{C_T} V_t + \frac{Q_{fg}}{C_T} \tag{3.3}$$

It is worthwhile to note that, $C_g >> C_{fgb}$, C_{fgd} and C_{fgs}; also, $V_t C_g \gg C_{fgb}, C_{fgd}$ is zero when floating gate pre-charging is complete. Hence, (3.3) can be approximately simplified as:

$$V_{fg} = \frac{C_g}{C_T} V_g + \frac{Q_{fg}}{C_T} \tag{3.4}$$

Where Q_{fg} is the hole charge from the tunnelling process as depicted in Fig. 3. 3(c). It can thus be calculated from the tunnelling current expression [23], [31], given by:

$$I_{tun} = \rho A E_{Tun}^2 e^{-\frac{\theta}{E_{Tun}}} \tag{3.5}$$

Where ρ and θ are fit parameters, A is the tunnel-gate injection area ($A=W_T L_T$, with W_T and L_T being width and length of tunnel gate *masking* the floating gate)I_{to}, E_{Tun} is the electric field through thin oxide from tunnel-gate to floating-gate ($E_{Tun}= [V_t - V_{fg}]/T_{ox}$, with *Tox* being the tunnel-gate-to-floating-gate thin-oxide thickness). So that, integrating the tunnelling current for a given tunnelling duration (*t2 - t1*),

$$Q_{fg} = \int_{t1}^{t2} I_{tun}\, dt \tag{3.6}$$

Therefore, the floating gate voltage in (3.4) can be further expressed as:

$$V_{fg} = \frac{C_g}{C_T} V_g + \frac{\rho W_T L_T}{C_T T_{ox}^2} \int_{t1}^{t2} (V_t - V_{fg})^2 e^{-\frac{\theta T_{ox}}{V_t - V_{fg}}} dt \tag{3.7}$$

Where, (3.7) is an implicit equation that can be solved iteratively to determine the final floating-gate voltage at the end of the charging duration.

3.22 Drain-to-source Current

The floating-gate voltage is a function of the control-gate voltage and the tunneling voltage. Combining the effects of the terminals G and T into the terminal FG as the composite gate terminal, we can create another n-channel FGMOSFET equivalent circuit model as shown in Fig. 3. 5. Here the composite voltage of the terminal FG is determined by (3.7).

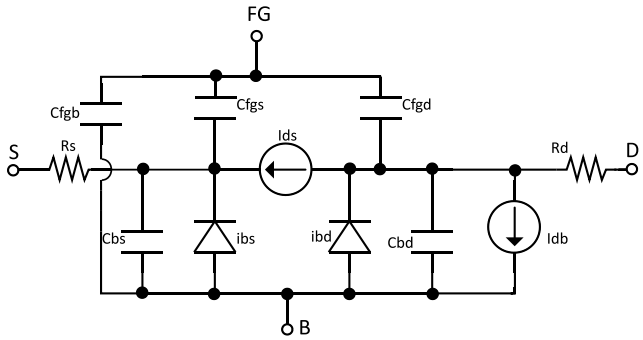


Fig. 3. 5 Simplified n-channel FGMOSFET Equivalent circuit with the effect of control-gate and tunnel-gate consolidated into the floating-gate.

Using the Shichman-Hodges MOSFET Model [29] to analyse the circuit in Fig. 3. 5, along-with, V_{fgs} =(V_{fg}-V_s), we can partition the regions of operation for the n-channel FGMOSFET as follows:

Subthreshold region (V_{fgs} - $V_{thf} \leq 0$):

$$I_{ds} = 0 \tag{3.8}$$

Triode region ($V_{ds} \leq V_{fgs} - V_{thf} > 0$):

$$I_{ds} = \mu_n C_{ox} \frac{W}{L - 2L_D}(1 + \lambda V_{ds})(V_{fgs} - V_{thf} - \frac{V_{ds}}{2})V_{ds} \tag{3.9}$$

Saturation region ($V_{ds} > V_{fgs} - V_{thf} > 0$):

$$I_{ds} = \frac{\mu_n C_{ox}}{2} \frac{W}{L - 2L_D}(1 + \lambda V_{ds})(V_{fgs} - V_{thf})^2 \tag{3.10}$$

where μ_n is the electron mobility; V_{thf} is the n-channel FGMOSFET threshold voltage; C_{ox} C_{ox} is the oxide capacitance per unit area, calculated from oxide thickness (t_{ox}) below the floating-gate and the oxide permittivity ($\mathcal{E}_{ox}$)ε_{ox}): $C_{ox} = \mathcal{E}_{ox}/t_{ox}$ $C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$; L_D is the under-channel lateral S/D diffusion, and, λ is the channel-length modulation constant.

3.23 Transconductance (g_m)

In accordance with the saturation region current in (3.10) and the floating gate voltage V_{fg} in (3.7), we can derive the FGMOSFET design parameter g_m as follows:

$$\begin{aligned} g_m &= \left.\frac{\partial I_{ds}}{\partial V_{gs}}\right|_{0<V_{fgs}-V_{thf}<V_{ds}} \\ &= \frac{C_g}{C_T}\mu_n C_{ox}\frac{W}{L-2L_D}(1+\lambda V_{ds})\left[\frac{C_g}{C_T}V_g + \right. \\ &\left. \frac{\rho W_T L_T}{C_T T_{ox}^2}\int_{t1}^{t2}(V_t - V_{fg})^2 e^{-\frac{\partial T_{ox}}{V_t - V_{fg}}}dt - V_s - V_{thf}\right] \end{aligned} \tag{3.11}$$

Eq. (3.11) shows the effect of the gate-voltage and stored floating-gate charge on the trans-conductance in strong inversion saturation. In the triode region, the trans-conductance is given by,

$$\begin{aligned} g_m &= \left.\frac{\partial I_{ds}}{\partial V_{gs}}\right|_{0<V_{fgs}-V_{thf}\geq V_{ds}} \\ &= \frac{C_g}{C_T}\mu_n C_{ox}\frac{W}{L-2L_D}(1+\lambda V_{ds})V_{ds} \end{aligned} \tag{3.12}$$

The g_m in the triode region varies with the drain voltage [32] and is usually not utilized in trans-conductance amplifiers.

3.24 Output Impedance (r_o)

In a similar way as determining the g_m, the r_o expression for FGMOSFET can also be derived as follows, When $V_{ds} \leq V_{fgs} - V_{thf} > 0$:

$$r_o = \frac{1}{\left.\frac{\partial I_{ds}}{\partial V_{ds}}\right|_{V_{ds} \leq V_{fgs} - V_{thf} > 0}} = \frac{1}{\mu_n C_{ox} \frac{W}{L - 2L_D} \left\{ -\frac{3}{2} \lambda V_{ds}^{\ 2} + [2\lambda (V_{fgs} - V_{thf}) - 1] V_{ds} + V_{fgs} - V_{thf}) \right\}} \tag{3.13}$$

Which is the triode regime resistance of the FGMOSFET for operation as a switch. Also, when, $V_{ds} > V_{fgs}-V_{thf}>0$

$$r_o = \frac{1}{\left.\frac{\partial I_{ds}}{\partial V_{ds}}\right|_{V_{ds} > V_{fg} - V_s - V_{thf} > 0}} = \frac{1}{\frac{\mu_n C_{ox}}{2} \frac{W}{L - 2L_D} \lambda (V_{fg} - V_s - V_{thf})^2} \tag{3.14}$$

For a non-ideal current source (in the strong inversion saturation region. As there is charge stored on the floating gate, V_{fg} is somewhat larger than the gate-voltage of traditional NMOS. Thus, the output impedance of the FGMOSFET is usually less than that of the common MOS transistor.

3.25 Threshold Voltage for FGMOSFET (V_{thf})

Considering similar thin-oxide thickness compared to a normal MOSFET and similar gate-poly material, the threshold voltage required (induced voltage at floating-gate with respect to the source) for strong inversion operation of the FGMOSFET would be similar to that of the normal MOSFET. Hence,

$$V_{thf} = V_{to} + \gamma \left(\sqrt{2\phi_f + V_{sb}} - \sqrt{2\phi_f} \right) \quad , V_{sb} \geq 0 \tag{3.15}$$

where, V_{to} is the threshold voltage when $V_{sb}=0$; γ is the body effect parameter; $\phi_f = \frac{KT}{q} \ln(\frac{N_{sub}}{n_i})$ ϕf =

$\frac{kT}{q}\ln(\frac{N_{sub}}{Ni}$ is the surface inversion potential, which can be calculated from substrate doping (N_{sub}) and intrinsic carrier concentration (n_i).

3.26 Bulk Current

The bulk(body) current is mainly constituted by impact ionization, drain and source reverse biased diodes and other mechanisms. In addition, an occasional tunneling effect occurs when gate-voltage causes carriers to tunnel through the oxide to the substrate due to significant energy band bending. In the FGMOSFET, there are two oxide layers and the device can be in strong inversion for a small gate voltage due to coupled electric fields and corresponding energy levels as shown in Fig. 3.1(d). The tunneling current is usually quite negligible. Hence, the source and drain region reverse-biased diode currents (i_{bd} and i_{bs}) along-with impact ionization current (I_{db}) [30] are only considered for bulk current as shown in the simplified FGMOSFET model in Fig. 3. 5. Thus, the bulk current relationship is given by:

$$I_b = i_{bs} + i_{bd} - I_{db} \quad I_b = i_{bs} + i_{bd} - I_{db} \tag{3.16}$$

$$i_{bs} = is(e^{\frac{V_{bs}}{V_T}} - 1) \tag{3.17}$$

$$i_{bd} = is(e^{\frac{V_{bd}}{V_T}} - 1) \tag{3.18}$$

where ***is*** is a reverse bias saturation current and V_T is thermal voltage (≈ 25.85mv @ 300K). Also, I_{db} is a drain-to-bulk current produced by impact ionization [30] given by:

$$I_{db} = \eta I_{ds}(\alpha V_{ds} - \beta V_{dfg} + V_{thf})e^{\frac{-\sigma}{\alpha V_{ds} - \beta V_{dfg} + V_{thf}}} \tag{3.19}$$

Where $\eta, \alpha, \beta \; and \; \sigma$ are fit parameters and V_{dfg} is the drain-to-floating gate voltage. Hence the total bulk current is given by:

$$I_b = is(e^{\frac{V_{bs}}{V_T}} - 1) + is(e^{\frac{V_{bd}}{V_T}} - 1) - \eta I_{ds} \cdot (\alpha V_{ds} - \beta V_{dfg} + V_{thf})e^{\frac{-\sigma}{\alpha V_{ds} - \beta V_{dfg} + V_{thf}}} \tag{3.20}$$

3.3 Simulation and Verification Results

In order to verify the simplified model, all the parameters and equations were explored, tested and adjusted on the MATLAB platform. The MATLAB code is shown in Appendix B. These equations were then coded in Cadence Verilog-A script [32] [33]. The flow chart of the Verilog-A functional program is shown in the Fig. 3. 6. The symbol of Fig. 3. 4(b) is generated by the compiled code (Appendix C). Fig. 3. 7 demonstrates the generated FGMOSFET symbol and its properties in a Cadence pop-up window. This symbol can then be instanced from a menu as an IC cell in similarity with the other symbols that already exist in the analog library. Fig. 3. 8 shows the consequent Cadence Verilog compiled simulation results for the entire charging process of tunneling holes into the floating gate. From 0-4ms, the gate voltage is 100mv and the tunneling voltage is 0mv. Because of capacitive coupling, the floating-gate attains a voltage of 86.707mv as shown in Fig. 3. 8 (b). For the interval between 4ms -5ms, a tunneling voltage of respectively 8.4V, 8.6V, 8.8V, 9.0V and 9.2V is applied in 0.2V steps (as shown in Fig. 3. 8 (a)), as 5 separate charging events. In each case, the applied tunnel-gate voltage immediately reflects a rising floating-gate voltage until the end of the tunneling pulse-period when it becomes constant. After the 5 ms time-instant, tunneling voltage is removed and the charging process is accomplished. Now, the charge has been trapped in the floating gate and its voltage remains unchanged. The simulation parameters for the iterative solution of the tunneling process in (3.17) using Cadence Verilog-A (Appendix A 1) are shown in Table 3.1. The achieved floating-gate voltage in each case is shown in Fig. 3. 8(b).

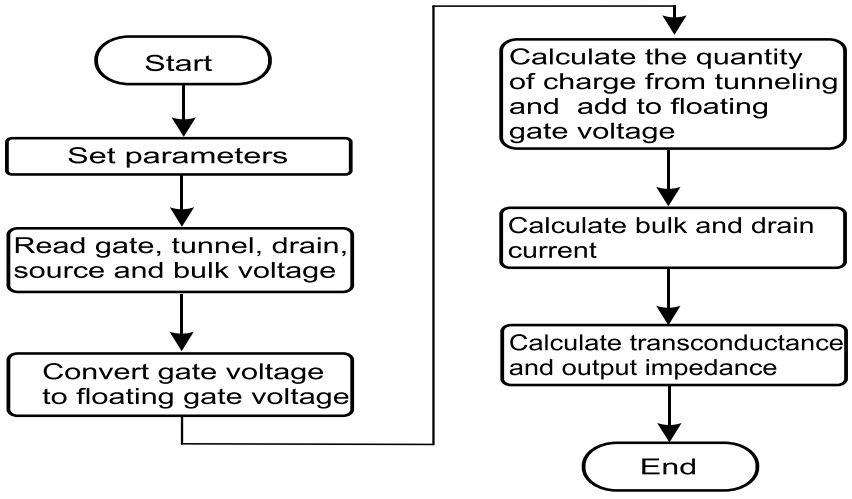


Fig. 3. 6 Flow chart of Verilog-A code.

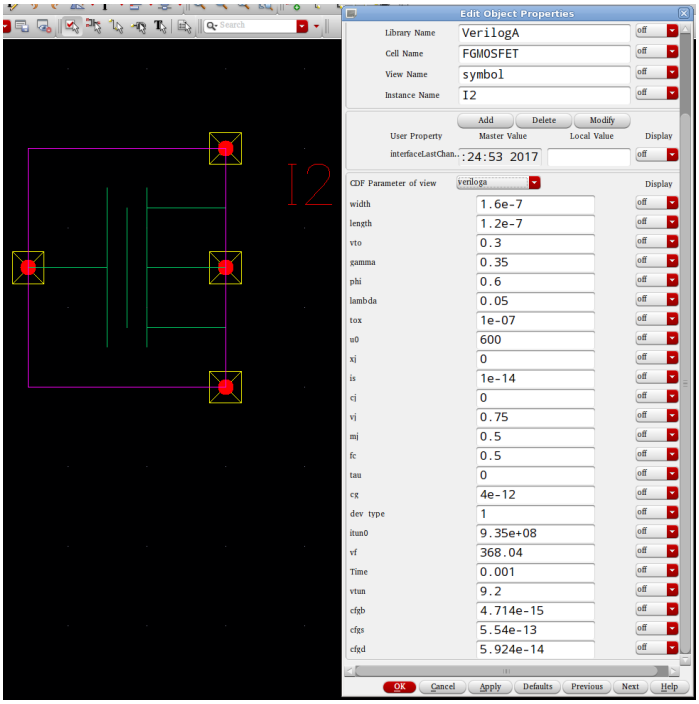


Fig. 3. 7 Cadence integrated FGMOSFET symbol and its properties in a pop-up window.

TABLE 3. 1 Model Parameters for the Charging Process

Parameter	Value	Description
C_g	4pF	Gate-floating gate overlap capacitance
C_T	4.6132pF	Total capacitance surrounding FG
ρ	2.02E+5	An area fit parameter
W_T	160nm	The width of tunnel gate injection area
L_T	120nm	The length of tunnel gate injection area
T_{ox}	22Å	Thin oxide thickness of tunnel gate
θ	1.73E+11	An exponential coefficient

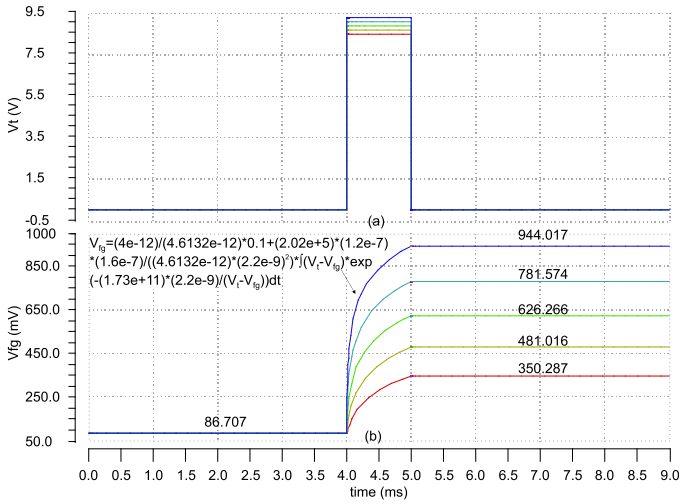


Fig. 3. 8 Simulation of the Fowler-Nordheim tunneling process

(a) a 1 ms tunneling pulse is applied at the T-gate for the interval between 4 ms and 5 ms time instants of amplitudes 8.4V to 9.2V in increments of 0.2V, (b) the resulting sequence of floating-gate voltages due to the corresponding stored charge.

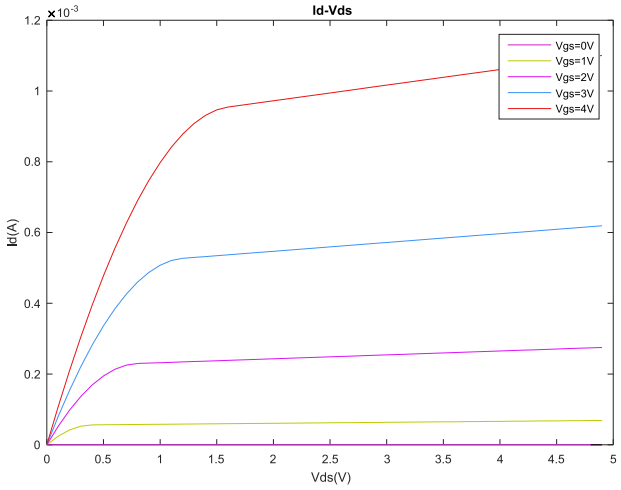


Fig. 3. 9 Uncharged FGMOSFET drain-to-source current versus drain-to-source voltage for 0≤Vgs≤4.0V in MATLAB

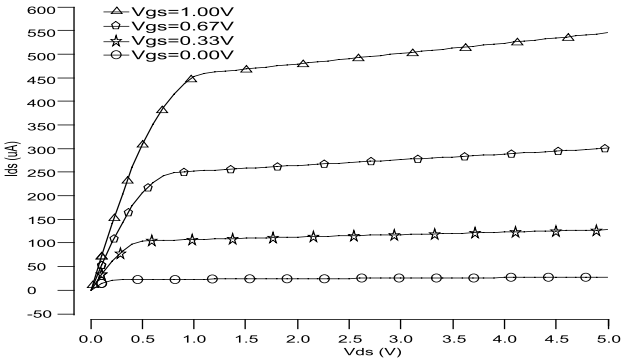


Fig. 3. 10 Charged FGMOSFET drain-to-source current versus drain-to-source voltage for 0≤Vgs≤1.0V.

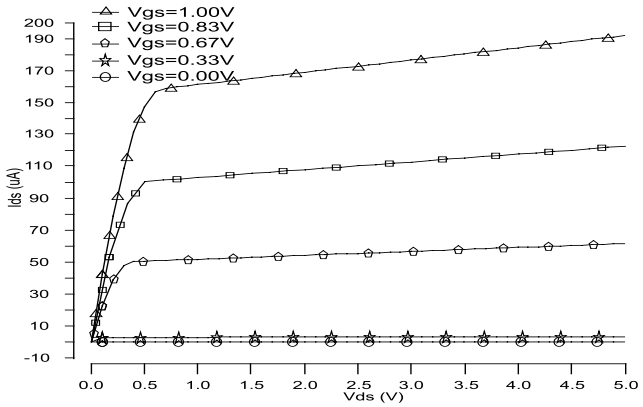


Fig. 3. 11 Uncharged FGMOSFET drain-to-source current versus drain-to-source voltage for 0≤Vgs≤1.0V.

Following sub-section *III.E* threshold voltage for a NMOS device (thin-oxide device) in Global Foundries 130 nm CMOS technology has been employed as the V_{thf} for the n-channel FGMOSFET device. Fig. 3. 10 shows the charged FGMOSFET's drain-to-source current variation with drain-to-source voltage. In this case of Fig. 3. 10, the FGMOSFET has been charged by a 9.2V tunneling pulse voltage for 1ms before simulating the I_{DS} vs. V_{DS} behavior. These models are built and transferred from MATLAB code and simulated in Cadence. Therefore, they are matched very well between Fig. 3. 9 and Fig. 3. 11. The characteristics of the charged FGMOSFET indicate that it can operate in strong inversion saturation even for very small gate voltages. This is a major difference between FGMOSFET and MOSFET. When the FGMOSFET is uncharged, it has similar characteristics as the traditional MOSFET as shown in Fig. 3. 11. The only difference is that the acquired floating-gate voltage ($=\frac{C_g}{C_T}V_g$) is smaller than the conventional MOSFET regular gate voltage ($=V_g$). Thus, the uncharged FGMOSFET can also be treated as a normal transistor. The relationships between the drain current and gate voltage are also shown in Fig. 3. 12 and Fig .3. 13 respectively for charged and uncharged FGMOSFET. When the drain voltage is kept constant, the drain-to-source current increases along with the gate voltage. This is because the rising gate voltage will lead to an increase in the channel charge. Comparing

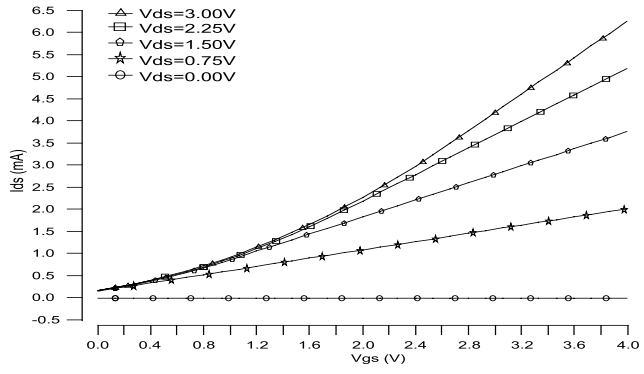


Fig. 3. 12 Charged FGMOSFET drain-to-source current versus gate voltage for 0≤Vds≤3.0V.

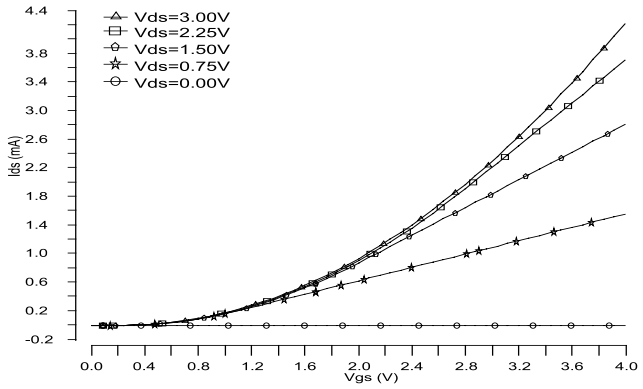


Fig .3. 13 Uncharged FGMOSFET drain-to-source current versus gate voltage for 0≤Vds≤3.0V.

Fig. 3. 12 and Fig .3. 13, it can be noticed that the charged FGMOSFET's drain current variation has a wider linear range than that of the uncharged FGMOSFET for a gate voltage variation in the range 0-1V. This is because the channel inversion layer develops at a larger gate voltage in the case of an uncharged FGMOSFET. Moreover, the charged FGMOSFET's drain current is larger than that of the uncharged FGMOSFET for the same gate and drain voltages. The above differences between charged and uncharged FGMOSFET are attributable to the band-structure shown in Fig. 3. 3 (d). Fig. 3. 14 shows the simulation results of bulk (body) current variation with drain voltage, with body @ 0V, @ -2V, @ -4V and @ -6V with respect to the source (@ground).

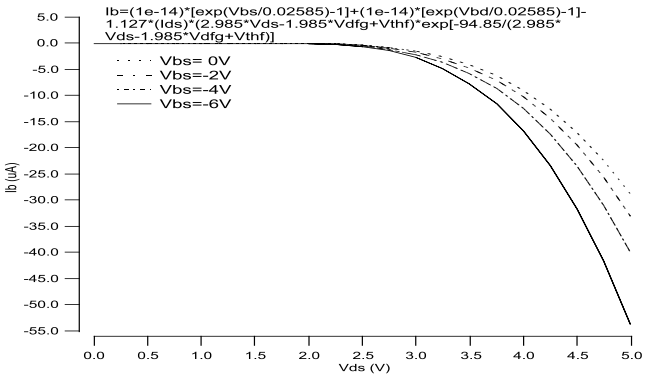


Fig. 3. 14 N-channel FGMOSFET bulk (body) current versus drain voltage for Vbs=0V, -2V, -4V and -6V respectively.

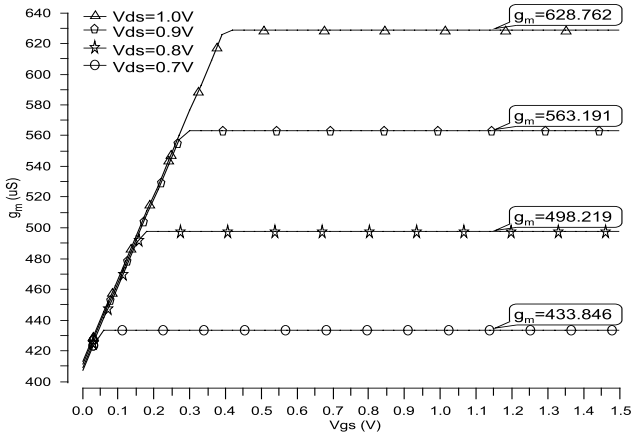


Fig. 3. 15 Charged FGMOSFET transconductance (g_m) versus gate-voltage for Vds= 0.7V, 0.8V, 0.9V and 1V.

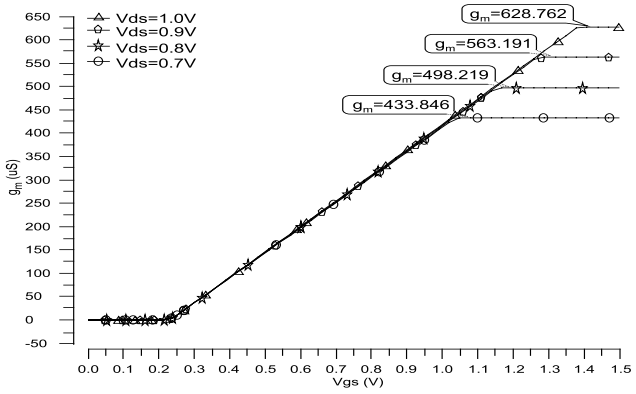


Fig. 3. 16 Uncharged FGMOSFET transconductance (gm) versus gate voltage for Vds= 0.7V, 0.8V, 0.9V and 1V.

The contribution of the bulk-to-drain and bulk-to-source reverse diode current are always very small as they approach the low reverse saturation current values in each case. The effect of impact ionization is also very small for lower drain voltages such as in the range 0V - 2V. As the drain voltage increases in the range 2V - 5V, the impact ionization current from drain-to-bulk becomes more and more pronounced as shown in Fig. 3. 14. When the impact ionization current becomes more significant, the parasitic power drain of the FGMOSFET engulfs a higher proportion of the overall device power budget. Hence, a voltage greater than 2.5V is normally not suitable to be employed at the drain terminal in most cases. Also, for the same drain voltage (for Vds > 2V) the impact ionization current increases for higher negative values of Vbs due to its effect on the capacitively coupled floating-gate voltage and consequent change in the value of V_{dfg}.

Fig. 3. 15 and Fig. 3. 16 illustrate the variation of the FGMOSFET's trans-conductance (g_m). The simulation results reflect the transconductance expressions in (3.11) and (3.12) for saturation and triode regions of operation respectively. When $V_{fgs} - V_{thf} = V_{ds}$, just at the crossover point of saturation and triode regions, *gm* reaches its maximum value. It can be observed, for

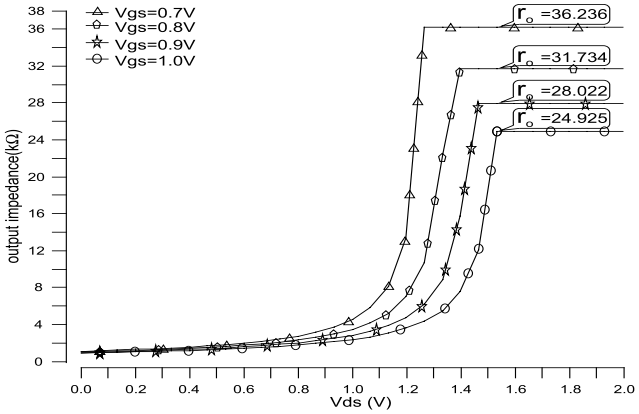


Fig. 3. 17 Charged FGMOSFET output impedance versus gate voltage for Vgs=0.7V, 0.8V, 0.9V and 1V.

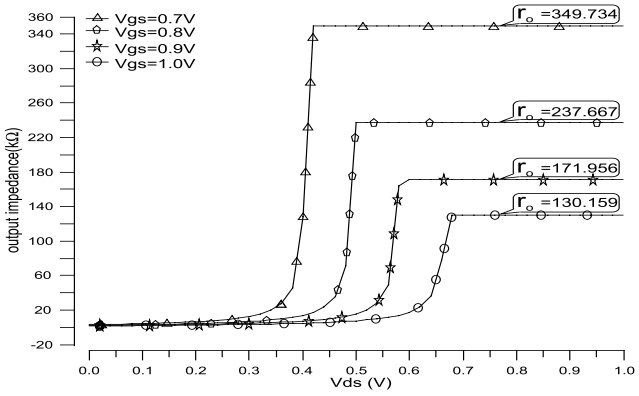


Fig. 3. 18 Uncharged FGMOSFET output impedance versus gate voltage for Vgs=0.7V, 0.8V, 0.9V and 1V.

example (@ Vds=1V), that the gate voltage (≈ 0.35V) needed by the charged FGMOSFET to arrive at its maximum g_m value is smaller than that for the uncharged FGMOSFET (≈ 1.45V). For smaller values of Vds, the gate voltage needed to arrive at the maximum g_m is even smaller, with that required for the charged FGMOSFET being always smaller than that needed for the uncharged FGMOSFET. In both cases, the device is transitioning from saturation to the triode region at this gate voltage. In other words, the charged floating gate device requires a lower gate voltage to obtain the same g_m than the normal single-poly transistors. However, the device is usually not biased to operate at maximum g_m when employed in a trans-conductance amplifier in order to ensure small-signal operation within the saturation region.

Fig. 3. 17 and Fig. 3. 18 depict the output impedance (r_o) of the single FGMOSFET. As per discussion based on (3.13) and (3.14), the r_o of charged FGMOSFET is smaller than that of the normal MOSFET and the uncharged FGMOSFET. This is because, for the same applied bias gate-voltage the floating-gate voltage is larger in the case of a charged FGMOSFET compared to an uncharged FGMOSFET resulting in a larger bias drain-current and consequently a smaller output impedance. It can also be noticed that for the same Vgs, the charged FGMOSFET requires a larger Vds to stay in saturation compared to an uncharged FGMOSFET.

The complete process of building a FGMOSFET model, its simulation and verification have been described in detail. As a first step, theoretical analysis of FGMOSFET, its equivalent circuit and device equations are discussed. Next, the equations are modified and tested in MATLAB for a deeper understanding of the FGMOSFET. Eventually, hardware description language (Verilog-A script) is used to transform the equations into the code and a device symbol that is integrated into Cadence simulation library. It can be instanced as component/cell along-with properties on the analog simulation platform. A series of simulation results have been obtained, including the Fowler-Nordheim tunnelling process, I-V characteristics, transconductance and output impedance. The behaviour of the FGMOSFET modeled in the form of an equivalent MOSFET that can store charge makes it quite distinct from a normal MOSFET. It can operate in the saturation region even if the gate voltage is zero and requires a lower gate voltage to obtain the same gm than the normal MOS transistors. However, owing to the stored floating-gate charge, the output impedance of FGMOSFET is smaller than that of the traditional MOSFET. The design employs the Shichman-Hodges Model for effective and efficient FGMOSFET modelling. However, it doesn't include sub-threshold conduction or short-channel effects for which more precise BSIM4 model may be needed. The entire methodology for creating a FGMOSFET CAD component for analysis and design discussed here, can still be employed using a different model. The advantage of this approach is that, it provides open source model and enables engineers to have access to model equations directly.

3.4 Single Polysilicon FGRADFET

When the simulation model is completed, next step is to find the equations between radiation dose and floating gate voltage. The process is presented in the following paragraphs.

3.41 The Theory of FGRADFET

The cross-section view of the FGRADFET's basic structure and top view have described in Fig. 2. 9. The process about total ionizing dose (TID) effect [35] [36] in FGRADFET is drawn in Fig. 3. 19.

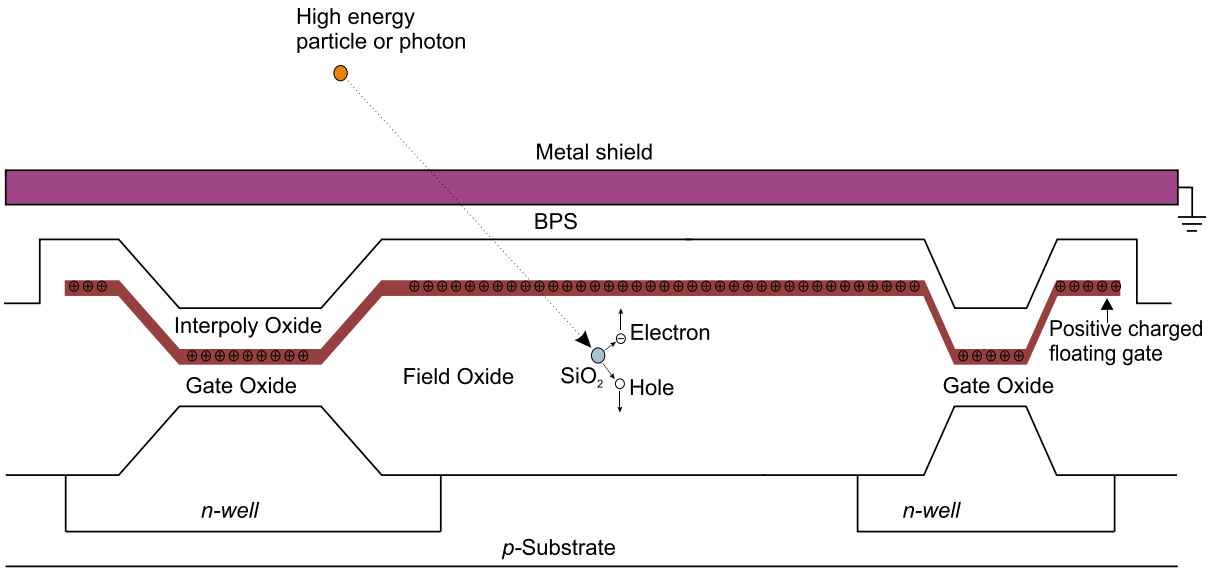


Fig. 3. 19 TID effect in FGRADFET.

When incident particles impact the SiO_2 in field oxide layer and the energy of particles is bigger enough, the electron-hole pair generates from SiO_2. The minimum energy for electron-pair generation is 17eV according to [37]. Because the positive charges are stored in the floating gate, there is an electric field from floating gate to *p*-substrate. Electrons will move towards to the floating gate and combine with positive charges under the electric field. The relationship between the variation of floating gate charges and total dose is described in equation 3.21 [20].

$$Q_{col} = \left[1 - R(\varepsilon)\right] \cdot \frac{q\rho_{SiO_2} A t_{ox}}{W_{e-h}} \cdot D \tag{3.21}$$

Where Q_{col} is the total charge collected; R(Ɛ) is the recombination rate of electron-hole pair which is proportional to electric field across the field oxide; $W_{e\text{-}h}$ is the energy of an electron-hole pair generation which is about 17eV for SiO_2 [21][22]; *q* is the charge of an electron which is 1.6e-19C; ρ_{sio2} is the density of silicon oxide. A is the area of field oxide which is 200μm×125μm in this FGRADFET design. T_{ox} is the thickness of field oxide. D is the total dose absorbed by the FGRADFET.

The variation of charges in floating gate will lead to the change of floating gate voltage. Its expression is shown in equation 3.22.

$$\nabla V_{fg} = \frac{\nabla Q_{fg}}{C_T} = \frac{-Q_{col}}{C_T} \tag{3.22}$$

Therefore, next work is to design the readout circuit to get the variation of floating gate voltage, which is a quite challenge. Because the variation of floating gate is very small that is almost equal to

the noise signal. In other words, radiation signal may be distorted by the noise signal. The methods that how to filter these noises and amplify small radiation signal are presented in the following chapters.

Chapter 4 Radiation Sensor Frontend Readout Circuit Design

This chapter illustrates the radiation sensor front-end readout circuit design, which includes the whole diagram, floating gate voltage readout circuit design, differentiator circuit design, source-follower preamplifier buffer design, modulation and demodulation chopper circuit design and two-stage differential amplifier design.

4.1 Block Diagram for The Whole Dosimeter Circuit

The block diagram for the whole dosimeter circuit is shown in Fig. 4. 1.

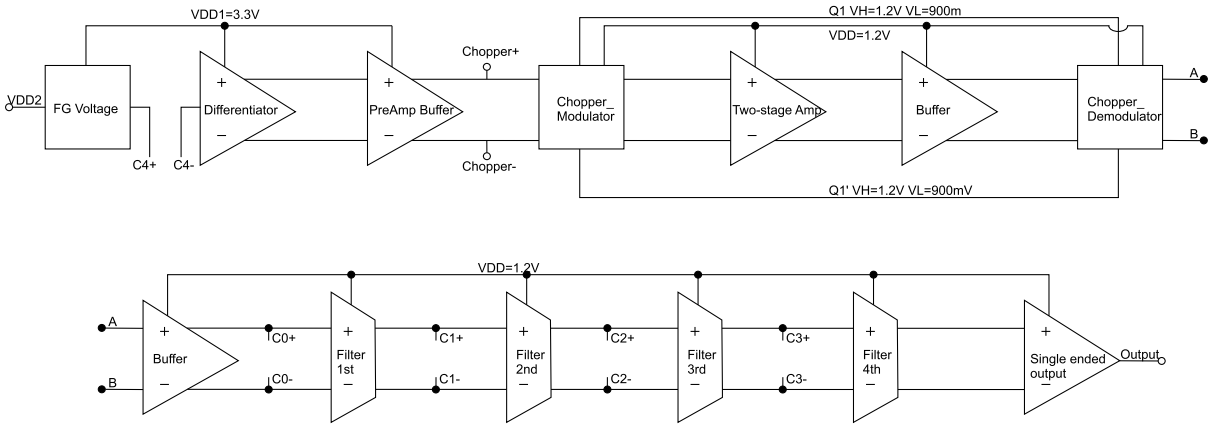


Fig. 4. 1 Block diagram for the whole dosimeter circuit.

The aim of the whole circuit is to find the slope of floating gate voltage and amplify it. At first, a couple of current mirror circuits are used to read the floating gate voltage of FGRADFET sensor. Then, the slope of floating gate voltage is calculated by the differentiator. Owing to the tiny voltage of slop, the chopper is placed next to differentiator to modulate the small signal. The modulated signal is amplified by a two-stage amplifier and then is demodulated. The chopper amplifier can immune flicker noise effectively. After that, a four-order low-pass filter and the single ended output circuit are utilized in order to get rid of chopped noise and obtain a single output. In this circuit, there are three power supplies which are VDD (1.2V), VDD1 (3.3V) and VDD2. VDD2 is used to charge the floating gate, which is a pulse power supply as shown in Fig. 3. 8. In addition, Q1 and Q1’ is the clock pulse signal for chopper amplifier. C0+, C0- to C4+, C4- are eight ports, which are used to connect 4 equal external capacitors (1nF). Chopper+ and Chopper- are the pins which set to test chopper amplifier. Next sections will introduce each part of the whole dosimeter circuit in detail.

4.2 Floating Gate Voltage Readout Circuit Design

The variation of floating gate voltage can be calculated by measuring the drain current of FG transistor [38]- [40] or through indirect measuring the FG potential [41]. In the first method, the proposed circuit to measure the drain current is shown in Fig. 4. 2 [39]. The sensor is a *n*-type FG transistor which is charged before it is employed to work. Therefore, it can work even though there is no connection at the gate. N2, N3 and OA composite of g_m-boost common gate amplifier. P1 and P2 are current mirrors that can mirror the amplified drain current to the output.

Fig. 4. 2 Proposed simplified schematic to measure the drain current of FGMOSFET radiation sensor [39].

Fig. 4. 3 The current versus temperature for the circuit shown in Fig. 4. 2 [39].

From Fig. 4. 3, we can find that the current is affected by temperature during the irradiation with 1.65krad total dose and pre-irradiation. The unit of k-rad is very big. Therefore, the current is affected

by temperature heavily actually. Considering this, the second case is preferred one. The proposed simplified schematic to measure the gate voltage of FGMOSFET radiation sensor is shown in Fig. 4. 4. M1 is a charged floating gate sensor which is used to sense the radiation. M2 is an uncharged floating gate transistor that has same geometry parameters with M1. The low-noise OP-27 operational amplifier amplifies the drain current of M1 and M2, then adjust the bias voltage of M2 until the two inputs of OP27 (drain currents) are equal. Since the size and power supply of R1 and M1 are exactly same with R2 and M2, and they suffer the same temperature effect. The output voltage (bias voltage) will extract the accurate floating gate voltage of M1.

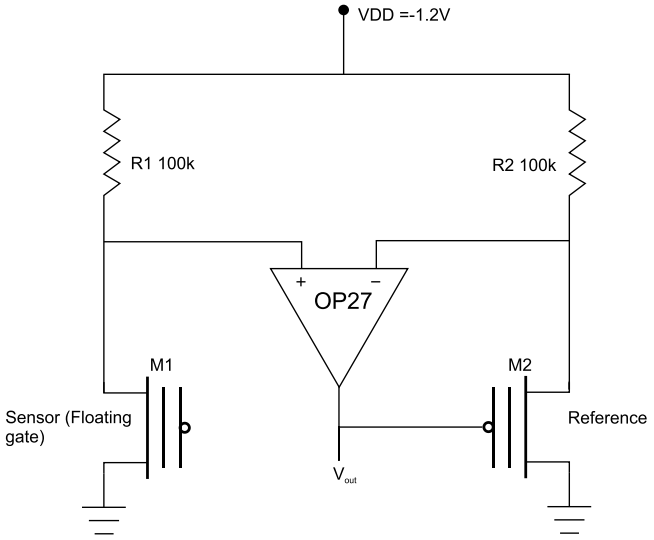


Fig. 4. 4 Proposed simplified schematic to measure the gate voltage of FGMOSFET radiation sensor [21].

According to the design schematic in Fig. 4. 4, another floating gate voltage readout circuit is designed as depicted in Fig. 4. 5. This FG voltage readout circuit uses cascode current mirrors to read the floating gate voltage directly. FGRADFET is made up of a single poly PMOS transistor (M1 and M2) and sixteen shorted PMOS transistors as the injectors (M7-M22). M2 and M23-M38 work as reference transistors.

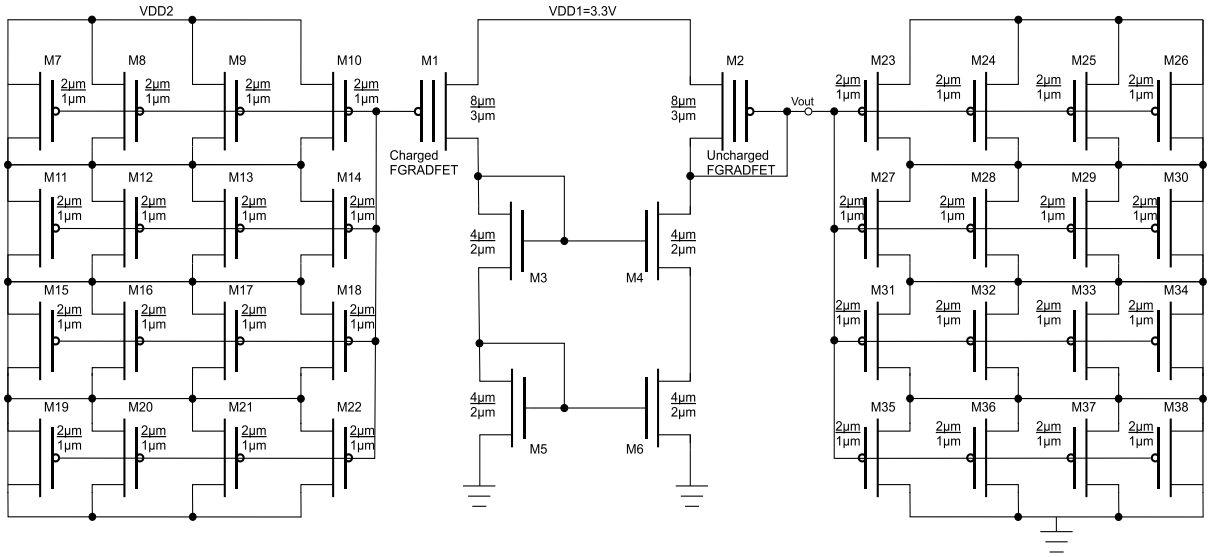


Fig. 4. 5 Floating gate voltage readout circuit

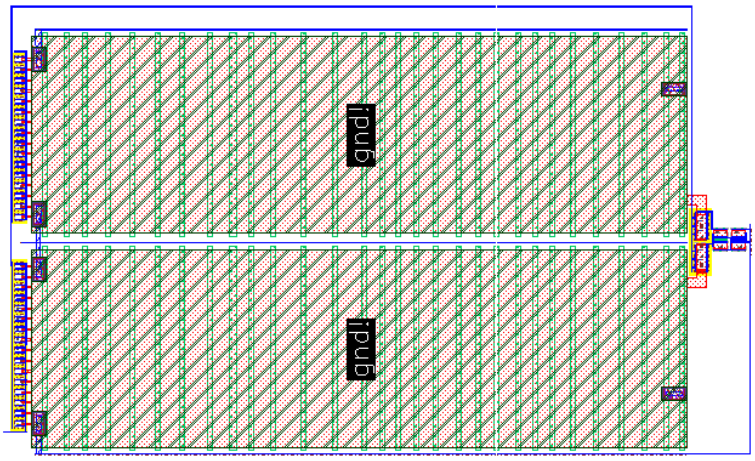


Fig. 4. 6 The layout of floating gate voltage readout circuit

In this circuit, two groups of current mirrors are employed so that both of charged FGRADFET and uncharged FGRADFET drive the exact same drain current and same drain voltage. According to equation (3.10) and identical geometry structure of M1 and M2, both charged FGRADFET and uncharged FGRADFET have same gate voltage and threshold voltage. Therefore, this circuit can accurately extract floating gate voltage of charged FGRADFET. The layout of floating gate voltage readout circuit is shown in Fig. 4. 6.

In the simulation, the variation of V_{fg} owing to radiation effect is modeled by Verilog-A language shown in Appendix A 2. The simulation results of the floating gate voltage extraction are illustrated in Fig. 4. 7 and Fig. 4. 8. As Fig. 4. 7 shown, the output voltage is almost same with floating gate voltage. After calculating, output variation is 0-700uV difference with floating gate voltage, which is much smaller than monitoring drain current of FG transistor.

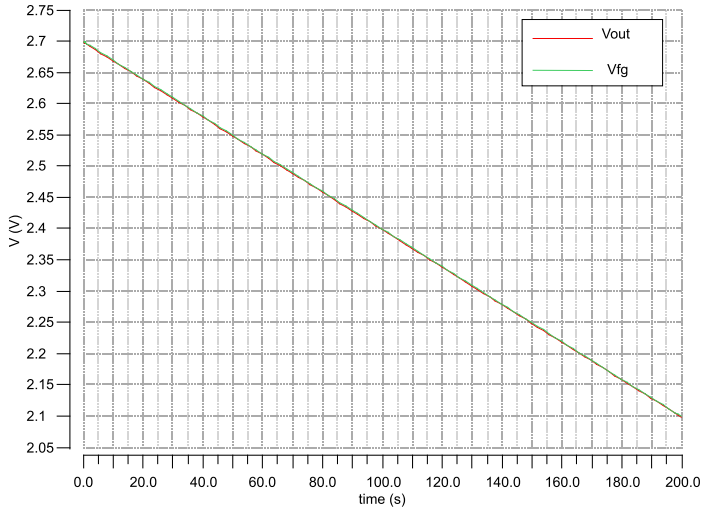


Fig. 4. 7 Transient analysis of FG voltage readout circuit

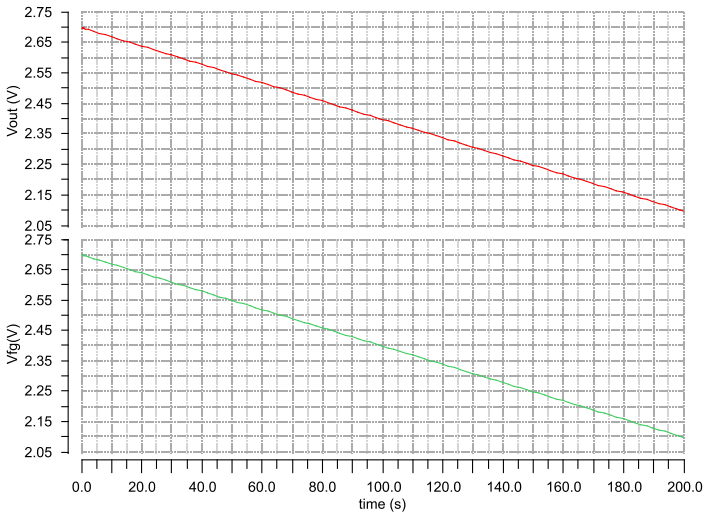


Fig. 4. 8 Transient analysis of FG voltage readout circuit in separate windows

4.3 Differentiator Circuit Design

In the measurement process of ionizing radiation, the important indicator is dose rate which represents the amount of radiation absorbed in each unit time. From the circuit in Fig. 4. 5, we can only infer the total dose from the output of floating gate voltage as shown in Fig. 4. 8. Therefore, differentiator circuit is designed to find the slope of floating gate voltage. According to [42], the proposed simplified schematic is presented in Fig. 4. 9. The differentiator is made up of an op-amplifier, capacitor and resistor. Using superposition at node A:

$$\frac{Cd(V_A - V_{in})}{dt} + \frac{V_A - V_{out}}{R_f} = 0 \tag{4.1}$$

According to virtual ground at node A:

$$V_A = 0 \tag{4.2}$$

Combine equation 4.1 and 4.2:

$$V_{out} = -CR_f \frac{dV_{in}}{dt} \tag{4.3}$$

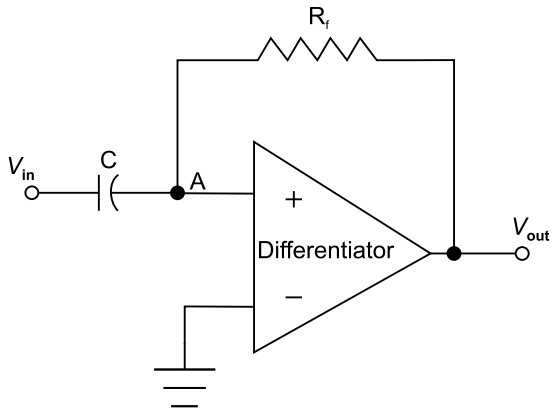


Fig. 4. 9 Proposed basic op-amp differentiator [42].

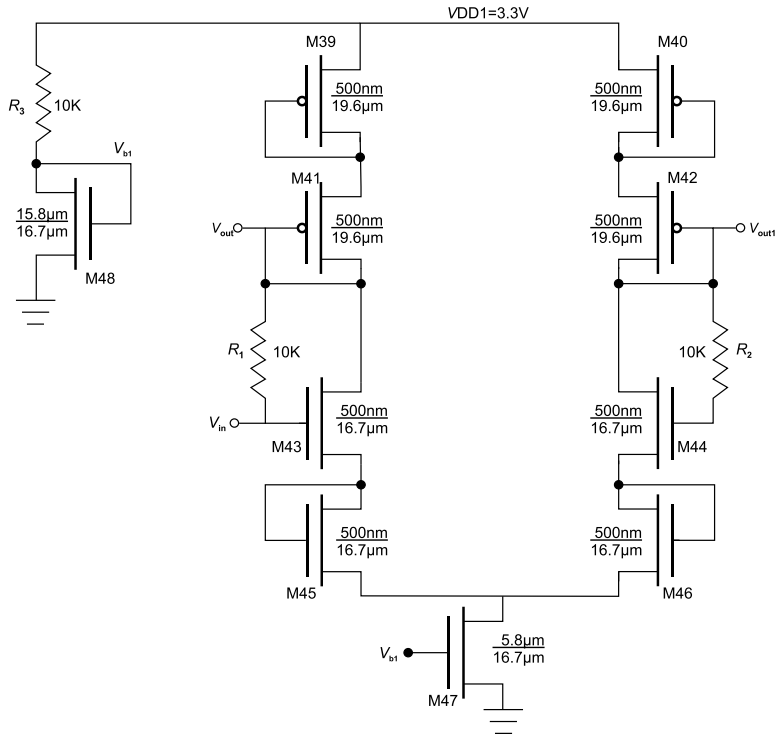


Fig. 4. 10 Differentiator circuit with differential output.

According to the basic op-amp differentiator, differentiator circuit is designed as depicted in Fig. 4. 10. Fig. 4. 11 is the layout of this differentiator. M39-M47 composites of a differential op-amplifier. The capacitor is connected to an external capacitor (C4, *1nF*) as shown in Fig. 4. 1. The R_f is a 10K resistor (R1 and R2). The bias circuit for transistor M47 is made by diode-connected transistor M48 and resistor R_3. The layout of this differentiator is shown in Fig. 4. 11.

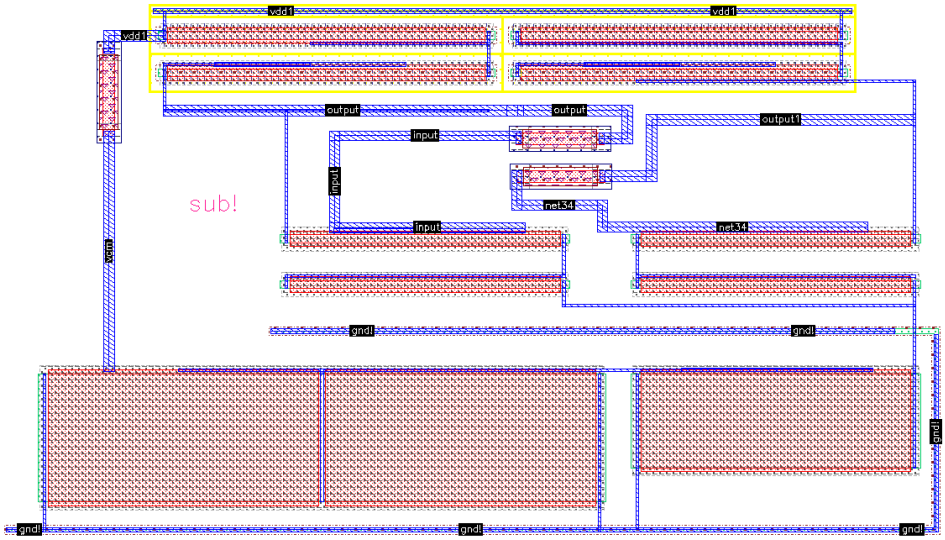


Fig. 4. 11 The layout of differentiator

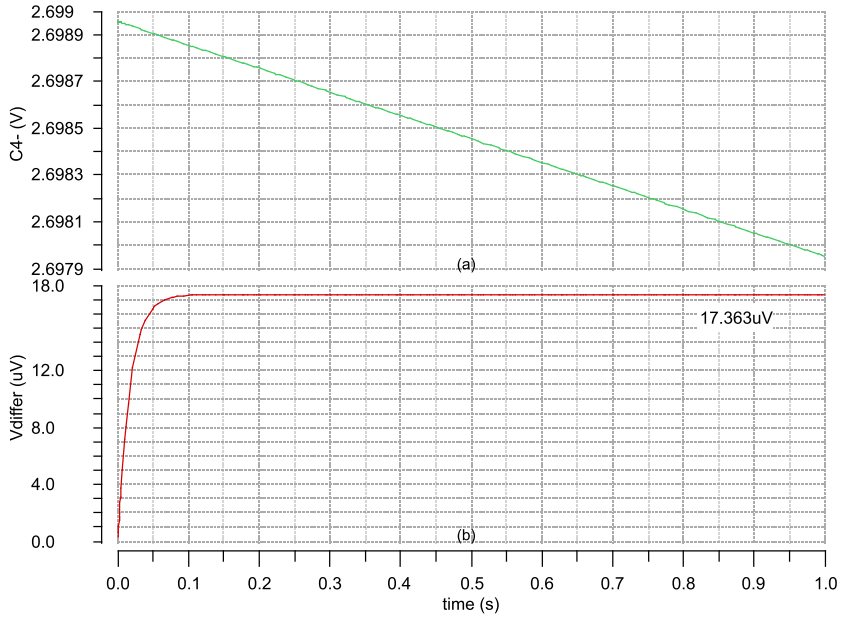


Fig. 4. 12 Simulation results of a differentiator.

(a) Floating gate voltage coming from the output of readout circuit in section 4.2. (b) The difference between two differential output which is the slope of floating gate voltage.

The simulation results of differentiator are shown in Fig. 4. 12. Fig. 4. 12 (a) shows floating gate voltage with the decreasing of 4.3mV per second owing to the ionizing radiation in equation 3.22. The differential output of differentiator is 17.363uV as described in Fig. 4. 12 (b).

4.4 Source-follower Preamplifier Buffer Design

The output voltage of differentiator is very small (17.363uV). We should amplify the signal and filter the noise at the same time. The circuit following the differentiator is a preamplifier buffer, which is used to block the effect between differentiator and another following circuit, and provide suitable offset voltage for the circuit in next section. The preamplifier buffer circuit is depicted in Fig. 4. 13. This is a source follower buffer, which

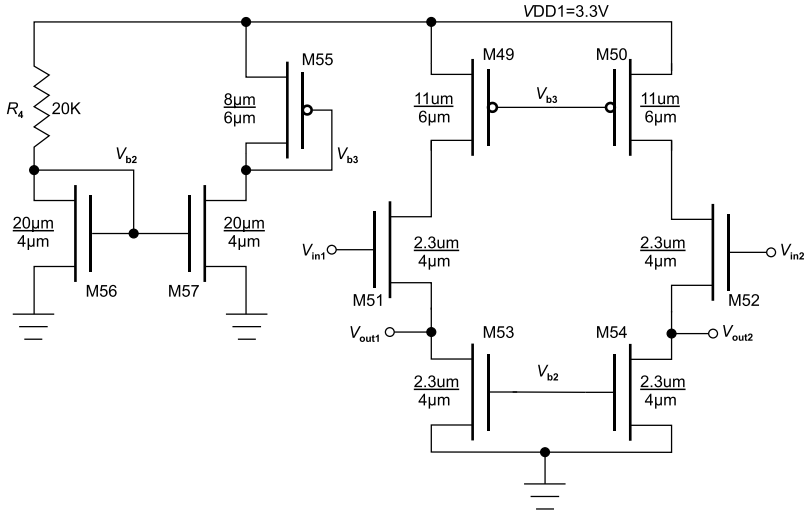


Fig. 4. 13 The schematic of source-follower preamplifier buffer

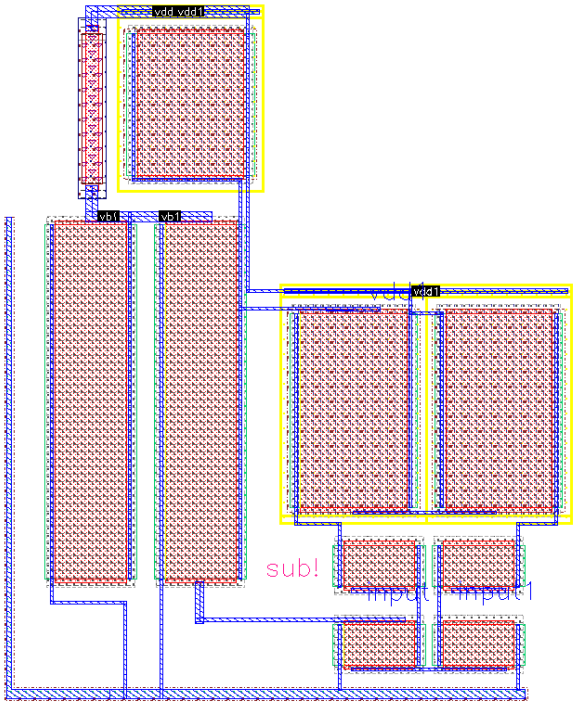


Fig. 4. 14 The layout of source-follower preamplifier buffer

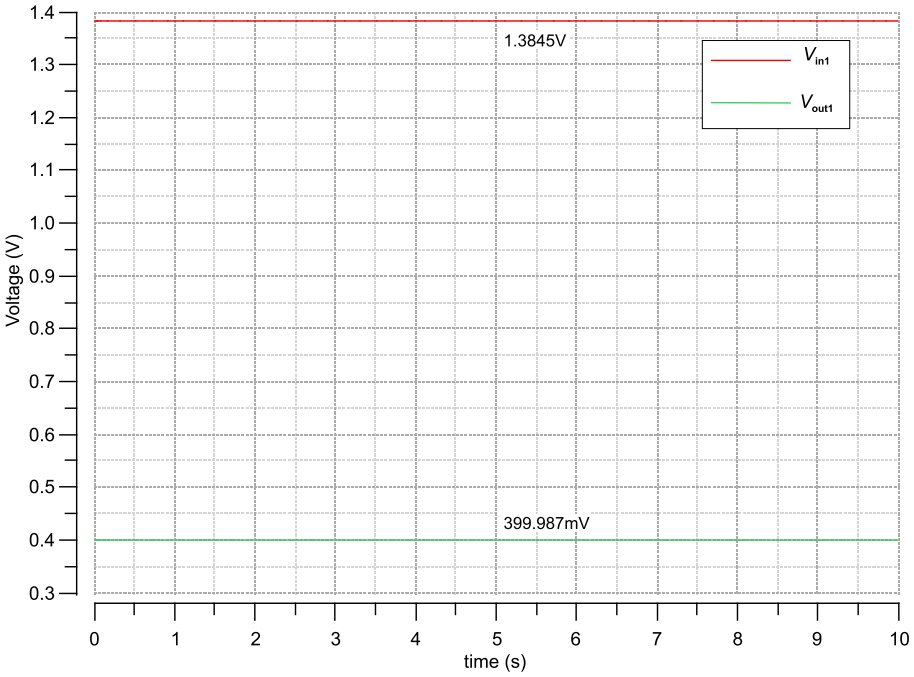


Fig. 4. 15 Simulation results of source-follower preamplifier buffer

does not change the amplitude of the signal. It is biased by V_{b2} and V_{b3} that come from the left part (bias circuit) of this circuit. The layout of this circuit in Fig. 4. 13 is shown in Fig. 4. 14. The simulation results of source-follower preamplifier buffer are shown in Fig. 4. 15. This buffer shifts the dc input voltage from 1.3845V to, dc output voltage, 399.987mV that is prepared for chopper amplifier.

4.5 Modulation and Demodulation Chopper Circuit Design

Because the output signal from differentiator is very small. It is necessary to design a chopper [43] circuit to modulate and demodulate this signal to avoid noise being amplified. The theory of chopper amplifier circuit is shown in Fig. 4. 16. When the signal comes in, it is chopped by a chopper in a frequency f_0. The chopped signal can be expressed as

$$V_{chopper} = V_{in} \cdot f_0 \tag{4.4}$$

Next, the unwanted offset voltage (V_{os}) and noise (V_n) will combine with the chopped signal as shown in equation 4.5 and Fig. 4. 17 (b).

$$V_b = V_{in} \cdot f_0 + V_{os} + V_n \tag{4.5}$$

All of them will be amplified.

$$V_A = AV_{in} \cdot f_0 + A(V_{os} + V_n) \tag{4.6}$$

After that, a de-chopper will chop the signal to previous frequency, and chop V_{os} and V_n to f0 frequent as shown in equation 4.7 and Fig. 4. 17 (c).

$$\begin{aligned} V_{dechopper} &= AV_{in} \cdot f_0^{\,2} + A(V_{os} + V_n) \cdot f_0 \\ &= AV_{in} + A(V_{os} + V_n) \cdot f_0 \end{aligned} \tag{4.7}$$

Finally, the low-pass filter can easily filter high-frequency signal V_{os} and V_n.

$$V_{out} = AV_{in} \tag{4.8}$$

The power spectral density (PSD) of chopper amplifier for (a)(b)(c)(d) in Fig. 4. 16 is presented in Fig. 4. 17.

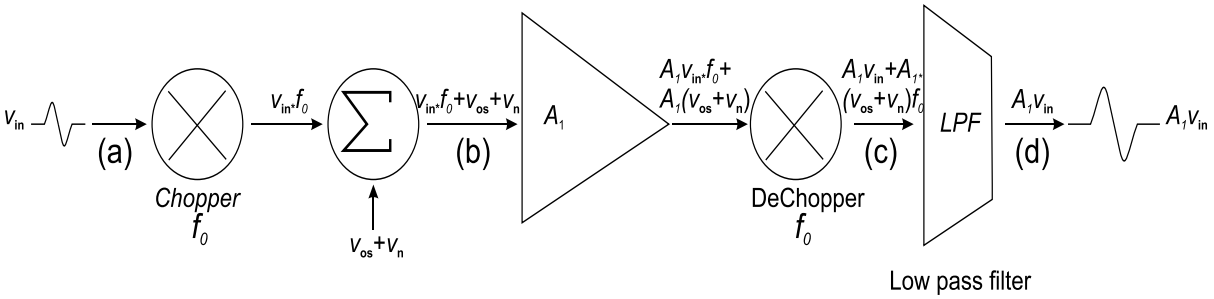


Fig. 4. 16 The working principle of chopper amplifier.

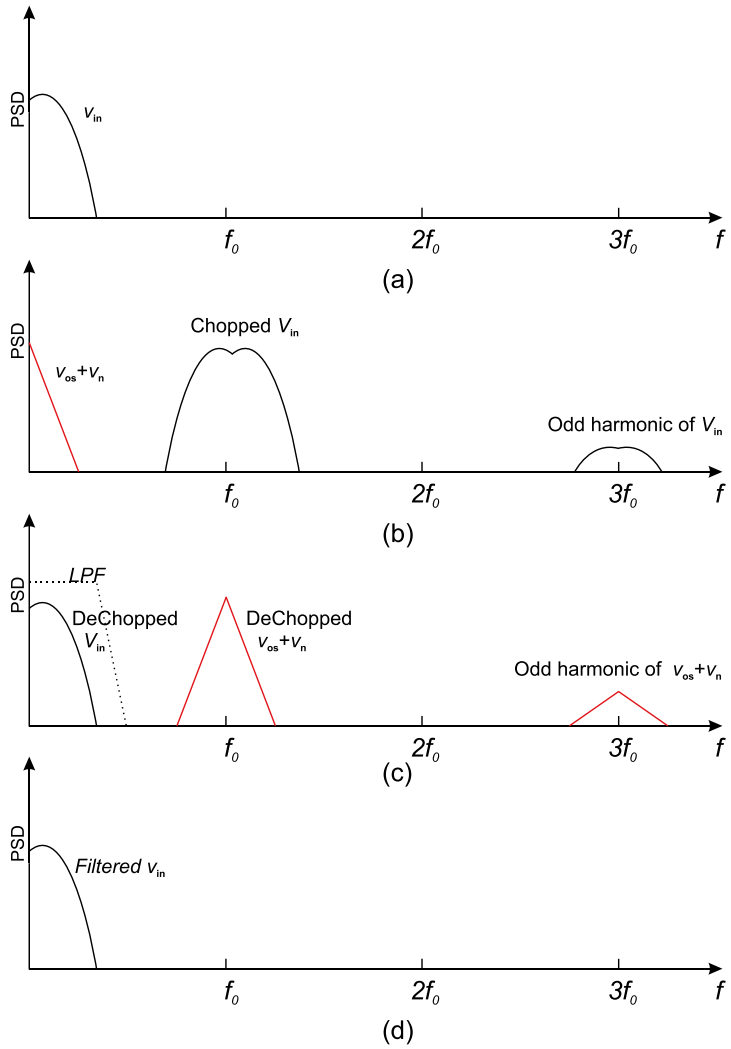


Fig. 4. 17 The power spectral density (PSD) of chopper amplifier of Fig 4.12.

(a) PSD of the input signal. (b) After chopped, the input signal is shifted to odd multiples of f_0 while the V_{os} and V_n still sit around the DC voltage. (c) PSD of demodulation chopper. V_{in} is chopped back to around DC. V_{os} and V_n are shifted up to chopping frequency which can be filtered by a low-pass filter. (d) PSD of filtered V_{in}. (a) (b) (c) (d) are one to one correspondence with (a) (b) (c) (d) in Fig. 4. 16.

The circuit of modulation chopper and demodulation chopper is same with the circuit presented in Fig. 4. 18, and its layout in Fig. 4. 19. The chopper is controlled by a clock signal, Q1 and Q1', which have opposite phase. When Q1 is high and Q1' is low in a period of 50us, M58-M61 are on and M62-M65 are off. $V_{out1}=V_{in1,}$ $V_{out2}=V_{in2}$. When Q1 is low and Q1' is high in a period of 50us, M58-M61 are

off and M62-M65 are on. $V_{out1}= V_{in2}$, $V_{out2}= V_{in1}$. And doing like this, the input signal is chopped to a new signal with a frequency of $f_0 = \frac{1}{100us}$ =10K Hz. In the demodulation chopper, the process is same with modulation chopper. Signal is chopped to DC around frequency, and unwanted offset and noise will be shifted up to 10K Hz frequency. The simulation results of the chopper and demodulation chopper are illustrated in Fig. 4. 20.

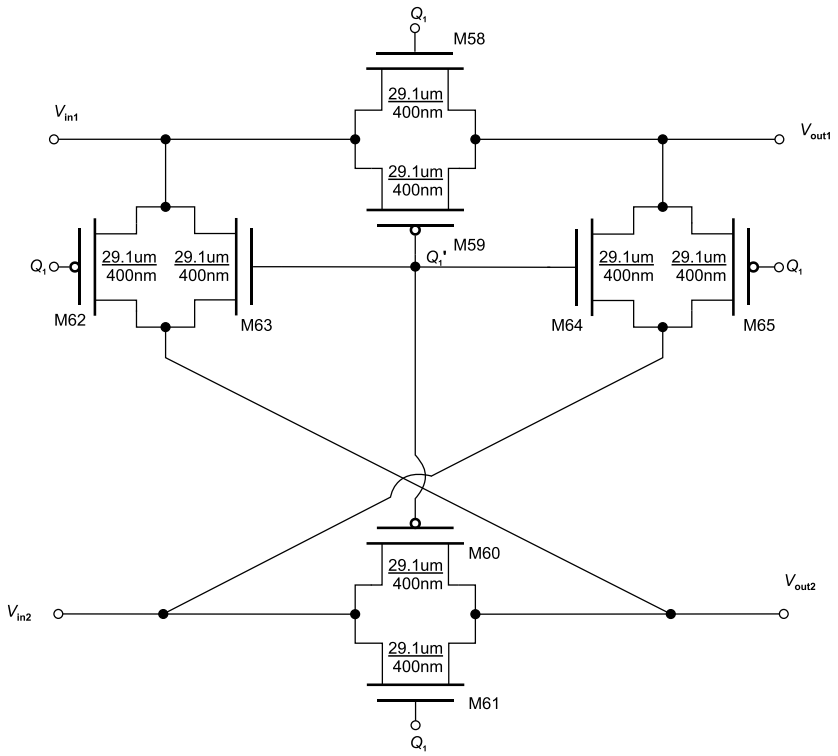


Fig. 4. 18 The schematic of modulation and demodulation chopper

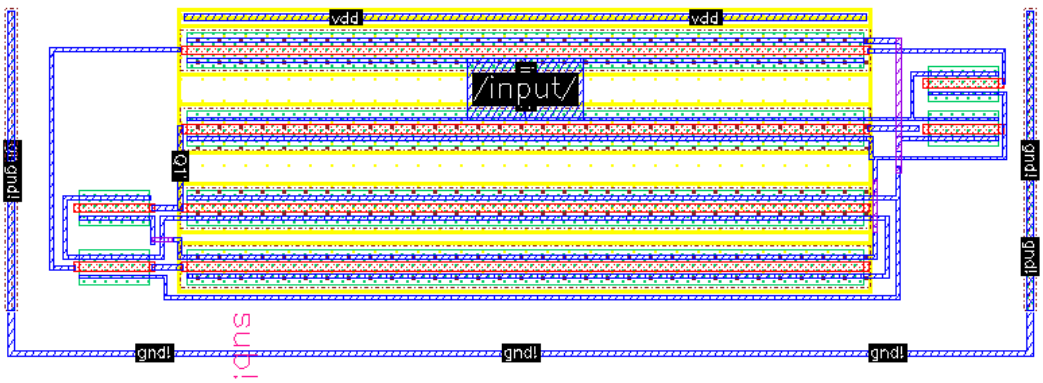


Fig. 4. 19 The layout of modulation and demodulation chopper

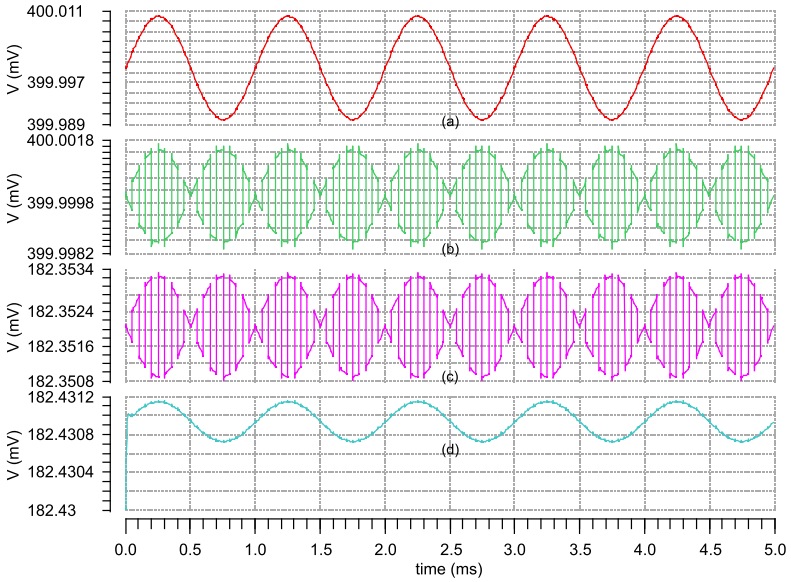


Fig. 4. 20 The simulation results of the chopper with a sinewave input.

(a) A sinewave input as the test signal. (b) Chopped sinewave in a 10K Hz chopping frequency. (c) The output from the buffer. (d). Demodulated sinewave in a 10K Hz de-chopping frequency.

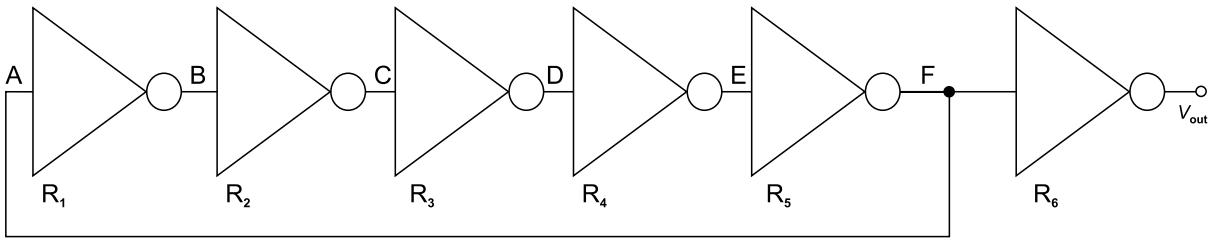


Fig. 4. 21 The theory of ring oscillator.

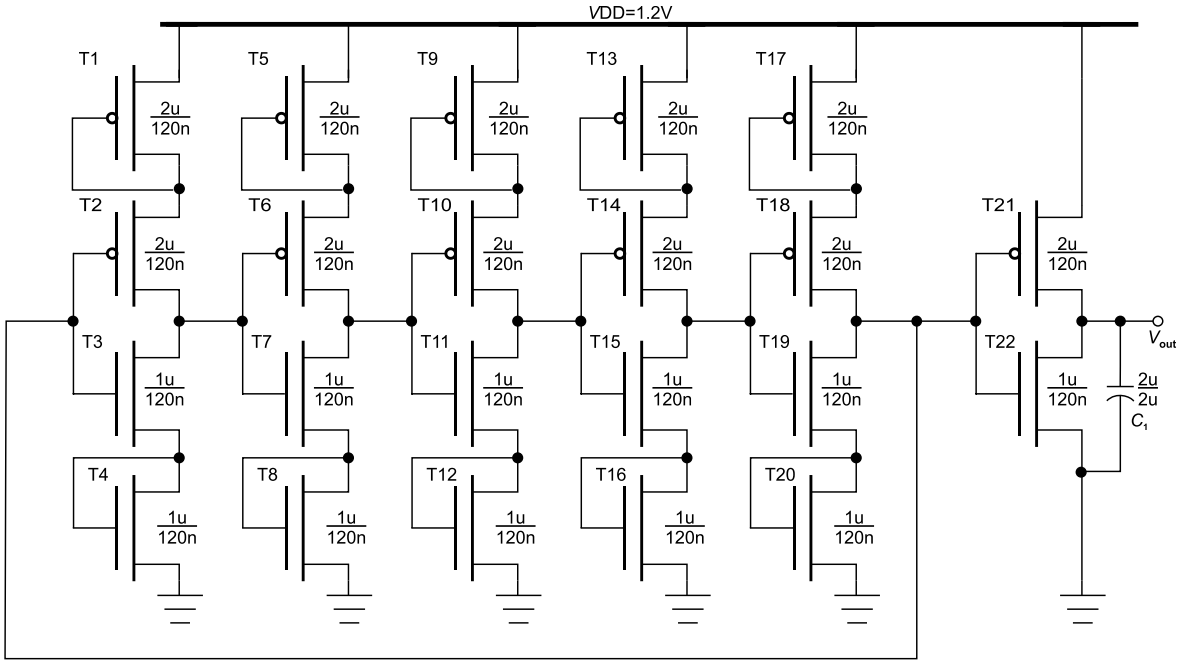


Fig. 4. 22 The schematic of the ring oscillator.

In the design of chopper, we made some attempts to design an oscillator that can be integrated into this dosimeter chip and produce the clock signal Q1 and Q1' internal. The first experiment is a ring oscillator, whose theory is shown in Fig. 4. 21. The number of the inverter in ring oscillator is always odd, which can make the oscillation happen. The key to trigger this oscillation in the simulation is a supply voltage, which should equip a rise period that is also used to simulate the action of switch on. The schematic of this ring oscillator is depicted in Fig. 4. 22. T1-T4 is the modified inverter with NMOS and PMOS diodes load in source and drain. The ring oscillator connects to an inverter with a capacitor load that can filter some ripple noise and get a better shape clock signal.

It is valuable to compute the smallest voltage gain each stage in Fig. 4. 22 that is required for oscillation. Ignoring the effect of the gate-drain overlap capacitance (C_{GD}) and only considering the drain-body overlap capacitance (C_{DB}), and per stage contributing the transfer function by $-A_0/(1+s/w_0)$, we can get the loop gain:

$$H(s) = -\frac{A_0^{\,5}}{(1+\frac{s}{w_0})^5} \tag{4.9}$$

The condition for circuit oscillation is that the frequency phase shift should be equal to 180^o (Every stage denotes 36^o). Thus, the frequency is given by

$$\tan^{-1}\frac{w_{osc}}{w_0} = 36^\circ \tag{4.10}$$

Hence: $$w_{osc} = 0.72654 w_0 \tag{4.11}$$

The smallest voltage gain at each stage should be that the magnitude of the loop gain is equal to unity at W_{osc}:

$$\left|H(s)\right| = \frac{\left|A_0^{\,5}\right|}{\left[\sqrt{1+(\frac{W_{osc}}{w_0})^2}\right]^5} = 1 \tag{4.12}$$

Combing equation 4.11 and 4.12,

$$A_0 = 1.314 \tag{4.13}$$

This five-stage ring oscillator requires a low-frequency gain of 1.314 for each stage and oscillates with a $2\pi*0.72654w_0$ frequency. Since every stage contributes a 36^o frequency-dependent phase shift

the waveforms at the five points of this oscillator of Fig. 4. 21 as well as the low-frequency inversion [45]. Each node has a 216º (or 72º) phase shift with reference to its next-door nodes as shown in Fig. 4. 23.

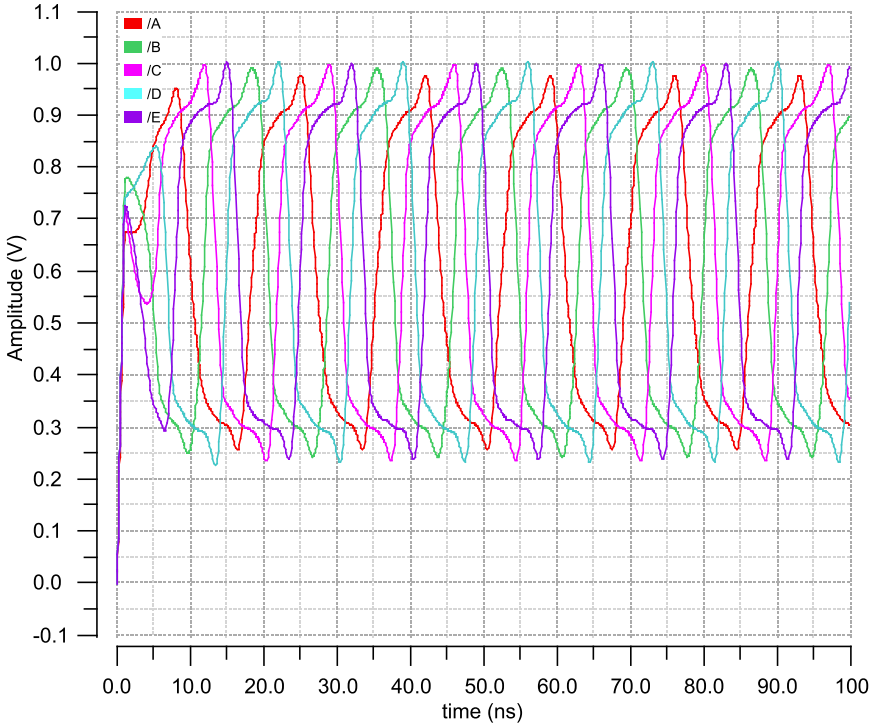


Fig. 4. 23 Waveforms of a five-stage ring oscillator.

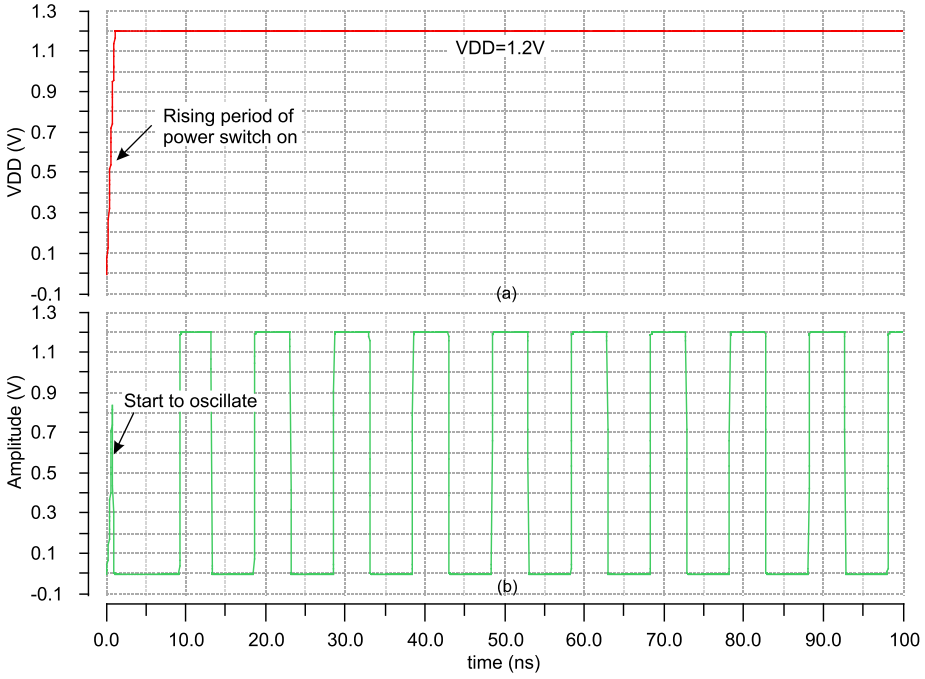


Fig. 4. 24 Transient analysis of ring oscillator.

(a) The power supply has a 1ns switch on rising period. (b) The output of the ring oscillator.

The transient analysis of this ring oscillator is shown in Fig. 4. 24, the key to start the simulation, the trigger, is the rising period (1ns) of the power switch on described in Fig. 4. 24 (a). Once the ring oscillator sensed the rising signal, it starts to oscillate depicted in Fig. 4. 24 (b). The frequency of this oscillator is 100M Hz.

In order to tune this frequency, this oscillator can be updated to a voltage control oscillator (VCO). Its schematic is illustrated in Fig. 4. 25. According to [43], the frequency is decided by this equation:

$$f_{osc} = \frac{I_{ctrl}}{2NV_{osc}C_g} \tag{4.14}$$

where I_{ctrl} is the control current flowing in each stage, V_{osc} is the oscillation amplitude which is 1V in this oscillator, N is the stage number (Here is 5), and C_g is the gate capacitance of PMOS and NMOS.

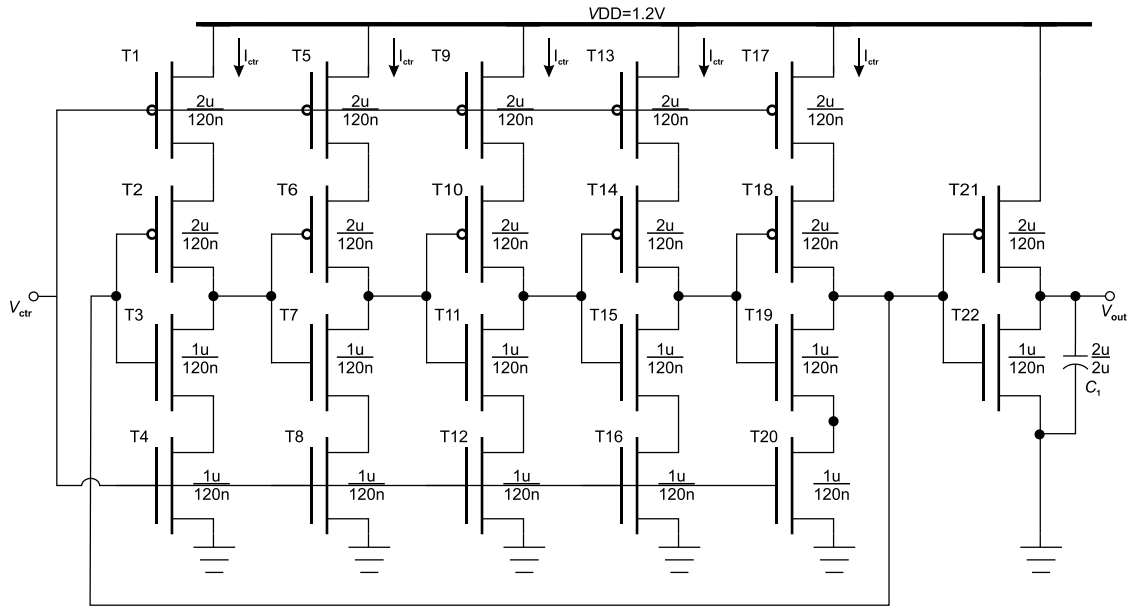


Fig. 4. 25 Voltage control ring oscillator

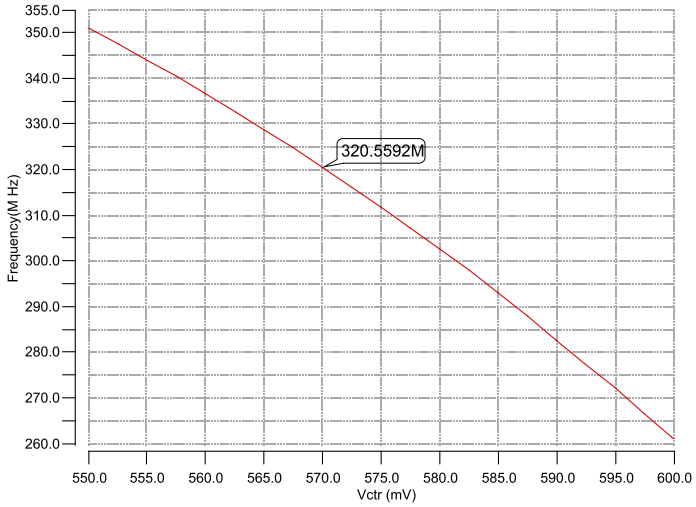


Fig. 4. 26 Control voltage versus frequency analysis for VCO

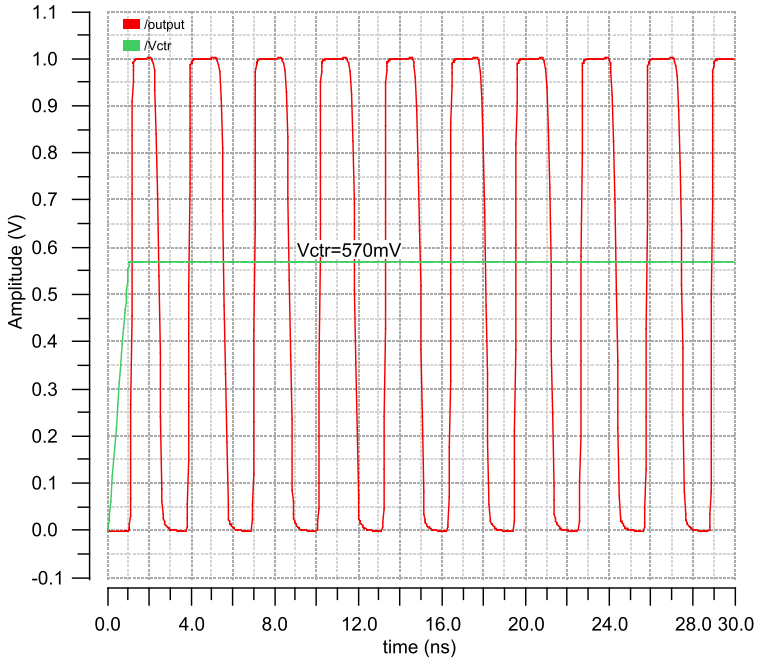


Fig. 4. 27 Transient analysis of VCO @Vctr=570mV.

The variation of frequency along with control voltage from 550mV to 600mV is shown in Fig. 4. 26. The effect of control voltage variation on PMOS is bigger than NMOS. Therefore, the rising of control voltage leads to the decreasing of the drain current of PMOS, which will contribute the fall of frequency according to Equation 4.14. When the control voltage is 570mV, the frequency is 350.5592M Hz. The transient analysis at this point is shown in Fig. 4. 27.

The clock signal Q can be produced from this VCO, and Q' can be obtained by adding an inverter at the output of this VCO. Since the frequency is not accurately locked and an external oscillator can be employed to this experiment, we did not add this VCO in the final chip that might affect the accuration of this chopper amplifier. Further research work is needed for phase locked loop VCO.

4.6 Two-stage Differential Amplifier Design

The amplifier is an essential component in the whole circuit. In this case, the amplifier has a work to amplify a signal from 10uV to 70mV (Av=7000, i.e. dB=77). The requirement to design this amplifier is low noise, low power dissipation, and high gain. According to the comparison of the performance of various operational amplifiers in table 4.1 [45], the two-stage amplifier is the best one, which has high gain, low noise and highest output swing.

TABLE 4. 1 Comparison of Performance of Various Op Amp

Types	Gain	Output Swing	Speed	Power Dissipation	Noise
Cascode Telescopic	Medium	Medium	Highest	Low	Low
Folded-Cascode	Medium	Medium	High	Medium	Medium
Two-Stage	High	Highest	Low	Medium	Low
Gain-Boosted	High	Medium	Medium	High	Medium

In order to design the best amplifier, a lot of attempts are done. One of the valuable experiment is a fully differential self-biased amplifier [46], which is shown in Fig. 4. 28. It provides a wide range of input Common Model (CM) range. If there are no transistors T1, T3 and T4, what happens when the input CM level drops under the minimum given above. The transistor T2 enters the triode region, which will lower the transconductance and crash this amplifier. A simple method for extending the input CM range is to combine both NMOS and PMOS differential pairs together as depicted in Fig. 4. 28. As the falls of the CM level of V_{in} to the ground potential, the NMOS (T2, T5 and T6) pair's transconductance is also reduced, in the end dropping to zero. Nevertheless, the PMOS (T1, T3 and T4) pair remains alive, which can be providing the normal operation. On the contrary, even though the input CM level approaches V_{DD} (1.2V), T2, T5 and T6 start to turn off. T1, T2 and T4 still work properly. The variation of the total transconductance of this amplifier as the input CM level changes is shown in Fig. 4. 29.

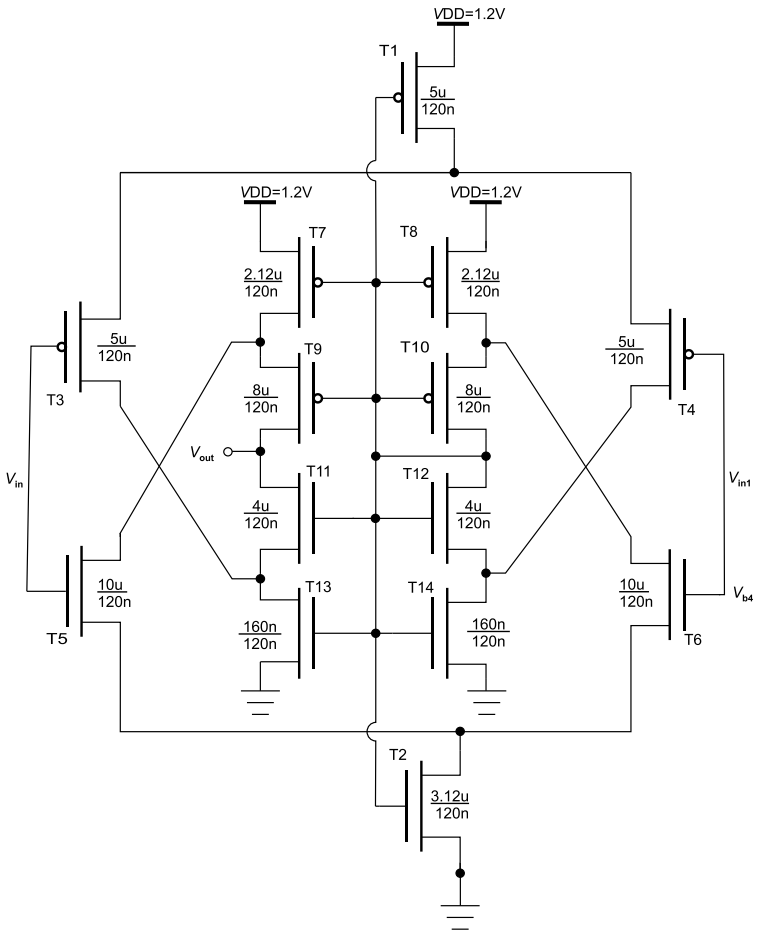


Fig. 4. 28 Folded-cascode fully differential self-biased single-ended amplifier.

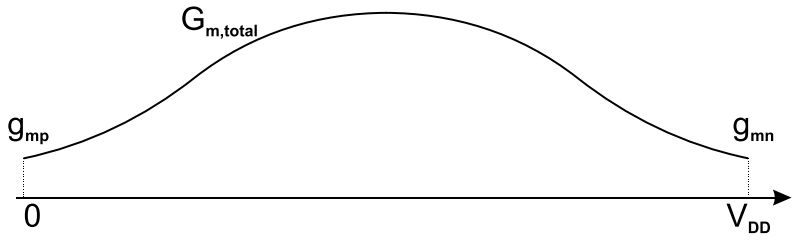


Fig. 4. 29 Variation of overall g_m versus the input CM level.

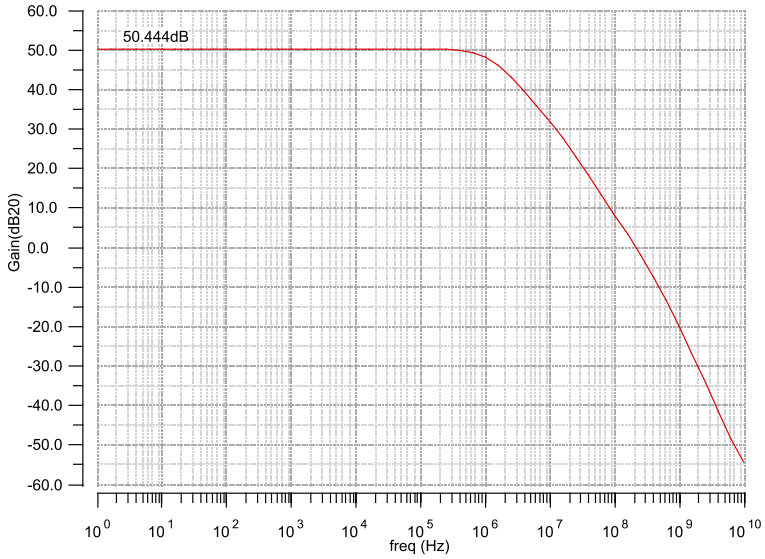


Fig. 4. 30 AC analysis of folded-cascode fully differential self-biased single-ended amplifier

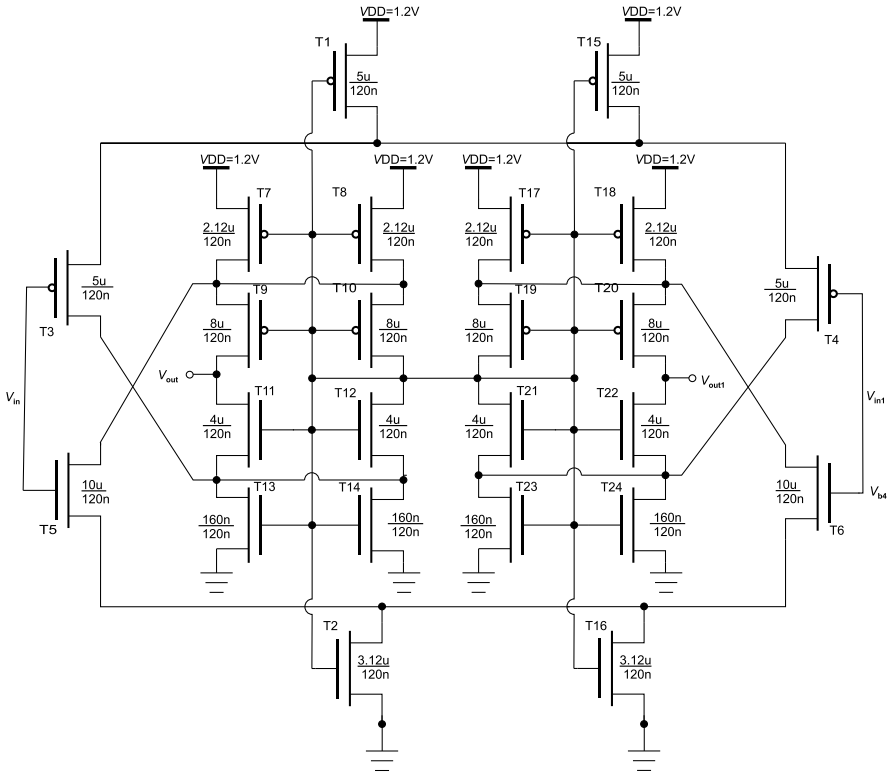


Fig. 4. 31 Folded-cascode fully differential self-biased amplifier.

All the parameters shown in Fig. 4. 28 of this amplifier are calculated and chosen with ADE XL software tool. AC simulation of folded-cascode fully differential self-biased single-ended amplifier with these parameters is depicted in Fig. 4. 30. The gain is 50.444dB.

To get the differential output, this folded-cascode fully differential self-biased single-ended amplifier can be extended as shown in Fig. 4. 31.

Considering the low gain (50.444dB) of this self-biased amplifier (The minimum gain of the amplifier for this design is 77dB), another two-stage differential amplifier is designed. The schematic and layout of this two-stage differential amplifier are shown in Fig. 4. 32 and Fig. 4. 33, respectively. The optimized parameters for this circuit are also found by analog design environment (ADE)

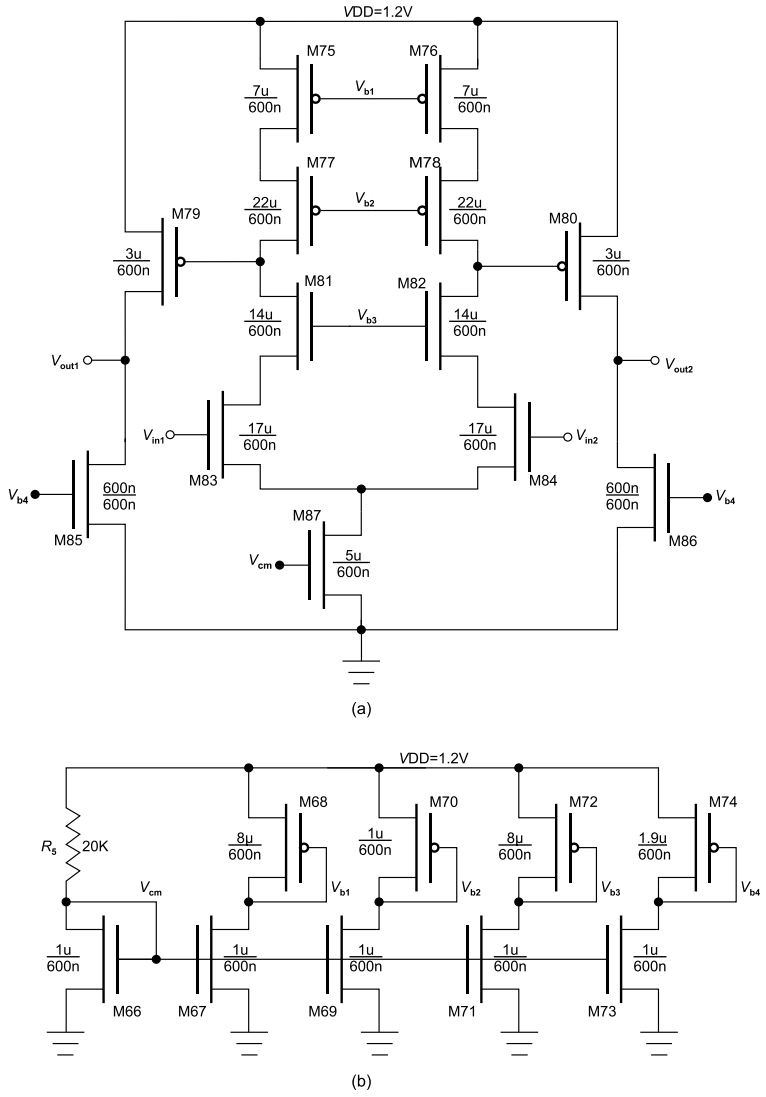


Fig. 4. 32 The schematic of the two-stage differential amplifier.

(a) The main circuit of the amplifier. (b) A bias circuit for the amplifier.

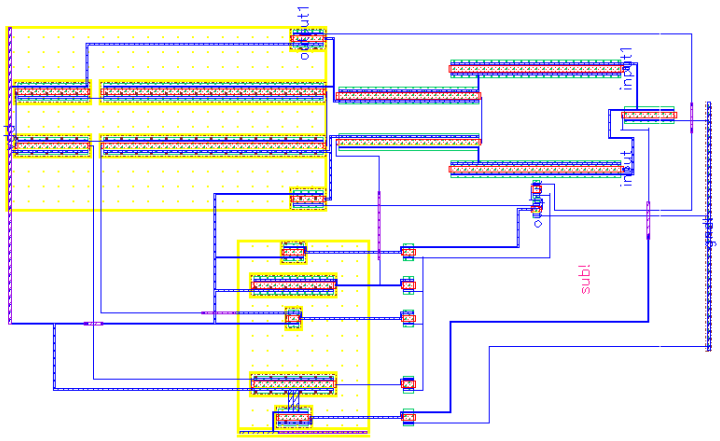


Fig. 4. 33 The layout of two-stage differential amplifier

XL tool automatically. The signal is amplified in the first stage by a cascode circuit, and then it is amplified in the second stage by a simple common source circuit. The output signal has a high swing after the amplification of second stage. To analysis the gain in the equation, we first draw the AC equivalent circuit for left part of the first stage in Fig. 4. 32 (a) (M75, M77, M81 and M83) as shown in Fig. 4. 34. All DC bias voltages are ac ground. In order to find the gain of the first stage, we employ the double times short circuit ways to find the composite trans-conductance G_m and the composite output impedance R_{out} [47]. Then, the mid-band gain of the small signal is $G_m * R_{out}$ [48]. First, we short the V_{out} to find the G_m. The circuit is shown in Fig. 4. 35 (a). The output is shorted to ground with a capacitor. Then, the ac current signal flows through the capacitor rather than M77 and r_{o75}. Thus, the trans conductance can be decided by this equation:

$$G_m = \frac{i_{out}}{V_{in1}} \tag{4.15}$$

To find the i_{out} of this shorted output circuit, the small signal model is drawn in Fig. 4. 35 (b). Simplify this circuit by replacing the Norton current source with a Thevenin voltage source, g_{m81} and g_{mb81} with two resistors. We can get the simplified circuit shown in Fig. 4. 36.

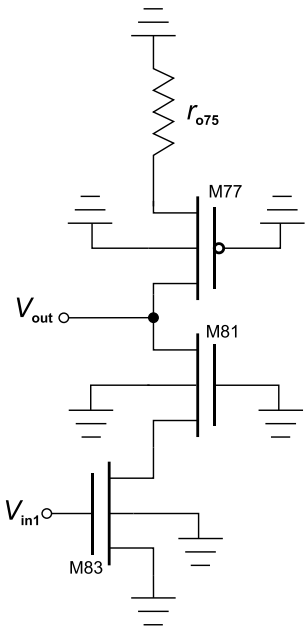


Fig. 4. 34 AC equivalent circuit for left part of first stage Fig. 4. 32 (a).

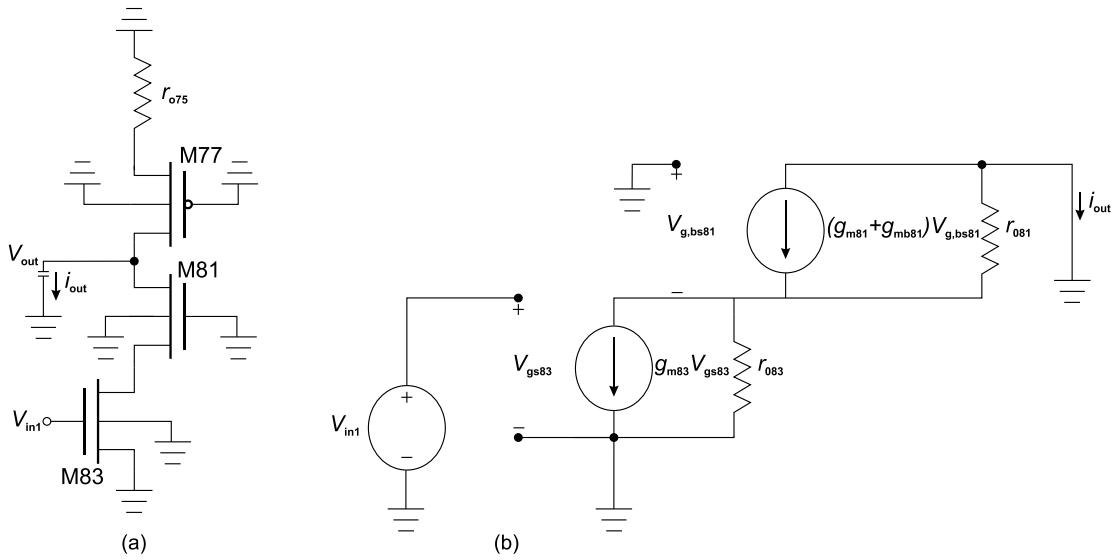


Fig. 4. 35 Output short circuit to determine G_m

(a) Output shorted AC equivalent circuit. (b) Small signal mode analysis for (a).

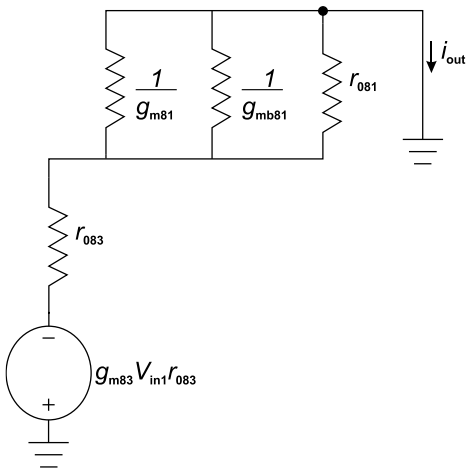


Fig. 4. 36 Simplified small signal model analysis

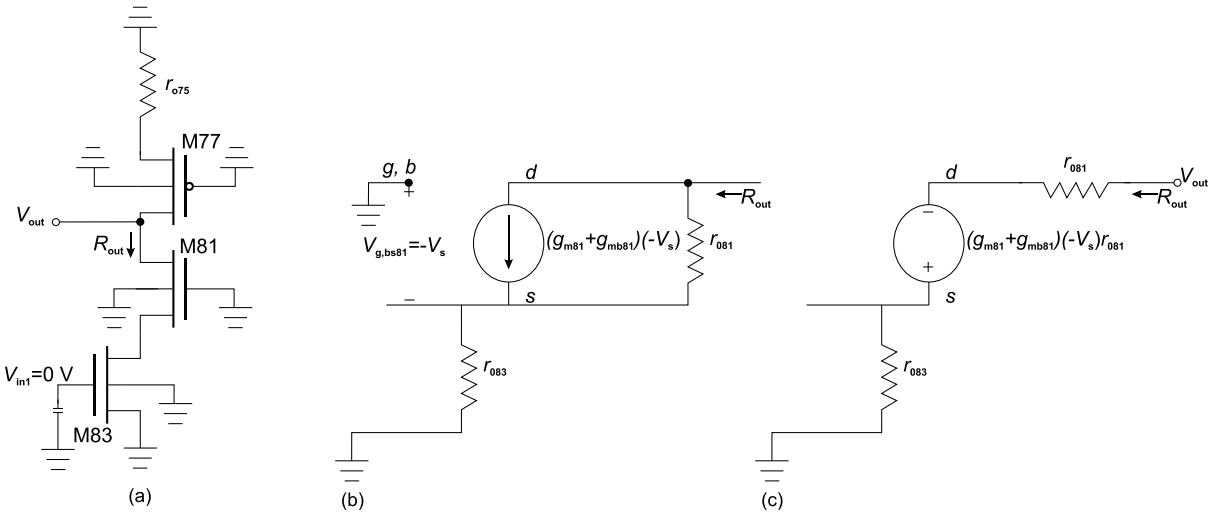


Fig. 4. 37 Input short circuit to determine R_{out}.

(a) Input shorted AC equivalent circuit. (b) Small signal model analysis for (a). (c) Simplified small signal model analysis for (b).

$$G_m = \frac{i_{out}}{V_{in1}} = -\frac{g_{m83}V_{in1}r_{o83}}{V_{in1}\left(r_{o83} + \dfrac{1}{g_{m81} + g_{mb81} + \dfrac{1}{r_{o81}}}\right)} = -\frac{g_{m83}r_{o83}\left[\left(g_{m81} + g_{mb81}\right)r_{o81} + 1\right]}{r_{o81} + r_{o83}\left[\left(g_{m81} + g_{mb81}\right)r_{o81} + 1\right]} \tag{4.16}$$

The second step is to find R_{out} by shorting input at the gate of M83 with an AC grounding capacitor. The circuit is shown in Fig. 4. 37. Since gate, source and body of M83 are AC ground, its ac model can be presented with a channel length resistor r_{o83}. For M81, the trans-conductance g_{m81} and body trans-conductance g_{mb81} are then merged together because its gate and body are AC ground. Final step

is to simplify the small signal mode by replacing the Norton current source with a Thevenin voltage source. Therefore, R_{out} can be expressed as:

$$\begin{aligned} R_{out} &= r_{o81} + r_{o83} + \frac{(g_{m81} + g_{mb81})r_{o81}(-V_s)}{\frac{-V_s}{r_{o83}}} \\ &= r_{o81} + r_{o83} + (g_{m81} + g_{mb81})r_{o81}r_{o83} \end{aligned} \tag{4.17}$$

Combining the product of (4.16) and (4.17), obtain voltage gain of the first half stage from the double short-circuit method,

$$A_{V1} = G_m R_{out} = -g_{m83}r_{o83}\left[(g_{m81} + g_{mb81})r_{o81} + 1\right] \tag{4.18}$$

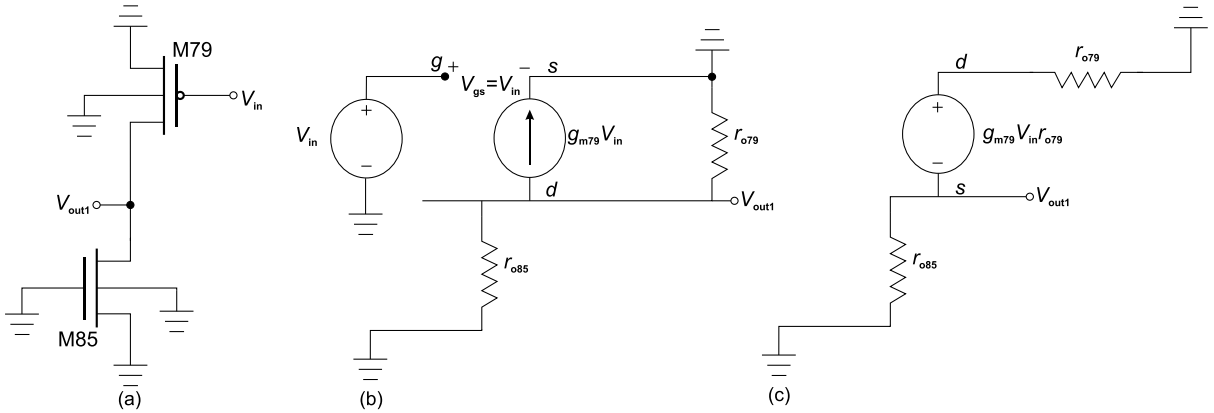


Fig. 4. 38 AC equivalent circuit for left part of first stage Fig. 4. 32 (a).
(a) AC ground equivalent circuit. (b) Small signal mode analysis for (a). (c) Simplified small signal model analysis for (b).

The AC equivalent circuit for left part of the second stage is drawn in Fig. 4. 38. The V_{in} from the first stage is the input signal which is:

$$V_{in} = A_{V1}V_{in1} = -g_{m83}r_{o83}\left[(g_{m81} + g_{mb81})r_{o81} + 1\right]V_{in1} \tag{4.19}$$

In Fig. 4. 38 (a), the gate and body are ac ground. Thus, it can be modeled with a resistor r_{o85}. The body effect of M79 is neglected because its V_{bs}=0. Then, simplify this small signal model to Thevenin voltage source. We can get the final gain equation:

$$\begin{aligned} A_V &= \frac{V_{out}}{V_{in1}} = \frac{g_{m79}V_{in}r_{o79}}{(r_{o79} + r_{o85})V_{in1}} \\ &= -\frac{g_{m79}r_{o79}g_{m83}r_{o83}\left[(g_{m81} + g_{mb81})r_{o81} + 1\right]}{r_{o79} + r_{o85}} \end{aligned} \tag{4.20}$$

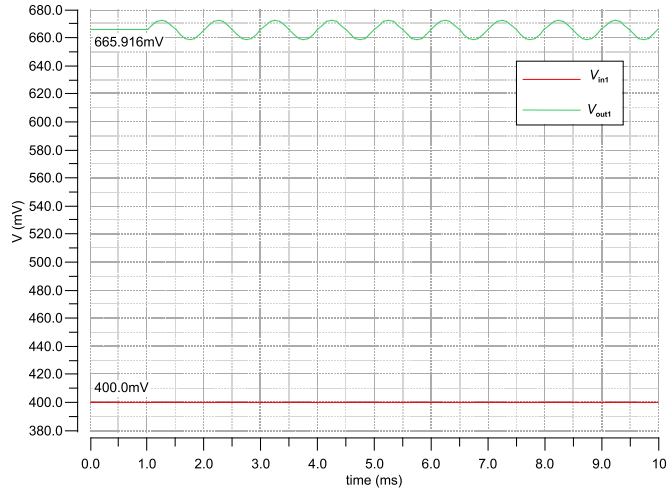


Fig. 4. 39 The transient simulation results of the two-stage differential amplifier.

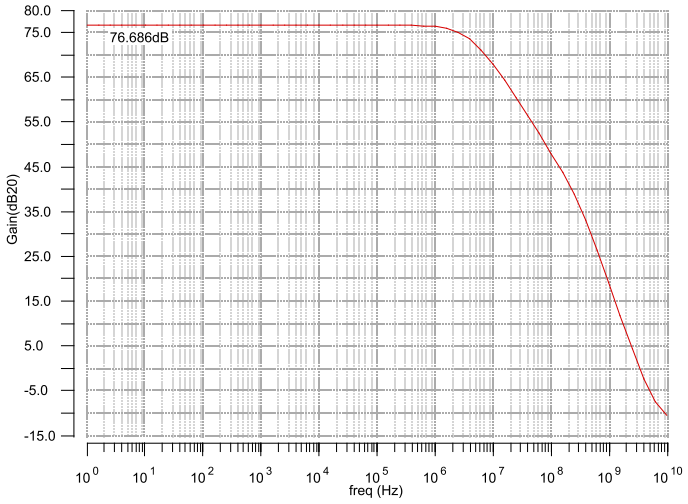


Fig. 4. 40 AC analysis of two-stage differential amplifier.

The transient analysis and AC analysis are shown in Fig. 4. 39 and Fig. 4. 40, respectively. Because the gain of the amplifier is very high, 76.686dB. The amplitude (10uV) of sinewave test signal (red curve) is relatively lower than the output signal (green curve). Thus, we only can see the output sinewave in the common window. As we can see the dc level of input is 400mV. The dc level of output is 665.916mV, which is easier to get a high swing. Because the power supply is 1.2V that is nearly the double dc level of output.

Chapter 5 Radiation Sensor Output Circuit Design

In this chapter, two main types of output circuits, low-pass filter and single-ended output, are presented. The overall layout of dosimeter is illustrated at the end of this chapter.

5.1 Pre-filter Circuit Design

In order to eliminate the effect of the filter to chopper amplifier, a pre-filter is designed and placed between chopper amplifier and low-pass filter as shown in Fig. 5. 1. This circuit consists of two groups of PMOS current mirrors as shown in Fig. 4. 5, which can exactly track the input signal and keep the dc level. The layout of this pre-filter is presented in Fig. 5. 2.

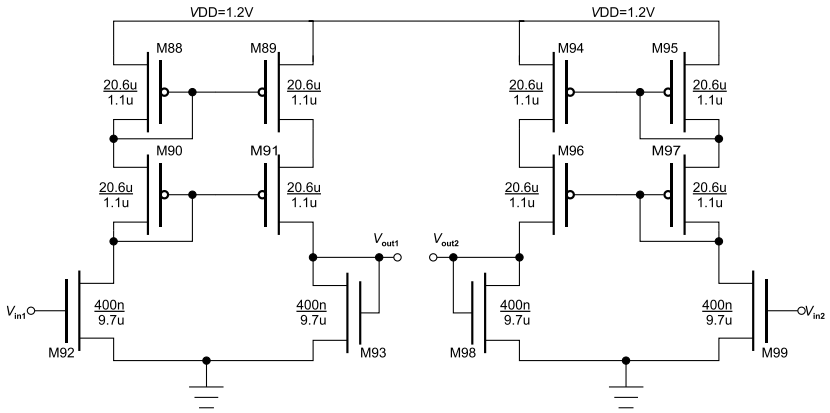


Fig. 5. 1 The schematic of pre-filter circuit

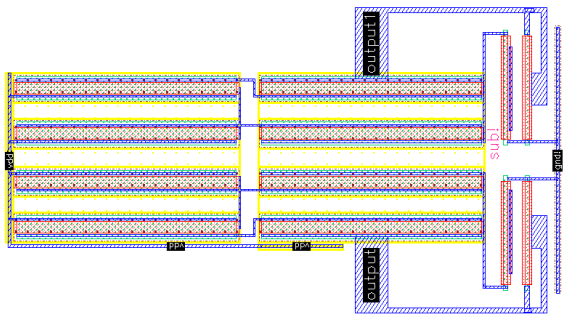


Fig. 5. 2 The layout of pre-filter circuit

The transient analysis of pre-filter is plotted in Fig. 5. 3. The dc level of input and output signal are almost same about 665mV.

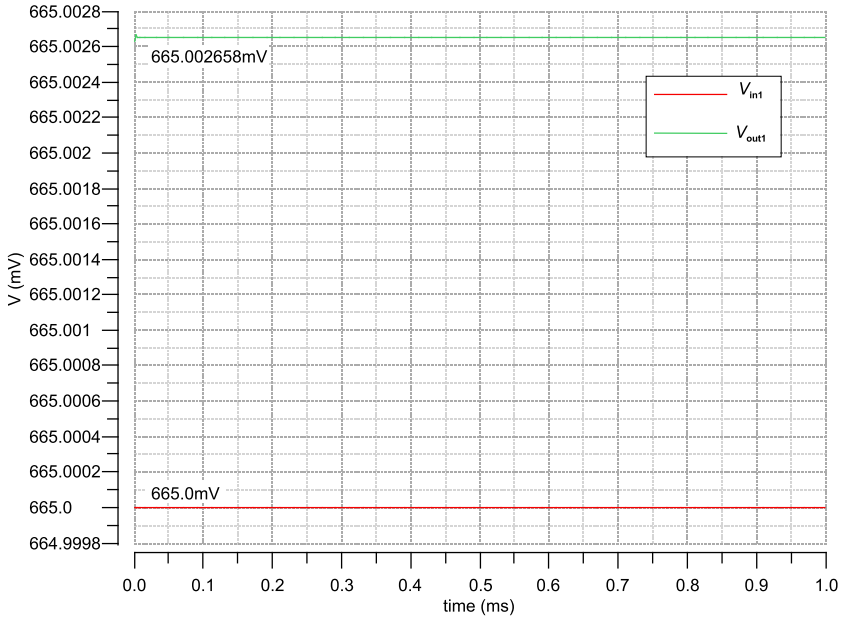


Fig. 5. 3 The transient analysis of pre-filter.

5.2 Four-order Low-pass Filter Circuit Design

The block diagram of low-pass filter consists four single stage and four external 1nF capacitors as shown in Fig. 5. 4. The aim to design a low-pass filter is to filter the residual offset and spike noise voltage as described in section 4.5. Each stage of the low-pass filter is the same circuit and made up by six transistors as presented in Fig. 5. 5 and its layout depicted in Fig. 5. 6.

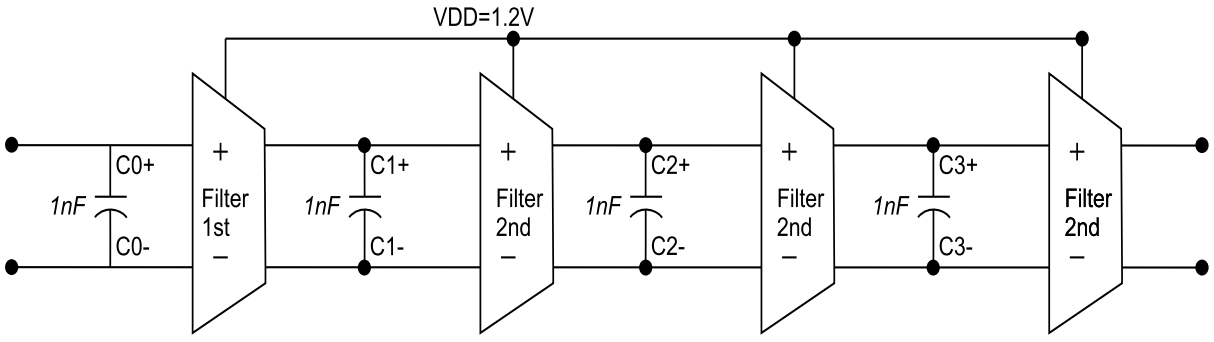


Fig. 5. 4 A four-stage low-pass filter.

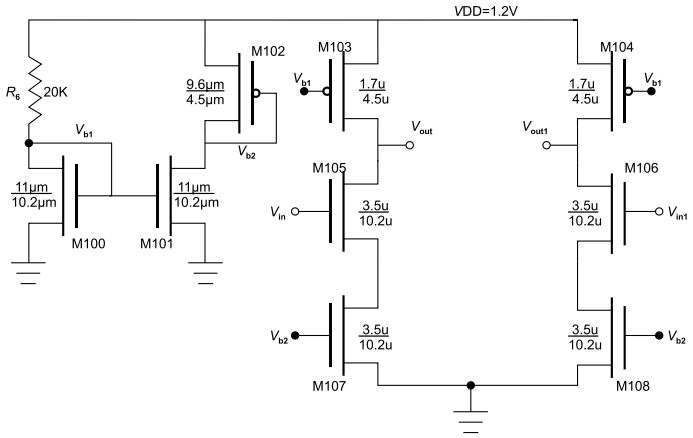


Fig. 5. 5 The schematic of the low-pass filter for stage1, 2, 3 and 4. This same circuit is used for each stage. A 1nF capacitor is connected between Vin and Vin1 as shown in Fig. 5.4.

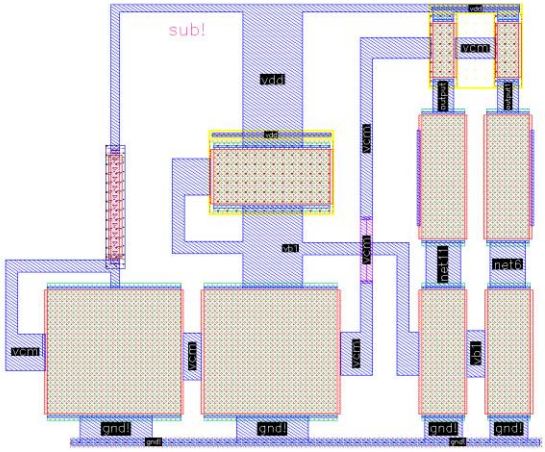


Fig. 5. 6 The layout of single stage for low-pass filter

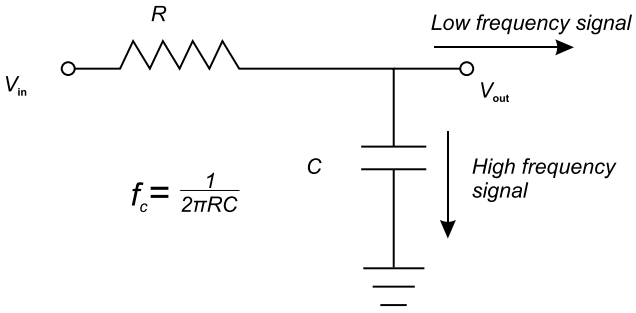


Fig. 5. 7 The schematic of first order low pass filter

The schematic of first order low pass filter is shown in Fig. 5. 7 [49]. This is a simple schematic to illustrate how the low pass filter works. It is composed of a resistor and an external capacitor (*1nF*). This resistor is provided by the gate resistance (M105) in Fig. 5. 5. The cutoff frequency is:

$$f_C = \frac{1}{2\pi RC} \tag{5.1}$$

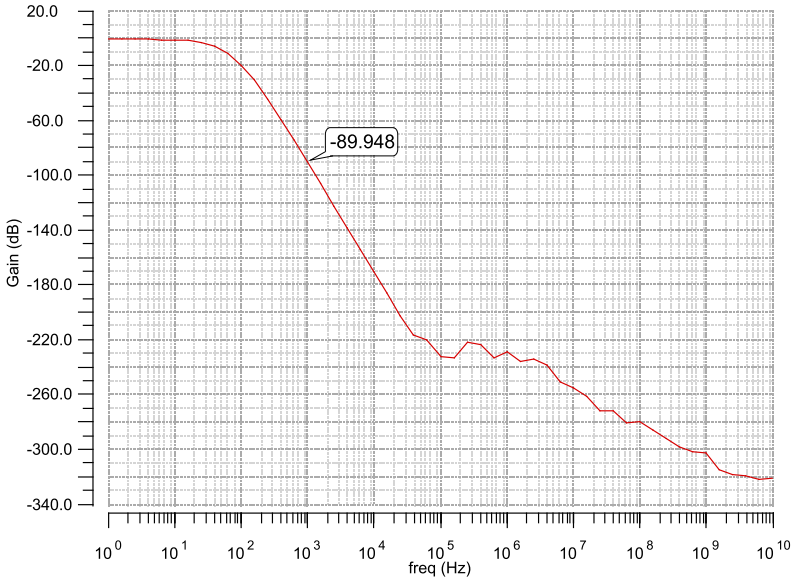


Fig. 5. 8 AC analysis of four-stage low-pass filter.

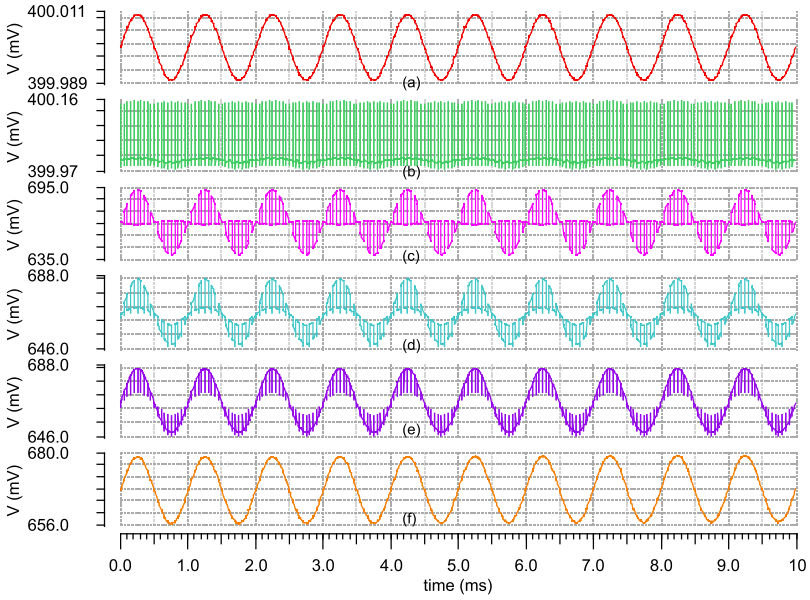


Fig. 5. 9 The simulation results of the chopper with a sinewave input.

(a) A sinewave input as the test signal. (b) Chopped sinewave in a 10K Hz chopping frequency. (c) Amplified signal. (d) The output from the buffer. (e). Demodulated sinewave in a 10K Hz de-chopping frequency. (f) The output of the low-pass filter.

When the value of input signal frequency is higher than the cutoff frequency f_C, it will flow through the capacitor. Because the capacitor provides a very low-resistance path for high frequency and high-resistance for low frequency. Current always choose the least-resistance path to go. Therefore, we will get the low-frequency signals that lower than f_c at the output.

The AC analysis of this filter is shown in Fig. 5. 8. From 0-10 Hz, the gain is about 0dB. When the frequency is 10k Hz, the gain is -89.948dB. Therefore, a low-pass filter can filter the chopped residual offset and spike noise (10k Hz).

Fig. 5. 9 shows the transient analysis of low-pass filter. A sinewave (a) is set as the test signal. The input signal is chopped (b), amplified (c), buffered (d), demodulation chopped (e) and filtered. We can see that low-pass filter filters the residual offset and spike noise voltage (e) successfully.

5.3 Single-ended Output Circuit Design

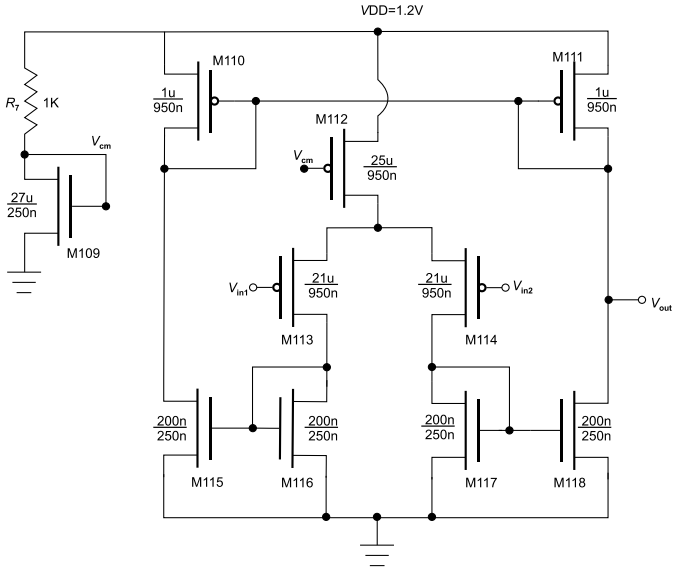


Fig. 5. 10 The schematic of Single-ended Output

In most applications, the output of the whole circuit is single-ended. It is convenient for processing and reading the signal in the next stage. Thus, the single-ended output circuit is also designed as shown in Fig. 5. 10. M113 and M114 are common source amplifier. They pass the input signal to the current mirror of M115-M118. Finally, current mirrors of M110 and M111 combine the signal input1 and input2 to the output. Moreover, the phase of input1 is opposite with output. When the input1 signal rises, the drain to source current of PMOS M113 decreases, which will be mirrored to the output current. It is easier to read radiation dose rate with an opposite phase of the single-ended output circuit. According to the equation 3.21 and 3.22, the variation of floating gate voltage is opposite with dose rate. Therefore, the output signal from single-ended output circuit directly represents the number of dose rate. The layout of this circuit is presented in Fig. 5. 11. The transient analysis of single-ended output circuit is shown in Fig. 5. 12.

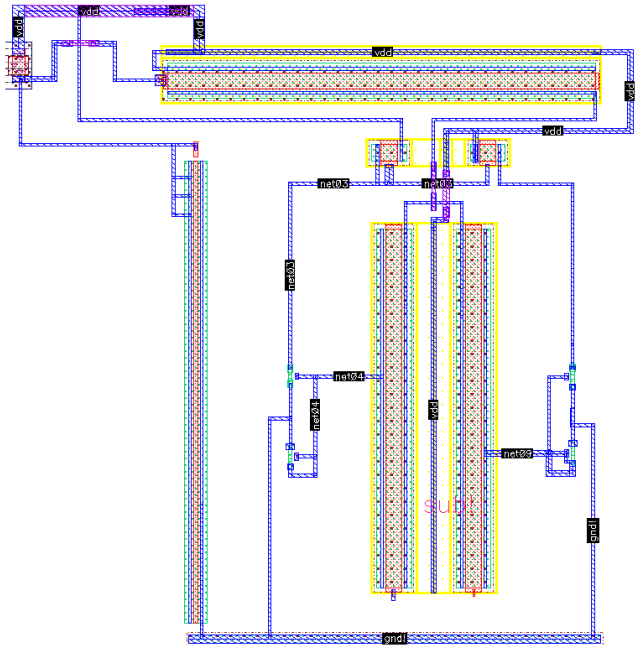


Fig. 5. 11 The layout of Single-ended Output

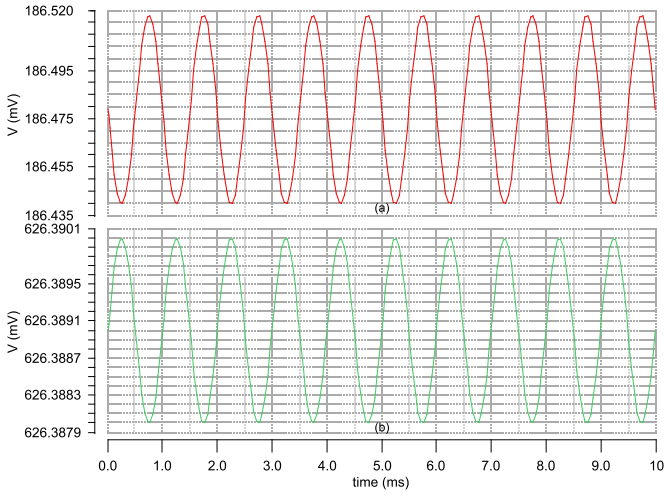


Fig. 5. 12 The simulation results of Single-ended Output.

(a) Output signal. (b) A sinewave input as the test signal.

5.4 Overall Layout for The Dosimeter

The overall layout for the dosimeter is shown in Fig. 5. 13, which includes FG voltage readout, differentiator, pre-amplifier buffer, chopper modulator, two-stage amplifier, buffer, chopper

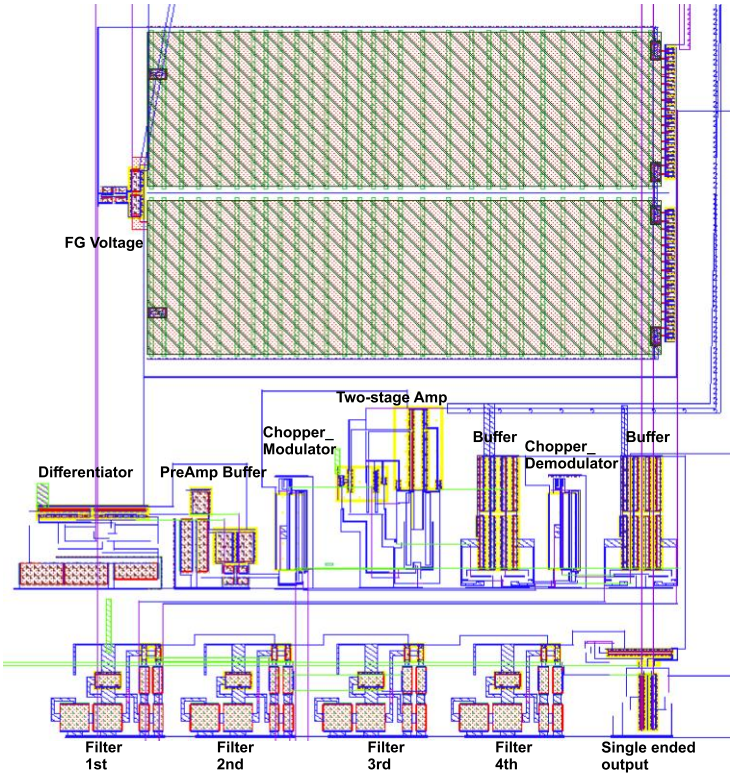


Fig. 5. 13 The overall layout for the dosimeter

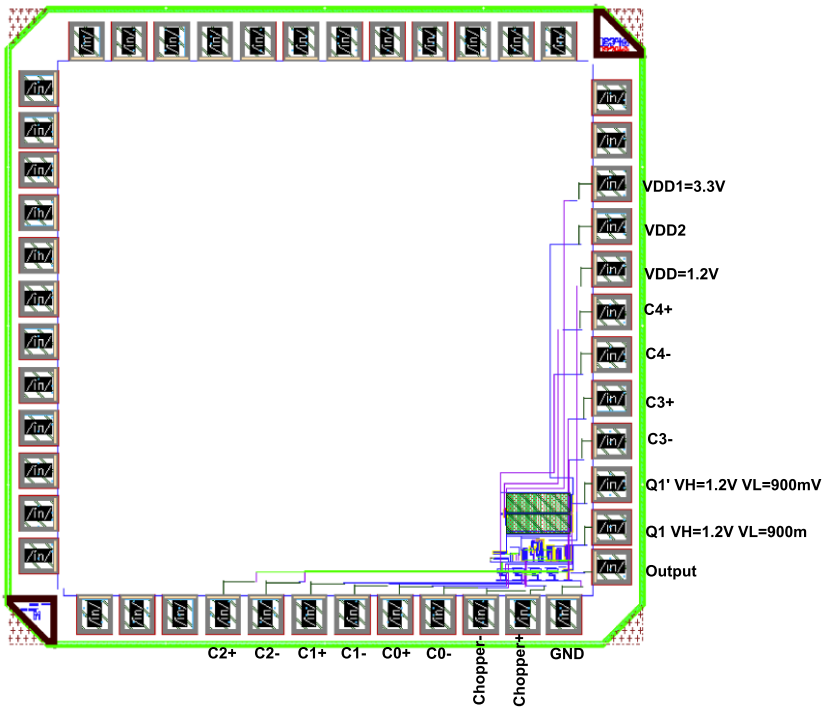


Fig. 5. 14 The overall layout for the dosimeter sitting in the *2mm×2mm* chip

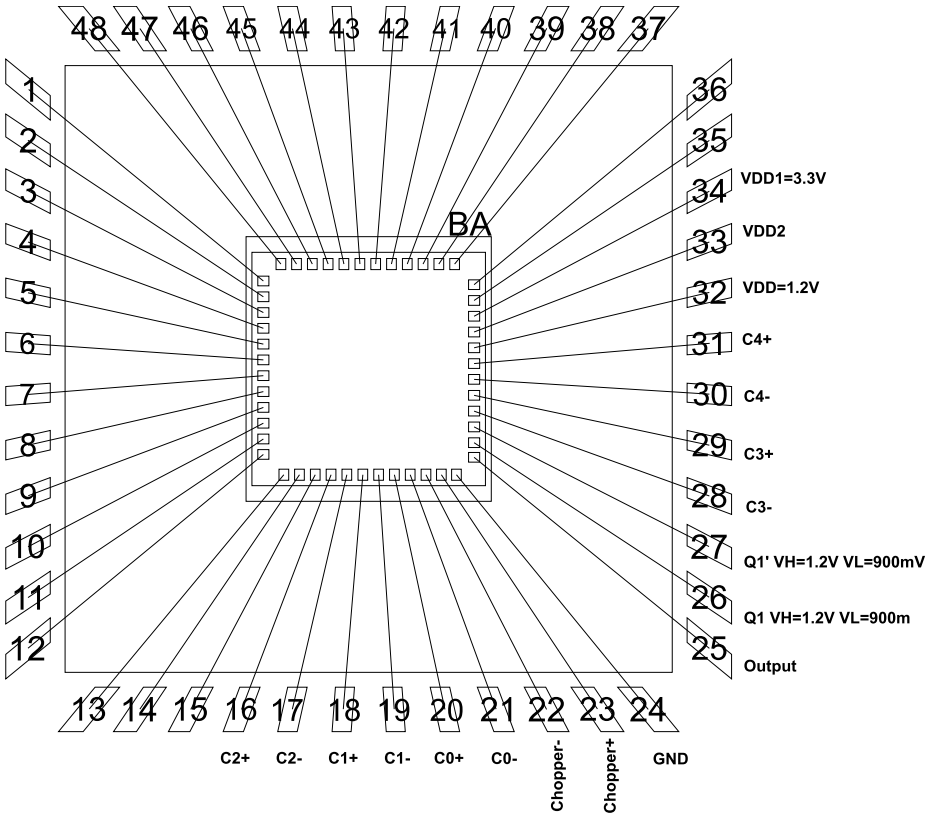


Fig. 5. 15 The Chip package

demodulator, low-pass filter and single-ended output. The layout is extracted from block schematic as same as Fig. 4. 1 and it corresponds to the schematic diagram one by one. Fig. 5. 14 shows the dosimeter chip *(2mm×2mm)*, which has 19 pins that have been described in section 4.1. The empty area is used by Ms. Meera Kumari, Ms. Sara Han, my great colleagues, who are pursuing Ph.D. degree in Massey University. We share a chip to save some resource. Finally, the package of this chip is shown in Fig. 5. 15. The pin numbers of 16-34 are same with 19 pins shown in Fig. 5. 14.

Chapter 6 Simulation and Experimental Analysis

This chapter introduces transient analysis for the whole circuit which is colse to the real result of the dosimeter. DRC, LVS and PEX simulation for the whole layout are also presented.

6.1 Transient Analysis for The Whole Circuit

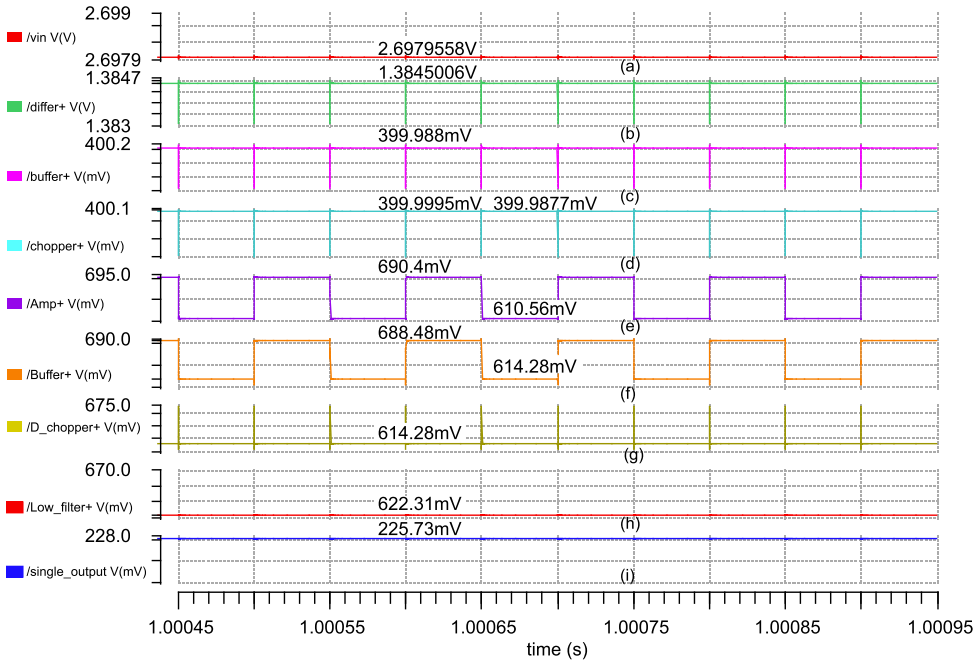


Fig. 6. 1 Transient analysis for the whole circuit.

Transient analysis for the whole circuit is shown in Fig. 6. 1, which is simulated in spectre language presented in Appendix D. From (a) to (i), These curves are input signal Vin (a), differentiator's positive output (b), buffer's positive output (c), chopper's positive output (d), amplifier's positive output (e), buffer's positive output (f), demodulation chopper's positive output (g), low-pass filters' positive output (h) and single-ended output (i). The input signal (a) has a slop of 1mV per second decreasing owing to the ionizing radiation. Differentiator senses the slope of the input signal. Then buffer shifts the dc level of differentiator's output to 399.988mV (c). Chopper modulates the slope signal to 399.9995mV and 399.9877mV (d). Next, the two-stage amplifier amplifies the modulated signal to 690.4mV and 610.56mV (e). The buffer is used again to reduce the effect between the demodulation chopper and two-stage amplifier. Demodulation chopper chops the signal back to 614.28mV. Then, the low-pass filter filters the residual offset and spike noise voltage. Finally, single-

ended circuit combines the filters' positive output and negative output to single-ended output (i), which represents the slope of the input signal that also is called dose rate.

Fig. 6. 2 shows the variation of single-ended output along with dose rate. It exhibits a nonlinear variation and rising trend. When the dose rate is 0.23mGy/s, the single-ended output voltage is 225.7369mV. When the dose rate is 2.3mGy/s, the single-ended output voltage 967.4426mV.

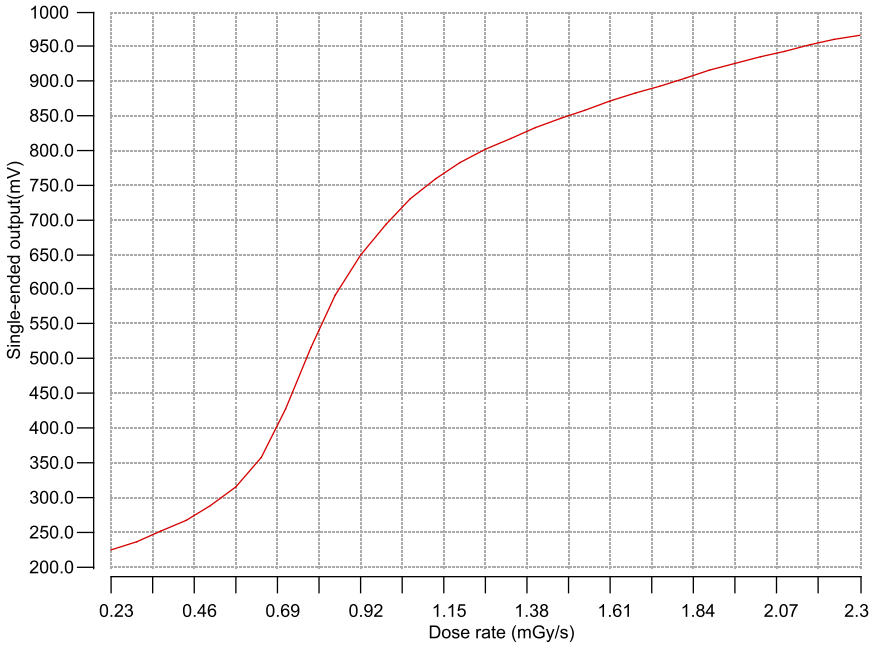


Fig. 6. 2 The plot of the single-ended output voltage vs. the dose rate.

6.2 DRC, LVS and PEX Analysis for The Whole Layout

When the layout of design is finished and sent the to foundry, they only check Design Rule Check (DRC) simulation. If there are any errors, they cannot fabricate this chip. Thus, DRC is very important. At the same time, it is very trivial, for example, the CA to CA and M1 to M1 space should be wider than 0.28um, the space of RX(N^+) to adjacent NW should be bigger than 0.3um and so on.

After DRC simulation, the Layout vs Schematic (LVS) simulation should be done until there is no extraction warning and comparison results are clean. It is to check whether Layout and Schematic are consistent.

The last step for layout is Practices Extraction (PEX) analysis, which extracts the parasitic wire capacitances and resistances from the layout. Check the .pex netlist, we can see hundreds and thousands of resistors and capacitors in the netlist. It is very necessary to do PEX simulation for the

highest level of accuracy. It is helpful for us to predict the delay of the design and power dissipation through these capacitances and resistances.

Chapter 7 Conclusion and Future Work

7.1 Conclusion

In conclusion, a CMOS radiation sensor is designed in 130nm CMOS technology, which achieves the detection of massive ionizing radiation and has a 3.205mW power consumption and 2.33mGy - 23mGy measuring range.

The main achievements of this research:

(1) Building a new FGMOSFET device model to facilitate circuit design.

(2) Designing a FGRADFET sensor that has an extra silicon area $125\mu m \times 200\mu m$ as an antenna to sense the radiation from the environment and 16 PMOS transistors ($1\mu m \times 2\mu m$ *each*) beneath the edge of the antenna to charge the floating gate.

(3) Designing a series of readout circuits that include differentiator, pre-amplify buffer, chopper amplifier, low-pass filter and single-ended output amplifier.

7.2 Future Work

Further research could be implemented to improve this integrated dosimeter. These improvements include:

(1) Using more advanced industry standard 28nm CMOS technologies, which can minimize the size and power consumption of the whole design, and enhance the overall performance of this radiation sensor.

(2) Using more accurate MOSFET model to build the FGMOSFET model.

(3) Designing an integrated phase locked loop (PLL) and integrated voltage control oscillator (VCO) to produce a precise clock signal for chopper amplifier.

(4) Designing another radiation sensor that has the ability to work continuously and does not need charging.

(5) Designing an integrated RF circuit to equip a wireless function for this dosimeter.

References

[1] Price, S. G., Silvius, A. A., & Izaguirre, E. W. "Feasibility study and first results of a real time imaging dosimeter for external beam radiation therapy." In *Nuclear Science Symposium and Medical Imaging Conference (NSS/MIC)*, 2011 IEEE (pp. 2822-2826), Oct. 2011.

[2] Fontbonne, J. M., Iltis, G., Ban, G. A., Battala, A., Vernhes, J. C., Tillier, J., ... & Motin, J. C. "Scintillating fiber dosimeter for radiation therapy accelerator." *IEEE Transactions on Nuclear Science*, *49(5)*, 2223-2227, 2002.

[3] Raphael, G., Berka, C., Kintz, N., Tan, V., Behneman, A., & Johnson, R. "Interactive Neuro-Educational Technologies (I-NET): Enhanced training of threat detection for airport luggage screeners." In *Technologies for Homeland Security (HST)*, 2010 IEEE International Conference on (pp. 536-542), Nov. 2010.

[4] Davis, V. A., Mandell, M. J., Baker, N. R., Brown-Hayes, M., Davis, G. T., Maurer, R. H., & Herrmann, C. "Surface-charging analysis of the radiation belt storm probe and magnetospheric MultiScale spacecraft." *IEEE Transactions on Plasma Science*, *40(2)*, 262-273, 2010.

[5] Brent R. "Pregnancy and Radiation Exposure. Health Physics Society website." Accessed at hps.org/hpspublications/articles/pregnancyandradiationexposureinfosheet.html, Jul. 2015.

[6] Yadegari, B. "Low Power Gamma-ray FG-MOSFET Dosimeter in 0.13 um CMOS Technology." (Doctoral dissertation, Carleton University), 2012.

[7] Siegbahn, K. (Ed.). "Alpha-, beta-and gamma-ray spectroscopy." Elsevier, 2012.

[8] Kawarabayashi, J., Mardiyanto, M. P., Uritani, A., Iguchi, T., Kaneko, J., & Takeuchi, H. "Digital waveform analysis for ^{3}He ionization chamber." *2000 IEEE Nuclear Science Symposium.* Conference Record (Cat. No.00CH37149), Lyon, pp. 9/193-9/195 vol.2, 2000.

[9] Meric, I., Johansen, G. A., Holstad, M. B., Calderon, A. F., & Gardner, R. P. "Enhancement of the intrinsic gamma-ray stopping efficiency of Geiger–Müller counters." *Nuclear Instruments and Methods in Physics Research Section A*: Accelerators, Spectrometers, Detectors and Associated Equipment, 696, 46-54, 2012.

[10] Furuta, E., & Kawano, T. "A plastic scintillation counter prototype." *Applied Radiation and Isotopes*, *104*, 175-180, 2015.

[11] Moreno, E. G., Picos, R., Isern, E., Roca, M., Bota, S., & Suenaga, K. "Radiation Sensor Compatible with Standard CMOS Technology." In *IEEE Transactions on Nuclear Science*, *56(5)*, 2910-2915, Oct. 2009.

[12] Fröhlich, L., Casarin, K., Quai, E., Holmes-Siedle, A., Severgnini, M., & Vidimari, R. "Online monitoring of absorbed dose in undulator magnets with RADFET dosimeters at FERMI@ Elettra." *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*, *703*, 70-79, 2013.

[13] Vasović, N. D., & Ristić, G. S. "A new microcontroller-based RADFET dosimeter reader." *Radiation Measurements*, *47(4)*, 272-276, 2012.

[14] Arsalan, M., Shamim, A., Shams, M., Tarr, N. G., & Roy, L. "Ultra-low power CMOS-based sensor for on-body radiation dose measurements." *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, *2(1)*, 34-41, 2012.

[15] Wang, Y., Wang, Y., Tarr, G., and Iniewski, K. "A temperature, supply voltage compensated floating gate MOS dosimeter using V/sub TH/extractor." In *System-on-Chip for Real-Time Applications*. Proceedings. Fifth International Workshop on IEEE, 176-179, Jul. 2005.

[16] Rodriguez-Villegas, E., and Barnes, H. "Solution to trapped charge in FGMOS transistors." *IEEE Electronics Letters*, *39(19)*, 1416-1417, 2003.

[17] Hasler, P., Minch, B. A., and Diorio, C. "Adaptive circuits using pFET floating-gate devices." In *Advanced Research in VLSI*. Proceedings. 20th Anniversary Conference on IEEE, pp. 215-229, Mar. 1999.

[18] Ochoa-Padilla, J. L., Gomez-Castañeda, F., and Moreno-Cadenas. J. A. "Floating-Gate MOS charge programming using pulsed hot-electron injection." *In Electrical Engineering, Computing Science and Automatic Control (CCE)*. 10th International Conference on IEEE, pp. 478-481, Sep. 2013.

[19] Basu, A., and Hasler, P. "A fully integrated architecture for fast programming of floating gates." In *Circuits and Systems*, 2007. ISCAS 2007. International Symposium on IEEE, pp. 957-960, May. 2007.

[20] Compagnoni, C. M., Ielmini, D., Spinelli, A. S., & Lacaita, A. L. "Modeling of tunneling P/E for nanocrystal memories." in *IEEE Transactions on Electron Devices*, *52(4)*, 569-576, Apr. 2005.

[21] Tarr, N. G., Shortt, K., Wang, Y., & Thomson, I. "A sensitive, temperature-compensated, zero-bias floating gate MOSFET dosimeter." *IEEE Transactions on Nuclear Science*, *51(3)*, 1277-1282, 2004.

[22] Pease, R. L., Simons, M., & Marshall, P. "Comparison of pMOSFET total dose response for Co-60 gammas and high-energy protons." *IEEE Transactions on Nuclear Science*, *48(3)*, 908-912, 2001.

[23] Pavan, P., Larcher, L., Cuozzo, M., Zuliani, P., & Conte, A. "A complete model of E2PROM memory cells for circuit simulations." In *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, *22(8)*, 1072-1079, Aug. 2003.

[24] Scheick, L. Z., McNulty, P. J., & Roth, D. R. "Measurement of the effective sensitive volume of FAMOS cells of an ultraviolet erasable programmable read-only memory." In *IEEE Transactions on Nuclear Science*, *47(6)*, 2428-2434, Dec. 2000.

[25] Saheb, Z. "Transit and dc model of floating gate transistor in 90nm CMOS technology." (Doctoral dissertation), 2013. Accessed at http://dalspace.library.dal.ca/handle/10222/31441

[26] Saheb, Z., & El-Masry, E. "Practical Simulation Model of Floating-Gate MOS Transistor in Sub 100nm Technologies." *World Academy of Science, Engineering and Technology, International Journal of Electrical, Computer, Energetic, Electronic and Communication Engineering*, *9*(8), 857-861, 2015.

[27] Larcher, L., Pavan, P., Pietri, S., Albani, L., & Marmiroli, A. "A new compact DC model of floating gate memory cells without capacitive coupling coefficients." In *IEEE Transactions on Electron Devices*, *49(2)*, 301-307, Feb. 2002.

[28] Angelov, G., Panayotov, I., and Hristov, M. "EKV MOSFET model implementation in Matlab and Verilog-A." In *Microelectronics*, 2008. MIEL 2008. 26th International Conference on IEEE, pp. 515-518. May. 2008.

[29] Zhou, Y., Li, Y., and Wang, B. “Spice modeling of 4H-SiC MOSFET based on the advanced mobility model.” In *Wide Bandgap Power Devices and Applications (WiPDA)*, 2016 IEEE 4th Workshop on IEEE, pp. 1-7, Nov. 2016.

[30] Rahimi, K., Diorio, C., Hernandez, C., and Brockhausen, M. D. “A simulation model for floating-gate MOS synapse transistors.” In *Circuits and Systems*, 2002. ISCAS 2002. IEEE International Symposium on, IEEE, Vol. 2, pp. II-II, 2002.

[31] Thomsen, A., & Brooke, M. A. “A floating-gate MOSFET with tunneling injector fabricated using a standard double-polysilicon CMOS process.” In *IEEE Electron Device Letters*, *12(3)*, 111-113, Mar. 1991.

[32] Cullinan, M. “Equation defined device modelling of floating gate MOSFETs” (Doctoral dissertation, London Metropolitan University). Accessed at Http://repository.londonmet.ac.uk/960/. 2015.

[33] Li, J., Joshi, S., Barnes, R., & Rosenbaum, E. “Compact modeling of on-chip ESD protection devices using Verilog-A.” *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, *25(6)*, 1047-1063, Jun. 2006.

[34] Wang, X., Xu, B., & Chen, L. “Efficient Memristor Model Implementation for Simulation and Application.” In *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol, PP, no. 99, pp.1-1, 2017.

[35] Aguirre, C., and Wirth, G. “Simulation of TID effect on floating gate cells.” In *Microelectronics Technology and Devices* (SBMicro), 2013 Symposium on IEEE, pp. 1-5, Sep. 2013.

[36] Tarr, N. G., Shortt, K., Wang, Y., and Thomson, I. “A sensitive, temperature-compensated, zero-bias floating gate MOSFET dosimeter.” *IEEE Transactions on Nuclear Science*, *51(3)*, 1277-1282, 2004.

[37] Martin, M. N., Roth, D. R., Garrison-Darrin, A., McNulty, P. J., & Andreou, A. G. “FGMOS dosimetry: Design and implementation.” *IEEE Transactions on Nuclear Science*, *48(6)*, 2050-2055, 2001.

[38] Garcia-Moreno, E., Isern, E., Roca, M., Picos, R., Font, J., Cesari, J., & Pineda, A. “Floating gate CMOS dosimeter with frequency output.” *IEEE Transactions on Nuclear Science*, *59(2)*, 373-378, 2012.

[39] Garcia-Moreno, E., Isern, E., Roca, M., Picos, R., Font, J., Cesari, J., & Pineda, A. “Temperature compensated floating gate MOS radiation sensor with current output.” *IEEE Transactions on Nuclear Science*, *60(5)*, 4026-4030, 2013.

[40] Scheick, L. Z., & McNulty, P. J. “Floating Gate Dosimetry Based on Measurement of Incremental Charge Injection.” Http://s3.amazonaws.com/zanran_storage/parts.jpl.nasa.gov/ContentPages/16477365.pdf

[41] Tarr, N. G., Shortt, K., Wang, Y., and Thomson, I. “A sensitive, temperature-compensated, zero-bias floating gate MOSFET dosimeter.” *IEEE Transactions on Nuclear Science*, *51(3)*, 1277-1282, 2004.

[42] Ragheb, A. N., Mohamed, M. G. A., & Kim, H. “Differentiator based sensing circuit for efficient noise suppression of projected mutual-capacitance touch screens.” In *Electronics, Information, and Communications (ICEIC)*, 2016 International Conference on (pp. 1-5), Jan. 2016.

[43] Sheikholeslami, A. “Chopper Amplifier [Circuit Intuitions].” in *IEEE Solid-State Circuits Magazine*, 8(2), pp. 7-9, Spring 2016.

[44] Zhao, X., Chebli, R., & Sawan, M. "A wide tuning range voltage-controlled ring oscillator dedicated to ultrasound transmitter." In *Microelectronics, 2004. ICM 2004 Proceedings*. The 16th International Conference on (pp. 313-316), Dec. 2004.

[45] Behzad, R. "Design of analog CMOS integrated circuits." *International Edition*, 400, 2001.

[46] Milovanović, V., & Zimmermann, H. "On fully differential and complementary single-stage self-biased CMOS differential amplifiers." In *EUROCON*, 2013 IEEE (pp. 1955-1963), Jul. 2013.

[47] Hasan, S. R. "Novel inspection-based mid-band derivations for CMOS cascodes and gm-boosted topologies along-with simplified compound structure gain-analysis." *Analog Integrated Circuits and Signal Processing, 91(1)*, 21-41, 2017.

[48] Rezaul Hasan, S. M. "Simplified analog CMOS mid-band small-signal analysis utilizing short-circuits and incremental perturbations." *International Journal of Electrical Engineering Education (IJEEE), 52(4)*, 356–369, 2015.

[49] Rosales, E. B. O., & Ibarra, F. S. "A 100Hz Low-Pass 2nd Order Sallen-and-Key Active Filter: A Design Proposal." in *IEEE Latin America Transactions*, *12(2)*, 73-77, Mar. 2014.

Appendix A

1. THE KEY VERILOG-A CODE OF THE PROPOSED OPEN SOURCE FGMOSFET MODEL

```
/*Calculate the induced floating-gate voltage due to
quantity of tunneling charge and the gate voltage */

@(cross(V(vtun)-vgs, +1)) begin
   t1=$abstime;
end
@(cross(V(vtun), -1)) begin
   t2=$abstime;
end
if(V(vtun)>vgs) begin
   flag=1;
   vox=V(vtun)-V(Vfg);
   V(Vfg)<+ (cg/cT)*vgs +((roh*WT*LT)/(cT*tox*
   tox))*vox*vox*exp(-theta*tox/vox)*($abstime-t1);
end else
   if(flag==0)
```

2. THE VERILOG-A CODE OF THE PROPOSED VARIABLE FLOATING GATE VOLTAGE

```
/*Variable floating gate voltage under the ionizing
radiation in Verilog-A*/

`include "constants.vams"
`include "disciplines.vams"
module Vout (Vfg, Dose);
input Dose;
output Vfg;
electrical Dose,Vfg;
real c;
analog begin
V(Vfg)<+2.7-V(Dose)*$abstime;
end
endmodule
```

Appendix B

```
%%%%%%%%%%%%%%%%%%%%%%%%MOSFET level 1 model in MATLAB%%%%%%%%%%%%%%%%%%
%vgs=2;
vbs=0;
u0 = 600;
EPS0=8.8541879239442001396789635e-12;
EPS_OX=3.9*EPS0/100.0;
tox = 1e-7;
width = 1e-6;
length = 3e-6;
xj = 0;
vto = 1;
gamma = 0.05;
phi = 0.6;
lambda = 0.05;
vth = vto + gamma*sqrt (2*phi + vbs);
leff = length - 2*xj;
kp = u0*EPS_OX/tox;
beta = kp*width/leff;
 %%vds1=0:0.1: vgs-vth;
   for vgs=1.0548: 0.4 :3
      vds2=vgs-vth:0.1: 5;
      vds1=0:0.1: vgs-vth;
      id1 = beta*(vgs - vth - vds1/2). *vds1. *(1 + lambda*vds1);       %Triode region
      id2 = beta*0.5*(vgs - vth) *(vgs - vth) *(1 + lambda*vds2);       %Saturation region
   plot (vds1, id1, 'k', vds2, id2, 'k');
   hold all;
   end
   title (' Id-Vds');
   xlabel('Vds(V)');
   ylabel('Id(A)');
legend ('Vgs=0V', 'Vgs=1V','Vgs=2V', 'Vgs=3V', 'Vgs=4V');

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%Test Ib ionizing%%%%%%%%%%%%%%%%%%%%%%%%%
x=1: 1: 4;
Idb=[];
b=2.985;
Vds=3.6;
d=1.985;
Vdfg=3;
Vth=0.7;
Vbi=(b*Vds-d*Vdfg+Vth);
Ids=1e-12;
a=1.127;
c=94.85;
Is=0;
for number=1: 1: 4
 Idb= [Idb (a*(Ids)*Vbi*exp((-c)/Vbi))];
% Idb=Idb*100;
 Ids=Ids*100;
end;
plot (x, Idb, 'r-d');

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%Test injection charge%%%%%%%%%%%%%%%%%%%%%%%%%
%Is=linspace(10e-12, 10e-4, 31);
%Iihi=(1.30e-5)*Is*exp(-155.75/((1+0.702)*1.702)+3.6);
%plot(Is, Iihi);
vgs=2;
vbs=0;
u0 = 600;
EPS0=8.8541879239442001396789635e-12;
EPS_OX=3.9*EPS0/100.0;
tox = 1e-7;
width = 1e-6;
length = 3e-6;
xj = 0;
vto = 1;
gamma = 0;
phi = 0.6;
lambda = 0.05;
vth = vto - gamma*(sqrt(2*phi - vbs) - sqrt(2*phi));
```

```
leff = length - 2*xj;
kp = u0*EPS_OX/tox;
beta = kp*width/leff;
      vds1=0:0.01: vgs-vth;
      vds2=vgs-vth:0.01: 5;
      id1 = beta*(vgs - vth - vds1/2).*vds1.*(1 + lambda*vds1);
      id2 = beta*0.5*(vgs - vth)*(vgs - vth)*(1 + lambda*vds2);
      Iihi1=(1.30e-5)*id1.*exp(-155.75/((2+0.702)*3.702)+vds1);
      Iihi2=(1.30e-5)*id2.*exp(-155.75/((2+0.702)*3.702)+vds2);
   plot (vds1, Iihi1, 'r', vds2, Iihi2, 'r');
   hold all;

%%%%%%%%%%%%%%%%%%%%%%%%Test tunnelling current%%%%%%%%%%%%%%%%%%%%%
x = 8: 0.05: 9;
Itun1 = [];
for Vox=8: 0.05: 9
   Itun1 = [Itun1 ((9.35e+8)*exp(-368.04/Vox))];
end
plot (x, Itun1, '-d');
%Itun1=(9.35e+8)*exp(-368.04/Vox);
%plot (Vox, Itun1, '-d');
%hold all

%%%%%%%%%%%%%%%%%%%%%%%%Test Diode%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
is=1e-14;
vt=25.85e-3;
for Vdb=0:0.01:1
Ibd=is*(exp(-Vdb/vt)-1);
plot( Vdb, Ibd, '-d');
hold on;
end;
```

Appendix C

```
//FGMOSFET model in verilog A
`include "discipline.h"
`include "constants.h"

`define n_type 1
`define p_type 0

module mos_level1(vdrain, vgate, vsource, vtun, vbody, Vg);
inout vdrain, vgate, vsource, vbody, vtun, Vg;
electrical vdrain, vgate, vsource, vbody, vtun, Vg;
parameter real width = 0.1n from (0:inf);          //  width  = [m]
parameter real length = 0.3n from (0:inf);         //  length = [m]
parameter real vto = 0.2 from (0:inf);             //  vto    = threshold voltage [V]
parameter real gamma =0 from [0:inf);              //  gamma  = bulk threshold []
parameter real phi = 0.6 from (0:inf);             //  phi    = bulk junction potential [V]
parameter real lambda = 0.05 from [0:inf);         //  lambda = channel length modulation []
parameter real tox = 1e-7 from (0:inf);            //  tox    = oxide thickness []
parameter real u0 = 600 from (0:inf);              //  u0     = transconductance factor []
parameter real xj = 0 from [0:inf);                //  xj     = metallurgical junction depth []
parameter real is = 1e-14 from (0:inf);            //  is     = saturation current []
parameter real cj=0 from [0:inf);                  //  cj     = bulk junction capacitance [F]
parameter real vj=0.75 exclude 0;                  //  vj     = bulk junction voltage [V]
parameter real mj=0.5 from [0:1);                  //  mj     = bulk grading coefficient []
parameter real fc=0.5 from [0:1);                  //  fc     = forward bias capacitance factor []
parameter real tau = 0 from [0:inf);               //  tau    = parasitic diode factor []
parameter real cgbo = 0 from [0:inf);              //  cgbo   = gate-bulk overlap capacitance [F]
parameter real cgso = 0.554p from [0:inf);         //  cgso   = gate-source overlap capacitance [F]
parameter real cgdo = 59.24f from [0:inf);         //  cgdo   = gate-drain overlap capacitance [F]
parameter real cg = 4p from [0:inf);               //  cg   = gate-floating gate overlap capacitance [F]
parameter integer dev_type = `n_type;              //  dev_type   = the type of mosfet used []
parameter real itun0 = 9.35e+8 from [0:inf);       //  itun0   = a pre-exponential current [A]
parameter real vf = 368.04 from [0:inf);           //  vf   = a constant that varies with oxide thickness []
parameter real Time =1e-3 from [0:inf);            //  Time   = Charge time []
//parameter real vtun = 9 from [0:inf);            //  vtun   = tunneling voltage [F]

`define EPS0                                       8.85418792394420013967896 35e-12
`define EPS_OX                                     3.9*`EPS0/100.0

`define F1(m, f, v)  ((v/(1 - m))*(1 - pow((1 - f), m)))
`define F2(m, f)     (pow((1 - f), (1 + m)))
`define F3(m, f)     (1 - f*(1 + m))

  //
  // visible variables.
  //
  real vds,  vgs, vbs, vbd, vgb, vgd, vth, vfg, vts, vox, VG, id, ibs,   ibd, qgb, qgs, qgd, qbd, qbs, ct, power,  gm, gds, ro;
  real   t1, t2, flag=0; // charging parameters
  real kp, fc1, fc2, fc3, fpb, leff;
  real beta;
  integer dev_type_sign;

  analog begin

@ ( initial_step or initial_step("static") ) begin
 leff = length - 2*xj;
 kp = u0*`EPS_OX/tox;
fc1 = `F1(mj, fc, vj);
fc2 = `F2(mj, fc);
fc3 = `F3(mj, fc);
 fpb = fc*mj;
 ct=cgso+cgdo+cg;
 vfg=0;

 if( dev_type == `n_type )  dev_type_sign =1;
else dev_type_sign = -1;
end
     vds = dev_type_sign*V(vdrain, vsource);
//   vgs = dev_type_sign*(V(vgate, vsource)*(cg/ct)+(1/ct)*itun0*exp(-vf/9.2)*(1e-3));
     vgs = dev_type_sign*V(vgate, vsource);
     vgb = dev_type_sign*V(vgate, vbody);
     vgd = dev_type_sign*V(vgate, vdrain);
```

```
    vbs = dev_type_sign*V(vbody, vsource);
    vbd = dev_type_sign*V(vbody, vdrain);
    vts =dev_type_sign*V(vtun,  vsource);
//  vox=vts+vto;
    if (vbs > 2*phi) begin
      vth =dev_type_sign* (vto - gamma*sqrt(2*phi));
    end else begin
      vth =dev_type_sign* (vto + gamma*(sqrt(2*phi - vbs) - sqrt(2*phi)));
    end
                                                                    //
    //the voltage charged by tunneling
                                                                    //
/*@(cross(V(vtun)-vgs, +1)) begin
      t1=$abstime;
   end
   @(cross(V(vtun), -1)) begin
      t2=$abstime;
   end
   if(V(vtun)>vgs) begin
      flag=1;
      V(Vg)<+(1/ct)*itun0*exp(-vf/(vox-V(Vg)))*($abstime-t1)*(vox-V(Vg))*(vox-V(Vg))+(cg/ct)*vgs;
   end else
   if(flag==0)
      V(Vg)<+(cg/ct)*vgs;
    else if(flag==1)
      V(Vg)<+(1/ct)*itun0*exp(-vf/(vox-V(Vg)))*(t2-t1)*(vox-V(Vg))*(vox-V(Vg))+(cg/ct)*vgs;*/

// V(Vg)<+vgs;                                                  //charged


@(cross(V(vtun)-vgs, +1)) begin
   t1=$abstime;
end
@(cross(V(vtun), -1)) begin
   t2=$abstime;
end
if(V(vtun)>vgs) begin
   flag=1;
   vox=vts;
   V(Vg)<+(1/ct)*itun0*exp(-vf/(vox-V(Vg)))*(vox-V(Vg))*(vox-V(Vg))*($abstime-t1)+(cg/ct)*vgs;
end else
if(flag==0)
   V(Vg)<+(cg/ct)*vgs;
else if(flag==1)
   V(Vg)<+(1/ct)*itun0*exp(-vf/(vox-V(Vg)))*(vox-V(Vg))*(vox-V(Vg))*(t2-t1)+(cg/ct)*vgs;
//
// parasitic diodes...
//
   ibd = is*(exp(vbd/$vt) - 1);
   ibs = is*(exp(vbs/$vt) - 1);

   if (vbd <= fpb) begin
   qbd = tau*ibd + cj*vj*(1 - pow((1 - vbd/vj), (1 - mj)))/(1 - mj);
   end else begin
   qbd = tau*ibd + cj*(fc1 + (1/fc2)*(fc3*(vbd - fpb) +
   (0.5*mj/vj)*(vbd*vbd - fpb*fpb)));
end

if (vbs <= fpb) begin
   qbs = tau*ibs + cj*vj*(1 - pow((1 - vbs/vj), (1 - mj)))/(1 - mj);
end else begin
   qbs = tau*ibs + cj*(fc1 + (1/fc2)*(fc3*(vbs - fpb) +
   (0.5*mj/vj)*(vbs*vbs - fpb*fpb)));
end

//
// channel component of drain current. (channel charge ignored)...
//
   beta = kp*width/leff;
if (vgs <= vth) begin
   id = 0;
end else if (vgs > vth && vds < vgs-vth) begin

//
// linear region.
```

```
//
    id = beta*(vgs - vth - vds/2)*vds*(1 + lambda*vds);
end else begin

//
// saturation region.
//
    id = beta*0.5*(vgs - vth)*(vgs - vth)*(1 + lambda*vds);
end
      gm  =ddx(id ,V(vgate));
      gds =ddx(id ,V(vdrain));
      ro  =1/ddx(id, V(vdrain));
      power =vds*id;
      qgb = cgbo * vgb;
      qgs = cgso * vgs;
      qgd = cgdo * vgd;
      I(vdrain, vsource) <+ dev_type_sign *  id;
      I(vbody, vdrain)   <+ dev_type_sign * (ibd + ddt(qbd));
      I(vbody, vsource)  <+ dev_type_sign * (ibs + ddt(qbs));
      I(vgate, vbody)    <+ dev_type_sign *  ddt(qgb);
      I(vgate, vsource)  <+ dev_type_sign *  ddt(qgs);
      I(vgate, vdrain)   <+ dev_type_sign *  ddt(qgd);
   end
endmodule
```

Appendix D

```
// Generated for: spectre
// Generated on: Sep 10 18:10:03 2017
// Design library name: Test
// Design cell name: Test_Dosimeter
// Design view name: schematic
simulator lang=spectre
global 0 sub!
parameters v=1m delay=1 VH=1.2 VL=900m Voffset=400m
include "$PDK_HOME/Spectre/models/design.scs"
include "$PDK_HOME/Spectre/models/allModels.scs" section=tt

// Library name: Test
// Cell name: Low_pass_filter
// View name: schematic
subckt Low_pass_filter in in1 _net0 output1 vdd inh_substrate
    T7 (vdd vb1 vb1 vdd) pfet l=4.5u w=9.6u nf=1 m=1 par=1 ngcon=1 \
        ad=5.28e-12 as=5.28e-12 pd=20.3u ps=20.3u nrd=0.0229 nrs=0.0229 \
        rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
        rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
        panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
        sb=5.5e-07 sd=0u dtemp=0
    T6 (_net0 vcm vdd vdd) pfet l=4.5u w=1.7u nf=1 m=1 par=1 ngcon=1 \
        ad=9.35e-13 as=9.35e-13 pd=4.5u ps=4.5u nrd=0.1294 nrs=0.1294 \
        rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
        rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
        panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
        sb=5.5e-07 sd=0u dtemp=0
    T3 (vdd vcm output1 vdd) pfet l=4.5u w=1.7u nf=1 m=1 par=1 ngcon=1 \
        ad=9.35e-13 as=9.35e-13 pd=4.5u ps=4.5u nrd=0.1294 nrs=0.1294 \
        rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
        rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
        panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
        sb=5.5e-07 sd=0u dtemp=0
    T2 (net11 vb1 0 inh_substrate) nfet l=10.2u w=3.5u nf=1 m=1 par=1 \
        ngcon=1 ad=1.925e-12 as=1.925e-12 pd=8.1u ps=8.1u nrd=0.0629 \
        nrs=0.0629 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
        lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
        panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
        sa=5.5e-07 sb=5.5e-07 sd=0u dtemp=0
    T1 (_net0 in net11 inh_substrate) nfet l=10.2u w=3.5u nf=1 m=1 par=1 \
        ngcon=1 ad=1.925e-12 as=1.925e-12 pd=8.1u ps=8.1u nrd=0.0629 \
        nrs=0.0629 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
        lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
        panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
        sa=5.5e-07 sb=5.5e-07 sd=0u dtemp=0
    T0 (output1 in1 net6 inh_substrate) nfet l=10.2u w=3.5u nf=1 m=1 par=1 \
        ngcon=1 ad=1.925e-12 as=1.925e-12 pd=8.1u ps=8.1u nrd=0.0629 \
        nrs=0.0629 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
        lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
        panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
        sa=5.5e-07 sb=5.5e-07 sd=0u dtemp=0
    T4 (0 vcm vcm inh_substrate) nfet l=10.2u w=11.0u nf=1 m=1 par=1 \
        ngcon=1 ad=6.05e-12 as=6.05e-12 pd=23.1u ps=23.1u nrd=0.02 \
        nrs=0.02 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
        lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
        panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
        sa=5.5e-07 sb=5.5e-07 sd=0u dtemp=0
    T38 (0 vcm vb1 inh_substrate) nfet l=10.2u w=11.0u nf=1 m=1 par=1 \
        ngcon=1 ad=6.05e-12 as=6.05e-12 pd=23.1u ps=23.1u nrd=0.02 \
        nrs=0.02 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
        lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
        panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
        sa=5.5e-07 sb=5.5e-07 sd=0u dtemp=0
    T5 (net6 vb1 0 inh_substrate) nfet l=10.2u w=3.5u nf=1 m=1 par=1 \
        ngcon=1 ad=1.925e-12 as=1.925e-12 pd=8.1u ps=8.1u nrd=0.0629 \
        nrs=0.0629 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
        lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
        panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
        sa=5.5e-07 sb=5.5e-07 sd=0u dtemp=0
    I7 (0 inh_substrate) subc l=4u w=2u dtemp=0
    OPrrp0 (vdd vcm inh_substrate) oprrpres w=740.00n l=8.49u r=20.01037K \
```

```
      sbar=1 m=1 par=1 sh=1 bp=3 dtemp=0.0 rsx=50
ends Low_pass_filter
// End of subcircuit definition.

// Library name: Test
// Cell name: mytest1
// View name: schematic
subckt mytest1 _net0 vdd1 inh_substrate
   V1 (net031 0) vsource dc=v type=dc
   I85 (Vfg net031) Vout
   T9 (net03 Vfg vdd1 vdd1) pfet33 l=3u w=8u nf=1 m=1 par=1 ngcon=1 \
      ad=4.8e-12 as=4.8e-12 pd=17.2u ps=17.2u nrd=0.0275 nrs=0.0275 \
      rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
      rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
      panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=6e-07 sb=6e-07 \
      sd=0u dtemp=0
   T10 (_net0 _net0 vdd1 vdd1) pfet33 l=3u w=8u nf=1 m=1 par=1 ngcon=1 \
      ad=4.8e-12 as=4.8e-12 pd=17.2u ps=17.2u nrd=0.0275 nrs=0.0275 \
      rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
      rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
      panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=6e-07 sb=6e-07 \
      sd=0u dtemp=0
   I55 (0 inh_substrate) subc l=4u w=2u dtemp=0
   T7 (net08 net08 0 inh_substrate) nfet33 l=2u w=4u nf=1 m=1 par=1 \
      ngcon=1 ad=2.4e-12 as=2.4e-12 pd=9.2u ps=9.2u nrd=0.055 nrs=0.055 \
      rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
      rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
      panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=6e-07 sb=6e-07 \
      sd=0u dtemp=0
   T6 (net017 net08 0 inh_substrate) nfet33 l=2u w=4u nf=1 m=1 par=1 \
      ngcon=1 ad=2.4e-12 as=2.4e-12 pd=9.2u ps=9.2u nrd=0.055 nrs=0.055 \
      rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
      rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
      panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=6e-07 sb=6e-07 \
      sd=0u dtemp=0
   T1 (net03 net03 net08 inh_substrate) nfet33 l=2u w=4u nf=1 m=1 par=1 \
      ngcon=1 ad=2.4e-12 as=2.4e-12 pd=9.2u ps=9.2u nrd=0.055 nrs=0.055 \
      rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
      rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
      panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=6e-07 sb=6e-07 \
      sd=0u dtemp=0
   T2 (_net0 net03 net017 inh_substrate) nfet33 l=2u w=4u nf=1 m=1 par=1 \
      ngcon=1 ad=2.4e-12 as=2.4e-12 pd=9.2u ps=9.2u nrd=0.055 nrs=0.055 \
      rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
      rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
      panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=6e-07 sb=6e-07 \
      sd=0u dtemp=0
ends mytest1
// End of subcircuit definition.

// Library name: Test
// Cell name: Two_stage_Amp
// View name: schematic
subckt Two_stage_Amp _net3 input1 _net2 output1 vdd inh_substrate
   T13 (vdd net5 _net2 vdd) pfet l=600n w=3u nf=1 m=1 par=1 ngcon=1 \
      ad=1.65e-12 as=1.65e-12 pd=7.1u ps=7.1u nrd=0.0733 nrs=0.0733 \
      rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
      rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
      panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
      sb=5.5e-07 sd=0u dtemp=0
   T11 (net17 vb1 vdd vdd) pfet l=600n w=7u nf=1 m=1 par=1 ngcon=1 \
      ad=3.85e-12 as=3.85e-12 pd=15.1u ps=15.1u nrd=0.0314 nrs=0.0314 \
      rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
      rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
      panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
      sb=5.5e-07 sd=0u dtemp=0
   T10 (net5 vb2 net17 vdd) pfet l=600n w=22.0u nf=1 m=1 par=1 ngcon=1 \
      ad=1.21e-11 as=1.21e-11 pd=45.1u ps=45.1u nrd=0.01 nrs=0.01 \
      rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
      rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
      panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
      sb=5.5e-07 sd=0u dtemp=0
   T45 (net13 vb2 net9 vdd) pfet l=600n w=22.0u nf=1 m=1 par=1 ngcon=1 \
      ad=1.21e-11 as=1.21e-11 pd=45.1u ps=45.1u nrd=0.01 nrs=0.01 \
      rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
```

```
    rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
    panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
    sb=5.5e-07 sd=0u dtemp=0
T46 (vdd vb1 net13 vdd) pfet l=600n w=7u nf=1 m=1 par=1 ngcon=1 \
    ad=3.85e-12 as=3.85e-12 pd=15.1u ps=15.1u nrd=0.0314 nrs=0.0314 \
    rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
    rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
    panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
    sb=5.5e-07 sd=0u dtemp=0
T37 (vb2 vb2 vdd vdd) pfet l=600n w=1u nf=1 m=1 par=1 ngcon=1 \
    ad=5.5e-13 as=5.5e-13 pd=3.1u ps=3.1u nrd=0.22 nrs=0.22 rf_rsub=1 \
    plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
    rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
    panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
    sb=5.5e-07 sd=0u dtemp=0
T33 (vcm vcm vdd vdd) pfet l=600n w=3u nf=1 m=1 par=1 ngcon=1 \
    ad=1.65e-12 as=1.65e-12 pd=7.1u ps=7.1u nrd=0.0733 nrs=0.0733 \
    rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
    rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
    panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
    sb=5.5e-07 sd=0u dtemp=0
T41 (vb4 vb4 vdd vdd) pfet l=600n w=1.9u nf=1 m=1 par=1 ngcon=1 \
    ad=1.045e-12 as=1.045e-12 pd=4.9u ps=4.9u nrd=0.1158 nrs=0.1158 \
    rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
    rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
    panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
    sb=5.5e-07 sd=0u dtemp=0
T16 (vb3 vb3 vdd vdd) pfet l=600n w=8u nf=1 m=1 par=1 ngcon=1 \
    ad=4.4e-12 as=4.4e-12 pd=17.1u ps=17.1u nrd=0.0275 nrs=0.0275 \
    rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
    rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
    panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
    sb=5.5e-07 sd=0u dtemp=0
T43 (output1 net9 vdd vdd) pfet l=600n w=3u nf=1 m=1 par=1 ngcon=1 \
    ad=1.65e-12 as=1.65e-12 pd=7.1u ps=7.1u nrd=0.0733 nrs=0.0733 \
    rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
    rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
    panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
    sb=5.5e-07 sd=0u dtemp=0
T40 (vb1 vb1 vdd vdd) pfet l=600n w=8u nf=1 m=1 par=1 ngcon=1 \
    ad=4.4e-12 as=4.4e-12 pd=17.1u ps=17.1u nrd=0.0275 nrs=0.0275 \
    rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
    rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
    panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
    sb=5.5e-07 sd=0u dtemp=0
T8 (output1 vb4 0 inh_substrate) nfet l=600n w=600n nf=1 m=1 par=1 \
    ngcon=1 ad=3.3e-13 as=3.3e-13 pd=2.3u ps=2.3u nrd=0.3667 \
    nrs=0.3667 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
    lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
    panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
    sa=5.5e-07 sb=5.5e-07 sd=0u dtemp=0
T44 (net14 vb3 net9 inh_substrate) nfet l=600n w=14.0u nf=1 m=1 par=1 \
    ngcon=1 ad=7.7e-12 as=7.7e-12 pd=29.1u ps=29.1u nrd=0.0157 \
    nrs=0.0157 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
    lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
    panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
    sa=5.5e-07 sb=5.5e-07 sd=0u dtemp=0
T4 (0 vcm vcm inh_substrate) nfet l=600n w=1u nf=1 m=1 par=1 ngcon=1 \
    ad=5.5e-13 as=5.5e-13 pd=3.1u ps=3.1u nrd=0.22 nrs=0.22 rf_rsub=1 \
    plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
    rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
    panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
    sb=5.5e-07 sd=0u dtemp=0
T5 (net5 vb3 net022 inh_substrate) nfet l=600n w=14.0u nf=1 m=1 par=1 \
    ngcon=1 ad=7.7e-12 as=7.7e-12 pd=29.1u ps=29.1u nrd=0.0157 \
    nrs=0.0157 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
    lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
    panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
    sa=5.5e-07 sb=5.5e-07 sd=0u dtemp=0
T42 (vb4 vb4 0 inh_substrate) nfet l=600n w=1u nf=1 m=1 par=1 ngcon=1 \
    ad=5.5e-13 as=5.5e-13 pd=3.1u ps=3.1u nrd=0.22 nrs=0.22 rf_rsub=1 \
    plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
    rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
    panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
    sb=5.5e-07 sd=0u dtemp=0
```

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    T39 (0 vb2 vb2 inh_substrate) nfet l=600n w=1u nf=1 m=1 par=1 ngcon=1 \
        ad=5.5e-13 as=5.5e-13 pd=3.1u ps=3.1u nrd=0.22 nrs=0.22 rf_rsub=1 \
        plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
        rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
        panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
        sb=5.5e-07 sd=0u dtemp=0
    T38 (0 vb1 vb1 inh_substrate) nfet l=600n w=1u nf=1 m=1 par=1 ngcon=1 \
        ad=5.5e-13 as=5.5e-13 pd=3.1u ps=3.1u nrd=0.22 nrs=0.22 rf_rsub=1 \
        plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
        rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
        panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
        sb=5.5e-07 sd=0u dtemp=0
    T0 (net14 input1 net8 inh_substrate) nfet l=600n w=17.0u nf=1 m=1 \
        par=1 ngcon=1 ad=9.35e-12 as=9.35e-12 pd=35.1u ps=35.1u nrd=0.0129 \
        nrs=0.0129 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
        lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
        panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
        sa=5.5e-07 sb=5.5e-07 sd=0u dtemp=0
    T1 (net022 _net3 net8 inh_substrate) nfet l=600n w=17.0u nf=1 m=1 \
        par=1 ngcon=1 ad=9.35e-12 as=9.35e-12 pd=35.1u ps=35.1u nrd=0.0129 \
        nrs=0.0129 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
        lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
        panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
        sa=5.5e-07 sb=5.5e-07 sd=0u dtemp=0
    T35 (vb3 vb3 0 inh_substrate) nfet l=600n w=1u nf=1 m=1 par=1 ngcon=1 \
        ad=5.5e-13 as=5.5e-13 pd=3.1u ps=3.1u nrd=0.22 nrs=0.22 rf_rsub=1 \
        plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
        rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
        panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
        sb=5.5e-07 sd=0u dtemp=0
    T2 (net8 vcm 0 inh_substrate) nfet l=600n w=5u nf=1 m=1 par=1 ngcon=1 \
        ad=2.75e-12 as=2.75e-12 pd=11.1u ps=11.1u nrd=0.044 nrs=0.044 \
        rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
        rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
        panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
        sb=5.5e-07 sd=0u dtemp=0
    T7 (_net2 vb4 0 inh_substrate) nfet l=600n w=600n nf=1 m=1 par=1 \
        ngcon=1 ad=3.3e-13 as=3.3e-13 pd=2.3u ps=2.3u nrd=0.3667 \
        nrs=0.3667 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
        lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
        panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
        sa=5.5e-07 sb=5.5e-07 sd=0u dtemp=0
    I7 (0 inh_substrate) subc l=4u w=2u dtemp=0
ends Two_stage_Amp
// End of subcircuit definition.

// Library name: Test
// Cell name: Single_ended_output
// View name: schematic
subckt Single_ended_output _net2 input1 _net3 vdd inh_substrate
    I55 (0 inh_substrate) subc l=4u w=2u dtemp=0
    OPrrp0 (vdd vcm inh_substrate) oprrpres w=740.00n l=1.06u r=1.07334K \
        sbar=1 m=1 par=1 sh=1 bp=3 dtemp=0.0 rsx=50
    T8 (net04 _net2 net07 vdd) pfet l=950.0n w=21.0u nf=1 m=1 par=1 \
        ngcon=1 ad=1.155e-11 as=1.155e-11 pd=43.1u ps=43.1u nrd=0.0105 \
        nrs=0.0105 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
        lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
        panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
        sa=5.5e-07 sb=5.5e-07 sd=0u dtemp=0
    T0 (net07 input1 net09 vdd) pfet l=950.0n w=21.0u nf=1 m=1 par=1 \
        ngcon=1 ad=1.155e-11 as=1.155e-11 pd=43.1u ps=43.1u nrd=0.0105 \
        nrs=0.0105 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
        lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
        panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
        sa=5.5e-07 sb=5.5e-07 sd=0u dtemp=0
    T1 (vdd vcm net07 vdd) pfet l=950.0n w=25.0u nf=1 m=1 par=1 ngcon=1 \
        ad=1.375e-11 as=1.375e-11 pd=51.1u ps=51.1u nrd=0.0088 nrs=0.0088 \
        rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
        rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
        panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
        sb=5.5e-07 sd=0u dtemp=0
    T7 (vdd net03 net03 vdd) pfet l=950.0n w=1u nf=1 m=1 par=1 ngcon=1 \
        ad=5.5e-13 as=5.5e-13 pd=3.1u ps=3.1u nrd=0.22 nrs=0.22 rf_rsub=1 \
        plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
        rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
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      panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
      sb=5.5e-07 sd=0u dtemp=0
   T6 (vdd net03 _net3 vdd) pfet l=950.0n w=1u nf=1 m=1 par=1 ngcon=1 \
      ad=5.5e-13 as=5.5e-13 pd=3.1u ps=3.1u nrd=0.22 nrs=0.22 rf_rsub=1 \
      plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
      rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
      panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
      sb=5.5e-07 sd=0u dtemp=0
   T3 (_net3 net09 0 inh_substrate) nfet l=250.0n w=200n nf=1 m=1 par=1 \
      ngcon=1 ad=1.1e-13 as=1.1e-13 pd=1.5u ps=1.5u nrd=1.1 nrs=1.1 \
      rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
      rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
      panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
      sb=5.5e-07 sd=0u dtemp=0
   T5 (net04 net04 0 inh_substrate) nfet l=250.0n w=200n nf=1 m=1 par=1 \
      ngcon=1 ad=1.1e-13 as=1.1e-13 pd=1.5u ps=1.5u nrd=1.1 nrs=1.1 \
      rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
      rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
      panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
      sb=5.5e-07 sd=0u dtemp=0
   T4 (0 net09 net09 inh_substrate) nfet l=250.0n w=200n nf=1 m=1 par=1 \
      ngcon=1 ad=1.1e-13 as=1.1e-13 pd=1.5u ps=1.5u nrd=1.1 nrs=1.1 \
      rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
      rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
      panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
      sb=5.5e-07 sd=0u dtemp=0
   T2 (0 net04 net03 inh_substrate) nfet l=250.0n w=200n nf=1 m=1 par=1 \
      ngcon=1 ad=1.1e-13 as=1.1e-13 pd=1.5u ps=1.5u nrd=1.1 nrs=1.1 \
      rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
      rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
      panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
      sb=5.5e-07 sd=0u dtemp=0
   T9 (0 vcm vcm inh_substrate) nfet l=250.0n w=27.0u nf=1 m=1 par=1 \
      ngcon=1 ad=1.485e-11 as=1.485e-11 pd=55.1u ps=55.1u nrd=0.0081 \
      nrs=0.0081 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
      lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
      panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
      sa=5.5e-07 sb=5.5e-07 sd=0u dtemp=0
ends Single_ended_output
// End of subcircuit definition.

// Library name: Test
// Cell name: buffer_33
// View name: schematic
subckt buffer_33 _net7 input1 _net6 output1 vdd1 inh_substrate
   I55 (0 inh_substrate) subc l=4u w=2u dtemp=0
   T2 (vb1 vb1 0 inh_substrate) nfet33 l=4u w=20u nf=1 m=1 par=1 ngcon=1 \
      ad=1.2e-11 as=1.2e-11 pd=41.2u ps=41.2u nrd=0.011 nrs=0.011 \
      rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
      rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
      panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=6e-07 sb=6e-07 \
      sd=0u dtemp=0
   T9 (vb2 vb1 0 inh_substrate) nfet33 l=4u w=20u nf=1 m=1 par=1 ngcon=1 \
      ad=1.2e-11 as=1.2e-11 pd=41.2u ps=41.2u nrd=0.011 nrs=0.011 \
      rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
      rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
      panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=6e-07 sb=6e-07 \
      sd=0u dtemp=0
   T7 (0 vb1 output1 inh_substrate) nfet33 l=4u w=2.3u nf=1 m=1 par=1 \
      ngcon=1 ad=1.38e-12 as=1.38e-12 pd=5.8u ps=5.8u nrd=0.0957 \
      nrs=0.0957 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
      lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
      panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
      sa=6e-07 sb=6e-07 sd=0u dtemp=0
   T1 (_net6 vb1 0 inh_substrate) nfet33 l=4u w=2.3u nf=1 m=1 par=1 \
      ngcon=1 ad=1.38e-12 as=1.38e-12 pd=5.8u ps=5.8u nrd=0.0957 \
      nrs=0.0957 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
      lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
      panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
      sa=6e-07 sb=6e-07 sd=0u dtemp=0
   T4 (output1 input1 net07 inh_substrate) nfet33 l=4u w=2.3u nf=1 m=1 \
      par=1 ngcon=1 ad=1.38e-12 as=1.38e-12 pd=5.8u ps=5.8u nrd=0.0957 \
      nrs=0.0957 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
      lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
      panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
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      sa=6e-07 sb=6e-07 sd=0u dtemp=0
   T5 (net02 _net7 _net6 inh_substrate) nfet33 l=4u w=2.3u nf=1 m=1 par=1 \
      ngcon=1 ad=1.38e-12 as=1.38e-12 pd=5.8u ps=5.8u nrd=0.0957 \
      nrs=0.0957 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
      lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
      panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
      sa=6e-07 sb=6e-07 sd=0u dtemp=0
   OPrrp0 (vdd1 vb1 inh_substrate) oprrpres w=740.00n l=8.49u r=20.01037K \
      sbar=1 m=1 par=1 sh=1 bp=3 dtemp=0.0 rsx=50
   T0 (vdd1 vb2 net07 vdd1) pfet33 l=6u w=11.0u nf=1 m=1 par=1 ngcon=1 \
      ad=6.6e-12 as=6.6e-12 pd=23.2u ps=23.2u nrd=0.02 nrs=0.02 \
      rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
      rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
      panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=6e-07 sb=6e-07 \
      sd=0u dtemp=0
   T8 (net02 vb2 vdd1 vdd1) pfet33 l=6u w=11.0u nf=1 m=1 par=1 ngcon=1 \
      ad=6.6e-12 as=6.6e-12 pd=23.2u ps=23.2u nrd=0.02 nrs=0.02 \
      rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
      rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
      panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=6e-07 sb=6e-07 \
      sd=0u dtemp=0
   T3 (vb2 vb2 vdd1 vdd1) pfet33 l=6u w=8u nf=1 m=1 par=1 ngcon=1 \
      ad=4.8e-12 as=4.8e-12 pd=17.2u ps=17.2u nrd=0.0275 nrs=0.0275 \
      rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
      rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
      panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=6e-07 sb=6e-07 \
      sd=0u dtemp=0
ends buffer_33
// End of subcircuit definition.

// Library name: Test
// Cell name: differentiator
// View name: schematic
subckt differentiator _net9 _net8 output1 vdd1 inh_substrate
   OPrrp0 (vdd1 vcm inh_substrate) oprrpres w=740.00n l=4.58u r=10.04486K \
      sbar=1 m=1 par=1 sh=1 bp=3 dtemp=0.0 rsx=50
   OPrrp2 (_net8 _net9 inh_substrate) oprrpres w=740.00n l=4.57u \
      r=10.01937K sbar=1 m=1 par=1 sh=1 bp=3 dtemp=0.0 rsx=50
   OPrrp7 (output1 net34 inh_substrate) oprrpres w=740.00n l=4.57u \
      r=10.01937K sbar=1 m=1 par=1 sh=1 bp=3 dtemp=0.0 rsx=50
   T1 (vcm vcm 0 inh_substrate) nfet33 l=16.7u w=15.8u nf=2 m=1 par=1 \
      ngcon=1 ad=3.476e-12 as=9.48e-12 pd=16.68u ps=34.0u nrd=0.0139 \
      nrs=0.0139 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
      lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
      panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
      sa=6e-07 sb=6e-07 sd=4.4e-07 dtemp=0
   T3 (net21 net34 output1 inh_substrate) nfet33 l=16.7u w=500n nf=1 m=1 \
      par=1 ngcon=1 ad=3e-13 as=3e-13 pd=2.2u ps=2.2u nrd=0.44 nrs=0.44 \
      rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
      rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
      panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=6e-07 sb=6e-07 \
      sd=0u dtemp=0
   T2 (_net8 _net9 net27 inh_substrate) nfet33 l=16.7u w=500n nf=1 m=1 \
      par=1 ngcon=1 ad=3e-13 as=3e-13 pd=2.2u ps=2.2u nrd=0.44 nrs=0.44 \
      rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
      rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
      panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=6e-07 sb=6e-07 \
      sd=0u dtemp=0
   T4 (net27 net27 net20 inh_substrate) nfet33 l=16.7u w=500n nf=1 m=1 \
      par=1 ngcon=1 ad=3e-13 as=3e-13 pd=2.2u ps=2.2u nrd=0.44 nrs=0.44 \
      rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
      rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
      panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=6e-07 sb=6e-07 \
      sd=0u dtemp=0
   T5 (net20 net21 net21 inh_substrate) nfet33 l=16.7u w=500n nf=1 m=1 \
      par=1 ngcon=1 ad=3e-13 as=3e-13 pd=2.2u ps=2.2u nrd=0.44 nrs=0.44 \
      rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
      rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
      panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=6e-07 sb=6e-07 \
      sd=0u dtemp=0
   T7 (net20 vcm 0 inh_substrate) nfet33 l=16.7u w=5.8u nf=1 m=1 par=1 \
      ngcon=1 ad=3.48e-12 as=3.48e-12 pd=12.8u ps=12.8u nrd=0.0379 \
      nrs=0.0379 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
      lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
      panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
```

```
      sa=6e-07 sb=6e-07 sd=0u dtemp=0
   T21 (vdd1 net31 net31 vdd1) pfet33 l=19.6u w=500n nf=1 m=1 par=1 \
      ngcon=1 ad=3e-13 as=3e-13 pd=2.2u ps=2.2u nrd=0.44 nrs=0.44 \
      rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
      rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
      panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=6e-07 sb=6e-07 \
      sd=0u dtemp=0
   T13 (vdd1 net29 net29 vdd1) pfet33 l=19.6u w=500n nf=1 m=1 par=1 \
      ngcon=1 ad=3e-13 as=3e-13 pd=2.2u ps=2.2u nrd=0.44 nrs=0.44 \
      rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
      rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
      panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=6e-07 sb=6e-07 \
      sd=0u dtemp=0
   T22 (net31 output1 output1 vdd1) pfet33 l=19.6u w=500n nf=1 m=1 par=1 \
      ngcon=1 ad=3e-13 as=3e-13 pd=2.2u ps=2.2u nrd=0.44 nrs=0.44 \
      rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
      rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
      panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=6e-07 sb=6e-07 \
      sd=0u dtemp=0
   T14 (net29 _net8 _net8 vdd1) pfet33 l=19.6u w=500n nf=1 m=1 par=1 \
      ngcon=1 ad=3e-13 as=3e-13 pd=2.2u ps=2.2u nrd=0.44 nrs=0.44 \
      rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
      rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
      panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=6e-07 sb=6e-07 \
      sd=0u dtemp=0
   I55 (0 inh_substrate) subc l=4u w=2u dtemp=0
ends differentiator
// End of subcircuit definition.

// Library name: Test
// Cell name: Buffer1
// View name: schematic
subckt Buffer1 _net10 input1 _net11 output1 vdd inh_substrate
   T3 (net04 input1 0 inh_substrate) nfet l=9.7u w=400n nf=1 m=1 par=1 \
      ngcon=1 ad=2.2e-13 as=2.2e-13 pd=1.9u ps=1.9u nrd=0.55 nrs=0.55 \
      rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
      rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
      panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
      sb=5.5e-07 sd=0u dtemp=0
   T2 (output1 output1 0 inh_substrate) nfet l=9.7u w=400n nf=1 m=1 par=1 \
      ngcon=1 ad=2.2e-13 as=2.2e-13 pd=1.9u ps=1.9u nrd=0.55 nrs=0.55 \
      rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
      rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
      panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
      sb=5.5e-07 sd=0u dtemp=0
   T1 (net06 _net10 0 inh_substrate) nfet l=9.7u w=400n nf=1 m=1 par=1 \
      ngcon=1 ad=2.2e-13 as=2.2e-13 pd=1.9u ps=1.9u nrd=0.55 nrs=0.55 \
      rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
      rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
      panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
      sb=5.5e-07 sd=0u dtemp=0
   T0 (_net11 _net11 0 inh_substrate) nfet l=9.7u w=400n nf=1 m=1 par=1 \
      ngcon=1 ad=2.2e-13 as=2.2e-13 pd=1.9u ps=1.9u nrd=0.55 nrs=0.55 \
      rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
      rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
      panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
      sb=5.5e-07 sd=0u dtemp=0
   T10 (net04 net04 net05 vdd) pfet l=1.1u w=20.6u nf=1 m=1 par=1 ngcon=1 \
      ad=1.133e-11 as=1.133e-11 pd=42.3u ps=42.3u nrd=0.0107 nrs=0.0107 \
      rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
      rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
      panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
      sb=5.5e-07 sd=0u dtemp=0
   T9 (net016 net04 output1 vdd) pfet l=1.1u w=20.6u nf=1 m=1 par=1 \
      ngcon=1 ad=1.133e-11 as=1.133e-11 pd=42.3u ps=42.3u nrd=0.0107 \
      nrs=0.0107 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
      lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
      panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
      sa=5.5e-07 sb=5.5e-07 sd=0u dtemp=0
   T8 (net017 net06 _net11 vdd) pfet l=1.1u w=20.6u nf=1 m=1 par=1 \
      ngcon=1 ad=1.133e-11 as=1.133e-11 pd=42.3u ps=42.3u nrd=0.0107 \
      nrs=0.0107 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
      lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
      panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
      sa=5.5e-07 sb=5.5e-07 sd=0u dtemp=0
```

```
    T7 (net06 net06 net07 vdd) pfet l=1.1u w=20.6u nf=1 m=1 par=1 ngcon=1 \
       ad=1.133e-11 as=1.133e-11 pd=42.3u ps=42.3u nrd=0.0107 nrs=0.0107 \
       rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
       rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
       panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
       sb=5.5e-07 sd=0u dtemp=0
    T6 (net05 net05 vdd vdd) pfet l=1.1u w=20.6u nf=1 m=1 par=1 ngcon=1 \
       ad=1.133e-11 as=1.133e-11 pd=42.3u ps=42.3u nrd=0.0107 nrs=0.0107 \
       rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
       rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
       panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
       sb=5.5e-07 sd=0u dtemp=0
    T44 (vdd net07 net017 vdd) pfet l=1.1u w=20.6u nf=1 m=1 par=1 ngcon=1 \
       ad=1.133e-11 as=1.133e-11 pd=42.3u ps=42.3u nrd=0.0107 nrs=0.0107 \
       rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
       rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
       panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
       sb=5.5e-07 sd=0u dtemp=0
    T5 (net07 net07 vdd vdd) pfet l=1.1u w=20.6u nf=1 m=1 par=1 ngcon=1 \
       ad=1.133e-11 as=1.133e-11 pd=42.3u ps=42.3u nrd=0.0107 nrs=0.0107 \
       rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
       rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
       panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
       sb=5.5e-07 sd=0u dtemp=0
    T4 (vdd net05 net016 vdd) pfet l=1.1u w=20.6u nf=1 m=1 par=1 ngcon=1 \
       ad=1.133e-11 as=1.133e-11 pd=42.3u ps=42.3u nrd=0.0107 nrs=0.0107 \
       rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
       rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
       panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
       sb=5.5e-07 sd=0u dtemp=0
    I7 (0 inh_substrate) subc l=4u w=2u dtemp=0
ends Buffer1
// End of subcircuit definition.

// Library name: Test
// Cell name: Chopper
// View name: schematic
subckt Chopper Q1 Q1\' _net12 input1 _net13 output1 vdd inh_substrate
    I7 (0 inh_substrate) subc l=4u w=2u dtemp=0
    T8 (_net12 Q1 output1 vdd) pfet l=400n w=29.1u nf=1 m=1 par=1 ngcon=1 \
       ad=1.6005e-11 as=1.6005e-11 pd=59.3u ps=59.3u nrd=0.0076 \
       nrs=0.0076 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
       lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
       panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
       sa=5.5e-07 sb=5.5e-07 sd=0u dtemp=0
    T5 (output1 Q1\' input1 vdd) pfet l=400n w=29.1u nf=1 m=1 par=1 \
       ngcon=1 ad=1.6005e-11 as=1.6005e-11 pd=59.3u ps=59.3u nrd=0.0076 \
       nrs=0.0076 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
       lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
       panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
       sa=5.5e-07 sb=5.5e-07 sd=0u dtemp=0
    T3 (_net12 Q1\' _net13 vdd) pfet l=400n w=29.1u nf=1 m=1 par=1 ngcon=1 \
       ad=1.6005e-11 as=1.6005e-11 pd=59.3u ps=59.3u nrd=0.0076 \
       nrs=0.0076 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
       lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
       panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
       sa=5.5e-07 sb=5.5e-07 sd=0u dtemp=0
    T10 (input1 Q1 _net13 vdd) pfet l=400n w=29.1u nf=1 m=1 par=1 ngcon=1 \
       ad=1.6005e-11 as=1.6005e-11 pd=59.3u ps=59.3u nrd=0.0076 \
       nrs=0.0076 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
       lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
       panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
       sa=5.5e-07 sb=5.5e-07 sd=0u dtemp=0
    T9 (_net12 Q1\' output1 inh_substrate) nfet l=400n w=3u nf=1 m=1 par=1 \
       ngcon=1 ad=1.65e-12 as=1.65e-12 pd=7.1u ps=7.1u nrd=0.0733 \
       nrs=0.0733 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
       lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
       panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
       sa=5.5e-07 sb=5.5e-07 sd=0u dtemp=0
    T0 (_net12 Q1 _net13 inh_substrate) nfet l=400n w=3u nf=1 m=1 par=1 \
       ngcon=1 ad=1.65e-12 as=1.65e-12 pd=7.1u ps=7.1u nrd=0.0733 \
       nrs=0.0733 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
       lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
       panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
       sa=5.5e-07 sb=5.5e-07 sd=0u dtemp=0
```

```
    T1 (output1 Q1 input1 inh_substrate) nfet l=400n w=3u nf=1 m=1 par=1 \
        ngcon=1 ad=1.65e-12 as=1.65e-12 pd=7.1u ps=7.1u nrd=0.0733 \
        nrs=0.0733 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
        lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
        panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
        sa=5.5e-07 sb=5.5e-07 sd=0u dtemp=0
    T11 (input1 Q1\' _net13 inh_substrate) nfet l=400n w=3u nf=1 m=1 par=1 \
        ngcon=1 ad=1.65e-12 as=1.65e-12 pd=7.1u ps=7.1u nrd=0.0733 \
        nrs=0.0733 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
        lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
        panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
        sa=5.5e-07 sb=5.5e-07 sd=0u dtemp=0
ends Chopper
// End of subcircuit definition.

// Library name: Test
// Cell name: D_chopper
// View name: schematic
subckt D_chopper Q1 Q1\' _net14 input1 _net15 output1 vdd inh_substrate
    I7 (0 inh_substrate) subc l=4u w=2u dtemp=0
    T8 (_net14 Q1 output1 vdd) pfet l=400n w=29.1u nf=1 m=1 par=1 ngcon=1 \
        ad=1.6005e-11 as=1.6005e-11 pd=59.3u ps=59.3u nrd=0.0076 \
        nrs=0.0076 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
        lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
        panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
        sa=5.5e-07 sb=5.5e-07 sd=0u dtemp=0
    T5 (output1 Q1\' input1 vdd) pfet l=400n w=29.1u nf=1 m=1 par=1 \
        ngcon=1 ad=1.6005e-11 as=1.6005e-11 pd=59.3u ps=59.3u nrd=0.0076 \
        nrs=0.0076 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
        lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
        panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
        sa=5.5e-07 sb=5.5e-07 sd=0u dtemp=0
    T3 (_net14 Q1\' _net15 vdd) pfet l=400n w=29.1u nf=1 m=1 par=1 ngcon=1 \
        ad=1.6005e-11 as=1.6005e-11 pd=59.3u ps=59.3u nrd=0.0076 \
        nrs=0.0076 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
        lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
        panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
        sa=5.5e-07 sb=5.5e-07 sd=0u dtemp=0
    T10 (input1 Q1 _net15 vdd) pfet l=400n w=29.1u nf=1 m=1 par=1 ngcon=1 \
        ad=1.6005e-11 as=1.6005e-11 pd=59.3u ps=59.3u nrd=0.0076 \
        nrs=0.0076 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
        lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
        panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
        sa=5.5e-07 sb=5.5e-07 sd=0u dtemp=0
    T9 (_net14 Q1\' output1 inh_substrate) nfet l=400n w=3u nf=1 m=1 par=1 \
        ngcon=1 ad=1.65e-12 as=1.65e-12 pd=7.1u ps=7.1u nrd=0.0733 \
        nrs=0.0733 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
        lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
        panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
        sa=5.5e-07 sb=5.5e-07 sd=0u dtemp=0
    T0 (_net14 Q1 _net15 inh_substrate) nfet l=400n w=3u nf=1 m=1 par=1 \
        ngcon=1 ad=1.65e-12 as=1.65e-12 pd=7.1u ps=7.1u nrd=0.0733 \
        nrs=0.0733 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
        lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
        panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
        sa=5.5e-07 sb=5.5e-07 sd=0u dtemp=0
    T1 (output1 Q1 input1 inh_substrate) nfet l=400n w=3u nf=1 m=1 par=1 \
        ngcon=1 ad=1.65e-12 as=1.65e-12 pd=7.1u ps=7.1u nrd=0.0733 \
        nrs=0.0733 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
        lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
        panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
        sa=5.5e-07 sb=5.5e-07 sd=0u dtemp=0
    T11 (input1 Q1\' _net15 inh_substrate) nfet l=400n w=3u nf=1 m=1 par=1 \
        ngcon=1 ad=1.65e-12 as=1.65e-12 pd=7.1u ps=7.1u nrd=0.0733 \
        nrs=0.0733 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
        lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
        panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
        sa=5.5e-07 sb=5.5e-07 sd=0u dtemp=0
ends D_chopper
// End of subcircuit definition.

// Library name: Test
// Cell name: Test_Dosimeter
// View name: schematic
C6 (C4\+ C4\-) capacitor c=10n
```

```
C3 (C3\+ C3\-) capacitor c=1n
C2 (C2\+ C2\-) capacitor c=1n
C1 (C1\+ C1\-) capacitor c=1n
C0 (C0\+ C0\-) capacitor c=1n
V2 (vdd 0) vsource dc=1.2 type=dc
V1 (vdd1 0) vsource dc=3.3 type=dc
V3 (Q1\' 0) vsource type=pulse val0=VL val1=VH period=100.0u delay=delay \
      rise=10p fall=10p width=50u
V0 (Q1 0) vsource type=pulse val0=VH val1=VL period=100.0u delay=delay \
      rise=10p fall=10p width=50u
I16 (C0\+ C0\- C1\+ C1\- vdd sub!) Low_pass_filter
I0 (net035 net034 C0\+ C0\- vdd sub!) Low_pass_filter
I18 (C1\+ C1\- C2\+ C2\- vdd sub!) Low_pass_filter
I2 (C2\+ C2\- C3\+ C3\- vdd sub!) Low_pass_filter
I195 (C4\+ vdd1 sub!) mytest1
I122 (chopper chopper1 Amp Amp1 vdd sub!) Two_stage_Amp
I193 (C3\+ C3\- _net0 vdd sub!) Single_ended_output
I183 (differ differ1 buffer buffer1 vdd1 sub!) buffer_33
I10 (C4\- differ differ1 vdd1 sub!) differentiator
I182 (Amp Amp1 Buffer Buffer1 vdd sub!) Buffer1
I187 (D_chopper D_chopper1 net035 net034 vdd sub!) Buffer1
I1 (Q1 Q1\' buffer buffer1 chopper chopper1 vdd sub!) Chopper
I185 (Q1 Q1\' Buffer Buffer1 D_chopper D_chopper1 vdd sub!) D_chopper
simulatorOptions options reltol=1e-3 vabstol=1e-6 iabstol=1e-12 temp=27 \
    tnom=27 scalem=1.0 scale=1.0 gmin=1e-12 rforce=1 maxnotes=5 maxwarns=5 \
    digits=5 cols=80 pivrel=1e-3 sensfile="../psf/sens.output" \
    checklimitdest=psf
tran tran stop=1.001 write="spectre.ic" writefinal="spectre.fc" \
    annotate=status maxiters=5
finalTimeOP info what=oppoint where=rawfile
modelParameter info what=models where=rawfile
element info what=inst where=rawfile
outputParameter info what=output where=rawfile
designParamVals info what=parameters where=rawfile
primitives info what=primitives where=rawfile
subckts info what=subckts where=rawfile
saveOptions options save=allpub
ahdl_include "/home/cham/design/130nm/VerilogA/Vout/veriloga/veriloga.va"
```

Paper under review

Paper titled “A New Open Source Floating-Gate MOSFET Device Model for Analog Circuit Simulation and Design,” submitted for publication in IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems on 24-Jul-2017 is presently under review.