# STUDIES OF FAULT CURRENT LIMITERS FOR POWER SYSTEMS PROTECTION

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To my parents:

Balbir Singh Malhi

and

Paramjit Kaur Malhi

# ABSTRACT

In today's technological world, electrical energy is one of the most important forms of energy and is needed directly or indirectly in almost every field. Increase in the demand and consumption of electrical energy leads to increase in the system fault levels. It is not possible to change the rating of the equipment and devices in the system or circuits to accommodate the increasing fault currents. The devices in electronic and electrical circuits are sensitive to disturbance and any disturbance or fault may damage the device permanently so that it must be replaced. The cost of equipment like circuit breakers and transformers in power grids is very expensive. Moreover, replacing damaged equipment is a time and labour consuming process, which also affects the reliability of power systems. It is not possible to completely eliminate the faults but it is possible to limit the current during fault in order to save the equipment and devices in the circuits or systems. One solution to this problem is to use a current limiting device in the system. There are many different types of approaches used for limiting fault currents

Two different approaches to limit fault currents have been discussed by the author. One is Passive Magnetic Current Limiter (MCL) and another is High Temperature Superconductor Fault Current Limiter (HTSFCL). Both are passive devices and they do not need any sensor or external sources to perform their current limiting action. The first device consists of two ferrite cores and a permanent magnet which is sandwiched between the two saturated cores and it is called Magnetic Current Limiter. Experimental results with the MCL in circuit are discussed. Both field and thermal models of the MCL have been simulated using finite element software, FEMLAB.

The demonstration of the High Temperature Superconductor Fault Current Limiter (HTSFCL) in power systems has been explained. The MATLAB simulation of the HTSFCL has been done and the results with and without the fault are shown. Power System Analysis Toolbox (PSAT) software has been used to locate the optimum or the best location of HTSFCL in a nine bus system. It has been shown that it is possible to find a solution that limits the fault current in power systems. Depending on the size of the system, either the MCL or the HTSFCL can be implemented. The location of the HTSFCL is to be carefully selected to achieve optimum results.

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# Chapter 1
# Introduction

## 1.1 Introduction

In today's world, electrical energy is unquestionably the most versatile and universally useful form of energy available. Electricity is only one of the many forms of energy used in industry, homes, businesses, and transportation. With increase in the industry, consumption of electrical energy is increased. As a result there is increase in the size of the generating station and the interconnected networks called power grids. Due to increase in the size of the grids and generating stations this also increases the possibility of abnormal operation in the systems. There may be sudden decreases in the impedance of the power systems network, which lead to an increase in current, known as fault current, and faults in the electrical power systems are inevitable.

Often generating stations are located far away from urban areas and the electrical energy is transmitted from generating station through long overhead transmission lines. These transmission lines are naked and exposed to the atmosphere. Wind may blow down electric poles and ground the wires or lightning may cause severe faults in the system resulting in the flow of large fault currents in the system which can damage the equipment installed at the power grids and generating station. The increase in the electrical energy consumption necessitates a large power system, resulting in considerable increase in the system fault current levels. These large fault currents generate large mechanical forces which endanger the mechanical integrity of the power system hardware, transformers and other equipment may overheat. As the equipment in the power networks is very expensive, their protection from large fault currents is needed. The reliability of the power systems is the most important factor for their efficient operation. It is not possible to completely eliminate the faults in the system but it is possible to lower the harmful effects of fault on the systems by decreasing the current during fault.

The electrical and electronic industry is rapidly flourishing due to which the demand for as well as the power quality of the electricity is increasing. To have continuous and reliable operation of the power systems the fault currents in the system needed to limit to a lower value.

## 1.2 Consequences of the Fault

During fault in the system, the current rises to a very high value which is many times the normal current in the system. Due to the flow of very high current in the system during fault, damage can occur to any equipment installed in the system. The equipment in the power grids like circuit breakers and transformers are very expensive. The equipment connected in series with the fault current path is exposed to high fault current and the design of components must take into consideration the maximum value of the fault current.

It is not economical to design high rating components that can handle high fault currents. An alternative solution to this problem would be to change the system configuration, which is a very labour consuming job and affects the reliability and integrity of the system. The other option would be to apply some fault current limiting device in the system to avoid any damage to the costly equipment in the power systems. For the above reasons the importance of a Fault Current Limiter (FCL) has been increased. With a FCL, a circuit breaker with a low rating can be used, this is cost efficient compared to breaker replacement.

The following requirement should be fulfilled in order to have the desired and reliable operation of a fault current limiter in the power systems.

1. To limit the first peak of the fault current,
2. Low impedance during normal operation (low voltage drop across the device),
3. Low losses,
4. Compatibility with existing or planned protection schemes,
5. It should have smooth and gradual change of impedance from normal mode to fault mode and vice versa,
6. Low maintenance cost and requirements,
7. High reliability,
8. Zero reset time,
9. Low impact on the environment and fail-safe operation.

There are many other factors to be considered before installing the fault current limiter in the system, such as the effect of the fault current limiter on the system and the effect of the system on the fault current limiter.

## 1.3 Why Current Limiters are required?

The equipment installed at power grids and at generating station is very expensive and its cost, if estimated, would be in millions of dollars. In order to save this expensive equipment from fault currents during faults and short circuits, fault current limiters are required.

There might be many consequences of faulty operation in the system some of which are:-

1. Permanent damage of the equipment installed in the power grids,
2. System configuration might need to be changed,
3. Affects to the integrity of the system,
4. There may be blackouts.

All the above described points have significant disadvantages as explained below:

Permanent damage of equipment like circuit breakers, if the fault current exceeds the rating of the breaker. The cost of replacing a breaker would run into thousands of dollars.

To change system configuration as a permanent solution is not acceptable, as it affects the power system reliability, actually reduces system reliability, plus there is an increase in the system losses.

As today's industry is totally dependent on electrical energy, it requires a continuous flow of electrical energy and blackouts are strictly unacceptable. The most accurate and desired solution would be to limit the fault current during fault or short circuit by installing a FCL in the power systems.

## 1.4. Literature survey

Before the research and development of the fault current limiter, the main area of research was to break the circuit during fault in order to save the expensive equipment at power grids from large fault currents generated during fault. In order to handle large fault currents circuit breaker with large rating were developed. But the problem with the circuit breakers is that they have a limited life period, and cannot break the circuit until the first current cycle goes to zero. The research and development of fault current limiters started many years ago. First the basic idea was to limit the fault current so it does not matter if the system is disconnected from

supply. Many other methods were used, like air core reactors, basically it was a good approach but the only disadvantage was very high voltage drop in normal operation, for which volt-ampere reactive (VAR) compensation was required. The increase in the size of the system is the other disadvantage of this approach.

The specifications of the Fault Current Limiter and a description of the limiting behaviour and the installation of the FCL are discussed in [1].

The FCL based on the Microprocessor/computer controlled method is discussed by M.M.A.Salama [2, 3]. It consists of an LC circuit tuned to minimum impedance at supply frequency and a thyristor controlled reactor as a shunt which is connected across the capacitor. The current is limited by varying the firing angle of the thyristor, due to which the circuit breaker and other protective systems can operate. The sensor and control circuits should operate accurately to detect the fault current.

Fault Current Limiter reported in [4] is based on an electromagnetic circuit with iron core and adjustable air gap. Basically the impedance is much less during normal supply operation. During fault the forces produced by the fault current on the plunger causes the inductance of the device to increase, which limits the current during fault. The proper mechanical movement of the plunger is the main concern.

Different approaches of limiting fault current by using PTC thermistors have been explained by Dougal [5]. The results show that the path is good enough to limit the fault current but at the same time the material characteristics need to be known in order for it to work efficiently.

The sensor is used to detect the fault current and the action to limit the current is carried out rapidly [6]. This limits the first peak of the fault current.

A thyristor controlled series capacitor (TCSC) circuit is used to improve the performance of the Con Edison distribution substation at 138kV voltage levels during increase in the load [7]. Basically the idea here is, without increasing the fault current in the substation the power during normal operation is increased [16,17].

The Inrush Current Limiter (ICL) has been discussed by Samii [8]. It is a thermistor with negative temperature co-efficient (NTC). The resistance of the Thermistor drops logarithmically as its temperature increases. Here the size matters because the amounts of power that can be handled by ICL depend on its size.

The design, characteristics and principle in different modes of the Passive Fault current Limiter have been explained in literature [9,10,11,12and13].The core operates in saturation during normal operation offering very low impedance and during fault the core comes out of saturation in alternative half cycle. The most important aspect

of the FCL is that it is a passive device and is therefore reliable, compact in size and has fail safe operation. It does not need any external sources or power to perform its operation. Saturable core materials and Nd-Fe-B permanent magnet is used. Core materials with low saturable flux density are preferred. Care should be taken during design to have uniform flux density under normal operation; otherwise the core will come out of saturation even during normal operation. It is possible to design MCL both for single phase and three phase application [14].

The importance of the High Temperature Superconductor Fault Current Limiters in the local distribution systems is explained [18]. It explains the use of HTSFCL in the network and the ideal characteristics of the HTSFCL that are desired to have a more reliable power system. The High Temperature Superconductor's materials are also discussed.

D. Ito [22] explained the design and working of the Superconductor Fault Current Limiter, made of ultra fine NbTi filaments. It consists of non-inductive wound superconductor trigger coil and a superconducting limiter coil which act as a reactor. Its limits currents up to 120 A at a terminal voltage of 420 V and cannot be applied to high voltage systems. The experimental results show it can recover to the initial state in a short period of time.

E.Thuries [23] has presented an approach towards 25 kV Single Phase Superconductor Fault Current Limiter, having a low loss AC superconducting wire with very fast transition characteristics. This prototype consists of NbTi superconducting coil without an iron core which is kept inside a conventional cryostat with liquid helium. The low temperature SFCL is discussed in [20].

S.Shimizu [24] shows the results of a Three Phase Superconductor Limiting Reactor to a single-line–to-ground fault, the fault current is limited by a large zero-phase-sequence reactance of the limiter and in the case of Two Phase Short Circuit; the fault current is limited by the resistance of the winding.

The working of the Hybrid Inductive Type Superconductor Fault Limiter has been explained by Tixador [25]. In this limiter two superconducting windings are used, one used for triggering and the other is used to limit the current during fault. Due to the use of the two superconducting coils the heating in the limiter is reduced but at the same time it increases the cost.

The development of the 6.6kV/1.5kA class Superconducting Fault Current Limiter has been explained by D.Ito [26]. The Limiter has 42 strands AC Superconducting wire with ultra-fine NbTi filaments with high resistivity. It is shown

that the limiter was able to limit fault current to a lower value, which was 55kA during short circuit in the system.

The High Temperature Superconductor of inductive type with iron core has been explained and fabricated by J.R.Cave [27]. The Superconductor is cooled by liquid nitrogen at 77K and the prototype less than 1kVA has been fabricated.

The causes which affect or degrade the performance of the Superconductor Fault Current Limiter are investigated by T.Verhaege [28]. These causes include wire deformation, ac losses, self magnetic field, heating and mechanical affects.

The method of reducing ac losses in the 6.6kV Superconductor Fault Current Limiter coil is reported by T.Yazawa [29]. The conductor is double-twisted multi-filament NbTi cable which consists of strands in high resistivity CuNi matrix and the diameter of the filament is reduced in order to reduce the AC losses in the Limiter

The design and simulation using numerical calculation model in computer of a magnetic-shield type superconducting fault current with high Tc Superconductor limiter has been reported by K.Kajikawa [30]. The ceramic superconductors are used at liquid nitrogen temperature. The flux jumping phenomenon is derived and its requirements are explained.

The critical current, resistivity and flux flow creep properties of the high Jc Bi2223 and YBCO superconducting bulks are investigated and from the experimental results, applicability of the bulk to superconductor fault current limiter device has been explained by D.Ito[31] The results show Bi2223 has high resistivity and YBCO has high critical current density.

Surge protection of the power girds has been explained by E.Leung [32]. The positioning of the Fault Current Limiter in the network and the advantages of the Limiters in the network has been explained.

Different types of Superconducting Fault Current Limiters, their characteristics, superconductor materials used are discussed by Will Paul [33]. Both the shield core and resistive types Superconductor Fault Current Limiter has been explained and the commercial outlook of the SFCL is also discussed.

The technical and economical benefits and the application of the Fault Current Limiter along with simulation and test results are presented [34]. In this paper the principle of the High Temperature Superconductor Fault Current Limiter with resistive and shielded core type has been explained. The large size and its use only for AC Current is the main disadvantage of the shield core type. The transient behaviour of the Fault Current has also been discussed.

A 15 kV/20 kA HTS inductive/electronic Fault Current Limiter has been developed [35]. The Department of Energy Superconductivity Partnership Initiative phase II has also played a part to develop the Limiter. The coils in the Limiter operate at 35K and can carry a continuous DC current of 2000A and AC current pulse of 9000A.

The development of the HTS Three-Phase Saturated Core Fault Current Limiter prototype model has been discussed [36]. A single DC HTS coil has been used to saturate the iron yokes of all the three phases.

The 6.4 MVA Superconductor Fault Current Limiter has been demonstrated by ABB [37]. The Bi-2223 ceramic superconductor is used in the limiter and novel conductor design is used with Bi-2223 fabrication technology.

The formation of the America Superconductor in 1987 enhances the development of the High Temperature Superconductor applications. The American Superconductor is also developing the HTSFCLs [38].

A MATLAB-based power system toolbox (PST) dynamic simulation and design concepts of the power system has been explained [39]. The purpose of this MATLAB based Power System Toolbox is to provide a flexible environment for performing power system simulations. The MATLAB coded functions are in the equipment models that can be used in simulation. It can only be used for design or simulation of small power systems and is mainly used for teaching in the institutes to undergraduate students.

The analysis of the faults in the interconnected power system has been explained in this paper [40]. Experiments were done by the undergraduate students of the Drexel University's Interconnected Power Systems Laboratory (IPSL). The behaviour of the current and voltage during fault is analysed. The paper explains how to create a fault in the system. The hardware and software tasks performed during experiments are explained.

The short circuit currents and fault currents of an industrial plant have been analysed in this paper [41]. In this paper mathematical modelling of each component is done and the fault currents are calculated from the mathematical expression of the components. The Digital simulation is done using Power System Blockset (PSB) of MATLAB. The model is Graphical User Interface as well.

The factors affecting the Stability of the Power Systems has been discussed and explained in [42]. The factors and the relationship between them are explained and the transient stability of the power system has also been discussed. Different types of the

Power System Stabiliser are explained. Basically this paper covers all the factors that affect the stability of the power systems and methods to improve the stability of the system are also discussed.

The advantage of the open software over the commercial (closed) software has been explained [43]. This paper explains the new MATLAB based Power System Analysis Toolbox (PSAT). It explains the different simulation that can be done in PSAT on the Power System networks. PSAT is also provided with a complete set of user-friendly graphical interfaces and a Simulink-based editor of one-line network diagram. The use of PSAT in universities and commercially is explained in the [44]. The power systems web virtual laboratory is becoming popular and is being used in the universities for teaching of power systems. This paper also explains how the problems of the people who use PSAT are solved through PSAT web forum.

## 1.5 The different Current Limiter approaches

A few approaches of limiting fault current are discussed.

The approaches are

1. Superconductor based devices.
2. In Line fuse devices
3. Resonant circuit devices
4. Switched devices.

## 1.6 Superconductor based devices

Basically there are three configurations of superconductor based fault current limiting devices. In each case the superconductor element is placed parallel with the impedance element. The three types of devices based on the superconductor element are superconductive shunt with a resistive bypass element, superconducting shunt with an inductive bypass element and transformer coupled superconductor shunt.

### 1.6.1 Superconductive shunt with a resistive bypass element

The superconductive shunt with resistive bypass is shown in figure 1.1[22]. In this case the bypass element limits the current during fault. The fault current is limited when it is more than the critical current of the superconductor element and it operates in high resistance state which limits the fault current. Superconductor material of high resistivity in its non-superconductor state is preferred as it will limit the current during

fault. During normal operation the R2 is zero and when there is fault, resistance R2 becomes very high which limits the current during fault. The resistance R is the bypass resistance. During fault the fault current is transferred from resistance R2 to R.

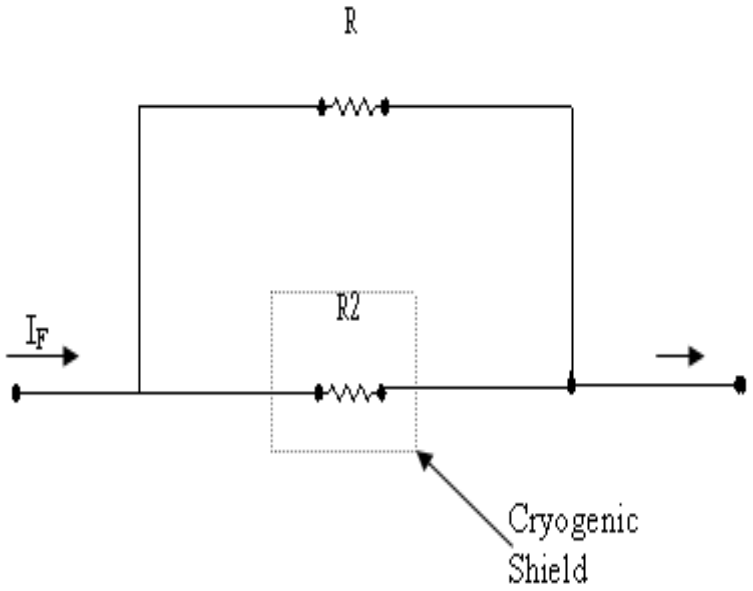



**Figure 1.1** Superconductor Fault Current Limiter, Resistive Shunt type

An external source or magnetic field is needed to bring the superconductor into its off-state. The superconducting device takes a long time to recover from its fault current limiting properties as the coolant must be cooled back to its prefault temperature. The main disadvantage of this approach is the cost as well as the reliability of the cooling system for the superconductor, as it has to be cooled to the temperature of helium and the cooling system requires maintenance from time to time.

### 1.6.2 Superconductor FCL with an inductive by pass element.

Figure 1.2 shows the circuit for a superconductor FCL with inductive bypass element [25]. The trigger coil is wrapped over the other coil with low inductance design. During normal operation the current is very low and the superconductor element remains in superconductor state and the voltage drop is also very low.

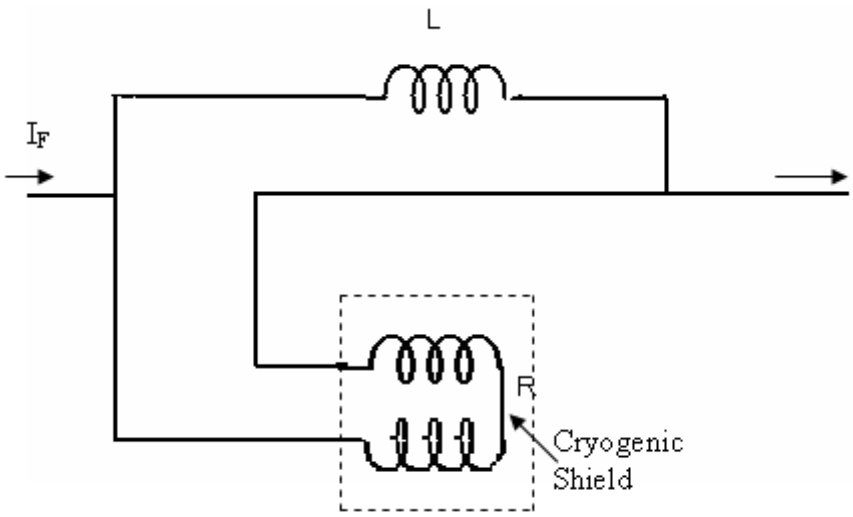



**Figure1.2** Superconductor FCL with inductive bypass element

During fault large amount of fault current is transferred to the bypass element. The ratio of the bypass coil impedance and the non superconducting element impedance determine the current level in the trigger coil during the fault.

### 1.6.3 Transformer coupled superconductor FCL

Figure 1.3 [23] shows the transformer coupled superconductor FCL. During normal operation there is no interaction of the field due to current within the interior of the inner coil. Due to very small air gap between the inner and the outer coil, results in a low inductance design. During fault the current becomes greater than the critical current of the superconductor FCL, the effective inductance increases to a high value because the flux links with the centre of coil. During fault the current is transferred to the bypass element and due to high impedance the fault current is limited.

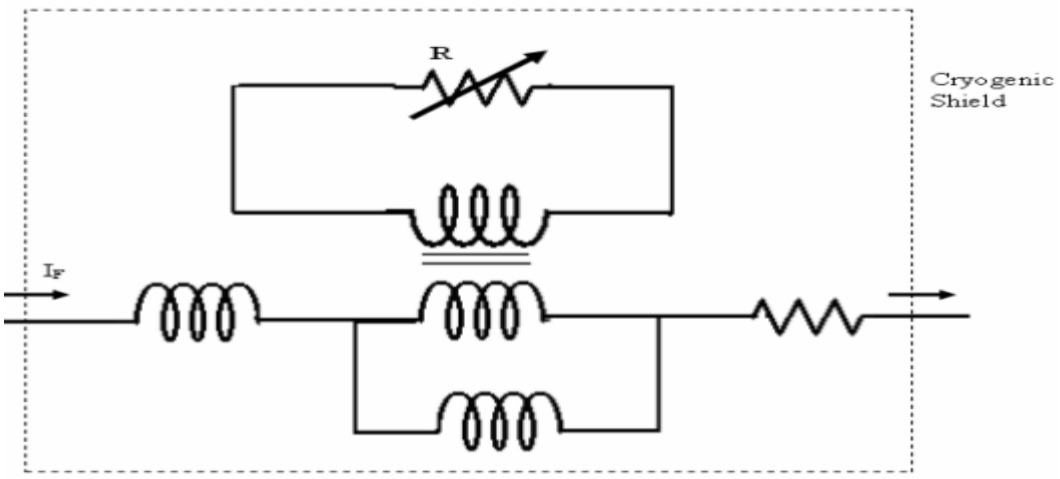



**Figure1.3** Transformer coupled Superconductor FCL

## 1.7 Resonant Circuit Limiter

The circuit of the resonant limiter is shown in Figure 1.4 [15].

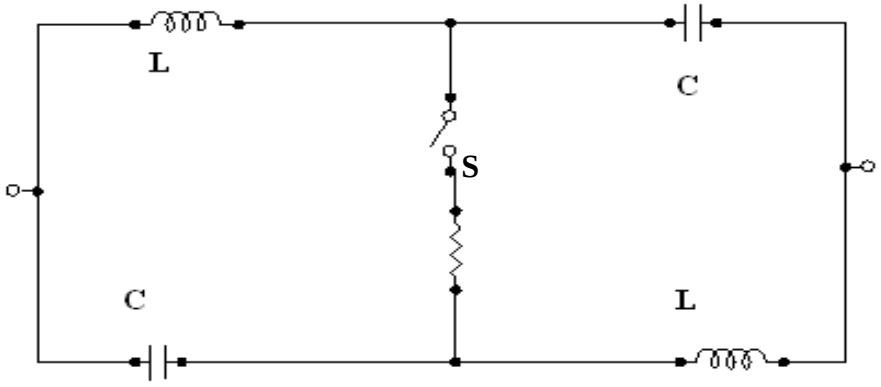



**Figure 1.4** Resonant Circuit Limiter

During normal operation the switch S is open and the effective impedance of the circuit is very low as the capacitor and inductor in both sides are in series.

During fault the effective impedance increases, this becomes equal to equivalent reactance in series with equivalent resistance. Due to high resistance the fault current is limited to a lower value. Due to switching action there might be a spark across the switch because of the voltage appearing across one of the capacitors. If one of the components, the capacitor or reactor becomes faulty, the current limiting action of the circuit will no longer be valid. The cost and large size are its main drawbacks.

## 1.8 Using Fuse as a Fault Current Limiter

Figure 1.5 shows the circuit of using a fuse as a limiter. The basic idea is that when the switch opens it generates a voltage arc and the current in the arc is transferred to the silver sand fuse. Once the fuse melts the current is transferred to the resistor across it.

The main thing to be considered with this approach is the mechanism associated with the operation of the bypass switch. The other method used, based on this approach, is the current limiting protector which is mainly used in the distribution systems. In this method the sensing and the switch operation mechanism are separated from each other.

This circuit consists of silver sand fuse and a copper conductor which is parallel to the fuse and has s series of notches. The fuse melts upon fault, this is accomplished by high arc voltage which limits current. The melted fuse and the notches on the copper conductor limit the fault current. The sensor detects the fault current.

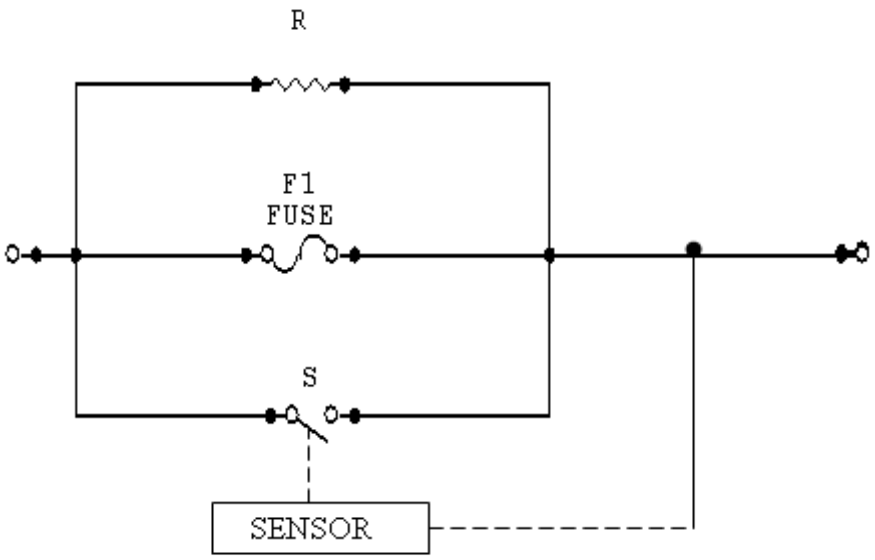



**Figure 1.5** Fuse based FCL

## 1.9 Switched devices for limiting fault current

In this method the devices used as FCL consist of commutation of the current from an opening of the switch to very high impedance element, which is in parallel to the switch. There are three types of switched devices; vacuum switches, fuses and forced chemical devices. In the vacuum switched method, the device is set into operation by artificially making the current zero by discharging a precharged capacitor through a second interrupting device.

The second method is used in transmission systems [15]. In this method, when there is fault the contacts of the protective switch open quickly. The low voltage arc is formed during opening of the contacts because they open in the vacuum. The interaction of the magnetic field and the arc causes the arc length to increase to a point where the arc no longer exists. Due to low voltage across the shunt capacitor the arc rapidly goes to zero. The fault current is transferred to the capacitor branch and the capacitor voltage rises; this voltage across the capacitor is limited by the voltage drop across the bypass resistor. The main advantage of this device is that the continuous current is carried by the device, the voltage rating can be increased by placing the switches in series, the coils and the power supply can be isolated from the line voltage and the current commutation is not polarity sensitive. The main drawback of this approach is that the current to be interrupted depends on the sensor response and the operating time of the mechanism.

## 1.10 Ways of dealing with Fault Current

From the literature survey most of the FCL are active devices and they need an external source to perform their current limiting action. The methods which are used in the past are shown in Table 1.1. The most common are still in use today as well as the circuit breaker. The circuit breaker can interrupt the current at zero crossing only. The high impedance transformers are used to avoid large fault currents during fault, again due to high impedance there is a large voltage drop and power losses during normal operation. The other ways to deal with fault current are shown in the table 1.1. These are fuse, air core reactors, low temperature superconductor fault current limiters and changing system configuration. The advantages and disadvantages of these approaches are shown in table 1.1

**Table 1.1 Ways of dealing with Fault Current**

| **Serial No.** | **Device** | **Advantages** | **Disadvantages** |
|---|---|---|---|
| 1 | Circuit Breaker | # Reliable<br># Disconnect the circuit during fault | # High Cost<br># Breaks the circuit at only current zero passage.<br># Less life |
| 2 | High Impedance Transformer | # Reliable<br># Used in the distribution and Transmission Systems | # High Losses<br># Low efficiency |
| 3 | Fuse | # Simple in design<br># Low Cost | # Needed to be replaced after every fault current.<br># Low capacity to withstand fault currents and breaks very soon. |

| | | | |
|---|---|---|---|
| 4 | Air Core Reactors | # Proven to be effective | # Very large voltage drops<br><br># Power losses during normal operation |
| 5 | System Reconfiguration | # Good and reliable for growing areas | # Reduces System Reliability and operating flexibility<br><br># High cost. |
| 6 | Low Temperature Superconductor Fault Current Limiters | # Effective in limiting current during Fault.<br><br># Low losses during normal operation | # High cost of Superconductor<br><br># High cost of cooling System<br><br># Takes a long time to return to its initial state |

## 1.11. The Purpose of the Research

The research has been carried out and the new approach of limiting current during fault using Passive Magnetic Current Limiter (MCL) and High Temperature Superconductor Fault Current Limiter (HTSFCL) has been discussed. MCL consist of the ferrite cores, permanent magnet and windings. In the past FCL devices used mostly sensing devices and coils to detect the fault current before it can limit it. The approaches used earlier are mostly dependent on the signal from the sensing element. The recovery time of some of the FCLs is not fast. The device must be reset after the fault is cleared.

The Passive MCL discussed does not need any sensing device to detect the fault current in the circuit which has a MCL in it. Moreover there is no need to reset the Passive MCL, it is automatically reset to its initial state after the fault is cleared. The voltage drop during normal operation across the MCL is low and during fault it has a very high voltage drop across it. The configuration of the Passive MCL is simple, low

cost and offers reliable operation. The main advantage of this device is that it does not need any external source to perform its operation.

In this work, the working and the design considerations of the passive fault current limiter has been explained. As explained earlier it is a passive device and consists of a permanent magnet sandwiched between ferrite cores. The connection of the winding is such that the direction of the magnetomotive forces and the alternative current are same in one core and opposite in the second core at the same time. As the cores operate in saturation during normal operation the effective impedance of the MCL is very low. During fault the cores come out of saturation in alternative half cycle of current as the magnetic flux during fault becomes greater than the flux due to permanent magnet, so the impedance increases which in turn automatically limits the current without the help of any external source. The experimental results for single and three phase circuits are reported with ferrite and steel core. The High Superconductor Fault Current Limiter for high voltage application has also been reported and the MATLAB simulation is performed to show its operation during fault and normal operation. The results obtained stand close to the ideal results.

The advantages of the Passive Magnetic Current Limiter are:

1. It is a passive device and does not require any external source to perform its function; this eliminates the cost of the sensing devices.
2. Simple structure and less cost
3. The function of the passive fault current limiter is automatic
4. Easy to understand the operating principle
5. No resetting of the device is needed as it resets automatically after the fault is cleared.

## 1.12 Organization of the thesis

This thesis is divided into eight chapters

In chapter 1 a brief introduction, literature survey and the different current limiter approaches used are discussed. Chapter 2 explains the operating characteristics and experimental results of the magnetic fault current limiter. In chapter 3 the field and thermal models of the device are made using FEMLAB. The variation of the magnetic flux and temperature with change in the current is shown. The operating principle and the MATLAB simulation of the High Temperature Superconductor

Fault Current Limiter (HTSFCL) are explained in chapter 4. The results with and without fault are shown in this chapter. Chapter 5 explains the design of the nine bus network in the PSAT and also shows the power flow results. Chapter 6 contains the results of the nine bus system during normal and fault operation in PSAT and the optimum location of the HTSFCL is discussed. Chapter 7 consists of conclusions and future work. References are provided after chapter7.

# Chapter 2
# Operating Principle
# of
# Magnetic Current Limiter

## 2.1 Introduction

Fault currents are a major problem in the operation of electrical equipment, often causing severe damage to the electrical components. An increased level of electricity consumption has led to a need for development of a device that can limit such fault currents to prevent or limit damage to electrical systems. The Magnetic Current Limiter (MCL) is a passive device which seeks to overcome some of the limitations of traditional fault limiters.

The Magnetic Current Limiter consists of two magnetic devices. Each device consists of a permanent magnet and ferrite core. The operating principle and the design parameters of the fault current limiter are described in this chapter. The behaviour of the cores under saturation and unsaturation state is discussed in this chapter. The topological configuration of different schemes of MCL has also been described in this chapter.

## 2.2 Operating Principle of Magnetic Current Limiter

The configuration of Magnetic Current Limiter (MCL) consists of two magnetic devices connected in series and with opposing magneto motive forces (mmf). Each magnetic device consists of permanent magnet and ferrite core. The permanent magnet is sandwiched between the pole faces of the two low saturation flux density materials, for example the ferrite core as shown in the Figure 2.1. The permanent magnet is used to saturate the core under normal operating conditions. The connection to the coil is such that the mmf generated by alternative current source and the permanent magnet are in the same direction in core #1 and opposite in the core #2 at the same time.

Under the normal operation, the current has a low value and both the cores remain saturated below a specific value of current. The effective impedance of both

the cores is low as they are in saturation and represented as the sum of the saturated differential inductance of both cores. During fault, current rises to a high value that forces both the cores to come out of saturation in alternative half cycles of current. As the current rises to a high value the effective impedance of the core rises, this becomes equal to unsaturated inductance of one core plus saturated inductance of the other core and the flow of a large fault current is restricted. The material used for the cores should have a low value of saturated flux density compared to permanent magnet in order to keep the core in saturation under normal operation. The ferrite core is used instead of steel because the saturation flux density of steel is greater than the remanant flux density of permanent magnet (NdFeB). The ferrite core remains in saturation under normal operation because it has a low saturation flux density as compared to steel. The other benefit of using ferrite as a core material is that the same cross section area of the core can be used as that of a permanent magnet, which would not be possible for steel core. The MCL is represented as FCL in Figure 2.1.

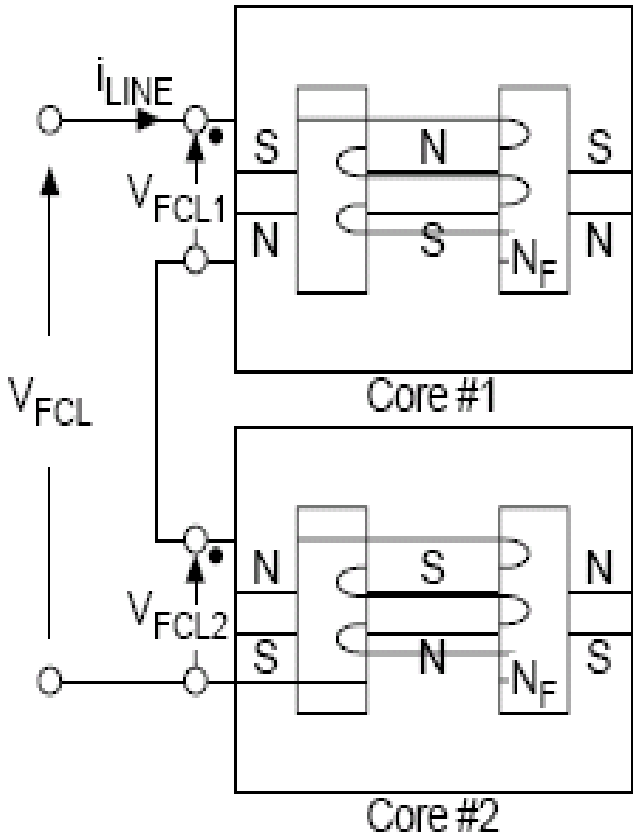



**Figure 2.1** The Basic structure and configuration of MCL

## 2.3 B-H Characteristics of MCL

The B-H characteristics are used to derive the expressions for B and H in the core and the permanent magnet. The B-H characteristic curves are assumed to be simple straight lines for the purpose of the numerical analysis. However, in reality the curves for both the permanent magnet and the core would be smooth curves, since the value of the relative permeability in each material is not constant.

The basic operation of the Magnetic Current Limiter depends on the saturation properties of the core. If the current in the coil is increased from zero, to increase H, then B also increases along with H up to the point referred to as the "saturated magnetism" as shown in Figure 2.2. After this point B does not increase significantly with further increase in H and the material or core is said to be "saturated". In saturation, the reluctance is very high; therefore it has a low value of inductance. It can be observed from Figure 2.2 that before the point $B_{sat}$. B and H increased simultaneously, but as B reached $B_{sat}$, there was no significant increase in the value of B along with increase in the value of H.

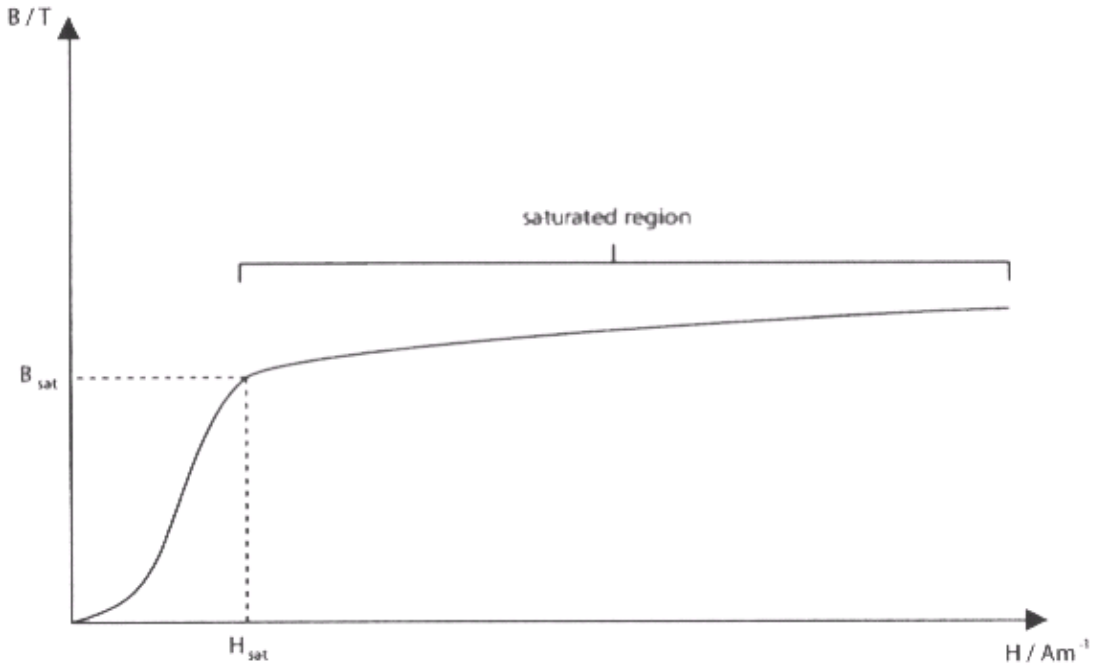
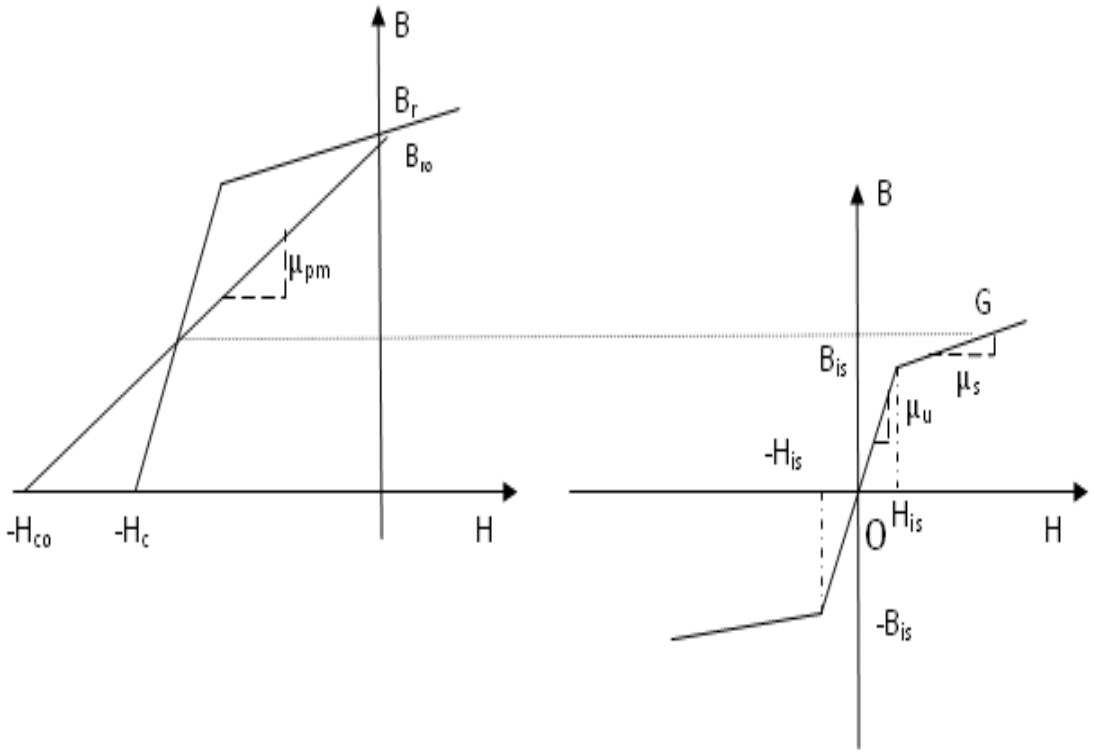



**Figure 2.2** Magnetisation curve showing the saturated region

The B-H characteristic of the permanent magnet and ferrite core are shown in Figure 2.3. The B-H characteristic of the permanent magnet is represented by straight

line having constant recoil permeability $\mu_{pm}$. The permanent magnet operates or forces the core in the saturation which has low impedance under normal operation.

The characteristics of the ferrite core are approximated with constant lines having different gradients. Where the ferrite core operates in saturation under normal operation, the permeability has been shown as $\mu_s$ and in unsaturation as $\mu_u$.




**(a)** **(b)**

**Figure 2.3** The B-H characteristics of the permanent magnet and Ferrite core

In Figure 2.3(b) $B_{is}$ is value of B at which the core becomes saturated and the corresponding value of H is $H_{is}$.

The permanent magnet forces the core to operate in saturation at point G as shown in Figure 2.3(b). The operating point has an offset at zero current operation. The new offset characteristic for the core in the positive half of current can be obtained by shifting the origin O to point G as shown in Figure 2.4.

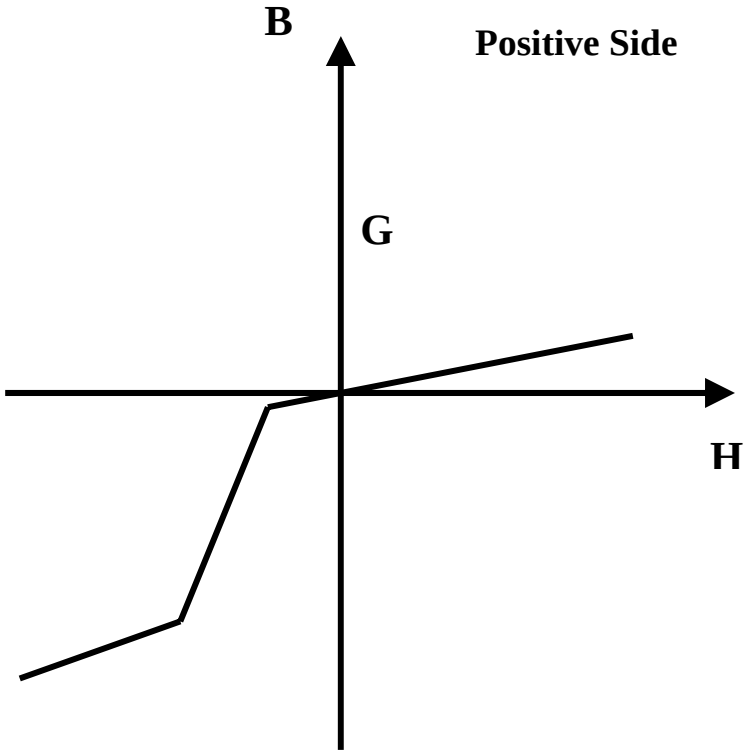



**Figure 2.4** Characteristic of core used in positive half of current

During the negative half of the current the new offset characteristic of the core has been represented in Figure 2.5. The origin is shifted from O to G.

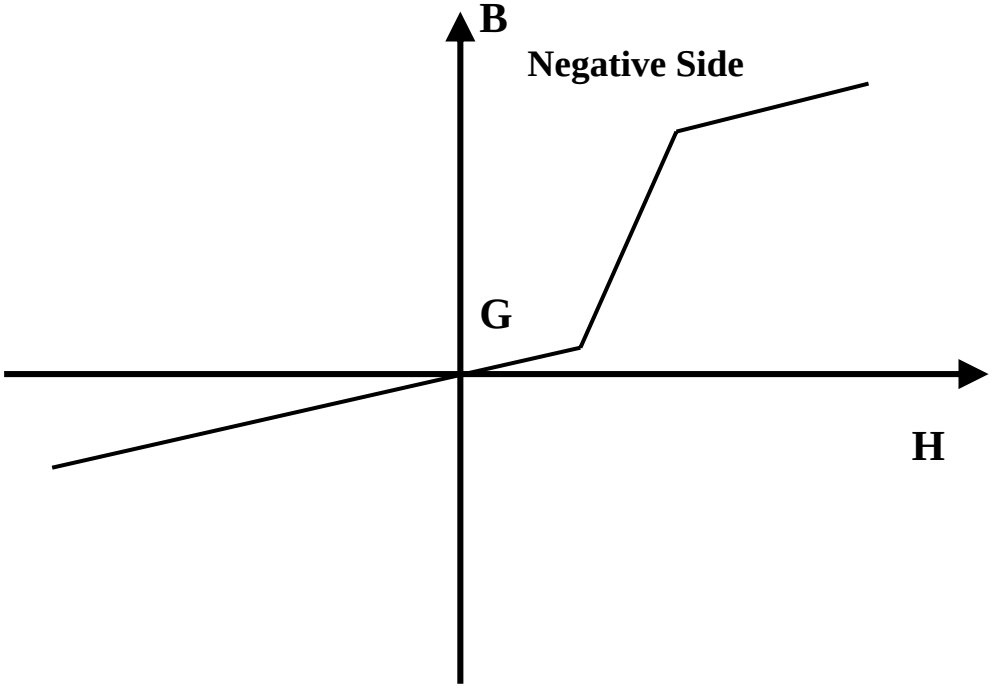



**Figure 2.5** Characteristic of core used in negative half of current

The new offset characteristic under normal operation shows that the core is forced to saturation for both halves of the current. The operational characteristic of the MCL shown in Figure 2.6 is the combination of the two halves of current. The figure shows the ideal characteristic of the MCL for both the halves of the current. The observed characteristic exhibits a constant change in the gradient as the magnetic field intensity changes. The constant change in the gradient of the observed characteristics represents the non uniform distribution of flux throughout the core, which is not desired in the operation of MCL. Due to constant change in the gradient some portions of the core come out of saturation at lower levels of the current. It is desirable that the core used should have a low saturation flux density and a very low value of saturated magnetic permeability in order to avoid it to coming out of saturation during normal operation and when there is a low current.

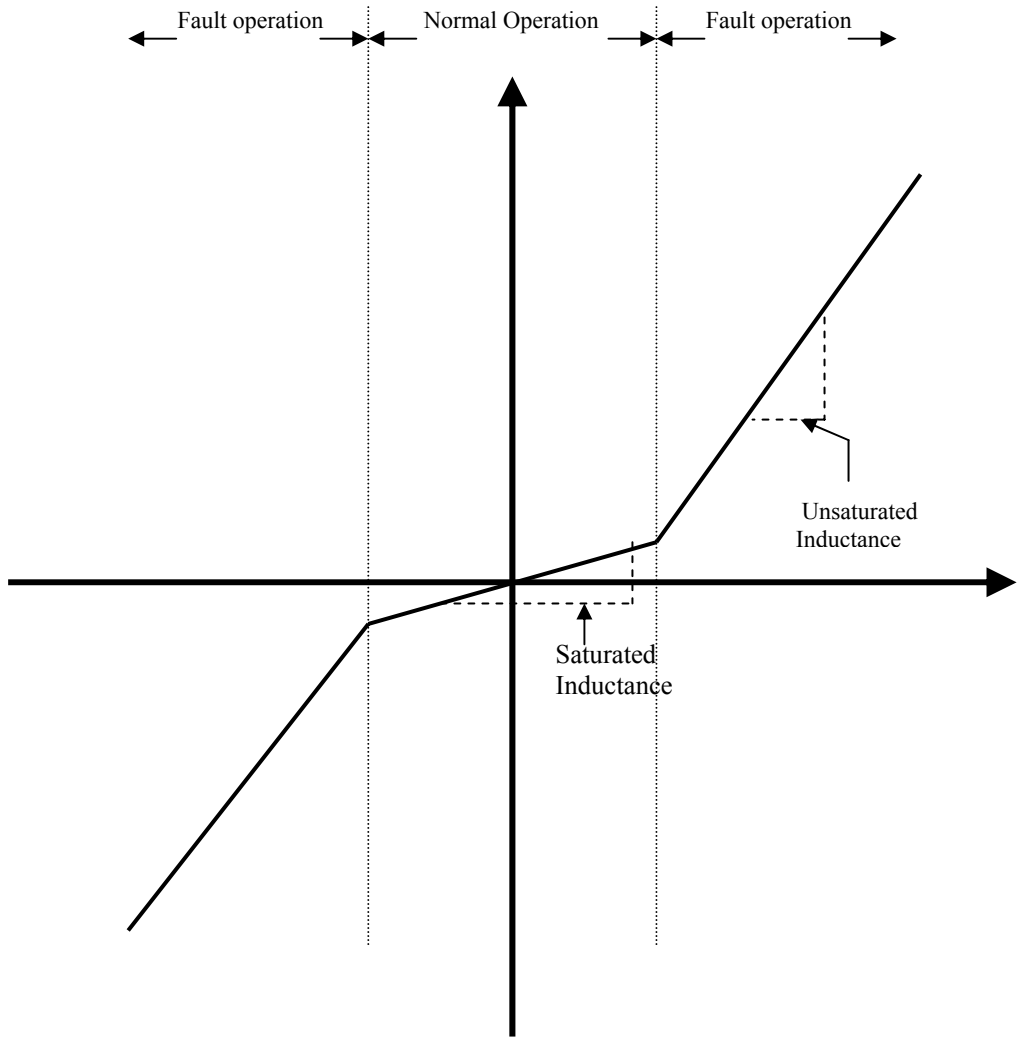



**Figure 2.6** The combined ideal B-H characteristic of MCL

From the above Figure 2.6 it can be observed that during normal operation, the core operates in saturation which has saturation inductance ($L_s$). Because saturation inductance is considerably less, the MCL has low impedance under normal operation and during fault the cores come out of saturation, $L_u$ is the unsaturated inductance which has a very high value thus resulting in the current limiting action of the MCL.

The B-H characteristics of the permanent magnet and core in Figure 2.3(b) are used to derive expressions for B and H in the saturated and unsaturated regions.

The core operates in two regions, an unsaturated region and a saturated region

**In the unsaturated region** ($B < B_{is}$)

From the B-H characteristics (Figure 2.3(b)), $\boldsymbol{B_{is}}$ and $\boldsymbol{H_{is}}$ is the core's flux density and magnetic field intensity at knee point respectively

B is given by

$$B = \mu_u \; H_{core} \tag{1}$$

Where $\mu_u$ is the permeability of the core in the unsaturated region, $H_{core}$ is the magnetic field intensity of the core.

Now Rearranging for $\boldsymbol{H_{core}}$

$$H_{core} = \frac{B}{\mu_u} \tag{2}$$

**In the saturated region** ($B > B_{is}$)

The B versus H curve is a straight line in the saturated region, the expression for B in the saturated region is given by

$$B = B_{is} + \mu_{is}(H_{core} - H_{is}) \tag{3}$$

Where $\mu_{is}$ is the permeability of the core in the saturated region

Rearranging for $\boldsymbol{H_{core}}$ gives,

$$H_{core} = \frac{B - B_{is}}{\mu_{is}} + H_{is} \qquad (4)$$

**Permanent magnet**

From Figure 2.3(a) the B versus H curve is a straight line with constant gradient The expression for B is as follows,

$$B = \mu_{pm} (H_{pm} + H_c)$$

Where $\mu_{pm}$ the permeability of the permanent magnet and $H_c$ is the value of $H$ when $B=0$,

So rearranging for $H_{pm}$ gives,

$$H_{pm} = \frac{B}{\mu_{pm}} - H_c. \qquad (5)$$

**Ampere's Magnetic Circuit Law**

The electrical behaviour of the Magnetic Current Limiter is studied using Ampere's law and its functional characteristics are mainly dependent on the amount of flux that exists in the MCL.

Ampere's Circuit Law for the closed magnetic circuit is

$$H_{core}l_{core} + H_{pm}l_{pm} = Ni \qquad (6)$$

Where $l_{core}$ and $l_{pm}$ are the lengths of the core and permanent magnet respectively, and $N$ is the number of coil turns, substituting the expression for $H_{pm}$ obtained from equation (5) gives,

$$H_{core}l_{core} + \left(\frac{B}{\mu_{pm}} - H_c\right) l_{pm} = Ni \qquad (7)$$

The relationship between B and current (i) in the saturated and unsaturated region can be derived,

**Unsaturated region** ($B < B_{is}$)

Substituting the value of $H_{core}$ from equation (2) in the equation (7) of the Ampere's circuit equation, we get

$$\frac{B\, l_{core}}{\mu_u} + \left(\frac{B}{\mu_{pm}} - H_c\right) l_{pm} = Ni$$

Rearranging for *B*,

$$B = \frac{Ni + H_c l_{pm}}{\left(\frac{l_{core}}{\mu_u} + \frac{l_{pm}}{\mu_{pm}}\right)}$$

**Saturated region** ($B > B_{is}$)

Now substitute the value $H_{core}$ form equation (4) into equation (7), we get

$$\left(\frac{B - B_{is}}{\mu_{is}} + H_{is}\right) l_{core} + \left(\frac{B}{\mu_{pm}} - H_c\right) l_{pm} = Ni$$

Rearranging for B yields

$$B = \frac{Ni + H_c l_{pm} + \frac{B_{is} l_{core}}{\mu_{pm}} - H_{is} l_{core}}{\left(\frac{l_{core}}{\mu_{is}} + \frac{l_{pm}}{\mu_{pm}}\right)}$$

Rewriting the equation (4) of the permanent magnet in terms of flux, mmf and reluctance. Multiplying $l_{pm}$ by both sides, we get

$$H_{pm}l_{pm} = \frac{B}{\mu_{pm}} l_{pm} - H_c l_{pm}$$

$$H_{pm}l_{pm} = - H_c l_{pm} + B\, S_{pm} . \frac{l_{pm}}{\mu_{pm} S_{pm}}$$

$$= - H_c l_{pm} + \phi_{pm}\, r_{pm} \qquad (8)$$

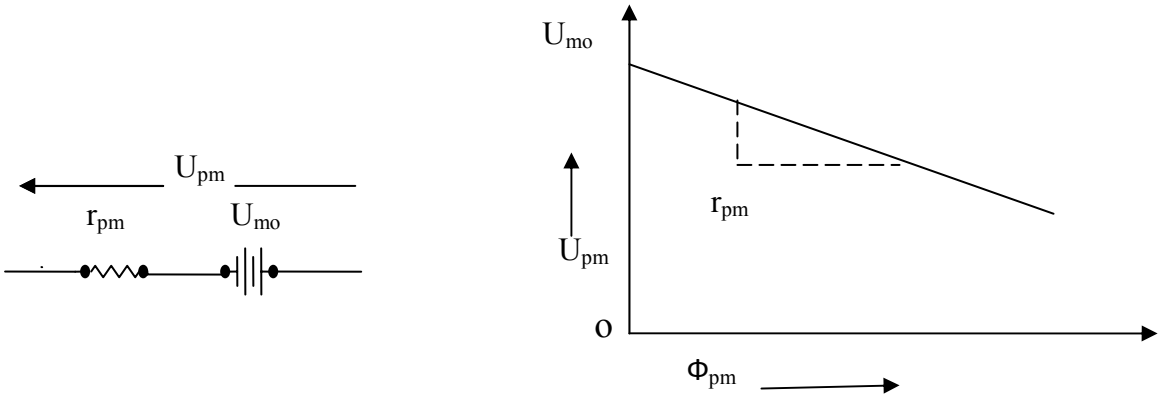
In terms of mmf and flux the above equation can be written as,

$$u_{pm} = U_{mo} + \phi_{pm}\, r_{pm} \qquad (9)$$

here $U_{mo} = - H_c l_{pm}$

The above equation (9) is represented in Figure 2.7(a) and Figure 2.7(b) which show its characteristics. Where $u_{pm}$ is the mmf across the permanent magnet and $U_{mo}$ is the mmf corresponding to the coercive force. $\phi_{pm}$ is the flux through the permanent magnet and $r_{pm}$ is the reluctance of the permanent magnet and is given by,

$$r_{pm} = \frac{l_{pm}}{\mu_{pm} S_{pm}}$$




**(a)** **(b)**

**Figure 2.7** Permanent Magnet's circuit and it's characteristics in the MCL

Now writing the equation of the core in terms of mmf, flux and reluctance.

**In the unsaturated region** ($B < B_{is}$)

Multiplying both sides of the equation (2) by $l_{core}$, we get

$$H_{core} l_{core} = \frac{B}{\mu_u} . l_{core},$$

$$= \frac{l_{core}}{\mu_u S_{core}} . B S_{core} \left( \frac{1}{S_{core}} \right)$$

$$u_f = r_u . \phi_f$$

**In the saturated region** ($B > B_{is}$)

Multiplying both sides of the equation (4) by $l_{core}$,

$$H_{core} l_{core}, = l_{core},. \frac{B - B_{is}}{\mu_{is}} + H_{is} l_{core},$$

$$H_{core} l_{core} = \frac{B_{is}}{\mu_u} l_{core}, + \frac{l_{core}}{\mu_{is}} (B - B_{is})$$

Or $$u_f = r_u \phi_{knee} + r_{is}(\phi_f - \phi_{knee})$$

$$= -(r_{is} - r_u) \phi_{knee} + r_{is}$$

$$u_f = -U_{01} + r_{is} . \phi_f \qquad (10)$$

Where $\phi_{knee} = B_{is} S_{core}$ and $\phi_f = B.S_{core}$

The equivalent circuit of the above equation (10) is represented in Figure 2.8 and its characteristic is presented in Figure 2.9.

Where $u_f$ and $\phi_f$ are the mmf across the core and flux through the core respectively. $r_u$ and $r_{is}$ are the reluctances of the core in unsaturated and saturated region respectively and are given as,

$$r_u = \frac{l_{core}}{\mu_u S_{core}}$$

And

$$r_{is} = \frac{l_{core}}{\mu_{is} S_{core}}$$

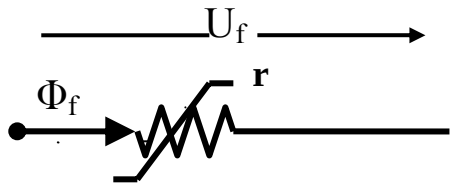



**Figure 2.8** Equivalent circuit of Ferrite core in the MCL

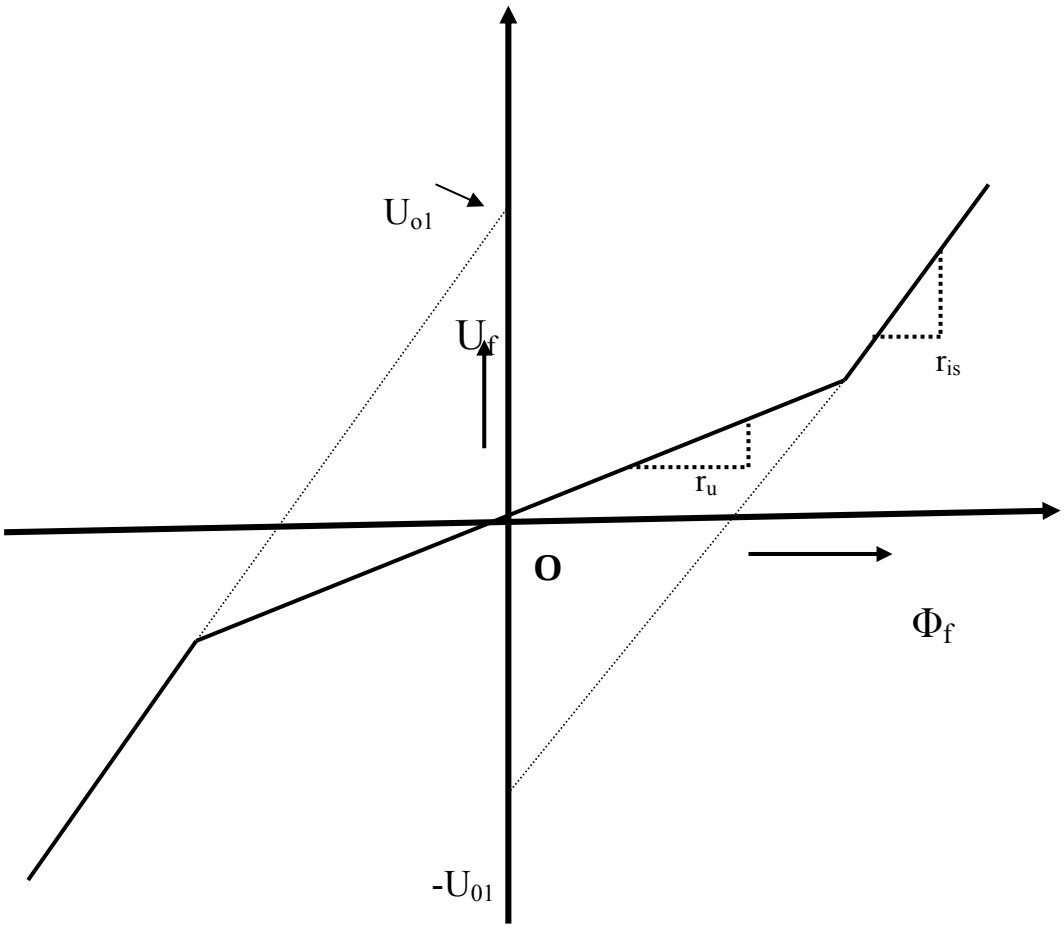



**Figure 2.9** Characteristic of the ferrite core in the MCL

## 2.4 Operation of MCL in the AC mode

When the AC current flows in the winding of the MCL, the operation is represented by the Ampere Law equation (8). The mode of operation, normal mode or fault, depends upon the magnitude of the current in the winding. The flux corresponding to the current can be any one of the following three:-

1. $\phi < -\phi_{knee}$

2. $\phi_{knee} < \phi < -\phi_{knee}$

3 $\phi > \phi_{knee}$

The operation of the two cores, core #1 and core #2 are considered separately. Considering core #1's operation in the positive half of current the flux linked with it is $\phi$ and considering core #2's operation in the negative half of current, flux linked with it is $-\phi$. The operation of each core is as follows

For core #1,

(i) $0 < \phi < \phi_{knee}$

(ii) $\phi > \phi_{knee}$

For core #2,

(i) $\phi < -\phi_{knee}$

(ii) $-\phi_{knee} < \phi < 0$

The equation (5) can be expressed in terms of flux and reluctances for core #1,

Condition (i) $0 < \phi < \phi_{knee}$

From B-H characteristics of the core, core #1 operates in the unsaturated region, the equation (6) can be written as,

$$- H_c l_{pm} + \phi_{pm} r_{pm} + \phi_f r_{1u} = Ni$$

$$\phi = \frac{Ni + H_c l_{pm}}{r_{pm} + r_{1u}}$$

Where [$\phi = \phi_{pm} = \phi_f$] and $r_{1u} = \frac{l_{core1}}{\mu_u S_{core1}}$, reluctance of the core#1, $S_{core1}$ and $l_{core1}$ are the area and length of the core #1

i, is negative in the condition (i)

Condition (ii) $\phi > \phi_{knee}$ ; From the B-H characteristics (see Figure 2.3(b)) of the core, core #1 operates in the saturation region, the equation (6) can be written as

$$- H_c l_{pm} + \phi_{pm} r_{pm} + r_{1is} (\phi_f - \phi_{knee}) = Ni$$

$$\phi = \frac{Ni + H_c l_{pm} + \phi_{knee} r_{1is}}{r_{pm} + r_{1is}} \qquad (11)$$

In this condition (ii) current, i can have either a positive or negative value. The $r_{1is}$ is the reluctance of the core #1 in the saturation and is given by,

$$r_{1is} = \frac{l_{core1}}{\mu_{is} S_{core1}}$$

and

$$\phi_{knee} = B_{is} S_{core1}$$

As explained earlier the suffix “is” and “u” represent the saturated and unsaturated state respectively.

Similarly expression for flux for core #2 is as follows:

Suppose $r_{2is}$ and $r_{2u}$ are the reluctance of core #2 in the saturation and unsaturation region respectively

As the length and area of both cores are equal, the reluctance for both the cores will be equal and can be written as,

$$r_{is} = r_{1is} = r_{2is}$$

and

$$r_u = r_{1u} = r_{2u}$$

For $\phi < -\phi_{knee}$

$$\phi = -\left[\frac{N i + H_c l_{pm} + \phi_{knee} r_{is}}{r_{pm} + r_{is}}\right] \quad (12)$$

Based upon the above equation a general expression for flux, $\phi$ can be written as,

For $-\phi_{knee} < \phi < \phi_{knee}$

$$\phi = \pm\left[\frac{Ni + H_c l_{pm}}{r_{pm} + r_u}\right] \quad (13)$$

In the equation (13) a "-"sign is used for the core #2 and a "+" sign is used for core #1. Current i can have any value, positive or negative.

In the expression for $I_{knee}$ and $I_{max}$ related to the knee point flux, $\phi_{knee}$ can be obtained by replacing i in the equations (11), (12) and (10) by i, $I_{max}$ and $I_{knee}$, we get

$$I_{knee} = \frac{H_c l_{pm} - \phi_{knee}(r_{pm} + r_u + r_{is})}{N}$$

and the maximum current, $I_{max}$ is related to knee point flux by

$$I_{max} = \frac{H_c l_{pm} + \phi_{knee}(r_{pm} + r_u + r_{is})}{N}$$

Now in order to obtain the AC flux, $\phi_{ac}$, the DC flux, $\phi_{dc}$ should be subtracted from $\phi$ obtained from equations (11), (12) and (13).

## 2.5 DC operation of MCL

In the DC operation of the MCL, the mmf due to permanent magnet and the mmf due to current will be opposite to each other. The circuit representation is shown in Figure 2.10.

$u_f = -u_{pm}$

$u_f + u_{pm} = 0$

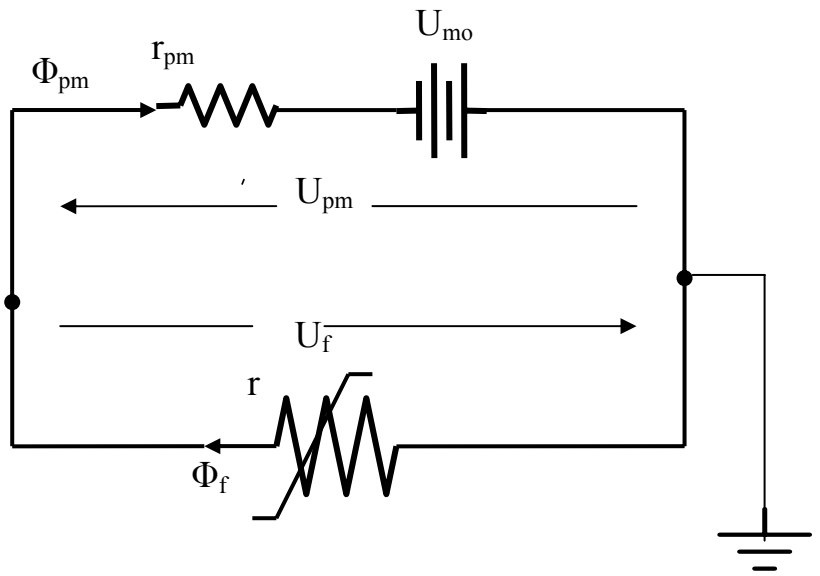



**Figure 2.10** DC circuit of the MCL

When the core is operating in saturation the same amount of flux will be passing through the core and the permanent magnet, that is $\phi_f = \phi_{pm} = \phi_{dc}$ , where $\phi_{dc}$ is the flux in the DC operation.

Now calculating $\phi_{dc}$ ,

$$r_u \phi_{knee} + r_{is}(\phi_{dc} - \phi_{knee}) - U_{mo} + \phi_{dc} r_{pm} = 0$$

$$\phi_{dc} (r_{is} + r_{pm}) = U_{mo} + (r_{is} + r_u) \phi_{knee}$$

$$\phi_{dc} = \frac{1}{r_{is} + r_{pm}} [U_{mo} + (r_{is} - r_u)\phi_{knee}] \qquad (14)$$

For core #2 the value of the dc flux is - $\phi_{dc}$

Figure 2.11 shows the characteristic $\phi_{ac}$ versus I of the MCL. The flux, $\phi_{ac}$ is obtained by subtracting the DC flux obtained from Equation (14), from the flux obtained from Equation (11), (12) and (13).The gradient S1 and S2 represent the saturation and unsaturation regions. $I_{knee}$ is the maximum value of the current in the normal operation, when the current becomes greater than the $I_{knee}$ , the gradient S2 comes into the picture and the core comes out of saturation. $I_{demag}$ is the value of the

current at which the permanent magnet becomes demagnetized and the current limiting action of MCL no longer exists. $I_{max}$ is the maximum current it can limit.

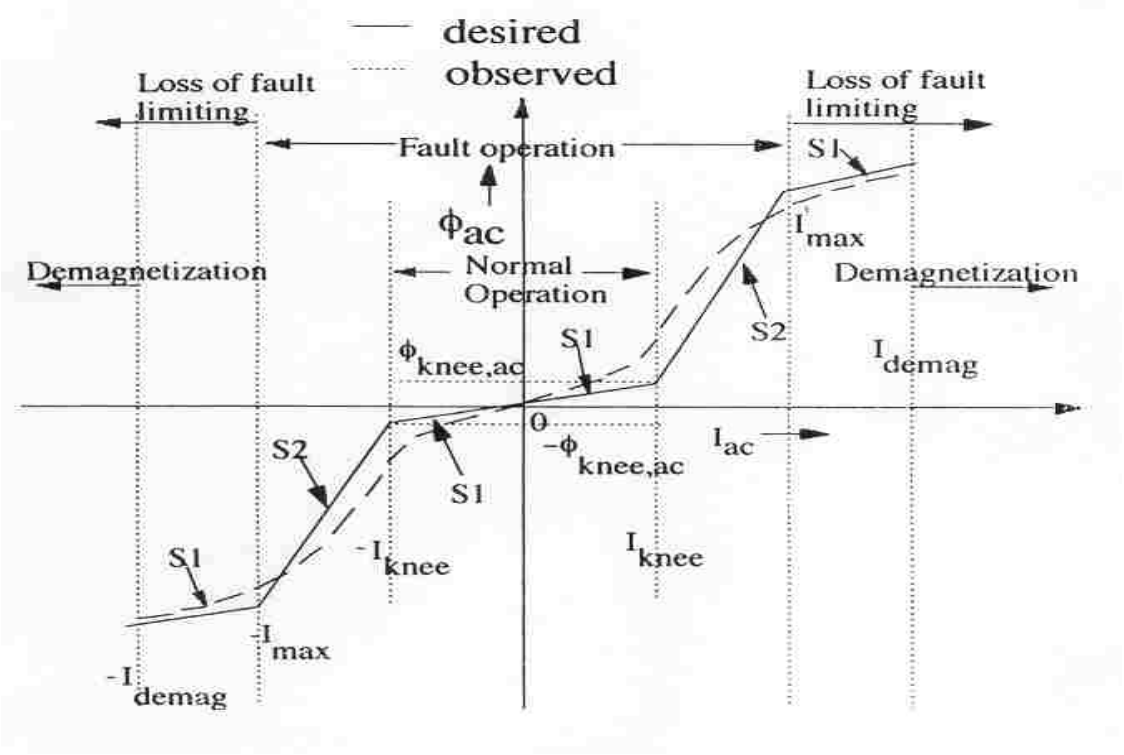



**Figure 2.11** Idealized $\phi_{ac}$ versus $I_{ac}$ characteristic

In the above Figure 2.11, the solid line shows the desired characteristics and the dashed line shows the observed characteristics. In the observed characteristics, there is a gradual change in the gradient due to non-uniform flux distribution and because of that the gradient S2 shows the fault condition. The area between $\pm$ $I_{demg}$ and $\pm$ $I_{max}$ shows gradient S1, here the current limiting action is no longer valid because the permanent core comes out of saturation under normal operation. This can be avoided by selecting a core which has low saturation flux density. The maximum current of the MCL is represented by $I_{max}$ and $I_{demg}$ is the current at which magnet becomes demagnetised. From Figure 2.11 the gradient S1 represents normal operation and the magnet gets demagnetised due to the flow of a large amount of current in the windings of the MCL.

## 2.6 Design Considerations

From the operating principle of the Magnetic Current Limiter, it can be observed that the MCL behaves as a variable inductor. The saturated inductance $L_s$ of the MCL

has a very low value during normal operation or when there is a low value of current, due to which it has a very low voltage drop across it. When there is fault the current increases to a large value which is more than a specific current ($I_{knee}$). The inductance during the fault is called unsaturated inductance. The core comes out of saturation in the alternative half cycle of current and $L_u$ has a very large value which limits the current. During fault the total inductance is equal to unsaturated inductance ($L_u$) and saturated inductance ($L_s$) of the other core, as the cores come out of saturation in alternative half cycles of current. In order to increase the effective saturated and differential unsaturated inductance of the MCL two devices in series can be placed, due to which the saturated inductance $L_s$ doubles to become equal to $2L_s$.

In order to see the effect of the different parameters on the design, Figure 2.12 shows the desirable volt-current characteristics of the Magnetic Current Limiter. It can be seen that the voltage drop during normal operation, when current has a small value, is much less and during fault when the current becomes greater than $I_{knee}$ the voltage drop increases. Here the gradients M1 and M2 are similar to gradients S1 and S2 in Figure 2.11. The only difference is that the gradients M1 and M2 represent the ratio of change of the voltage across the MCL to the change of current through the MCL and the gradients S1 and S2 are the ratio of change of flux to change of mmf.

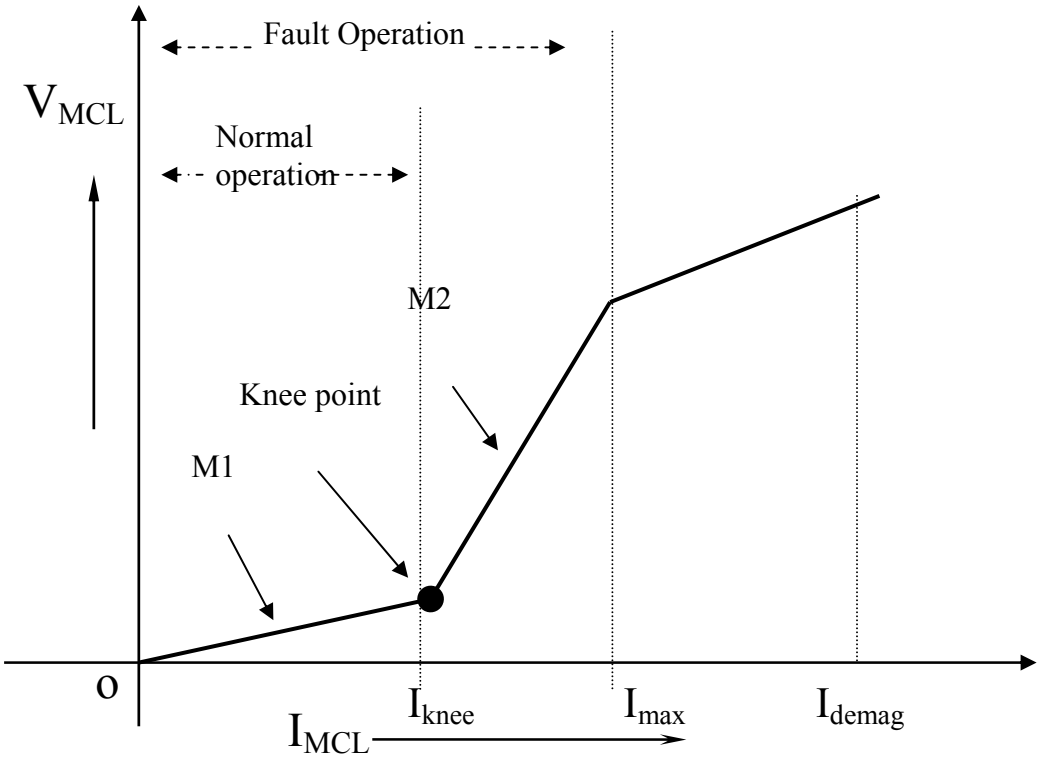



**Figure 2.12** Desire Voltage and Current Characteristics of the MCL

From the Figure 2.12 the design consideration of the MCL depends upon the following quantities:

a) Gradient, M1, during normal operation which depends on $2L_s$ as two devices in series

b) Gradient, M2, during fault and it depends on $L_u$ and $L_s$

c) Knee point current ($I_{knee}$)

d) $I_{max}$ Maximum current at or after which there is no current limiting action of MCL

e) Ratio gradients M2 to M1

f) $I_{demag}$ current above which the permanent magnet gets demagnetised

### 2.6.1 Saturated inductance, $L_s$

$$L_s = \frac{N^2}{r_{pm} + r_{is} + r_u} \tag{15}$$

$r_u$ is neglected as it is very small as compared to $r_{pm}$ and $r_{is}$ , $r_{pm}$ is also very small therefore,

$$L_s = \frac{N^2 \mu_{is} S_{core}}{l_{core}}$$

### 2.6.2 Unsaturated inductance, $L_u$

$$L_u = \frac{N^2}{r_{pm} + r_{is} + r_u}$$

In this case $r_{pm}$ is much greater than ($r_{is}$ and $r_u$), so,

$$L_u = \frac{N^2 \mu_{pm} S_{pm}}{l_{pm}} \tag{16}$$

And now taking the ratio of $L_u/L_s$

therefore,

$$\frac{L_u}{L_s} = \frac{r_{pm} + r_u + r_{is}}{r_{pm} + r_u} \tag{17}$$

it can be written as,

$$\frac{L_u}{L_s} = \left(1 + \frac{r_{is}}{r_{pm}}\right)$$

$$= \left(1 + \frac{\mu_{pm}}{\mu_{is}} * \frac{S_{pm}}{S_{core}} * \frac{l_{core}}{l_{pm}}\right) \tag{18}$$

Thus from equation (18) it can be seen that for a large value of $\frac{L_u}{L_s}$, a large ratio of $\frac{\mu_{pm}}{\mu_{is}}$, ($S_{pm}/S_{core}$) and ($l_{core}/l_{pm}$) is required.

## 2.7 Fabricated Models of Magnetic Current Limiter

Series and parallel models are fabricated. Figure 2.16 shows the series model based on ferrite core.

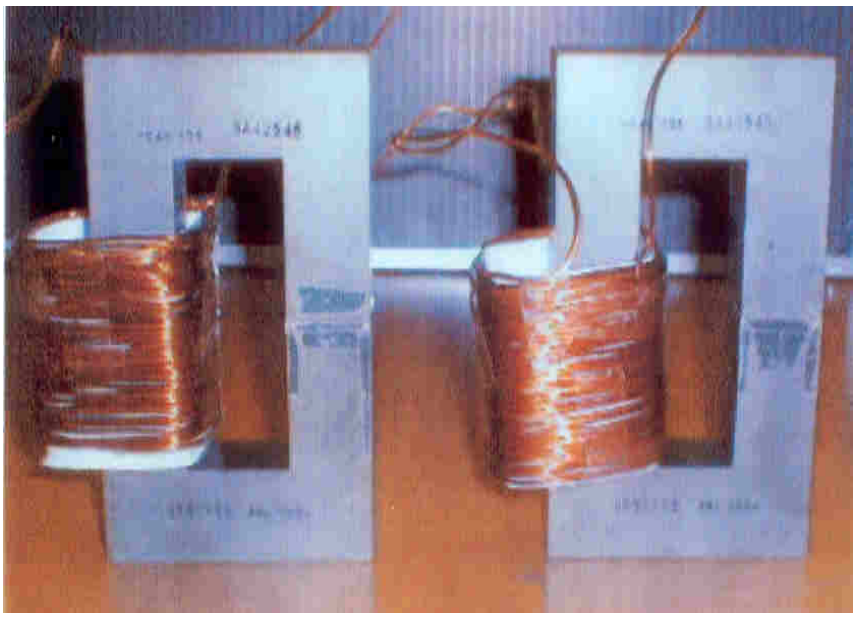


**Figure 2.16** Series fabricated model

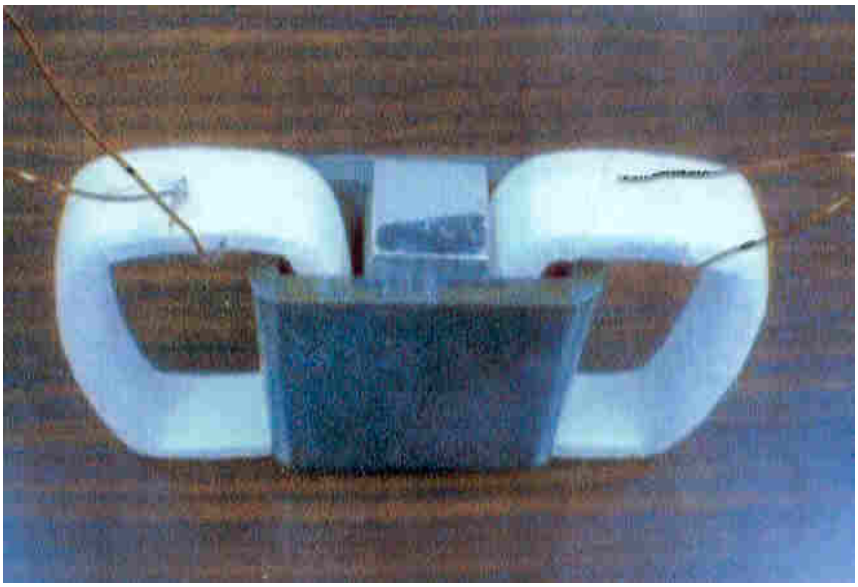


**Figure 2.17** Series based steel core fabricated model

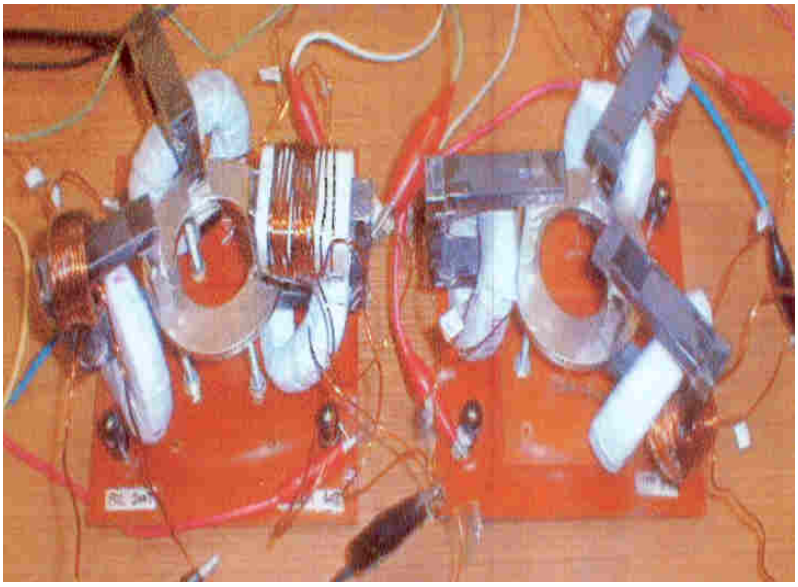


**Figure 2.18** Three phase power electronic system with MCL

## 2.8 Experimental Setup and Results

The circuits with a fault current limiter are shown in Figures 2.19 and 2.20. Figure 2.19 shows the single phase power electronic circuit with Magnetic Current Limiter and Figure 2.20 shows the three phase power electronic circuit with Magnetic Current Limiter. The MCL is installed near the power supply. During fault the voltage and the current behaviour is observed.

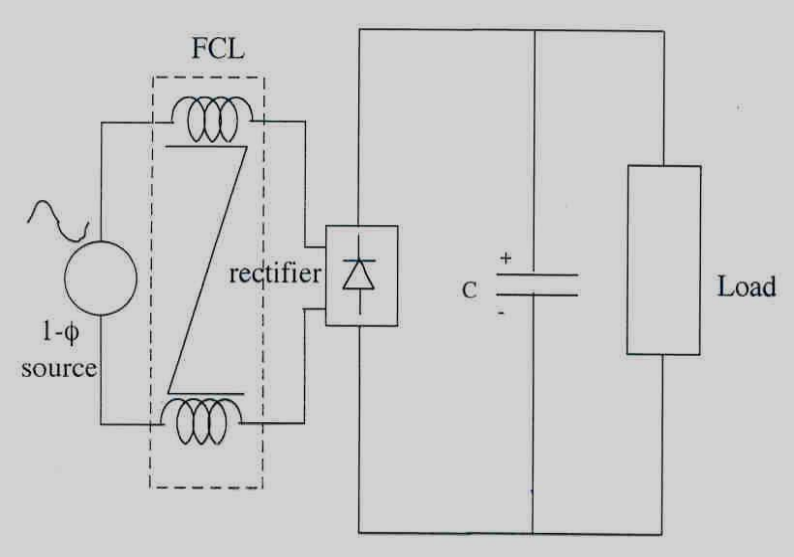



**Figure 2.19** Single Phase Power electronic circuit with MCL

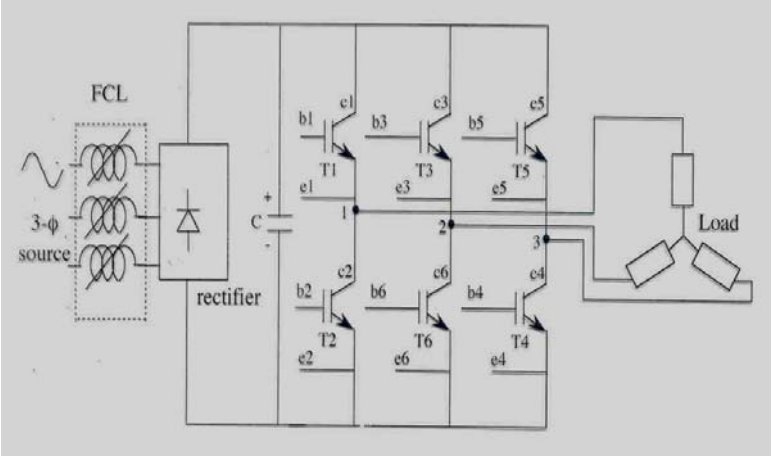



**Figure 2.20** Three Phase Power Electronic Circuit with MCL

The results showing current and voltage wave forms after and before the fault have all been observed. To show the advantage of having MCL in the system, wave form with and without MCL are shown. Figure 2.21 shows the current waveforms with and without MCL. In this figure the variation of voltage across the capacitor is also shown. It is observed that the voltage $V_{cap}$, development across the capacitor is considerably reduced with the MCL in the circuit. It can be seen in Figure 2.21 that peak (negative) current on fault reaches to 95A without MCL and it is limited to 55A with MCL, which is less than 200% of nominal peak current. Time taken by the MCL after fault is about a fraction of a second. As it is a passive device and it depends on

the magnetic properties (flux linkage), it switches to fault mode in a fraction of a second.

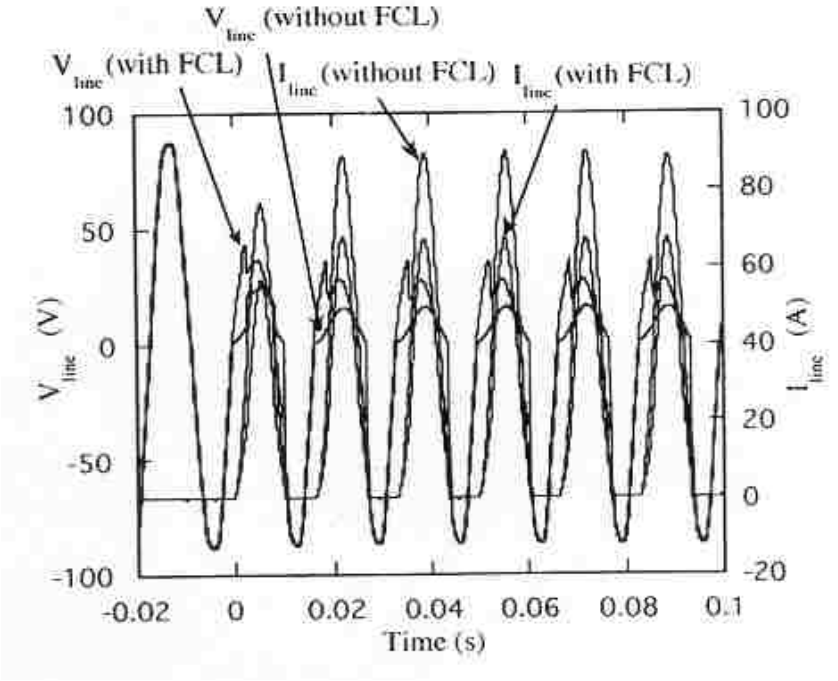



**Figure 2.21** Current Waveforms with and without MCL

Figure 2.22 shows current and voltage waveforms under shorted diode condition. It has been observed that the peak fault current is considerably reduced with the implementation of MCL in the circuit as compared to the fault current without MCL and the time taken to limit current is very small.

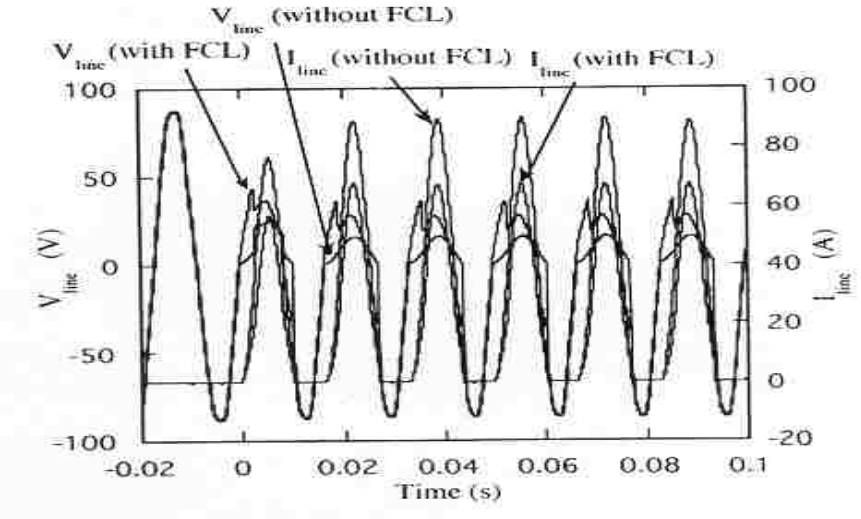



**Figure 2.22** Current and voltage waveforms under shorted diode

From the above figure it has been observed that a fraction of a second is taken to limit the faulty current. During the short circuit diode the current goes to a high value

(95A) without any current limiting device in the circuit. It has been observed that with MCL in the circuit the fault current is limited to 60A, which is desirable in order save the system components from damage.

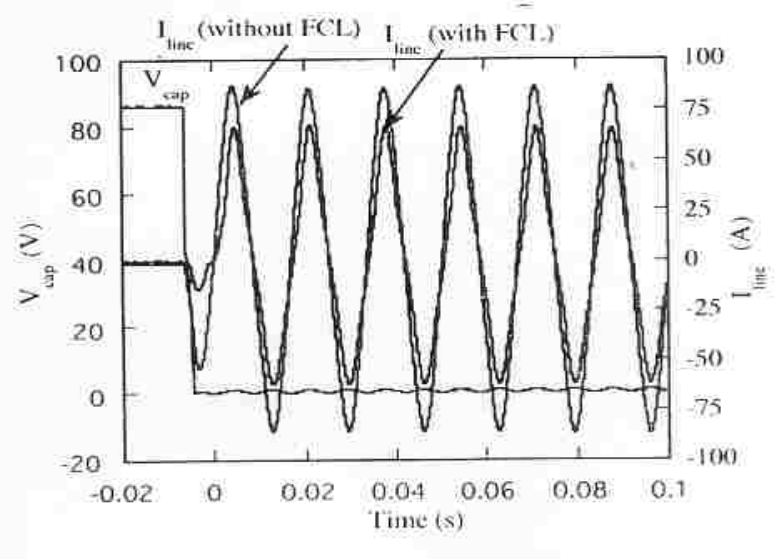



**Figure 2.23** Current Waveforms during Shorted diode output condition

The results with three phase MCL under normal operation are shown in Figure 2.24, which shows the current and voltage in the u phase.

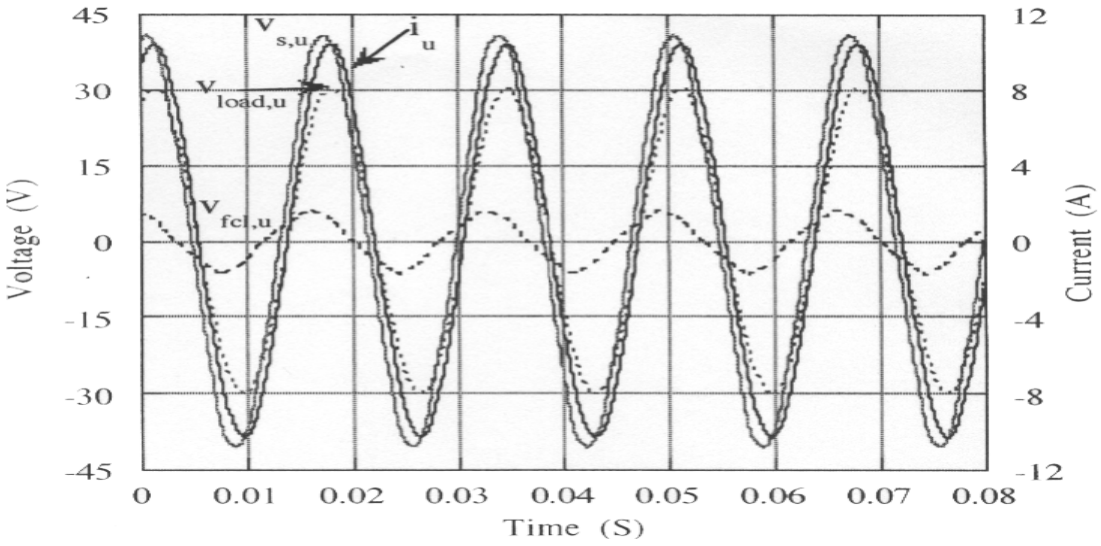



**Figure 2.24** Current and voltage waveform in the u-phase of 3-phase MCL under normal operation

The currents in the u-phase are shown in Figure 2.24, which shows the normal operation of the system.

The switch across the load is closed to initiate the fault in the circuit and the current and voltage waveform during three phase fault is shown in Figure 2.25. The

current in all the three phases w, v and u during fault is shown in Figure 2.25. The uneven value of the fault current is the three phases is observed, this may be due to unbalance of the three phases.

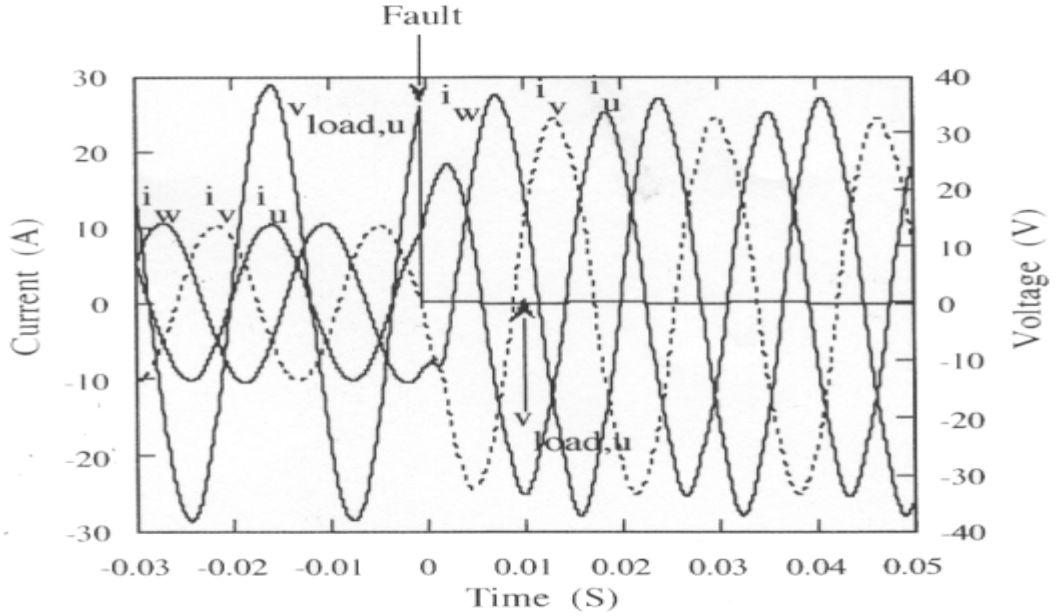



**Figure 2.25** Results during three phase fault condition

The single line to ground fault has been applied and the results are shown in Figure 2.26.

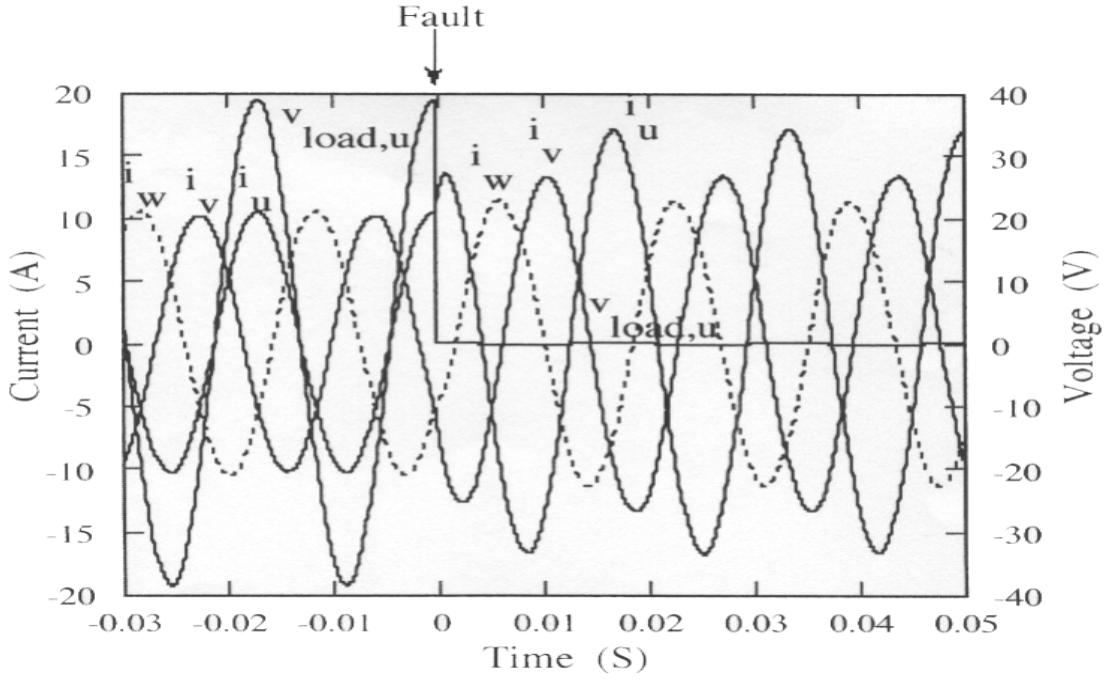



**Figure 2.26** Current and voltage waveforms for S-L-G fault condition

## 2.9 Conclusion

The operating principal, characteristics, design consideration and experimental results of the Magnetic Current Limiter have been explained in this chapter. Basically it has two modes of operation, one is the normal mode and the other is during fault. During normal operation it offers low impedance due to which it has a very low voltage drop across it. From the experimental results it has been observed that the time taken by the MCL to perform its operation is much less and the MCL does not require any external source to perform its operation. From the characteristic of the Magnetic Current Limiter (Figure 2.11) it has been observed that there is constant change in the gradient of the observed line due to which the core comes out of saturation during normal operation. In order to see the functioning and behaviour of the flux inside the MCL, during operation the field and thermal models are studied in the next chapter.

# Chapter 3
# Field and Thermal Model
# of
# Magnetic Current Limiter

## 3.1 Introduction

It is important to know the flux distribution inside the core of the Magnetic Current Limiter under normal and fault condition. Since the operation of the Magnetic Current Limiter is entirely dependent on the flux state of the magnetic core, knowledge of magnetic field distribution inside the core is very much necessary. In this chapter the field analysis of the Magnetic Current Limiter has been carried out using finite element modelling software. The finite element software FEMLAB by COMSOL Inc. has been used to model and analyse the field distribution inside the MCL. COMSOL Multiphysics™ is an engineering tool that performs equation-based multiphysics modeling in an interactive environment. COMSOL Multiphysics makes modeling and simulating physics phenomena very easy.

## 3.2 Model Formulation in the FEMLAB

The Figure 3.1 shows the Model Navigator, which is the window that appears when we start a new modeling session in FEMLAB, COMSOL. The 2-D model of the Magnetic Current Limiter has been made in the FEMLAB. In Figure 3.1 the space dimension is used to select the model type, like 1-D, 2-D or 3-D. Using the symmetry of the problem the 2-D model has been used to get a fast analysis. By using solid modeling or boundary modeling the 2-D model of the MCL has been drawn. The thermal model has also been developed to observe the affect of temperature on the operation of Magnetic Current Limiter. Depending on the magnitude of the current, the limiter offers a saturated inductance ($L_s$) or an unsaturated inductance ($L_u$). The eddy currents are also generated, both in permanent magnet and ferrite core because there is fluctuation of flux due to alternating current in the coil.

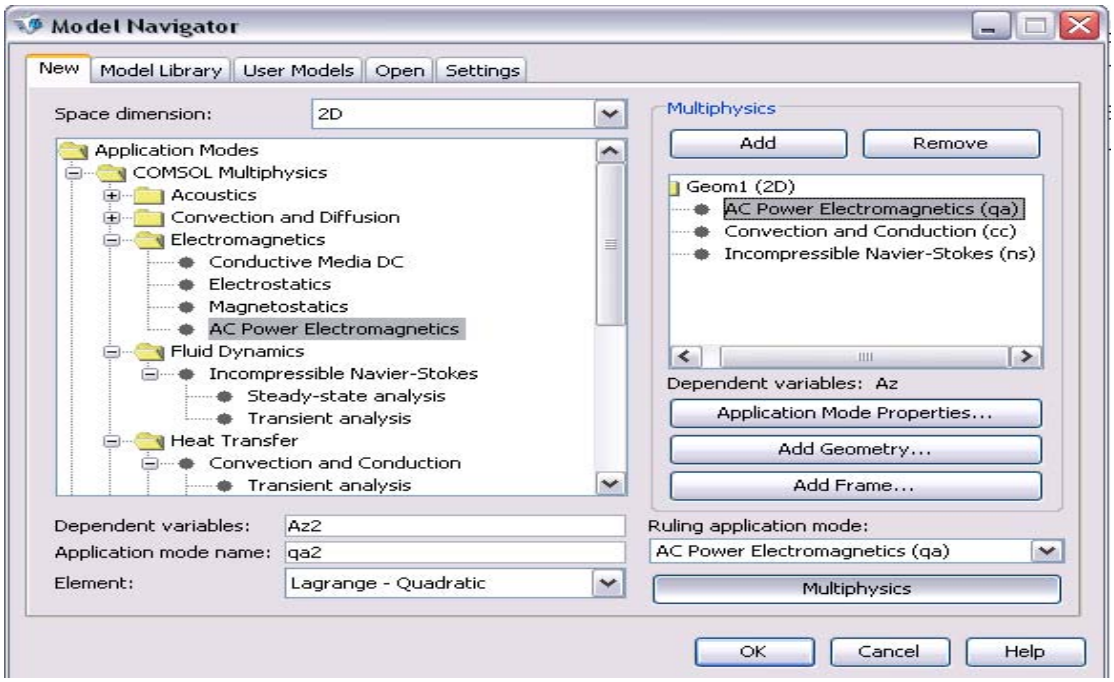



**Figure 3.1** Model Navigator window of FEMLAB software

The Figure 3.2 shows the 2-D model of the MCL.

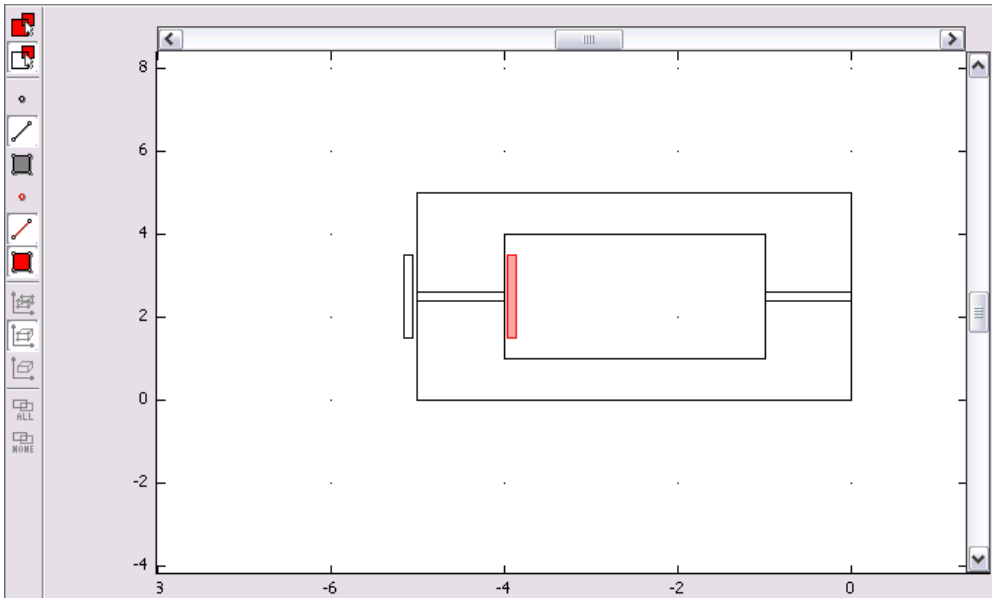



**Figure 3.2** 2-D Geometry of the Magnetic Current Limiter

The eddy currents are neglected in the core, due to high resistivity of the ferrite core. The flux distribution at different current value is investigated. The change in the temperature associated with the change in the current value is observed and the results are reported.

To obtain the field and thermal modelling of the magnetic current limiter three application modes are used in FEMLAB namely AC Power Electromagnetics, Incompressible Navier-Stokes and Convection and Conduction. The right top corner of Figure 3.1 shows the above three modes of application selected for 2-D model of the MCL.

The AC Electromagnetic mode of FEMLAB performs and specifies the material dependent interactions between fundamental physical quantities. Many physical quantities are fundamental to electromagnetics. They are current density, ***J***; Magnetic Flux density, ***B***; Electrical field intensity, ***E***; Electrical displacement, ***D***; Magnetic field intensity, ***H***; and electric charge density, $\rho$. The values of theses quantities are defined in the sub domain setting window (Figure3.4). In this mode the electrical and magnetic behaviour of the model is performed. The model in the FEMLAB has eight sub domain selections and for each domain magnetic and electrical parameter are defined. The boundary conditions, taken together with Maxwell's equations and constitutive relations are used to describe the field distribution. The Figure 3.3 shows the window for boundary settings.

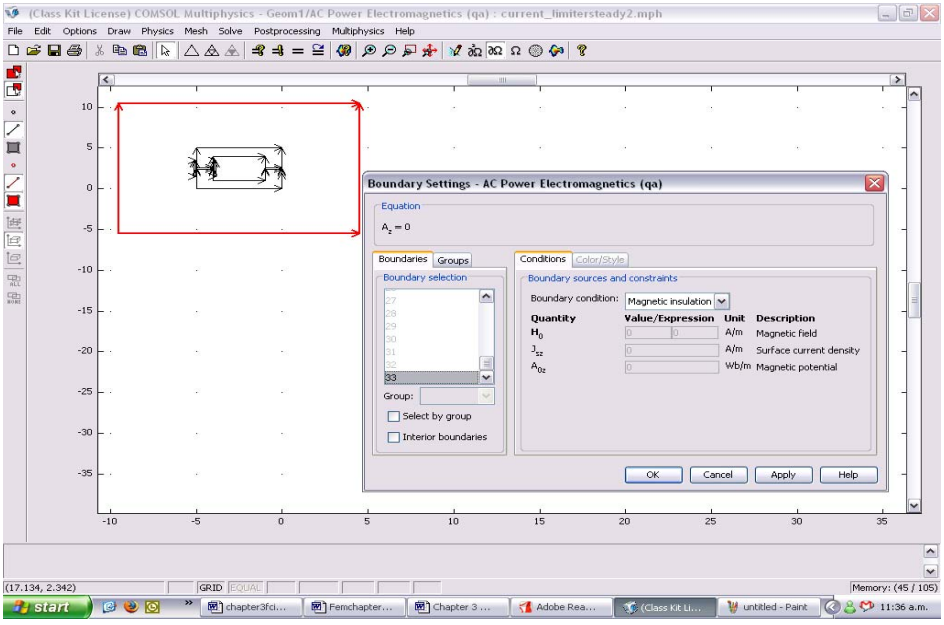



**Figure 3.3** Window for boundary setting of the field model

In the Convection and Conduction mode of the FEMLAB the heat generated and transfer due to alternating current in the coil and eddy currents in the ferrite core and PM assembly is calculated and analysed (thermal modelling).

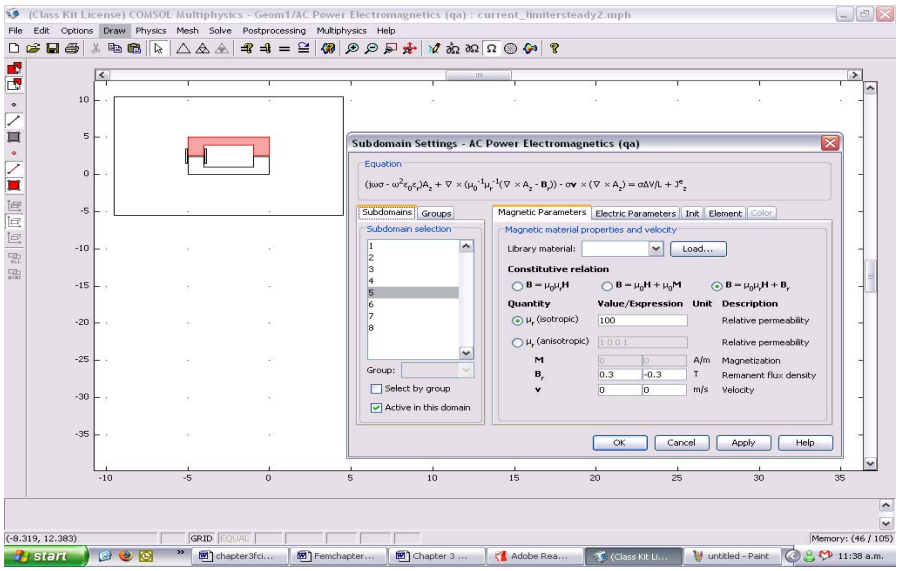



**Figure 3.4** Window for sub domain setting of the thermal model

In order to see the behaviour of the flow and movement of the particles in the medium the Incompressible Navier-Stokes mode is applied. It describes the flow of the heat and flux in the medium around the model. The Figure 3.5 shows the values of the constants used. The first row shows the value of the current, the current value can be changed to observe the effect on the flux distribution and thermal modelling of the MCL corresponding to different values of current. The T0 is the initial temperature of the MCL. The diameter of the MCL is taken as 0.009 m.

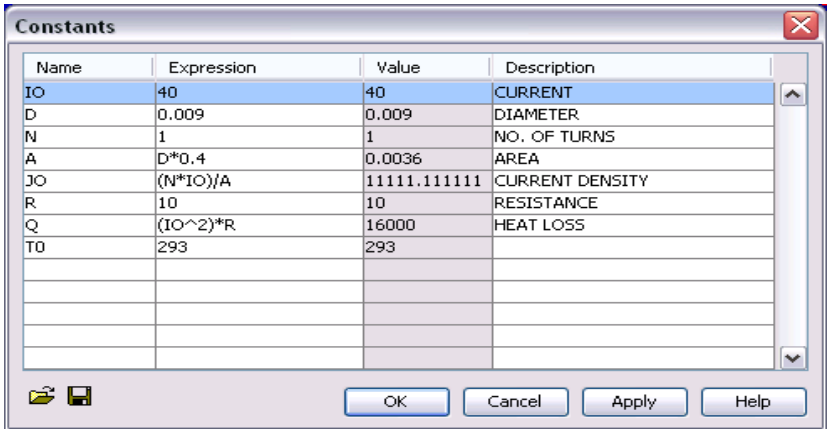



**Figure 3.5** Window for constants

## 3.3 Normal mesh of Magnetic Current Limiter

The Figure 3.6 shows the normal mesh configuration of the MCL. The window for selecting parameters for the mesh configuration is shown in Figure 3.7

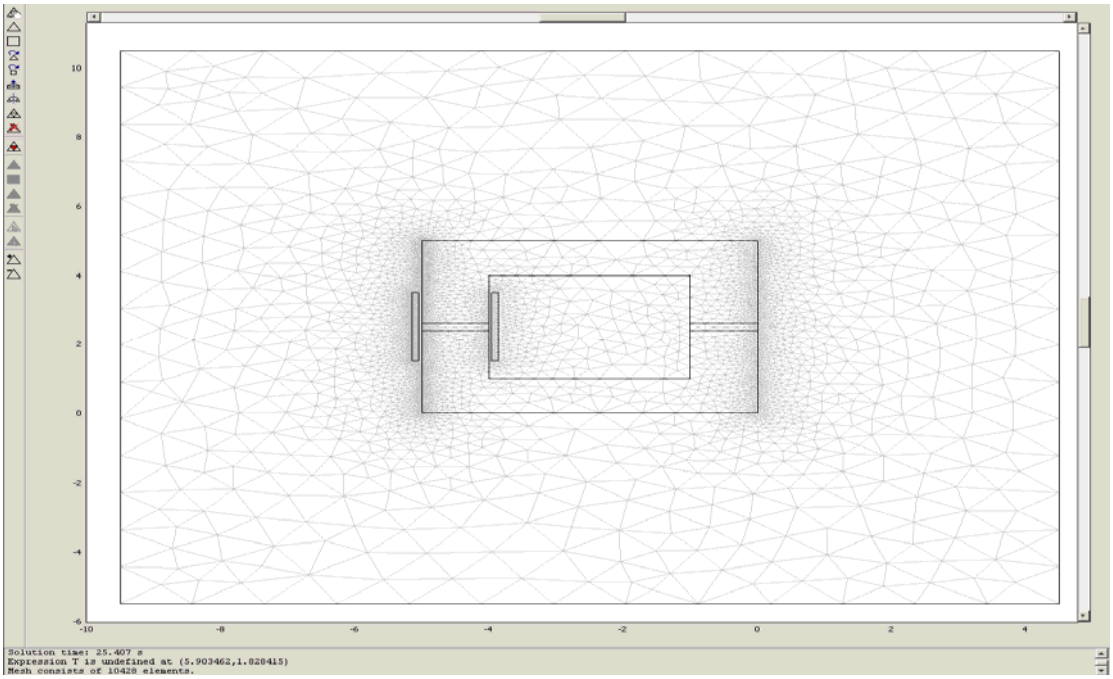


**Figure: 3.6** Normal Mesh Size of the MCL

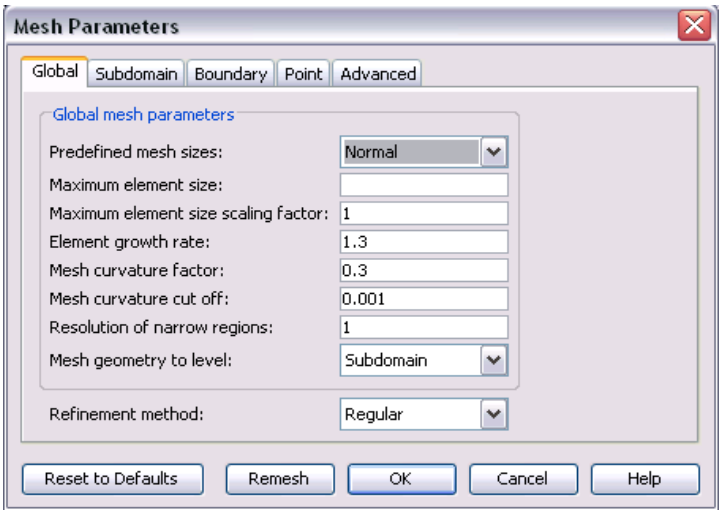



**Figure 3.7** Window for Mesh Parameters

In order to have normal mesh of the MCL the predefined mesh size is changed to the normal in the Mesh Parameter window.

## 3.4 Field Distribution in the MCL

The field models at different current levels have been developed in FEMLAB to investigate the situation of a limiter under normal and fault operation. The variation of the flux can be seen at different current values. In Figure 3.8 the flux distribution in

the MCL can be seen with no current in the coil. The flux in this Figure is mainly due to the permanent magnet and the magnitude of flux density inside the core is quite large compared to the saturation flux density of the core. So almost the whole core is in saturation and the value of the impedance is very low. It can be seen there are an appreciable number of flux lines outside the core (in air). Since the core is at saturation the magnetic reluctance offered by the core is also large and a significant number of flux lines pass through air.

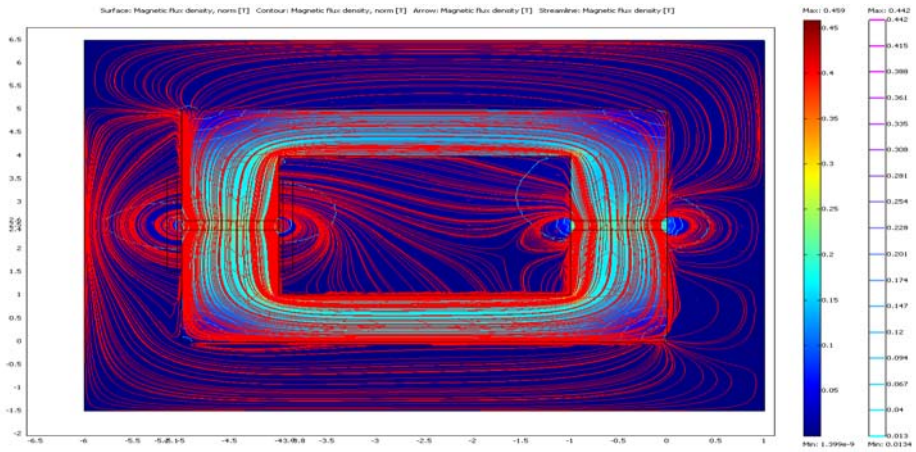


**Figure 3.8** Flux distribution of MCL with no current in windings

When the current in the coil is increased to 10A in the positive half of current the magnetic flux density increases and due to increase in the magnetic flux density the core remains in saturation as is shown in Figure 3.9 and the value of saturated inductance ($L_S$) is very low.

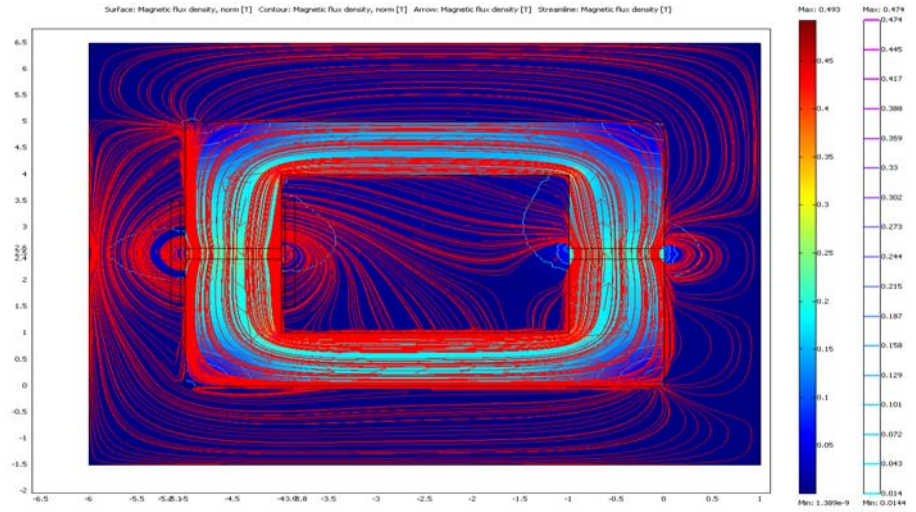


**Figure 3.9** Flux distribution of MCL with low current corresponding to positive half cycle of current

The Figure 3.9 shows the flux line distribution around the model. In this model the total magneto motive force is a result of the permanent magnet and current in the winding. From Figure 3.9 it is seen that magnetic flux density has increased. This is because the mmf due to permanent magnet and current in coil is in the same direction. This makes the magneto motive force additive so the magnetic flux density increases and the core remain in saturation. Now if we increase the current in the coil to a high value the magnetic flux again increase.

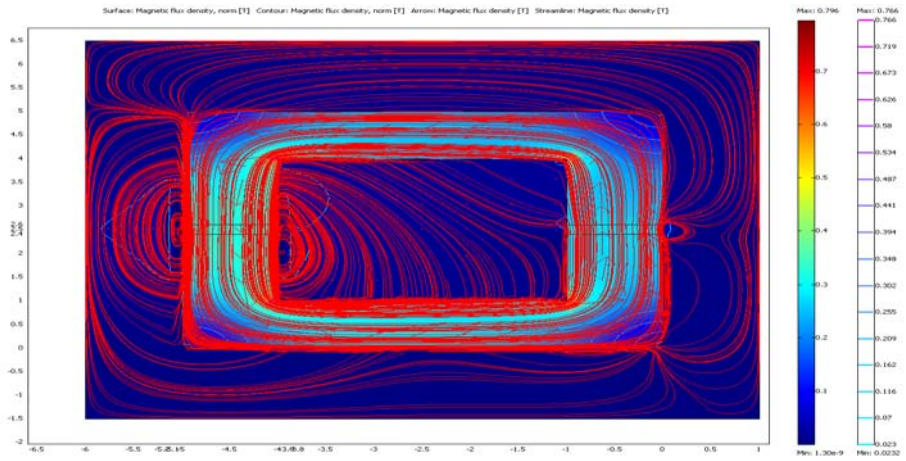


**Figure 3.10** Model of MCL with large current corresponding to positive half cycle of current

The finite element model corresponding to negative current half is shown in Figure 3.11. Under normal operation the value of the current is low and due to which the decrease in the flux density is very low. The high flux due to permanent magnet forces the core to operate in saturation.

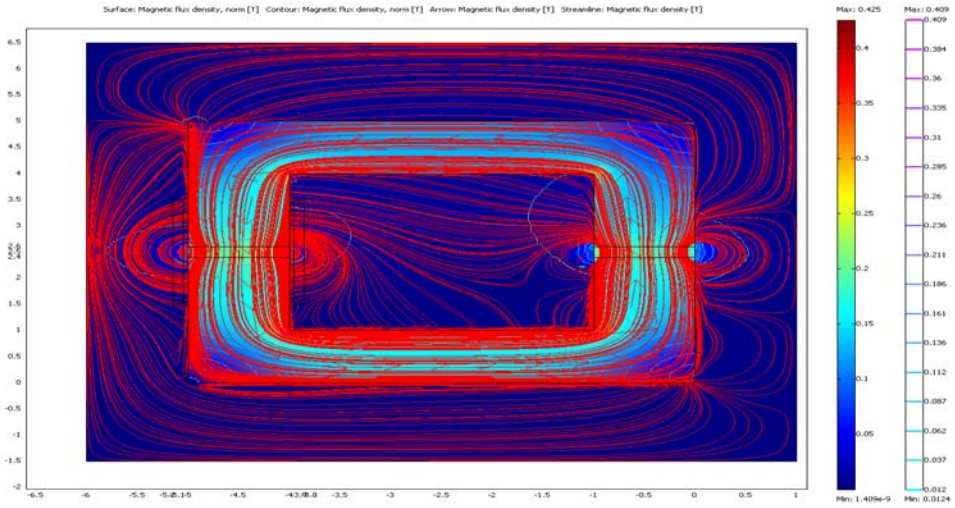


**Figure 3.11** Model of MCL with low current corresponding to negative half cycle of current

The MCL has been modelled in Figure 3.12 with a large current corresponding to the negative half of current. This simulates a fault in the system due to which the mmf corresponding to the fault current is increased. Figure 3.12 shows the flux distribution in the core during fault. It can be seen that magnetic flux density in the core is decreased and therefore the core comes out of saturation. So during fault the cores come out of saturation in the alternative half cycle of current. This means the effective impedance of the MCL is increased, which restricts the flow of fault current to a lower value in the circuit that has the Magnetic Current Limiter. The reason for the increase in the impedance of the MCL is that the mmf due to fault current is higher and in opposition to the mmf due to permanent magnet, which results in the increase of inductance of the cores. The current during fault should be restricted so that the mmf due to fault current does not exceed the mmf of the permanent magnet as this will lead to demagnetisation of the permanent magnet.

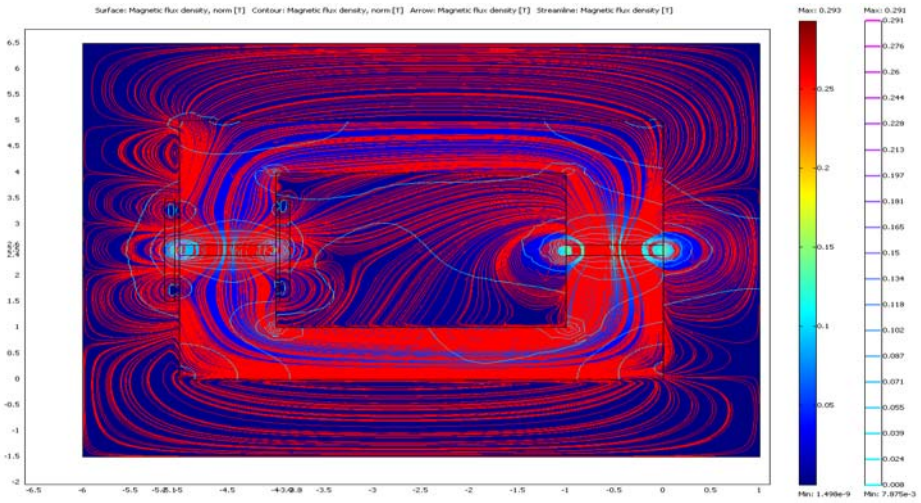


**Figure 3.12** MCL with high negative current during fault

From the field distribution models it can be observed that during fault the cores come out of the saturation in the alternative half cycle of current. It can be observed with increase in current corresponding to the positive half cycle the magnetic flux density increases and keeps the core to remain in saturation. During the negative half cycle of current the increase in current results in a decrease in the flux density and when current increases beyond a specific value the core comes out of saturation and the effective impedance of the MCL increases which limits the flow of fault current. The table 3.1 shows the change in value of magnetic flux density with respect to current.

**Table 3.1** Variation of Magnetic flux density (T) with current (A)

| Serial No. | Current (A) | Magnetic Flux Density(T) |
|---|---|---|
| 1 | 0.0 | 0.459 |
| 2 | 10 | 0.493 |
| 3 | 40 | 0.796 |
| 4 | -8 | 0.425 |
| 5 | -50 | 0.278 |

## 3.5 Thermal modelling of the Magnetic Current Limiter

Along with the increase in current there is a rise in the temperature of the MCL. This is shown in the thermal model of the MCL. The temperature is observed at different current levels to show that the temperature of the MCL increases with the rise in the current. The finite element modelling software FEMLAB is used to see the effect of the rise in temperature of the MCL during fault and normal operation.

### 3.5.1 Thermal modelling at different current levels using FEMLAB

At different current levels the changes in the temperature are observed. The results obtained are presented below. When a low current about 5A is passed through the MCL there is a small change in the temperature. The figure 3.13 shows the MCL model in FEMLAB which describes the effect on the temperature at 5A. The ambient temperature has been assumed to be 297$^{o}$K.

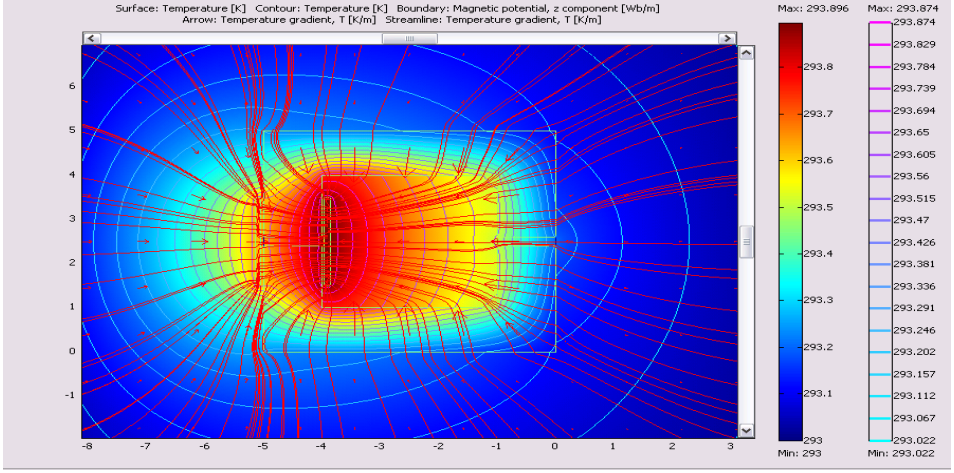



**Figure 3.13** MCL Model in FEMLAB at 5A

From the above Figure 3.13 it can be observer that there is a little increase in the temperature at a current of 5A.

Figure 3.14 shows the model when the value of current is increased to 10A and the rise in temperature is also observed.

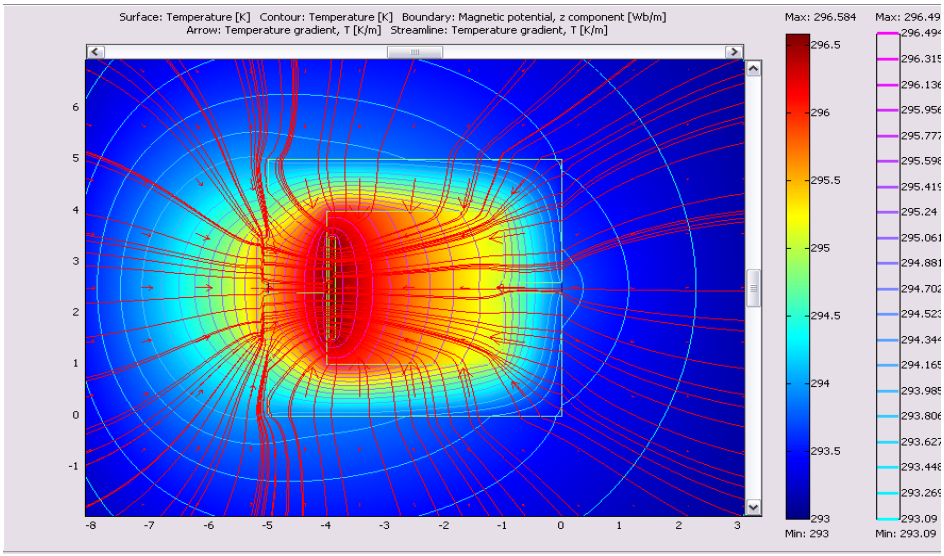



**Figure 3.14** Thermal model of MCL at 10A

When a current of 10A is applied to the windings there is increase in the temperature of the MCL. The temperature increases to 296.584 K from a value of 293.896K when current in the winding was 5A. When the current in the winding is increased to 20A there is further increase in the temperature is observed. Figure 3.15 shows the model in FEMLAB with 20A current in the winding.

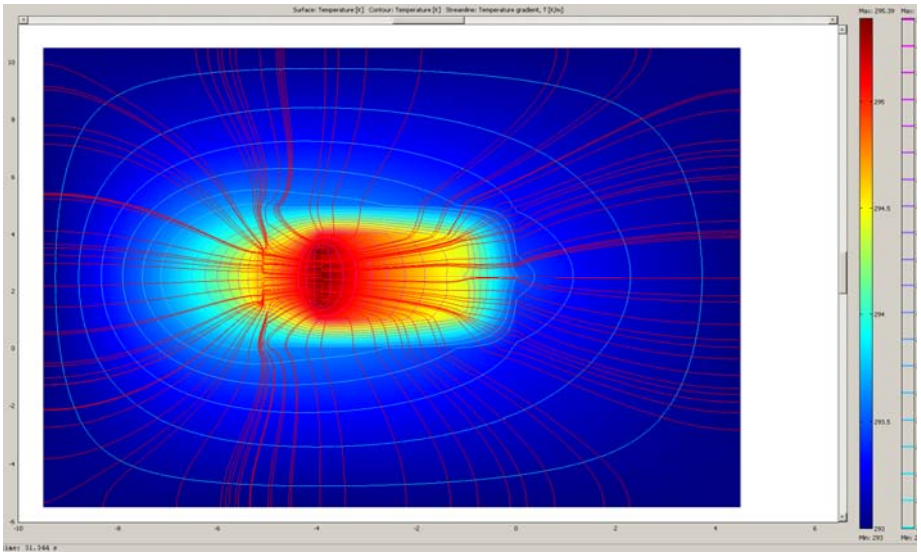


**Figure 3.15** MCL at current 20 A

The temperature increases to 296.789K which is greater than the temperature when the current in the windings was 10A. From the above Figure 3.15 it can be observed, the area around the winding is heated more than the other part of the MCL. Figure 3.16 shows the MCL model when the current applied to the winding is increased to 30A and it can be observed that there is further increase in the temperature mainly near the current winding of the MCL. Figure3.17 shows the MCL model when the current in the winding is 40A. The temperature of the model increases to 302.559K which is greater than the temperature when current in the winding was 20A. Increasing the current to 80A there is a further increase in the temperature. Figure 3.21 shows the MCL with the current at 80A, the increase in temperature is quite significant here compared to the rise in temperature when the current is increase from 40A to 60A. Figures 3.16 to 3.23 show the thermal models of the MCL in FEMLAB with current increase from 30A to100A with 10A increments.

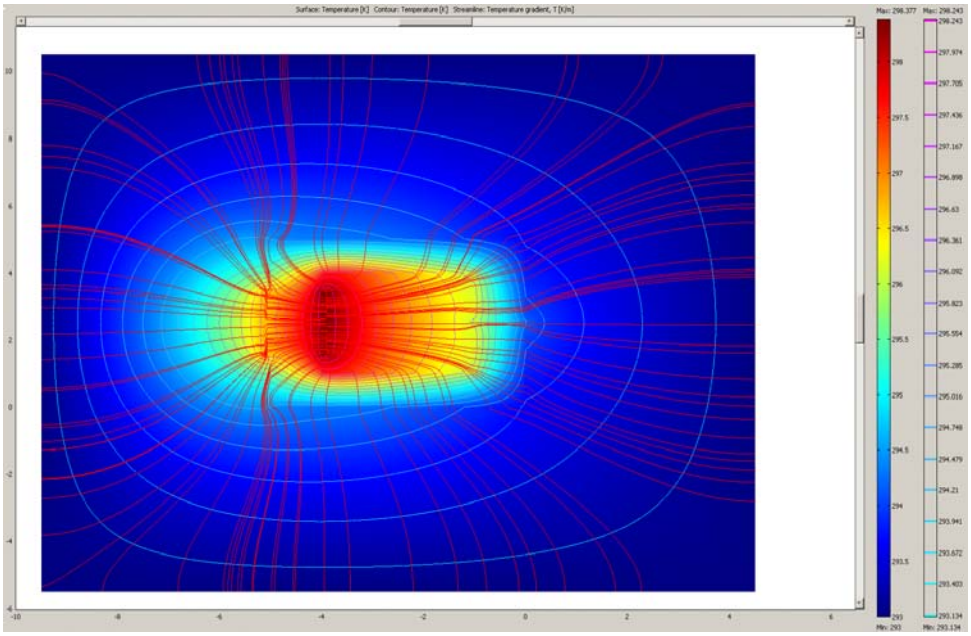


**Figure 3.16** MCL at current 30A

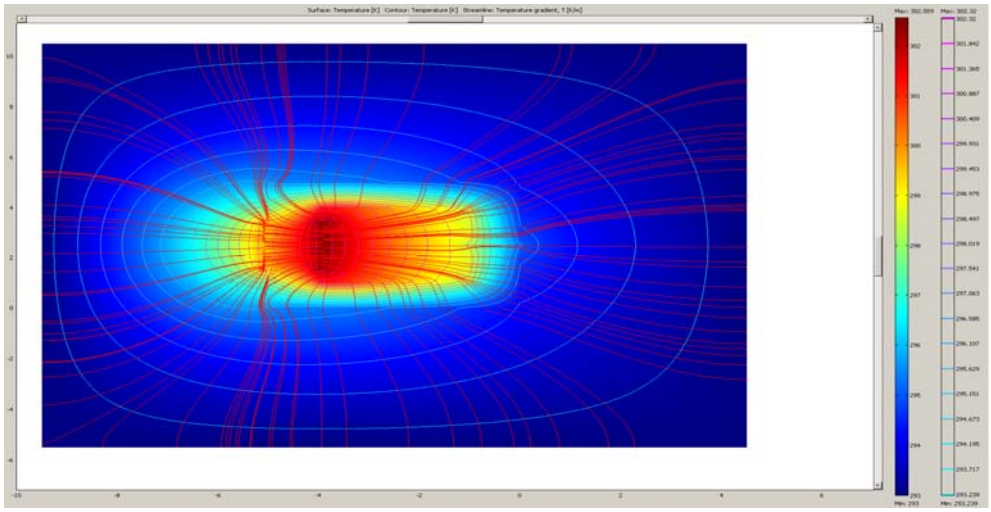


**Figure 3.17** MCL at 40A

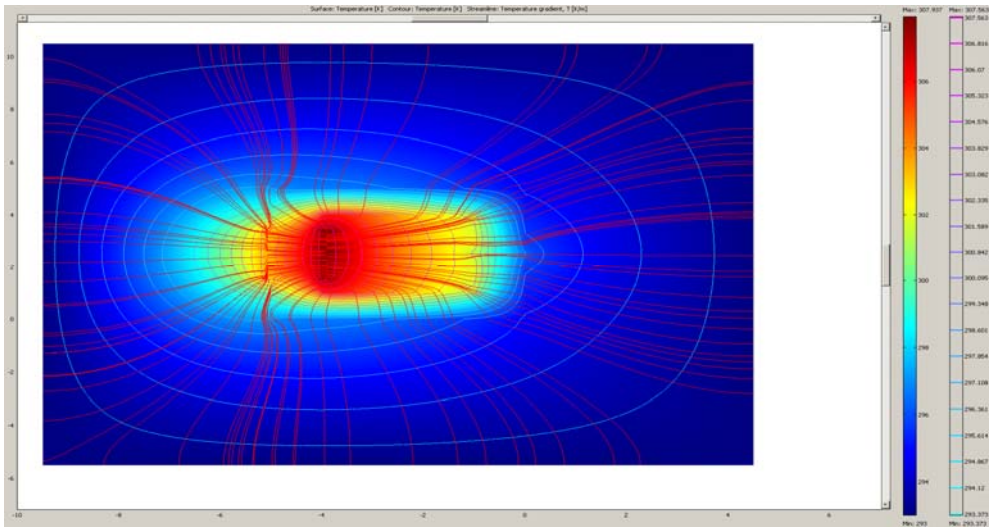


**Figure 3.18** MCL at 50A

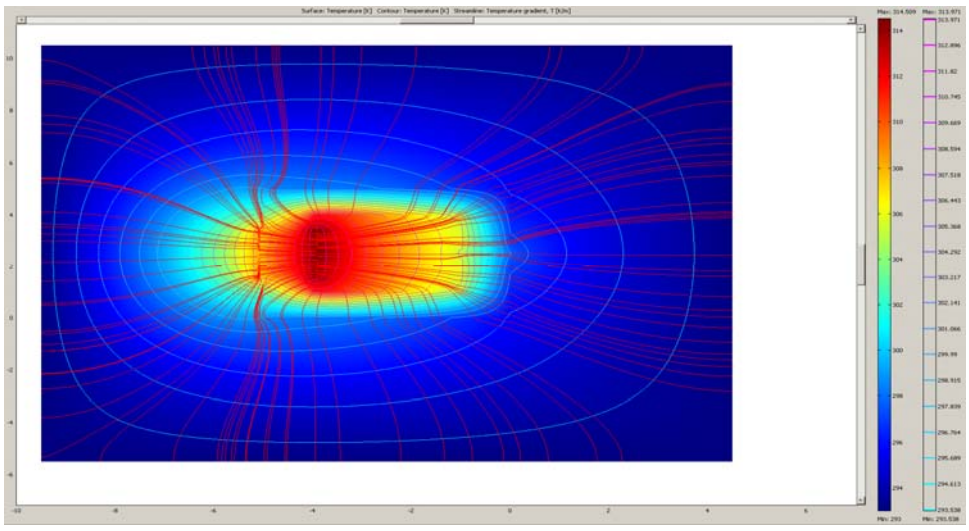


**Figure 3.19** MCL at 60A

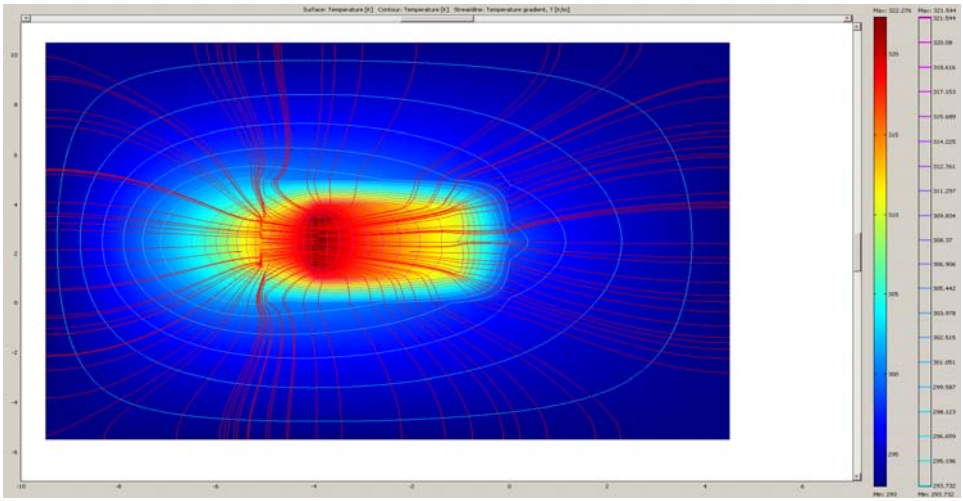


**Figure 3.20** MCL at 70A

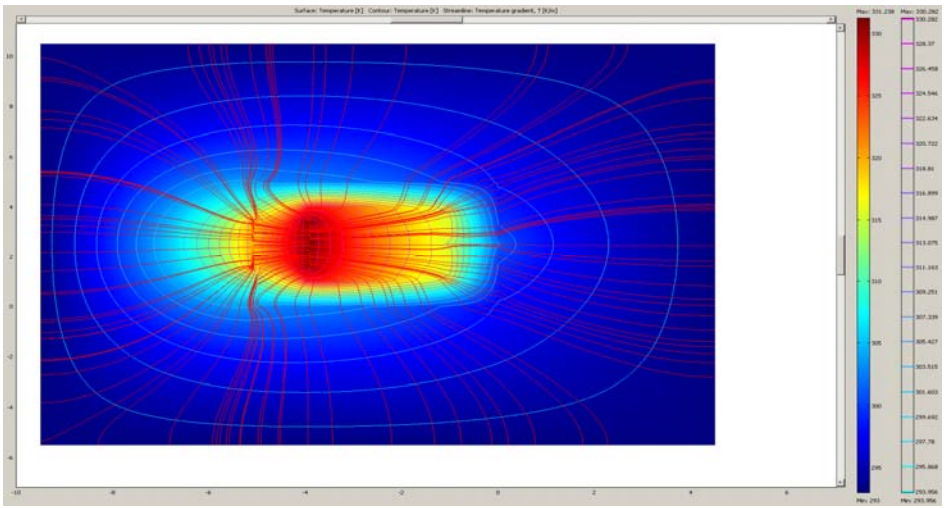


**Figure 3.21** MCL at 80A

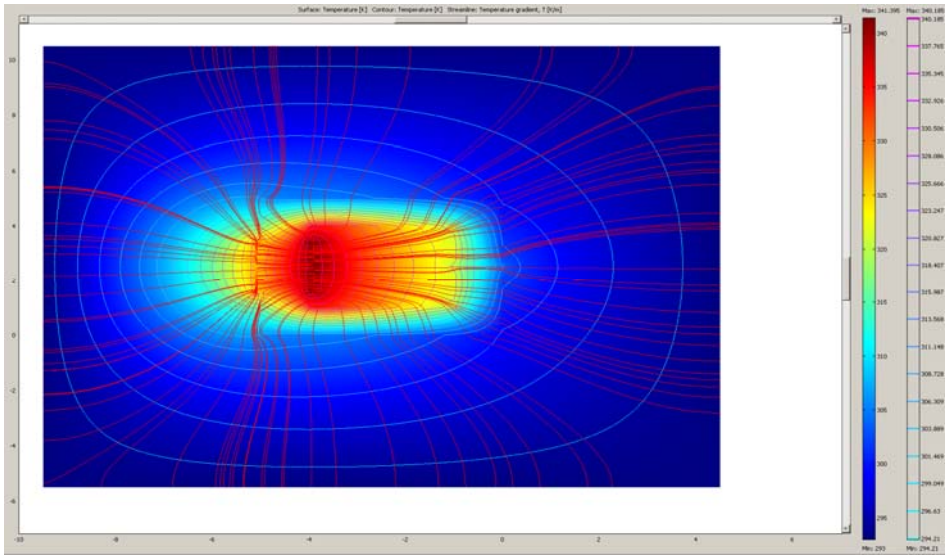


**Figure 3.22** MCL at 90A

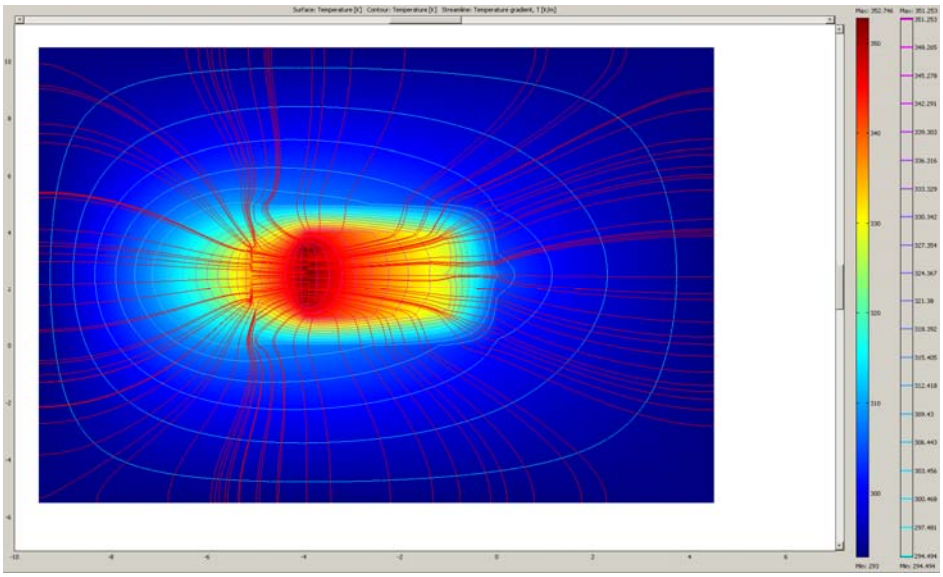


**Figure 3.23** MCL at 100A

On increasing the current to 100A, there is quite rise in temperature. The thermal modelling is important in design and rating of the MCL. For normal operation it is important to know the steady state temperature increase. The temperature rise should not be too high during normal operation. However during fault condition the current is very high and it is important to know the temperature rise.

Table 3.2 shows the change in the value of temperature with respect to current. Different values of current are applied and corresponding change in the temperature is observed (Figure 3.24). It is observed, under the normal operation of the MCL, when the current is low there is a little change in the temperature it remains almost constant up to current of 20A. Therefore this MCL is suitable for a normal current of around 20 A. Figure 3.24 shows the variation of temperature rise as a function of steady state current.

**Table 3.2** Variation of temperature (K) with current

| Serial No. | Current (A) | Temperature (K) |
|---|---|---|
| 1. | 5.0 | 293.19 |
| 2. | 10 | 293.59 |
| 3. | 20 | 295.39 |
| 4. | 30 | 298.37 |
| 5. | 40 | 302.55 |
| 6. | 50 | 307.93 |
| 7. | 60 | 314.51 |
| 8. | 70 | 322.27 |
| 9. | 80 | 331.24 |
| 10. | 90 | 341.40 |
| 11. | 100 | 352.75 |

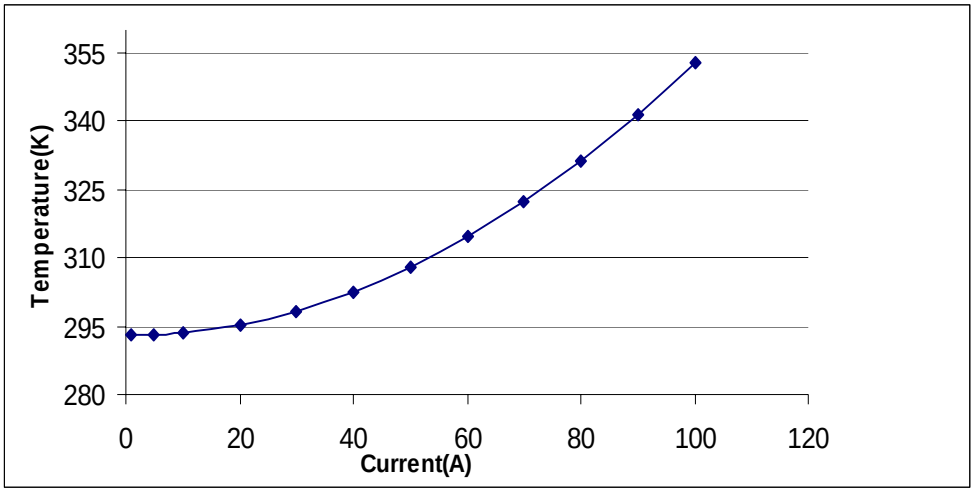



**Figure 3.24** Change in temperature with respect to current

## 3.6 Transient Thermal Model

From above it is observed that with the increase in current in the windings of the MCL there is also increase in the temperature. The thermal modelling of the MCL helps in selecting the design parameters and rating of the model in order to avoid thermal run away. Figure 3.25 shows the variation of temperature with time (transient).Here the temperatures is in Kelvin (K) and time in seconds. From Figure 3.25 it is observed that the increase in the temperature is linear with respect to time. After some time the temperature reaches a steady value and becomes constant. Transient response helps the designer in selecting the design parameters to give a high output, independent of the temperature rise in the MCL.

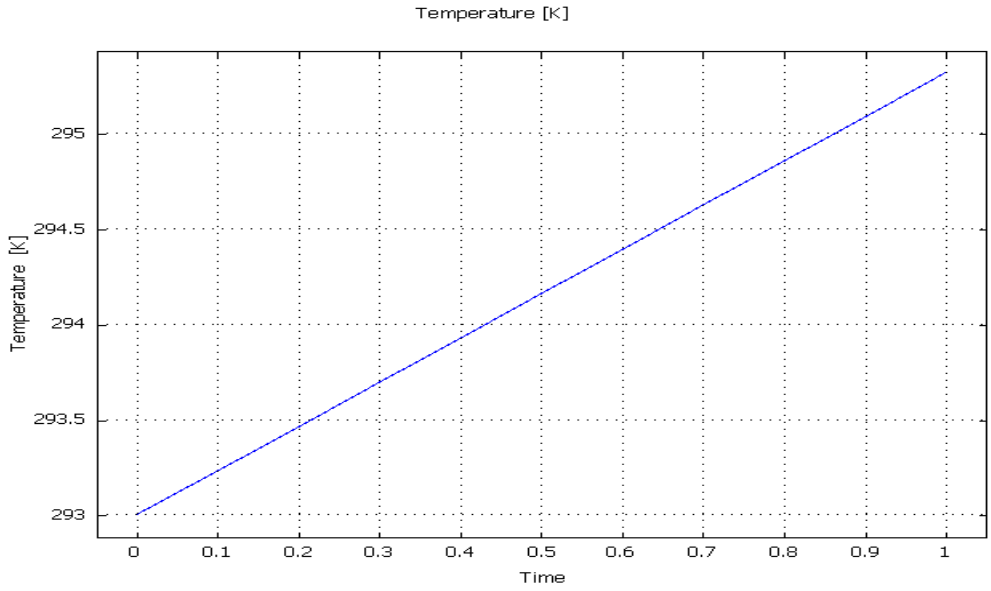



**Figure: 3.25** Transient Response of the MCL

## 3.7 Conclusions

Finite element modelling in FEMLAB has been investigated in this chapter. The results show that the core remains in saturation under normal operation as the flux during normal operation is due to the permanent magnet and inductance corresponding to saturation is $L_{s.}$ During fault the current in the coil and the mmf due to current both increase. The mmf due to fault current is opposite to the mmf due to permanent magnet. This causes the cores to come out of saturation in alternate half cycles of supply current and the effective inductance (equal to $L_s$ plus $L_u$) of the core increases due to which current is limited. Cores with a low saturation flux density and

a very low value of saturated magnetic permeability are used which will keep the core in saturation during normal operation of the MCL. Thermal modelling has also been described in this chapter. It is observed that the temperature is low during normal operation but under fault operation the temperature increases considerably.

# Chapter 4
# High Temperature Superconductor Fault Current Limiter Operating Principle and Results

## 4.1 Introduction

High Temperature Superconductor Fault Current Limiters (HTSFCL) use the unique relationship between the resistance and temperature in superconductors to limit potentially damaging short circuit currents after a fault has occurred. Superconductor materials like Bi-2222, Bi2223 and YBCO are perfect conductors of electricity, having zero resistance when they are cooled below critical temperature. The so called high temperature superconductor FCL is becoming increasingly prevalent due to the advantages of these devices present over traditional fault current limiting devices. The primary advantage of the HTSFCLs is that it offers an optimal solution to the problem of protecting against the short circuit currents because the peak short circuit current is automatically limited as the superconductor makes the transition from a superconducting state to a normal state. HTSFCLs have low impedance in its superconducting state but it increases to a high value during fault.

In 1911 superconductivity was first observed in mercury by Dutch physicist Heike Kamerlingh Onnes of Leiden University, When he cooled mercury to the temperature of liquid Helium, 4 degrees Kelvin (-452F, -269C), its resistance suddenly disappeared. Materials which have this property are called superconductors. The superconductors discovered in 1911 are called low temperature superconductors as they need to be cooled to the temperature of liquid Helium to have zero resistance. Discovered in late 1980s, the high temperature superconductor opened wide range of applications for electric power systems. The development of the high temperature superconductor enabled the development of the economical fault current limiters. Early ones were designed using low temperature superconductors. They were cooled with liquid Helium, a substance very expensive and difficult to handle. The high temperature superconductor operates at high temperature and can be cooled by liquid Nitrogen, which is less expensive. This increased interest in the High Temperature Superconductor Fault Current Limiter. Figures 4.1 and 4.2 show, the superconductor

wire and cable used. The superconductor cables are in the forms of filaments of superconductor materials.

**Figure 4.1** Superconductor wire

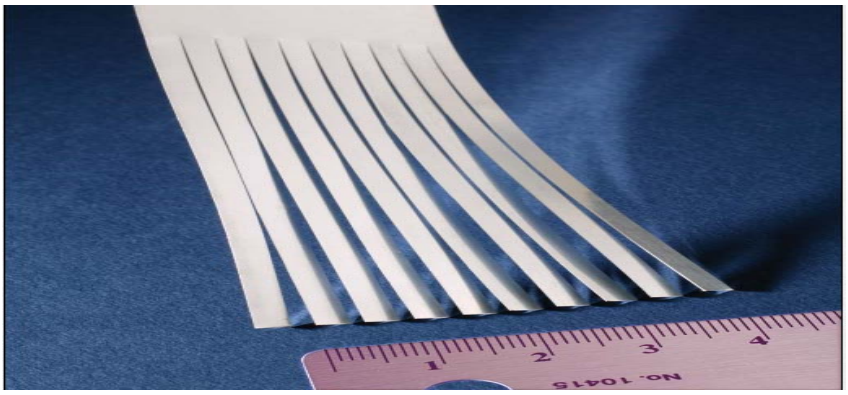


**Figure 4.2** Superconductor Cable based on today's technology

## 4.2 High Temperature Superconductor Fault Current Limiters (HTSFCL)

Superconductor based fault current limiters can be configured in one of the two ways: If the superconductor is inserted in series with the circuit, then it is the resistive type. If the superconducting short circuited secondary coil is magnetically coupled to the primary winding which is placed in series with the circuit, it is know as reactive type.

Here the investigation carried out is based on the computer modelling of the superconductor fault current limiter and MATLAB simulation is used for the modelling. The FCL under investigation is the resistive type. The superconducting material used is Bi-2223. The Bi-2223 is preferred as the superconductor material for FCL as compared to YBCO because the change in the resistivity with increase in temperature is faster in Bi-2223. Figure 4.3 shows the variation of resistivity with the

temperature, it can be seen the increase in resistivity of Bi-2223 is faster because of increase in temperature.

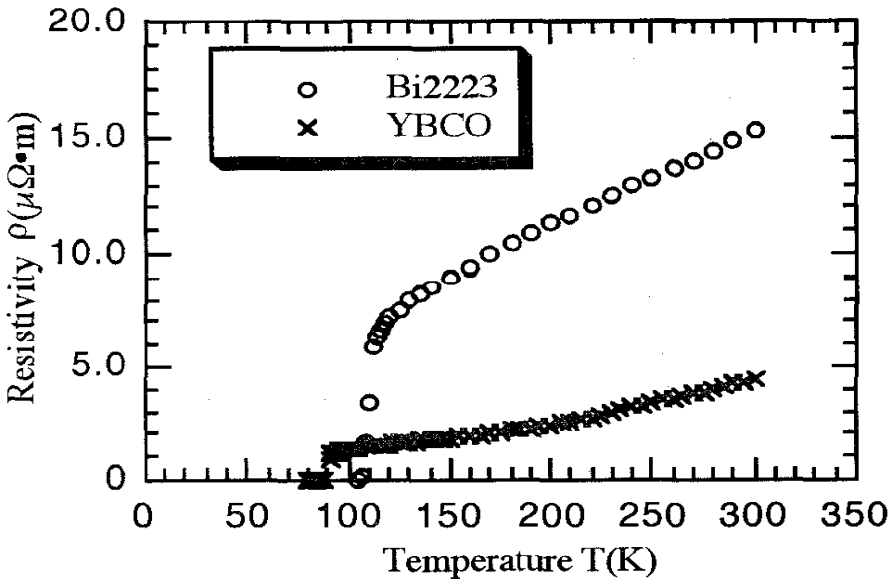



**Figure 4.3** Variation of Resistivity with Temperature of Bi-2223 & YBCO

### 4.2.1 Operating Principle of the HTSFCL

The HTSFCL that we are concerned with is the resistivity type. The resistive types are simply a length of superconductor. The current density of superconductor would exceed the critical current density $J_c$ when there is fault. Figure 4.4 (3D) shows the Temperature, Magnetic Field and Current Density (T-B-J) characteristics of the superconductor material.

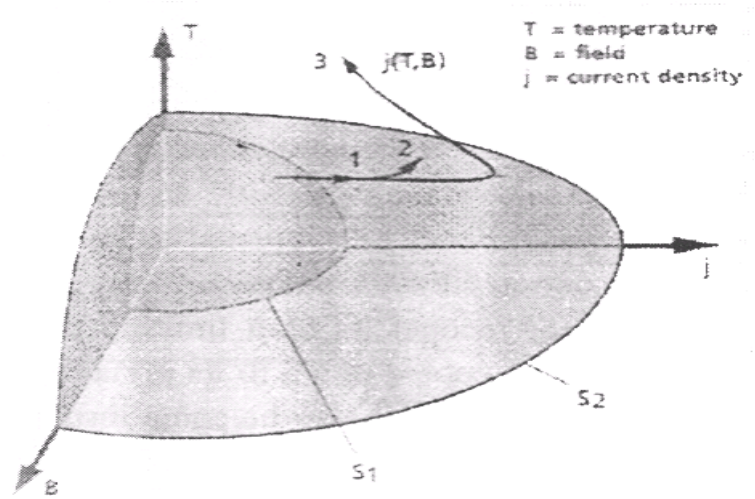



**Figure 4.4** T-B-J characteristics of superconductor material

From Figure 4.4 [33], it can be seen, the superconductor material can operate in three states, marked as 1, 2 and 3. The innermost surface (1) is called the zero resistance state; the surface beyond (2) is the normal conductance state and the transition state which is between surface (1) and (2). It is observed that with increase in the current density (J), there is increase in temperature (T), and magnetic flux density (B). When the current density exceeds the critical current density (Jc), the superconductor quickly changes to a high resistance state, and the fault current is limited to a low value.

## 4.3 Modelling of the High Temperature Superconductor Fault Current Limiter

### 4.3.1 MATLAB Simulation

In order to predict the limiting characteristics of the HTSFCL, it is implemented in the electrical system and MATLAB simulation is carried out. By solving the differential equations the current can be obtained at any point. In the simulation we apply Runge-Kutta method to solve the differential equations using time step of 0.00001s. The details can be found in the Appendix 1 which lists the complete MATLAB script.

The parameters that are considered are

- Thickness of the HTSFCL
- Length of the HTSFCL
- Specific heat capacity of the HTSFCL
- Specific resistance (Resistivity) of the HTSFCL
- Thermal conductivity of the HTSFCL

Figure 4.5 shows the circuit that has HTSFCL during steady state condition, where the current has nominal value of 9000*sqrt2 and temperature is constant at 77K as superconductor is submerged in the liquid Nitrogen. During normal operation the switch is open and the HTSFCL is in its superconducting state. The switch is closed (short circuit) in order to observe the working of the HTSFCL during fault. During fault the HTSFCL comes out of zero resistance state and the resistance of the superconductor rises to a high value, which results in an increase of temperature.

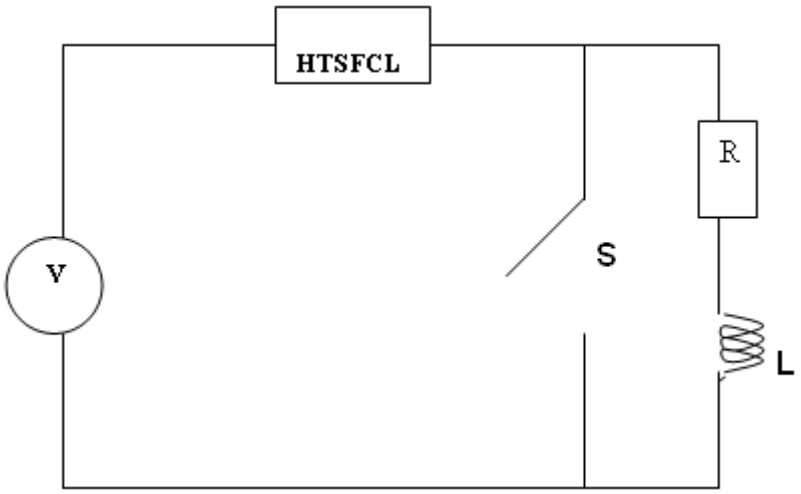



**Figure 4.5** Electrical Circuit with HTSFCL

Figure 4.6 shows the layout of the HTSFCL. The Superconductor layer of Bi-2223 is surrounded by stainless steel layers. The function of the stainless layers is to remove the heat from the superconductor element which helps to save the superconductor element from damage due to excess heat produced during fault.

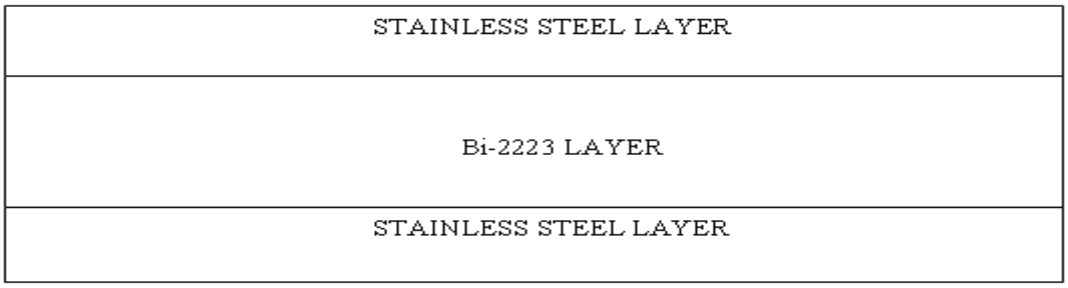



**Figure 4.6** The design of the HTSFCL

**4.3.2 Design of HTSFCL element: -** As explained above, the sample used for modelling is an 110kV, 9kA system.

1) Current

The critical current density of the Superconductor is $J_c$. In order to have tolerance during normal operation or condition the current density should not exceed k% of the $J_c$. $I_n$ is the value of nominal current. In this case the $I_p$ = 9000*sqrt2 is the peak current. The current Density is calculated by the dividing the current by the area it occupies (J = I/A). Here the $J_c = I_p/A$ and the critical current density should not

exceed k% of the $J_c$, so the value of the area should be calculated by $A= I_p/(k*J_c)$. The value of critical current density $J_c$ is 2e+7A/m^2. Results with a different value of k are shown later in this chapter. The current density is dependent on the material used.

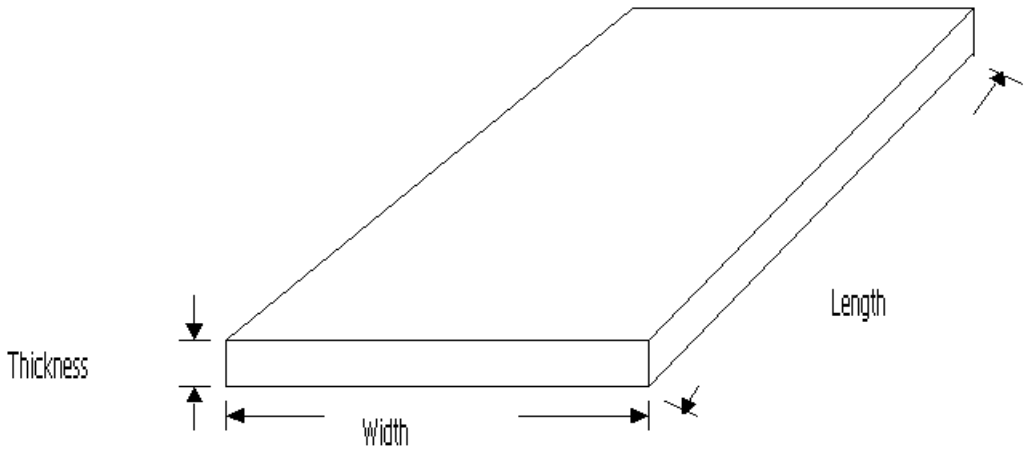



**Figure 4.7** High Temperature Superconductor

2) A = Thickness*Width

Referring to the above Figure 4.7 the area is calculated. In the modelling various thicknesses are modelled such as, 0.2mm and 0.9mm. The corresponding widths are calculated.

3) Length of the HTS (High Temperature Superconductor) wire

The sample used for modelling is on an 110kV and 9kA system. Figure 4.7 shows the typical superconductor. The area of the wire is calculated by, A= Thickness*Width. In the modelling various thicknesses are modelled and the corresponding width is calculated. The peak voltage ($V_{peak}$) of the system is given as 110000*sqrt2. This is related to the peak electric field ($E_{peak}$) and the HTSFCL length by the equation $V_{peak} = E_{peak}$*HTSFCL length. Various $E_{peak}$ values were used in the modelling. Results with different lengths of the superconductor are shown and analysed. The value of the electric field in the three distinguishable states; zero resistance (State 1), Transition State (State 2) and normal conductance (State 3) are obtained using the following equations, which is approximated by a power law.

**State 1**(Superconductor or Zero resistance state)

$E(j, T) = Ec*( j / jc(T))^{\alpha(T)}$

where $\alpha(T) = \max [ \beta, \alpha'(T) ]$, with

$\alpha'(T) = \log( Eo/Ec) / \log[( jc (77K) / jc (T))^{(1-1/\beta)} * ( Eo / Ec)^{1/\alpha(77K)}]$

where jc is the critical current density and Ec = 1 $\mu$ V/cm,

Eo,$\alpha$, $\beta$ at 77k depends on the material processing conditions and is within the following ranges

$0.1 \leq Eo \leq 10$ mV/cm,

$5 \leq \alpha \leq 15$,

$2 \leq \beta \leq 4$.

**State 2** (Transition state or flux flow state)

$E(j,T) = Eo*( Ec/Eo)^{\beta/\alpha(77K)}*jc(77K)/jc(T)*( j / jc(77K))^{\beta}$

**State 3** normal state or high resistance state

$E(j, T) = p (Tc)*T/Tc*j$

## 4.4 Results and Analysis

### 4.4.1 Normal Operation

During steady state or normal operation the switch S is open (Figure4.5). The flow of the current is shown in Figure 4.8. The start current is zero and start time, (t) is zero. From Figure 4.8 it can be seen that the current during normal operation is pure sinusoidal. The nominal current during normal operation is 9000*sqrt2 A.

Figure 4.9 shows the temperature–time graph during normal operation. It can be seen that temperature remains constant at 77 K as the superconductor is cooled by liquid Nitrogen. Due to the constant temperature of the superconductor, the HTSFCL remains in the superconductor state or zero resistance state.

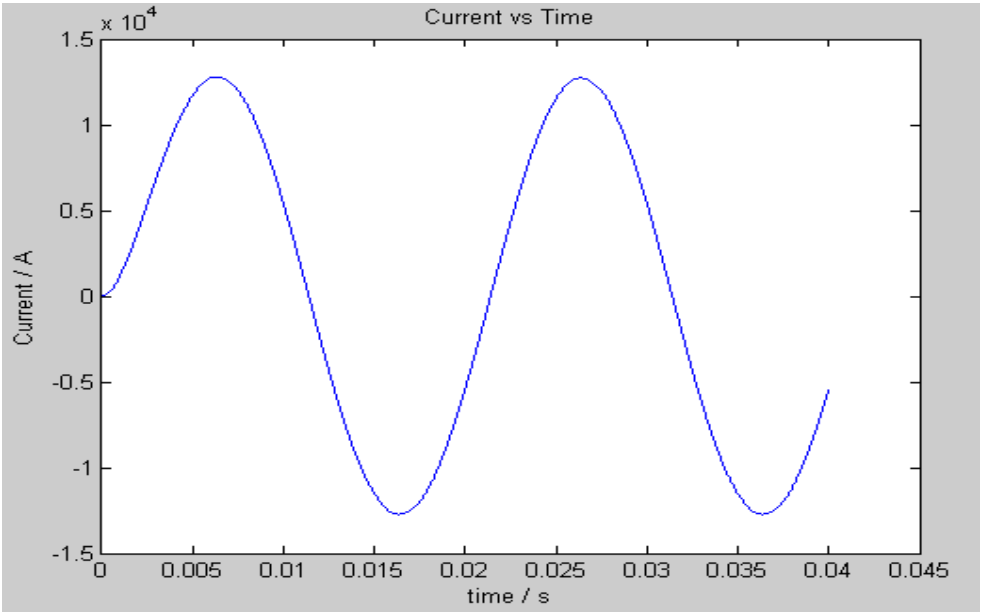



**Figure 4.8** Current Waveform during normal operation

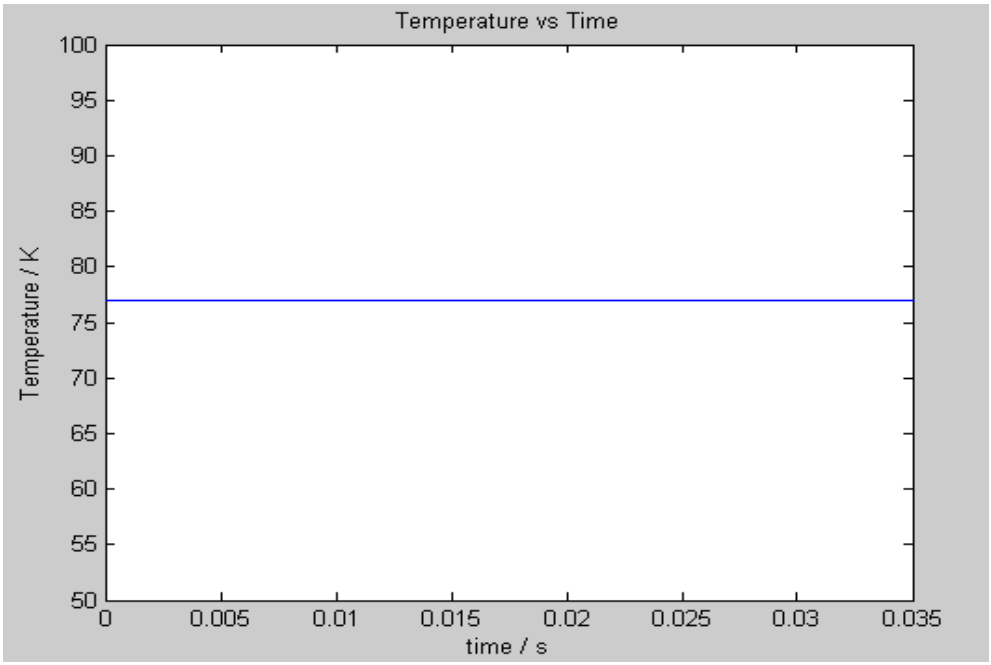



**Figure 4.9** Temperature vs. Time

The voltage drop across the HTSFCL during normal operation is very low (approx. zero) as it offers zero resistance in normal operation. The losses during normal operation are much less and therefore are neglected

### 4.4.2 Operation during Fault

In order to see operation of the HTSFCL during fault, the Switch S in Figure 4.5 is closed after two cycles. The Figure 4.10 shows the circuit during fault.

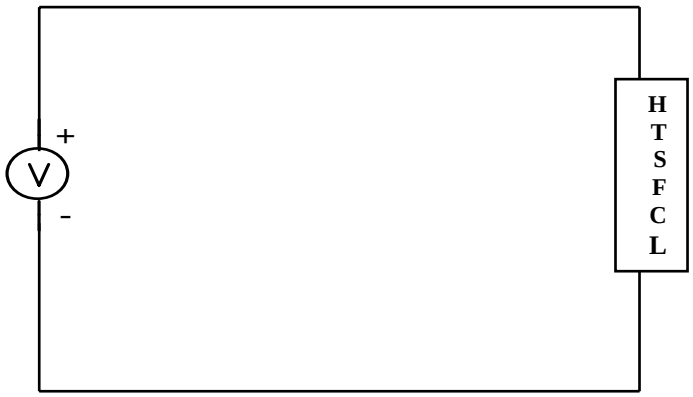



**Figure 4.10** Circuit under fault conditions

During fault the whole supply voltage appears across the HTSFCL. There is large voltage drop across the HTSFCL. Figure 4.11 shows the current waveform during fault. The switch S in Figure 4.5 is closed after two cycles (at 0.04esc).

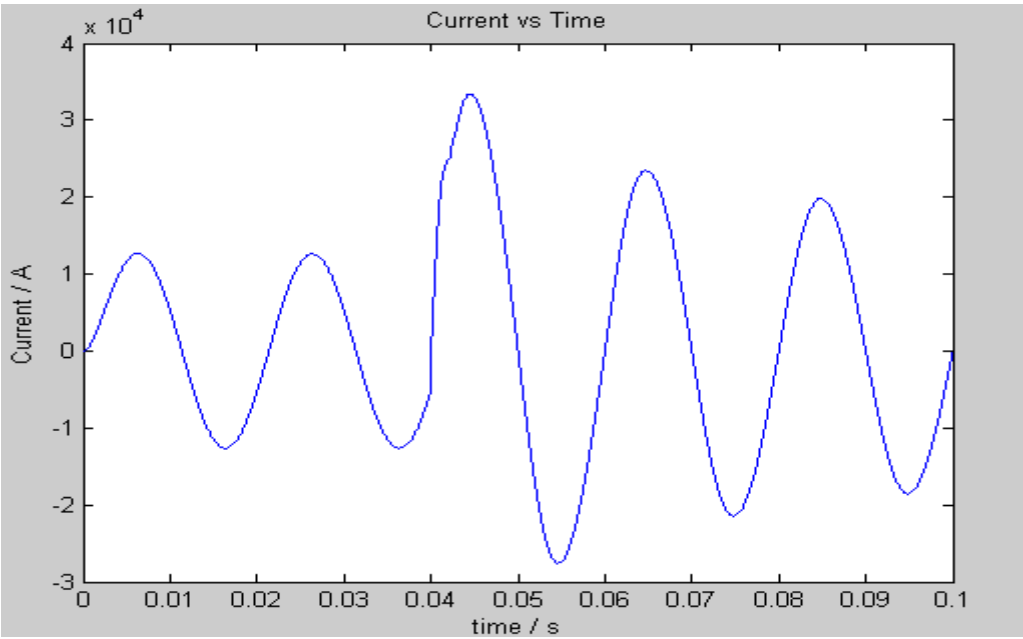



**Figure 4.11.** Current waveform during fault.

From Figure 4.11 it can be seen that the current rises to a large value at 0.04 seconds, when switch S is closed. The maximum fault current becomes more than 31KA, which is more than three times the nominal value of the current. From Figure 4.11, it can be seen that the HTSFCL takes a fraction of a second to limit the fault current. Figure 4.12 show the change in the resistance of the superconductor during fault.

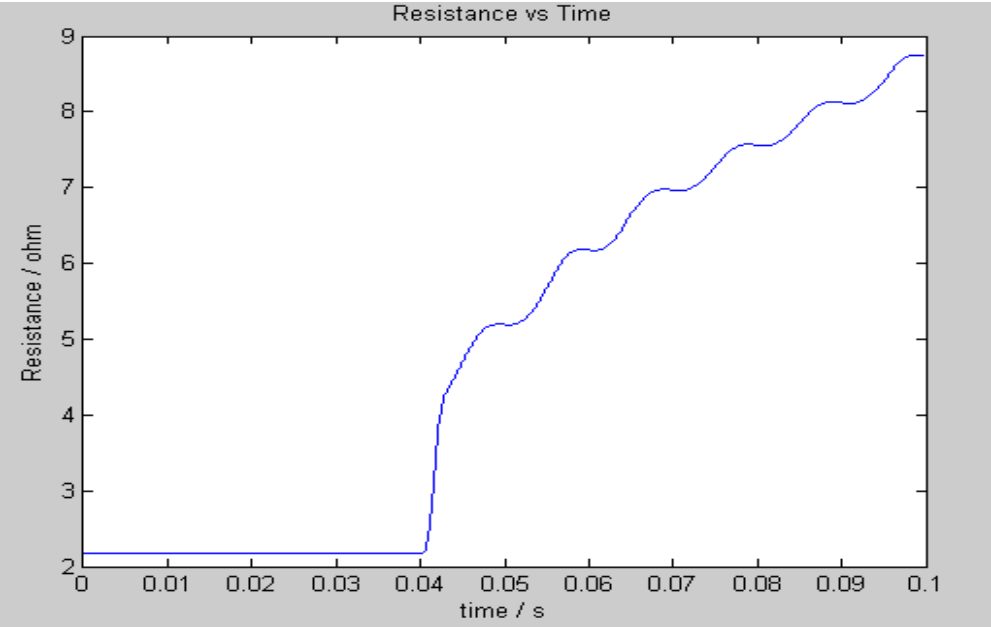



**Figure 4.12** Variation in resistance with time

Actually the exact value of the resistance of the superconductor cannot be known but from Figure 4.12 it can be shown that there will be sharp increase in the resistance of the HTFSFCL during fault. This sharp increase in the resistance of the HTSFCL limits the fault current. As the resistance increases, the HTSFCL comes out of superconductor state, or zero resistance state, and operates in normal conductance state, offering very high resistance to the fault current. Due to the high resistance of the superconductor during fault a very large amount of heat is produced which may damage the superconductor element in the HTSFCL. In order to avoid damage of the superconductor element due to heat the stainless steel around the superconductor takes the heat from superconductor and dissipates it.

Figure 4.13 shows the rise in temperature of the superconductor layers and the surrounding stainless steel layers. The critical temperature (Tc) is 108 K in this case. When the temperature becomes greater than the critical temperature of the

superconductor it switches to a high resistance state, due to which the fault current is limited to a low value, thus saving the equipment installed in the power grid or circuit.

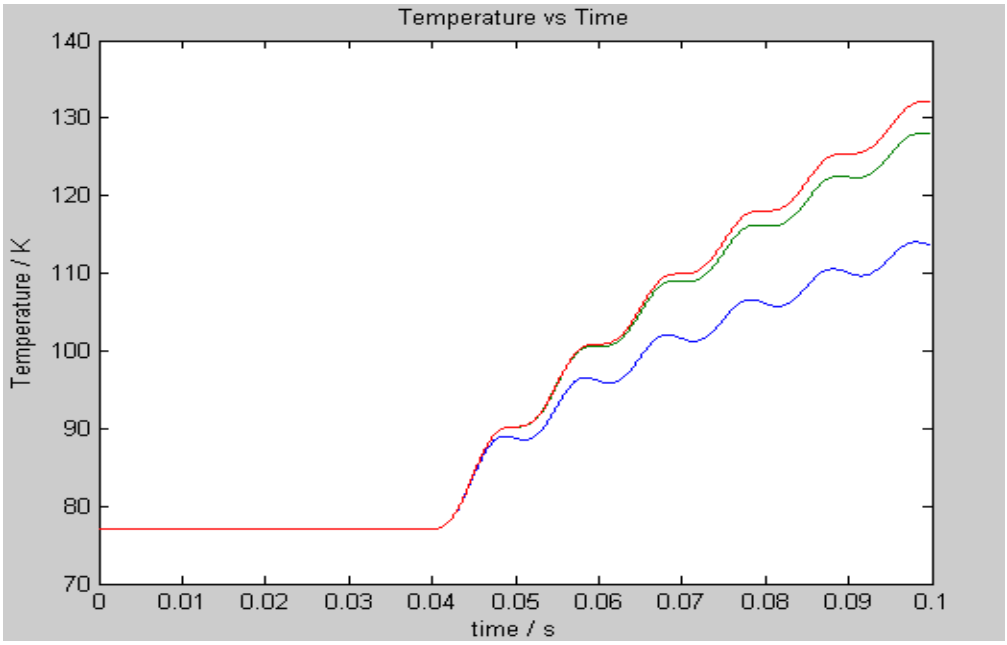



**Figure 4.13** Change in temperature of the HTSFCL

The transition state of the superconductor from superconducting state to normal state or high resistance state depends on heating of the superconductor. If the fault current is very high superconductor element heated up very fast. This causes the temperature of the superconductor to become more than the critical temperature so it operates in a high resistance state. Due to fast heating of the superconductor element, it very quickly switches to normal state or high resistance state. In slow heating the transition time is longer as compared to fast heating of the superconductor. During fault a large amount of fault current flows through the superconductor, resulting in heating of the superconductor element and which may result in formation of the hot spot, thus damages the superconductor. It is desirable that the heat generated in the superconductor during fault should be absorbed by the stainless steel layers around it, thus protecting the superconductor from damage. The behaviour of the HTSFCL is largely determined by its length and the type of material used. The shorter conductor length with fast heating no doubt saves expense on conductor material but there will be a large electric field distributed over the superconductor resulting in overheating. In a few hundred microseconds the HTSFCL enters the normal conductance zone or high resistance state. In this case there will be quite slow recovery of the

superconducting state. More over there will be severe over voltages along with current reduction, caused by the rapid transition to normal conduction state. In order to reduce these overvoltages, a normal resistor or reactor should be used in parallel to the HTSFCL.

Below some results are shown for changing the length of the superconductor.

**Table 4.1**

Fault Current & Temperature corresponding to different Length of Superconductor at k= 0.8, thickness = .002m and Specific heat capacity= 6.35e+5(kJ $kg^{-1}$ $K^{-1}$)

| Length (m) | E (v/m) | Fault Current (A) | Fault Current after 1 and 2 cycles(A) | Temperature (K) |
|---|---|---|---|---|
| 70 | 2222 | 40572 | 25976, 22019 | 151 |
| 80 | 1944 | 36700 | 24700, 20350 | 137 |
| 100 | 1555 | 30701 | 22718, 19130 | 120 |
| 120 | 1296 | 26298 | 21041, 17703 | 113 |

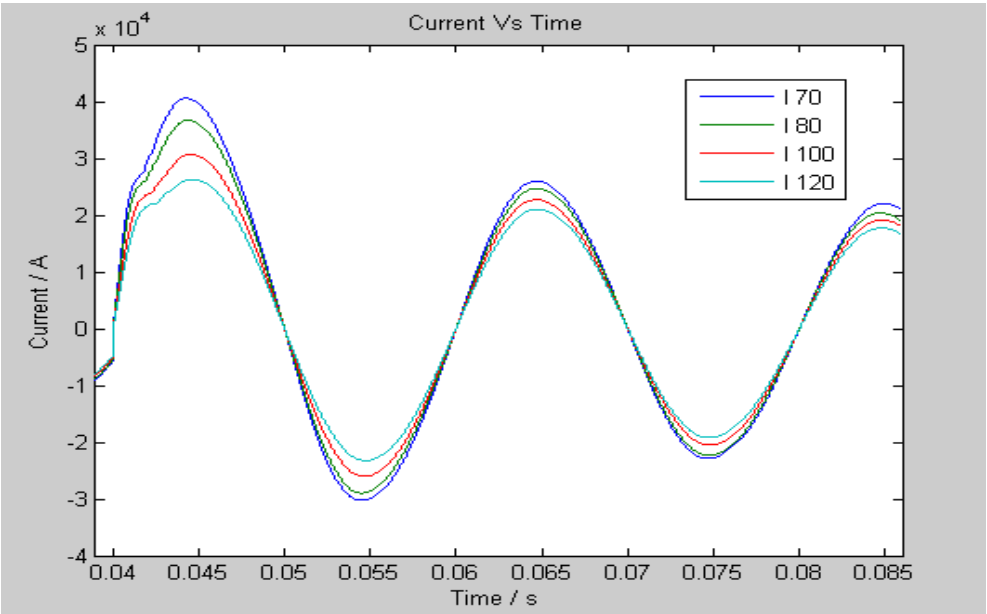



**Figure 4.14 (a)**

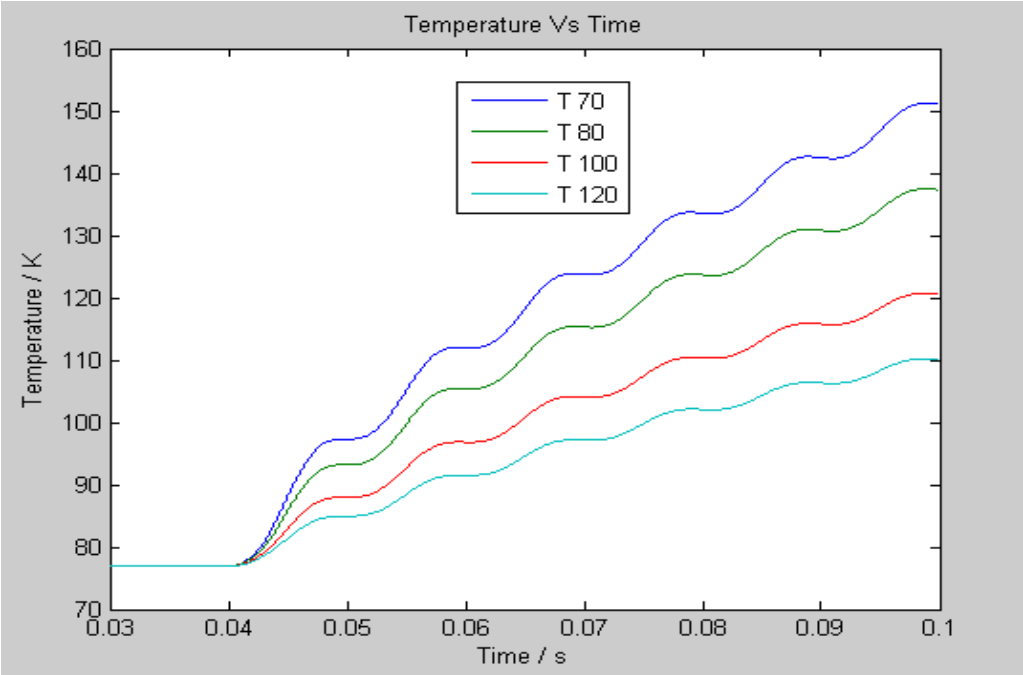



**Figure 4.14(b)**

**Figure 4.14 (a)** Fault Current and **(b)** Temperature corresponding to different length of the superconductor at thickness of 0.002m (k=0.8)

The above table 4.1 shows the value of fault current, electrical field and temperature corresponding to different values of length. The results shown in Figure 4.14 and table 4.1 are of superconductors for thickness equal to 0.002m and k=0.8. From table 4.1 it can be observed that with a smaller length of the superconductor a strong electric field is developed and also a large fault current flow in the model. As explained earlier with a short length of the superconductor a large amount of heat is produced and which may damage the superconductor. In Figure 4.14(b) the blue line (T 70) shows the temperature of a superconductor at length 70m, it can be observed that as the length of the conductor is increased, there is decrease in the electrical field which results in decrease in the fault current and also temperature of the superconductor.

Now we will change the thickness of the superconductor and will see its effect on the operation of the HTSFCL.

**Table 4.2**

Fault Current & Temperature corresponding to different Length of Superconductor at k =0.8, thickness of .009m and specific heat capacity= 6.35e+5(kJ $kg^{-1}$ $K^{-1}$)

| Length (m) | E (v/m) | Fault Current (A) | Fault Current after 1 and 2 cycles(A) | Temperature (K) |
|---|---|---|---|---|
| 70 | 2222 | 40588 | 25446, 21935 | 157 |
| 80 | 1944 | 36711 | 24267, 19377 | 142 |
| 100 | 1555 | 30706 | 22279,18581 | 124 |
| 120 | 1296 | 26301 | 20762, 17256 | 112 |

Table 4.2 shows the values of the fault current and temperature when the thickness of the superconductor is increased to 0.009m. If we compare the table 4.2 with table 4.1 it can be seen that the rise in temperature of same length is greater when the thickness of the superconductor is increased. The heat produced during fault is dissipated much faster if the thickness is less. Figure 4.15(a) shows the current waveforms corresponding to different length of the superconductor when the thickness is 0.009m. It is observed that the fault current is a little bit more in Figure 4.15(a) as compared with Figure 4.14(a). Figure 4.15(b) shows the change in the temperature of the superconductor corresponding to the change in length of the superconductor. The thickness of the conductor in this case is 0.009m, where it is 0.002m in Figure 4.14(b).

It can be seen that with an increase in the thickness of the superconductor the temperature also increases more than when the thickness is 0.002m. In Figures 4.14(a) and 4.15(a) the blue line (I 70) is the current corresponding to 70m length of the superconductor and the red line is the fault current corresponding to superconductor length 100m. It can be observed also that as the length is increased the fault current is reduced closer to its nominal value

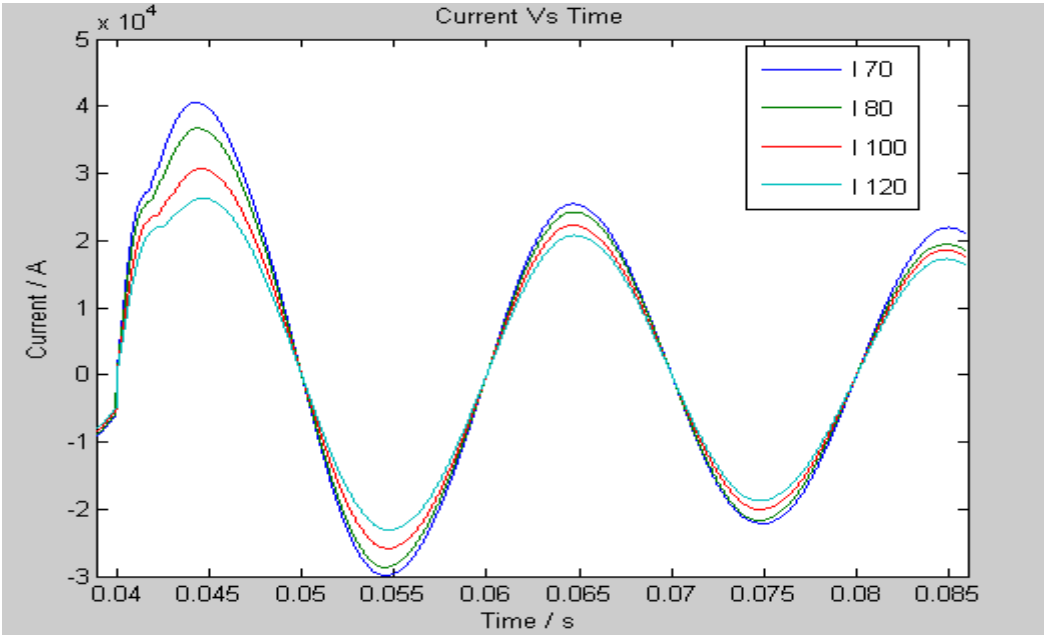



**Figure 4.15(a)**

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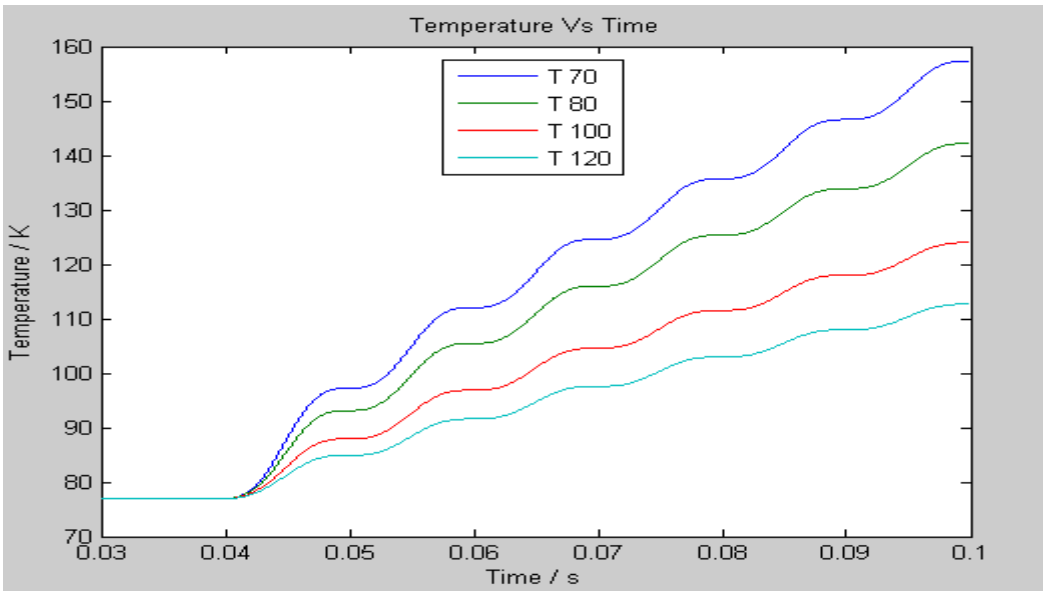



**Figure 4.15(b)**

**Figure 4.15 (a)** Fault Current **(b)** Temperature corresponding to different lengths and at thickness of 0.009m of the superconductor. (k=0.8)

Similarly in Figures 4.14(b) and 4.15(b), the blue line shows the rise in the temperature of the superconductor of length 70m during fault and red line shows the temperature rise in the superconductor corresponding to length of 100m. From the

above Figures 4.14(b) and Figure 4.15(b). It can be seen that as the length of the superconductor is increased the temperature is decreased. As explained earlier too short length of the superconductor is not suitable as it will damage the superconductor element in the HTSFCL due to large amount of heat is produced during fault. If very long superconductor is used, the amount of electric field to which it is exposed is very less and as the field varies in direct proportion with the voltage and inversely with the conductor length, which results in the critical current density to exceed only slightly and will stay within the outer boundary of the transition region. The conductor warms up slowly due to its length, causing high AC losses, which will result in heavier demand of the cooling system. Also due to the length of the conductor, the temperature is constant and the limiter does not heat up, so the device can be brought back into operation as soon as the breaker is closed. For a long conductor a large amount of superconductor is needed, results in additional cost. The other drawback of using a long conductor is that it takes a long time to return from its normal state to its superconducting state.

If a superconductor of intermediate length is used the electric field during fault will be high but still less than the electrical field imposed on a conductor of a very short length. In this case the current density rises to greater value during fault than it rises to in the case of a long conductor, although remains inside the transition region. The power dissipated will be higher in this case than in the case of a longer conductor, so the conductor will heat up and after a few tens of milliseconds it will pass the outer transition boundary and enter the normal conducting region.

As explained earlier, to keep a tolerance during normal operation the current density J should not exceed k% of $J_c$. The value of k was 0.8 for the above results, now we will change the value of k to 0.7 or 70% of $J_c$. The results for k=0.7 are reported and the change in the fault current and temperature is observed.

Table 4.3 shows the results when k=0.7 and the thickness is 0.002m. To keep a tolerance during normal operation the current density J should not exceed 70% of $J_c$. It is seen as we decrease the tolerance (k), a large fault current is produced during fault, which is greater than the fault current produced when the value of k was 0.8 for the same length.

**Table 4.3**

Fault Current & Temperature corresponding to different Length of Superconductor at k =0.7, thickness of .002m and specific heat capacity= 6.35e+5(kJ $kg^{-1}$ $K^{-1}$)

| Length (m) | E (V/m) | Fault Current (A) | Fault Current after 1 and 2 cycles (A) | Temperature (K) |
|---|---|---|---|---|
| 70 | 2222 | 46352 | 29616, 25155 | 151 |
| 80 | 1944 | 41930 | 28170, 23138 | 137 |
| 100 | 1555 | 35079 | 25903, 21797 | 121 |
| 120 | 1296 | 30050 | 24009, 20162 | 110 |

The temperature rise of the superconductor is shown in Figure 4.16(b). From Figure 4.14(b) and Figure 4.16(b) it can be seen that the temperature rise or change is the same for different values of k. The current after the first and second cycles is higher when we decrease the value of k from 80% to 70%.

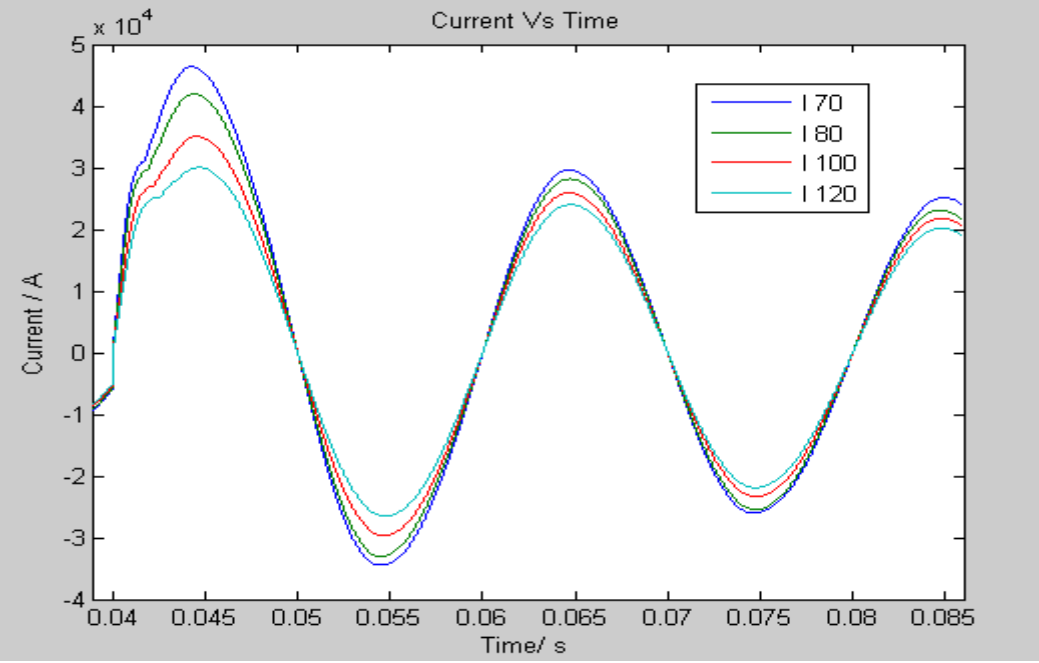



**Figure 4.16(a)**

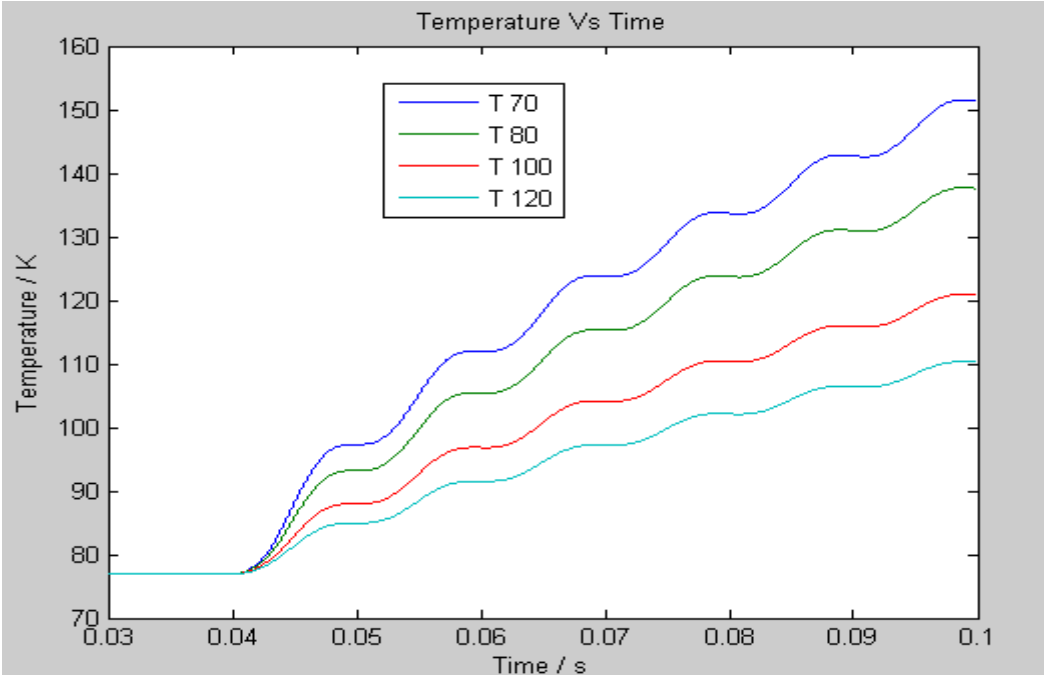



**Figure 4.16(b)**

**Figure 4.16(a)** Fault Current **(b)** Temperature corresponding to different lengths and at thickness of 0.002m of the superconductor (k=0.7)

The blue line (I 70) in Figure 4.16(a) shows the waveform of current when the length of the superconductor is 70m. In Figure 4.16 (b) blue line (T 70) shows the temperature change of the superconductor corresponding to length 70m. The values of the fault current after 1 and 2 cycles and corresponding to different lengths of the superconductor are shown in the table 4.3 with thickness kept constant at 0.002m and k =0.7.

**Table 4.4**

Fault Current & Temperature corresponding to different Length of Superconductor at k =0.7, thickness of .009m and specific heat capacity= 6.35e+5 (kJ $kg^{-1}$ $K^{-1}$)

| Length (m) | E (V/m) | Fault Current (A) | Fault Current after 1 and 2 cycles (A) | Temperature (K) |
|---|---|---|---|---|
| 70 | 2222 | 46384 | 29076, 25067 | 157 |
| 80 | 1944 | 41953 | 27729, 22149 | 142 |
| 100 | 1555 | 35091 | 25457, 21231 | 123 |
| 120 | 1296 | 30057 | 23725, 19718 | 112 |

The above table (4.4) shows the value of the fault current when the value of k=0.7 and thickness is 0.009m. On comparing the values of the fault current in the table 4.3 and table 4.4, we see the fault current values are slightly higher when the thickness of the superconductor is increased to 0.009m. Similarly it can be seen that there is an increase in the temperature of the superconductor when the thickness of the superconductor is increased. The results are shown in Figure 4.17(a) and 4.17 (b).

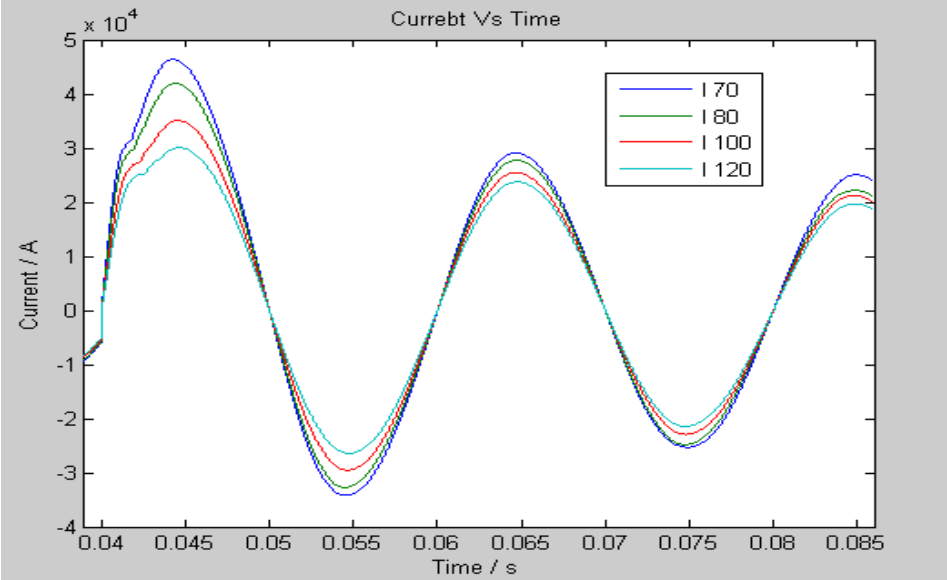



**Figure 4.17(a)**

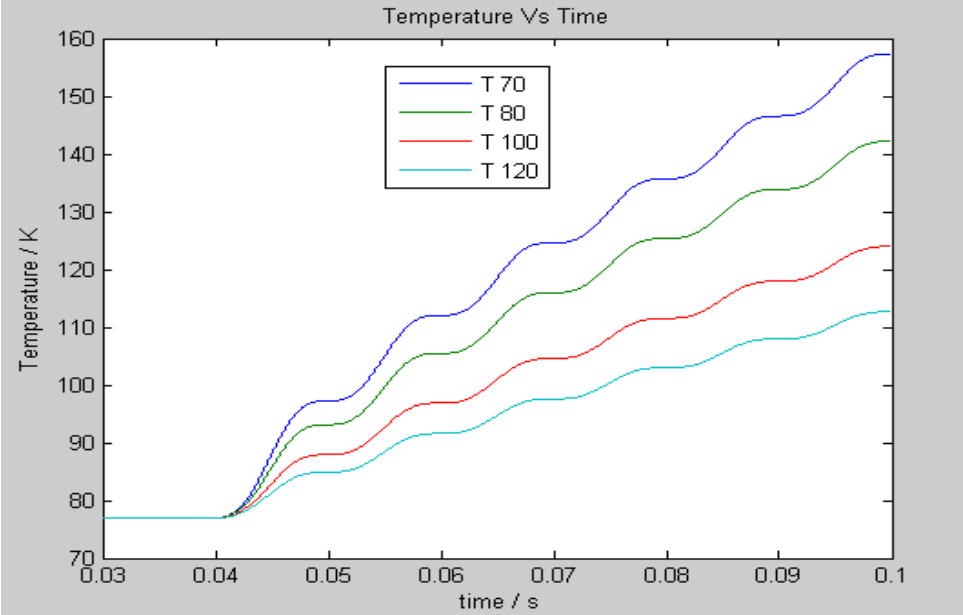



**Figure 4.17(b)**

**Figure 4.17(a)** Fault Current **(b)** Temperature corresponding to different lengths and at thickness of 0.009m of the superconductor (k=0.7)

Table 4.5 shows the results for k=0.9 and thickness = 0.002m. It can be seen that the fault current is limited to a lower value as compared to when k=0.8 and k=0.7. The temperature of the superconductor of length=70m rises to 151K which is less compared to temperature when k=0.8. The current at different length of superconductor and k=0.9 is shown in Figure 4.18(a) and temperature is shown in Figure 4.18(b). To increase tolerance limit k=0.8 is used.

**Table 4.5**

Fault Current & Temperature corresponding to different Length of Superconductor at k=0.9, thickness = 0.002m and specific heat capacity = 6.35e+5 (kJ $kg^{-1}$ $K^{-1}$)

| Length (m) | E (V/m) | Fault Current (A) | Fault Current after 1 and 2 cycles (A) | Temperature (K) |
|---|---|---|---|---|
| 70 | 2222 | 36073 | 23133, 19578 | 151 |
| 80 | 1944 | 32629 | 21991, 18162 | 137 |
| 100 | 1555 | 27294 | 20230, 17044 | 120 |
| 120 | 1296 | 23379 | 18727, 15778 | 110 |

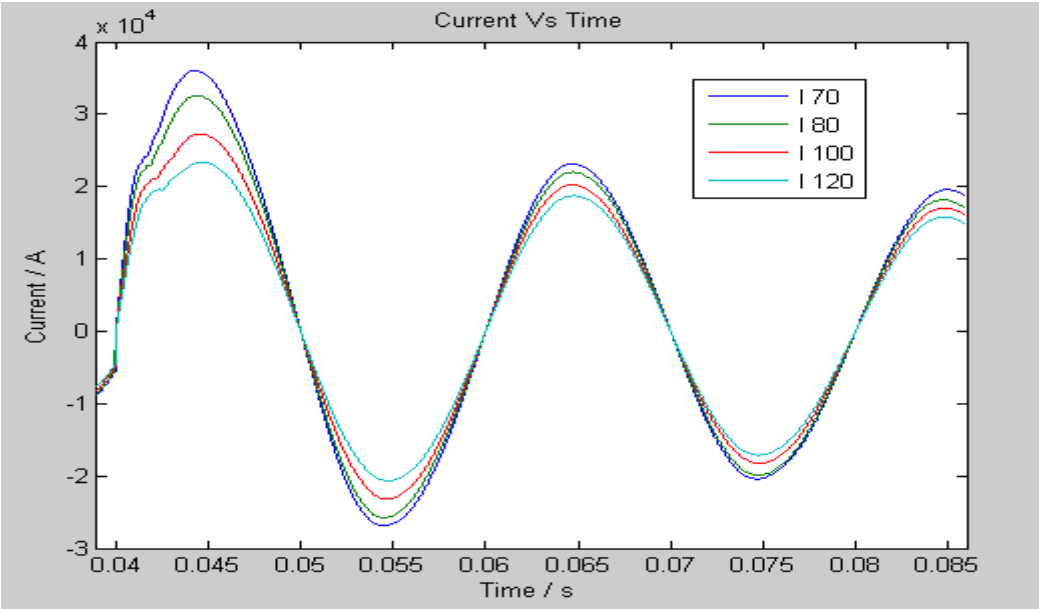



**Figure 4.18(a)**

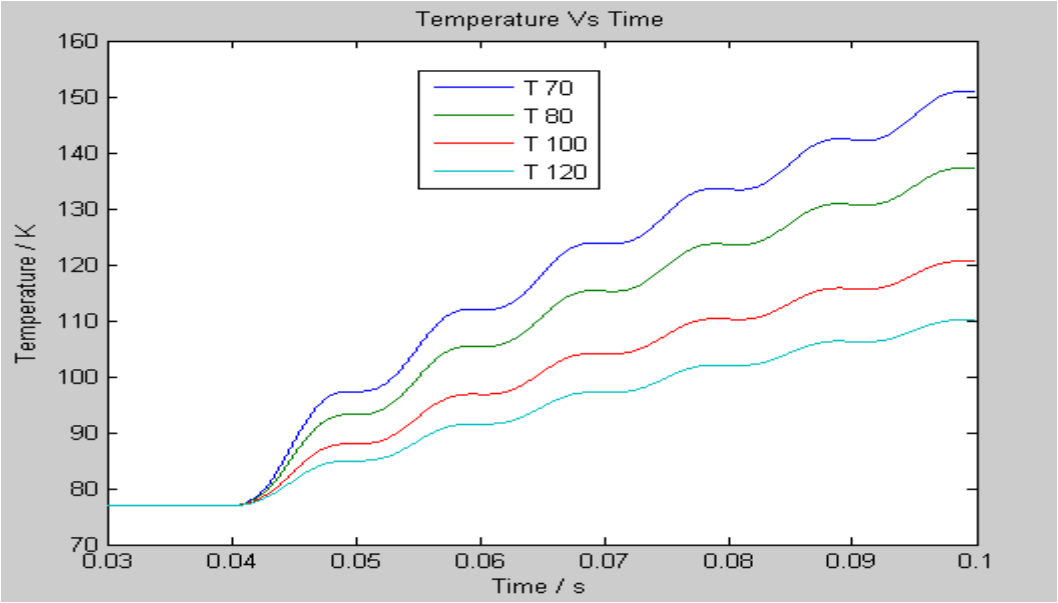



**Figure 4.18(b)**

**Figure 4.18(a)** Fault Current **(b)** Temperature corresponding to different lengths and at thickness of 0.002m of the superconductor (k=0.9)

Figure 4.19 and Figure 4.20 show the variation of temperature with thickness at different electric field. It can be seen that when increasing the thickness of the superconductor there is also increase in the temperature of the superconductor.

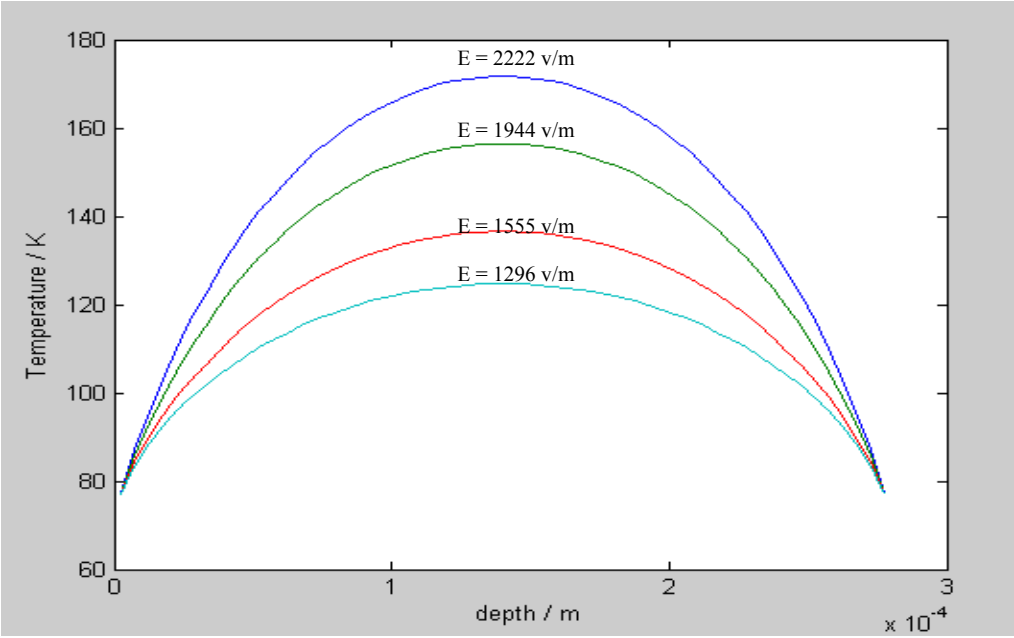



**Figure 4.19** Variation of the temperature with thickness (max. 0.0003m)

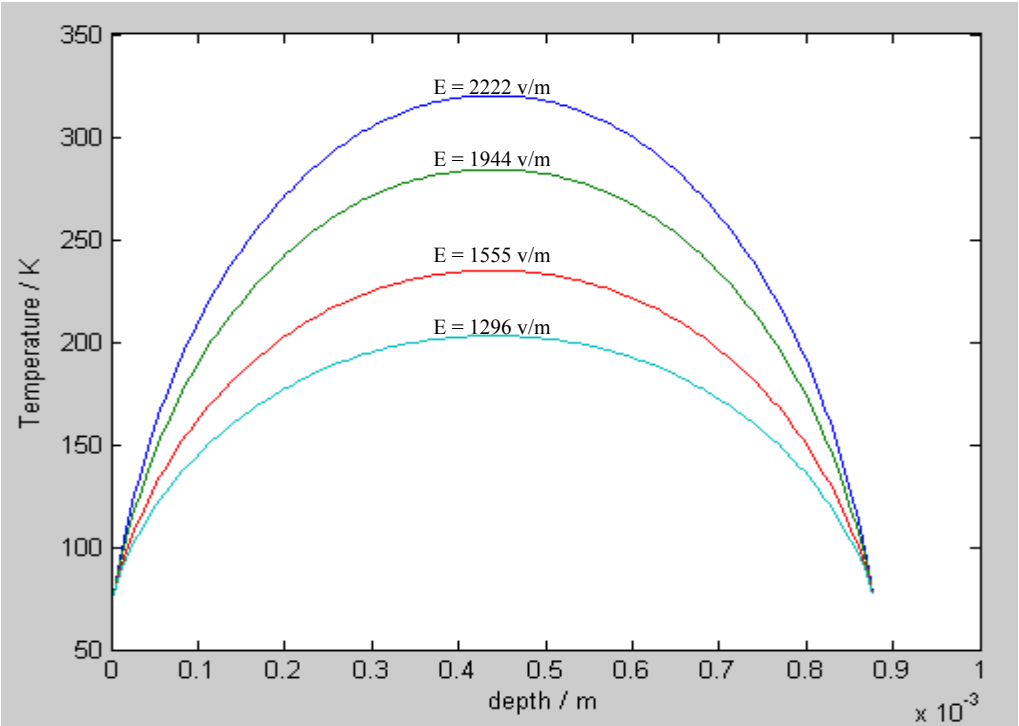



**Figure 4.20** Variation of the temperature with thickness (max. 0.0009m)

## 4.5 Conclusions

From the MATLAB simulation it is clear that the HTSFCLs are an effective technique for limiting the potentially damaging effects of the fault current on the equipment installed in the power systems. HTSFCLs are the most common uses of the superconductors and they are increasingly being used in electrical applications. As the MATLAB simulation uses simple circuit, the general principles are applicable in real world circuits. Results with different lengths of the superconductor are reported. It is observed that a superconductor of intermediate length is used. The length depends on the level of fault current to be interrupted. In order to apply some tolerance k=0.8 is used. The superconductor is cooled by liquid Nitrogen; as good and reliable cooling system is required in order to have efficient operation of the HTSFCL. Thickness of 0.002m is used because the temperature rise is less and heat from the superconductor can be easily removed during fault. The Superconductor element is surrounded by stainless steel in order to remove heat from the superconductor element during fault and avoid any damage to the superconductor. The detail of the MATLAB script used is shown in the Appendix 1.

# Chapter 5

# PSAT Based Analysis and Design

## 5.1 Introduction

In order to see the operation of power system circuits during fault and normal condition, Power System Analysis Toolbox (PSAT) has been used. PSAT is a MATLAB toolbox for electric power systems. This software is currently used by more than 50 countries in the world. PSAT is used in several universities to teach graduate and undergraduate courses. It also provides support to students and researches all over the world through its own Web forum. PSAT acts as virtual laboratory over the internet because the power systems laboratories have always been virtual as it is not possible or easy to perform practical experiments on high voltage transmission systems. Figure 5.1 shows a PSAT window.

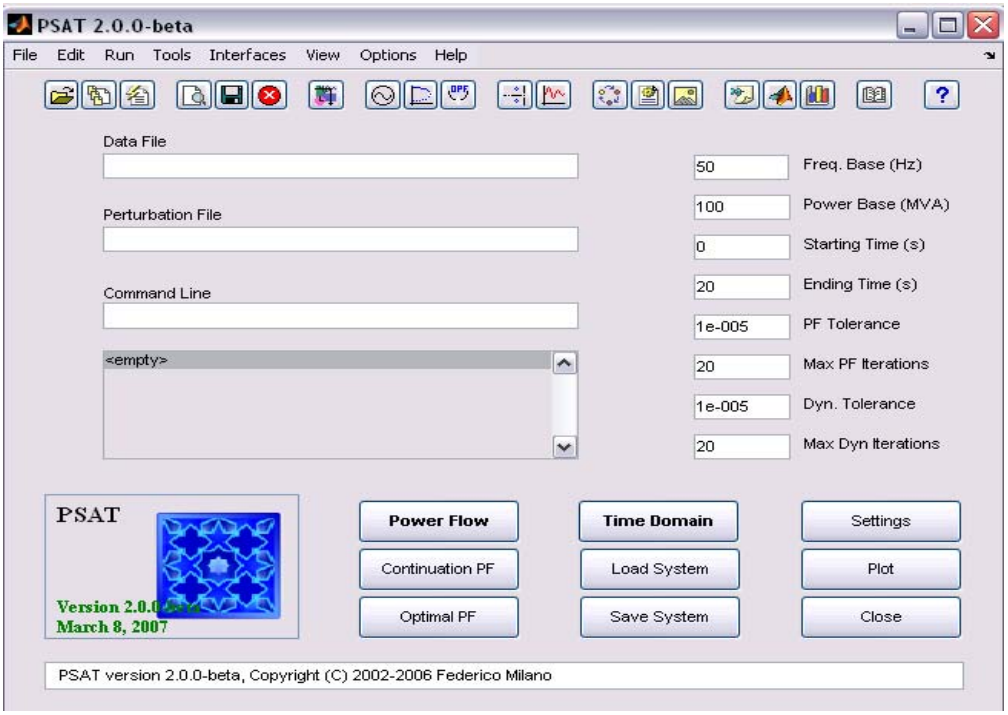



**Figure 5.1** Power System Analysis Toolbox Window

PSAT is open source software which allows in changes to the source codes and the addition new algorithms, as compared to the other commercial programs which are closed source; PSAT offers many advantages.

The nine buses with three machine model has been designed in the PSAT as shown in Figure 5.2 and its operation under normal and fault condition has been analysed. Power flow and time domain simulation has also been performed on the nine bus system. Results under normal condition are reported and analysed. In this chapter the modelling of the nine bus system is discussed and the power flow results are shown. The next section shows and explains the modelling of the nine bus model using PSAT simulink based library.

## 5.2 Modelling and Design of the 9 Bus System in PSAT

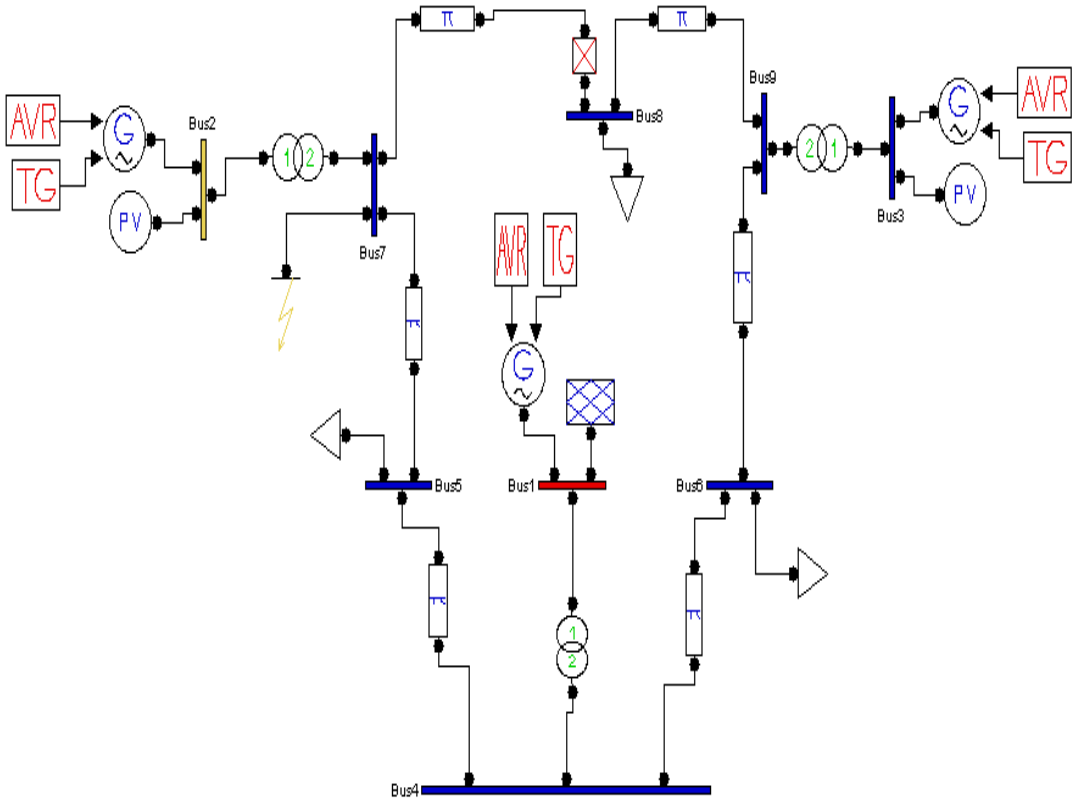



**Figure 5.2** Shows the 9 Bus and 3 machine network designed for simulation

The above Figure 5.2 shows the nine bus network design for simulation in the PSAT. The network has nine buses and three synchronous generators at buses 1, 2 & 3. The synchronous generator at bus 1 has a generating voltage of 16.5KV that of bus 2 has a generating voltage of 18.0KV and that of bus 3 with generating voltage of 13.8kv. The Transformers are connected between buses and synchronous generators to step-up the voltage to 230KV. A fault is applied at bus 7 in order to see the

operation of the system under fault. In the above network the simulation is run without applying fault and the results of the power flow are observed, The results are shown later in this chapter and the power flow report is shown in Appendix 2. The AVR (Automatic Voltage Regulators) and TG (Turbine Governors) blocks are connected to the synchronous generators, the function of these blocks is to bring the generators back to synchronism after the fault or during any disturbance in the system. The slack bus at bus 1 compensates for the losses in the system. The loads are connected to bus 5, 6 and 8. The circuit breaker is connected between the bus 7 and bus 8. Two PV generators are connected at bus 2 and bus 3. The AVR and TG blocks are connectected to all the Synchronous generators in the above system. The design of the above network in the PSAT simulink library is explained in the next section.

### 5.2.1 Modelling and design procedures of the 9 Bus network

Figure 5.3 shows the simulink Library main window in PSAT. The simulink library makes use of Physical Model Components (PMCs), thus allowing bidirectional connections. The components or block windows can be opened by clicking on the components in the main library window.

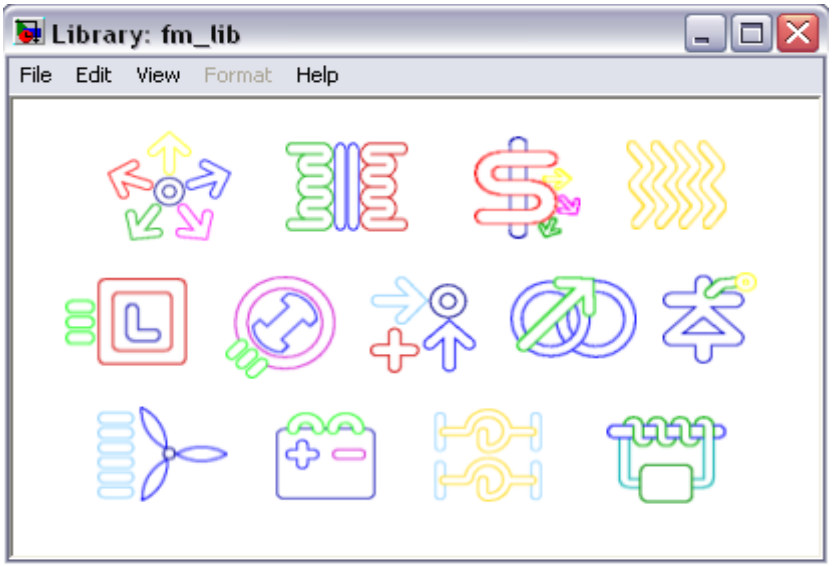



**Figure 5.3** Main Simulink Library window

The models are used as a graphical user interface. After connecting the blocks and making the model design, data from the model is extracted and a PSAT data file is created. The files created from simulink models are marked with the flag (mdl). If we double click on the first element of the simulink library main window shown in Figure

5.3, the window shown in the Figure 5.4 will open and blocks needed for the design of the network can be dragged from this window into the model window.

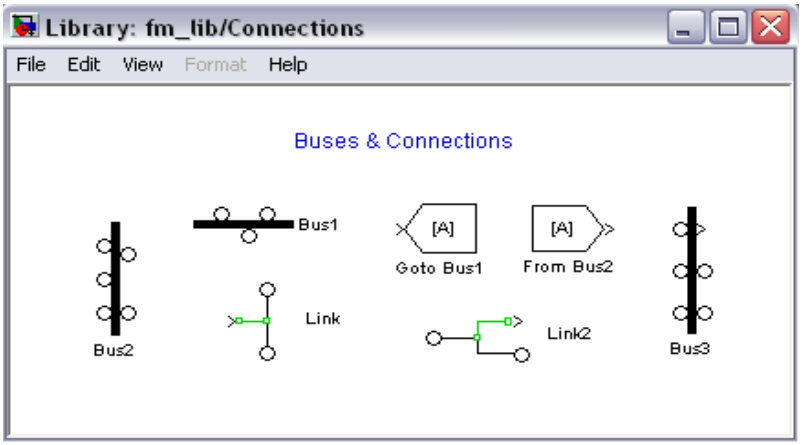



**Figure 5.4** Connections window in Simulink Library

If we drag bus1 block from the above Figure 5.4 with input port two and output port one and it is possible to change the number of input and output ports by simply double clicking on the bus1 block, causing the window shown in Figure 5.5 to appear. Figure 5.5 shows the window in which parameters of the bus block are to be entered. The top two rows show the number of the input output ports to be required. The third row shows the voltage rating of the bus and can be changed according to the ratings of the network to be designed. The nine bus blocks are required in the design of the nine bus system shown in Figure 5.2, which has a different number of input and output ports.

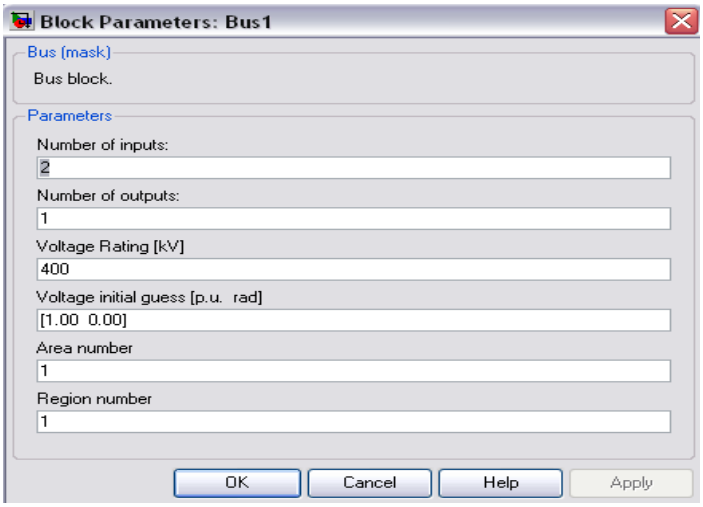



**Figure 5.5** Window for parameters of the Bus block.

Now we double click on the second element of the first row in the main window of the simulink library shown in Figure 5.3 and the window shown in Figure 5.6 will appears on the screen.

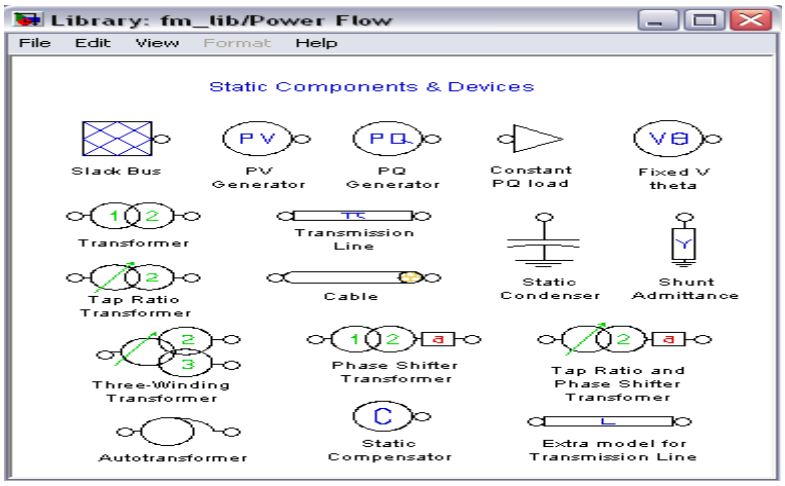
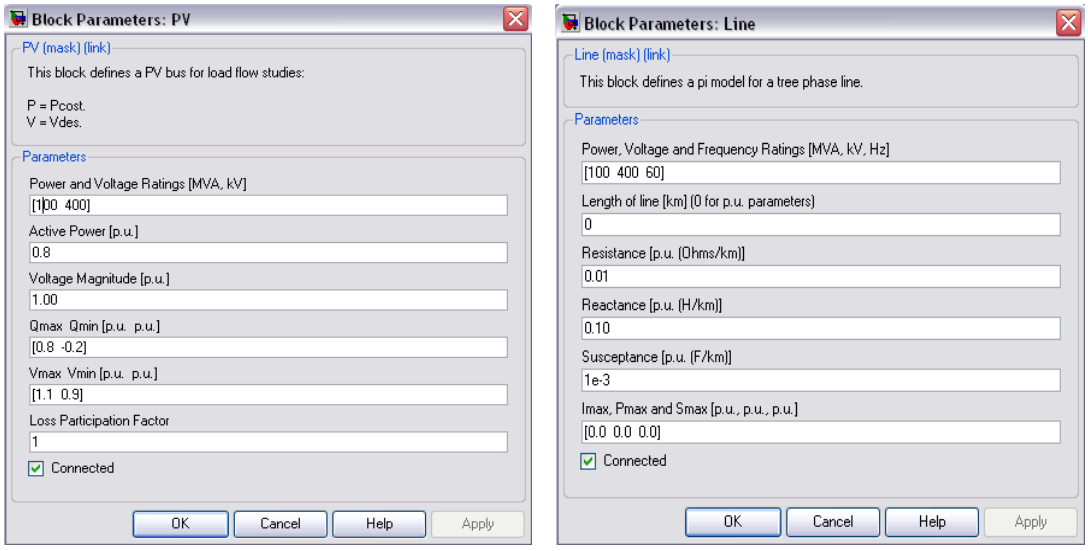



**Figure 5.6** Simulink Library Power flow data window.

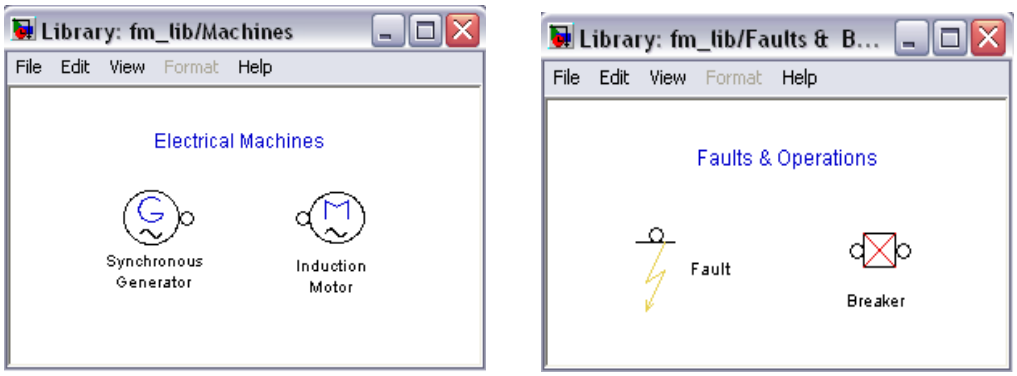
The window in Figure 5.6 is called the power flow data window. In the top row of the above Figure 5.6, the first element is the slack bus; the second component is the PV generator and the fourth component is the PQ load block. The second component of the second row of the power flow data window is the transmission line, which is used to connect the two buses in the network. The main components used in the design of the nine bus network from this window are transformers, slack bus, PV generators, PQload and transmission lines




**(a)** **(b)**

**Figure 5.7** Block parameter windows of **(a)** PV generator **(b)** Transmission Line

The input parameters of the above components such as power, resistance, reactance, active power and reactive power etc. are entered through the block mask window as show in Figure 5.7(a) and (b). The block mask window or block parameter window of PV generator and transmission lines are shown in Figure 5.7. The other components used in the design of a nine bus system are transformers, AVR, TG, circuit breaker, fault and synchronous generator. On double clicking the second element of the second row in the main window of the simulink library shown in Figure 5.3, the window shown in Figure 5.8(a) will open.




**(a)** **(b)**

**Figure 5.8 (a)** Electrical machine **(b)** Fault & Breaker windows of Simulink library

In Figure 5.8(a) the first component is the synchronous generator and it is dragged from this window to the model window. Figure 5.8(b) shows the fault and breaker windows, containing fault and circuit breaker components. Similarly these blocks contain mask windows in which the data is entered. Below, Figure 5.9 shows the Simulink window containing AVR and TG blocks

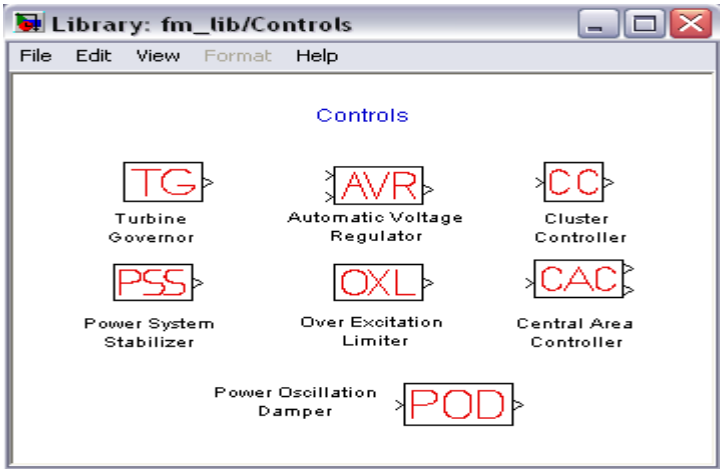



**Figure 5.9** Simulink Library: Control window

The simulink components from the simulink library are used to design the network shown in Figure 5.2. When the nine bus network is designed, it is saved and uploaded from the save location into the main PSAT window, to perform power flow simulation on the system. The window shown in Figure 5.10 is opened from the main PSAT window show in Figure 5.1 by clicking file and then opening the data file. The simulink files are in the format 'filename.**mdl'**, by clicking on the load button the file is loaded to the main PSAT window and then the power flow simulation is performed.

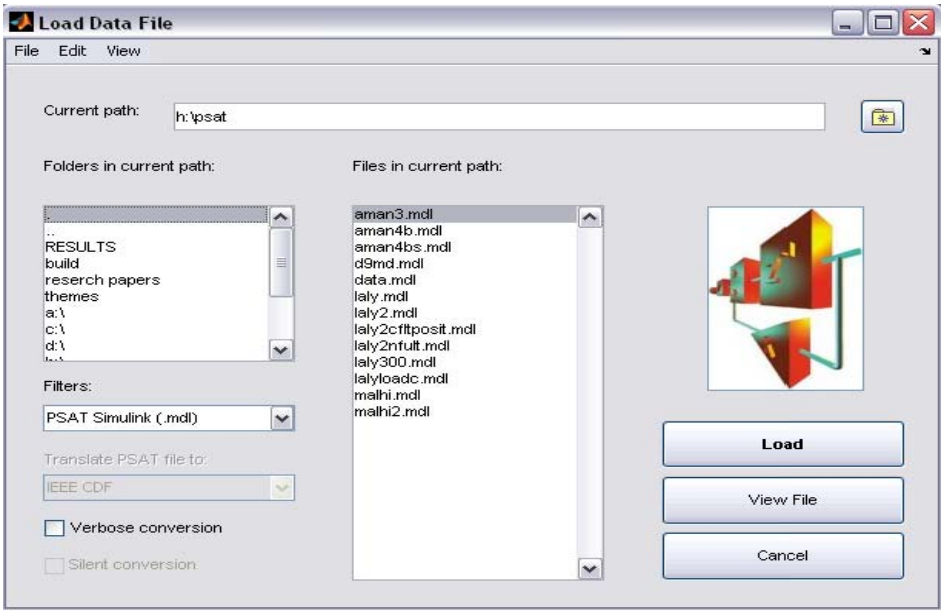



**Figure 5.10** Load Data Window of PSAT

## 5.3 Results after running Power Flow on the network

After loading the data in the main PSAT window shown in Figure 5.1, the power flow button on the window is clicked to run power flow simulation on the data. Figure 5.11 shows the results of the power flow. The power flows, real and reactive in all the transmission lines are shown. The positive and the negative sign show the flow of the power in and out from the bus. In Figure 5.11 P (Real power) and Q (Reactive power) are shown. The static report of the results is also shown in Figure 5.12. The power flow simulation is done in order to see that the system is working fine without error. After running the power flow, the powers at each bus are calculated and also the losses. The mismatch of the power is also calculated and it is desirable that the mismatch should be at its minimum value.

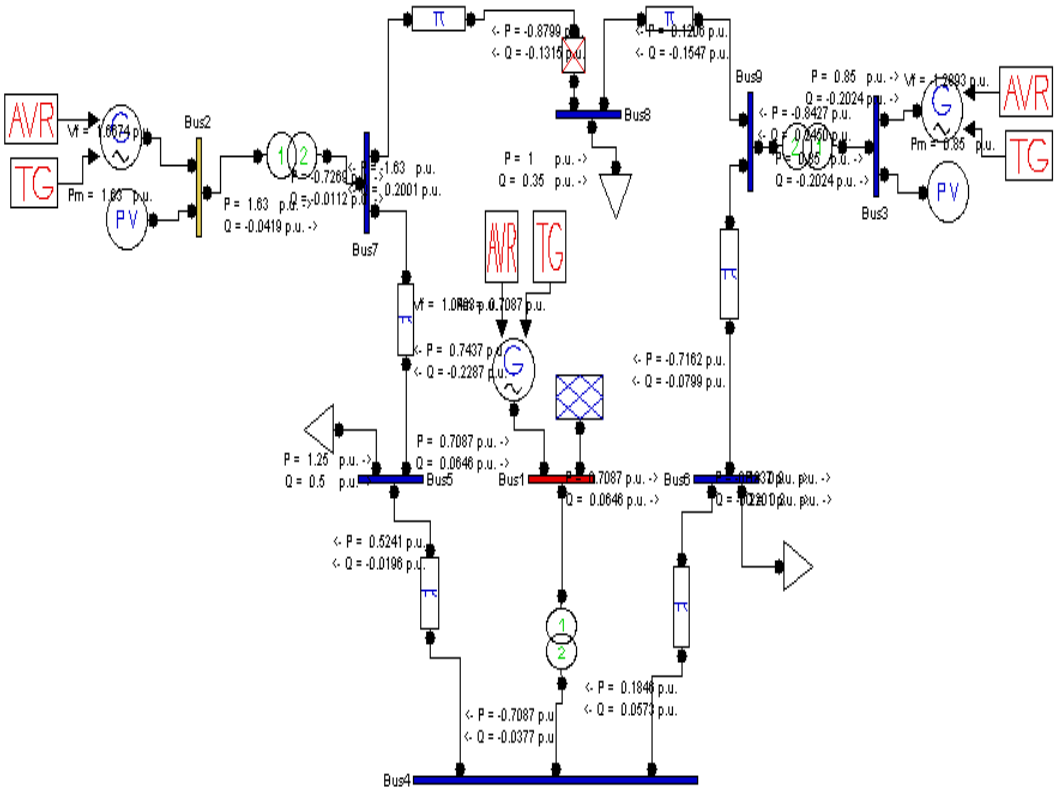



**Figure 5.11** Nine Bus network with Power flow results

To compensate for the losses the extra power is supplied by slack bus, which is a generator. All the values of the powers are in per unit(pu). The static report of the power flow results is shown in Figure 5.12.


**Figure 5.12** Static report of the power flow results

The first column in the static report shows the bus numbers and the next column shows the voltage magnitude on each Bus. The fourth and fifth column shows the real and reactive power at each bus, which is generator power minus load power ($P_g$-$P_L$). The values of the powers and voltage magnitude are all in pu, values in kW and kV can also be obtained. The bottom two columns show the value of the state variables and other variables in the network

The powers (real or reactive) and voltage magnitudes can be plotted to see what is happening at each bus. Figure 5.13 shows the voltage magnitudes at each bus in the network.

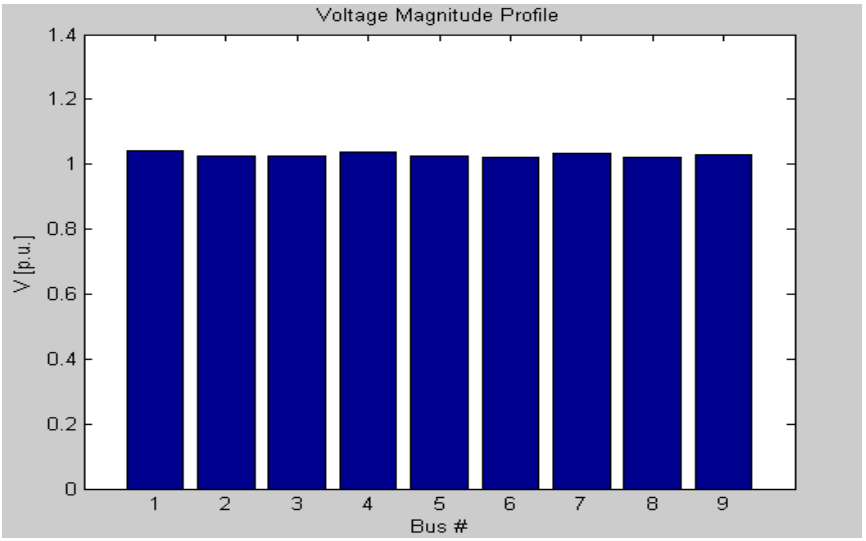



**Figure 5.13** Voltage magnitudes at the Buses in the Network

Similarly the angles at each bus can be plotted; Figure 5.14 shows the angle at the each bus in radians.

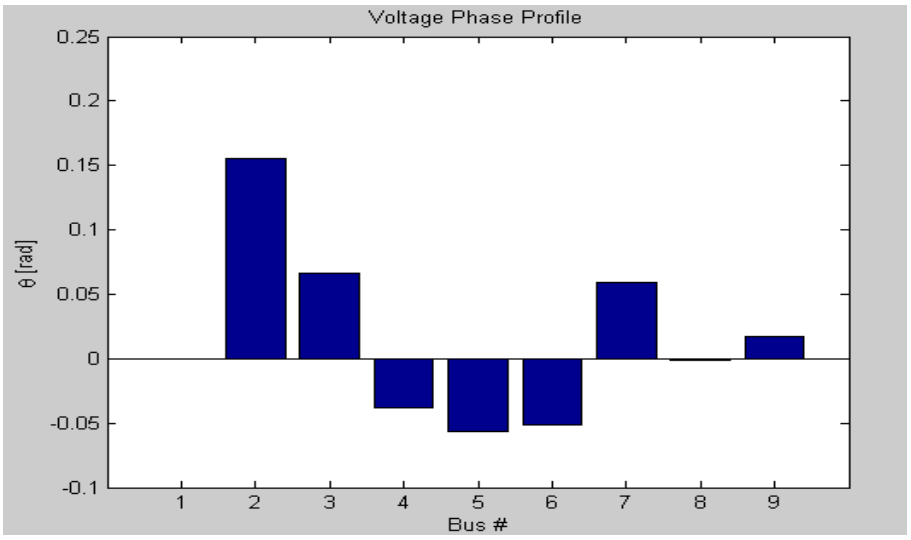



**Figure 5.14 A**ngles (rad) at Buses in the Network.

## 5.4 Conclusions

The power analysis diagram using PSAT of the nine bus system has been explained in this chapter. The power flow results show the normal operation of the system. The voltage at the each bus is plotted showing normal operation. It can be observed that it is easy to design a network using PSAT Simulink Library. The static report shows the powers at the buses and also the voltage magnitude at each bus. In the next chapter time domain simulation is run on the nine bus with three machine system which is designed in this chapter and analysis of results under normal and fault condition is done. The power flow report showing the powers at each bus and power flow in lines is shown in Appendix 2. The total losses in the real and reactive power are also shown, in other words the power flow report gives the detail of the network parameters, the number of components used in the network and the power flow in the network plus power losses in the network.

# Chapter 6

# Results and Analysis

## 6.1 Introduction

In the previous chapter the design of the nine bus network has been explained and the power flow results were shown. In this chapter the time domain simulation is run on the nine bus system with and without the application of fault in the system. The results after running the time domain simulation are plotted and the changes in the results with and without fault are observed. Based on the principle of the Fault Current Limiter, a dummy transmission line is added between the fault and the bus in order to show the effect of impedance of the FCL and to limit the fault current to a lower value using PSAT. To run the time domain simulation on the nine bus system, first the power flow is run and then before running the time domain simulation, the plot variables are selected which we need to plot during or after time domain simulation. Before running the time domain simulation the PQ loads are converted to constant impedance. The Figure 6.1 shows the select plot variables window. The variables to be plotted are selected from the left column of the window.

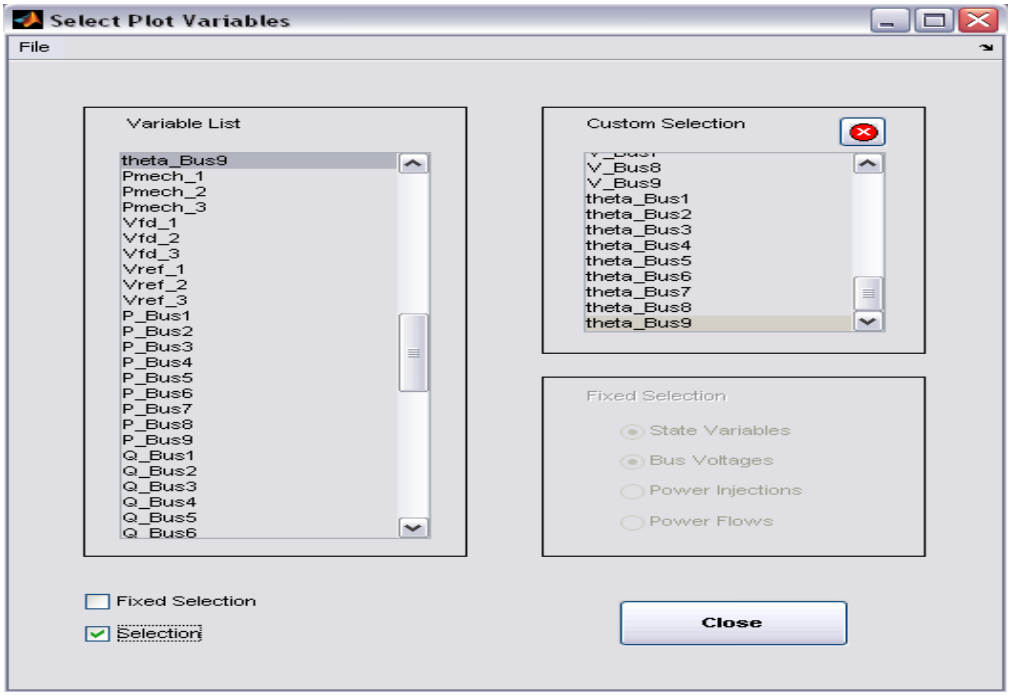


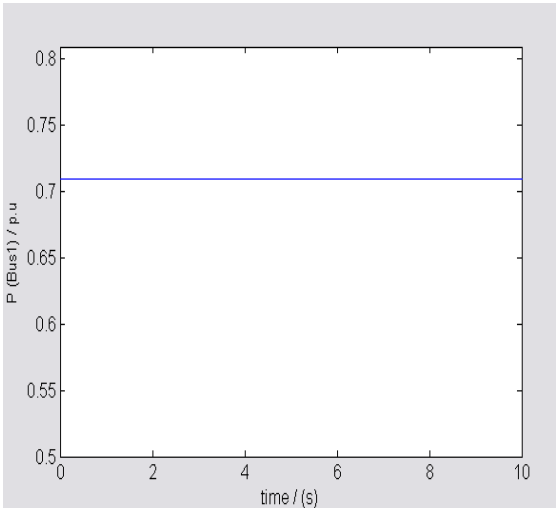

**Figure 6.1** Window for selecting plot variables.

After selecting the variables to be plotted the time domain simulation is run and the selected variables are plotted by clicking the plot button in the main PSAT window. The powers at all the buses in the network are observed under normal and fault condition.

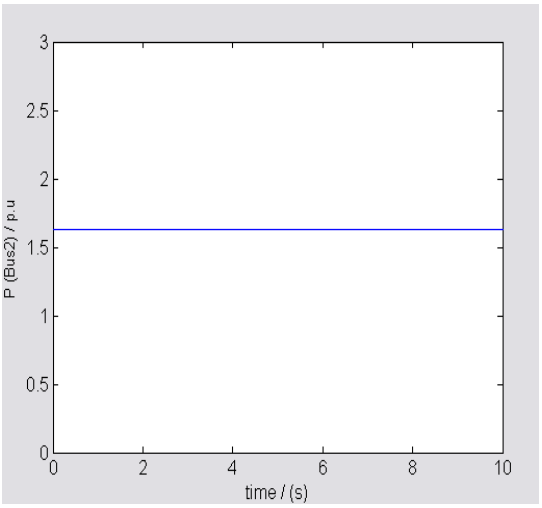
## 6.2 Results during normal operation

On running the time domain simulation on the nine bus system without applying fault, the operation under normal condition is observed.

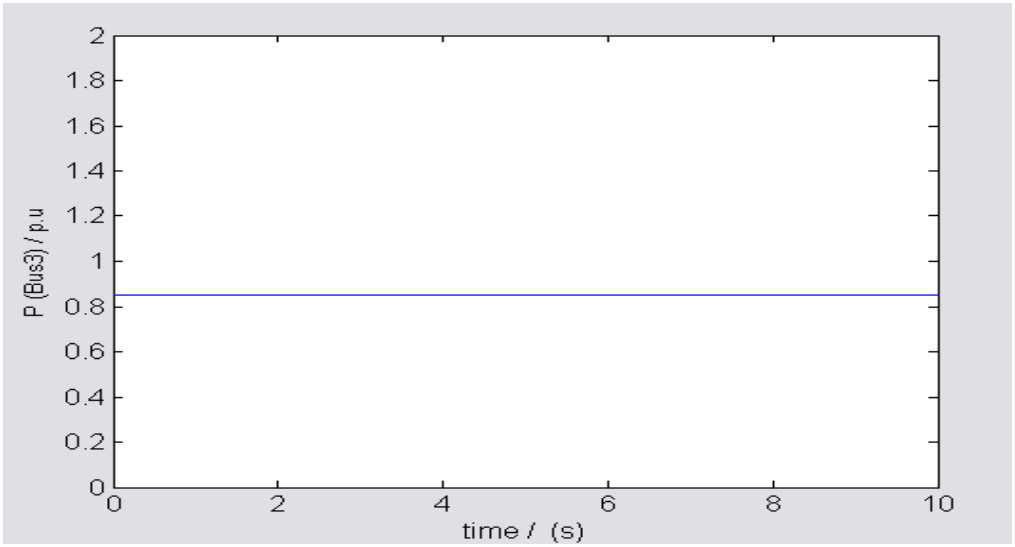
### 6.2.1 Real Power at the Bus 1, 2 and 3




**(a)**




**(b)**

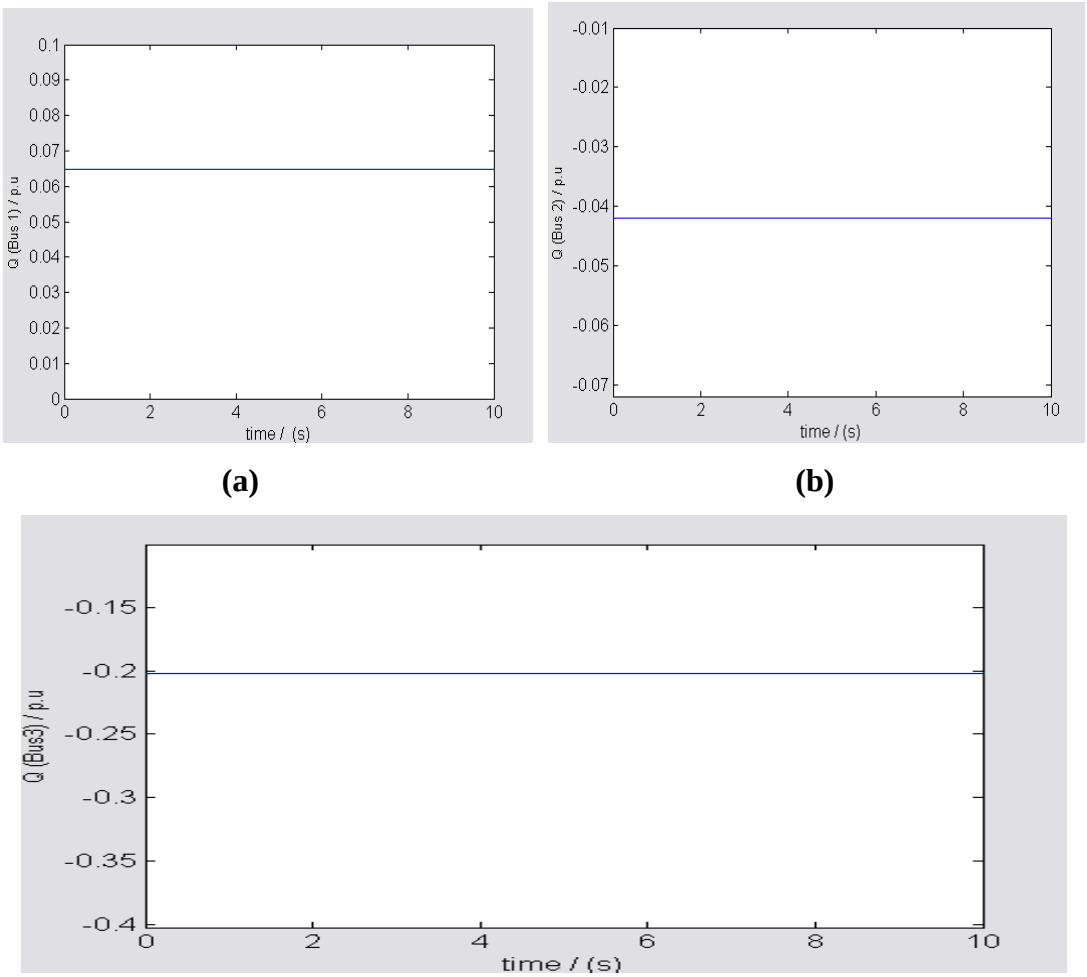



**(c)**

**Figure 6.2** Real Power **(a)** At Bus 1, **(b)** At Bus2, **(c)** At Bus 3

From the above Figure 6.2, a constant and continuous real power flow is observed at the buses 1, 2 and 3. All of the three buses have synchronous generators. All the powers are expressed in per unit with a base power of 100MVA. The synchronous generator at bus1 has ratings 100MVA and 16.5KV, the synchronous generator at bus 2 has ratings 100MVA and 18KV and the synchronous generator at bus 3 has ratings 100MVA and 13.8KV. The results shown in the above Figure 6.2 are during normal operation. From the nine bus network shown in the previous chapter, it can be seen that transformers are connected to buses which are connected to the synchronous generators in order to set up the generated voltage to 230KV. Similarly the reactive power at the buses 1, 2 and 3 is plotted, to see the reactive power generated at these buses.

### 6.2.2 Reactive Power at the Bus 1, 2, and 3



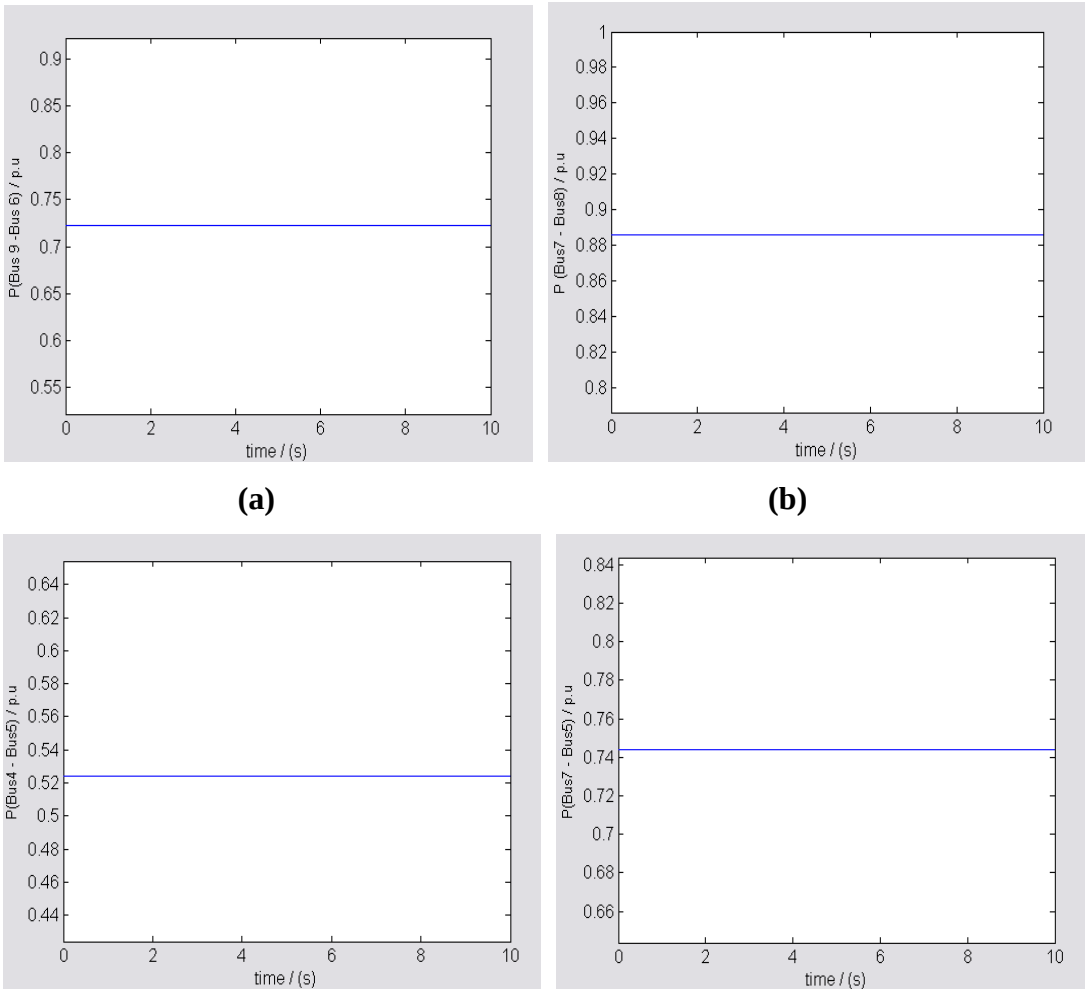

**(a)** **(b)**

**(c)**

**Figure 6.3** Reactive Powers **(a)** at Bus 1, **(b)** at Bus2, **(c)** at Bus 3

The time domain simulation is run for 10 seconds as shown in the above Figures 6.2 and 6.3. The negative and positive sign of the reactive power show the flow of the power into and out of the bus. From Figure 6.3 it can be seen that continuous power is flowing at the buses. Figures 6.2 and 6.3 show the real and reactive powers at buses 1, 2 and 3. Now we will see the power flowing in the transmission lines between the two buses during normal operation. Similarly the power between two buses is plotted, as it is shown in Figures 6.4 and 6.5. As there is no fault applied in the system, constant and continuous power should be flowing between the buses. After running power flow and before performing time domain simulation the plot variables which are power flows between the buses are selected. The real power flow between the buses is shown in Figure 6.4

### 6.2.3 Real Power Flow in the Transmission lines




**(a)** **(b)**

**(b)** (d)

**Figure 6.4** Real Power flow **(a)** from Bus 9 to 6, **(b)** from Bus 7 to 8, **(c)** from Bus 4 to 5, **(d)** from Bus 7 to 5.

The real power between the buses is shown in Figure 6.4. Figure 6.4 (a) shows the power flow from bus 9 to bus 6. It is possible to plot the power flow from bus 6 to bus 9 but in this case the power flow will be -0.725 p.u. Similarly the power flow from bus 7 to bus 8, from bus 4 to bus 5 and from bus 7 to bus 5 is also shown in the above Figure 6.4. Power is flowing from one bus to another showing the normal operation of the system. There is also continuous power flow between bus1 and bus 4, between bus 8 and bus 9 and between bus 4 and bus 6 (not shown in Figures).

### 6.2.4 Reactive Power Flow in the Transmission lines

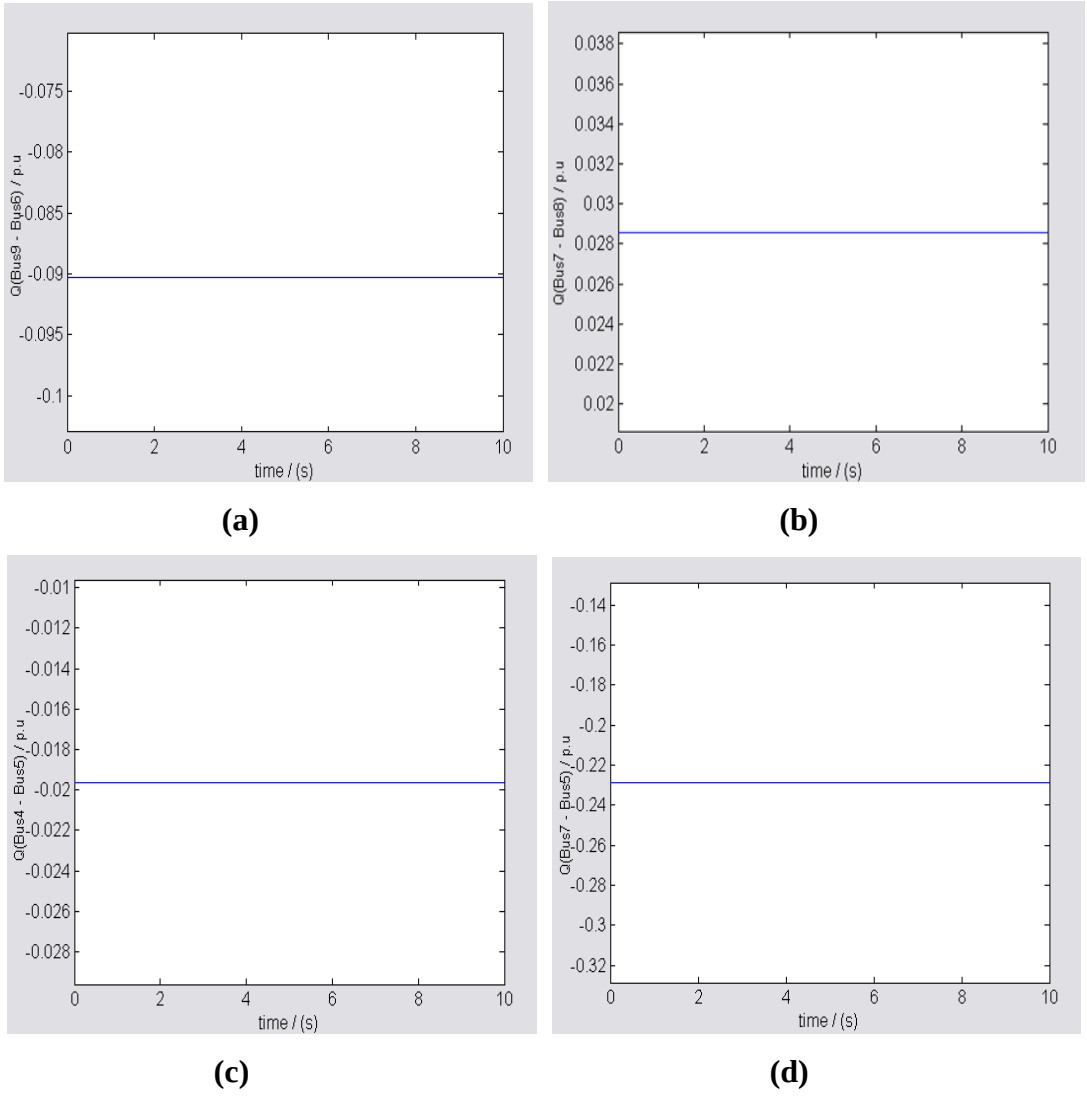



**Figure 6.5** Reactive Power flow **(a)** from Bus 9 to 6, **(b)** from Bus 7 to 8, **(c)** from Bus 4 to 5, **(d)** from Bus 7 to 5.

Figure 6.5 shows the flow of reactive power from one bus to another. Figure 6.5(a) show the reactive power flowing between bus 9 and bus6, it can be seen that the value

of the power flow has negative magnitude which means the reactive power is flowing from bus 6 to bus 9. The value of the reactive power depends on the type of the load connected. If the load is inductive, the demand of the reactive power will be high. Due to the inductive load the power factor of the system will decrease, causing the current to lag behind the voltage. In order to avoid this condition, there should be a capacitor bank in the system which compensates for the lagging power factor and keep the power factor near unity. The capacitor bank has not been installed in the nine bus system because the loads are not highly inductive. Figure 6.6 shows the voltage magnitude at some of the buses in the system during normal operation.

### 6.2.5 Voltage magnitude at the Buses

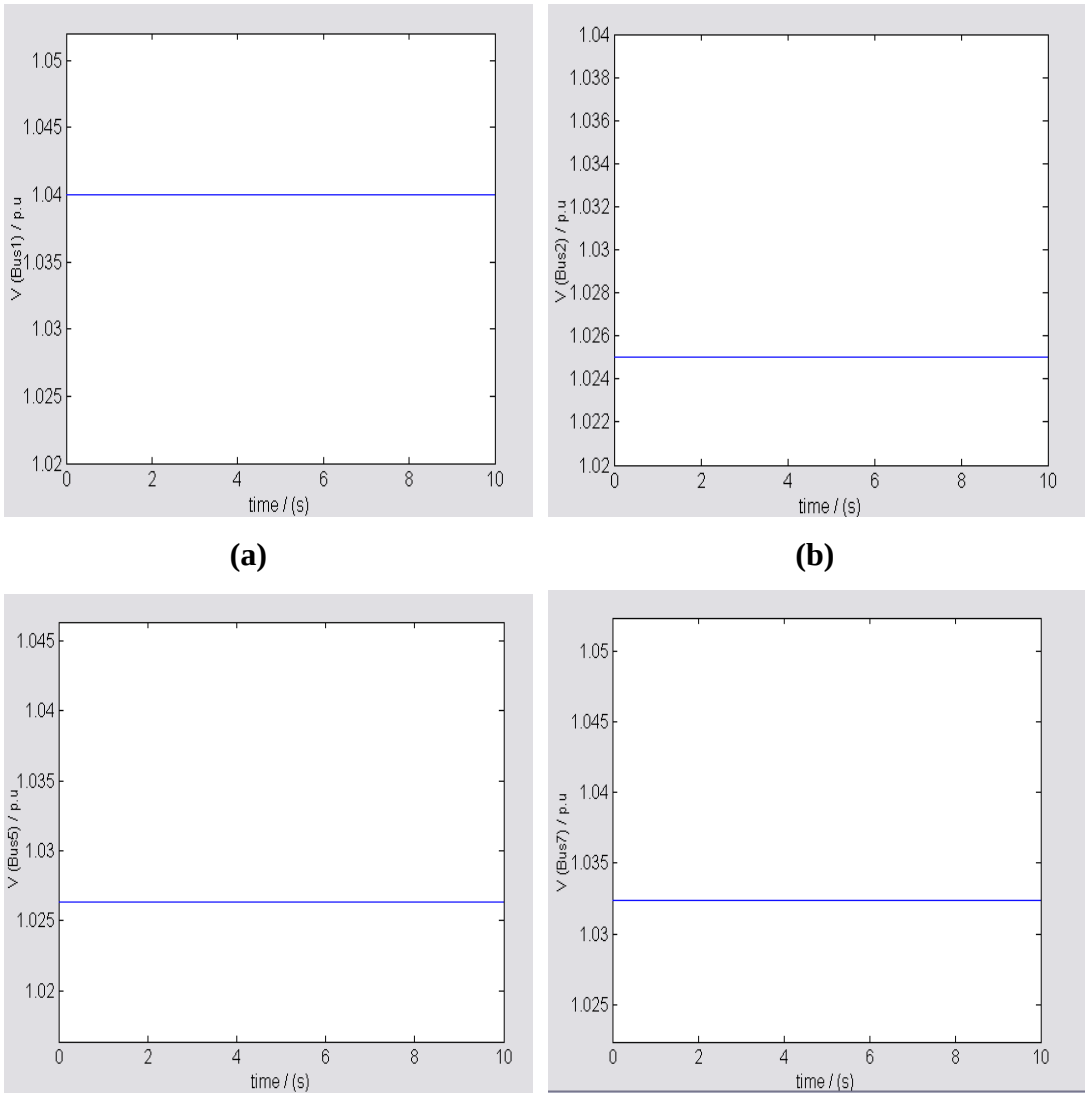


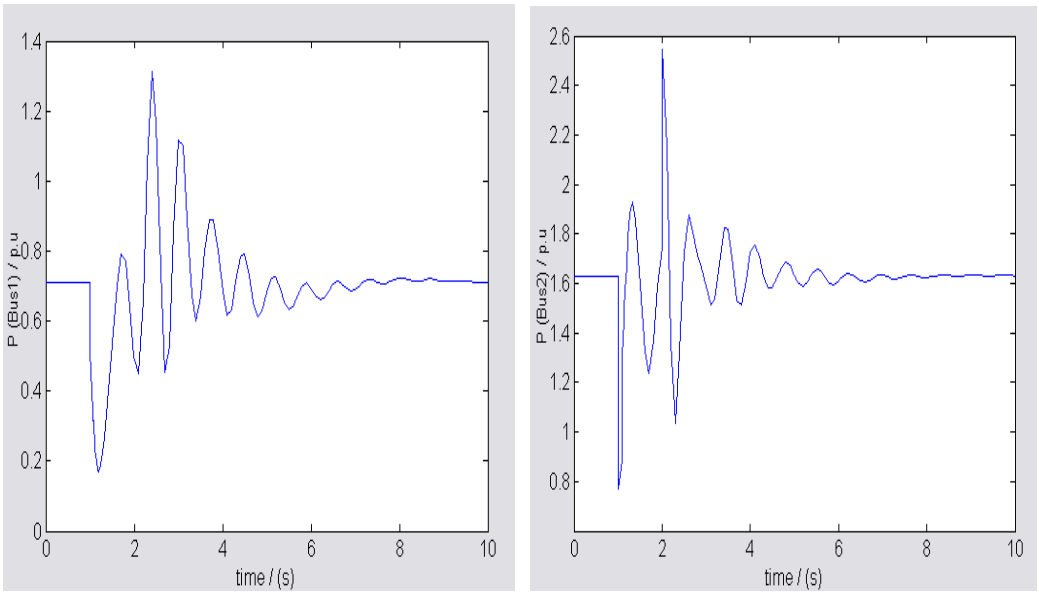

**Figure 6.6** Voltage magnitudes **(a)** at Bus 1, **(b)** at Bus 2, **(c)** at Bus 5, **(d)** at Bus 7

The voltage is constant at the buses during normal operation. The results shown in Figures 6.2 to 6.6 are during normal operation, a constant and continuous flow of power and voltage is observed.

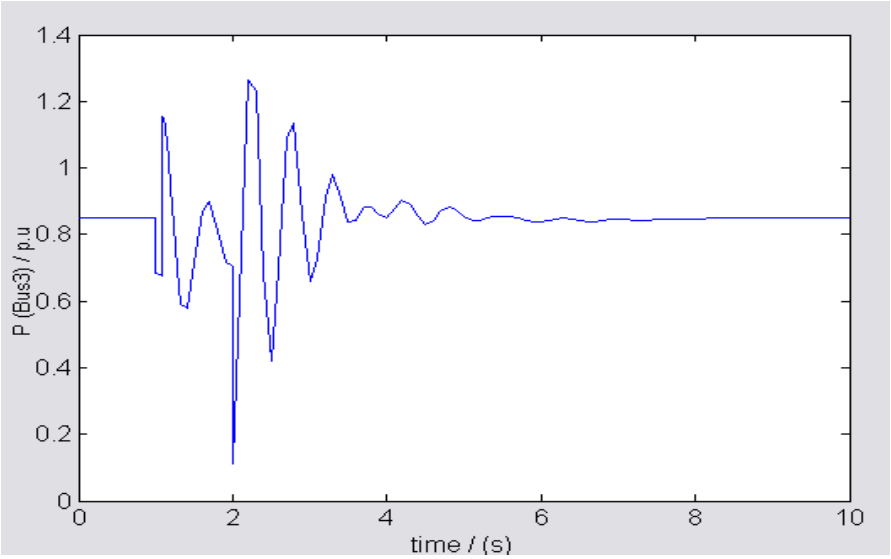
## 6.3 Results during fault in the system

### 6.3.1 Real Power at Bus 1, 2 and 3

On applying a fault at bus 7, as shown in Figure 5.2 in the previous chapter, the real power at the buses 1, 2 and 3 is shown in Figure 6.7. The fault time is 1 second and the fault clearing time is 1.083 seconds. The first intervention time for the circuit breaker is 1.083 seconds and the second intervention time, which is reclosing of the circuit breaker, is 2.0 seconds. From Figure 6.7 it can be seen that the power at the buses did not remain constant after one second, because the fault is applied at one second. It can be observed that there is a lot of disturbance between the time one second and three seconds. Even though the circuit breaker recloses at 2.0 seconds, due to synchronous generators at these buses, the time taken to come back to normal operation is longer than the power flow in the transmission lines which is shown later in this chapter.




**(a)** **(b)**



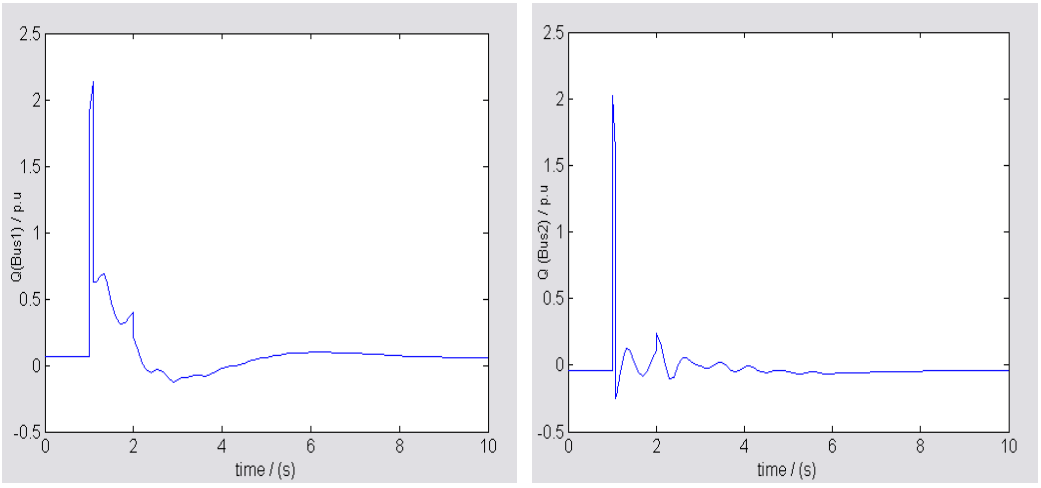

**(c)**

**Figure 6.7** Real Power, during fault on Bus 7 **(a)** at Bus 1, **(b)** at Bus 2, **(c)** at Bus 3

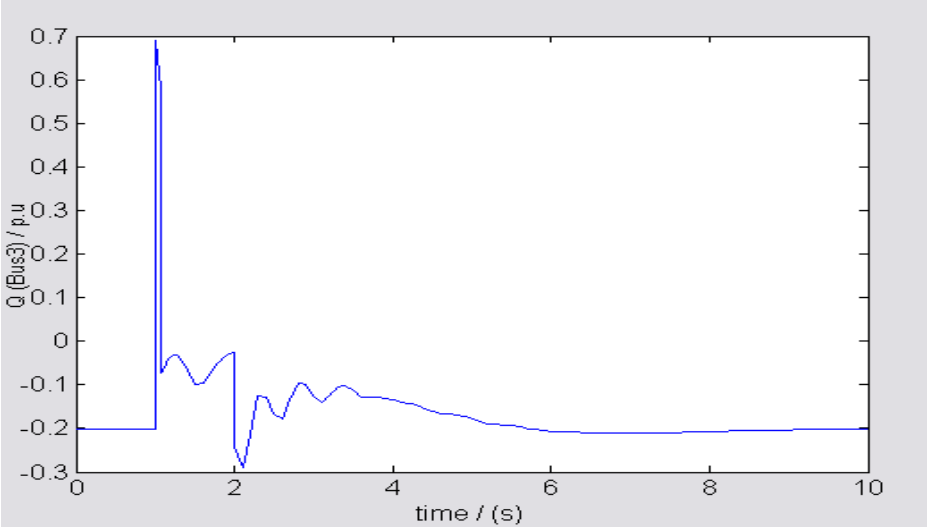
The reactive power at the Buses 1, 2 and 3 are shown in Figure 6.8.

### 6.3.2 Reactive Power at Bus 1, 2 and 3

It can be observed from Figure 6.8, which shows the reactive power, that the fault clearing time is 1.083 seconds. The reactive power at bus 1, 2 and 3 rises to a very high value at 1.00 second and comes back to a lower value at 1.083 which is fault clearing time. From the reactive powers shown in Figure 6.8 we can estimate that current will rises to a very high value as reactive power rises to high value during fault. The reactive power indirectly shows the current in the system. After two seconds the reactive power at bus 1, 2 and 3 comes back to original value which it was before fault.




**(a)** **(b)**



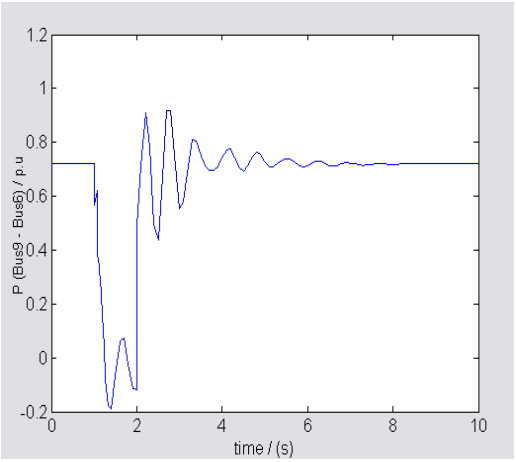

**(c)**

**Figure 6.8** Reactive Power, during fault on Bus7 **(a)** at Bus 1, **(b)** at Bus2, **(c)** at Bus3

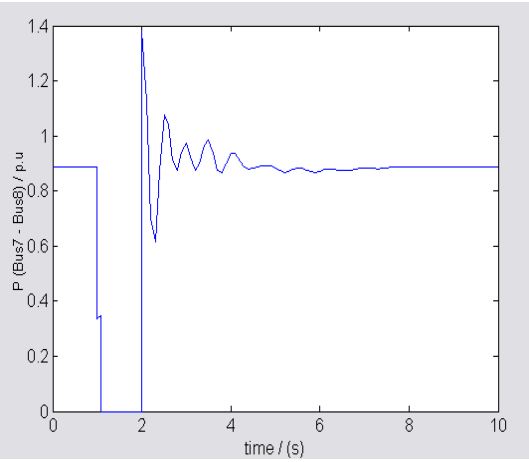
The time taken to come back to normal operation depends on the equipment connected at that bus. The flow of real and reactive powers between the buses is shown in Figures 6.9 and 6.10.

### 6.3.3 Real Power Flow in the Transmission lines

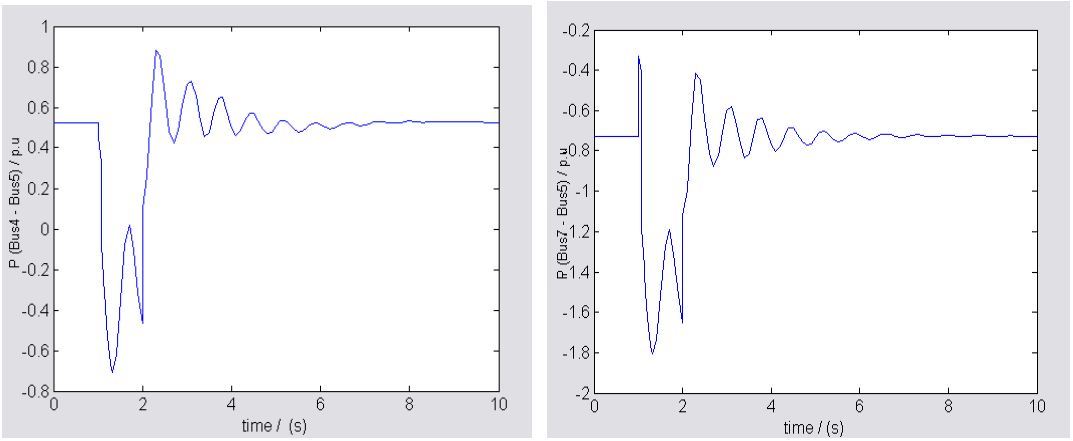
The behaviour of real power flow in the transmission lines or between the buses is shown in Figure 6.9. It can be seen that when the fault is applied at one second the real power decreases sharply to a lower value and becomes zero in Figure 6.9(b) because of circuit breaker in that line. In some of the transmission lines the real power decreases to a negative value during fault, which means the flow of the real power starts flowing in opposite direction to before fault.




**(a)**




**(b)**



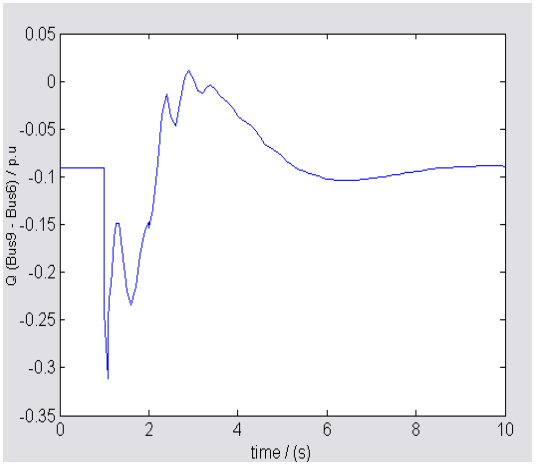

**(c)** **(d)**

**Figure 6.9** Real Power flow, during fault on Bus 7 **(a)** from Bus 9 to 6, **(b)** from Bus 7 to 8, **(c)** from Bus 4 to 5, **(d)** from Bus 7 to 5.

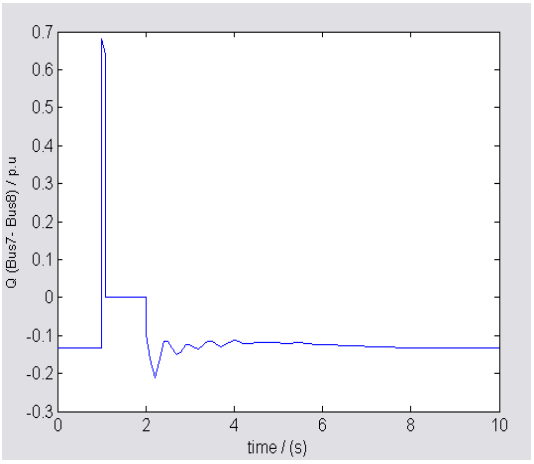
Similar results are observed in the other lines. It can be observed that on the buses or in the transmission lines near to bus 7 there is considerable decease in real power compared to the buses or the transmission lines which are far away from bus 7. Figure 6.9(a) which shows the real power flow between bus 9 and bus 6 far away from bus 7 where the fault is, the decrease in power is less than the decrease in power flow between bus 4 and bus 5 and between bus 7 and bus 5.

### 6.3.4 Reactive Power Flow in the Transmission lines

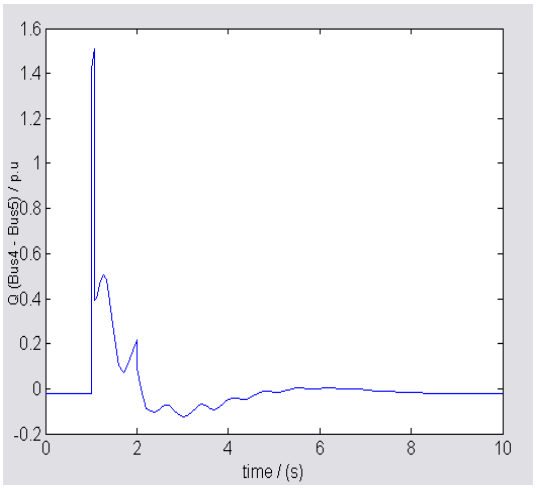
During fault the reactive power in the transmission lines increases to a high value. The increase in reactive power means there is considerable fault current flowing in the system, which may damage the equipment installed in the system, such as the circuit breaker, transformers, and generators etc. It can be seen that there is a sharp increase in the value of reactive power during fault, which is very high as compared to the value of reactive power during normal operation. The value of the fault current is calculated in the next section. The rise in the reactive power is more near to bus 7 as compared to the area far away from bus 7. The first intervention time of the circuit breaker is 1.083 seconds, which is also fault clearing time. Because of this the reactive power in Figure 6.10(b) becomes zero at 1.083 seconds and at the same time the circuit breaker opens. After 2 second the power between bus 7 and bus 8 comes to normal value because the circuit breaker recloses at 2 seconds.



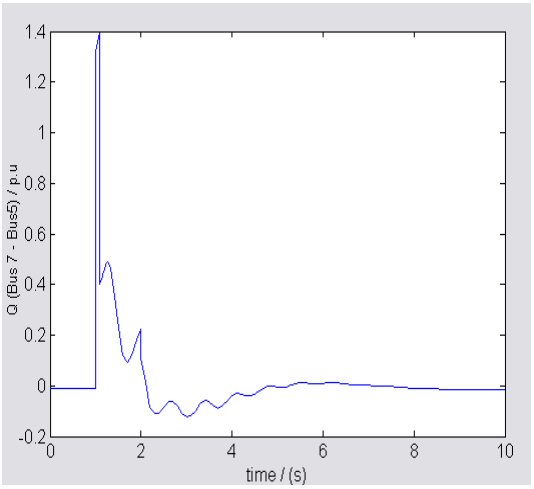

**(a)**




**(b)**



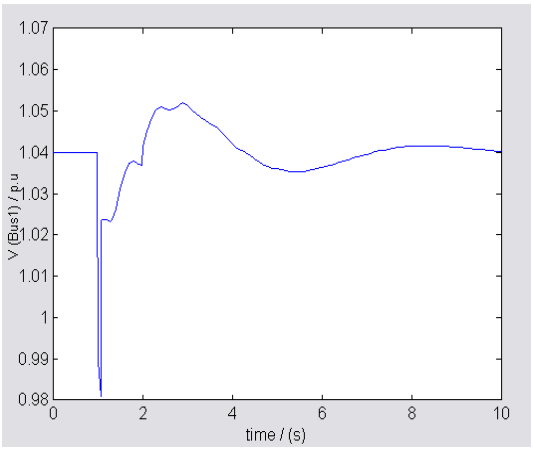

**(c)**



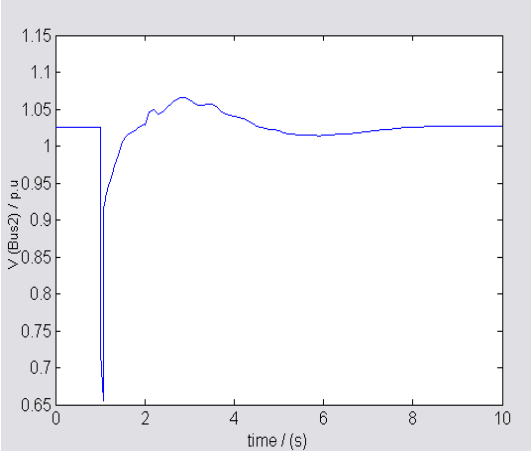

**(d)**

**Figure 6.10** Reactive Power flow during fault on Bus 7 **(a)** from Bus 9 to 6, **(b)** from Bus 7 to 8, **(c)** from Bus 4 to 5, **(d)** from Bus 7 to 5.

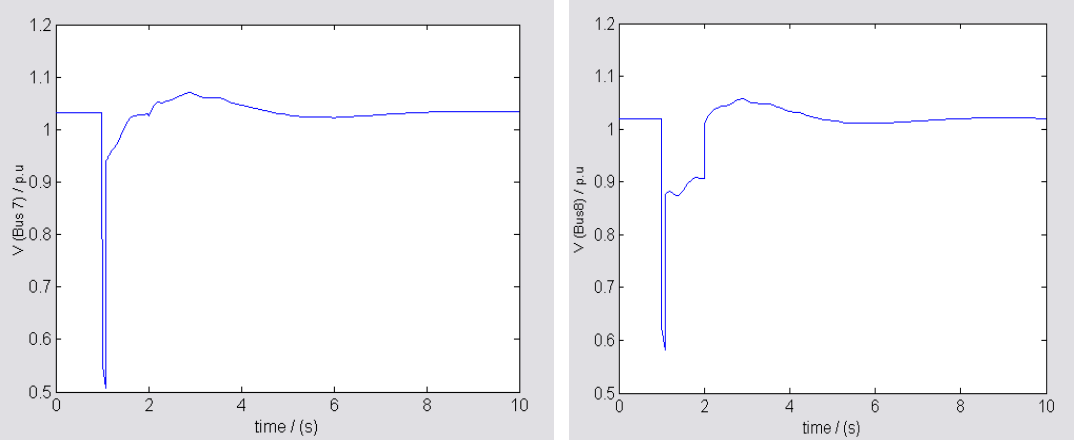
### 6.3.5 Voltage magnitude at the Buses




**(a)**




**(b)**




**(c)** **(d)**

**Figure 6.11** Voltage magnitudes, during fault on Bus7 **(a)** at Bus 1, **(b)** at Bus 2, **(c)** at Bus 7, **(d)** at Bus 8

From the above Figure 6.11, we see that the voltage at the buses decreases to a very low value during fault and once the fault is cleared the voltage return to its normal value. But the voltage at bus 8 remains at zero, even after the fault is clear at 1.083 seconds because the circuit breaker opens at 1.083 seconds and it recloses at 2.0 seconds, so after 2.0 seconds the voltage returns to its normal value. The time taken to return to normal value depends how much time is taken to bring the generators in synchronism, which is done by the TG blocks in the network. Similarly the voltage is decreased to a lower value at other buses in the network. The voltage during fault deceases to a very low value and the reactive power during fault increases to a high value. This means the current in the network during fault will increase to a very high value, which is called fault current.

## 6.4 Optimal location of the Fault Current Limiter

To locate the best position for the Fault Current Limiter in the nine bus network, the value of the current at each bus during fault is calculated. In the present version of PSAT it is not possible to calculate the value of the current in the network. The value of the current in the network at each bus is calculated from the values of real and reactive power at that bus.

The value of the current, ***I***, is calculated as follows,

Real Power = $P = V I \cos\phi$

Reactive Power = $Q = V I \sin\phi$

Voltage Magnitude = ***V,***

Now,

Apparent Power, $S = V I = \sqrt{P^2 + Q^2}$

Current, $I = S/V$. (6.1)

Using the above expression, the value of the current at each bus is calculated. The value of the current is expressed in per unit. To find the optimum location of the Fault Current Limiter, the position of the Fault Current Limiter nearest to the bus with the highest value of current during fault is selected. From Expression 6.1 the value of the current is calculated and, the value of the current at each Bus is shown in Figure 6.12. The current shown in Figure 6.12 is the r.m.s value.

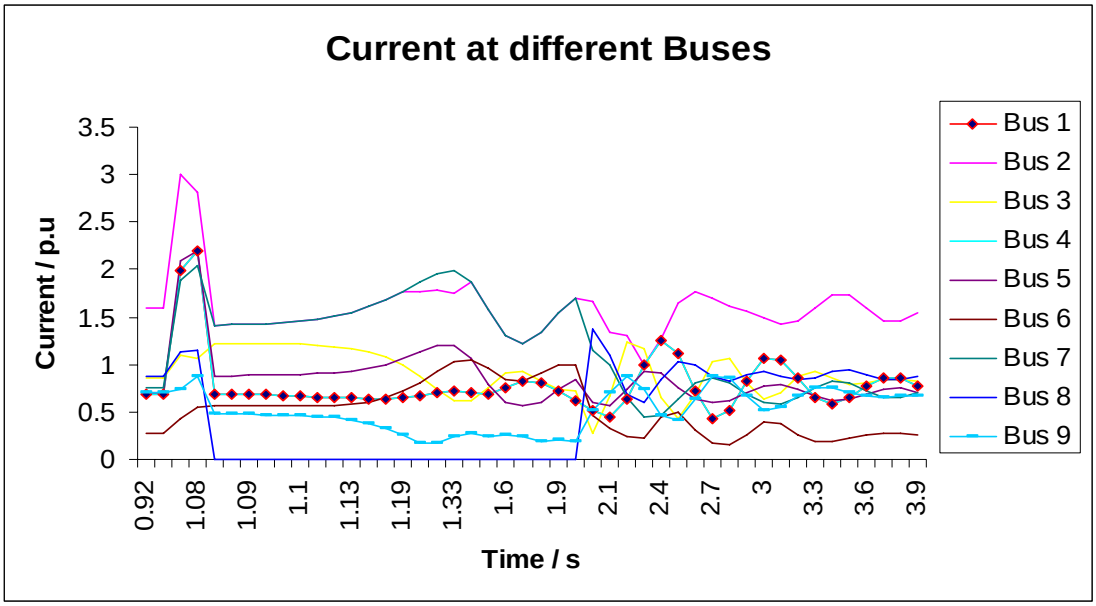



**Figure 6.12** Current at different Buses during fault at Bus 7

Now we observe the fault period, which is between 1.00 seconds and 4.00 seconds because the disturbance lasts more than the fault clearance time, the value of the current during this period is calculated and analysed. The current during fault at all the nine buses is shown in Figure 6.12. It is observed that the fault current is highest on the bus 2, bus 7, bus 4, bus 5 and also bus 1, because these buses are near to fault

position, which is at Bus 7. The buses which are less affected by the fault are bus 9, 6, 3 and 8. The fault current on theses buses is not very high compared to the value of the fault current on the other buses in the network. Even thought bus 8 is connected to bus 7, the value of the fault current is not too high, because the circuit breaker in that line opens and the current becomes zero until it recloses at 2.0 seconds as shown in Figure 6.12. The fault clearance time is 1.083 seconds and it can be seen that the current at each bus return to normal value after that. However there is also some disturbance at time 2.00 seconds because the circuit breaker recloses then and the generators have to supply more power. When all the three generators come in synchronism with each other, the current returns to its normal value. If we see from Figure 6.12 the optimal location of the Fault Current Limiter would be near bus 7, because it will limit the current during fault.

Based on the principle of Fault Current Limiter, the impedance of the FCL increases during fault, which limits the current during fault. To show the affect of the increase in impedance during fault, a dummy line is added between bus 7 and fault. Bus 10 is also added between bus 7 and fault, because PSAT does not allow us to connect fault to the transmission line. The dummy line is shown in Figure 6.13.

### 6.4.1 Nine Bus system with Dummy line

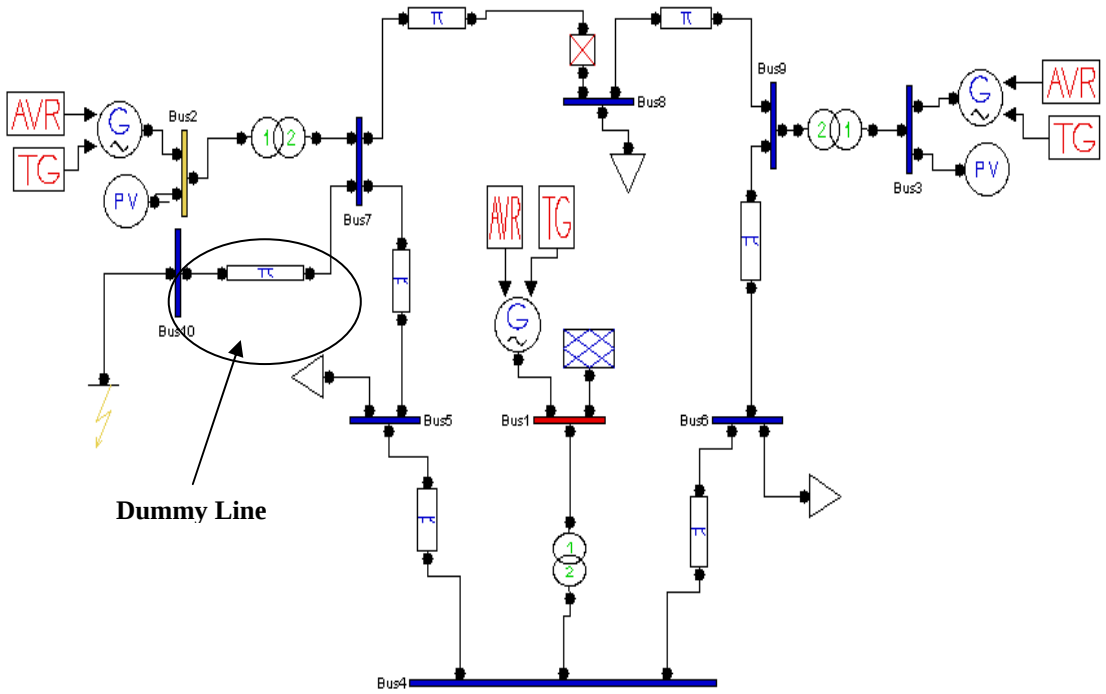



**Figure 6.13** Nine Bus System with Dummy line at Bus 7

The addition of the dummy line in the nine bus system is shown in the above Figure 6.13. The impedance of the dummy line is increased, to lower the fault current during fault. The current during fault is calculated and shown in Figure 6.14.

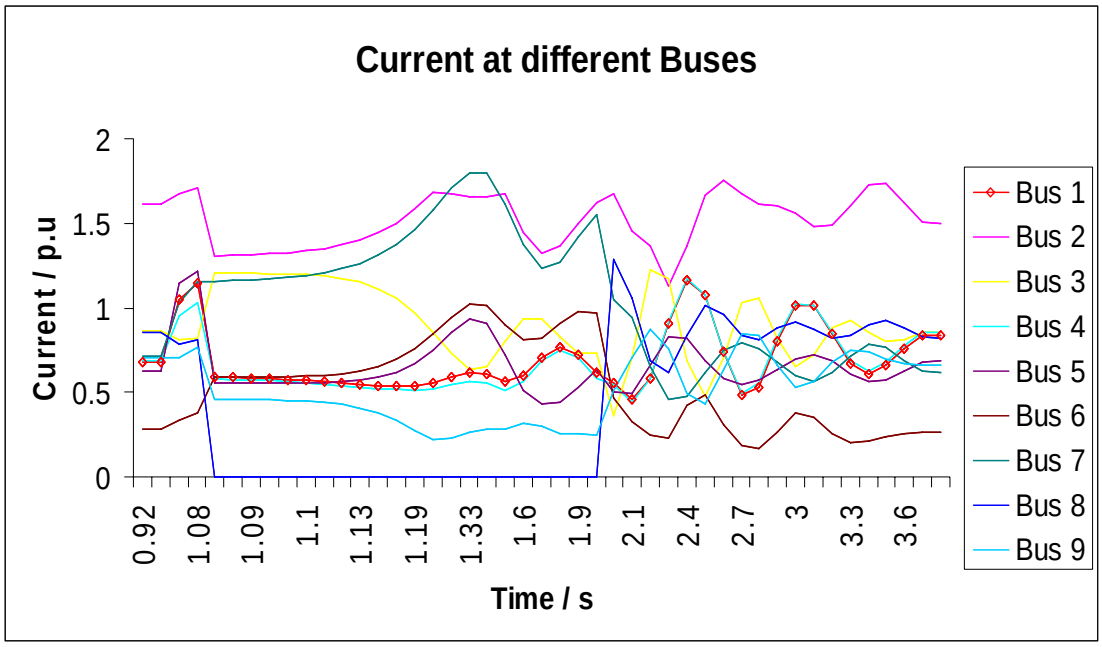



**Figure 6.14** Fault Currents reduced at different Buses with Fault at Bus 7

Increasing the impedance of the dummy transmission line, (the line between fault and bus 7), the current during fault is considerably reduced to a lower value as shown in Figure 6.14. The fault time is 1.00 seconds and the fault clearing time is 1.803 seconds. The current during this period was very high before the increase in the impedance between the fault and bus 7 as shown in Figure 6.12. The fault current on bus 2 is 3 p.u, which is very high to damage the equipment installed in the system because the current during normal operation is 1.5 p.u. on bus 2. From Figure 6.14 it can be seen that the fault current is considerably reduced to a lower value close to its value during normal operation. Similarly the fault currents are reduced at bus 7, 4, 5 and 1. The current at bus 2, 7, 5 and 6 increases slightly after they are reduced during fault. The Fault Current Limiter cannot be kept in its high impedance state for too long. The Fault Current Limiter switches to high impedance state during fault, it does not require any external source to perform its operation, and this depends on the value of the current. For fault on bus 7, the optimum position of the FCL or HTSFCL would be around bus 7. From Figure 6.14 it can be observed that the fault current at the

buses around bus 7 is considerably reduced compared to the values of the fault current in Figure 6.12.

In the next section we will change the position of the fault in the system and apply the fault at bus 9. The current at each bus is again calculated and plotted. In order to show the affect of the increased impedance during fault, a dummy line is added between the fault and bus 9.

### 6.4.2 Nine Bus system with fault at Bus 9

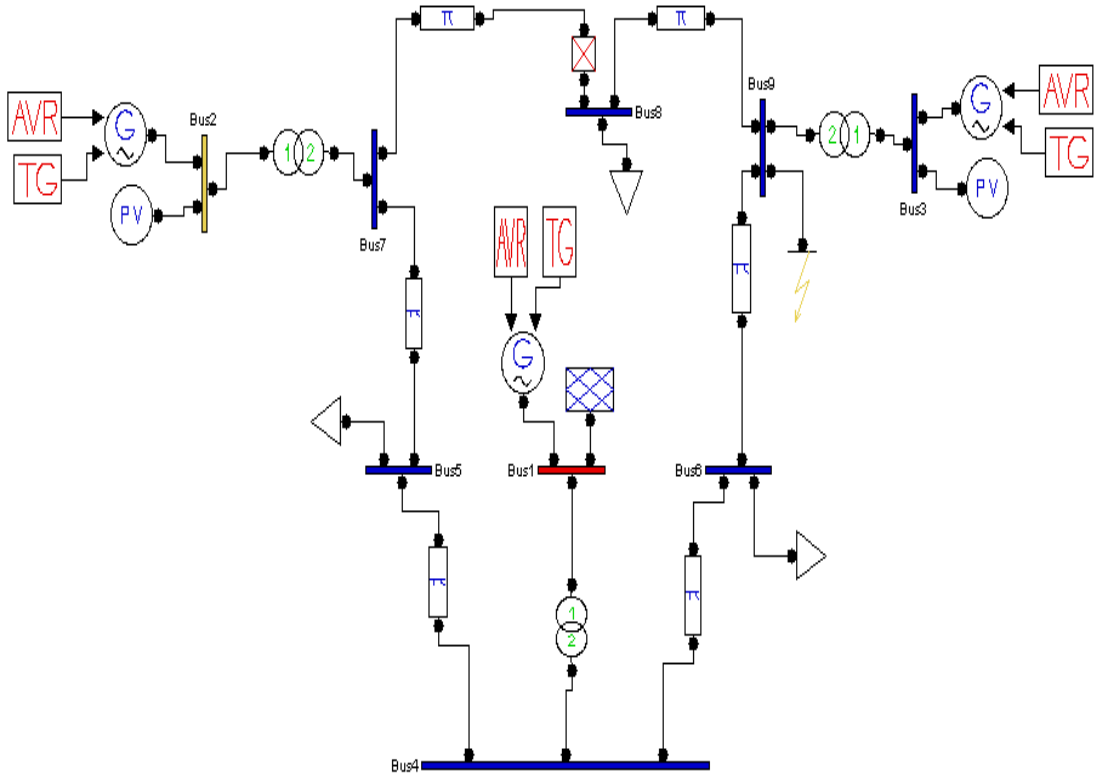



**Figure 6.15** Nine Bus Network with Fault at Bus 9

By changing the position of the fault from bus 7 to bus 9, the current during fault is calculated and analysed. The fault time is the same as it was on bus 7 that is 1.00 seconds and the fault clearing time is 1.083 seconds. In this case the circuit breaker between bus 7 and bus 8 is not operated during fault. The fault current at each bus is shown in Figure 6.16. The current during fault is very high on bus 9, followed by bus 3, bus 4 and bus 6. The area near the fault is more affected than the area far away from the fault.

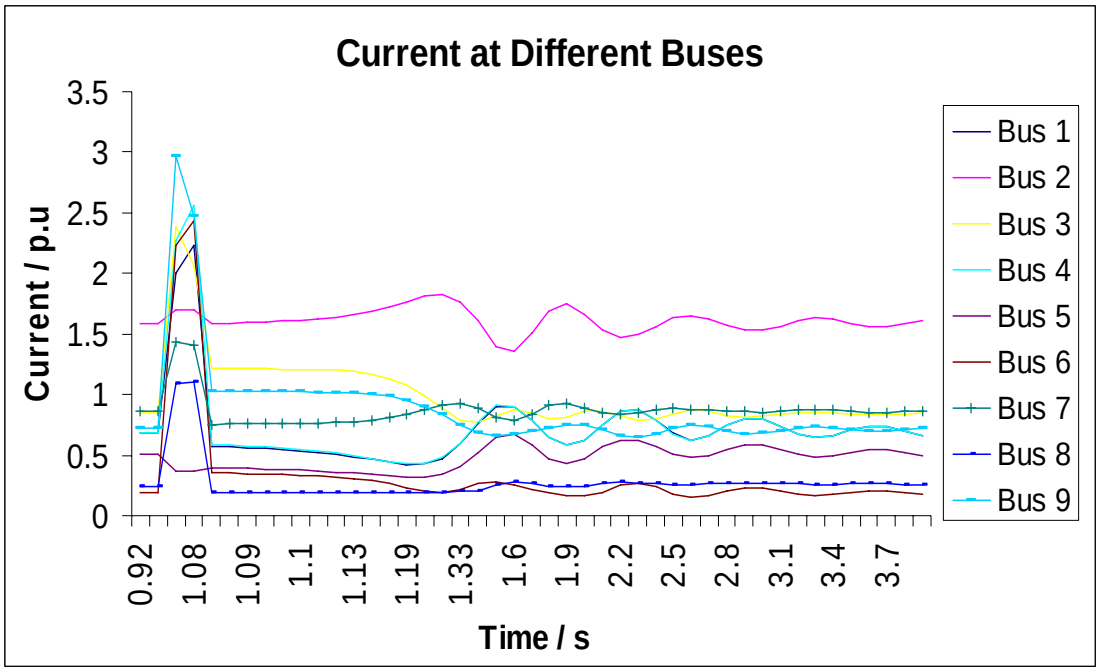



**Figure 6.16** Fault Current during fault at Bus 9

The least affected buses are 5, 7 and 2 which were the most affected when the fault was on bus 7. As the circuit breaker is not operated and the current at each bus return to normal value after the fault is cleared. Bus 1 is affected in both cases, when the fault was at bus 7 and also when the fault is at bus 9. Bus 4 is also affected during both cases. Bus 2 had the highest current and bus 3 was the least affected when the fault was on bus 7 but when the fault is applied on bus 9, bus 2 is the least affected and bus 3 has the high value of current during fault. It can be concluded that the area around the fault is the more affected than the area far away from the fault. The generator at bus1 has a generating voltage of 16.5KV and the generator at bus 3 has a generating voltage of 13.8KV. There is a lot of disturbance on these generators during fault at bus 9. Now we will add a dummy line between the fault and bus 9 with high impedance, to reduce the current during fault.

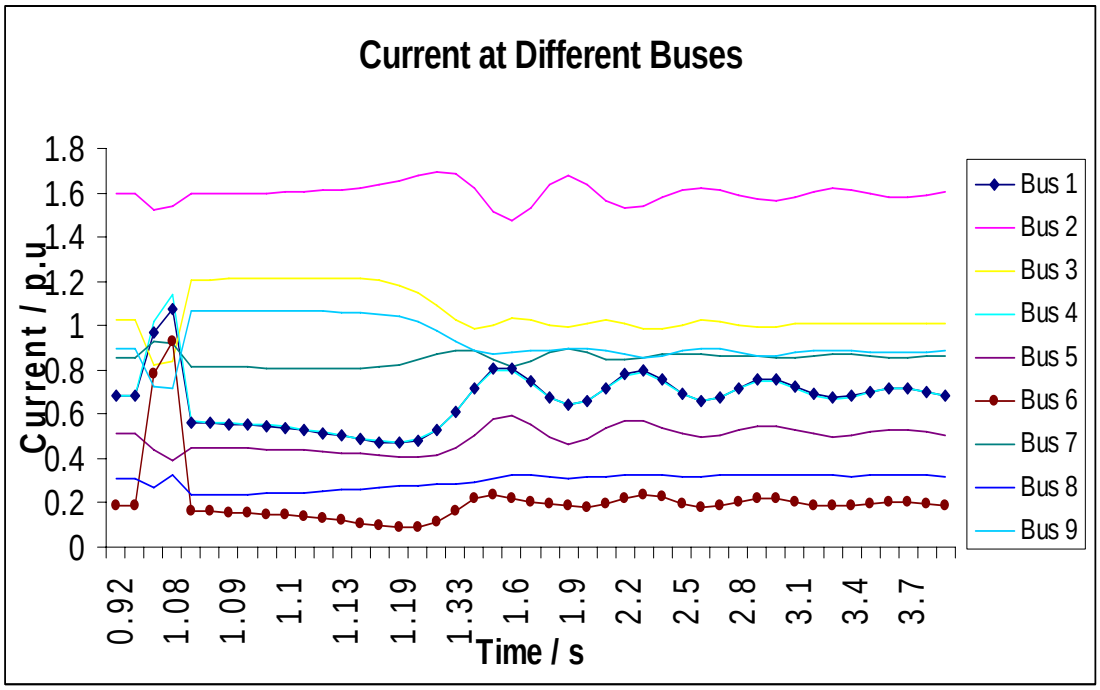



**Figure 6.17** Fault Currents reduced at different Buses with Fault at Bus 9

By adding a dummy line between the fault and bus 9 and the impedance of the dummy line increased due to which the current during fault is reduced to lower value as shown in Figure 6.17. If we compare the fault currents in Figure 6.16 with the fault currents in Figure 6.17, the fault current at bus 9 which was very large has been reduced and similarly the fault currents are reduced at bus3, 4, 8, 6 and at 1. The current at bus1 and bus 4 are same because the generator at bus1 also supplies power to bus 4. The generators at the buses take time to come back into synchronism after disturbance, as can be seen in Figure 6.17. The turbine governor (TG) tries to bring the generators back in synchronism within a short period of time. The value of the fault current at bus 6 is little bit high but if we compare it with the value in Figure 6.16, it is very much reduced. In the next section we will again change the position of the fault, from bus 9 to bus 4.

### 6.4.3 Nine Bus System with fault at Bus 4

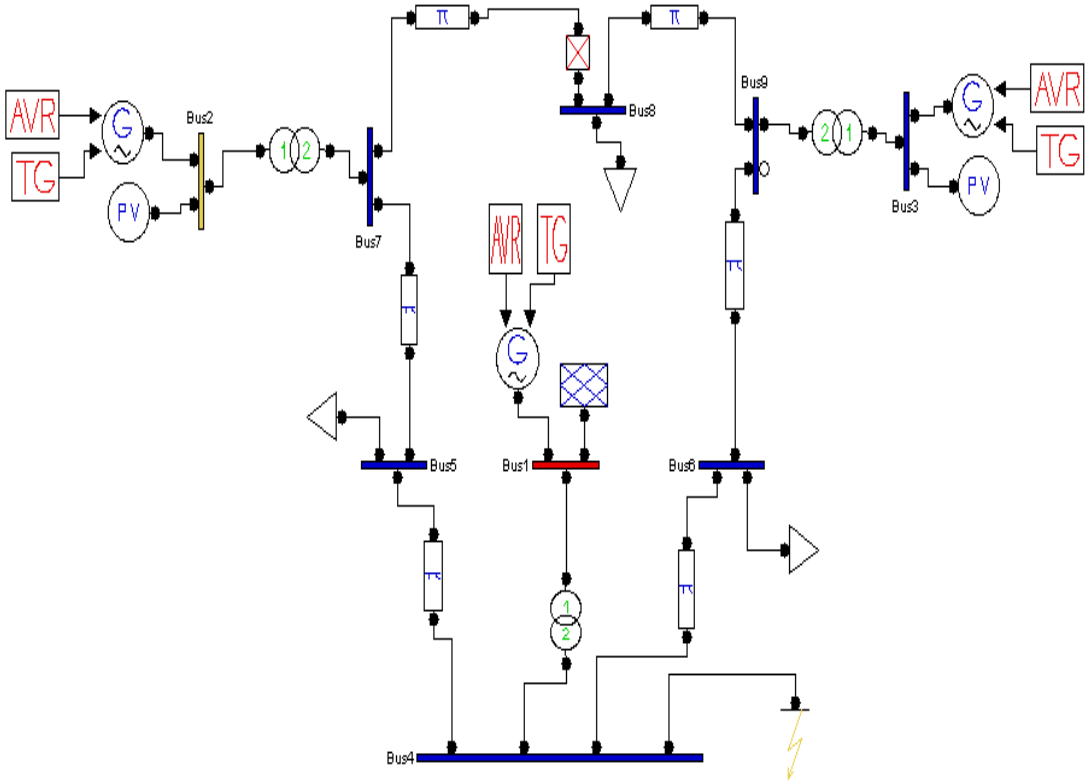



**Figure 6.18** Nine Bus Network with Fault at Bus 4

The above Figure 6.18 shows the network with a fault at bus 4. The buses connected to the bus 4 are bus 5, bus1 and bus 6. Similarly to the above cases the fault current is calculated at each bus. The fault currents at all buses are shown in Figure 6.19.

During fault at bus 4, the most affected bus is bus 1 as shown in Figure 6.19. There is a slight rise in the current at bus 4 and bus 6. We saw in the previous cases (with the fault was on bus 7 and bus 9), the fault current rushes towards the sources. The nearest source to bus 7 was bus 2 and for bus 9 was bus 3, so these two buses have the highest current during fault near to them. Bus1 has one synchronous generator and a slack bus; due to the fault on the bus 4 the maximum fault current rushes towards the bus1 so the value of the fault current is very large on bus1.

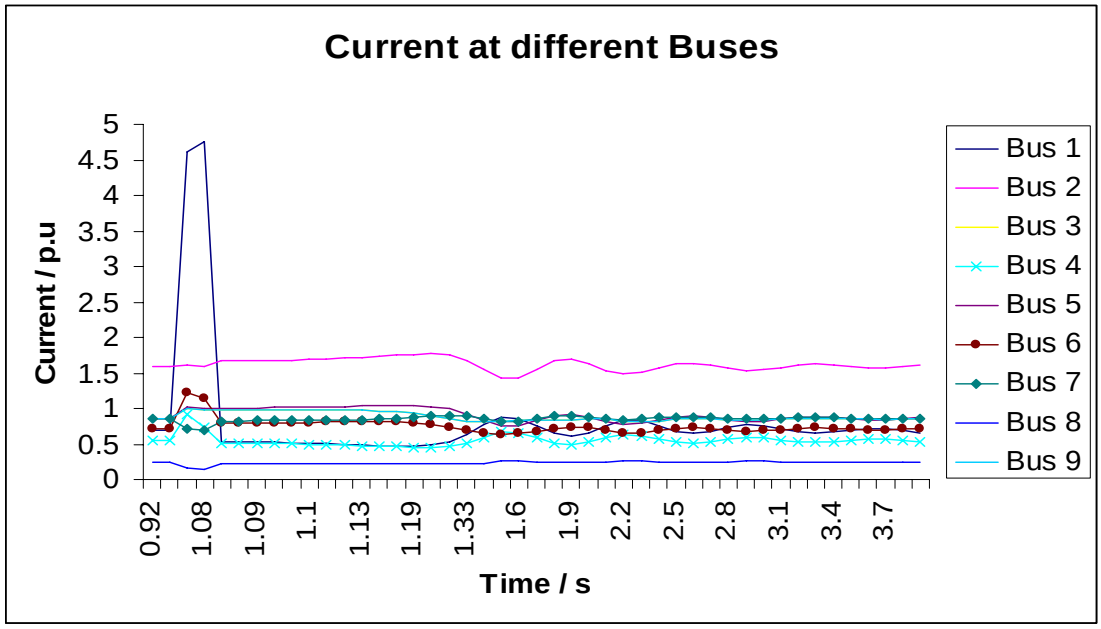



**Figure 6.19** Fault Current during fault at Bus 4

Comparing the fault on each bus with different position of fault it is can be observed that bus1 is always affected with large fault current for all the three positions of the fault. If the FCL is installed near bus 4, the damage from the fault current can be reduced on bus 1 as well as on the system.

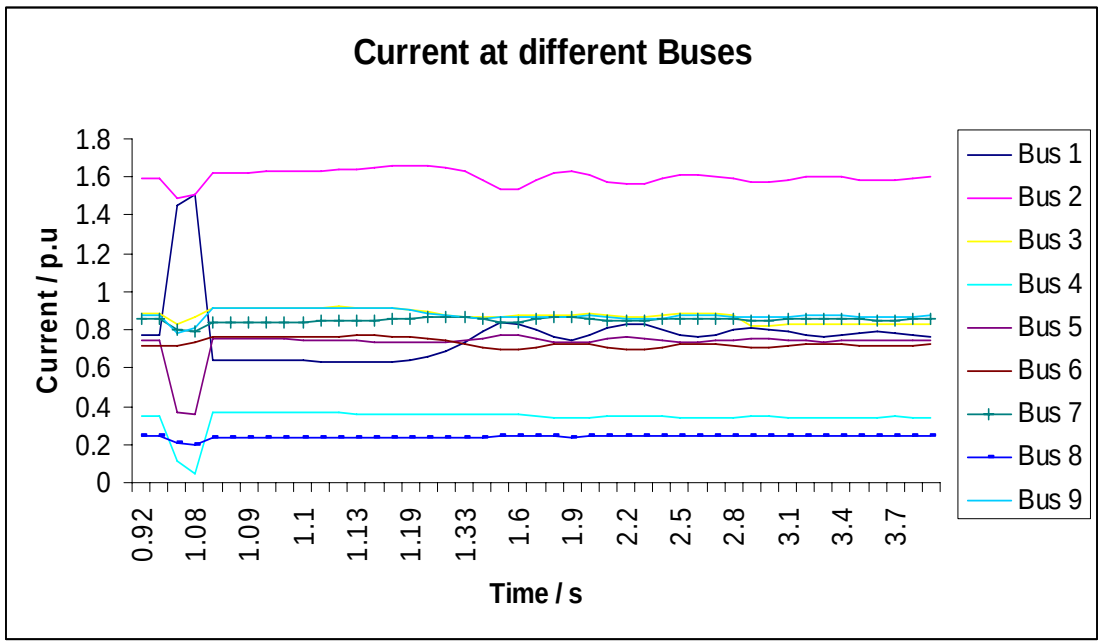



**Figure 6.20** Fault Currents reduced at different Buses with Fault at Bus 4

The fault current at bus 1 are reduced to 1.4 p.u which was more than 4.5 p.u before increasing the impedance of the line between fault and bus 4 shown in Figure 6.20. The fault currents at all the other buses are reduced below the normal value of the current during normal operation, but it will be not possible if the FCL is installed in the system. The FCL will limit the fault current to a lower value which will not do any damage to the equipment in the system during fault. The FCL can limit the fault current below the current during normal operation but the length of the superconductor element in the FCL should be large, which is not economical and a large cooling system is required. It is observed that bus 1 is the bus which is affected every time there is fault in the system, no matter where the fault is. The losses in the network are supplied by slack bus at bus 1 and bus 1 has one synchronous generator. Therefore bus 1 supplies the most of the power to the system as compared to bus 2 and bus 3, so bus 1 is affected during any disturbance in the system irrespective of the location of the disturbance. The optimum location of the fault current limiter would be close to bus 4, which will limit the large current during fault at bus 1, as well as on the other buses in the network.

## 6.5 Conclusions

The operation of the nine bus system under normal and fault operation is explained and the results are reported. The real and reactive powers during normal and fault operation are shown and analysed. The reactive power during fault rises to a high value, causing the current during fault rises to a very large value. A dummy transmission line is added between the fault and system to show the affect of the increase impedance during fault. The fault current during fault are plotted and the fault currents are reduced, by increasing the impedance of the dummy line between the fault and the system. The position of the fault is changed and the fault current during each position of fault is calculated and analysed. It is observed that the area close to fault is the more affected than the area away from the fault. The fault is applied on bus 7, bus 9 and bus 4, and bus 1 has a large fault current for all the three locations of fault. The bus 1 has a generator and also a slack bus, due to which it always has a large fault current during fault. The optimum location of the Fault Current Limiter is analysed by the changing the position of the fault and calculating the current during fault on each bus in the system. The optimum location of the FCL

in the nine bus system would be near bus 4 because bus 1 has a large fault current during all the three position of the fault in the system. In case of the FCL, once the current becomes more than the critical value of the current of the FCL, it will switch to its high impedance state, which will limit the fault current to a lower value, thus saving the equipment installed in the system.

# Chapter 7

# Conclusions and future work

## 7.1 Conclusions

The operating principle, design consideration and the experimental results of two types of fault current limiters are reported and discussed in this thesis. The passive Magnetic Current Limiter (MCL) device which consists of two ferrite cores and a permanent magnet sandwiched between two saturated ferrite cores. The permanent magnet forces the cores to operate in saturation during normal operation and the mmf due to current in the windings and permanent magnet are in the same direction in one core and opposite in the other core. Ferrite is used as core material because it has a low saturable flux density, so the cores remain in saturation during normal operation. During fault the cores come out of saturation in alternative half cycle of the current and the effective impedance of the device becomes equal to saturated inductance of core #1 plus the unsaturated inductance of the core #2. The field and the thermal model of the Magnetic Current Limiter device have been reported and the variation of the temperature with current has been discussed.

The High Temperature Fault Current Limiter (HTSFCL), resistive type, for use in power systems has been discussed and MATLAB simulation of the HTSFCL has been carried out for 110kV and 9kA systems. The current during normal operation and fault was calculated and it was observed that fault current is decreased to a low value during fault and the time taken by HTSFCL to perform its operation is very less. The HTSFCL with different length of superconductor has been reported and the variation of the fault current with different lengths has also been reported.

The single phase and three phase experimental results of the device are discussed. From the experimental results the fault current is limited to a lower value in a fraction of second after the fault. During fault there is a large voltage drop across the FCL, due to high impedance of the device during fault which limits the fault current.

The nine bus model has been designed in PSAT and its operation under normal and fault operation has been observed. Based on the principle of FCL the effect of the increased impedance during fault is shown in PSAT with a dummy line between the

fault and the nine bus network, and results show there is a decrease in the fault current when the impedance of the dummy line is increased.

The passive Magnetic Current Limiter and HTSFCL does not require any external source or sensing device to detect the fault current or other components to perform their operation. It automatically switches to a high impedance state if the current in the circuit rises above a certain value of current during normal operation. After the fault is cleared it is automatically reset and reset time is zero.

The characteristics of the passive fault current limiters can be summarised as follows:-

1. No need for any sensing device and external source to detect the fault current in the circuit.
2. The operation is totally automatic with zero reset time.
3. Very low voltage drop across the device during normal operation.
4. Simple structure and easy to design
5. The field model of the MCL in FEMLAB without current in the windings shows there is uniform distribution of magnetic flux in both the cores and the cores operate in saturation during normal operation.
6. The experimental results with the fabricated models of MCL have been reported.

## 7.2 Future Work

There are some areas in which there are a need to improve the performance of the model further. A core material of very low saturation flux density is required so that the core does not come out of saturation during normal operation. In this model it can be observed from the flux and current characteristics that sometimes the cores come out of saturation during normal operation.

There is a need to reduce the size of the device. In case of HTSFCL the cooling cost is very high and we need to check that a superconductor of an appropriate length is used. Fault Current Limiters have been installed in U.S, Canada, Switzerland, Germany and many other countries. Due to FCLs these countries have more reliable power systems. To improve the reliability of power systems network in New Zealand we need to apply Fault Current Limiters as may be a future possibility. More research work is required in order to apply HTSFCL to more complex power systems.

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# APPENDIX 1

```
format long

% Initializing variables

V = 110000*sqrt(2);% Input Supply Voltage
w = 2*pi*50;    % frequency
R = 9;        % load Resistance
Eo = 0.05;
b = 3.0;
p = 20e-6;
jc = 2e+7; %Current  Density
Ec = 1e-4;
Tc=108; % Critical Temperature of the High Temp. Superconductor
a = 7.5;

In = 9000*sqrt(2);  % Nominal Current
thick_hts = 2e-3;   % thickness of HTS  (check this value)
wth_hts = In/(0.7*jc*thick_hts);    % width of HTS
thick_ss = 4e-2;    % thickness of stainless steel
wth_ss = 2e-3;      % width of stainless steel
A = wth_hts*thick_hts;     % Area of HTS
l = 80;          % length of HTS     (check this value)
L1 = 0.0165;       % initial inductance
h = 0.00001;    % Runge-Kutta step size
I = 0;          % current at starting
t = 0;          % starting time
TT = 77;         % initial temperature of superconductor
NSS = 20;       % stainless steel layers
NHTSC = 40;       % HTS layers
KSS = 8;        % thermal conductivity of stainless steel
KHTSC = 1;        % thermal conductivity of HTS
CSS = 2.34e+6;  % specific heat capacity of stainless steel
CHTSC = 6.35e+5;   %specific heat capacity of HTS

% Initialising temperature for all layers
for j=1:(2*NSS+NHTSC+1)
    T(j) = TT;
end
```

```
% Layer constants

% Stainless steel
for j=1:NSS
    K(j) = KSS;     % thermal conductivity
    C(j) = CSS;     % specific heat capacity
end

K(NSS+1) = 0.5*(KSS+KHTSC);   % thermal conductivity at interface 1
C(NSS+1) = 0.5*(CSS+CHTSC);   % specific heat capacity at interface 1

% HTSC
for j=NSS+2:NSS+NHTSC
    K(j) = KHTSC;     % thermal conductivity
    C(j) = CHTSC;     % specific heat capacity
end

K(NSS+NHTSC+1) = 0.5*(KSS+KHTSC);   % thermal conductivity at
interface 2
C(NSS+NHTSC+1) = 0.5*(CSS+CHTSC);   % specific heat capacity at
interface 2

% Stainless steel
for j=NSS+NHTSC+2:2*NSS+NHTSC
    K(j) = KSS;     % thermal conductivity
    C(j) = CSS;     % specific heat capacity
end

% The following part creates E vs. J look-up tables

a1 = (log(Eo/Ec))/(log((jc/jc)^(1-(1/b))*(Eo/Ec)^(1/a)));
for(i=1:50)
    jss(i)=((i*0.1)*1.0e+7)+2.0*1e7;
    E(i) = (Ec)*((jss(i)/jc)^a1);
end
jss1=jss(50);
%The Flux flow regime
for(i=1:50)
```

```
    jss(50+i)=((i*0.05)*1.0e+8)+jss1;
    E(50+i) = [(Eo)*(Ec/Eo)^(b/a)]*[(jss(50+i)/jc)^b];
end
jss2=jss(100);
%The Normal conducting regime
for(i=1:50)
    jss(100+i)=((i*0.05)*1.0e+8)+jss2;
    E(100+i)=(p*TT*jss(100+i))/Tc;
end



% Create T vs. rho look-up tables

T_values = [50 60 70 77 77.5 78 78.5 79.0 79.5 80 81 82 84 86 88 90
92 94 96 98 100 105 110 115 120 125 130 150 175 200 250 300 350 400
450 500 550 600 650 700 750 800 850 900 950 1000];
rho_values = (1.4e-6)*[.7 .75 .8 .9 1.8 4.1 9.3 14.5 19.8 24.2 26.8
27.5 28.6 29.7 30.8 31.9 33 34.2 35.4 36.6 38.1 41.8 44.5 47.2 50 53
57 58 59 60 61 62 63 64 65 66 67 68 69 70 71 72 73 74 75 76];

% Calculate initial superconductor resistance.

rho = interp1(T_values, rho_values, T);
R_sup = rho * l / A;

 for m=1:10000
    Current(m) = I;
    Time(m) = t;
    J =I/A;



  if (m>4000) % Close switch after two cycles.
      V1 =V*sin(w*t);
      %Current(m) = I;
      %Time(m) = t;
      E1 =abs(V1)/l;



      % Current density for layers
```

```
  cur_den1 = 0.1*abs(I)/(wth_ss*thick_ss*2*NSS); %Stainless Steel
  cur_den2 = 0.9*abs(I)/(wth_hts*thick_hts*NHTSC);% HTS

for j=1:NSS
    JJ(j) = cur_den1;
end

for j=NSS+NHTSC+2:2*NSS+NHTSC
    JJ(j) = cur_den1;
end

for j=NSS+2:NSS+NHTSC+1
    JJ(j) = cur_den2;
end

% Interface values
JJ(NSS+1) = 0.5*(cur_den1+cur_den2);
JJ(NSS+NHTSC+1) = 0.5*(cur_den1+cur_den2);

% Calculating Q
SS_layer = thick_ss/NSS;
HTSC_layer = thick_hts/NHTSC;
Q(1) = 0;
for j=2:NSS
    Q(j) = JJ(j)*E1;     % Heat input for SS layer
end

for j=NSS+1:NSS+NHTSC
    Q(j) = JJ(j)*E1;     % Heat input for Superconductor layer
end

for j=NSS+NHTSC+1:2*NSS+NHTSC
    Q(j) = JJ(j)*E1;     % Heat input for SS layer
end

% Calculating Temperature

for j=2:NSS
```

```
T(j) = T(j)+[K(j)*h*(T(j+1)-2*T(j)+T(j-
1))]/[(C(j)*SS_layer*SS_layer)]+Q(j)*h/C(j);
      if(j==3)
          TT1(m) = T(j);
      end
      if(j==15)
          TT2(m) = T(j);
      end

  end

  for j=NSS+1:NSS+NHTSC
 T(j) = T(j)+[K(j)*h*(T(j+1)-2*T(j)+T(j-
 1))]/[(C(j)*HTSC_layer*HTSC_layer)]+Q(j)*h/C(j);
       if(j==24)
          TT3(m) = T(j);
      end
      if(j==30)
          TT4(m) = T(j);
      end
      if(j==36)
          TT5(m) = T(j);
      end
  end

  for j=NSS+NHTSC+1:2*NSS+NHTSC
       T(j) = T(j)+[K(j)*h*(T(j+1)-2*T(j)+T(j-
       1))]/[(C(j)*SS_layer*SS_layer)]+Q(j)*h/C(j);
       if(j==45)
          TT6(m) = T(j);
      end
      if(j==56)
          TT7(m) = T(j);
      end
  end

  % Calculation of average temperature of HTS layer
  sum = 0;
  for j=NSS+1:NSS+NHTSC+1
      sum = sum+T(j);
```

```
    end

    T_av = sum/NHTSC;

    % Calculate new superconductor resistance

    rho = interp1(T_values, rho_values, T_av);
    R_sup = rho * l / A;
    R_sup_values(m) = R_sup;

    I =V1/R_sup;

    t =t+h;  % increment of time

end

     if (m <=4000)

          if abs(J) <= jss1
       E1 = (Ec)*((abs(J)/jc)^a1);
    elseif (abs(J) > jss1) & (abs(J) < jss2);
          E1 = [(Eo)*(Ec/Eo)^(b/a)]*[(abs(J)/jc)^b];
       else
          E1=(p*T*abs(J))/Tc;
       end
       L=L1;
    % Current density for layers
    cur_den1 = 0.1*abs(I)/(wth_ss*thick_ss*2*NSS); % SS Layer
    cur_den2 = 0.9*abs(I)/(wth_hts*thick_hts*NHTSC); % HTS Layer

    for j=1:NSS
        JJ(j) = cur_den1;
    end

    for j=NSS+NHTSC+1:2*NSS+NHTSC
        JJ(j) = cur_den1;
    end

    for j=NSS+2:NSS+NHTSC+1
```

```
    JJ(j) = cur_den2;
end

% Interface values
JJ(NSS+1) = 0.5*(cur_den1+cur_den2);
JJ(NSS+NHTSC+1) = 0.5*(cur_den1+cur_den2);

% Calculating Q
SS_layer = thick_ss/NSS;
HTSC_layer = thick_hts/NHTSC;
Q(1) = 0;
for j=2:NSS
    Q(j) = JJ(j)*E1;     % Heat input for SS layer
end

for j=NSS+1:NSS+NHTSC
    Q(j) = JJ(j)*E1;     % Heat input for SC layer
end

for j=NSS+NHTSC+1:2*NSS+NHTSC
    Q(j) = JJ(j)*E1;     % Heat input for SS layer
end

% Calculating Temperature

for j=2:NSS
   T(j) = T(j)+[K(j)*h*(T(j+1)-2*T(j)+T(j-
   1))]/[(C(j)*SS_layer*SS_layer)]+Q(j)*h/C(j);
    if(j==3)
        TT1(m) = T(j);
    end
    if(j==15)
        TT2(m) = T(j);
    end

end

for j=NSS+1:NSS+NHTSC
```

```
    T(j) = T(j)+[K(j)*h*(T(j+1)-2*T(j)+T(j-
    1))]/[(C(j)*HTSC_layer*HTSC_layer)]+Q(j)*h/C(j);
     if(j==24)
        TT3(m) = T(j);
    end
    if(j==30)
        TT4(m) = T(j);
    end
    if(j==36)
        TT5(m) = T(j);
    end
end

for j=NSS+NHTSC+1:2*NSS+NHTSC
     T(j) = T(j)+[K(j)*h*(T(j+1)-2*T(j)+T(j-
     1))]/[(C(j)*SS_layer*SS_layer)]+Q(j)*h/C(j);
     if(j==45)
        TT6(m) = T(j);
    end
    if(j==56)
        TT7(m) = T(j);
    end
end

% Calculation of average temperature of HTS layer
sum = 0;
for j=NSS+1:NSS+NHTSC+1
    sum = sum+T(j);
end

T_av = sum/NHTSC;

% Calculate new superconductor resistance

rho = interp1(T_values, rho_values, T_av);
R_sup = rho * l / A;
R_sup_values(m) = R_sup;
% One step of fourth order Runge-Kutta to solve DE for current.
```

```
    K1 = h*(V*sin(w*t) - (R_sup + R)*I)*(1/L);
    K2 = h*(V*sin(w*(t+h/2)) - (R_sup + R)*(I+K1/2))*(1/L);
    K3 = h*(V*sin(w*(t+h/2)) - (R_sup + R)*(I+K2/2))*(1/L);
    K4 = h*(V*sin(w*(t+h)) - (R_sup + R)*(I+K3))*(1/L);
    I = I + (1/6)*(K1 + 2*K2 + 2*K3 + K4);
    t = t + h;

    end


 end

%figure
plot(Time,Current)
%figure

%pause
%plot(Time, R_sup_values)

%figure
%pause
%plot(Time,TT3,Time,TT4,Time,TT5)
%pause




title('Current vs Time');
XLABEL('time / s');
YLABEL('Current / A');
```

# APPENDIX 2

## POWER FLOW REPORT

P S A T 2.0.0-beta

Author: Federico Milano, (c) 2002-2006
e-mail: fmilano@thunderbox.uwaterloo.ca
website: http://thunderbox.uwaterloo.ca/~fmilano

File: h:\psat\laly2.mdl
Date: 29-Jun-2007 16:05:15

NETWORK STATISTICS

Buses: 9
Lines: 6
Transformers: 3
Generators: 3
Loads: 3

SOLUTION STATISTICS

Number of Iterations: 4
Maximum P mismatch [p.u.] 0
Maximum Q mismatch [p.u.] 0
Power rate [MVA] 100

POWER FLOW RESULTS

| Bus | V [p.u.] | phase [rad] | P gen [p.u.] | Q gen [p.u.] | P load [p.u.] | Q load [p.u.] |
|---|---|---|---|---|---|---|

| | | | | | | |
|---|---|---|---|---|---|---|
| Bus1 | 1.04 | 0 | 0.70878 | 0.06468 | 0 | 0 |
| Bus2 | 1.025 | 0.1554 | 1.63 | -0.04197 | 0 | 0 |
| Bus3 | 1.025 | 0.06656 | 0.85 | -0.20246 | 0 | 0 |
| Bus4 | 1.0372 | -0.03786 | 0 | 0 | 0 | 0 |
| Bus5 | 1.0264 | -0.05627 | 0 | 0 | 1.25 | 0.5 |
| Bus6 | 1.0216 | -0.05161 | 0 | 0 | 0.9 | 0.3 |
| Bus7 | 1.0324 | 0.05898 | 0 | 0 | 0 | 0 |
| Bus8 | 1.0194 | -0.00083 | 0 | 0 | 1 | 0.35 |
| Bus9 | 1.0295 | 0.01742 | 0 | 0 | 0 | 0 |

STATE VECTOR

| | |
|---|---|
| delta_Syn_1 | 0.0413 |
| omega_Syn_1 | 1 |
| | |
| e1q_Syn_1 | 1.0416 |
| e1d_Syn_1 | 0 |
| delta_Syn_2 | 0.9589 |
| omega_Syn_2 | 1 |
| e1q_Syn_2 | 0.69915 |
| e1d_Syn_2 | 0.67948 |
| delta_Syn_3 | 1.0715 |
| omega_Syn_3 | 1 |
| e1q_Syn_3 | 0.70786 |
| e1d_Syn_3 | 0.66814 |
| vm_Exc_1 | 1.025 |
| vr1_Exc_1 | 1.7478 |
| vr2_Exc_1 | -0.30013 |
| vf_Exc_1 | 1.6674 |
| vm_Exc_2 | 1.04 |
| vr1_Exc_2 | 1.0661 |
| vr2_Exc_2 | -0.18887 |
| vf_Exc_2 | 1.0493 |
| vm_Exc_3 | 1.025 |

| | |
|---|---|
| vr1_Exc_3 | 1.3216 |
| vr2_Exc_3 | -2.3207 |
| vf_Exc_3 | 1.2893 |
| tg_Tg_1 | 0 |
| tg_Tg_2 | 0 |
| tg_Tg_3 | 0 |

MECHANICAL POWERS & FIELD VOLTAGES

| | |
|---|---|
| Pmech_1 | 0.70878 |
| Pmech_2 | 0.85 |
| Pmech_3 | 1.63 |
| Vfd_1 | 1.0493 |
| Vfd_2 | 1.2893 |
| Vfd_3 | 1.6674 |

EXCITER REFERENCE VOLTAGES

| | |
|---|---|
| Vref_1 | 1.1124 |
| Vref_2 | 1.0933 |
| Vref_3 | 1.0911 |

LINE FLOWS

| From Bus | To Bus | Line | P Flow [p.u.] | Q Flow [p.u.] | P Loss [p.u.] | Q Loss [p.u.] |
|---|---|---|---|---|---|---|
| Bus9 | Bus6 | 1 | 0.72208 | -0.0903 | 0.00586 | -0.1702 |
| Bus7 | Bus8 | 2 | 0.88629 | 0.0286 | 0.00636 | -0.10295 |
| Bus5 | Bus4 | 3 | -0.52302 | -0.48871 | 0.00112 | -0.50832 |
| Bus5 | Bus7 | 4 | -0.72698 | -0.01129 | 0.01674 | -0.24002 |
| Bus6 | Bus4 | 5 | -0.18378 | -0.2201 | 0.00086 | -0.16278 |

| | | | | | | |
|---|---|---|---|---|---|---|
| Bus8 | Bus9 | 6 | -0.12007 | -0.21845 | 0.00058 | -0.37319 |
| Bus1 | Bus4 | 7 | 0.70878 | 0.06468 | 0 | 0.02698 |
| Bus3 | Bus9 | 8 | 0.85 | -0.20246 | 0.00727 | 0.04258 |
| Bus2 | Bus7 | 9 | 1.63 | -0.04197 | 0 | 0.15816 |

LINE FLOWS

| From Bus | To Bus | Line | P Flow [p.u.] | Q Flow [p.u.] | P Loss [p.u.] | Q Loss [p.u.] |
|---|---|---|---|---|---|---|
| Bus6 | Bus9 | 1 | -0.71622 | -0.0799 | 0.00586 | -0.1702 |
| Bus8 | Bus7 | 2 | -0.87993 | -0.13155 | 0.00636 | -0.10295 |
| Bus4 | Bus5 | 3 | 0.52414 | -0.01961 | 0.00112 | -0.50832 |
| Bus7 | Bus5 | 4 | 0.74371 | -0.22873 | 0.01674 | -0.24002 |
| Bus4 | Bus6 | 5 | 0.18464 | 0.05732 | 0.00086 | -0.16278 |
| Bus9 | Bus8 | 6 | 0.12065 | -0.15474 | 0.00058 | -0.37319 |
| Bus4 | Bus1 | 7 | -0.70878 | -0.03771 | 0 | 0.02698 |
| Bus9 | Bus3 | 8 | -0.84273 | 0.24505 | 0.00727 | 0.04258 |
| Bus7 | Bus2 | 9 | -1.63 | 0.20013 | 0 | 0.15816 |

GLOBAL SUMMARY REPORT

TOTAL GENERATION

REAL POWER [p.u.] 3.1888
REACTIVE POWER [p.u.] -0.17975

TOTAL LOAD

REAL POWER [p.u.] 3.15
REACTIVE POWER [p.u.] 1.15

TOTAL SHUNT

REAL POWER [p.u.] 0

REACTIVE POWER (IND) [p.u.]  0

REACTIVE POWER (CAP) [p.u.]  0

TOTAL LOSSES

REAL POWER [p.u.]  0.03878

REACTIVE POWER [p.u.]  -1.3298

# Publication

# Protection of Electronic Circuits: A Magnetic Current Limiter Based Approach

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**Abstract:** Every Electronic circuit that consists of semiconductor devices can be protected by using the proposed magnetic current limiter. The increase in the demand of electrical power has also increased the fault current levels in the system. The semiconductor devices used in these systems should be rated to accommodate the large fault current levels. However, rating the devices to higher current levels is not an appropriate solution to this problem. The best solution is to limit the level of fault current in the circuit. Magnetic current limiter is a passive device based on permanent magnet sandwiched between the pole faces of two saturable cores. A model has been fabricated and the experimental results have been reported. The thermal and field model has been developed using FEMLAB to investigate the situation of limiter under fault condition as well as under normal condition.

**Keywords:** Magnetic current limiter, permanent magnet, semiconductor devices, saturable core, field and thermal model, finite element analysis, magnetomotive force.

## 1. INTRODUCTION

Due to increase in the power demand the possibility of faults also increases. Due to the increase in fault levels large faults currents are produced which generate large mechanical forces which may damage the circuit components. To overcome this problem the circuit configuration is to be when the Fault occurs in the circuit. It is unacceptable in the most of cases as it reduces the system reliability and increases the system losses. During fault and other abnormal conditions such as short circuit etc, Magnetic fault current limiter is used to limit the current to lower value during fault.

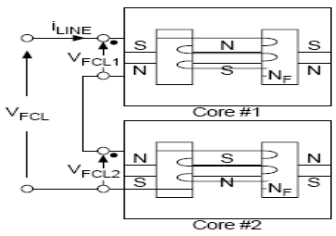


Figure 1: Basic structure of MCL

Under normal operation it offers low impedance and when some fault occurs, impedance increases to high value which lowers the value of fault current thus protecting the devices in the circuit having fault current limiter.

## 2. OPERATING PRINCIPLE OF MAGNETIC CURRENT LIMITER

Magnetic current limiter (MCL) consists of permanent magnet which is sandwiched between the saturable cores as shown in figure 1. The permanent magnet is used to saturate the core under normal operating condition. The direction of the alternating current and magnetomotive force in the core#1 is same and opposite in the core#2 at the same time. During normal operation when current is low the effective impedance of the system is low as both the cores are in saturation. On fault condition, the current rises to a large value that forces the both cores come out of saturation in alternative half cycle of the current and impedance of the system rises, which becomes equal to unsaturated inductance of one core in combination with the saturated inductance of the second core which restricts the flow of large fault current. To saturate the core such as ferrite, it should have a very low value of saturation flux density compared to PM. Fig 2 shows the B-H characteristics of PM and core and indicates the operating point of one core. The complete flux current characteristics of both the core and PM assembly are shown in figure2

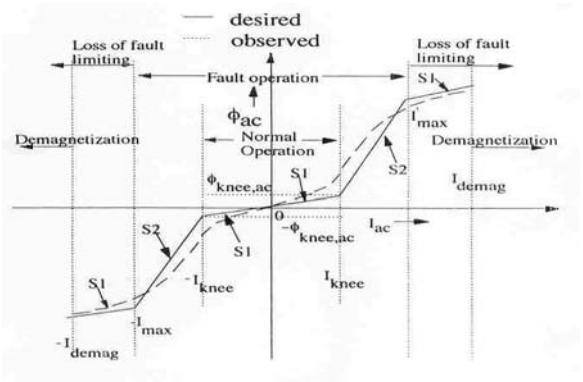


Figure 2: The ϕ-i characteristics of the complete system

A different type of magnetic current limiter has been fabricated and experiments were performed applying the above principles. These include in series and parallel fabrication. Figure 3 shows the series fabricated biased limiter based on ferrite core and permanent magnet made of Nd-Fe-B. In this fabrication the magnetomotive force of PM and coil act in series. Figure 4 shows the parallel fabricated biased limiter based on steel core and PM. Models shown in figure 3 and 4 are used for single phase system and model of figure 5 is used for three phase system.

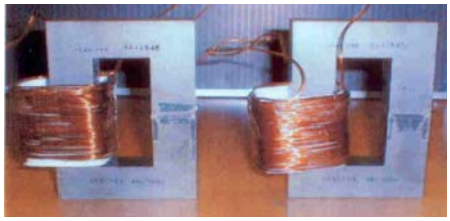

Figure 3: Series biased MCL based on ferrite core and permanent magnet

Figure 4: Parallel biased MCL based on steel core and permanent magnet

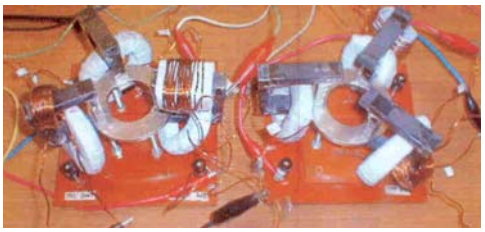

Figure 5: series biased MCL based on ferrite core and ring type permanent magnet for three phase system

## 3. DESIGN AND APPLICATION OF MCL

The design aspects of magnetic current limiter are described in this part. When there is fault condition, to avoid the loss of current limiting and demagnetization zone of PM (as shown in the Fig. 2), the following condition is to be satisfied:

$$H_c l_m \geq NI_{\max} \qquad (1)$$

Where $H_c$ *is* the coercive force of the PM and $l_m$ is the length of the PM. $I_{max}$ is the maximum current allowed during the fault condition. $H_c$ is stated by the PM and is not under designer's control. The minimum number of turns of coil is one. The maximum value of current depends on the magnet length.

Under normal operation the voltage drop across the MCL is given by

$$V_{NOR} = X_s I = 2(2\pi f L_s) I = 4\pi f L_s I \qquad (2)$$

and the voltage across the MCL during fault is given by

$$V_{FAULT} = X_u I = 2\pi f (L_s + L_u) I \qquad (3)$$

From the above equations it is clear that voltage drop during normal operation is very small and it rises to very high value during fault condition. $L_s$ and $L_u$ are the saturated and unsaturated inductance respectively and are given by:

$$L_s = \frac{N^2}{R_m + R_s} \text{ (4) and } L_u = \frac{N^2}{R_m + R_u} \qquad (5)$$

$R_m$, $R_s$ and $R_u$ are the reluctance of the PM, saturated reluctance of the core and unsaturated reluctance of the core respectively and given by

$$R_m = \frac{l_m}{\mu_m S} (6),\ R_s = \frac{l_{core}}{\mu_s S} (7), \text{and } R_u = \frac{l_{core}}{\mu_u S} \ (8)$$

Here $S$ is the common area of the PM or core, $\mu_m$, $\mu_s$ and $\mu_u$ are the permeabilities of PM, saturated core and unsaturated core respectively. During fault condition the full voltage appears across the MCL and is given by

$$V_{supply} = X_u I_{FAULT} \ (9)$$

The ratio of the normal drop across MCL to the supply voltage is given by

$$\frac{V_{NOR}}{V_{supply}} = \frac{X_s I_{NOR}}{X_u I_{FAULT}} = \frac{1}{k}\frac{X_s}{X_u} = \frac{1}{k}\frac{2L_s}{L_s + L_u} = \frac{2}{k}\frac{1}{1 + L_u / L_s} \qquad (10)$$

where k is the ratio of $I_{FAULT}$ to $I_{NOR}$.

From above equations we can write

$\frac{L_u}{L_s} = 1 + \frac{\mu_m}{\mu_s}\frac{l_{core}}{l_m}$ (11); the reluctance $R_u$ is neglected with respect to $R_m$. For NdFeB PM, the permeability $\mu_m \approx 1.8\mu_0$ and assuming $l_{core}/l_m = 100$, we get $\frac{L_u}{L_s} = 1 + \frac{180}{\mu_{rs}}$ (12) ; $\mu_{rs}$ is the relative permeability of the core under saturated condition.

Figure 6 shows the variation of the ratio Lu/Ls as a function of $\mu_{rs}$ . From the figure it is observed that for higher value of $L_u/L_s$ a very low value of saturated permeability, $\mu_{rs}$ of core is required . So for this value of $\mu_{rs}$, it is not possible to have high value of $L_u/L_s$ which means that voltage drop during normal operation is quite large and due to this reason it is suitable

in power electronic based circuits which have supply system of voltage up to 600 V and current up to few hundreds of amperes as shown in figures 7 and 8.
The voltage in these circuits can be adjusted across the load so that the voltage drop across MCL under normal situation can be allowed a little more.

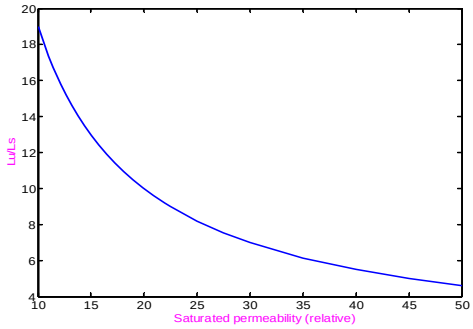


Figure 6: Variation of $L_u/L_s$ with $\mu_{rs}$

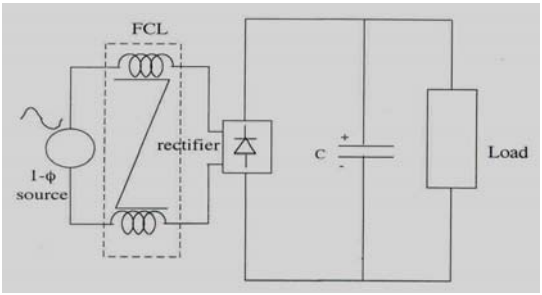


Figure 7: Single phase power electronic system with MCL

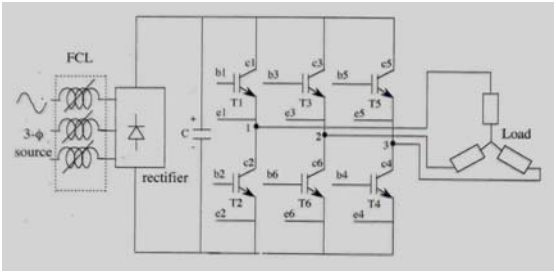


Figure 8: Three phase power electronic system with MCL

The advantage of having MCL in the electronic circuit of figure 7 with a discharged capacitor can be shown in figure 9. It is seen that in the absence of MCL the peak (negative) starting current reaches to 95 A. Presence of MCL in the circuit limits the peak(negative) current to 55 A, which is less than 200% of nominal peak current.

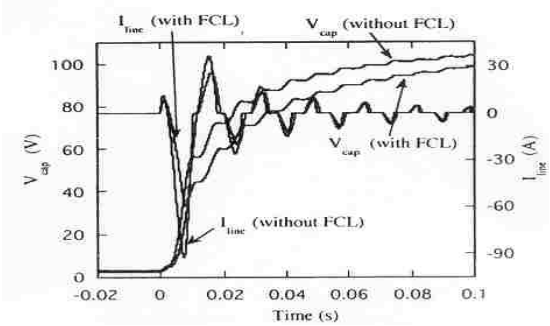


Figure 9:Current waveforms with and without MCL

Under shorted diode condition the current and voltage waveforms are shown in figure 10. It is observed that the peak current is considerably reduced with the implementation of MCL in the circuit.

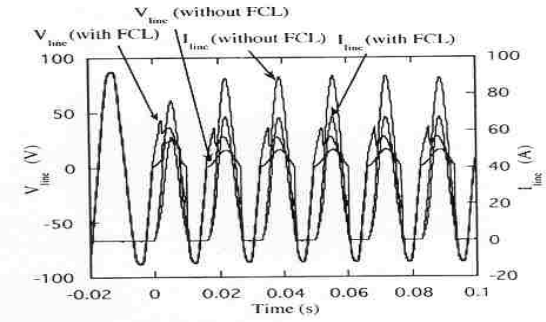


Figure 10: Current and voltage waveforms under a shorted diode condition

The line current and voltage of the shorted load condition is shown in the figure 11. It can be seen that the peak current is reduced to lower value due to MCL.

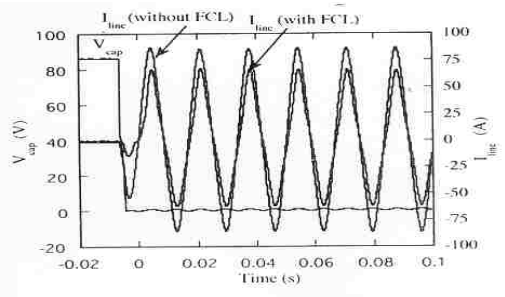


Figure 11: current waveforms during shorted output condition

## 4. FINITE ELEMENT MODELLING

The finite element software package FEMLAB has been used for analysing the flux distribution of the MCL both under normal and fault condition.
Figure 12 shows the model of the MCL when there is no current in the coil. The permanent magnet drives the core in the saturation region.

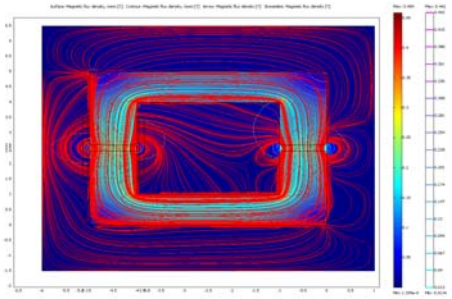

Fig.12 FEMLAB model of MCL with no current

Figure 13 shows the model of MCL with low positive current and from the figure we observe the magnetic flux density increases and the core remains in saturation region. Figure 14 shows the model of MCL when large positive current is passed into the coil. The magnetic flux density increases and remains in the saturation region.

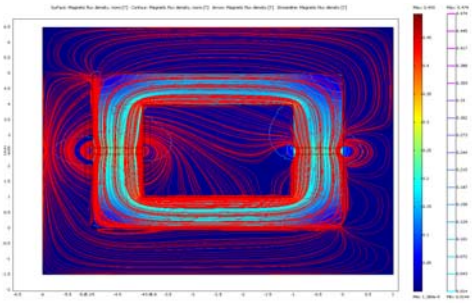

Figure 13: Model of MCL with low current corresponding to positive half of the cycle

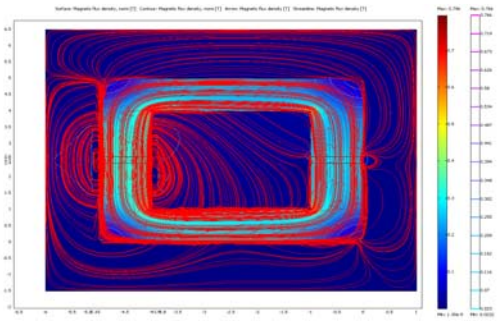

Figure 14: Model of MCL with large current corresponding to positive half of the cycle

The finite element model corresponding to negative half is shown in figure 15. A low negative current is applied to the system and it is seen the core remains in the saturation region as shown in the figure 15.

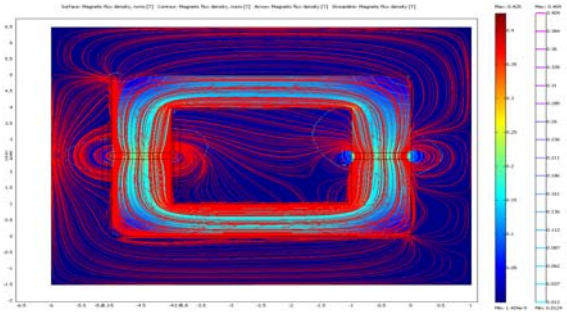

Figure 15: Model of MCL with low current corresponding to negative half of the cycle

When current increase to very high negative value (during fault) the magnetic flux density decrease as shown in figure 16. The core comes out of saturation and the effective impedance of the system increases which results in a current limiting action.

Since two cores are used as shown in figure 1, one core remains in saturation during positive half and goes to unsaturated region during the negative half during fault condition.

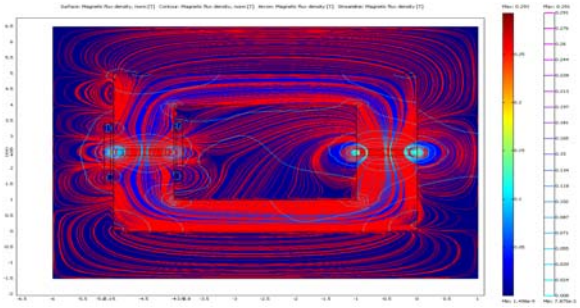

Figure 16: MCL with high negative current

The thermal model of the MCL is presented in the figure 17.

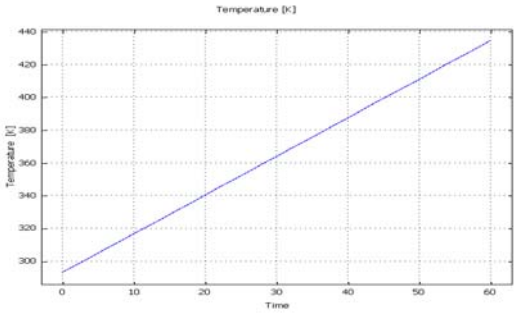


Figure17 shows the variation of Temperature with Time.

The variation of the temperature with the current is show in the figure 18. It is observed from the figure that as the current increases the temperature of the MCL also increases and due to which the cores comes out of saturation and the effective inductance of the core increases which results in current limiting action.

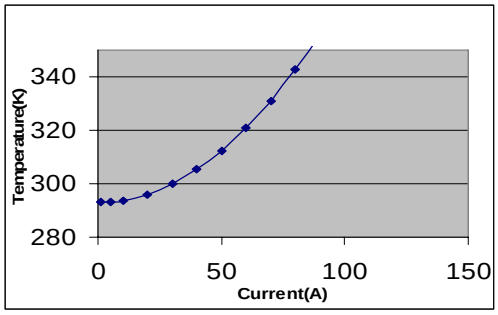

Figure 18 Variation of temperature with current

## 5. CONCLUSIONS

This paper has described the basic design philosophy and its use to protect semiconductor devices in electronic circuits of magnetic current limiter. A comprehensive analysis of design parameters has been carried out. This analysis can be used to design the MCL for a sample system and the critical optimum parameters for overall good performance. The analysis of electromagnetic field distribution has been carried out using finite element software. The thermal analysis of the model is also presented.

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# *Fault Current Limiter*

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## Outline of Presentation

- Introduction
- Operation of Fault Current Limiter (FCL)
- Experimental Results
- Flux distribution & Thermal Model of FCL
- High Temperature Superconductor(HTS) FCL in Power System.
- Optimum Location of HTSFCL
- Conclusion

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# Introduction

- Electronic & Electrical devices have wide applications in Industry
- Electronic & Electrical circuits are sensitive
- Most important concern about an device is its safe mode of operation
- Protection from fault or short circuit is needed

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# Introduction

- Consequences of faulty operation

1. Can permanently damage the device, which need to be replaced
2. Need to change the circuit configuration
3. Effects the integrity of system

And the Solution ?

- To limit fault current using Fault current limiter (FCL)

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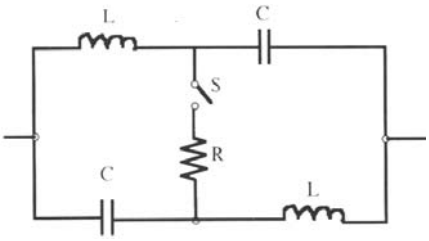
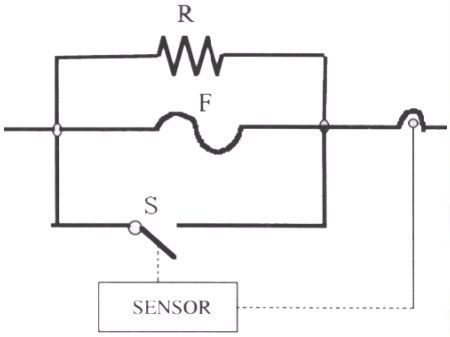
# Current Limiter Approaches

- **Resonant Circuit Limiters**
- **Switched Devices**
- **In line fuse devices**
- **Superconducting devices**

**Tuned impedance Current Limiter (fig.1)**




**Silver Sand fuse FCL (fig.2)**

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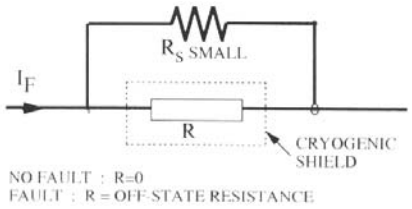
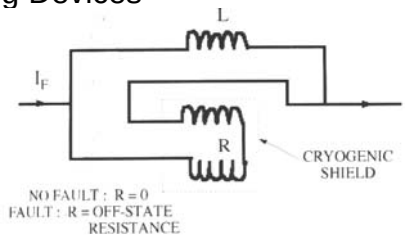
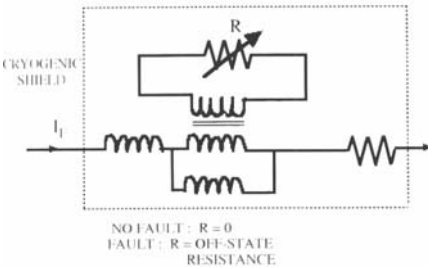
## Superconducting Devices




Fig(3)




Fig(4)




Fig(5)

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# Fault Current Limiter Based on Passive Devices

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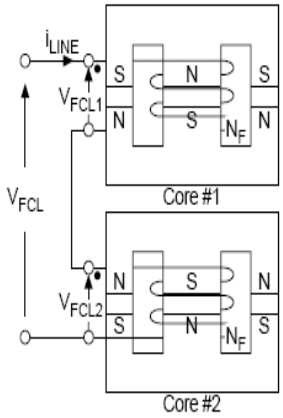
## Basic structure of FCL

- Consists of two cores
- Permanent Magnet
- Ferrite is used as core material

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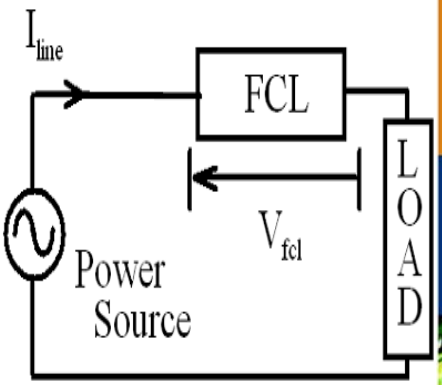
# Operating Principle of FCL

- Under Normal Operation
  1. Both cores operate in saturation
  2. Low effective impedance of system
  3. Low voltage drop
- The direction of current and MMF in cores

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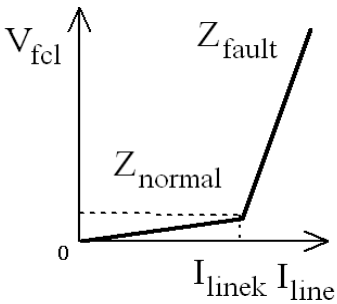
# Operating Principle of FCL

- During fault operation

1. Cores comes out of saturation in alternative half cycle
2. Effective Impedance of the system increases
3. Limits the fault current




Below $I_{linek}$ : Low impedance → Small voltage drop

Over $I_{linek}$ : High Impedance → Large Voltage Drop → **Current Limit**

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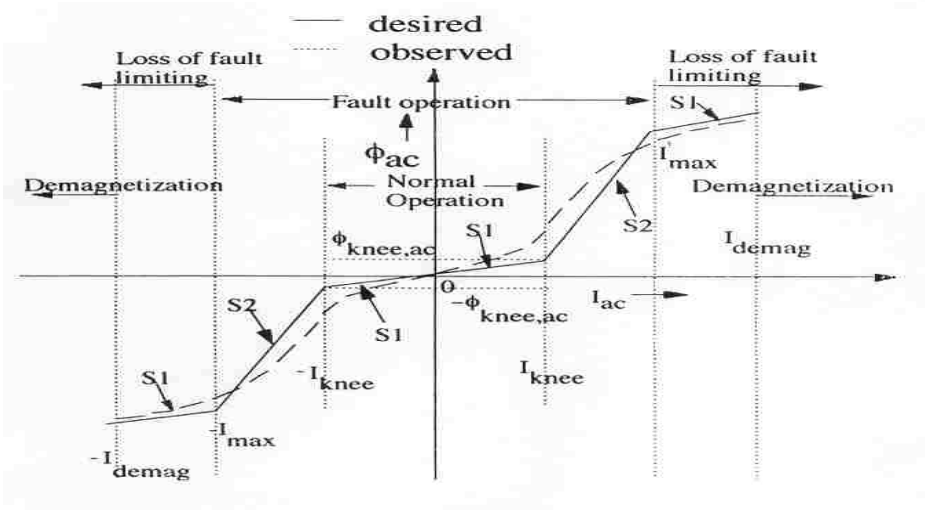
# $\phi$ - I Characteristics of FCL

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# Design Parameter of FCL

To avoid loss of current limiting action and demagnetization of PM

$$H_c l_m \geq N I_{\max}$$

Where $H_c$ is coercive force of PM

$l_m$ *is length of PM*

$I_{Max}$ is maximum current allowed during fault

Under normal operation the voltage drop across the FCL is given by

$$V_{NOR} = X_s I = 2(2\pi f L_s) I = 4\pi f L_s I$$

•The voltage across the FCL during fault is given by

$$V_{FAULT} = X_u I = 2\pi f (L_s + L_u) I$$

Contd..

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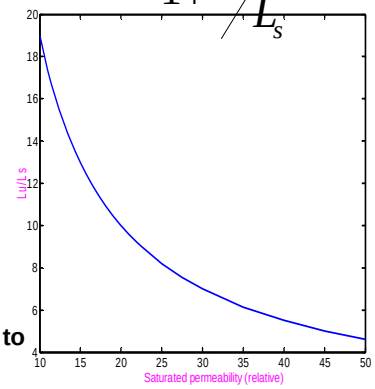
# Design Parameter of FCL

- Ratio of normal drop to supply voltage is given by.

$$\frac{V_{NOR}}{V_{supply}} = \frac{X_s I_{NOR}}{X_u I_{FAULT}} = \frac{1}{k}\frac{X_s}{X_u} = \frac{1}{k}\frac{2L_s}{L_s + L_u} = \frac{2}{k}\frac{1}{1 + L_u / L_s}$$

- k = $I_{fault}/I_{nor}$

$$\frac{L_u}{L_s} = 1 + \frac{180}{\mu_{rs}}$$




**For higher value of Lu/Ls, low value of Saturated permeability, $\mu_{rs}$**

**System voltage up to 600v and current up to few hundreds of amperes.**

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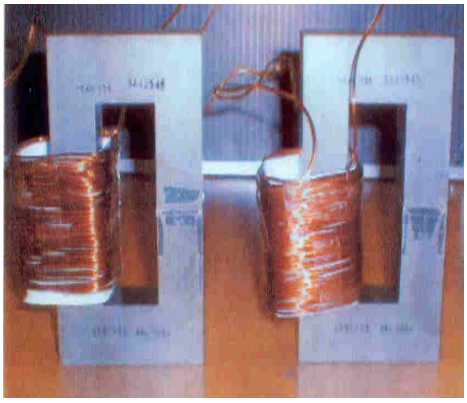
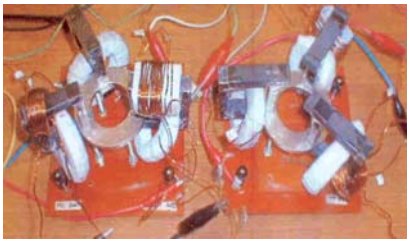
# Fabricated FCL





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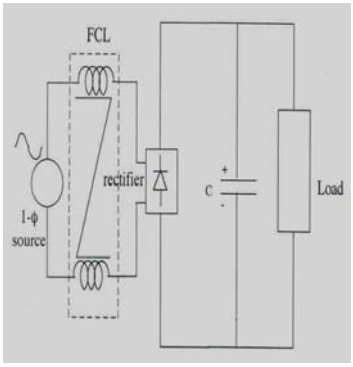
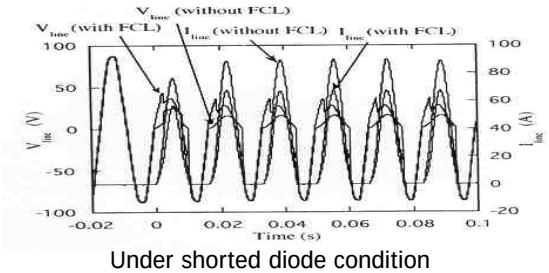
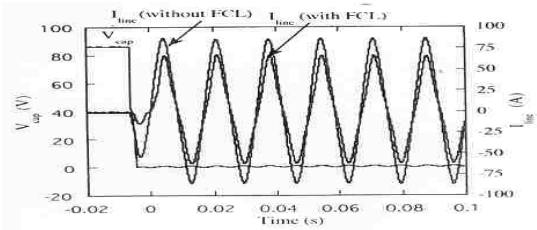
# Experimental Results




Circuit with FCL




Under shorted diode condition




Output at load under shorted condition.

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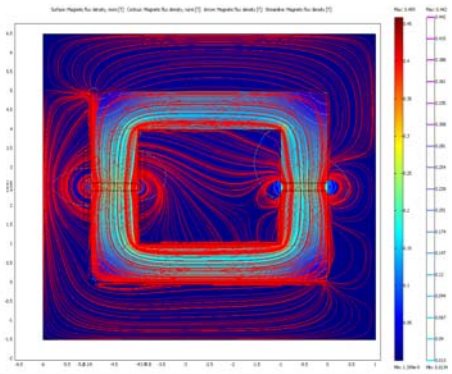
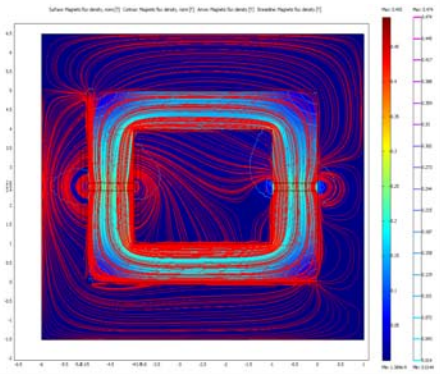
# Flux distribution of FCL using Finite element modelling



FEMLAB model of FCL with no current



Model of FCL with low current corresponding to positive half of the cycle

Contd..

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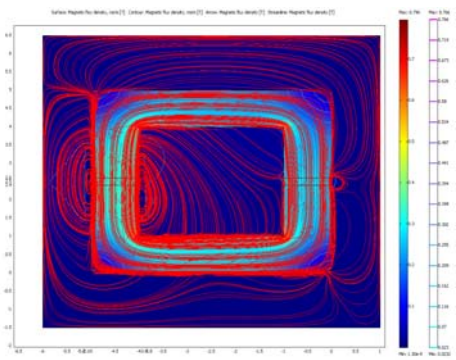
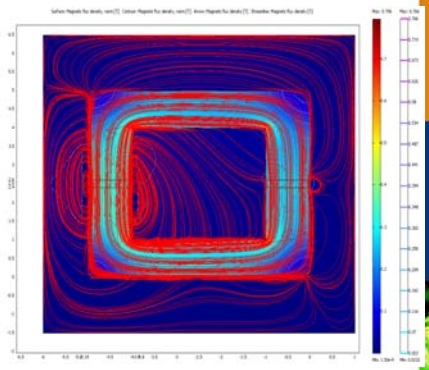
# Flux distribution of FCL using Finite element modelling



Model of FCL with large current corresponding to positive half of the cycle



Model of FCL with low current corresponding to negative half of the cycle

Contd..

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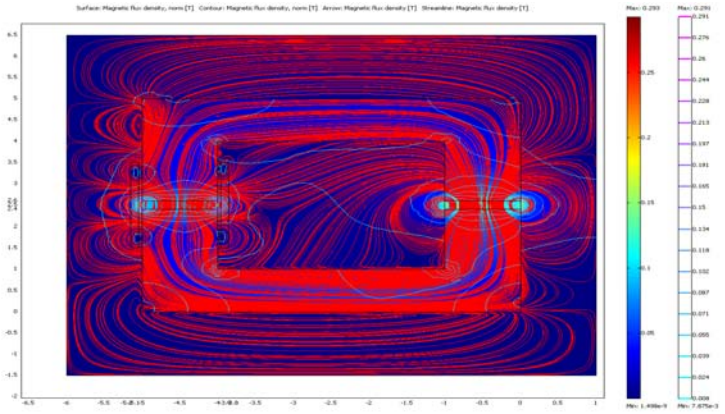
# Flux distribution of FCL using Finite element modelling

FEM. Model of FCL during Fault



FCL with high negative current

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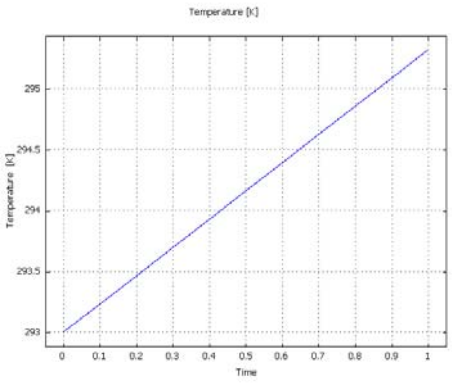
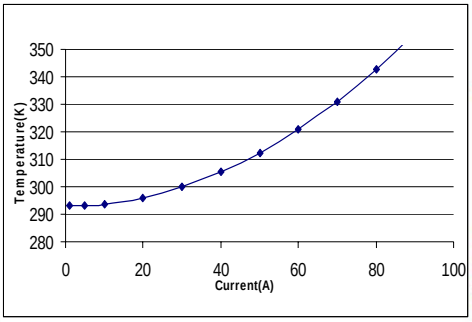
# Thermal Model of FCL




Variation of Temperature with Time (Transient)




Variation of temperature with current (Steady State)

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# Feature of FCL

- Easy to design as its a simple structure
- Passive device current limiter for AC usage using Inductive Method
- Relatively low cost as it composes of core, magnet and winding
- Maintenance free as its a simple structure
- Quick recovery time due to the usage of magnetic characteristics only

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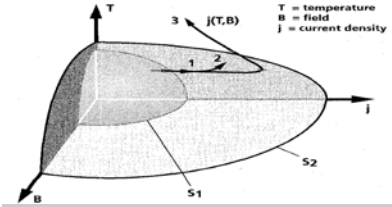
# High Temperature Superconductor FCL In Power System

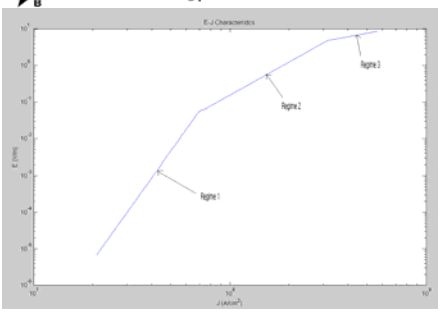
- Depends on T, B and J
- Jc → critical Current density
- Tc → critical temperature
- **Normal operation**
- J < Jc, T < Tc
- **Fault**
- J > Jc, T >Tc
- **Regime 1**

E (j,T) = Ec*( j / jc(T))^α(T)

where α(T) = max[ β, α'(T) ], with

- α'(T) = log( Eo/Ec) / log[( jc (77K) / jc (T))^(1-1/β)* ( Eo / Ec)^1/α(77K)]
- **Regime 2**
- E (j,T) = Eo*( Ec/Eo)^ β/α(77K)*jc(77K)/jc(T)*( j / jc(77K))^ β
- **Regime 3**
- E (j,T) = p(Tc)*T/Tc*j

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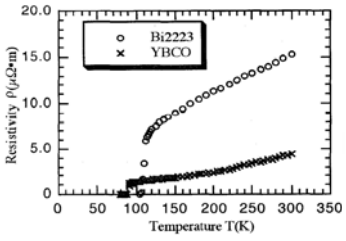
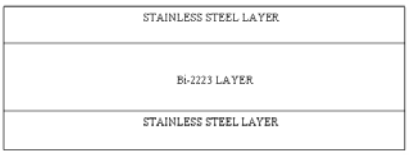
# Superconductor used for HTSFCL

- Bi2223
- YBCO




Layout of HTSFCL




V =11KV

I = 1KA

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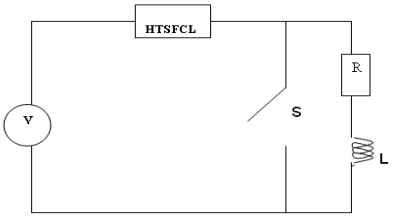
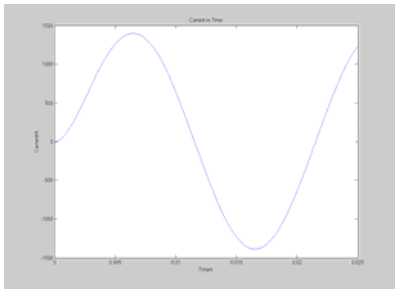
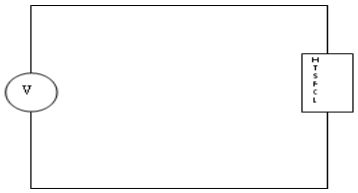
# Results

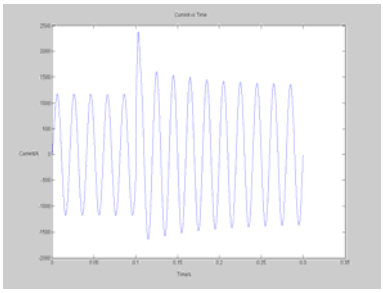
## Normal



## Under Fault



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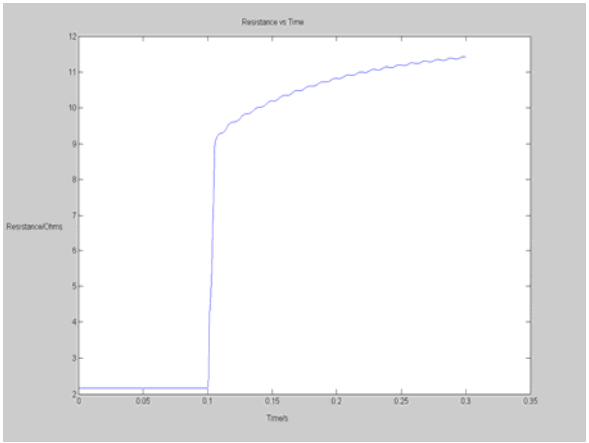
# Results

## Time vs Resistance

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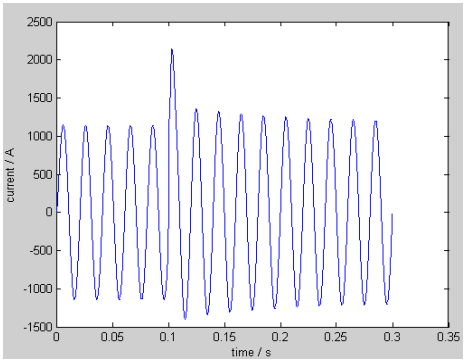
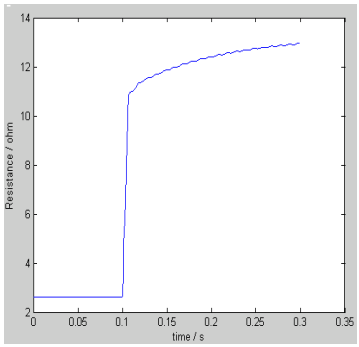
# Results with different lengths of HTSFCL

- Length =12m

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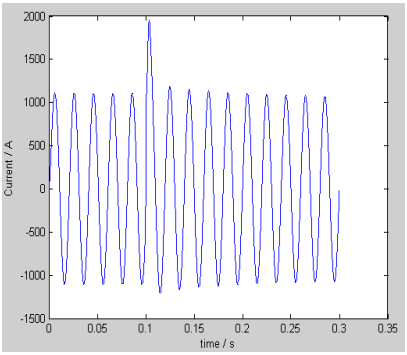
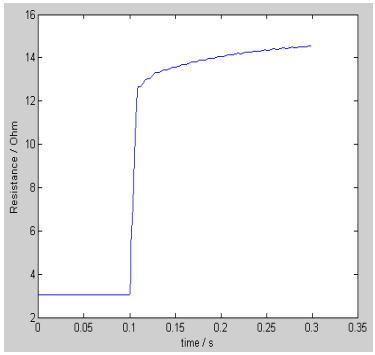
# Results

- Length=14m

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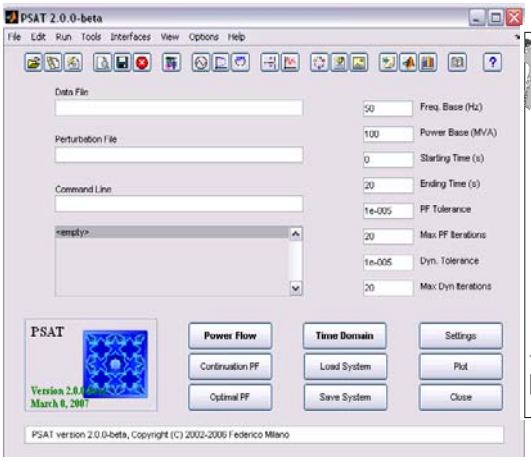
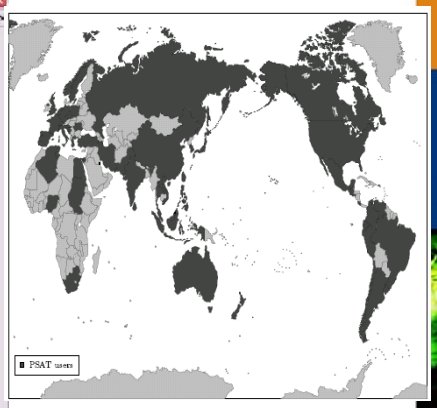
# PSAT

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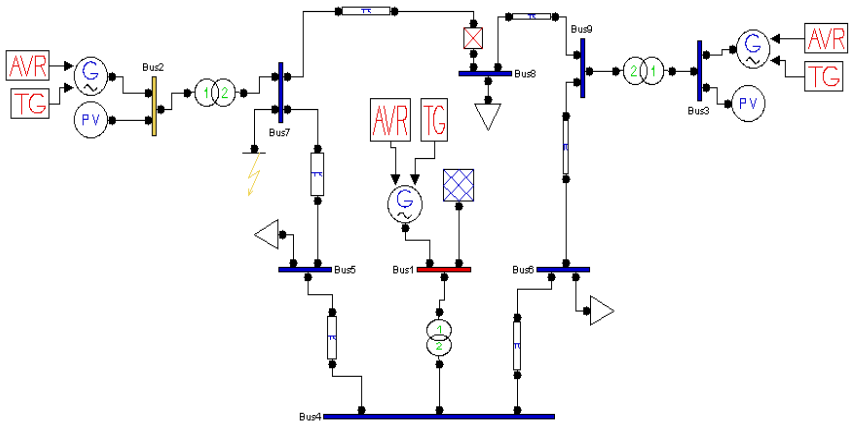
# Modelling In PSAT

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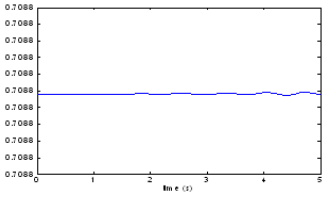
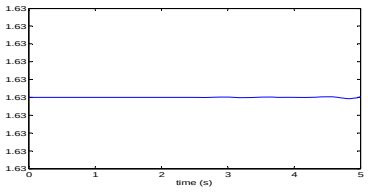
# Normal Operation

## Power at Buses

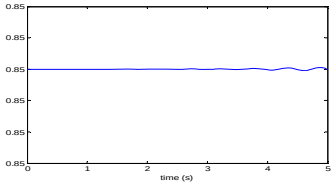
Bus1 _P



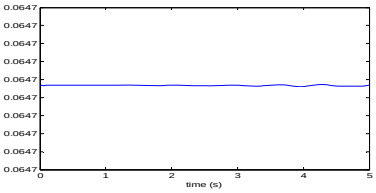
Bus2_P




- BusP_3




- BusQ_4

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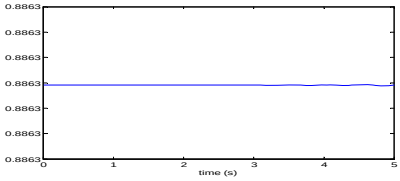
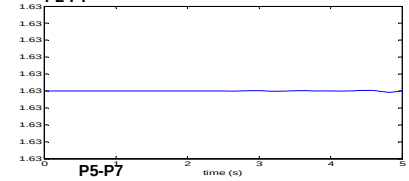
# Normal Operation

## Power flow

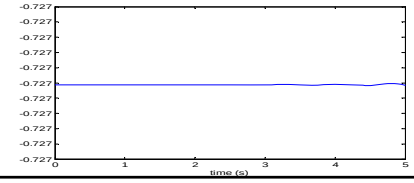
- P7-P8



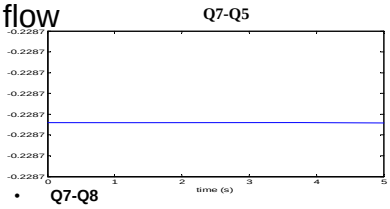

- P2-P7



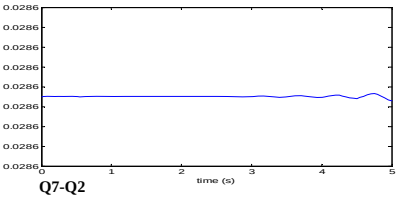

P5-P7



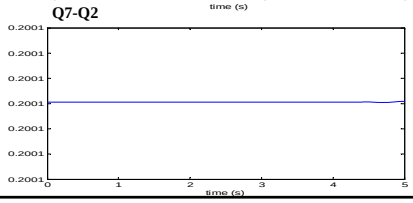

Q7-Q5




- Q7-Q8




Q7-Q2

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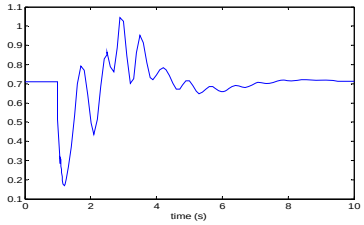
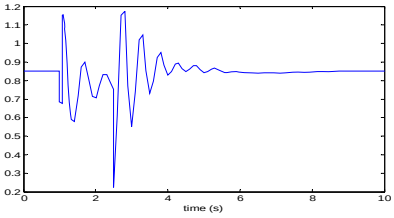
# During Fault

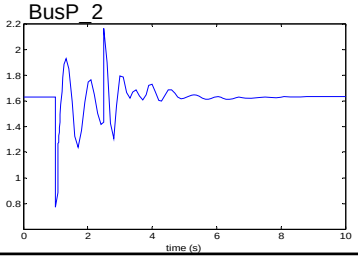
» BusP_1



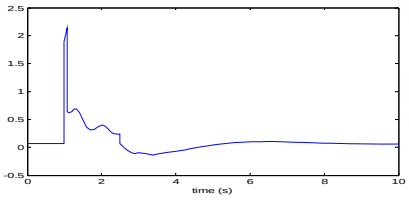

• BusP_3




• BusP_2




• BusQ_4

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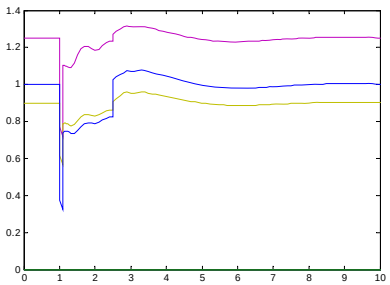
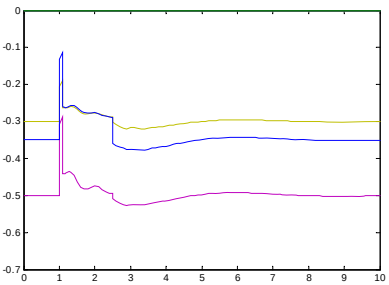
# During fault

- P_5,7,8



Q_5,7,8



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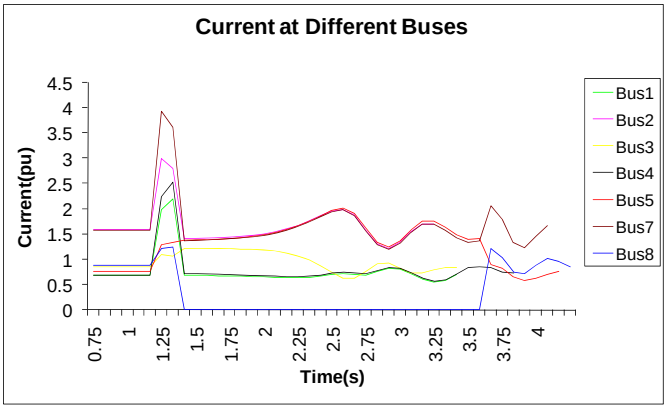
# Investigating the Optimum location of HTSFCL

- Current During Fault at different Buses

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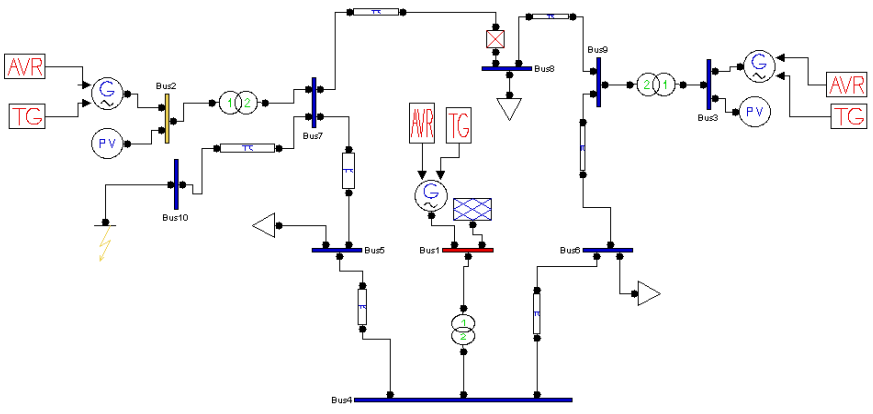
# Investigating the Optimum location of HTSFCL

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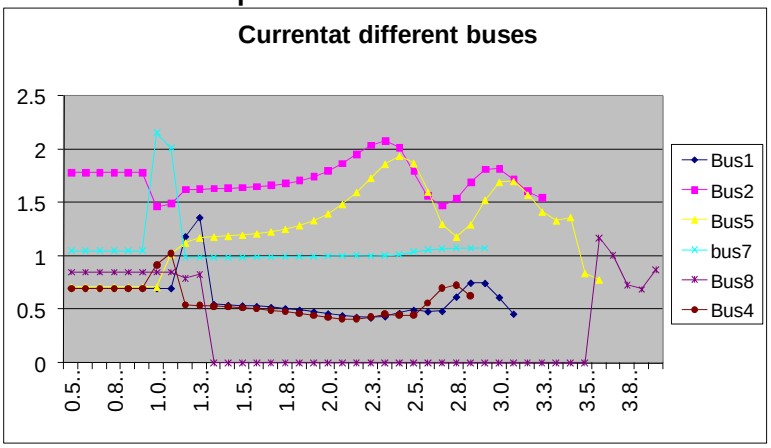
# Investigating the Optimum location of HTSFCL

## Increase in impedance

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# Conclusions

- Circuit analysis of FCL was performed using the magnetic circuit method
- Flux distribution of FCL has been analyzed in FEMLAB
- Expected current limit characteristics were obtained experimentally
- Thermal model of the FCL is obtained and analyzed
- Experimental results are close to the ideal characteristics.

**Future work**

- Performance improvement and optimum design procedure.
- Application to high voltage system in NZ.

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# *Thank you*

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