THE DEVELOPMENT OF A PULSE RF HIGH POWER AMPLIFIER FOR A PORTABLE NMR SPECTROMETER

TIANYANG TED JIANG

2008

THE DEVELOPMENT OF A PULSE RF HIGH POWER AMPLIFIER FOR A PORTABLE NMR SPECTROMETER

A thesis presented in partial fulfillment of the requirement for the degree of Master of Engineering at Massey University

TIANYANG TED JIANG

2008

ABSTRACT

The RF high power amplifier is a key module in the NMR spectrometer. Robustness, lower power consumption, and small size are requirements. In this thesis, devices are studied and different design approaches are considered. New ideas are introduced, and simulations are used to show if it these work. A real prototype is developed. Results from the prototype are satisfactory and in good agreement with the simulation results. This allows for the possibility of a real portable NMR spectrometer 'Lapspec'.

Points of note:

- Feedback to stabilize amplifier,
- Hard bias to improve rise time of pulse,
- A rugged device is chosen,
- Power limiter technology is used to avoid overdrive amplifier,
- Lower value attenuator at output of final stage to reduce load VSWR,
- Reason of spike is studied, the solution to reduce spike is given,
- The reason of instability of amplifier with NMR load is analyzed,
- A method is introduced to ensure there is no oscillation while the High Power Amplifier (HPA) is connected with the NMR probe.

ACKNOWLEDGMENTS

I would like to express my utmost thanks and gratitude to my supervisor Associate Professor Subhas C Mukhopadhyay for the opportunity for my Master degree, for guiding me in the research work, and for emotional support.

I would also like to thank Dr Robin Dykstra, another supervisor, for initiation, technical and financial guidance and support, as well as milestone checking and encouragement.

I thank Dr. Craig Eccles for general academic advice, helpful discussion, and valuable suggestions in my thesis writing. I really enjoyed the time working with him.

I also thank Dr. Andrew Coy, CEO of Magritek and Foundation for Research, Science & Technology of New Zealand for financial support in this project.

Thanks to Rob Ward, John Zisong Zhen, Dafnis and Alan for support in PCB design software, MS Word and photo processing, also mechanical work.

Finally, I would thank my wife, my son and my younger brother for their love, patience, constant support and encouragement.

CONTENTS

ABSTRACT 1-3

ACKNOWLEDGMENTS 1-4

CONTENTS 1-5

LIST OF FIGURES 1-9

LIST OF TABLES 1-13

1 CHAPTER ONE 1-15

INTRODUCTION 1-15

1.1 HPA and portable NMR system 1-15

1.2 Robustness of design 1-16

1.3 Pulse mode 1-17

1.4 Rise time and spike 1-17

1.5 Size 1-17

1.6 Power consumption 1-17

1.7 Search in market 1-17

1.8 Conclusion 1-18

2 CHAPTER TWO 2-19

SPECIFICATION AND DESIGN 2-19

2.1 Specification 2-19

2.2 Block diagram 2-21

2.3 Design principle of robust HPA 2-22

2.4 Choose key components 2-22

2.4.1 Criteria 2-22

2.4.2 BJT vs. MOSFET: 2-23

2.4.3 Pulse vs. CW: 2-24

2.4.4 High frequency device vs. low frequency device 2-25

2.4.5 Gate leakage vs. lift time 2-25

2.4.6 High voltage device vs. low voltage device 2-25

2.4.7 List of final stage device 2-25
2.4.8 List of devices for drive stage 2-26
2.4.9 List of devices for pre-drive stage 2-27
2.4.10 FET safe rules 2-28
2.5 RF shield 2-29
2.6 Thermal 2-29
2.7 Structure 2-29
2.8 Cost 2-29
2.9 Design transformer 2-29
3 CHAPTER THREE 3-31
SIMULATION 3-31
3.1 Introduction 3-31
3.2 Pre-drive stage 3-32
3.2.1 Introduction 3-32
3.2.2 SGA7489 3-32
3.3 Drive stage 3-35
3.3.1 Introduction 3-35
3.3.2 Push-pull with parallel SGA7489 3-36
3.4 Final stage 3-38
3.4.1 Introduction 3-38
3.4.2 Specification 3-39
3.4.3 Design procedure 3-39
3.4.4 New approach 3-39
3.4.5 Output match 3-40
3.4.6 Input match 3-41
3.4.7 Design and simulation 3-42
3.4.7.1 Initial circuit and simulation 3-42
3.4.7.2 DUT with negative feedback 3-53
3.4.7.3 DUT with hard bias and negative feedback 3-58
3.4.7.4 Discussion and optimum 3-65

3.4.7.5 Summary 3-71
3.5 Study of the final stage 3-72
3.5.1 Formula vs. simulation for the max Po 3-72
3.5.2 The Rise time vs. the LP of the output transformer 3-72
3.5.3 Spike vs. Idq 3-72
3.6 NMR probe as a part of HPA Principle 3-73
3.6.1 Principle 3-73
3.6.2 Initial results 3-75
3.6.3 Optimum results 3-77
3.6.4 Summary 3-79
3.7 ATT vs. load VSWR (Voltage Standing Wave Ratio) 3-79
3.7.1 Issue 3-79
3.7.2 Options and discussion 3-80
3.7.3 Solution 3-80
4 CHAPTER FOUR 4-82
FABRICATION AND EXPERIMENTS 4-82
4.1 Introduction 4-82
4.2 PCB and module 4-82
4.3 Boost 4-83
4.3.1 Introduction 4-83
4.3.2 Schematic and layout 4-84
4.3.3 DC operating voltage 4-87
4.3.4 Test gain 4-88
4.3.5 Test waveform 4-90
4.3.6 Test linearity of DUT 4-96
4.3.7 VSWR of DUT 4-101
4.3.8 Conclusion 4-104
4.4 Final stage and whole HPA 4-105
4.4.1 Schematic 4-105

4.4.2 Gate voltage without FET 4-106
4.4.3 FET and shield 4-107
4.4.4 One pulse test 4-107
4.4.5 Optimum Vgs 4-113
4.4.6 Gain and VSWR at lower power with frequency sweep 4-116
4.4.7 One pulse test for max safe Po at 50 ohm load 4-117
4.4.8 Linear test 4-119
4.4.9 Tolerance of output 4-122
4.4.10 Duty cycle test 4-123
4.4.11 Robustness test with 3 dB ATT plus Mole 4-124
4.4.12 Robust test with 1.5 dB ATT plus Mole 4-126
4.5 NMR experiment 4-127
4.5.1 Noise of power supply vs. NMR experience 4-127
4.5.2 NMR experience 4-128
4.6 Summary 4-129
5 CHAPTER FIVE 5-130
SUMMARY OF FINDINGS AND DISCUSSION 5-130
5.1 Feedback 5-130
5.2 Hard bias and combination of hard bias and feedback 5-130
5.3 ATT to reduce equivalent load VSWR 5-131
5.4 Real NMR probe as a load of HPA 5-131
6 CHAPTER SIX 6-133
IMPROVEMENT 6-133
6.1 Reduce power consumption by a pulse drive stage 6-133
6.2 Temperature compensation in bias 6-133
6.3 LED indication 6-134
7 CHAPTER SEVEN 7-135
CONCLUSION 7-135
8 REFERENCES 8-137

LIST OF FIGURES

Figure 1.1: HPA in NMR system 1-16

Figure 1.2: Load VSWR of the Mole, a typical NMR probe 1-16

Figure 2.1: Different NMR probes, (a) Mole for 3.26MHz and 100W, (b) Profile Mouse for 19MHz and 100W, (c) Cuff Magnet for 24MHz and 10W, (d) Mini probe for 30MHz and 10W, (e) Halbach for 12MHz and 10W, (f) Mouse for 19MHz and 100W 2-20

Figure 2.2: HPA block diagram 2-22

Figure 3.1: Single end 3-32

Figure 3.2: Gain and stable, Pi=-10dBm 3-33

Figure 3.3: Input power sweep, F=1-30MHz 3-34

Figure 3.4: Stable factor is 1.15 for R8 =10 ohm 3-35

Figure 3.5: Push-pull with a single device 3-36

Figure 3.6: Push-pull with parallel 3-36

Figure 3.7: Po-1 and Gain, push-pull with parallel, 1-30MHz 3-37

Figure 3.8: Frequency response, push-pull with parallel 3-37

Figure 3.9: The initial DUT of last stage 3-42

Figure 3.10: Simulation setting 3-44

Figure 3.11: Pulse result of the initial DUT, 8MHz, Pi=27dBm 3-45

Figure 3.12: Pulse result of the initial DUT, 8MHz, 29dBm 3-50

Figure 3.13: Gain and stable, initial DUT, P1=10 dBm 3-52

Figure 3.14: Gain and stable, initial DUT, Pi=27 dBm 3-52

Figure 3.15: Gain and stable, feedback, Pi=27 dBm 3-53

Figure 3.16: Gain and stable, feedback, Pi=10 dBm 3-54

Figure 3.17: Modified DUT for CW gain and stable 3-55

Figure 3.18: Gain and stable, Pi=10dBm 3-55

Figure 3.19: Pulse result, 8MHz, Pi=27 dBm 3-57

Figure 3.20: DUT with hard bias and feedback 3-59

Figure 3.21: Pulse result with hard bias, 8 MHz, Pi=30 dBm, L21/L22=10 uH 3-60

Figure 3.22: Pulse result with hard bias, 8 MHz, Pi=30 dBm, L21/L22=5.6 uH 3-61

Figure 3.23: Pulse result with hard bias, 8 MHz, Pi=10 dBm, L=5.6 uH 3-63

Figure 3.24: Gain and stable, Pi=10 dBm, 10 KHz to 30 MHz with step size 10 KHz 3-64

Figure 3.25: Gain and stable, Pi=30dBm, 10 KHz to 30 MHz with step size 10 KHz 3-65

Figure 3.26: Output impedance, no feedback, Pi=10 dBm 3-66

Figure 3.27: Output impedance, no feedback, Pi=30 dBm 3-66

Figure 3.28: Stable and VSWR, C55/C56=100 nF 3-67

Figure 3.29: Stable and VSWR, C55/C56=2000 nF 3-68

Figure 3.30: Pulse result, 8 MHz, Pi=30 dBm, gate bias drive 13.3 Vpp 3-69

Figure 3.31: Pulse result, 8 MHz, Pi=30 dBm, gate bias drive 10 Vpp 3-70

Figure 3.32: New DUT-1 3-71

Figure 3.33: Relationship of spikes 3-73
Figure 3.34: Reflection gain illustration 3-74
Figure 3.35: Set up for analysis of reflection performance 3-75
Figure 3.36: Final stage in original condition 3-76
Figure 3.37: HPA reflection with SGA7489+L8821P+SR401 in original condition (Lm=1.5uH) 3-77
Figure 3.38: SR401 stage 3-78
Figure 3.39: Reflection of HPA with optimum circuit 3-78
Figure 3.40: VSWR of the Mole 3-79
Figure 3.41: VSWR vs. ATT in experience 3-81
Figure 4.1: PCB and assembly 4-83
Figure 4.2: Heat sink 4-83
Figure 4.3: Pre-drive stage, 1 of 3 of boost 4-84
Figure 4.4: Drive stage, 2 of 3 of boost 4-85
Figure 4.5: DC power supply of boost, 3 of 3 of boost 4-86
Figure 4.6: Boost PCB Rev2.0, 35 mmX84 mmX1.5 mm, double side copper FR4 4-86
Figure 4.7: Boost rev2.0, 85 mmX36 mmX18 mm 4-87
Figure 4.8: DUT and system setting for testing gain 4-88
Figure 4.9: Gain at Pi=-60dBm 4-89
Figure 4.10: Gain with different Pi level 4-89
Figure 4.11: Test setting with 50 ohm load 4-90
Figure 4.12: Vo on 50 ohm of Boost Rev2.0 at 8 MHz, (a) Pi=-10 dBm, (b) Pi=-8 dBm, (c) Pi=-5 dBm, (d) Pi=0 dBm 4-91
Figure 4.13: Vo on 50 ohm of Boost Rev2.0 at 1MHz, (a) Pi=-10 dBm, (b) Pi=-8 dBm, (c) Pi=-5 dBm, (d) Pi=0 dBm 4-92
Figure 4.14: Vo on 50 ohm of Boost Rev2.0 at 25 MHz, (a) Pi=-10 dBm, (b) Pi=-8 dBm, (c) Pi=-5 dBm, (d) Pi=0 dBm 4-93
Figure 4.15: Waveform of Vo (ch1) on 50 ohm at Pi=-10 dBm, Gate blanking (ch2), (a) 1 MHz, (b) 8 MHz, (c) 25 MHz 4-94
Figure 4.16: Waveform of Vo (ch1) on 50 ohm at Pi=0 dBm, Gate blanking (ch2), (a) 1 MHz, (b) 8 MHz, (c) 25 MHz 4-95
Figure 4.17: Rise edge of Vo (ch1) at 8 MHz and Pi=0 dBm, gate blanking (ch2) 4-96
Figure 4.18: Test DUT linear 4-97
Figure 4.19: Check test system linear 4-98
Figure 4.20: Calibration Vi 4-98
Figure 4.21: Calibration output voltage 4-98
Figure 4.22: Check test system linear at 8 MHz 4-99
Figure 4.23: DUT linear at 8 MHz, Po-1=28 dBm 4-99
Figure 4.24: Output voltage waveform at 8 MHz and Pi=-5 dBm 4-100
Figure 4.25: (a) DUT and 40 dB ATT, (b) Calibration input voltage, (c) Kea and Oscilloscope, (d) DC power supply and reading 4-101

Figure 4.26: Test setting of input VSWR of DUT 4-102
Figure 4.27: Test setting of output VSWR 4-102
Figure 4.28: Input VSWR of DUT 4-103
Figure 4.29: (a) Test input VSWR, (b) Test output VSWR 4-104
Figure 4.30: Output VSWR of DUT 4-104
Figure 4.31: Schematic of DUT 4-106
Figure 4.32: Vgs without FET, max PM position, Vc=10 V 4-106
Figure 4.33: Final stage layout 4-107
Figure 4.34: Shield of last stage 4-107
Figure 4.35: Setting, 1 of 2 4-108
Figure 4.36: Setting, 2 of 2 4-108
Figure 4.37: Vo (ch1X10) and Vi (ch2X10) at TX=-30, (a) 2MHz, (b) 8 MHz, (c) 25 MHz 4-109
Figure 4.38: Test VSWR at 8 MHz and TX=-30, (a) Vf, (b) Vr, (c) Outline of Vf, (d) Outline of Vr4-110
Figure 4.39 Waveform of Vi (ch1X10), Vo (ch2X10) and gate blanking (ch3), (a) Rise edge of Vo, (b) Fall edge, (c) Vi and Vo at rise edge, (d) Envelope 4-111
Figure 4.40: Vgs (DC) and Vds (AC) at Vc=8 V and max position of MP, (a) Vgsh, (b) Vgsl, (c) Vdsh, (d) Vdsl 4-112
Figure 4.41: Vdsl detail 4-113
Figure 4.42: Rise time and spike at 8 MHz and TX=-20, Vf (ch1), Vo (ch2), Vgsh (ch3), (a) Vgsh, (b) Vf, Vo and Vgsh, (c) Vf, Vo and gate blanking, (d) Vf and Vo 4-115
Figure 4.43: Setting delay 4-115
Figure 4.44: Experienced rise time and spick at 8 MHz and TX=-20, Vf (ch1), Vo (ch2), Vgsh (ch3), (a) Delay 4 us, (b) Delay 3 us, (c) Delay 2 us. (d) Delay 1 us 4-116
Figure 4.45: Gain 4-117
Figure 4.46: VSWR 4-117
Figure 4.47:Vo (ch2) and Vf (ch1) (a) TX=-20, (b) TX=-10, (c) TX=-8, (d) TX=-6 4-118
Figure 4.48: Test system linearity at 8 MHz 4-119
Figure 4.49: Linearity of DUT at 8MHz 4-120
Figure 4.50: Vo at max sweep input, (a) 2 MHz, TX=-10, (b) 8 MHz, TX=-10 (c) 25 MHz, TX=-64-121
Figure 4.51: Waveform at 25MHz and max sweep input (TX=-6), (a) Vo, (b) Vf 4-122
Figure 4.52: SW setting 4-123
Figure 4.53: Vi (ch1) and Vo (ch2), (a) One pulse, (b) DC=4.6%, (c) DC=8.5%, (d) DC=12.8%4-124
Figure 4.54: DUT and test system 4-125
Figure 4.55: SW used and setting 4-125
Figure 4.56: Robust test at 195 W 4-126
Figure 4.57: Robust test at 184 W 4-126
Figure 4.58: Warm up HPA setting 4-127
Figure 4.59: CPMG-16 echo, 12.3 MHz, new Halbach 1#, 1# HPA R3.0 4-128
Figure 4.60: T1 sat, 12.3 MHz, new Halbach 1#, 1# HPA R3.0 4-128
Figure 4.61: T1 add, 12.3 MHz, new Halbach 1#, 1# HPA R3.0 4-129

Figure 7.1: (a), (b) and (c) HPA, (d) HPA in Kea NMR spectrometer 7-136

LIST OF TABLES

Table 1.1: Performance summary of HPA venders 1-18
Table 2.1: The specification of the HPA 2-20
Table 2.2: Bipolar transistor and RF power MOSFET characteristics when used as RF amplifiers [1] 2-23
Table 2.3: Device list of final stage 2-26
Table 2.4: Device list of drive stage 2-27
Table 2.5: List of devices for pre-drive stage 2-28
Table 3.1: Compare single and parallel device in push-pull 3-38
Table 3.2: Load line vs. Po-1 3-41
Table 3.3: The meaning of the sub-figure a) 3-46
Table 3.4: The meaning of the sub-figure b) 3-46
Table 3.5: The meaning of the sub-figure c) 3-47
Table 3.6: The meaning of the sub-figure d) 3-47
Table 3.7: The meaning of the sub-figure e) 3-47
Table 3.8: The meaning of the sub-figure f) 3-47
Table 3.9: The meaning of the sub-figure g) 3-48
Table 3.10: The meaning of the sub-figure h) 3-48
Table 3.11: The meaning of the sub-figure i) 3-48
Table 3.12: The meaning of the sub-figure j) 3-48
Table 3.13: The summary of the meaning of the frequency domain figure 3-51
Table 3.14: Impedance of SRC 3-58
Table 3.15: Gain vs. gate resistor 3-67
Table 3.16: Fine tuning Vgs 3-72
Table 3.17: Formula vs. simulation for the max Po 3-72
Table 3.18: Equivalent VSWR vs. ATT 3-81
Table 4.1: DC operating voltage 4-87
Table 4.2: Test order and term matrix 4-97
Table 4.3: Po-1 and Gain summary 4-100
Table 4.4: Gain and in VSWR 4-109
Table 4.5: OutVSWR 4-110
Table 4.6: Waveform and Gain vs. TX 4-113
Table 4.7: Gain and Po vs. Vgs 4-114
Table 4.8: Cold stat 4-114
Table 4.9: Linear vs. TX 4-118
Table 4.10: Po-1 of DUT 4-120
Table 4.11: xdB compression output of DUT 4-120

Table 4.12: Tolerance Po, G and Pi 4-122
Table 4.13: Vo vs. duty cycle 4-123

1 CHAPTER ONE

INTRODUCTION

1.1 HPA and portable NMR system

The portable **Nuclear Magnetic Resonance** (NMR) system has a similar block diagram as a normal NMR system, as shown in Figure 1.1.

The NMR spectrometer works in a similar way to radar. It sends a short radio frequency (RF) pulse to the sample. Once the sample is stimulated, it will produce an echo signal, which contains the information of the sample's structure. The receiver picks up the echo signal and amplifies it. Then the signal is processed and displayed on the screen for people to analyze the sample. The probe works as an antenna. It transmits the RF power to the sample and receives the echo signal from the sample. The duplexer co-operates with the transmitter and the receiver. It allows the transmitting signal to pass to the probe and protects the receiver during the transmitting mode. It allows the echo signal from the probe to pass to the receiver without loss and blocks any noise and interference from the transmitter.

The **High Power Amplifier** (HPA) is located between the duplex and the TX transmitter in the transmitter chain. It boosts the RF pulse power to a high level so that a sample can be stimulated. Typically, the power level is over 100 W.

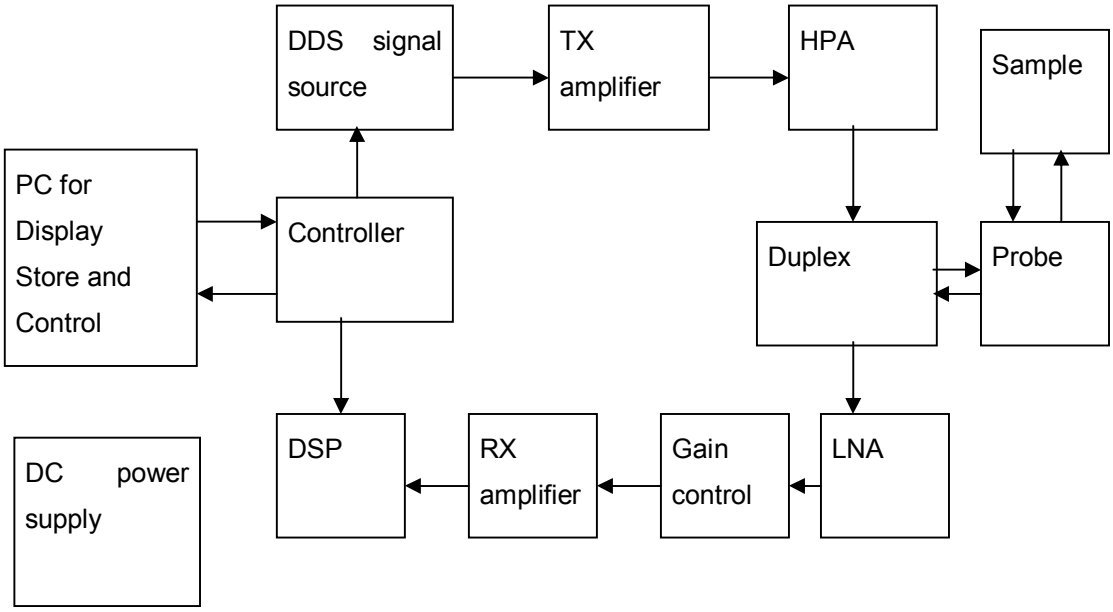


Figure 1.1: HPA in NMR system

1.2 Robustness of design

The Figure 1.2 shows that the load Voltage Standing Wave Ratio (VSWR) of the NMR probe is poor. The HPA will work on the high VSWR condition for most of the time. The bandwidth of VSWR 3:1 is only 1%! It is different from the way the HPA works under telecommunication or radar, where the bandwidth is typically more than 10%. The HPA should withstand this high VSWR without any damaging or degradation.

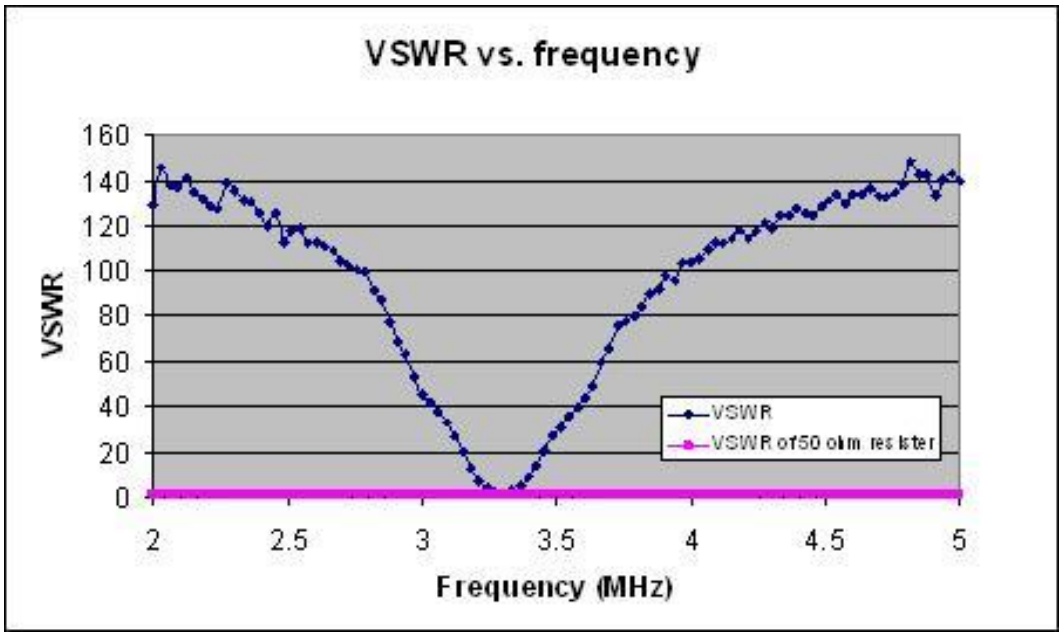


Figure 1.2: Load VSWR of the Mole, a typical NMR probe

1.3 Pulse mode

The NMR works with pulse excitation. The maximum duty cycle is about 10%. The gate blanking is used to turn off the HPA while no RF signal is coming. This significantly reduces power consumption. For a portable NMR spectrometer, it is the only way for the HPA to work.

1.4 Rise time and spike

The rise time is a measurement of how fast the output reaches the very close (90%) to the steady state value for the first time. The fast response is very important for the NMR system. The rise time should be less than 2 microsecond. The rise time should be much faster than that of a portable telecommunication equipment.

There is a large current in the HPA. It will produce a spike according to the basic physics principle. The higher the current is and faster the HPA switches, the higher the spike will be. The spike works as an additional RF signal. It adds the interference in the NMR experiment. The spike should be as low as possible.

1.5 Size

The size of the HPA is a key requirement for a portable NMR spectrometer. The whole instrument looks like a laptop PC. The space for the HPA is only 160 mm X100 mm X 80 mm including heat-sink.

1.6 Power consumption

The power consumption should be as low as possible from the thermal consideration and the battery lifetime.

A 24V DC voltage is supplied. This limits the range of the RF power devices that could be chosen.

1.7 Market Search

Table 1.1 is the result of a market search for a similar HPA.

Table 1.1: Performance summary of HPA vendors

Issue	Vendor	Frequency	Power	GB	VSWR pro	Pd	Size	PS	Cost
		MHz	W					V	US$
	Spec	1 to 30	100 to200	Yes	100/1	Low	Small	24	3000
Size, PS, robust	EMPower	1-100	300	No			Middle	110	6000
Size, GB	MiniCircuit	20-500	100	No			Middle	110	1500
Size, freq	Comtech	150 to 450	2000	Yes			Big	220	
Po, Pd, size, PS	AR Worldv	1 to 1000	40	No	Yes	High	big	220	
Freq, Size, PS	HotTek	0.01 to 10	200	Yes	Yes	Low	Big	130	
GB, Pd,Size, PS	E&I	0.3 to 35	150	No	Yes	High	Middle	220	
Size, PS	CPC	0.5 to 30	250	yes	Yes	?	Big	220	
Size, Pd, GB	Harris	1.6 to 29	400	No	Yes	High	Big	26	
Size, PS, Pd,robust	Tomco 1	1 to 150	200	Yes	No	Middle	Middle	48	5000
Size, Pd, PS	Tomco 2	2 to 30	200	Yes	Yes	High	Big	48	5000
GB, Pd, size	Acom	1.6-29	400	No	Yes	High	Big	26	
Big, PS	AMT	6-600	200-1000	Yes			Big	230	
Po, Size,GB	OPHIR-RF	1 to 1000	30	No			Middle	28	
Size, GB	DJM	0.15 to 230	150	No			Big		
Interested	Herley	6 to 220	300						

Notice:
GB: gate blanking for pulse to save power
Pd: DC power comsumption
PS: DC power supply voltage
Size: specification is 160X100X40mm; small is close to specification;Middle and big is far away specificatio
Linear power is Po-1

The Cell with red color means that this term doesn't meet the requirement. The main issues are:

- No gate blanking
- Too much DC power consumption
- Big size

1.8 Conclusion

There is no product available in the market which meets the above requirement. So there is a need to develop the HPA of above specification. The subsequent chapters will describe the design, development, fabrication and testing of the required system.

2 CHAPTER TWO

SPECIFICATION AND DESIGN

2.1 Specification

A summary of the specification is shown in the Table 2.1. In this chapter the necessary steps to finalize the specification are discussed.

The output power is based on the NMR probe, the frequency and the sample volume. To get a clear echo from the NMR sample, the NMR sample needs to be stimulated with enough RF power. The RF power applied on the sample depends on the quality of the NMR probe and the power fed in the probe. The higher the quality of a coil is the more power the sample receives. The quality of a coil depends on its structure and its frequency of operation. For the one side NMR probe at 3.3 MHz, Mole, the quality factor is only about 10. For Halbach array at 12.3 MHz, the quality is about 1000. Both of the Mole and the Halbach are the NMR load of this HPA. The HPA needs more power for a Mole. From calculation, the max power needed is around 60 to 80 W. With some margin, the power specification of the HPA is kept at 100 to 200 W.

Because the HPA will work with the NMR probe and its VSWR is high, the HPA should withstand this high VSWR. So the load VSWR specification is set at 20:1.

The power consumption should be lower and size should be small for a portable NMR spectrometer.

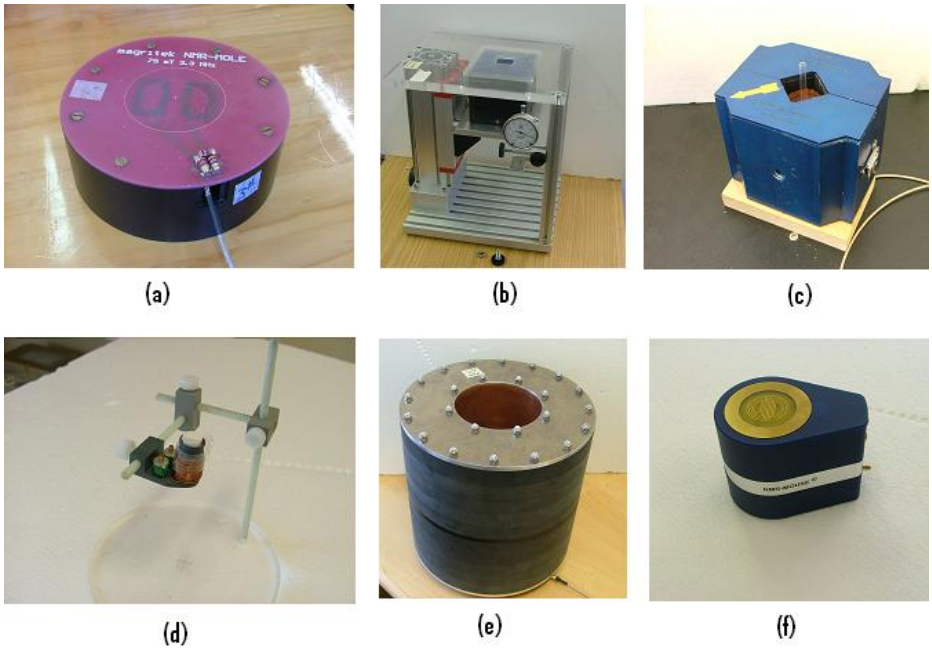


Figure 2.1: Different NMR probes, (a) Mole for 3.26MHz and 100W, (b) Profile Mouse for 19MHz and 100W, (c) Cuff Magnet for 24MHz and 10W, (d) Mini probe for 30MHz and 10W, (e) Halbach for 12MHz and 10W, (f) Mouse for 19MHz and 100W

Table 2.1: The specification of the HPA

			Specification		
Term	**Description**	**Unit**	**LSL**	**Typ**	**HSL**
Key specification:					
Frequency range		MHz	1		30
Output pulse power with 1dB compression		W	200		
Power consumption with pulse off		W			3
Load VSWR at any angle for ruggedness			1		20
Small size and light weight				Yes	
Other specification:					
Max output power		W	250		
Gain flatness		dB			1
Max pulse width		us			80
Min pulse width		us	1		
Max duty cycle					20%
Pulse repeat rate		KHz		1	
Input power	On 50 Ohm load	dBm	0		
DC power voltage		V		24	
Length of HPA		mm			160
Width of HPA		mm			100
Thick of HPA		mm			50
Turn on time		ns			1
Turn off time		ns			1
Shunt down final stage or all stage while pulse off				Yes	
Noise figure		dB			8
Phase stability	with different power, freq, pulse width	Degree			5
Input impedance				50	
Input impedance				50	
Even Harmonic	200W	dBc			-30
Odd harmonics	200W	dBc			-20
Spurious		dBc			-70
Gate trigger				TTL	
Input VSWR			1		4
Protection circuit				Yes	

2.2 Block diagram

We will estimate how many stages are needed and which topology is chosen.

First, we discuss stage structure. Output power of the HPA is 200 W or 53 dBm. Max out power from transmitter (TX) is 0 dBm. So total gain of the HPA is: G=Po-Pi = 53 dBm-0 dBm = 53 dB. If keeping 10 dB gain margin, total gain is 63 dB. For RF power FET, gain is about 13-17 dB at High VHF or lower UHF, say 150-250 MHz. But when frequency is down to HF band (0.3-30 MHz), gain could be up over 30 dB. For stable operation gain should be controlled between 20-30 dB at HF band. If mono microwave integrated circuit (MMIC) is used, gain is about 15-24 dB. As a summary, gain of each stage at HF band is about 20 dB. Number of stage is n=63/20=3. This means that the HPA is built by 3 stages of amplifier.

Second, we discuss topology of the amplifier. There are three kinds of amplifier topology for each stage: single, push-pull, and balance. Single is simple, but harmonic components are high. In pulse mode the spike, which is caused by the rising and falling edge of the bias current, will be high. Push-pull uses two devices which have their Phase 180 degrees out, so that odd harmonic is cancelled. The RF waveform is more close to sinusoid at high power level, and the spike is minimum if the circuits are symmetrical. Phase is 90 degrees different for a balanced amplifier. If there is a mismatch between load and output of the amplifier, the reflection power from the load will be back to the amplifier and never back to load. So from the load point of view, output impedance of the amplifier is 50 ohm. The question of interest to us: is there any reflection power from mismatched load? This reflection power may damage RF power FET. Unfortunately, the answer is yes - there is reflection power. In addition, output power and gain is lower than push-pull due to higher loss of 90 degree phase combination. The loss is about 1-2 dB. As a reference, loss of 180 degree phase combination is less than 0.5 dB. In summary, the best topology is push-pull. Another advantage of push-pull is that it can increase output power. This gives us the chance to use a low cost lower power device to reach higher power, which previously used an expensive high power device.

The block diagram of the HPA is shown in Figure 1.1. ATT after pre-drive improves the match between two amplifier stages. Output ATT is a buffer between HPA and NMR load to protect the HPA.

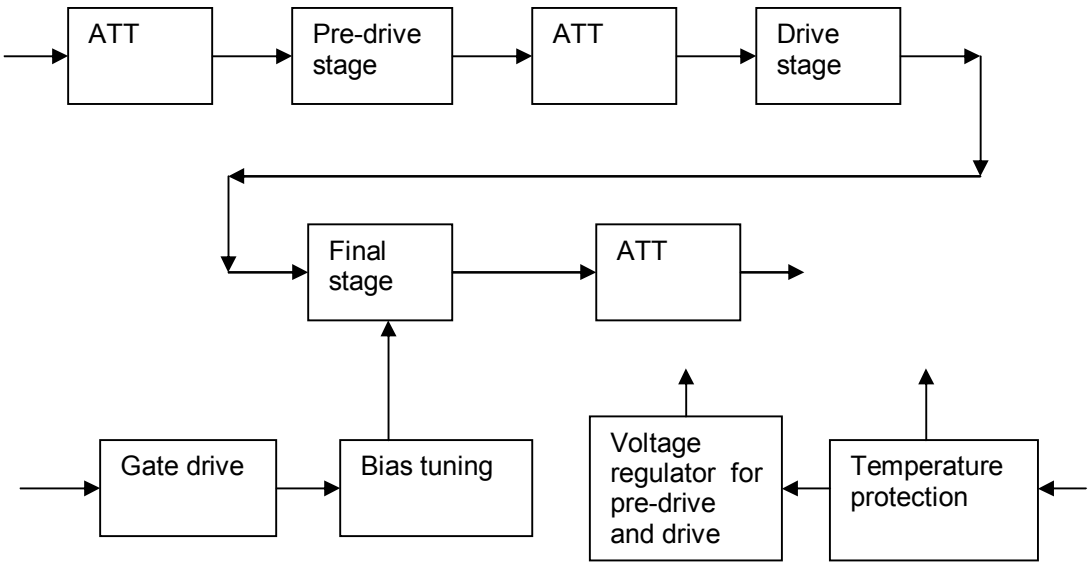


Figure 2.2: HPA block diagram

2.3 Design principle of robust HPA

- Avoid over drive amplifier
- Choose robust device
- Insert an attenuator between output of final stage and NMR load to reduce equivalent load VSWR
- Good input match while cascaded with previous stage
- Class A
- Stable check
- In design process, view NMR load as a part of final stage
- Working in linear zone as much as possible.

2.4 Choice of key components

2.4.1 Criteria

- Output power
- Gain
- Band
- Pulse mode
- Ruggedness (withstand with load mismatch)
- Stability (mainly depends on device itself)
- Cost
- Repeatability

- Credit (or reputation) of vendor
- Simple circuit
- Supply available for long term

2.4.2 BJT vs. MOSFET:

There are two kinds of transistors for solid state RF power: bipolar junction transistor (BJT) and field effect transistor (FET).The vertical channel silicon MOSFET is the most common RF power FET.

Table 2.2: Bipolar transistor and RF power MOSFET characteristics when used as RF amplifiers [1]

Characteristic	BJT	MOSFET
Zin, Rs /Xs (2.0 MHz)	3.80-j2.0 Ohm	19.0-j3.0 Ohm
Zin, Rs /Xs (150 MHz)	0.40+j1.50 Ohms	0.60-j0.65 Ohms
Z_{OI} (Load Impedance)	Nearly equal for each transistor, depending upon supply voltage and power output	Save as left
Biasing	Not required, except for linear operation. High current (I_C / h_{FE}) constant voltage source necessary.	Required for linear operation. Low current source, such as a resistor divider, is sufficient. Gate voltage can be varied to provide an automatic gain control (AGC) function.
Linearity	Low order distortion depends on electrical size of the die, geometry, and h_{FS}. High order intermodulation distortion (IMD) is a function of type and value of emitter ballast resistors.	Low order distortion worse than with bipolars for a given die size and geometry. High order IMD better due to lack of ballast resistors and associated nonlinear feedback.
Stability	Instability mode known as half f_o troublesome because of varactor effect in base-emitter junction. Higher ratio of feedback capacitance versus input impedance.	Superior stability because of lack of diode junction and lower ratio of feedback capacitance versus input impedance.

Ruggedness	Usually fails under high current conditions (over-dissipation). Thermal runaway and secondary breakdown possible. h_{FS} increases with temperature.	Over-dissipation failure less likely, except under high voltage conditions. g_{FS} decreases with temperature. Other failure modes: Gate punch through.
Advantages	Wafer processing simpler, making devices less expensive. Low collector-emitter saturation voltage makes low voltage operation feasible.	Input impedance more constant under varying drive levels. Better stability, better high order IMD, easier to broadband. Devices and die can be paralleled with certain precautions. High voltage devices easy to implement.
Disadvantage	Low input impedance with high reactive component. Internal matching required to increase input impedance. Input impedance varies with drive level. Devices or die cannot be easily paralleled.	Larger die required for comparable power level. Non-recoverable gate puncture. High drain-source saturation, which makes low voltage, high power devices less practical.

BJTs in general have higher peak power capability than MOSFETs. MOSFET can be used for pulse power operation, but they have some disadvantages as well as advantages over BJTs. The disadvantages include “pulse drooping,” which means that the trailing end of the pulse has lower amplitude than the leading end. It is caused by the decreasing g_{FS} of a MOSFET with temperature. Corrective circuitry can be used to compensate for this, but this adds to the circuit complexity. The advantages include small phase delays and faster rise and fall times[1].
In conclusion, MOSFET is best suitable for our requirement: stable, wide band, easy to pulse bias gate.

2.4.3 Pulse vs. Continuous Wave (CW)

Transistors made exclusively for pulse operation can produce peak power level of 5 to 6 times compared to their CW rating for a die of a similar size. With standard transistors designed for CW, the multiplying factor is more in the order of 3 to 4 [1].
To realize the high output power in pulse mode, load resistor should be reduced from the figure of continuous rating and input signal should be increased also.

Some devices are not suitable for pulse mode operation. In pulse mode, the device is suffering a series of electric shocks. So it is very important that the device must be chosen carefully.

2.4.4 High frequency device vs. low frequency device

To get good high frequency performance, the physical layout of device should be very thinner. But it will degrade the robustness at lower frequency. The operating band of the device should be close to the band of desired output.

2.4.5 Gate leakage vs. lift time

Igs (gate-source leakage current) is important for MOSFET biasing. It affects the associated device's long term reliability.

The FETs are sensitive to gate rupture. Rupture can be caused by excessive D.C. potential or an instantaneous transient between the gate and the source. This can be compared to exceeding the voltage rating of a capacitor, which usually results in a short or leakage. A power FET can be "restored" in some instances by applying a voltage lower than the rupture level between the gate and the source. It must be at a sufficient current, but not higher than 1 to 1.5 A to clear the gate short. A higher current would fuse one of the bonding wires to the area of the short on the die. A number of cells will always be destroyed, but with large devices, such as 30 W and higher, no difference in performance may be noticed. Long-term reliability after such an operation may be jeopardized and is not recommended in cases where very high reliability is required [1].

2.4.6 High voltage device vs. low voltage device

For pulse modulation, high supply voltage is good for linearity. At the same time, load resistor required by FET will increase, so that the turn ratio of output transformer will be reduced. It means more stability for amplifier and easy to design transformer.

2.4.7 List of final stage device

List of devices for final stage is shown in Table 2.3.

Table 2.3: Device list of final stage

Terms	SR704	SR401	SX60	IXZ210N50L	SD2932	DU28200M	BLF248	RF6V230	BLF278
used by	Arkin	Magritek		3T MRI	Tomc	Minicircuit			
Band used (MHz)	10/20	1/10		2/128	1/30	1/30		10/450	
Power (W)	300	300	400	400	300	200W	300	300	300
Gain (dB)	12	13	16	13	15	13	13	25.5	20
PP/SE?	PP	PP	PP	SE	PP	PP	PP	SE	PP
Vds (V)	28	28	28	150	50	28	28	50	50
Max VSWR	10:1	10:1	10:1		5:1	10:1	50:1	10:1	7:1
Test freq (MHz)	175	175	175	128	175	175	175	220	108
Pd (w)	350	465	515	470	500	389	500		500
max Ids (A)	20	27	30	60	40	20	25		18
Max Vds (V)	70	70	70	500	125	65	65	110	110
max Vgs (V)	20	20	20	20	20	20	20	10	20
Rjc (C/W)	0.5	0.35	0.3	0.32	0.35	0.45	0.45	0.24	0.45
Tj ©	200	200	200	175		200		200	200
Gm (Mho)	4.8	7.2	10	3.8	5	2.5	7.5		6.2
Price (US$)	150	150			151		180		110
Supplyer	Polyfet	Polyfet	Polyfe	IXYSRF	Digi-Key		Digi-Key		Digi-Key
Pakage	AR	AR	C-AR		C-AR	C-AR	C-AR		C-AR
FET type	VDMOS	VDMOS	DMO	MOSFET	N-C MOS	N-C DMOS	CVDM	LDMOS	-CVDMO
Vender	Polyfet	Polyfet	Polyfe	IXYSRF	ST	MA-COM	Philips	Freescale	Philips
Have data at 2MH	No	Yes	No	Yes	Yes	Yes	Yes	No	No
Used in pulse	Yes			Yes, spec	Yes	Yes		Yes	
Free sample?					Yes				
Most wanted									
Terms	SR704	SR401	SX60	IXZ210N50L	SD2932	DU28200M	BLF248	RF6V230	BLF278

As a summary, best device is BLF248. It has high max load VSWR, 50:1, which will give a robust HPA meanwhile its other specification is similar to other devices.

2.4.8 List of devices for drive stage

List of devices for drive stage is in Table 2.4.

Table 2.4: Device list of drive stage

Terms	L88016	BLF245B	BLF245	SGA-7489	BLF145	BLF1043	L8821P
used by	Arkin						
Band used (MHz)	10/20						
Power (W)	30	30	30	0.5	30	10	2
Gain (dB)	14	18	13.5	20	20	18.5	13
PP/SE?	PP	PP	SE	DPP	SE	SE	SE
Vds (V)	28	28	28	8	28	26	12.5
Idq (mA) total	1200	500	50	400	250	85	200
Class	Class A	Class A	Clacc B	Class A	Class AB	ClassAB	Class A
Max VSWR	5:1	50:1	50:1		50:1	10:1	5:1
Test freq (MHz)	500	175	175	1	28	220	108
Duty cycle (5%)	10%	10%	100%	100%	100%	100%	100%
Pd (W)	3.36	1.4	1.4	3.2	7	2.21	2.5
max Pd (w)	80	75	68	470	68	57	30
max Ids (A)	4.5	4.5	6	60	6	2.2	5
Max Vds (V)	70	65	70	500	65	65	36
max Vgs (V)	20	20	20	20	20	15	20
Rjc (C/W)	1.8	2.6	2.9	0.32	2.9	9	5
Tj ©	200	200	200	175	200	200	200
Gm (Mho)	0.8	0.85	1.9	3.8	1.2	0.5	1
Price (US$)	50	50	35	20	50		10
Supplyer	Polyfet	Digi-Key	Digi-Key	IXYSRF	Digi-Key		Polyfet
Pakage	AQ	SOT279A	SOT123A		SOT123A	SOT538A	S08P
FET type	VDMOS	VDMOS	VDMOS	MMIC	CVDMOS	LDMOS	VDMOS
Vender	Polyfet	Philips	Philips		Philips	Philips	Polyfet
Have data at 2MH	No	Yes	Yes	Yes	Yes	No	No
Used in pulse	Yes			No	Yes	No	No
Most wanted		1		2			
Terms	L88016	BLF245B	BLF245	SGA-7489	BLF145	BLF1043	L8821P
PP is Push-pull. SE is single end. DPP is double push-pull.							

As a summary, BLF245B is the best one due to high max load VSWR and lowest DC power consumption. Second one is SGA7489. It is simple, and low cost. L88016 has lowest max load VSWR, 5:1, so that is easy to be damaged.

2.4.9 List of devices for pre-drive stage

List of devices for pre-drive stage is in Table 2.5.

Table 2.5: List of devices for pre-drive stage

Terms	SGA7489	ERA-5SM
used by		
Band used (MHz)		
Po-1 (dBm)	23	17
Gain (dB)	23	20
DC V(V)	8	8
Idq (mA) total	110	65
Class	Class A	Class A
Max VSWR	10:1	
Test freq (MHz)	500	100
Duty cycle (5%)	100%	100%
Pd (W)	0.88	0.52
max Pd (w)	1.2	
max Ids (mA)	170	
Max DC V (V)	10	
Rjc (C/W)	82	133
Tj ©	150	
Price (US$)	5	2
Supplyer	Sirenza	Minicircuit
Pakage		
FET type	SiGe HBT MMIC	MMIC
Vender	Sirenza	Minicircuit
Have data at 2MH	Yes	Yes
Used in pulse	No	No
Most wanted	1	
Terms	SGA7489	ERA-5SM
PP is Push-pull. SE is single end. DPP is double push-pull.		

As a summary, SGA7489 is the best one because of high output power and gain. It will have enough power and gain margin after putting input and output ATT.

2.4.10 Rules for safe operation of FET

For FET safe, following rules are set:

- Don't attempt to measure the Vgs. Permanent gate damage will occur [1].
- Never measure the breakdown voltage (BV_{DSO}) with the gate open, even if it is a definition of BV BV_{DSO} . Permanent gate damage may occur [1].
- Always terminate a gate with a resistor or clamping diode to avoid static damage.
- Always apply the anti-static precaution during assembly and testing of FET
- Anti-static solution: contact all the objects nearby with ground. They include: circuit, instruments, human body (hand and foot), solder iron, table and floor.
- Minimize the test time and number of tests.
- Cover and turn off the rest of the stages while one stage is measured.
- Input and output of each stage should be well terminated.
- Always keep FET in an anti-static bag.

- Always start test FET with lower Vds, low Vgs, low input RF signal, narrow pulse width and less pulse scan.

2.5 RF shield

The complete system should be shielded as well as each stage to avoid any inference from external sources.

2.6 Thermal

Heat-sink plus fan, temperature switch to protect HPA

2.7 Structure

- Double-sided PCB, bottom side is for ground, top side is for traces and components.
- Power devices are mounted on heat-sink directly from the top of the PCB through a window cut on the PCB.
- The bottom of the PCB is also connected with the heat-sink .
- Two fans are attached on the heat-sink to cool the module.
- On top of the PCB, a metal box covers the whole PCB and divides it into several sub boxes for shielding.

2.8 Cost

Material cost is about US$300. Main cost is final stage device. Second is drive stage device. Third is PCB board.

2.9 Design transformer

Transformer is a key component in HPA. The functions are:

- Transform RF signal and power
- Impedance converter
- Converter between balance and single end
- Change phase relationship: in phase, 90 degree or 180 phase
- DC block
- DC power feeding

There are three kinds of transformers: conventional transformer, quarter wave line transformer and transmission line transformer.

A conventional transformer is simple and small in size, but is only suitable for lower frequency. Its max frequency is about 50 MHz.

A quarter wave line transformer is good for high frequency, which can be up to GHz, but the band is narrow.

A transmission line transformer has a wide band and reasonable size. The suitable frequency is from 1 MHz to 1000 MHz. Loss is lower. Frequency response of transmission line transformer is pretty flat.

Our HPA works in 1 to 30 MHz band with high power and small size. The best choice is a transmission line transformer.

Several different transformers will be used in the HPA. They have different power levels and other requirements.

Details of the transformer design are in author's another paper: Design transformer [80].

3 CHAPTER THREE

SIMULATION

3.1 Introduction

Using simulation software is a quick way to calculate the performance of a circuit based on the chosen topology and component values set.

For the RF circuit, high frequency simulation software is required. It is much more complex than general analysis of electronic circuits operating at DC and low frequency.

There are many RF simulation software packages in the market. Some of them are listed below:

- Microwave Office
- Z-land
- Advance Design System (ADS)
- Protel
- Sonnet

Current commercial RF simulation software gives good accuracy for engineering requirements, but there may still be a large error between the simulation results and actual performance.

To analyze small signal circuit and stability, a linear tool is needed. For high power circuit analysis, a non-linear analysis tool is needed, for example harmonic balance method can be used in non-linear analysis. To analyze pulse signal, a time domain analysis tool is needed, for example transient analysis or envelop analysis. To analyze coupling, radiation, interference and shielding, a 2.5D or 3D electromagnetic field tool is needed.

There are several ways to produce the device model. One is from a device vendor. Another is produced and modified by the author, which is a trial and error process. This is due to the model doesn't produce very accurate results.

Simulation software is only a tool. In many situations, the desired results is highly dependant on the knowledge and practical ideas of the designer.

In this thesis, ADS is used. It is produced by Agilent. The usage is permitted by Harris Stratex, who holds the license from Agilent Technologies.

3.2 Pre-drive stage

3.2.1 Introduction

Three functions for pre-drive stage: gain, power, match with source and input of drive stage. MMIC SGA7489 plus input ATT and output ATT is built to make the pre-drive stage. Because it works under CW mode and large signal, harmonic balance simulation tool is used.

3.2.2 SGA7489

First, single end SGA-7489 is simulated. Data of the model of SGA7489 is from datasheet. In/out return loss is from Rin/Rout experienced.
It is shown in Figure 3.1. Input series 10 ohm resistor and output series resistor 5 ohm are for stable operation. It will reduce gain 1 dB and output power 1 dB. Increasing DC block capacitor and Lp of transformer to let cut-off frequency is lower than 1 MHz.

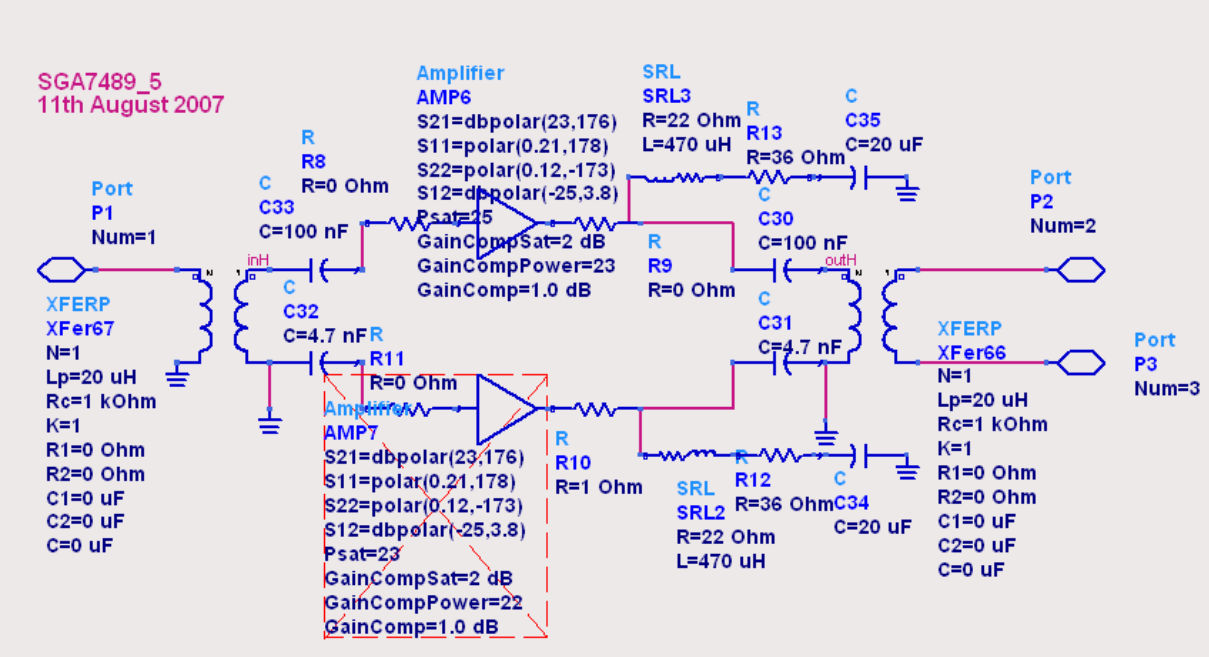
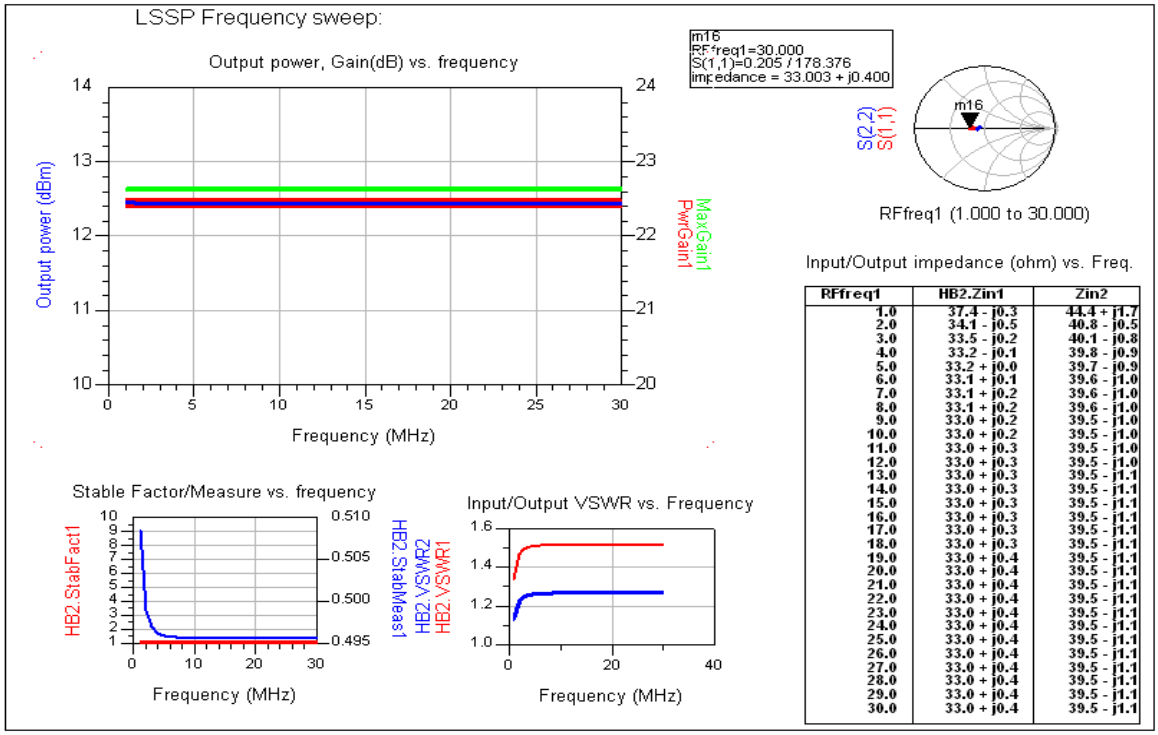


Figure 3.1: Single ended HPA



RFfreq1	HB2.Zin1	Zin2
1.0	37.4 - j0.3	44.4 + j1.7
2.0	34.1 - j0.5	40.8 - j0.5
3.0	33.5 - j0.2	40.1 - j0.8
4.0	33.2 - j0.1	39.8 - j0.9
5.0	33.2 + j0.0	39.7 - j0.9
6.0	33.1 + j0.1	39.6 - j1.0
7.0	33.1 + j0.2	39.6 - j1.0
8.0	33.1 + j0.2	39.6 - j1.0
9.0	33.0 + j0.2	39.5 - j1.0
10.0	33.0 + j0.2	39.5 - j1.0
11.0	33.0 + j0.3	39.5 - j1.0
12.0	33.0 + j0.3	39.5 - j1.0
13.0	33.0 + j0.3	39.5 - j1.1
14.0	33.0 + j0.3	39.5 - j1.1
15.0	33.0 + j0.3	39.5 - j1.1
16.0	33.0 + j0.3	39.5 - j1.1
17.0	33.0 + j0.3	39.5 - j1.1
18.0	33.0 + j0.3	39.5 - j1.1
19.0	33.0 + j0.4	39.5 - j1.1
20.0	33.0 + j0.4	39.5 - j1.1
21.0	33.0 + j0.4	39.5 - j1.1
22.0	33.0 + j0.4	39.5 - j1.1
23.0	33.0 + j0.4	39.5 - j1.1
24.0	33.0 + j0.4	39.5 - j1.1
25.0	33.0 + j0.4	39.5 - j1.1
26.0	33.0 + j0.4	39.5 - j1.1
27.0	33.0 + j0.4	39.5 - j1.1
28.0	33.0 + j0.4	39.5 - j1.1
29.0	33.0 + j0.4	39.5 - j1.1
30.0	33.0 + j0.4	39.5 - j1.1

Figure 3.2: Gain and stability of the system, Pi=-10dBm

Figure 3.2 provides the simulation results. Gain is 22 dB and flat across band of 1 MHz to 30 MHz, which is shown at the left top of the figure. In the top right sub-figure, input (Red color) and output impedance (blue color) are shown in Smith Chart. They are very good due to close to original point. In the bottom middle sub-figure, input VSWR, and output VSWR, are also shown. They are lower than 1.5:1. It is acceptable for a good system. In bottom left part of the figure, stabilty factor, and stable measure, are displayed. Stability factor should be more than 1.0. Current value is more than 1.2. Stable measure should be more than 0. Current value is 0.49. The input impedance is shown at the bottom part of the figure, Zin1, and output impedance, Zin2. They are about 33 and 40 ohm, which are close to 50 ohm. The figures are acceptable. In general it can be concluded that the performance figures are satisfactory.

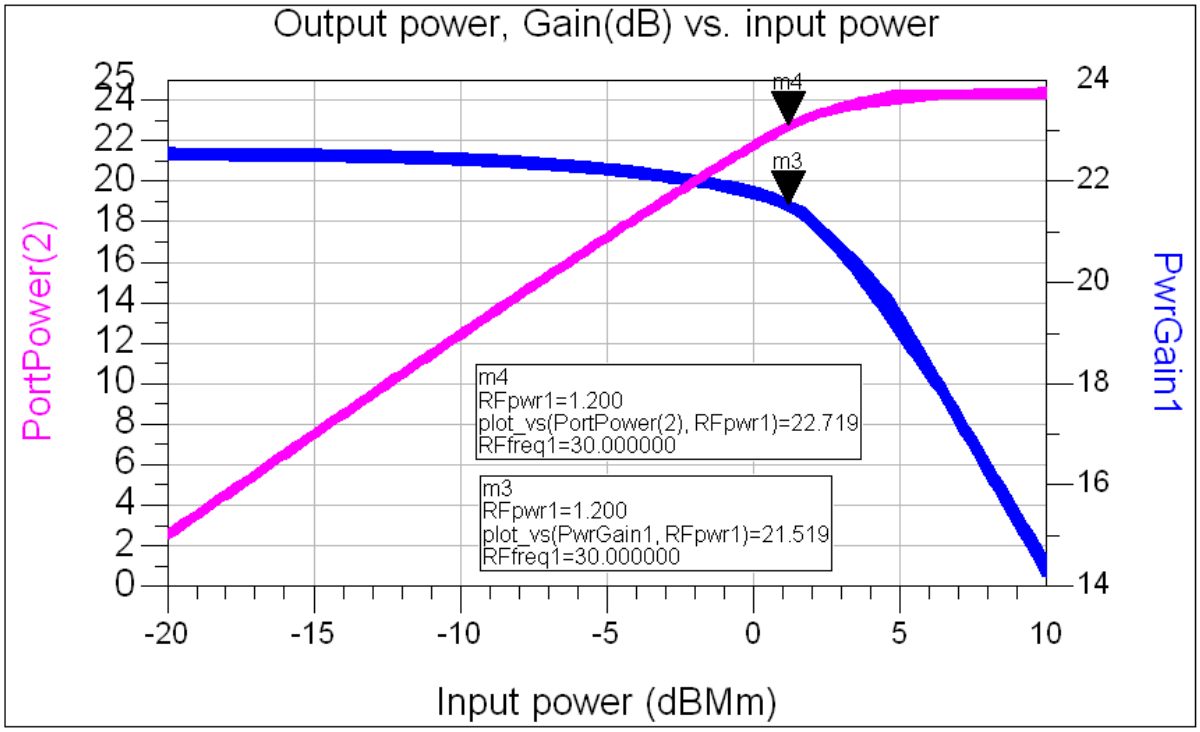


Figure 3.3: Input power sweep, F=1-30MHz

Figure 3.3 shows the linear characteristics of the device under test (DUT). There are two characteristics. The characteristic shown in red is the relationship between input power and output power. It is linear at lower input power. At large input power the output power doesn't follow the linear relationship and attains a constant value at large input power. Po-1 is an important specification for the linearity of DUT. It is an output power point, at which point gain drops 1dB from the gain of lower power. The characteristic shown in blue is the relationship between gain and input power. It is constant while input power is low. At large value of input power it starts dropping. Combination two curves, Po-1 is 22.7dBm. Linear gain is 22.3 dB. G-1 is 21.3 dB. The frequency is swiped from 1 MHz to 30 MHz, and the linear performance is constant across band. 0.3 dB Po and gain drop from specification is due to mismatch of in/output slightly. But overall, linearity is satisfactory.

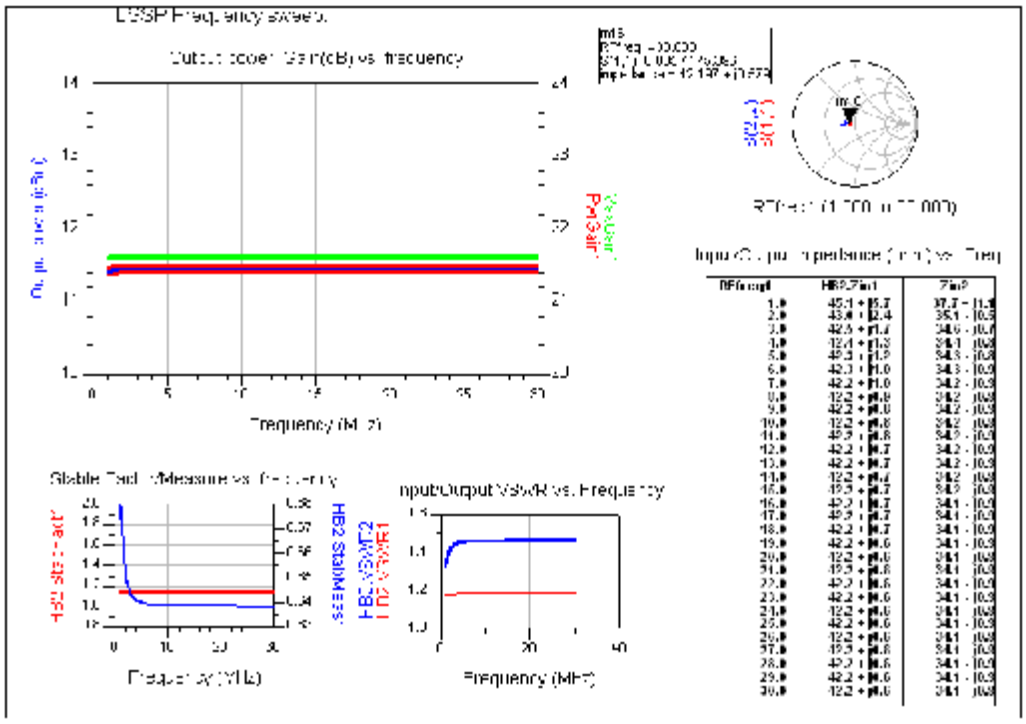


Figure 3.4: Stability factor is 1.15 for R8 =10 ohm

When R8 increases from 0 ohm to 10 ohm, stable factor is changed from 1.05 to 1.15 in cost of 1 dB gain drop. But Po-1, 22.7 dBm is same as before. It is seen that the system has sufficient gain margin and lack of power. This will be good enough to use it in the system.

3.3 Drive stage

3.3.1 Introduction

The purpose of the drive stage is delivering enough power to the last stage. It has enough gain also. It is stable and wide band with good input and output matching.

Key specification:

- 1 to 30 MHz
- >0.5 W or 27 dBm
- Input/output impedance: 50 ohm
- Gain: >15dB
- DC power consumption: <4W
- Spike: <0.3Vpp
- Cost: lower
- Size: small
- There are three options:
- Single end power FET,
- Push-pull power FET and

- Push-pull with MMIC
- For the power FET, the pulse bias has been used to reduce DC power consumption. For the single end power FET, A high spike is produced by the both edge of the gate blanking. It may damage the FET of the last stage. For the push-pull power FET, The amplifier should be tuned on carefully to reduce the spike. The price of the power FET is high also.
- MMIC is cheap and lower DC power consumption. So it can be used in CW mode to avoid the spike issue. To increase its output power, the power combining technique, push-pull, is used.

3.3.2 Push-pull with parallel SGA7489

At first, the push-pull with a single device is tested. The schematic is shown in the Figure 3.5. The gain is 20.4 dB and the Po-1 is 25.8 dBm with good matching.

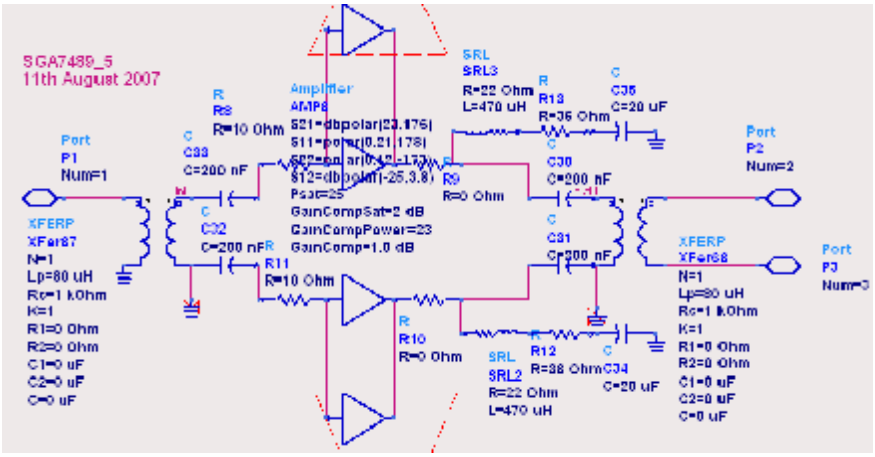


Figure 3.5: Push-pull with a single device

Then the push-pull with parallel devices is used. It is shown in the Figure 3.6.

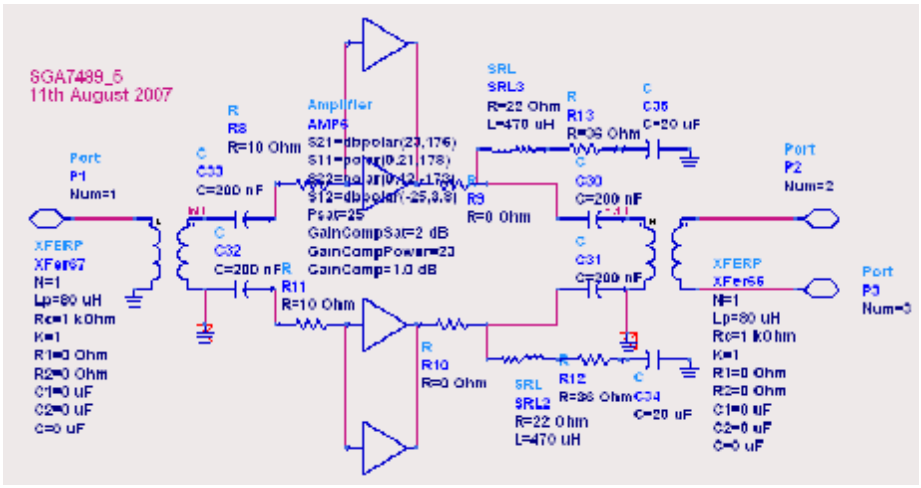


Figure 3.6: Push-pull with parallel configuration

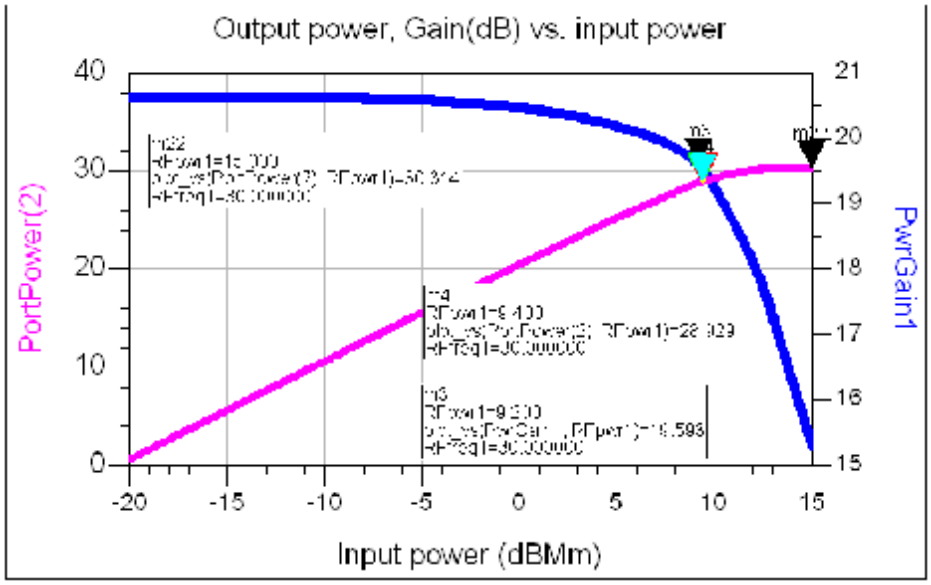


Figure 3.7: Po-1 and Gain, push-pull with parallel, 1-30MHz

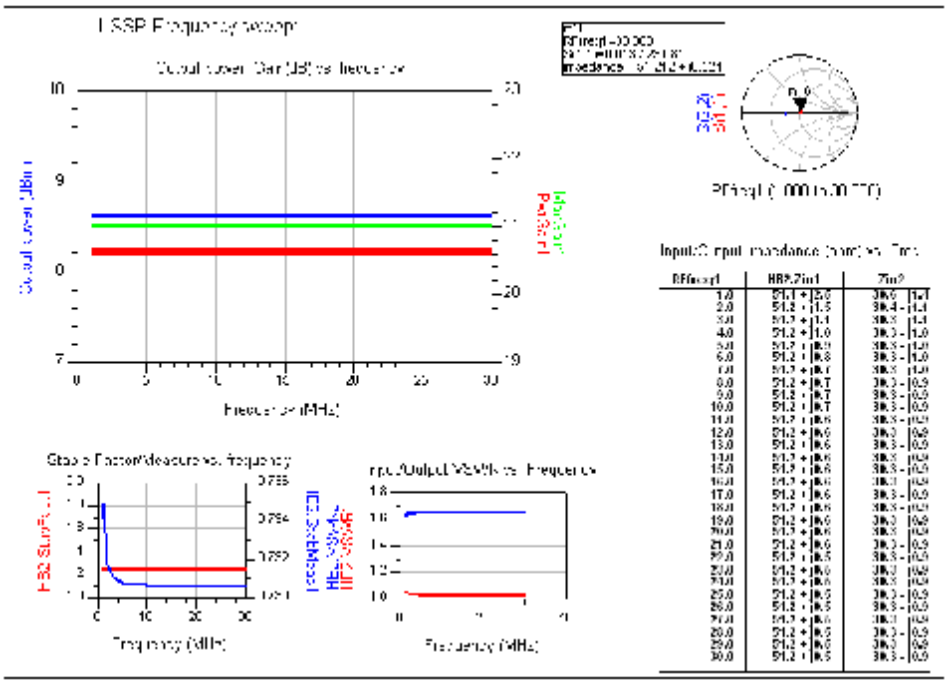


Figure 3.8: Frequency response, push-pull with parallel

The performance are shown in the Figure 3.7 and Figure 3.8. The gain is 20.8 dB and the P-1 is 28.8 dBm. The summary is shown in the Table 3.1.

Table 3.1: Compare single and parallel device in push-pull

	Push-Pull	Push-pull with paralle	Delta
G (dB)	20.4	20.8	0.2
Po-1 (dBm)	25.8	28.8	3
Nin	1	1	
Nout	1	1	
Zin (Ohm)	120	50	
Zout (Ohm)	97	30	
In VSWR	2.4	1.03	
Out VSWR	1.95	1.65	
Stable factor	1.2	1.25	
Stable measure	0.74	0.73	
SGA7489, psat=25dBm, Po-1=23dBm, G=23dB			

Push-pull with parallel works well. Po-1 is 6 dB higher than single device and 3 dB higher than the push-pull with a single device while the gain is the same. The stable status and the match are better than the push-pull with single device.

The minimum inductance of the RF chock is 100 uH for the band of 1 MHz to 30 MHz.

The push-pull with a parallel device meets the requirement.

3.4 Final stage

3.4.1 Introduction

The final stage delivers sufficient RF power to NMR load with efficiency and in a safe way. Its waveform and delay should meet the requirement of the NMR experiment.

The challenges are to achieve stability, robustness, rise time and gain flatness.

The suitable circuit topology and value set will be found after simulation.

The relationship of key performance and component values will be studied.

Following questions will be answered at the end of this section:

- Does it work?
- How to realize it?
- How sensitive?
- Stable?
- Robust?
- What are the simulation result?

3.4.2 Specification

According to the above discussion about the HPA requirements, the following specification is set up to build the final design stage.

- Frequency: 1-30 MHz
- Po-1: >150 W
- Gain: >23 dB
- Gain flatness: <3 dB
- Stable: from DC to 1 GHz
- Input VSWR: <2
- Output VSWR: <3
- Spike: <5 Vpp
- Overshoot: <10%
- Rise time: <3 μs
- Ruggedness with load: load VSWR 20:1 at any angle

3.4.3 Design procedure

Design procedure is as below:

- Output match
- Input match
- Transformer design
- Pulse gate blanking
- Thermal design

3.4.4 New approach

After careful consideration, some new approaches are taken which are described below:

- Push-pull topology
- Separate gate bias for each side FET to get balanced waveform.
- On board potentiometer for fine tuning against output waveform rather than Idq itself.
- Negative feedback to stabilize the DUT
- Higher permeability core for output transformer to improve performance at low end of operation band
- CW drive and pre-drive stage with no spike applied to gate of last stage
- Shield each stage to avoid unwanted feedback
- PRL in gate bias circuit to sharp the shape of gate blanking at gate of FET
- Vgs is between 4-5 V to limit DC power consumption
- RF Vgs<3.5 Vpp to avoid overdriving,

- Max Vgs< 7 V to avoid breakdown the gate insulation
- AM-PM<3 degree to keep Amplifier in Class A

3.4.5 Output match

The main task of power amplifier is delivering as high as possible output power with reasonable gain and reasonable matching. Output power is a function of load line. Load line is a load resistor of power FET at interface of FET drain. The left of the interface is source of FET only. The right of the interface includes the output capacitor, Cds, the inductor of package and load.
At HF and lower VHF band, the relationship of output power and load resistor of amplifier is given by the well know equation

$$R_L = \frac{(V_{ds} - V_{on})^2}{2P_o} \quad \textbf{(3.1)}$$

Where V_{on} = RF saturation voltage

R_o = output power level

V_{ds} = supply voltage

The formula is for single-ended amplifier. For push-pull, this formula gives one side only. It means that the Po is half of total output power; the RL is half of balance load resistor (drain to drain resistor).
On the other hand, while a output transformer is used, the relationship of the primary winding impedance and the outside load of the amplifier are given by the equation

$$R_p = \frac{R_{load}}{(\frac{N_s}{N_p})^2} \quad \textbf{(3.2)}$$

Where R_p = primary resistor of the transformer

R_{load} = load resistor of the transformer

N_s = turns of secondary winding

N_p = turns of primary winding

The goal of output match is to choose suitable Np and Ns to let Rp close to the load line, RL, of desired output power. Output power is here 1dB compression power, Po-1. It means the relationship we wanted is

$$R_p = 2R_L \quad \textbf{(3.3)}$$

The Von is given in the formula below

$$V_{on} = I_{dsq} R_{on} \quad \textbf{(3.4)}$$

Where I_{dsq} = quiescent drain- source current

R_{on} = FET drain- source resistor at on statue

For BLF248, Ron = 0.15 ohm. If Idsq = 13 A, Von = 13 X 0.15 = 2 V

The output power and the load line at different ratio of Ns to Np are given by the table below. If Ns / Np = 3, the load line is 2.8 ohm each side and output power is 170 W. If Ns / Np = 4, the load line is 1.6 ohm each side and output power is 300 W. If Ns / Np = 5, the load line is 1 ohm each side and output is 500 W. But the max output power is 300 W for the FET of BLF248 chosen; the option 3 is not applicable.

Table 3.2: Load line vs. Po-1

Options	Total power		Load line each side						
	Po-1	Po-1	Po-1	RL	Rp	Ns/Np	Rload	Vds	Von
	W	dBm	W	Ohm	Ohm		Ohm	V	V
1	170	52.3	85.0	2.8	2.8	3	50	24	2
2	300	54.8	150.0	1.6	1.6	4	50	24	2
3	500	57.0	250.0	1.0	1.0	5	50	24	2

As a summary, option 1 or option 2 is suitable for the output power requirement (100 W to 200 W). It means that the ratio of Ns to Np of output transformer is 3 or 4.

3.4.6 Input match

The purpose of input match is to reduce reflection power. It means that the input resistor of amplifier should be close to source resistor. In general, the source impedance is 50 ohm. The goal is to let input resistor be 50 ohm. Another purpose of input match is to get flat gain across band.

The input impedance of an RF power FET has significant dependence on the circuit load impedance due to internal feedback capacitance.

A quick look at nearly any MOSFET data sheet will show a huge change in input impedance across the useful frequency range of the device. The power gain of the FET follows a 6 dB per octave slope over the same frequency range.

For a multi-octave design, the solution to both the gain slope and impedance matching problem is an appropriate gate resistor from gate to source. A series capacitor has been used to block DC signal. If the gate resistor is small compared to the magnitude of Zin, power gain is nearly flat and is given by

$$G = g_m{}^2 R_L R_g \left(\frac{1}{1 + R_g / Z_{in}}\right) \quad \textbf{(3.5)}$$

Where g_m = transconductance

R_L = Load impedance (load line)

R_g = gate resistance

Z_{in} = Input impedance of FET

Once R_g is made, turn ratio of input transformer is chosen to converter it to 50 ohm.

If using negative feedback, the input impedance is reduced. Turn ratio of input transformer will be different.

3.4.7 Design and simulation

3.4.7.1 Initial circuit and simulation

The initial circuit is shown in Figure 3.9. It is a push-pull structure. Philips VDMOSFET, BLF248, is used. Its max RF output power is 300 W. Power supply voltage is 28 V. It can be used in our 24 V power supply in cost of reduced RF output power. As an advantage, the can withstand max load VSWR 50:1, which is best specification in the market.

The output transformer is a transmission line transformer with DC block function between primary and secondary winding. The central tap of primary winding is used as a DC drain power supply. The flex produced from the top half of the winding and from the bottom half of the winding are canceled each other due to out of phase. It reduces the risk of saturation the core. It lets the output circuit simple and small size also. The turn ratio of Ns /Np of output transformer is 4:1. The turn of primary winding is 1 turn and the turn of secondary of winding is 4. It gives an expected output power and good output match.

The R78 / R94 are ESD protection resistor. It supplies a DC path from the gate to the ground to avoid any high voltage at the gate of the FET. At same time, it doesn't affect other performance of the circuit due to its high resistance.

The R54 / R45 / R58 and R95 / R93 / R57 are used to stable the DUT by reducing gain of the DUT.

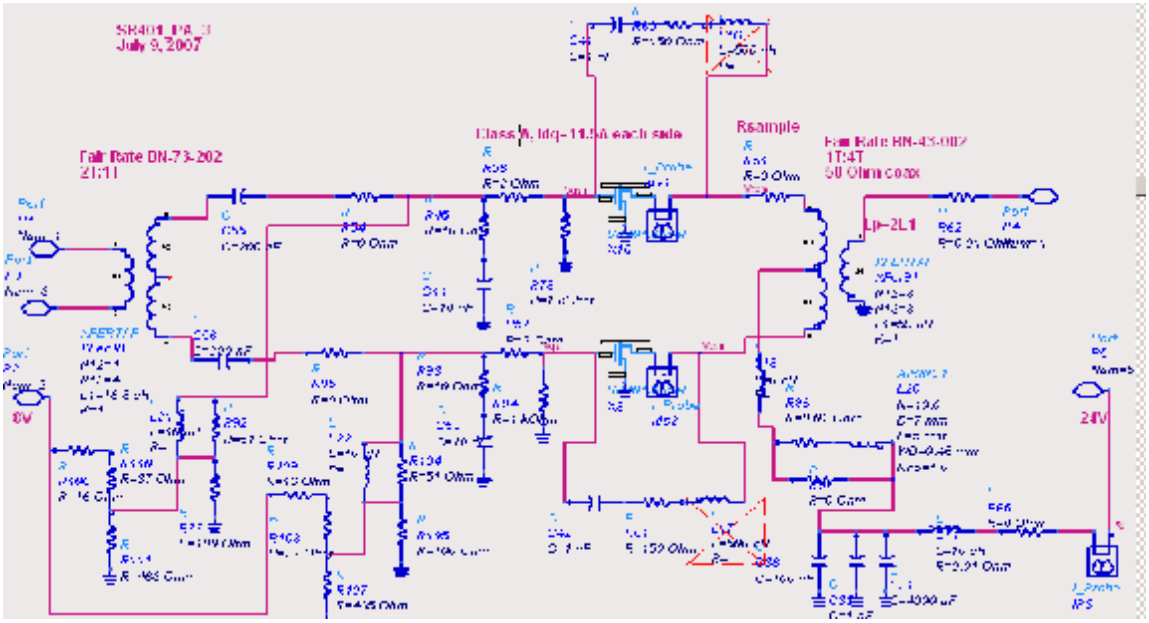


Figure 3.9: The initial DUT of last stage

The input impedance of the DUT is reduced by the branch of R45 plus C44 and R93 plus C53. In the operating band, the impedance of the capacitors is neglected comparing with the resistors, R45 / R93. The input impedance of DUT is dominated by R45 / R93 if they are very small comparing with the impedance of input of FET.

The C55 / C56 are the DC block capacitors in RF input path. It lets the gates of FET can be adjusted separately.

The input transformer is used to converter the input impedance of the DUT to a 50 ohm. A traditional transformer can be used. It has a DC block function. It has single end to balance or balance to balance converter function. Same as the output transformer, the two end of secondary winding is out of phase. It meets the requirement of push-pull circuit.

The rest of components in the input of DUT are for the gate bias. The gate bias is pulse gate bias rather than DC gate bias. There are three functions for the gate pulse bias. First is to apply the gate blanking voltage. Second is to avoid RF leakage from it. Third is to keep an ideal square shape gate planking waveform. Fourth is not to affect other RF performance.

The LC circuit connected with the central tap of the primary winding of the output transformer is for storing the energy for the large current during the pulse duration. It is also to decouple the RF signal from the DUT to avoid affecting the other circuits.

The negative feedback under the pulse bias condition is not recommended by some FET venders. They believe that it may cause a funny behave or the risk of the DUT unstable due to the time delay of the negative feedback. So it is not used at this moment.

The setting for the simulation is shown in Figure 3.10. The Module Under Test (MUT) is the final stage, which is shown in Figure 3.9. Two kind of simulation are used here: Large Signal S-parameter (LSSP) simulation for frequency domain performance; Envelope simulation for time domain performance under the AM modulation: pulse mode. Matching with the simulation tools, there are two kinds of RF signal sources and two kinds of gate bias source: the pulse sources and Continue Waveform (CW) sources. The pulse sources are for the Envelope simulation. The CW sources are for the LSSP simulation. There are two sets of Double Directional Coupler (DDC), one is at the input of the MUT, which is for testing the input VSWR and the input power; another is at the output of the MUT, which is for testing the output VSWR and the output power of the MUT. The ATTEN 1 / ATTEN 2 are the attenuators inserted between the load / the source and the MUT as a buffer to improve the matching. The icons on the left hand of the figure are for the performance of the MUT we want to know. For the example, the VSWR1 is for the input VSWR; VSWR2 is for the output VSWR; StableFact1 is for the stable factor of the MUT and so on. The current status shown in the figure is for the Envelop simulation.

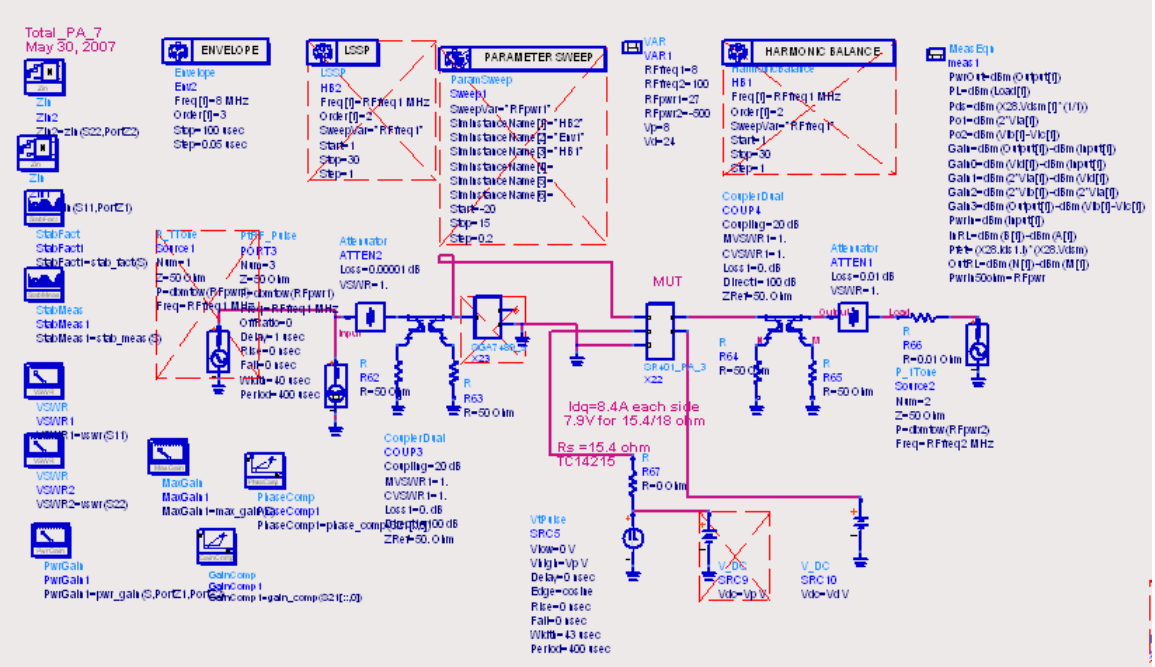


Figure 3.10: Simulation setting

Whatever the LSSP or the Envelope simulation, they both use the SPICE model of the FET. The reason is that both the simulations above are non-linear simulation, which needs a model of non-linear like the SPICE model. The SPICE model gives all non-linear information, say, Po-1, AM-PM, AM-AM, Idq, waveform, overdrive, spike and rise time at different power supply, gate voltage, input power.

There are several models for designing an amplifier: S-parameter, SPICE, Input / output impedance and pull-out data.

Why is the SPICE model needed? There are two reasons. One is linear and non-linear issue. The S-parameter model only gives a linear performance at low signal level. The DUT works under the condition in which the DUT is close to saturation. It is a non-linear condition so a non-linear model is needed. Another reason is the operating condition issue. The operating condition (say, the bias, the power supply voltage and the signal power level) of our case is big different from the condition given at the datasheet of the vender. The data of the vender may be useless in my case. For example, the condition of the datasheet recommended is: Idq = 0.25 A, Vds = 28 V and Po = 300 W; but the condition of my case is: Idq = 13A, Vds = 24 V and Po = 150 W. The input / output impedance and pull-out data are given at a special operating condition which is chosen by the vender rather than the users. On the other hand, the SPICE model lets us changing the bias condition and signal power level at any time with any way to meet my special requirements. As a summary, the SPICE model is best suitable for us.

There are two kinds of simulation results. One is time domain performance, which is from the envelope simulation. The typical figure is as Figure 3.11. Another is frequency domain performance, which is from the LSSP simulation. The typical figure is as Figure 3.13.

We will take some time to describe the meaning of the each sub-figure in the Figure 3.11 because it will be used often.

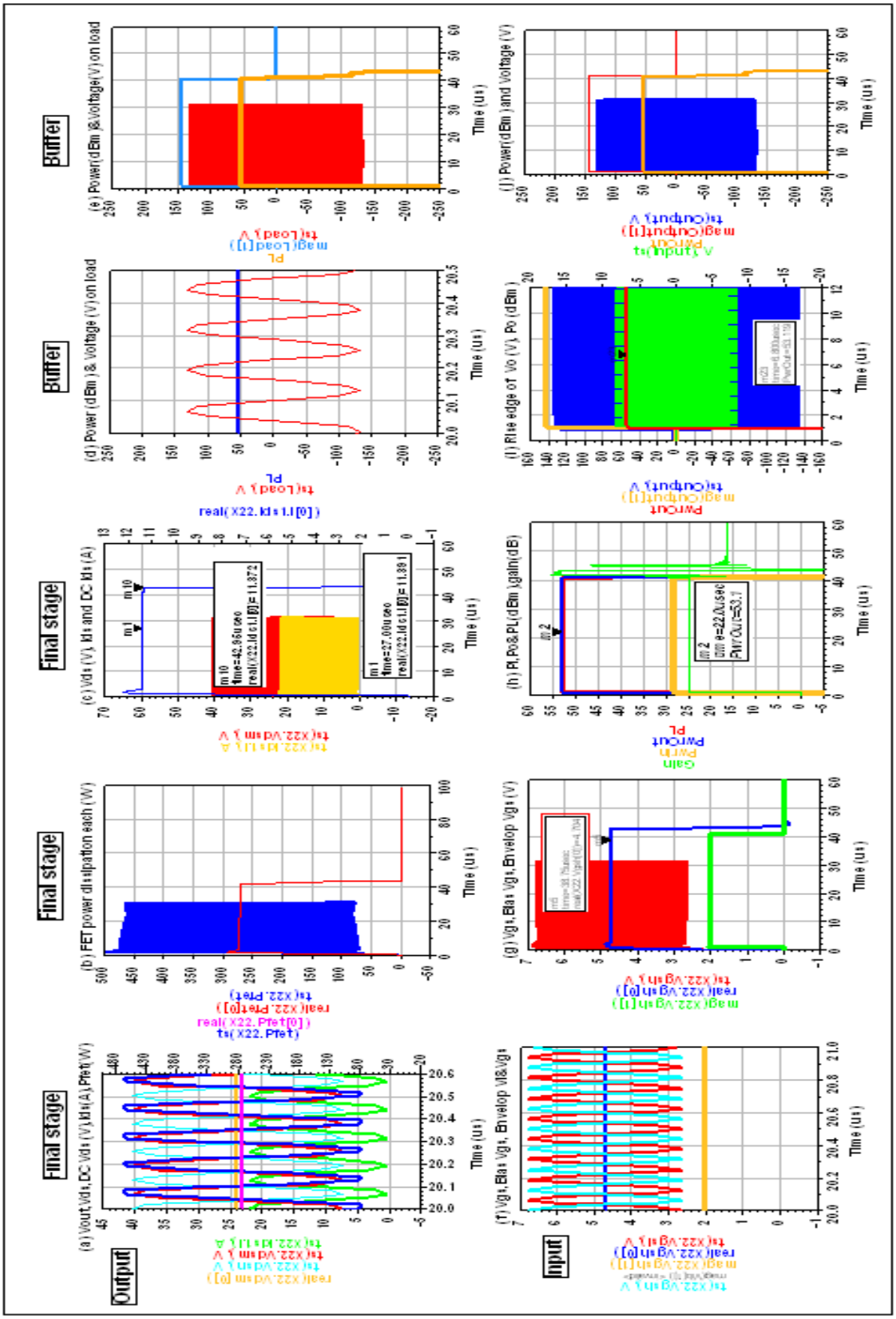


Figure 3.11: Pulse result of the initial DUT, 8MHz, Pi=27dBm

The time domain performance, say, RF waveform, pulse envelope, gate bias voltage, drain quiescent current, rise time and output power, are displayed in the Figure 3.11. It is for a frequency and a RF power level once a time. There are 10 sub-figures in it. They are marked with a) to g). Generally, top row is for the data of the output of the sub-part of the DUT; the bottom row is for the data of the input of the sub-part of the DUT. The columns of the sub-figures counted from left to right are response to the test points of the DUT counted from the input to the output. A lot of information is displayed but the place is limited. As the results, they are squeezed an figure with the A4 size, in which there are many sub-figures. The sub-figures are explained one by one in below.

a) This sub-figure has focussed on displaying the power consumption of the FET each side of the DUT. It is a function of the time. Like other sub-figures in this figure, the X axle is time with us unit. The power consumption of the FET of the high side, Pfet, is the curve with blue color and the unit of W. Its Y axle is on the right hand side. Because Pfet = Ids*Vds, Ids and Vds are displayed also. The drain-source current of high side of FET, Ids, is the curve with the green color and the unit of A. Its Y axle is on the left hand side. The drain-source voltage of the FET of high side, Vdsm, is the curve with the red color and the unit of V. Its Y axle is on the left hand side. As a reference, the drain-source voltage of the FET of the low side FET, Vdsn, is displayed also. It is the curve with the light blue color and the unit of V. Its Y axle is on the left hand side. From the figure, Vdsm is out of phase with Vdsn. Vdsm is out of phase with Ids. Pfet is in phase with Vdsm. The average Vdsm (DC Vdsm), DC Vds, and average Pfet (DC Pfet), real Pfet [0], are displayed also. The DC Vds is the curve with brown color and the unit of V at left hand side of the Y axle. The real Pfet [0] is the curve with the color of pink and the unit of W at the right hand of the Y axle. For quick checking, they are in the Table 3.3.

Table 3.3: The meaning of the sub-figure a)

Name	Symble	Unit	Color	Y axle
High side FET power consumption	Pfet	W	Blue	Right
High side drain-source voltage	Vdsm	V	Red	Left
High side drain-source current	Ids	A	Green	Left
Low side drain-source voltage	Vdsn	V	Light blue	Left
High side DC drain-source voltage	DC Vds	V	Brown	Left
High side DC FET power consumpotion	Real Pfet [0]	W	Pink	Right
Notice: This figure is for FET power consumtion of the detail of the RF waveform. All X axis is time domain with the unit of micro-second. Pfet = Vds*Ids				

b) It focuses on the FET power consumption of the outline. See Table 3.4.

Table 3.4: The meaning of the sub-figure b)

Name	Symble	Unit	Color	Y axle
High side FET power consumption	Pfet	W	Blue	Left
High side DC FET power consumpotion	Real Pfet [0]	W	Red	Left
Notice: This figure is for FET power consumtion of outline. All X axis is time domain with the unit of micro-second.				

c) It focuses on the FET power consumption of the outline. See Table 3.5. What is the

different between the average Ids and the quiescent drain-source current (Idq)? The former is the drain-source current during the RF signal. The later is the drain-source current during pulse gate blanking but without the RF signal. They may be different. So far we are talking about the current which is in the pulse gate blanking. If counting the whole period of the pulse blanking, The average (DC) current is different from the one above.

Table 3.5: The meaning of the sub-figure c)

Name	Symble	Unit	Color	Y axle
High side FET power consumption	Pfet	W	Blue	Left
High side DC FET power consumpotion	Real Pfet [0]	W	Red	Left
Notice: This figure is for FET power consumtion of outline. All X axle is time domain with the unit of us.				

d) It focuses on average and the voltage and power on the load in the detail of the RF waveform. See Table 3.4.

Table 3.6: The meaning of the sub-figure d)

Name	Symble	Unit	Color	Y axle
RF power on the load	PL	dBm	Blue	Left
RF voltage on the load	Load	V	Red	Left
Notice: This figure is for RF power and voltage on the load with the detail of RF waveform. All X axle is time domain with the unit of us.				

e) It focuses on the RF power and the RF voltage on the load with the outline. See Table 3.7.

Table 3.7: The meaning of the sub-figure e)

Name	Symble	Unit	Color	Y axle
RF power on the load	PL	dBm	Brown	Left
RF voltage and power on the load	Load	V	Red	Left
Magnitude of the fondamental RF power	mag PL[1]	V	Blue	Left
Notice: This figure is for the RF power and voltage on the load with outline. All X axle is time domain with the unit of us.				

f) See Table 3.8.

Table 3.8: The meaning of the sub-figure f)

Name	Symble	Unit	Color	Y axle
High side FET gate voltage	Vgsh	V	Light blue	Left
Low side FET gate voltage	Vgsl	V	Red	Left
High side DC FET gate voltage	Real Vgsh[0]	V	Blue	Left
High side FET fondamental gate voltage	mag Vdsh[1]	V	Brown	Left
Notice: This figure is the gate voltage of the FET with the detail of the RF waveform.				

g) See Table 3.9.

Table 3.9: The meaning of the sub-figure g)

Name	Symble	Unit	Color	Y axle
High side FET gate voltage	Vgsh	V	Red	Left
High side DC FET gate voltage	Real Vgsh[0]	V	Blue	Left
High side FET fondamental gate voltage	mag Vdsh[1]	V	Green	Left
Notice: This figure is the gate voltage of the FET with the outline. All X axle is time domain with the unit of us.				

h) See Table 3.10.

Table 3.10: The meaning of the sub-figure h)

Name	Symble	Unit	Color	Y axle
Gain of DUT	Gain	dB	Green	Left
Input power	Pin	dBm	Brown	Left
Output power of DUT	Pout	dBm	Blue	Left
Power on the load	PL	dBm	Red	Left
Notice: This figure is for the output power and gain with the outline. All X axle is time domain with the unit of us. An ATT, buffer, is inserted abetween the output of the DUT and the load. Pout is before the ATT and PL is after the ATT.				

i) See Table 3.11.

Table 3.11: The meaning of the sub-figure i)

Name	Symble	Unit	Color	Y axle
Output RF power	Pout	dBm	Red	Left
Output fondamental voltage	mag Output[1]	V	Brown	Left
Output RF voltage	Output	V	Blue	Left
Input voltage	Input	V	Green	Right
Notice: This figure is for the rise time of output voltage with outline. All X axle is time domain with the unit of us.				

j) See Table 3.12.

Table 3.12: The meaning of the sub-figure j)

Name	Symble	Unit	Color	Y axle
Output power	Poutput	dBm	Brown	Left
Envelop of the fundamental output voltage	mag Output[1]	V	Red	Left
Output voltage	Output	V	Blue	Left
Notice: This figure is for the output power and voltage with the outline. All X axle is time domain with the unit of us.				

The sub-figure (j) is checked against the sub-figure (e) to find the ATT's contribution.

As a summary, this figure of the pulse results includes a lot of information of DUT at time domain.

The Figure 3.11 above is under the condition of 8 MHz and Pi = 27 dBm. The Figure 3.12 below is under the condition of 8 MHz and Pi = 29 dBm. Output power increases from

53.1 dBm to 53.9 dBm while the input power increases from 27 dBm to 29 dBm. It shows that the DUT starts saturation. The output power 53 dBm (200W) is close to its max power. Rise time is less than 1us, it is good. DC gate voltage is about 4.9 V. The quiescent drain-source current is about 11.5 A each side of FET. The output RF voltage waveform is sinusoid at 200 W output: good. The output power is same as the power on the load because of no output buffer, ATT. The pulse results of the DUT is good.

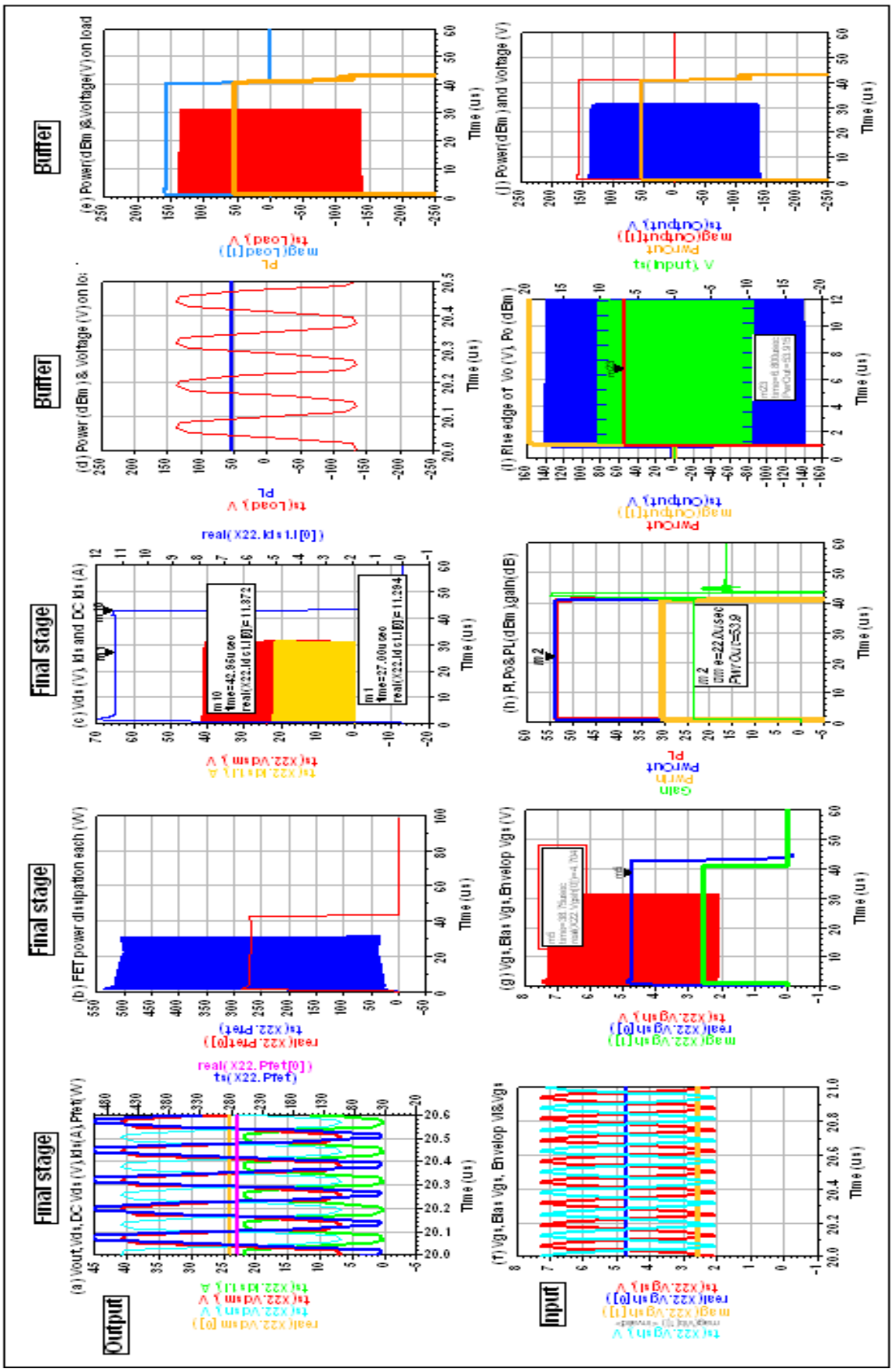


Figure 3.12: Pulse result of the initial DUT, 8MHz, 29dBm

The frequency domain performances are shown in Figure 3.13. The meaning of each sub-figure is same as the Figure 3.2. The detail description of its meaning is near by Figure 3.2. They are summarized in Table 3.13.

Table 3.13: The summary of the meaning of the frequency domain figure

Name	Symbol	Unit	Color	Sub-fugure	Y axle	Spec	Test
Gain	PwrGain1	dB	Red	Left top	Right	23-28	25
Gain flatness	PwrGain2	dB	Red	Left top	Right	<2	2
Output power	Output power	dBm	Blue	Left top	Left	>52	52
Input reflection coifficent	S(1,1)	Scale	Red	Right top		<0.3	0.25
Output reflection coifficent	S(2,2)	Scale	Blue	Right top		<0.3	0.9
Stable Factor	StableFactor1	Red	L	Left bottom	Left	>1	0.75
Stable Measure	StableMeas1	Blue	Red	Left bottom	Right	>0	0.15
Input VSWR	VSWR1	Red	Left	Middle bottom	Left	<3	4
Output VSWR	VSWR2	Blue	Left	Middle bottom	Left	<2	30
Input impedance	Zin1	Black		Right bottom		40-60	93
Output impedance	Zin2	Black		Right bottom		30-80	1285
Notice: It is focus on the frequency domain performance. All X axle are frequency with the unit of MHz.							

Let us analysis the performance of the DUT from the four figures above. From Figure 3.11 and Figure 3.12, it can be seen that pulse performance is good. Max output power is about 53.8 dBm with the turn ratio of 1:4 of the output transformer. The output power is close to the data from the formula (2). Optimum Idq is 11.5 A. As a reference, Idq is 8 A with the turn ratio of 1:3 of the output transformer. It is means that for the higher power, not only the turn ratio needs to be increased but also the Idq needs to be increased. The rise time is ideal. However, from the Figure 3.13 and Figure 3.14, there is 4 dB gain slope across the band and output impedance is a function of input power. This means output VSWR is poor at lower signal and low frequency. It will increase the risk of the oscillation. Furthermore, the DUT is unstable from 8 MHz to 24 MHz due to The Stable Factor is less than 1.

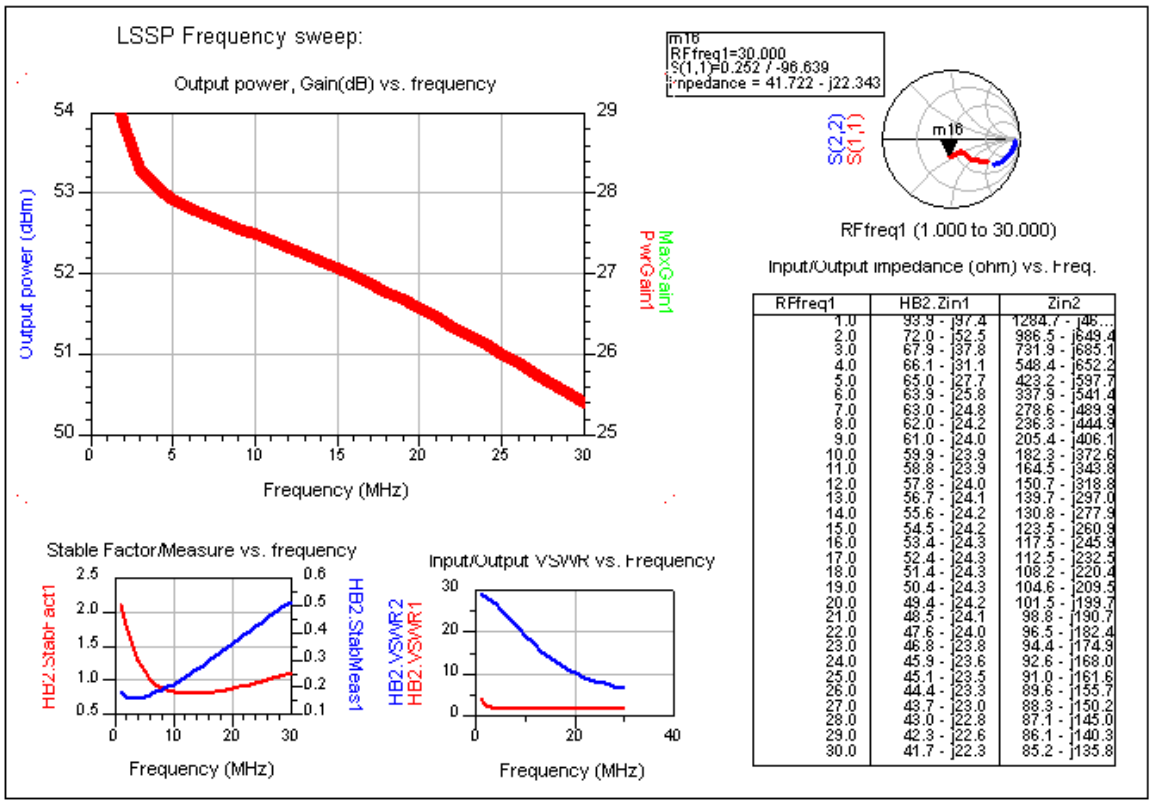


Figure 3.13: Gain and stable, initial DUT, P1=10 dBm

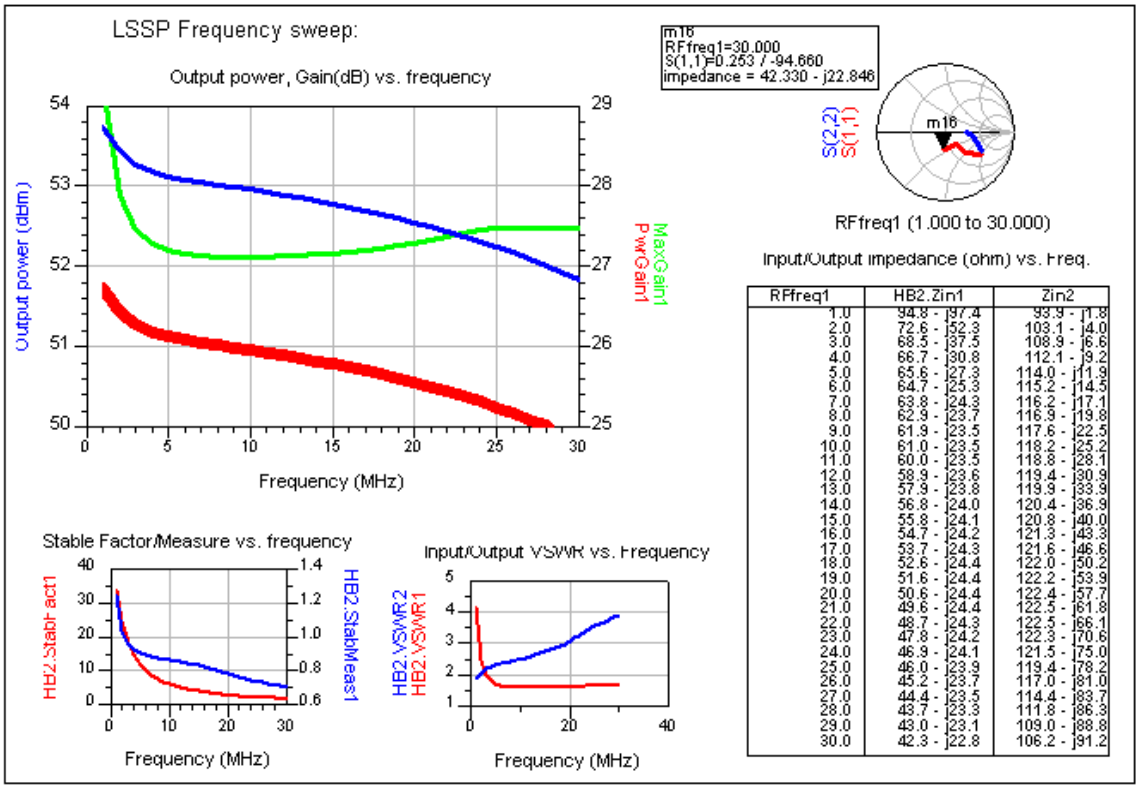


Figure 3.14: Gain and stable, initial DUT, Pi=27 dBm

As a summary, the initial DUT is not satisfied.

3.4.7.2 DUT with negative feedback

The issues of the initial DUT is:

Unstable in the operating band

Output impedance is a function of the input power

Gain slope

High output VSWR

To overcome the short points of the initial DUT, the negative feedback is introduced by using the feedback branch between the gate and the drain of the FET in the Figure 3.9.

Figure 3.15 and Figure 3.16 show that output impedance is a constant and gain response is flat with feedback across 3 to 30 MHz. However, when frequency is under 3 MHz, gain is increased and the DUT is under risk of becoming unstable. The negative feedback is improved the performance in band but it can't improve the stable at low frequency due to the limit of DC block capacitor of the feedback branch.

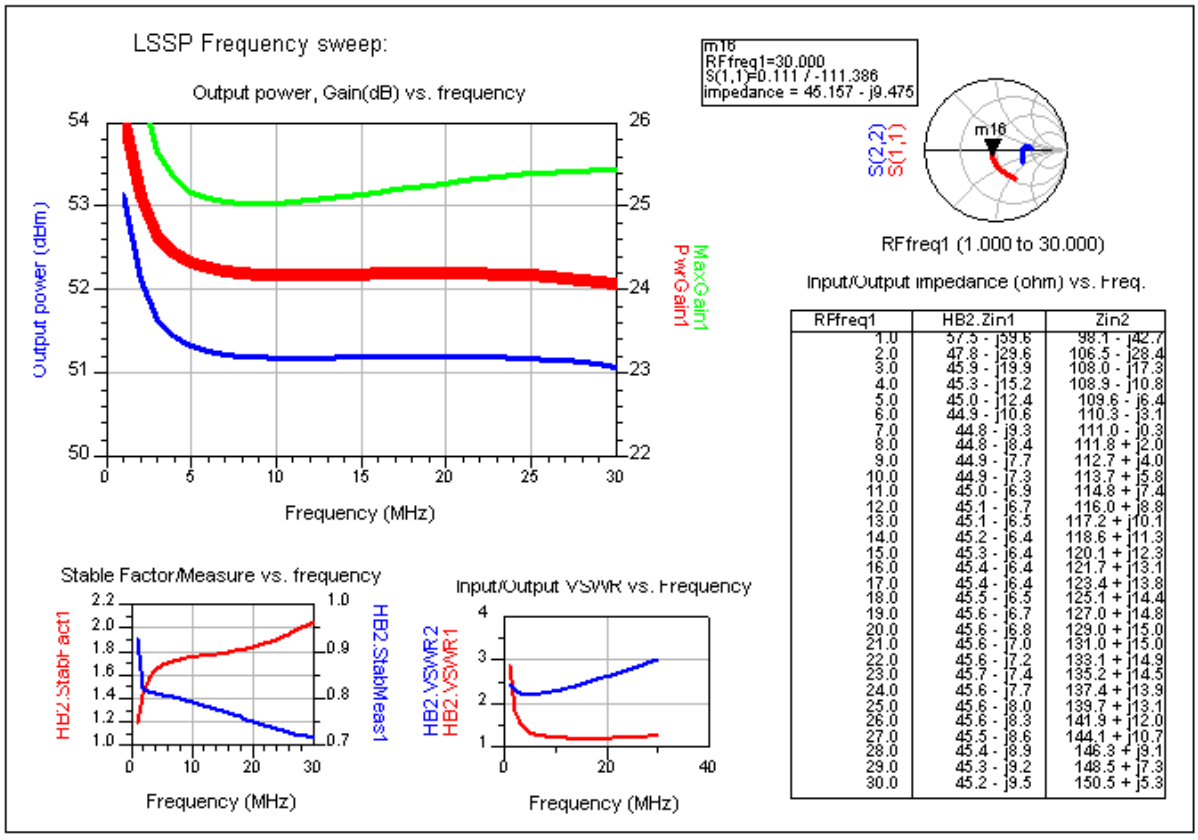


Figure 3.15: Gain and stable, feedback, Pi=27 dBm

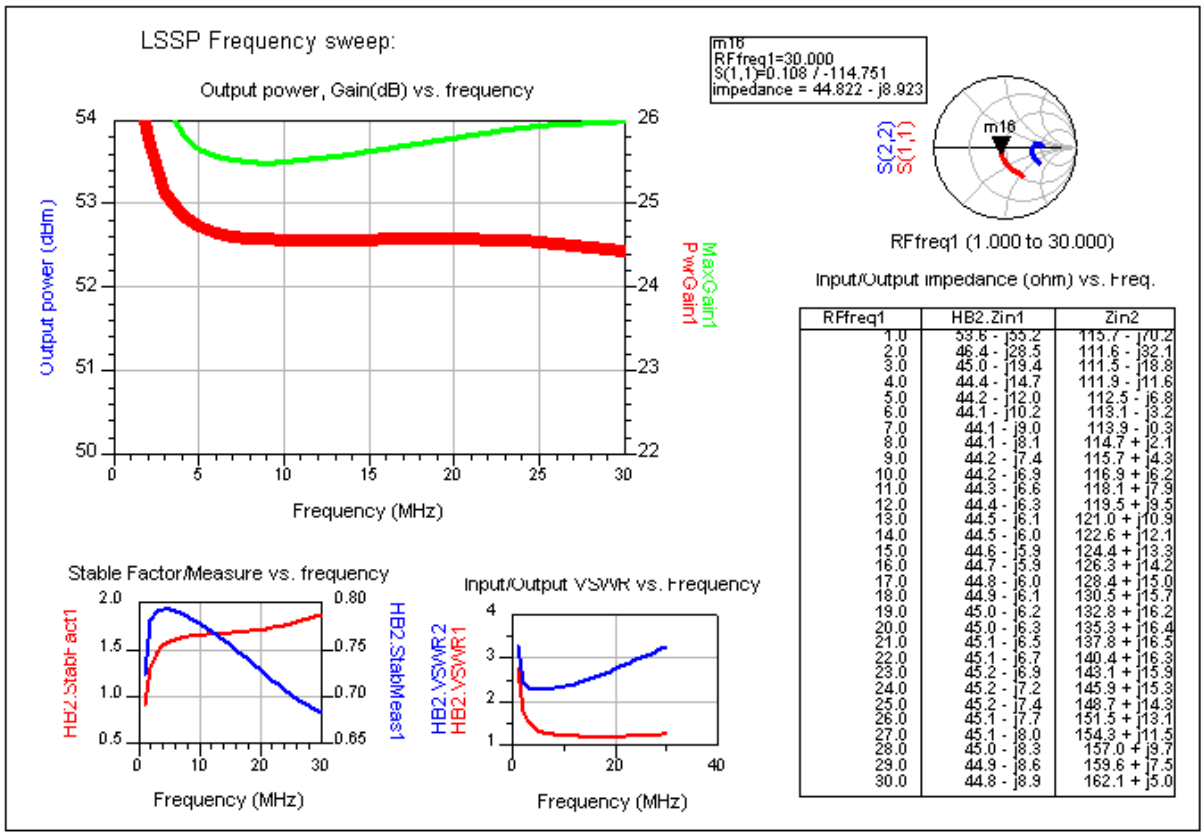


Figure 3.16: Gain and stable, feedback, Pi=10 dBm

We will try to improve the performance further here. Output impedance is improved if a 20 ohm resistor is inserted between drain of the FET. It drops output power only 10% due to 3 ohm load line. Gain drops 1 dB also. To reduce gain of low frequency and improve stability, The DC block capacitors of the feedback branch between the gate and the drain of the FET, C41/C42, is increased to 100 nF, the DC block capacitor of the gate SRC branch, C44/C53, is increased to 22 nF and the input DC block capacitors, C55/C56, is increased to 2000 nF. They are shown in the schematic of the Figure 3.17.

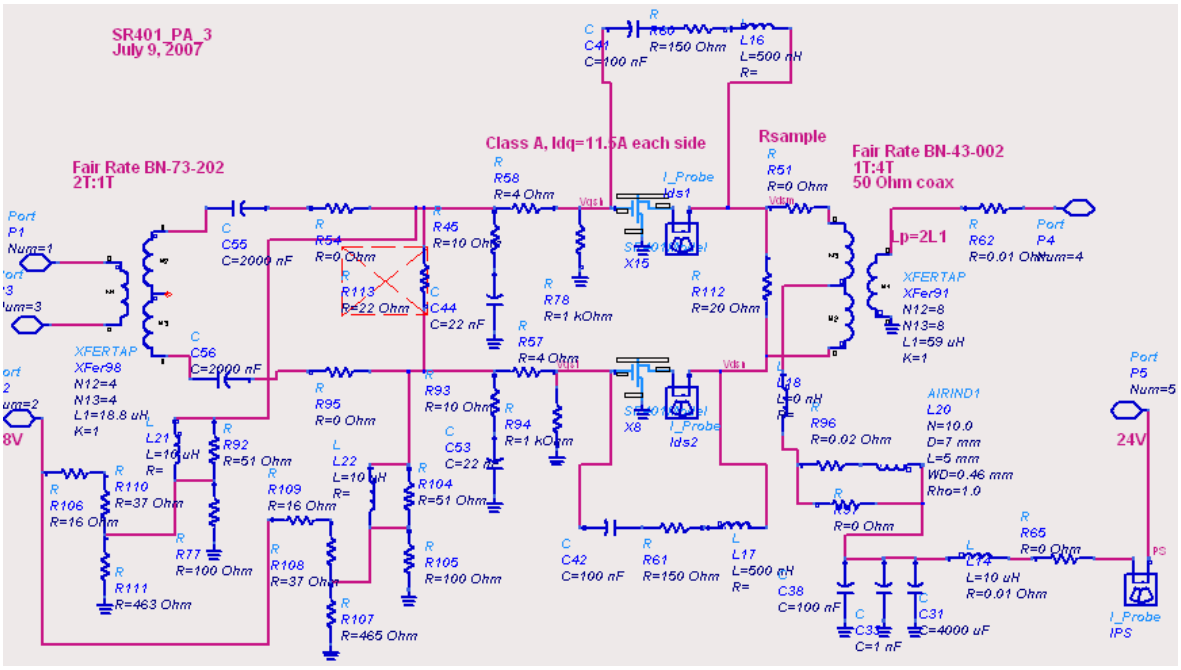


Figure 3.17: Modified DUT for CW gain and stable

The frequency domain performance with the schematic of the Figure 3.17 is shown in the Figure 3.18. It has a good performance in the operating band but it still has a risk of oscillation while the frequency is lower than 1 MHz.

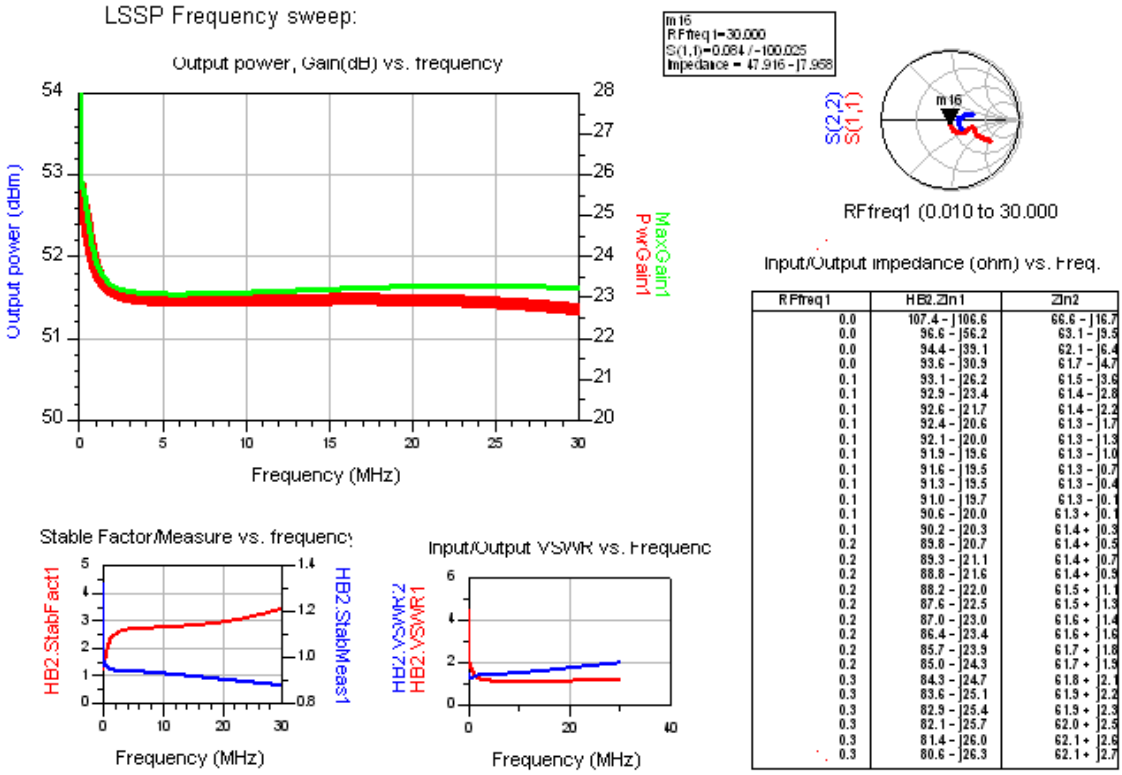


Figure 3.18: Gain and stable, Pi=10dBm

Pulse performance of the DUT setting of the Figure 3.17 is shown in the Figure 3.19. The envelopes of the Idq and Vgs are distorted. The rise time is increased and the output power is reduced. The time domain performance is not satisfied.

Summary:

The DUT with the negative feedback has a good performance in the operating band.

The stable of the DUT at very low frequency is still a issue.

The negative feedback degrades the time domain performance.

Under the condition of the negative feedback, how to improve the pulse performance and the stable of lower frequency is a challenge.

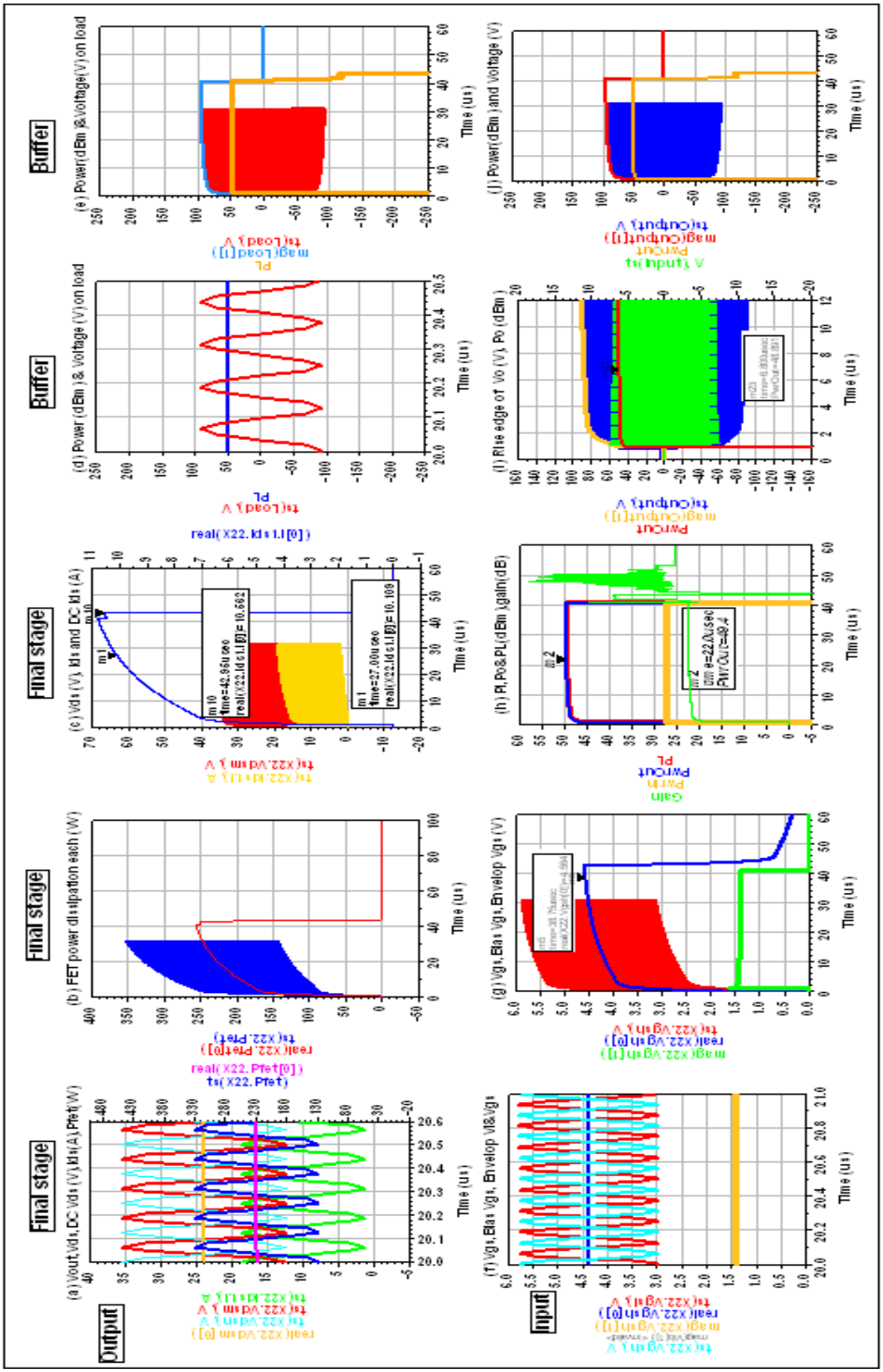


Figure 3.19: Pulse result, 8MHz, Pi=27 dBm

3.4.7.3 DUT with hard bias and negative feedback

So far there is a conflict between using the negative feedback or not. There is good output VSWR, constant output impedance whatever signal level, stable in band and gain flatness for feedback, but it degrades the rise time and the gain (drop 2 dB). There is good rise time and high gain without feedback, but it degrades the gain slope, the stable and the output VSWR. Output impedance is changed while input power is changed without feedback, which may cause instability due to poor output VSWR at weak signal (high output impedance).

Why does the negative feedback degrade the rise time? As we know, the voltage across the capacitor can't be changed suddenly. The drain voltage drops suddenly when the gate voltage rises suddenly. Through the feedback branch, the gate voltage will drop. This process reduces the DUT time response speed. So the rise time of the output voltage increases. The higher the DC block's capacitance, the greater the rise time. For low frequency stability and the gain flatness, the higher capacitance is needed.

Why can the negative feedback reduce the change of output impedance with the RF signal level? The output impedance is the ratio of the delta Vds to the delta Ids. This negative feedback samples the drain voltage so it reduces the delta Vds. Hence, the output impedance will be reduced.

How does the input impedance of the DUT change? At low HF band (<10 MHz), the input impedance of the FET is neglected comparing the Series Resistor and Capacitor (SRC) between the gate and the ground, which is the R45 and the C44 in the Figure 3.17. This SRC dominates the input impedance. If the capacitance is 10 nF and the resistance is 10 ohm, the impedance of the capacitor increases quickly while the frequency reduces. So the SRC impedance is higher and is dominated by the capacitor at low frequency. This is shown in the Table 3.14. This may cause instability of the DUT. It is ideal to have constant low impedance, say 10 ohm.

Table 3.14: Impedance of SRC

Freq. (MHz)	C (nF)	Zc (ohm)	R (ohm)	Total Z (ohm)
0.01	10	1592	10	1602
0.1	10	159	10	169
1	10	16	10	26
10	10	2	10	12
100	10	0	11	11

Why does the output impedance increase while the frequency reduces? There two reasons. One is Cds. Its impedance increases while the frequency reduces. Another is input SRC impedance, which increases while the frequency reduces. So the output impedance increases. Considering the gain of the FET increases while frequency reduces, both factors give more risk for DUT instability.

The way to use the negative feedback with a less ability of controlling the gate and to have a constant 10 ohm resistor at the gate is the direction to solve this issue.

A solution called the hard bias with the negative feedback is introduced below.

The circuit of the hard bias is putting a lower resistance resistor between the gate and the drain of the FET. It is shown in Figure 3.20 as the R45/R93. It is 10 ohm there. It gives a lower resistor across the wide band. The frequency can be down to DC. It has two advantages. One is stable of the DUT by supplying lower impedance at gate at very lower frequency. At such lower frequency, the negative feedback doesn't work due to the limit of its DC block capacitor. Another is to reduce the controlling ability of the negative feedback in the operating band. In this way, rise time may be improved.

The hard bias circuit also includes the circuits for the pulse banking bias pulse. It is L21 / L22, R92 / R104, R77 / R107 and R106 / R108. They will give a adjustable sharp square pulse with low source impedance.

The hard bias circuit needs a high DC bias current due to the DC path to ground. The bias current will be 0.5 A if the gate voltage is 5 V and the resistor is 10 ohm. The name of the hard bias is from here.

Combining the hard bias and the negative feedback, we may get the advantages of the both circuits and overcome the short points of them.

Key words: Hard bias, negative feedback, mixed control, rise time, input impedance, output impedance, stable, out VSWR

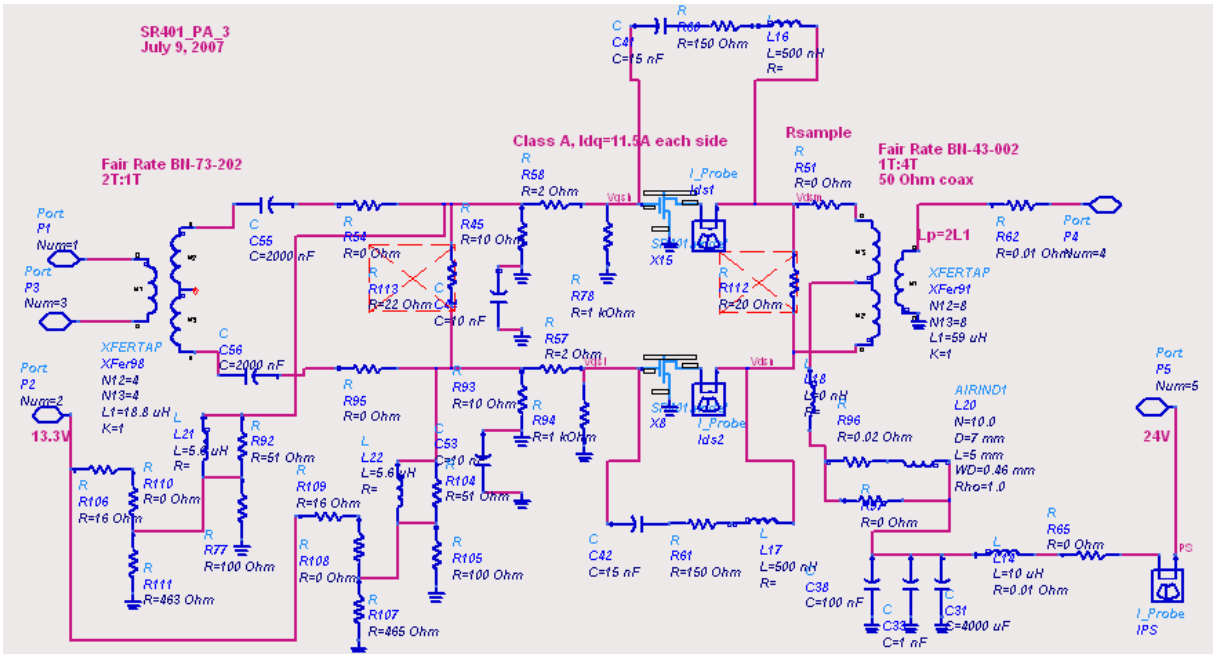


Figure 3.20: DUT with hard bias and feedback

With the schematic of the Figure 3.20, the time domain performance of DUT at 8MHz is shown in Figure 3.21. The rise time is 1us only. The output power is 53.2dBm (>200W) with the sinusoid waveform at the 30dBm input power. Idq is 11.5 A. The envelope of the gate voltage, the Idq and the output voltage is a ideal square. They are very good!

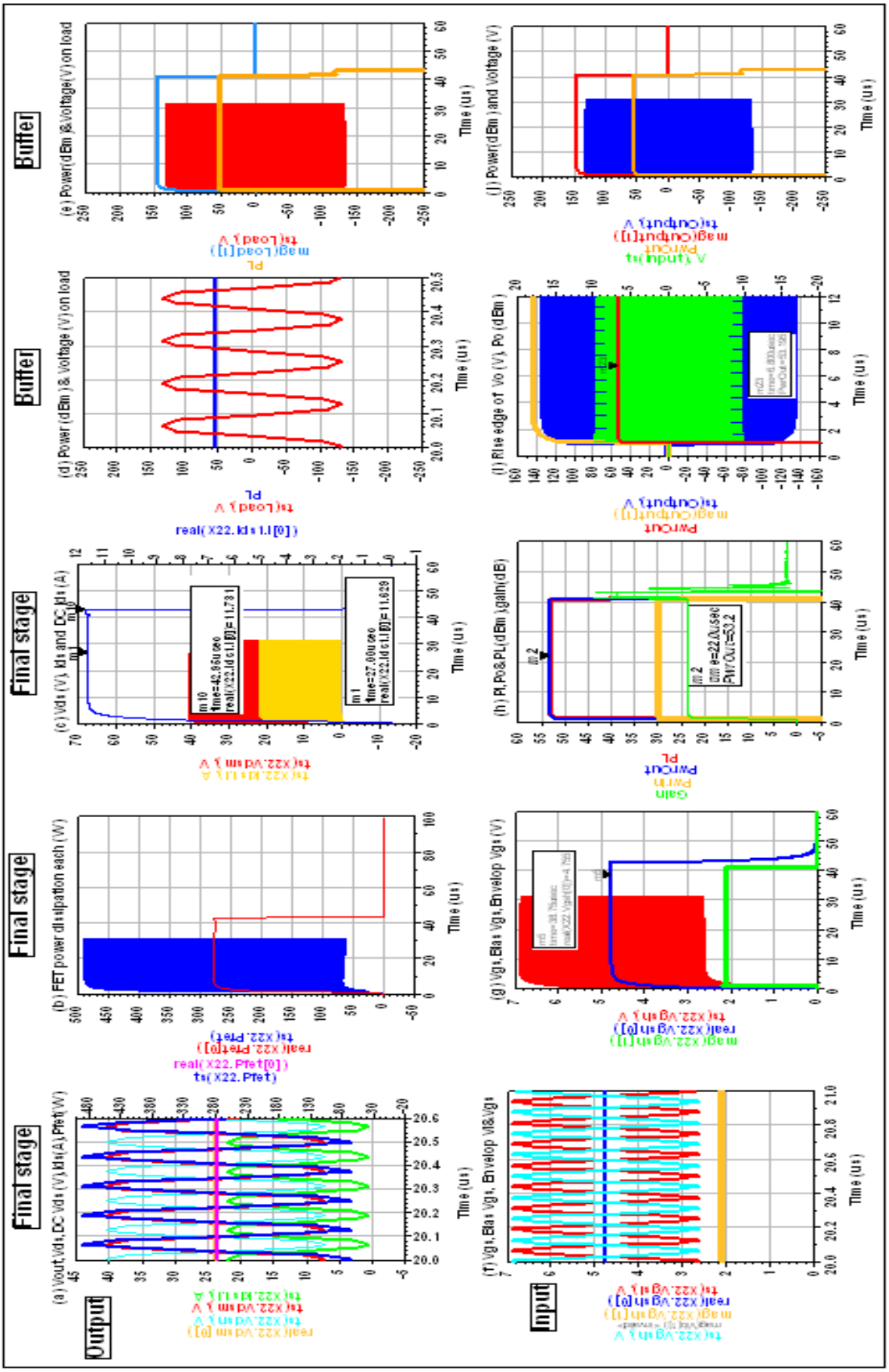


Figure 3.21: Pulse result with hard bias, 8 MHz, Pi=30 dBm, L21/L22=10 uH

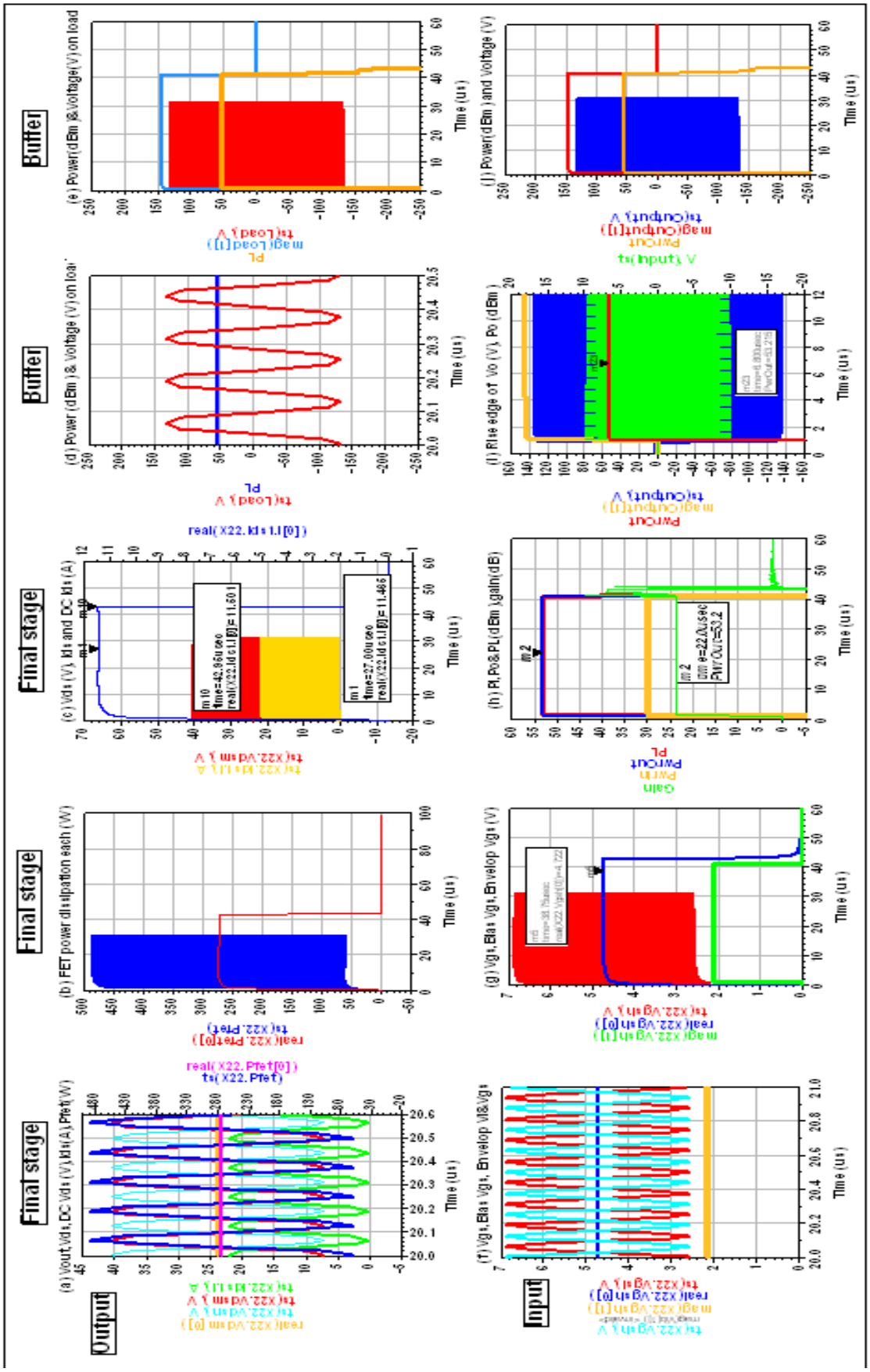


Figure 3.22: Pulse result with hard bias, 8 MHz, Pi=30 dBm, L21/L22=5.6 uH

The rise time is improved further by reducing the bias inductor, L21/L22, from 10 uH to 5.6 uH. The new rise time is so small that it can't be observed at the current time scale. It is less than 0.2 us. At same time, the rest of the pulse performance keeps same. The value of the bias inductor is very important for the rise time also. It will be optimized and tuned in the practice.

The pulse performance at lower RF signal level is simulated in the Figure 3.23. Everything is same as the one at large signal except the signal level itself. It is as expected.

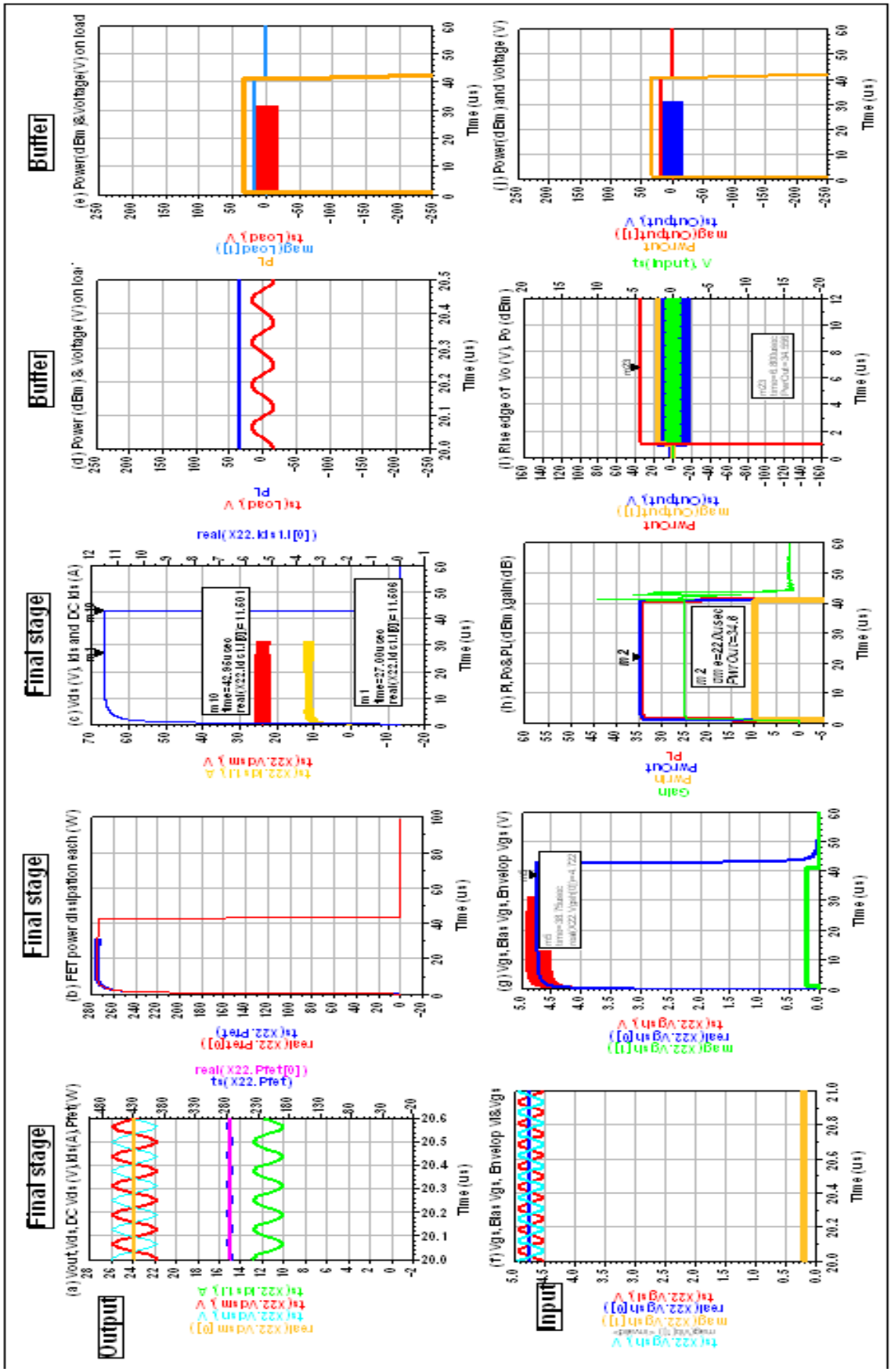


Figure 3.23: Pulse result with hard bias, 8 MHz, Pi=10 dBm, L=5.6 uH

The Figure 3.24 and the Figure 3.25 shows that the DUT is stable with the frequency down to 10 KHz, the input VSWR is good, the out VSWR is good while the frequency is over 30 KHz, the gain is flat across the band although there is a 1 dB bump around 30 KHz, the gain is over 24 dB. The frequency domain performances are very good.

With hard bias, a high current drive with low source impedance is needed. A higher power rate of the gate resistance is needed. DC Vgs needs to be adjusted once the gate resistor is changed.

Figure 3.22Hard bias DUT with the negative feedback is a solution to improve the rise time and the stability. The gate is controlled by the gate shunt branch and the feedback. The rise time is improved because the hard bias reduces the sensitivity of the feedback. A 10 ohm resistor to ground gives a wide band path which the frequency is down to DC so the input VSWR and the stability at the low frequency is improved. At the same time, the output impedance is a constant with the changing of the signal level.

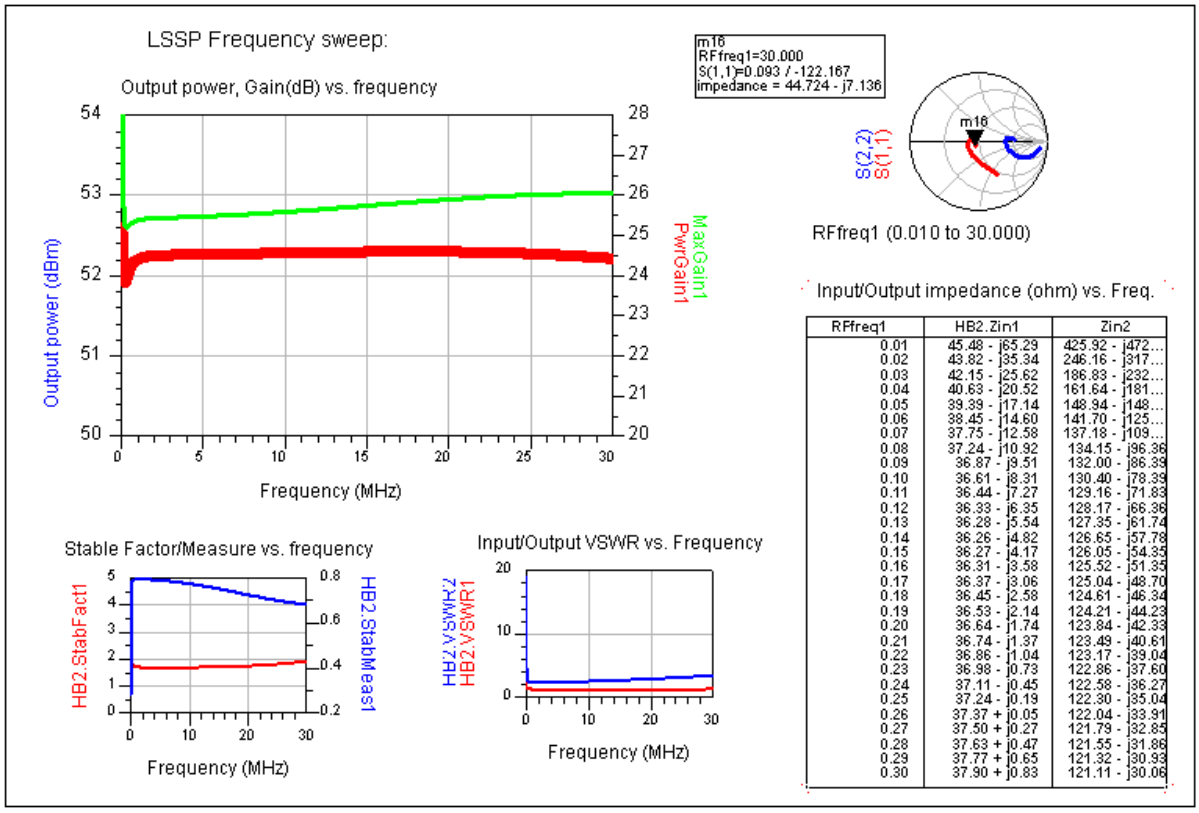
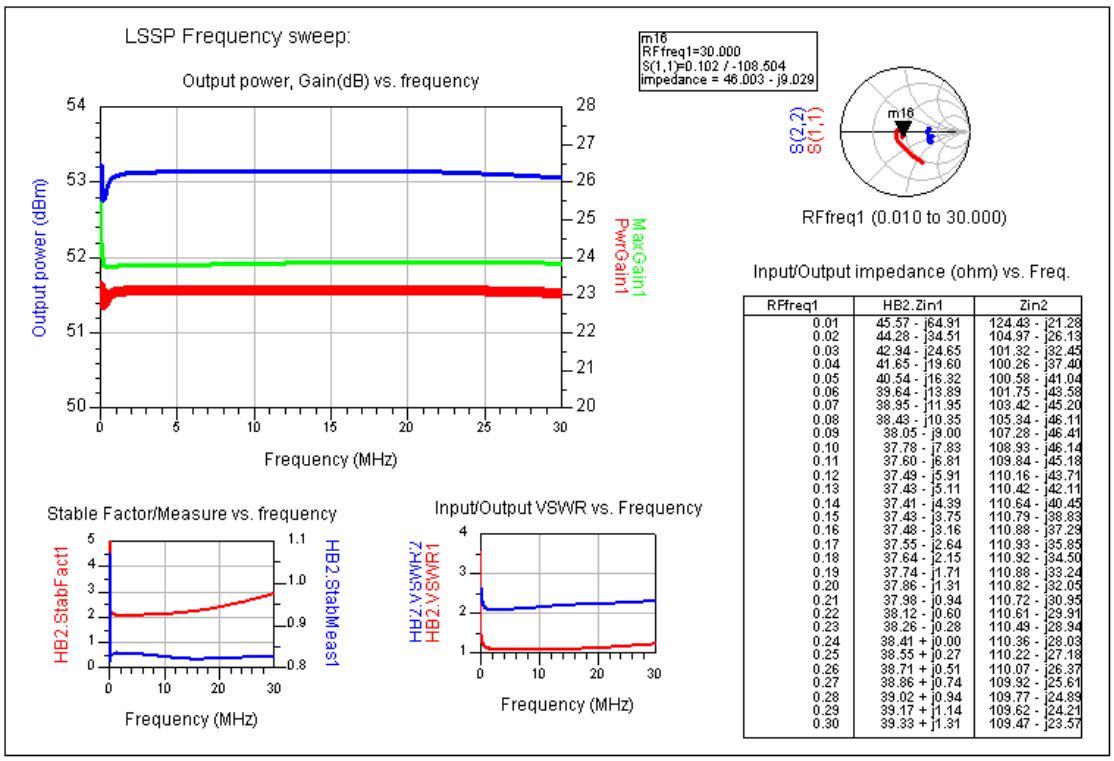


Figure 3.24: Gain and stable, Pi=10 dBm, 10 KHz to 30 MHz with step size 10 KHz



RFfreq1	HB2.Zin1	Zin2
0.01	45.57 - j64.91	124.43 - j21.28
0.02	44.28 - j34.51	104.97 - j26.13
0.03	42.94 - j24.65	101.32 - j32.45
0.04	41.65 - j19.60	100.26 - j37.40
0.05	40.54 - j16.32	100.58 - j41.04
0.06	39.64 - j13.89	101.75 - j43.58
0.07	38.95 - j11.95	103.42 - j45.20
0.08	38.43 - j10.35	105.34 - j46.11
0.09	38.05 - j9.00	107.28 - j46.41
0.10	37.78 - j7.83	108.93 - j46.14
0.11	37.60 - j6.81	109.84 - j45.18
0.12	37.49 - j5.91	110.16 - j43.71
0.13	37.43 - j5.11	110.42 - j42.11
0.14	37.41 - j4.39	110.64 - j40.45
0.15	37.43 - j3.75	110.79 - j38.83
0.16	37.48 - j3.16	110.88 - j37.29
0.17	37.55 - j2.64	110.93 - j35.85
0.18	37.64 - j2.15	110.92 - j34.50
0.19	37.74 - j1.71	110.88 - j33.24
0.20	37.86 - j1.31	110.82 - j32.05
0.21	37.98 - j0.94	110.72 - j30.95
0.22	38.12 - j0.60	110.61 - j29.91
0.23	38.26 - j0.28	110.49 - j28.94
0.24	38.41 + j0.00	110.36 - j28.03
0.25	38.55 + j0.27	110.22 - j27.18
0.26	38.71 + j0.51	110.07 - j26.37
0.27	38.86 + j0.74	109.92 - j25.61
0.28	39.02 + j0.94	109.77 - j24.89
0.29	39.17 + j1.14	109.62 - j24.21
0.30	39.33 + j1.31	109.47 - j23.57

Figure 3.25: Gain and stable, Pi=30dBm, 10 KHz to 30 MHz with step size 10 KHz

As a summary:

Both the time domain and the frequency domain performance are good and meet the requirements.

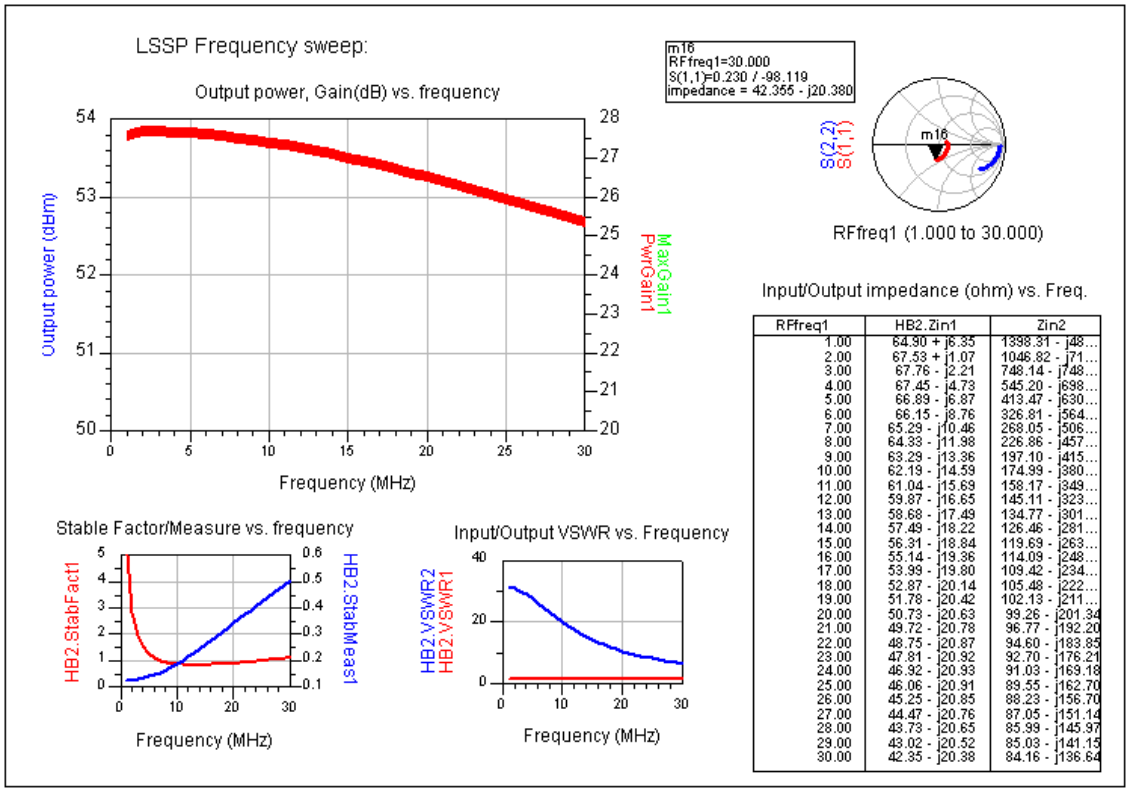
Hard bias DUT with feedback is a solution to improve the rise time and the stability.

The gate is controlled by the gate shunt branch and feedback. Rise time is improved because hard bias reduces the sensitivity of feedback. A 10 ohm resistor to ground gives a wide band path which frequency is down to DC so the input VSWR and the stability at the low frequency is improved. At the same time, output impedance is a constant with changing signal level.

3.4.7.4 Discussion and optimum

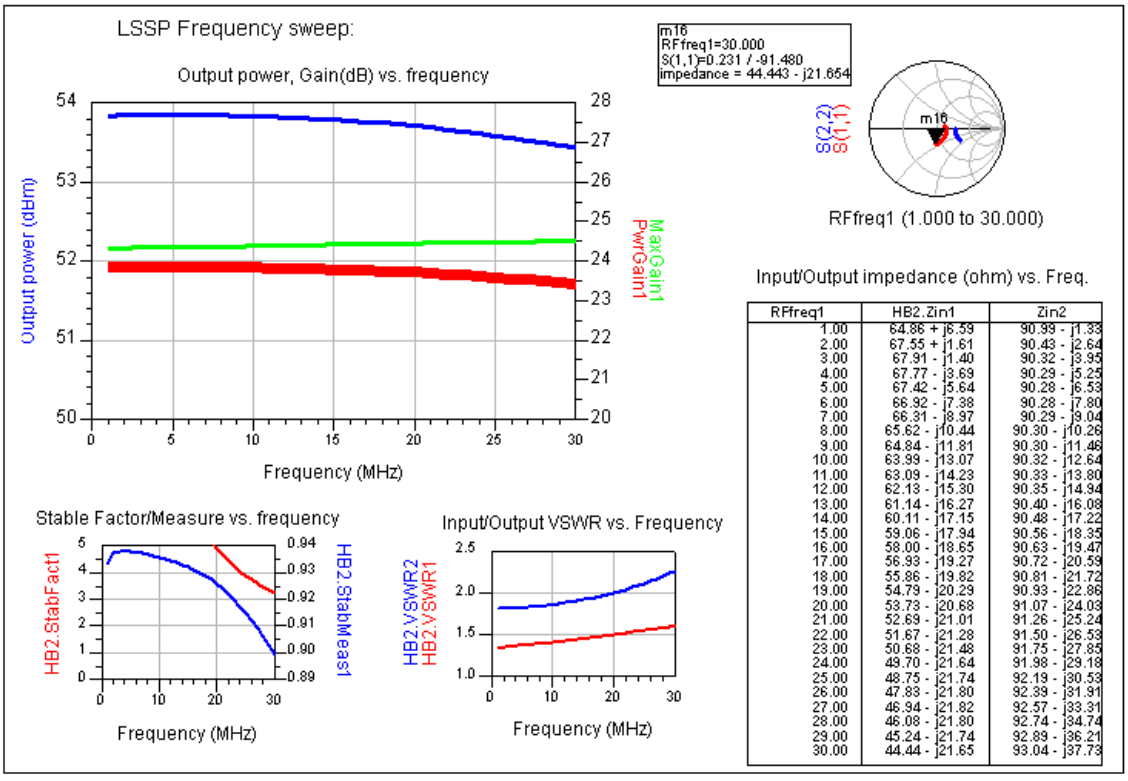
After the technology has been breakthrough, let us discuss some solutions and optimum the performance further.

Can the 10 ohm gate resistor keep the constant output impedance by itself without the negative feedback? The results without the negative feedback are shown in the Figure 3.26 and the Figure 3.27. The stable factor is less than 1 also. To get the desired performance, the hard bias has to combine with the negative feedback.



RFfreq1	HB2.Zin1	Zin2
1.00	64.30 + j6.35	1398.31 - j48...
2.00	67.53 + j1.07	1046.82 - j71...
3.00	67.76 - j2.21	748.14 - j748...
4.00	67.45 - j4.73	545.20 - j698...
5.00	66.89 - j6.87	413.47 - j630...
6.00	66.15 - j8.76	326.81 - j564...
7.00	65.29 - j10.46	268.05 - j506...
8.00	64.33 - j11.98	226.86 - j457...
9.00	63.29 - j13.36	197.10 - j415...
10.00	62.19 - j14.59	174.99 - j380...
11.00	61.04 - j15.69	158.17 - j349...
12.00	59.87 - j16.65	145.11 - j323...
13.00	58.68 - j17.49	134.77 - j301...
14.00	57.49 - j18.22	126.46 - j281...
15.00	56.31 - j18.84	119.69 - j263...
16.00	55.14 - j19.36	114.09 - j248...
17.00	53.99 - j19.80	109.42 - j234...
18.00	52.87 - j20.14	105.48 - j222...
19.00	51.78 - j20.42	102.13 - j211...
20.00	50.73 - j20.63	99.26 - j201.34
21.00	49.72 - j20.78	96.77 - j192.20
22.00	48.75 - j20.87	94.60 - j183.85
23.00	47.81 - j20.92	92.70 - j176.21
24.00	46.92 - j20.93	91.03 - j169.18
25.00	46.06 - j20.91	89.55 - j162.70
26.00	45.25 - j20.85	88.23 - j156.70
27.00	44.47 - j20.76	87.05 - j151.14
28.00	43.73 - j20.65	85.99 - j145.97
29.00	43.02 - j20.52	85.03 - j141.15
30.00	42.35 - j20.38	84.16 - j136.64

Figure 3.26: Output impedance, no feedback, Pi=10 dBm



RFfreq1	HB2.Zin1	Zin2
1.00	64.86 + j6.59	90.99 - j1.33
2.00	67.55 + j1.61	90.43 - j2.64
3.00	67.91 - j1.40	90.32 - j3.95
4.00	67.77 - j3.69	90.29 - j5.25
5.00	67.42 - j5.64	90.28 - j6.53
6.00	66.92 - j7.38	90.28 - j7.80
7.00	66.31 - j8.97	90.29 - j9.04
8.00	65.62 - j10.44	90.30 - j10.26
9.00	64.84 - j11.81	90.30 - j11.46
10.00	63.99 - j13.07	90.32 - j12.64
11.00	63.09 - j14.23	90.33 - j13.80
12.00	62.13 - j15.30	90.35 - j14.94
13.00	61.14 - j16.27	90.40 - j16.08
14.00	60.11 - j17.15	90.48 - j17.22
15.00	59.06 - j17.94	90.56 - j18.35
16.00	58.00 - j18.65	90.63 - j19.47
17.00	56.93 - j19.27	90.72 - j20.59
18.00	55.86 - j19.82	90.81 - j21.72
19.00	54.79 - j20.29	90.93 - j22.86
20.00	53.73 - j20.68	91.07 - j24.03
21.00	52.69 - j21.01	91.26 - j25.24
22.00	51.67 - j21.28	91.50 - j26.53
23.00	50.68 - j21.48	91.75 - j27.85
24.00	49.70 - j21.64	91.98 - j29.18
25.00	48.75 - j21.74	92.19 - j30.53
26.00	47.83 - j21.80	92.39 - j31.91
27.00	46.94 - j21.82	92.57 - j33.31
28.00	46.08 - j21.80	92.74 - j34.74
29.00	45.24 - j21.74	92.89 - j36.21
30.00	44.44 - j21.65	93.04 - j37.73

Figure 3.27: Output impedance, no feedback, Pi=30 dBm

Can the Gain be increased? Because the current input impedance is less than 50 ohm, creasing the gate resistance will increase the gain and the input impedance. The gain, the input impedance and the output impedance are studied when the gate resistor, Rg, changes from 10 ohm to 22 ohm. The detail is shown in Table 3.15. The output impedance reduces due to the more feedback. The 18 ohm gate resistor is the optimum value.

Table 3.15: Gain vs. gate resistor

Rg (ohm)	Gain (dB	Zin (ohm)	Zout (ohm)
10	24.5	44	120
12	25	48	109
15	25.7	52	100
18	26	57	94
20	25.4	63	91
22	24.2	70	93
Condition; 8MHz, pi=10dBm, harrd bias with negtive feedback			

Can the input DC block capacitance be reduced? The frequency domain performance is studied when the RF input DC block capacitor is changed from the 2000 nF to 100 nF. The results are in the Figure 3.28 and the Figure 3.28. The input impedance is degraded only at 0.01 MHz. It is not critical so the 100 nF is chosen.

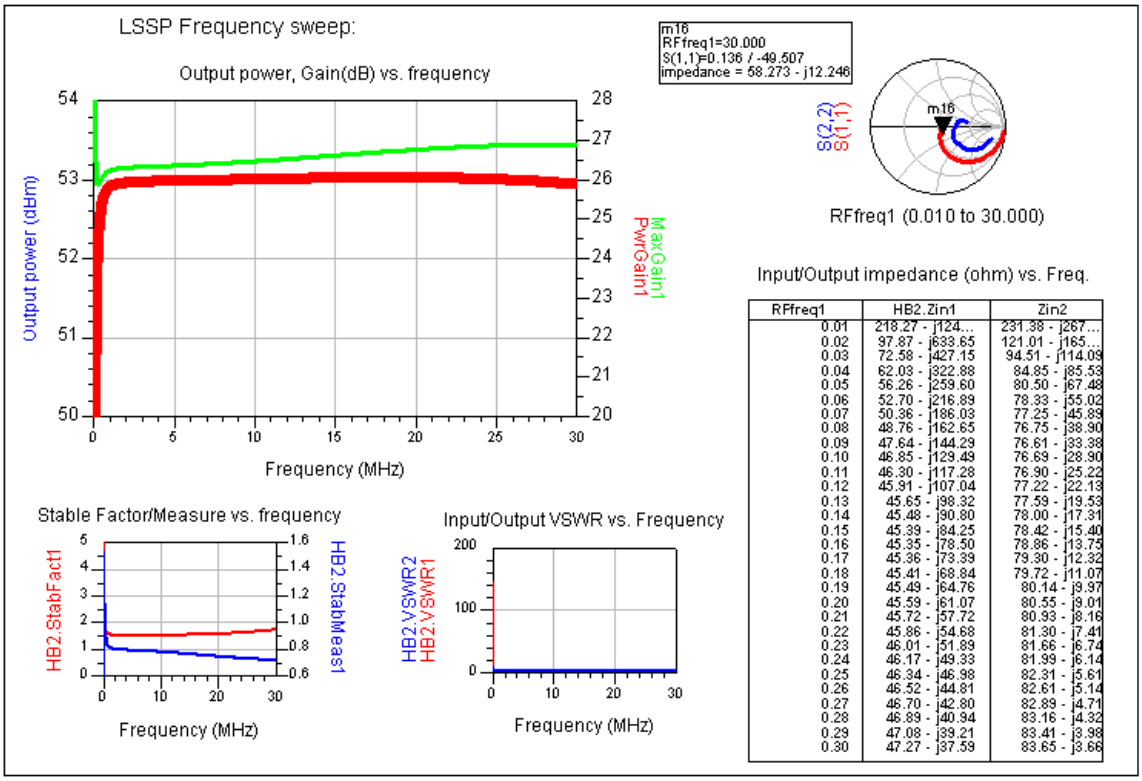
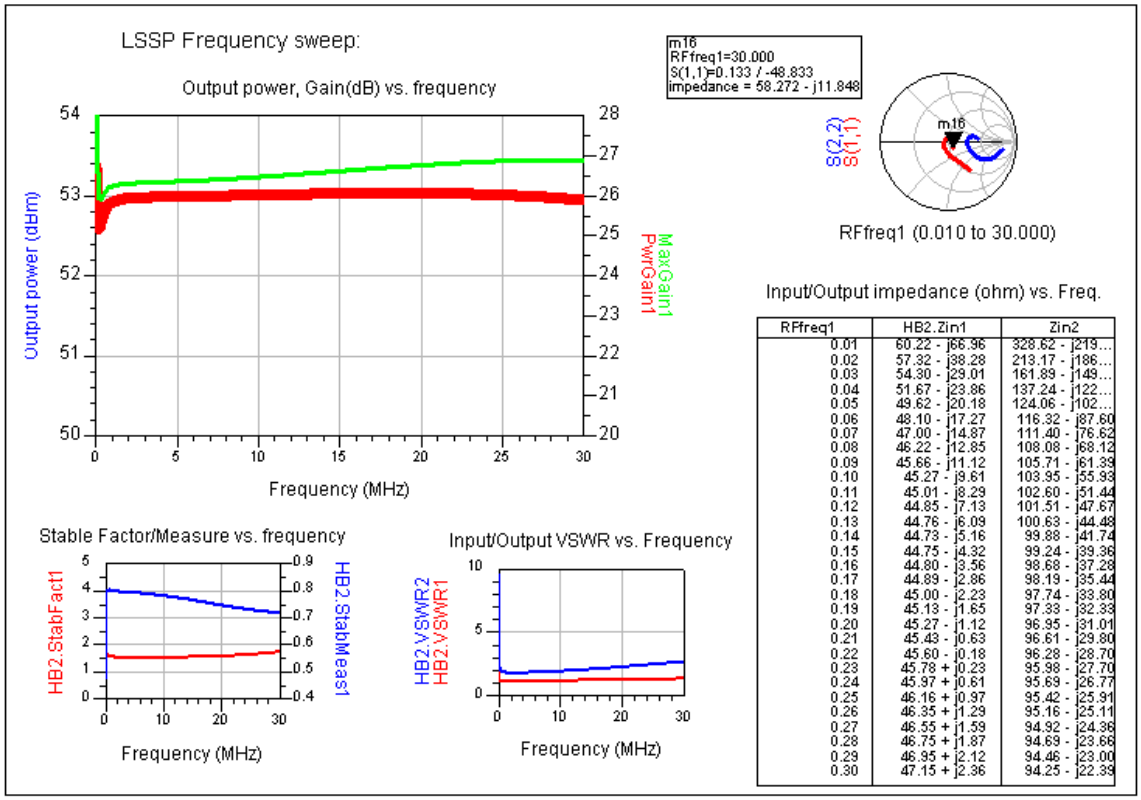


Figure 3.28: Stable and VSWR, C55/C56=100 nF



RFfreq1	HB2.Zin1	Zin2
0.01	60.22 - j66.96	328.62 - j219...
0.02	57.32 - j38.28	213.17 - j186...
0.03	54.30 - j29.01	161.89 - j149...
0.04	51.67 - j23.86	137.24 - j122...
0.05	49.62 - j20.18	124.06 - j102...
0.06	48.10 - j17.27	116.32 - j87.60
0.07	47.00 - j14.87	111.40 - j76.62
0.08	46.22 - j12.85	108.08 - j68.12
0.09	45.66 - j11.12	105.71 - j61.39
0.10	45.27 - j9.61	103.95 - j55.93
0.11	45.01 - j8.29	102.60 - j51.44
0.12	44.85 - j7.13	101.51 - j47.67
0.13	44.76 - j6.09	100.63 - j44.48
0.14	44.73 - j5.16	99.88 - j41.74
0.15	44.75 - j4.32	99.24 - j39.36
0.16	44.80 - j3.56	98.68 - j37.28
0.17	44.89 - j2.86	98.19 - j35.44
0.18	45.00 - j2.23	97.74 - j33.80
0.19	45.13 - j1.65	97.33 - j32.33
0.20	45.27 - j1.12	96.95 - j31.01
0.21	45.43 - j0.63	96.61 - j29.80
0.22	45.60 - j0.18	96.28 - j28.70
0.23	45.78 + j0.23	95.98 - j27.70
0.24	45.97 + j0.61	95.69 - j26.77
0.25	46.16 + j0.97	95.42 - j25.91
0.26	46.35 + j1.29	95.16 - j25.11
0.27	46.55 + j1.59	94.92 - j24.36
0.28	46.75 + j1.87	94.69 - j23.66
0.29	46.95 + j2.12	94.46 - j23.00
0.30	47.15 + j2.36	94.25 - j22.39

Figure 3.29: Stable and VSWR, C55/C56=2000 nF

The pulse performance is checked again after the DUT is modified. The Figure 3.30 shows that the Idq is increased from 11.5 A to over 18 A due to the gate resistor is changed from 10 ohm to 18 ohm; rise time is still good; Output power is lower slightly; Max RF Vgs is too high; input impedance is higher than 50 ohm at large signal because test input power (31 dBm) is higher than setting (30 dBm). In this setting, average Ids is different from the Idq, which is the overshoot at the end of envelope. The thumb of rule is that the average Ids should be same as the Idq. The power supply voltage of the gate drive should be reduced to let the gate bias voltage back to the original value. It is shown in the Figure 3.31.

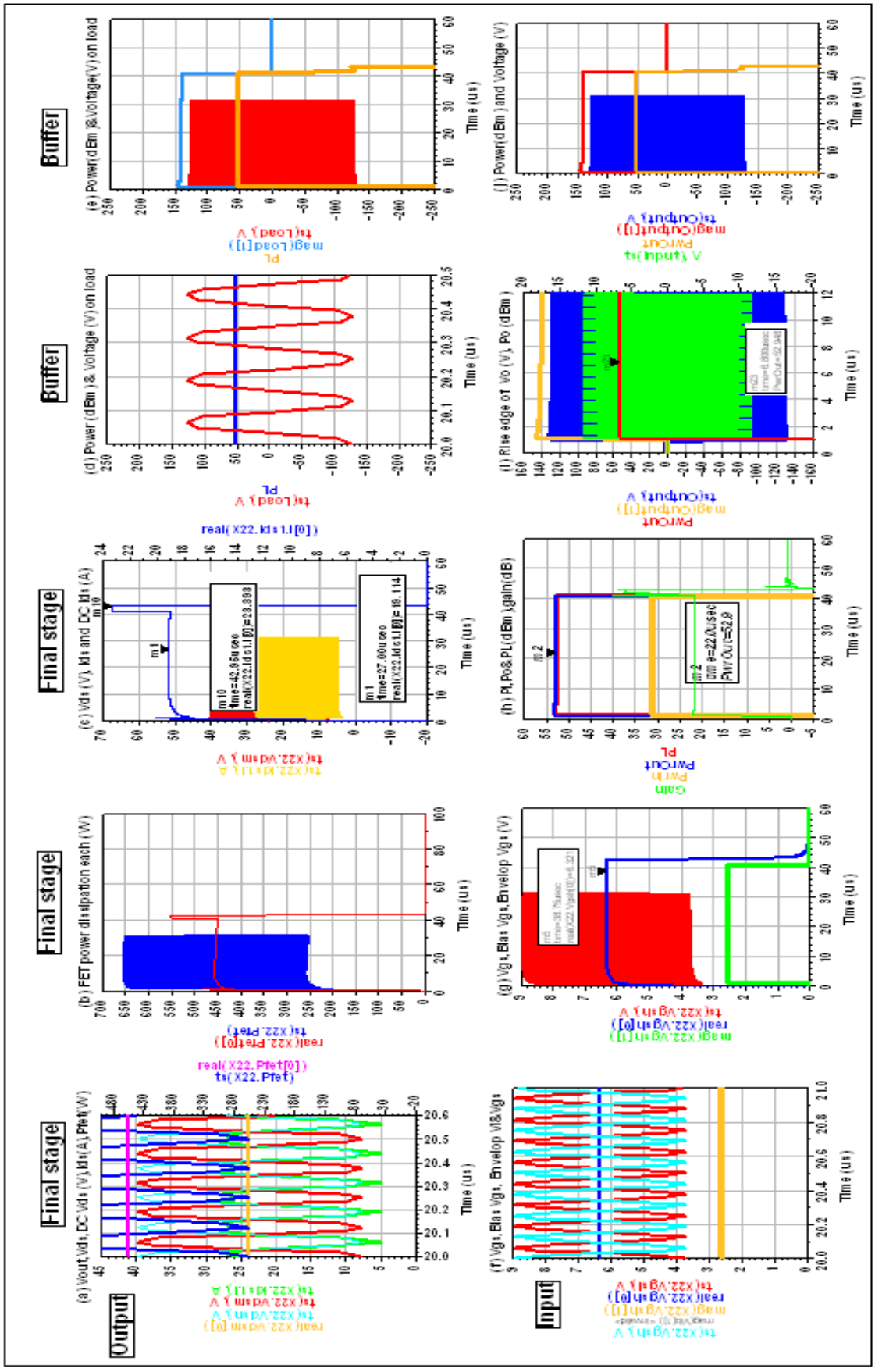


Figure 3.30: Pulse result, 8 MHz, Pi=30 dBm, gate bias drive 13.3 Vpp

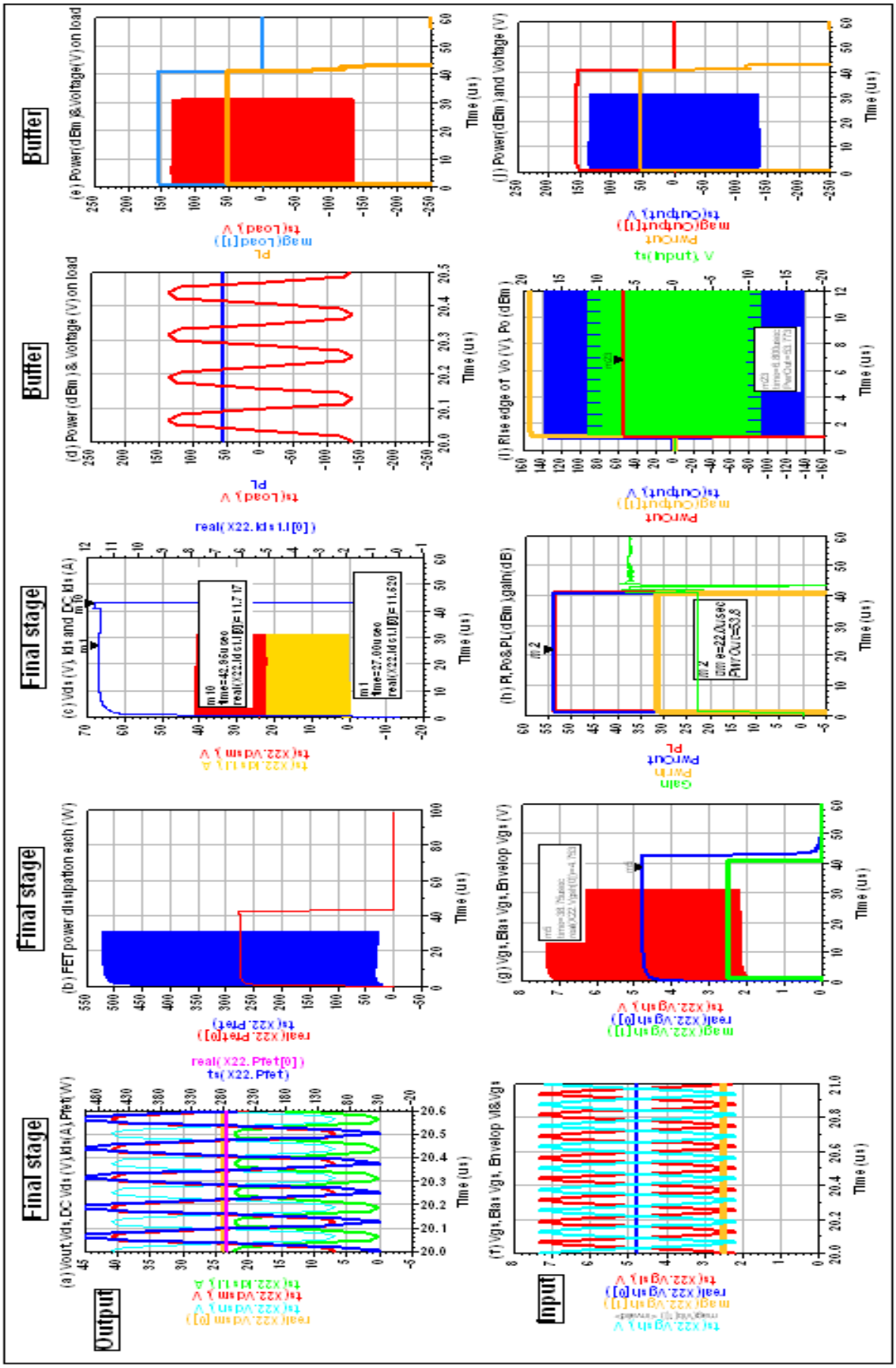


Figure 3.31: Pulse result, 8 MHz, Pi=30 dBm, gate bias drive 10 Vpp

Comparing the Figure 3.30 and the Figure 3.31, the gate drive voltage changes from 13.3 V to 10 V, Idq is back to the optimum values, which is the same as the DC Ids (average Ids). The gain is increased 1 dB, which lets the output power increase 1 dB and reaches 53.8 dBm. The gain reaches the maximum at the optimum Idq. Changing C55/C56 from 2000 nF to 100 nF doesn't affect any pulse performance.

So far, the setting of the DUT is as the Figure 3.32.

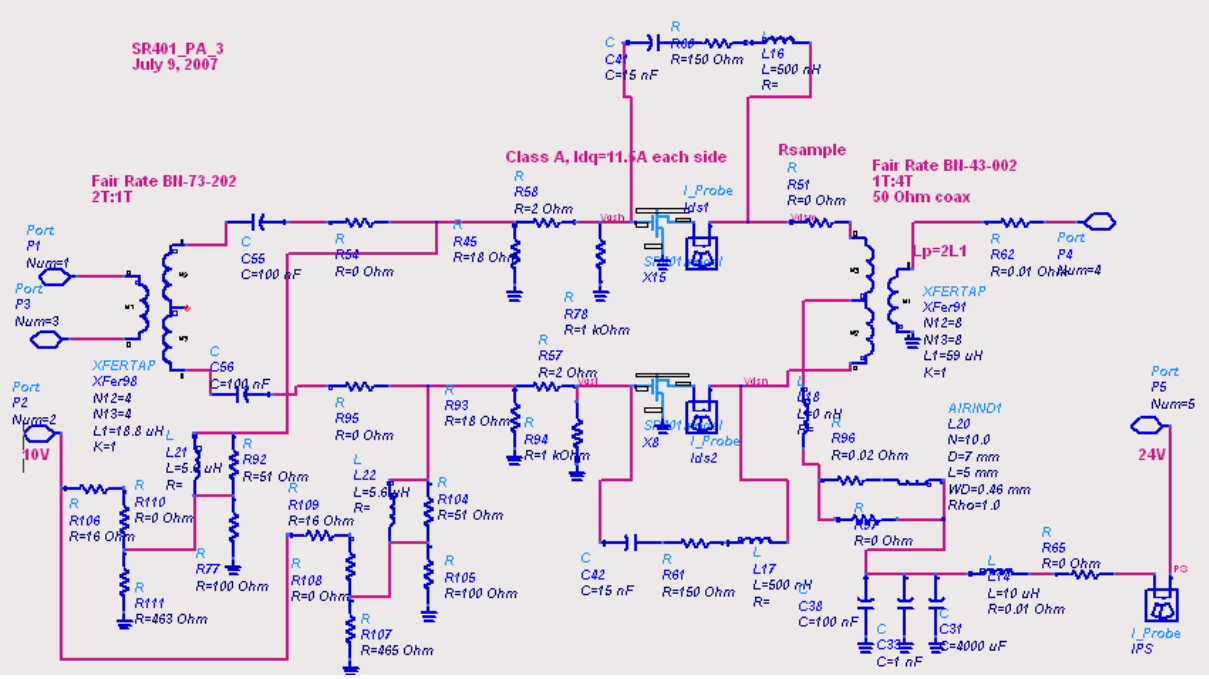


Figure 3.32: New DUT-1

The DUT gate bias circuit has been modified for simple operation as is shown in Figure 3.32. The 16 ohm of R106/R109 is the source resistance of the MOSFET drive TC1416. The R77/R105 is a 100 ohm potentiometer, which is for fine tuning of Vgs. The R55/R57 has been used for stability. The R78/R94 is for ESD protection. The R45/R93 is for the low input impedance and the low feedback sensitivity. The R111 / R107 can be reduced further.

3.4.7.5 Summary

As a summary, optimum schematic is in the Figure 3.32.

The time domain performance is in Figure 3.31.

The frequency domain performance is in Figure 3.28.

How can the Idq of FET be tuned? In the Figure 3.32, the R66 / R69 are the output resistor of the gate drive. The R77 / R105 are the potentiometer of a 100 ohm multi-turns. It is used in adjusting Idq of each side of FET. In Table 3.16, Idq vs. value of R77 / R105 are shown. The adjusting range of Idq of each side is in the expected range. If the higher gate voltage is wanted, the supply voltage of the TC1426 can be increased so the drive voltage is increased.

The max supply voltage can be up to 16 V. The drive voltage is the output voltage of the gate drive without the load.

Table 3.16: Fine tuning Vgs

R77 (ohm)	100	80	50	30
Idq (A)	12.5	11.5	10	7.5
Condition: Drive 10Vpp				

The results of both time domain and frequency domain are satisfied.

3.5 Study of the final stage

3.5.1 Formula vs. simulation for the max Po

Comparing the max output power from the formula (1) and the simulation in the Table 3.17, they are very similar and the simulation one is lower slightly.

Table 3.17: Formula vs. simulation for the max Po

	Fomular		Simulation		Idq	Gain
Transformer	W	dBm	W	dBm	A	dB
1:3	170	52.3		52	8.5	
1:4	300	54.8		53.9	11.5	25

3.5.2 The Rise time vs. the LP of the output transformer

No effect if other setting is right.

3.5.3 Spike vs. Idq

The spike depends on the difference of the Idq of each side FET rather than the Idq itself.
When the delay of the gate blank and RF signal is increased, the spike is separated with the envelope of RF signal and the envelope is ideally rectangular. This is shown in the Figure 3.33. The distorted envelope is caused by the spike only. If the spike can be remove or minimized, the envelope will be rectangular.
From the Figure 3.33, the spike of the output voltage is caused by the spikes of Vdsh and Vdsl. The spike of Vdsh/Vdsl is caused by the edge of Vgsh/Vhsl. Output spikes are built by four small spikes, two positive and two negative. The first two are caused by the rising edge of the gate blanking and the last two are caused by the falling edge of the gate blanking. Output spikes, V1 to V4, are the remainder of the canceling of the high and the low side voltage. The V1 is relative to the rising edge of the high side of the gate blank, the V2 is relative to the rising edge of the low side of the gate blank and so on. The amplitude of the output spike is defined as the maximum amplitude of the four output spikes.

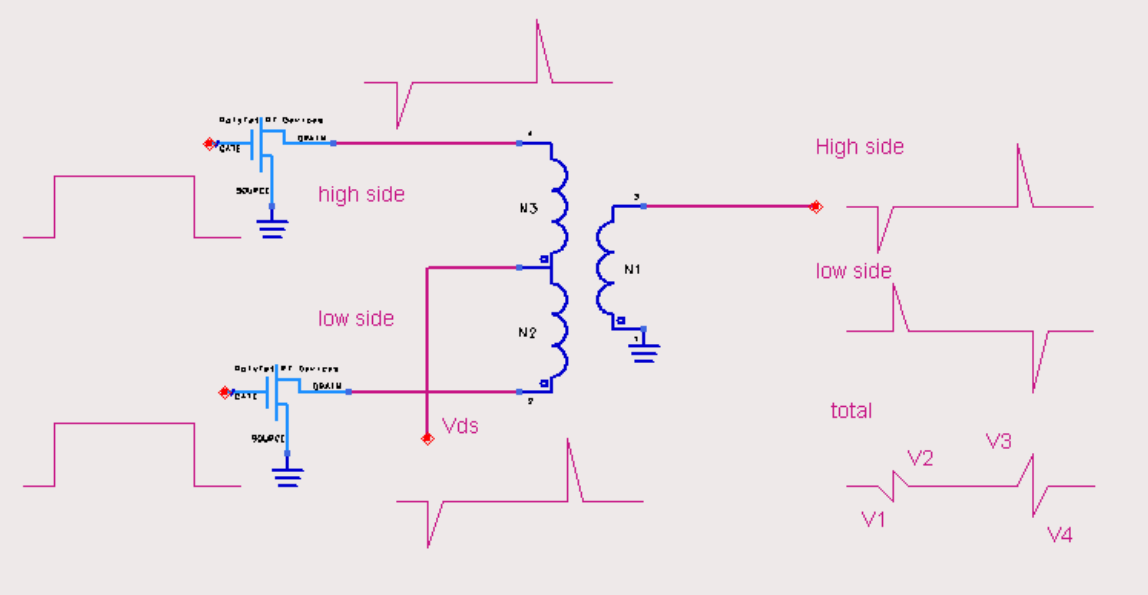


Figure 3.33: Relationship of spikes

For reducing the output spike, three criteria should be met:

- The amplitude of output voltage produced by each side FET should be the same.
- The delay of each side of FET should be the same.
- The quality factor of the input circuit of each side of FET should be the same.

Solutions of above criteria are:

- Adjust the Vgs of each side of FET
- Adjust the relative delay between each side of FET
- Adjust the loss of RC tank through a potentiometer at the input of each side of FET

Because of the method of feeding Ids (feed at central of primary wind of output transformer), the spike can be cancelled at output.

If the spikes come from the drive stage, how is it present at the output? From the principle of the push-pull, the output RF signal is the sum of each side of the FET. The spikes from the drive stage are viewed as a kind of RF signal. It can't be cancelled at the final stage. This is the reason to avoid using pulsed gate at the drive stage.

3.6 NMR probe as a part of HPA Principle

3.6.1 Principle

In designing an oscillator, a method called the reflection approach [49] has been used. It is called negative resistor approach also. If a circuit can oscillate and what can be the oscillation frequency is judged by this method.

A circuit is divided into two parts: Left Hand Side (LHS) circuit and Right Hand Side (RHS) circuit. The interface can be at any place of the circuit but the RHS circuit is a passive circuit (load) and the LHS is the active circuit (source) in general. It is shown in Figure 3.34.

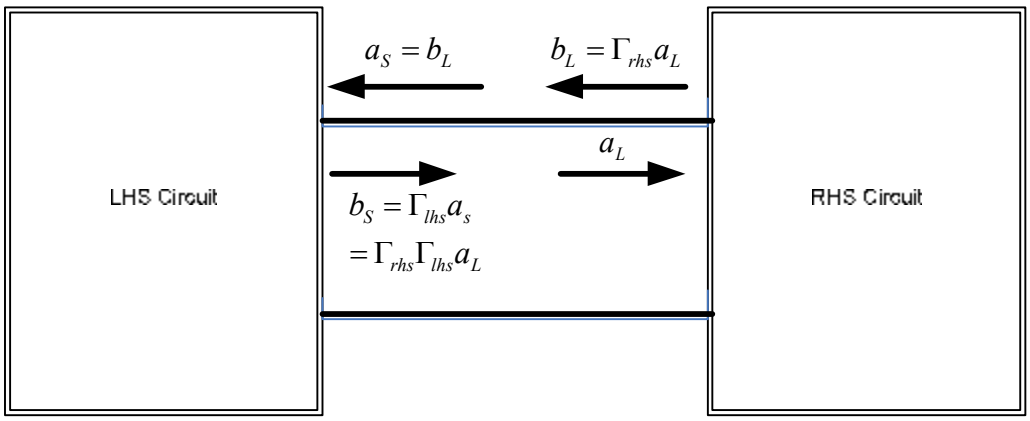


Figure 3.34: Reflection gain illustration

Steady-state oscillation will occur in a circuit when

$$b_L = \Gamma_{rhs} a_L \quad \textbf{(3.6)}$$

$$a_S = b_L \quad \textbf{(3.7)}$$

$$b_S = \Gamma_{lds} a_S \quad \textbf{(3.8)}$$

$$b_S = a_L \quad \textbf{(3.9)}$$

Where a_L is the incident signal on the load.

b_L is the reflected signal from the load.

a_S is the incident signal on the source.

b_S is the reflected signal from the source.

Γ_{lhs} is the reflection coefficient to the LHS.

Γ_{rhs} is the reflection coefficient to RHS.

The criteria of the steady-state oscillation are given by the four equations above:

$$\Gamma_{rhs} = \frac{1}{\Gamma_{rhs}} \quad \textbf{(3.10)}$$

It can also be expressed in:

$$\left|\Gamma_{rhs}\right| = \left|\frac{1}{\Gamma_{lhs}}\right| \quad \textbf{(3.11)}$$

And

$$\angle\Gamma_{lhs} = \angle\frac{1}{\Gamma_{rhs}} \quad \textbf{(3.12)}$$

The criteria of the start up oscillation are:

$$|\Gamma_{rhs}| \geq \left|\frac{1}{\Gamma_{lhs}}\right| \tag{3.13}$$

And

$$\angle\Gamma_{lhs} = \angle\frac{1}{\Gamma_{rhs}} \tag{3.14}$$

The oscillation strength can be expressed in transducer power gain:

$$G_T = \frac{\left[1-|\Gamma_{rhs}|^2\right]\left[1-|\Gamma_{lhs}|^2\right]}{\left|1-\Gamma_{lhs}\Gamma_{rhs}\right|} \tag{3.15}$$

The S-parameter simulation in frequency domain will be carried and the setting is shown in Figure 3.35. Where, S11 is Γ_{lhs}; S22 is Γ_{rhs} or m=1/S22=1/Γ_{rhs}. The RHS is a NMR probe, Mole. The resonant frequency of the Mole is 3.3 MHz. The LHS is the whole HPA.

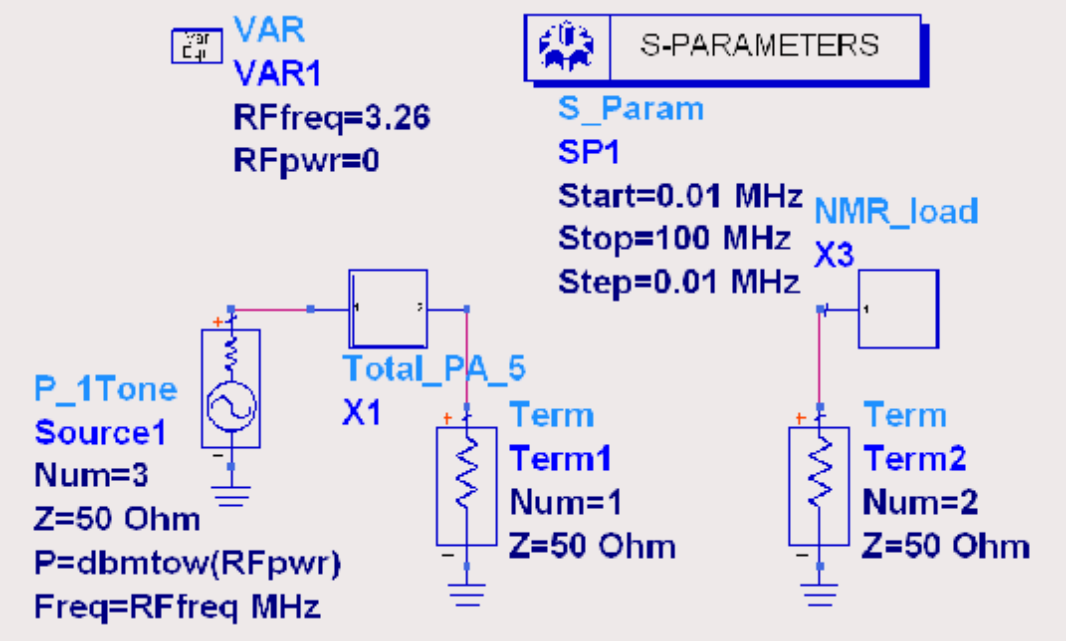


Figure 3.35: Set up for analysis of reflection performance

3.6.2 Initial results

The line up of the whole HPA is SGA7489 + L88016+ SR401. The schematic of the final stage is shown in the Figure 3.36.

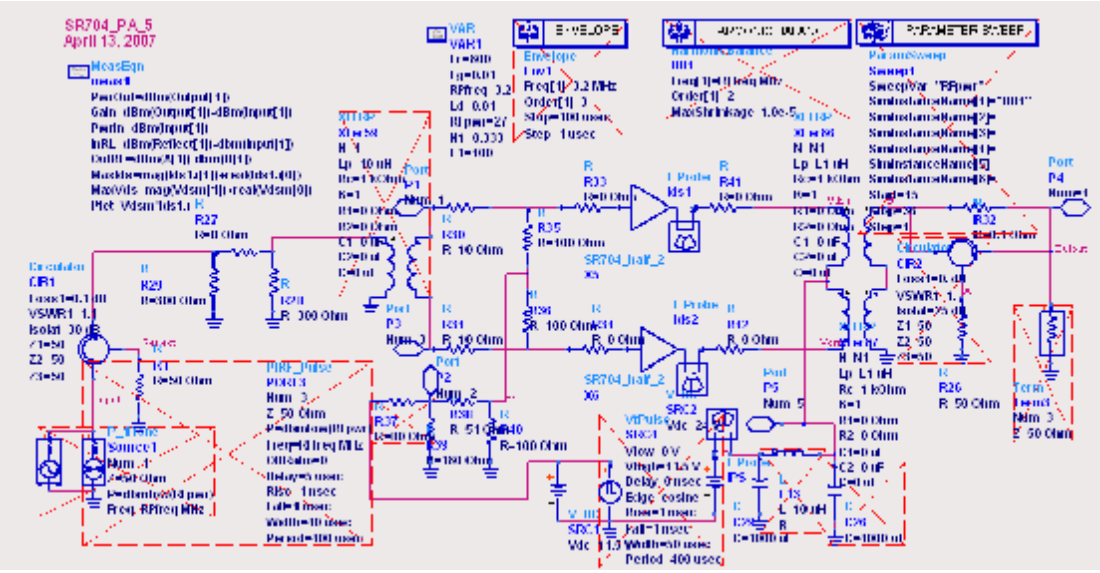


Figure 3.36: Final stage in original condition

The simulation results are shown in the Figure 3.37. There are four sub-figures in it. Left top one is the outline of the S11, m=1/S22 and the reflection gain, Grefl. Where Grefl = G_T. The phase of the S11 and S22 are on the right side of the Y axle. The magnitude of S11 and S22 and the Grefl are on the left side of Y axle. When the phase traces cross, the circuit may be oscillation. The oscillation frequencies are around the 0.8 MHz and around the 3.7 MHz. The 0.8 MHz point is zoomed in and is displayed in the Left bottom sub-figure. The magnitude and phase criteria are met at same frequency and the reflection gain is high. The HPA will oscillate at the 0.84 MHz! The 3.8 MHz point is zoomed in and is shown in the right bottom sub-figure. The phase criteria is met but the magnitude criteria is not meted. It will not oscillate in the theory but it is easy to turn to the oscillation status in practice if the gain is increased. So the 3.78 MHz is treated as an oscillation point. In the Smith chart of the right top sub-figure, the traces of the S11 and S22 are displayed. The S11 is more the 1 because it is out of the unit circle. It indicates there is a potential of the oscillation. On the other hand, if S11 is less than 1 (it is in the unit circle), the circuit is stable. Remember S22 is always less than 1 because it is a passive circuit.

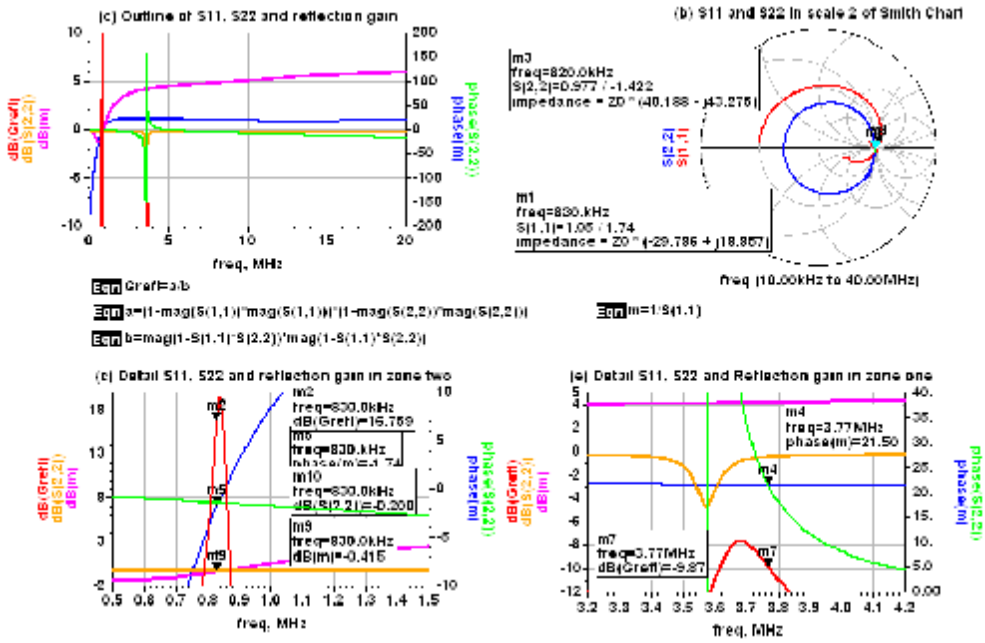


Figure 3.37: HPA reflection with SGA7489+L8821P+SR401 in original condition (Lm=1.5uH)

The oscillation is experienced while HPA works at the 1 MHz or the 3.7 MHz. They agree with simulation. It means the simulation is accuracy.

The NMR probe is a resonant. When it connected with an amplifier, the HPA turns to a typical oscillator. It will oscillate if the criteria are met. If the load is a 50 ohm resistor, it may not oscillate.

3.6.3 Optimum results

In last section, the reason of the oscillation was found. Here we will find the solution to kill the oscillation.

The NMR probe is a resonant. It is a good component for oscillator but it can't be removed because it is an important part of the NMR system. If the gain of the DUT is reduced, the magnitude criteria will be not met. The solution is:

- Input H type attenuator to reduce gain and reduce the impedance
- 1 ohm resistor between drain of the FET and the output transformer
- 1 dB attenuator between NMR probe and output of the DUT
- Lower impedance gate resistor between the gate and the ground to reduce the changing of the reactive part of the DUT
-
- The detail DUT setting is shown in the Figure 3.38.

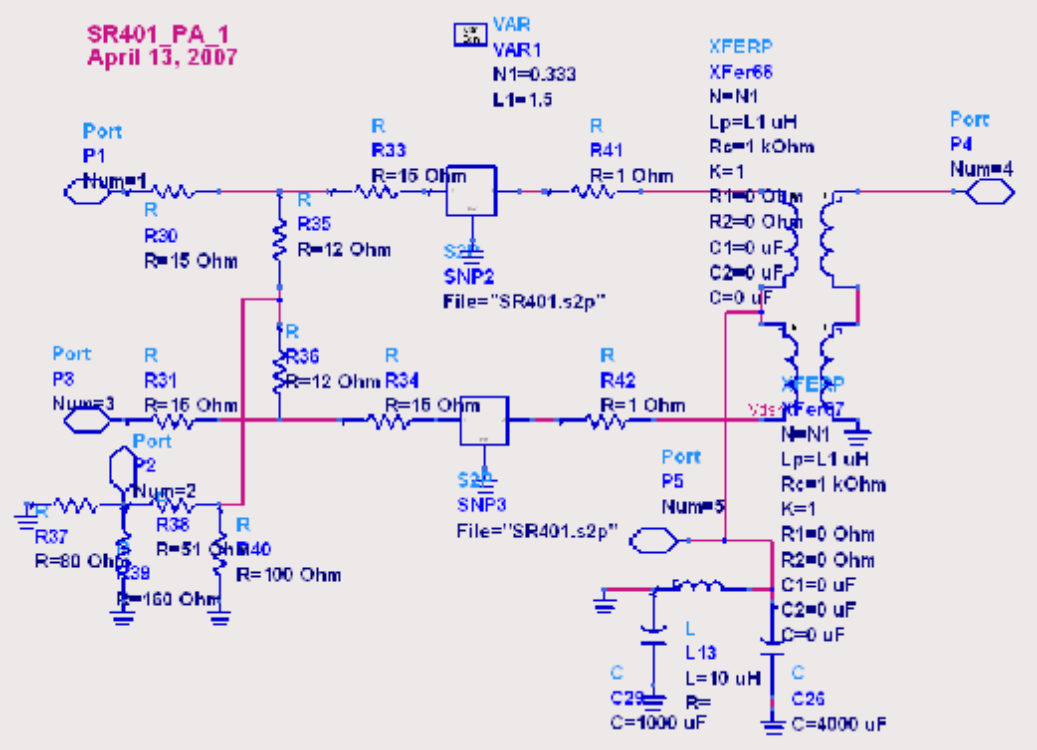


Figure 3.38: SR401 stage

The simulation results are shown in the Figure 3.39. In the Smith chart of the right top sub-figure, S11 is less than 1 so that the DUT is stable.

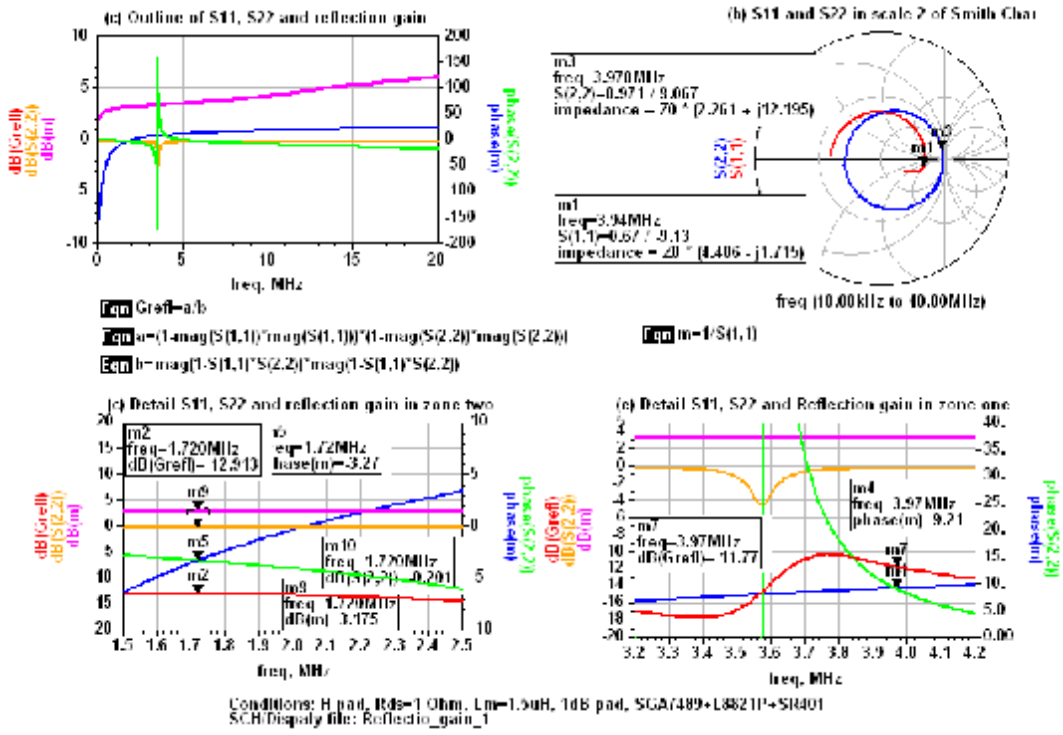


Figure 3.39: Reflection of HPA with optimum circuit

3.6.4 Summary

In this chapter a method has been reported to check whether the DUT will oscillate and to find the oscillation frequency. The simulation shows there is the oscillation if DUT is terminated with the Mole, a kind of NMR probe. The DUT turns to stable status after optimizing the parameters of the DUT. Points:

- The DUT is simulated not only in the load of 50 ohm but also in the load of NMR probe.
- Different simulation tools have different function. The envelop simulation can't find the oscillation. The reflection coefficient approach is a powerful tool to check the oscillation.
- Solutions to avoid the oscillation: the suitable RF power FET, the good matching between drive stage and the final stage, the input ATT pad and the 1dB output ATT pad.

3.7 ATT vs. load VSWR

3.7.1 Issue

The RF power FET of the last stage of the HPA may be damaged if it is terminated with the Mole, a NMR probe, although it works well with a 50 ohm load. The reason is the poor load VSWR of the Mole, which is shown in the Figure 3.40. The bandwidth of the VSWR is less than 10:1 is only about 200 KHz. It means that in most of time, The HPA will work in the condition in which the VSWR is higher than 10:1. On the other hand, the most of the RF power FET only can withstand with the max load VSWR of 10:1[34]. The reason of damaging The FET is that the operating condition of the load VSWR is out of the specification of the FET.

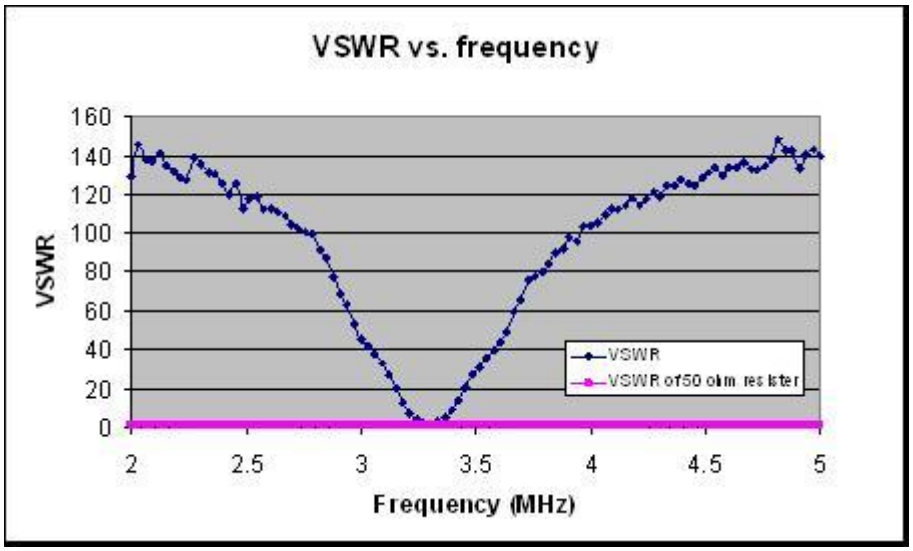


Figure 3.40: VSWR of the Mole

3.7.2 Options and discussion

There are several options to solve these issues:

- VSWR protection
- Power degradation
- Isolation
- Absorbing filter
- ATT

The VSWR protection is a negative feedback system. Once the high VSWR, it will shut down the gate bias of the last stage to protect the FET. The response time is about 20-60 us. The advantage is no degradation of the max output power if load VSWR is good and wide band. The disadvantage is: response time may not faster enough; the circuit is complex.

Power degradation is to protect the FET by reducing the output power from its max rate power. The advantage is simple and wide band. The disadvantage is that the output power may be reduced a lot to reach the safe level.

Isolation is inserting an isolator between the HPA and the NMR probe. The isolator is a one direction device. The reflection power from the probe will go to the isolation port and is consummated in the 50 ohm load of this port. If viewing towards the NMR probe from the output of the HPA, the load is viewed as an ideal 50 ohm without any reflection. The advantage is no degradation of the max output power and simple. The disadvantage is the bandwidth is narrow, which typical is less than 20%. In out condition, 1-30MHz wide bandwidth is needed.

The absorbing filter gives a 50 ohm load s

out of band. As a reference, general filter gives full reflection out of band. So the absorbing filter gives good VSWR whatever in band or out of band. The advantage is no degradation of the output power. The disadvantage is the narrow band. It is not suitable for our wide band requirement.

ATT is inserting an attenuator between the HPA and the NMR probe. It reduces the equivalent load VSWR to protect the FET. The advantage is simple and wind band. The disadvantage is the degradation of the output power.

3.7.3 Solution

From the discussion of the above section, the best option is the ATT.

What is the requirement of the load VSWR for safety of the FET? In the FET datasheet, there is a max load VSWR rate for the rated output power. The FET will be safe if the load VSWR is under this max rate load VSWR. For the PolyFET SR401, max load VSWR is 10:1 for CW300 W power at 175 MHz. The lower frequency it is, the lower max load VSWR it is. It is assumed that max load VSWR of SR401 is still 10:1 for pulse 200 W with 10% duty cycle at 1 MHz.

What is the value of the ATT?

The Table 3.18 shows the relationship between the equivalent VSWR and the ATT. The equivalent VSWR will be less than 9:1 if ATT is more than 1 dB so that The FET will be safe.

Table 3.18: Equivalent VSWR vs. ATT

ATT	NMR load VSWR	S22	S22	Equival VSWR	Notice
dB		dB			
0	100	0	1	100	
0.2	100	-0.4	0.95	43.4	
0.4	100	-0.8	0.91	21.7	
0.6	100	-1.2	0.87	14.5	
0.5	100	-1	0.89	17.4	
0.8	100	-1.6	0.83	10.9	
1	100	-2	0.79	8.7	Threshold
1.5	100	-3	0.71	5.8	
2	100	-4	0.63	4.4	
3	100	-6	0.50	3.0	
4	100	-8	0.40	2.3	
5	100	-10	0.32	1.9	
6	100	-12	0.25	1.7	
7	100	-14	0.20	1.5	
8	100	-16	0.16	1.4	
9	100	-18	0.13	1.3	
10	100	-20	0.1	1.2	
S22(dB)=2*ATT, S22=10^(S22(dB)/20), Equival VSWR=(1+S22)/(1-S22) Setting: DUT (FET)+ATT+NMR load					

The test results are shown in the Figure 3.41. The equivalent VSWR is 8:1 with 1 dB ATT. It is very close to the calculation data.

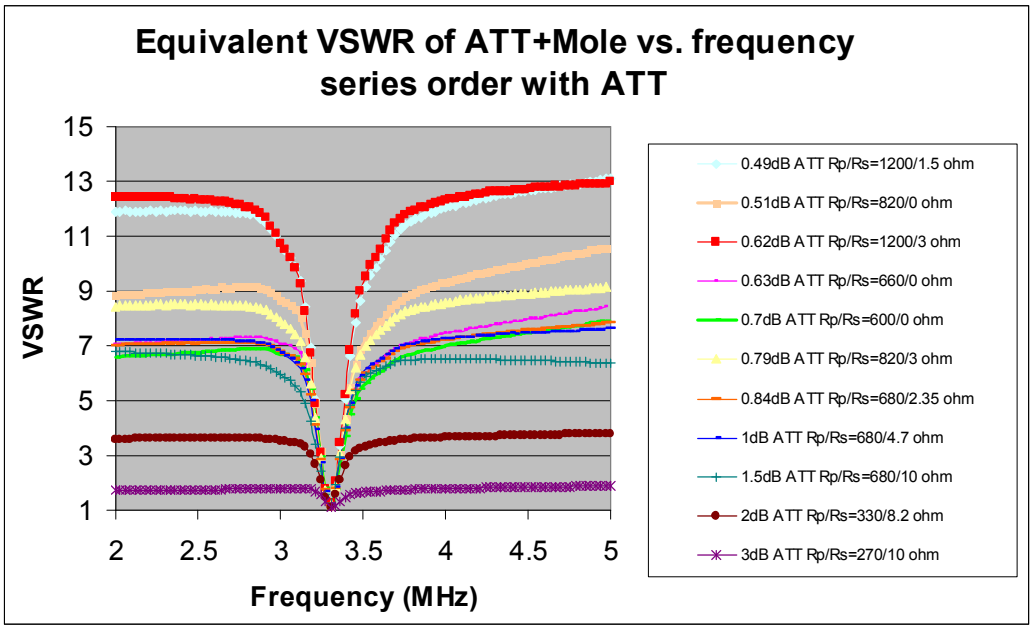


Figure 3.41: VSWR vs. ATT in experience

For the margin, 1.5 dB ATT is used. The output power will reduce from 180 W to 140 W but is still meets the requirement.

If the Philips FET BLF248 [30] is used, its max load VSWR is more than 50:1. It gives the more margin.

4 CHAPTER FOUR

FABRICATION AND EXPERIMENTS

4.1 Introduction

This chapter describes the assembly and test information for the HPA. Because the RF power FET is expensive, special care is taken during assembly and testing to avoid damaging the FET.

4.2 PCB and module

The HPA is built in three parts: PCB and assembly (Figure 4.1), heat sink (**Error! Reference source not found.**), and a metal box. The metal is on the PCB to shield the circuit. The RF power FET is screwed onto the heat sink and Thermal compound is applied in advance. Anti-static solution should be applied during assembly and testing.

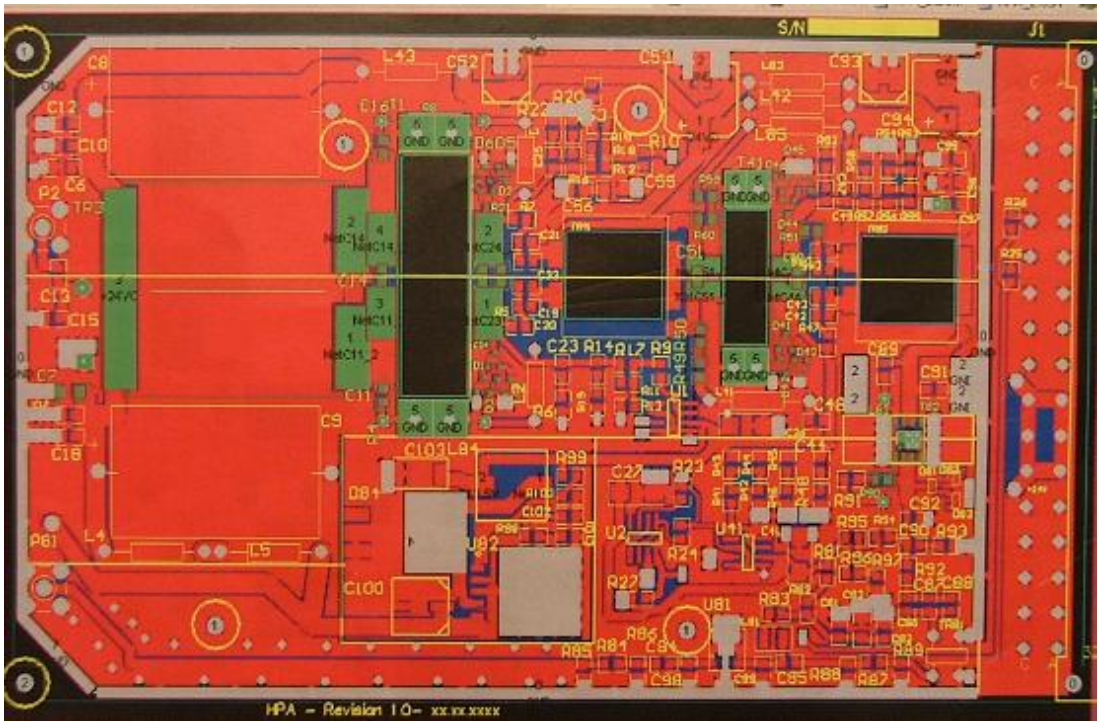


Figure 4.1: PCB and assembly

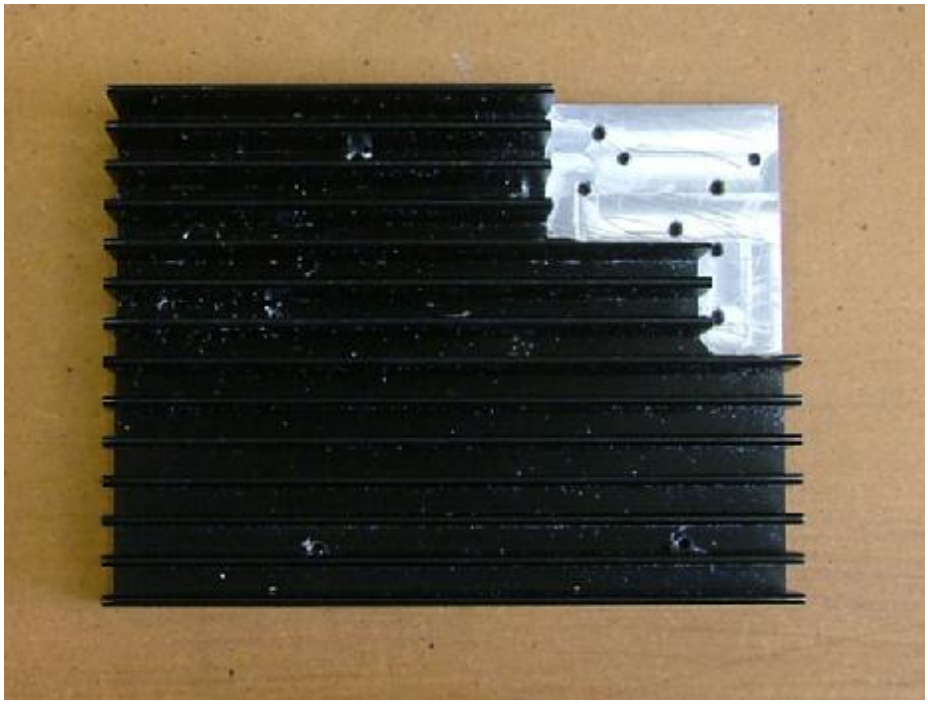


Figure 4.2: Heat sink

4.3 Boost

4.3.1 Introduction

Boost includes the pre-drive stage and the drive stage. This Continue wave (CW) mode boost is on a daughter board. The daughter board is connected with the heat sink for thermal dissipation. Circuit detail, test methods and results are shown in the following sections.

4.3.2 Schematic and layout

The schematic has three parts: pre-drive stage, drive stage, and power regulator.

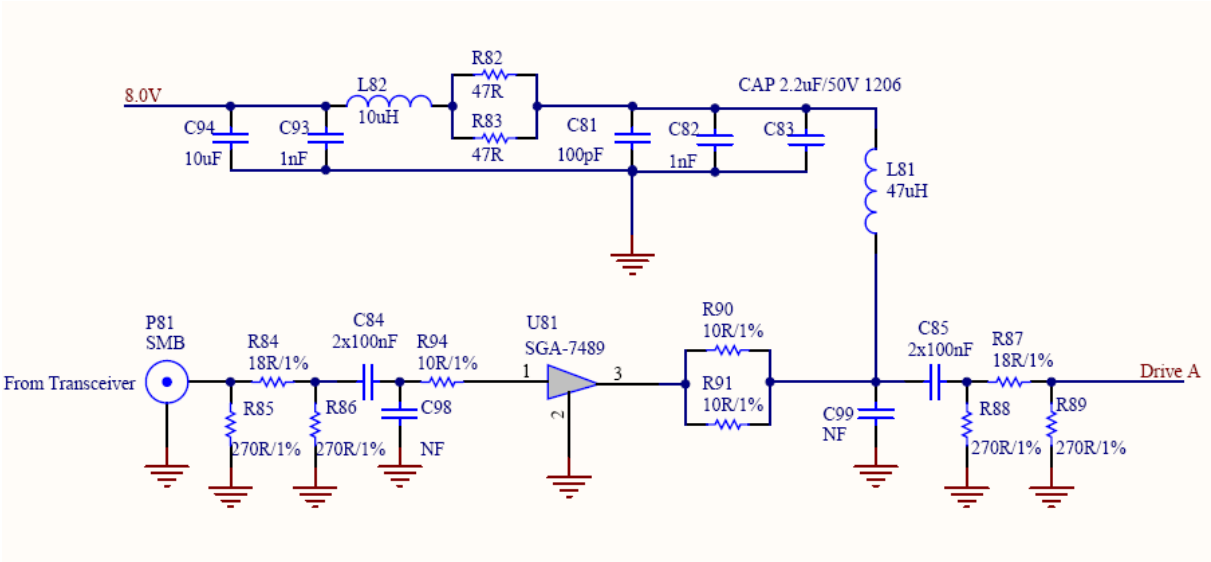


Figure 4.3: Pre-drive stage, 1 of 3 of boost

The above figure shows the pre-drive stage. A Sirenza MMIC, SGA7489 is used. It has a wide operating frequency band (DC-3 GHz), high gain (23 dB) and high output power (Po-1=23 dBm), as well as good input/output return loss. The current is about 105 mA, and the voltage is 5 V. The input attenuator (input ATT) is for improving the impedance match between SGA7489 and signal source of outside (transmitter of Kea). Output ATT is for improving the match between the drive stage and the pre-drive stage. It is also used to adjust the total gain of the HPA. R94, R90 and R91 are used to stabilize this active device. This is known as a damping resistor, which will reduce gain and output power slightly. The coupling capacitors C84 and C85 are for the DC block. Low cut off frequency of boost will depend on their value. L81 is a RF choke. It gives high impedance at the working band and allows DC current through. R82 and R83 are bias resistors, which limit the current and stabilize temperature sensitivity. L82 and the capacitors nearby are for RF decoupling to avoid RF signal leakage to other circuits through the DC path.

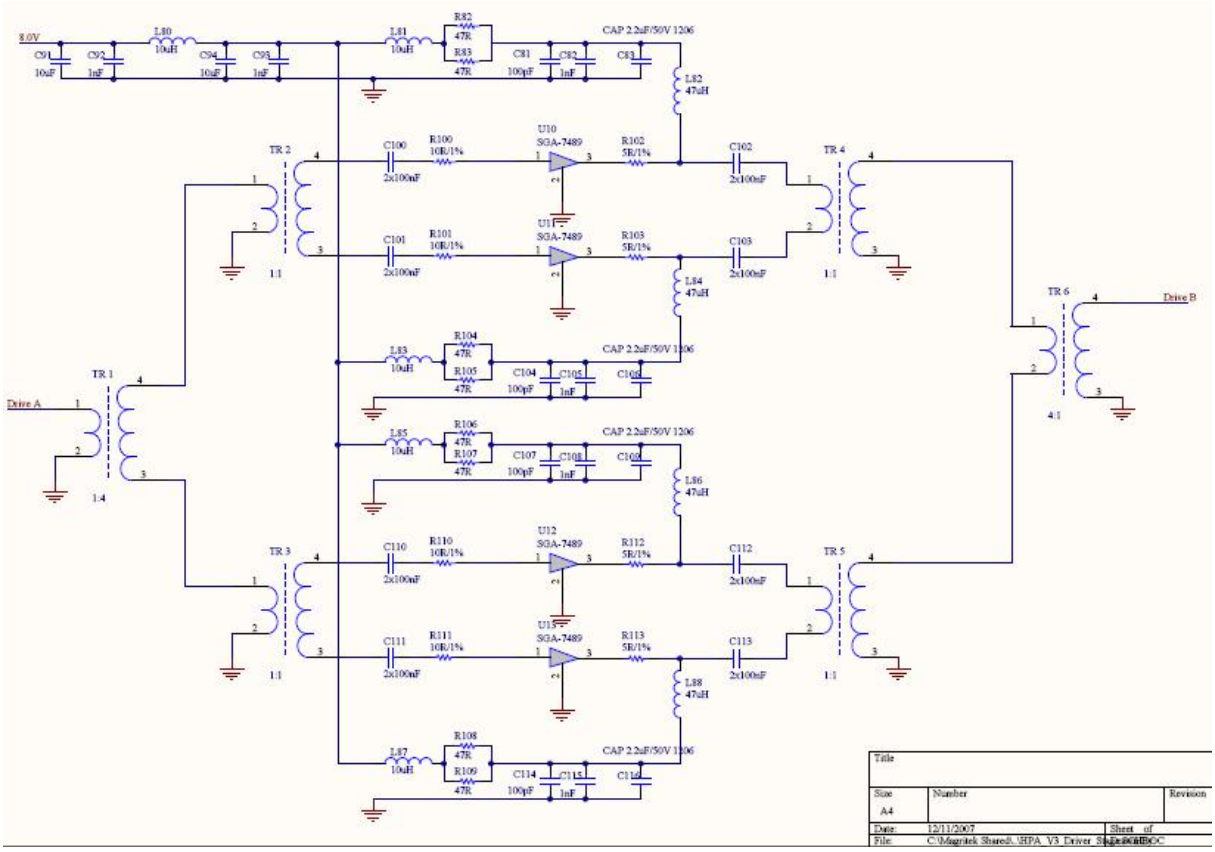


Figure 4.4: Drive stage, 2 of 3 of boost

The figure above shows the drive stage. The basic circuit is the same as the pre-drive stage. To increase output power, four stages are combined together with double push-pull topology. The top two stages and the bottom two stages are combined with push-pull style. Then, they are combined with push-pull style again. In this way, the amplifier will be more stable. There are four 1:1 transformers (TR2, 3, 4, 5). Each one has the same function: balance to single end or single end to balance; two 50 ohm impedance in series to 100 ohm; DC block. TR1 and TR6 are input and output transformers. They are the same module. Impedance ratio is 1:4. It converts 50 ohm of source or load impedance to 200 ohm so that the four stage's impedance can be matched. It has a single end to balance converter function also. In the DC power supply path, more inductors and capacitors are used to avoid any kind of feedback through this path. Power supply voltage is 8 V. Current is 420 mA. The total current included in the pre-stage is 525 mA.

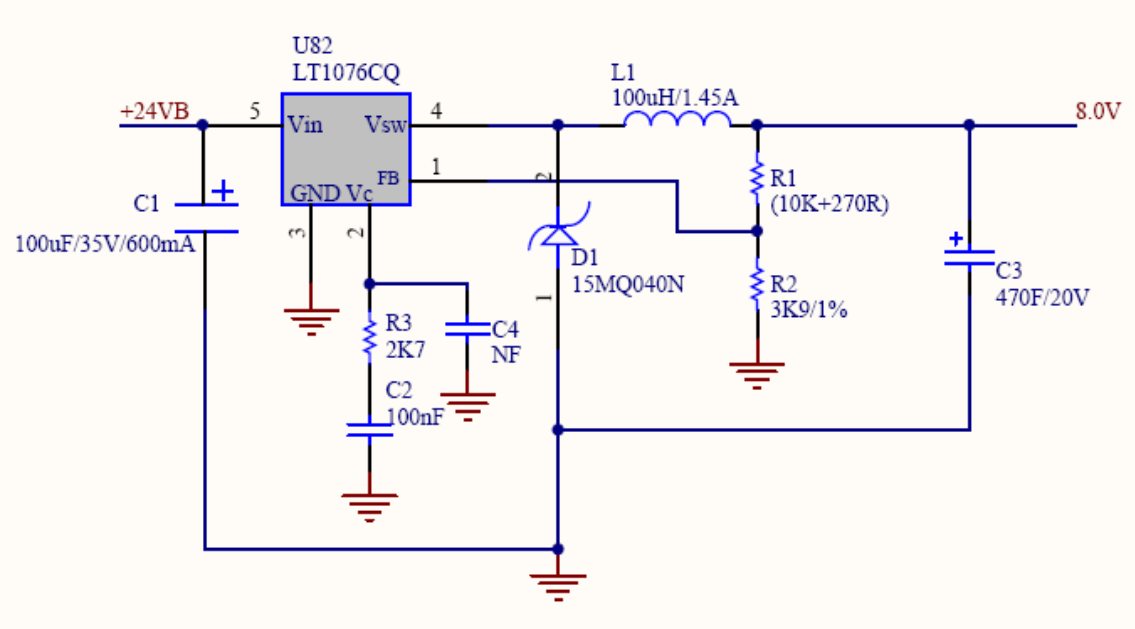


Figure 4.5: DC power supply of boost, 3 of 3 of boost

The figure above shows a switch mode DC-DC converter. It changes 24 V to 8 V for boost. The purpose for using switch mode is efficiency. Switch frequency is about 100 KHz. Ripple of output voltage is about 60 mVpp. This looks high, but it does not affect the NMR experience. Adjust R2 for changing output voltage. Increasing C3 value can reduce ripple.

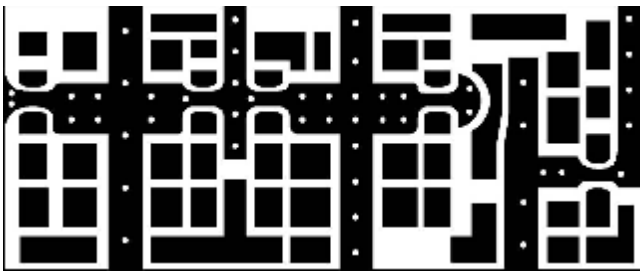


Figure 4.6: Boost PCB Rev2.0, 35 mmX84 mmX1.5 mm, double side copper FR4

The figure above shows the layout of the boost. The number of vias should be enough to get good ground grounding effort. As a guideline, the vias of a nearby active device should be close to the device as possible. The number of vias for the device should be more than 4. The assembled boost is shown in the Figure 4.7.

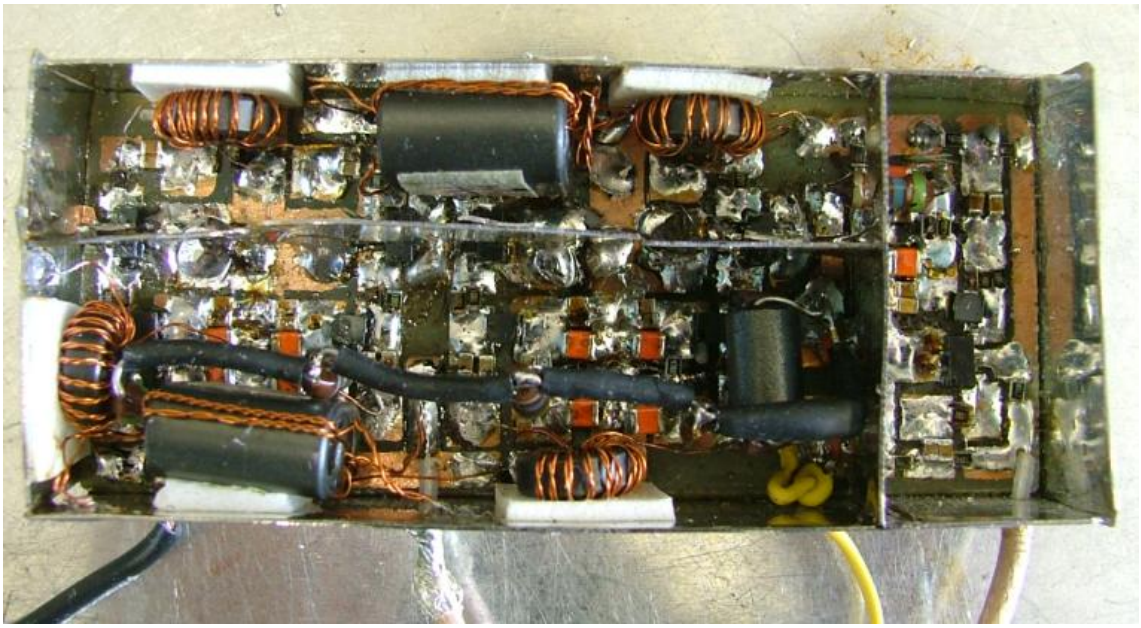


Figure 4.7: Boost rev2.0, 85 mmX36 mmX18 mm

4.3.3 DC operating voltage

After assembly, the DC voltage of the circuit is tested to make sure it is working well. The current is calculated according to the bias resistor, series resistor of the inductors and voltage at the output pin of the device. The goal is to keep the current at 105 mA at each stage. The Table 4.1 shows the results. The current of each stage is very similar.

Table 4.1: DC operating voltage

Idq (mA)				Voltage (V)			Resister (ohm)					Notice
Real	Specification											
	Min	Typ	Max	Vin	Vout	PS	R103	SRL1	R101	R104	SRL22	
Pre-drive:												
100	103	115	127	1.64	4.84	8.00	5	2.6	47	47	0.4	
Drive:												
103	103	115	127	1.62	4.76	8.00	5	2.6	47	47	0.4	1#
105	103	115	127	1.59	4.68	8.00	5	2.6	47	47	0.4	2#
103	103	115	127	1.62	4.75	8.00	5	2.6	47	47	0.4	3#
103	103	115	127	1.63	4.77	8.00	5	2.6	47	47	0.4	4#
Delt				0.04	0.09	0.00	5	2.6	47	47	0.4	
514	SUM											
520	SUM	Current reading form PS of MP-3087										
8.1	V	Voltage reading from PS of MP-3087										
Test is under cold temperature 5.2 ohm for 100UH inductor; 2.6 ohm for 47uH inductor. Goal: keep Idq at 108mA. PS will change from 7.9V to 8.1V. Interface of test PS voltage is at PS port of boost Test under no RF signal, In/out port are 50 ohm												

The vias are very important! Each device should have 4 vias, two for each side. If you find the voltage is lower than 4.3 V whether terminated with 50 ohm, open end or changing device, it is a result of oscillation due to lack of vias.

In summary, the DC operating voltage is satisfactory.

4.3.4 Test gain

The definition of gain is;

$$G = 20LOG(\frac{V_o}{V_i}) \quad \textbf{(4.1)}$$

Where Vo is output voltage on 50 ohm load; Vi is input voltage on 50 ohm load.

The test setting is shown in the figure below. To reduce the dynamic range of the test system, a 30 dB ATT is followed with DUT of 37 dB gain. To get the net gain of the DUT, the testing gain should add 30 dB. To get Vi, the Through module replaces the DUT plus 30 dB. To get Vo, DUT plus 30 dB is used.

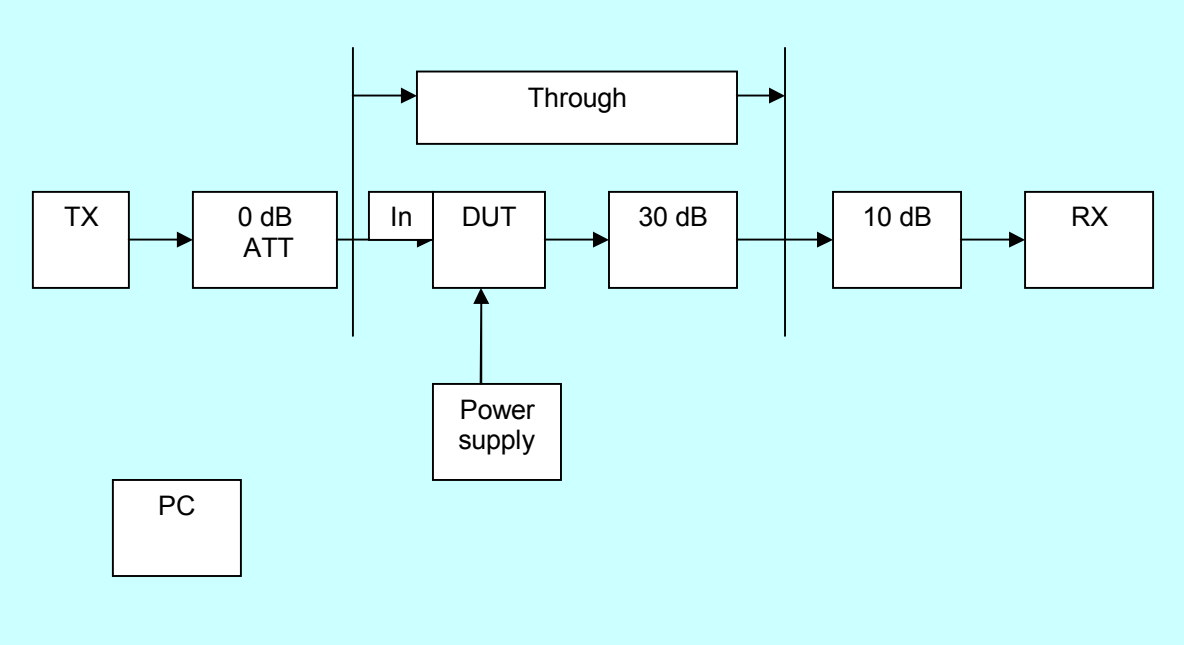


Figure 4.8: DUT and system setting for testing gain

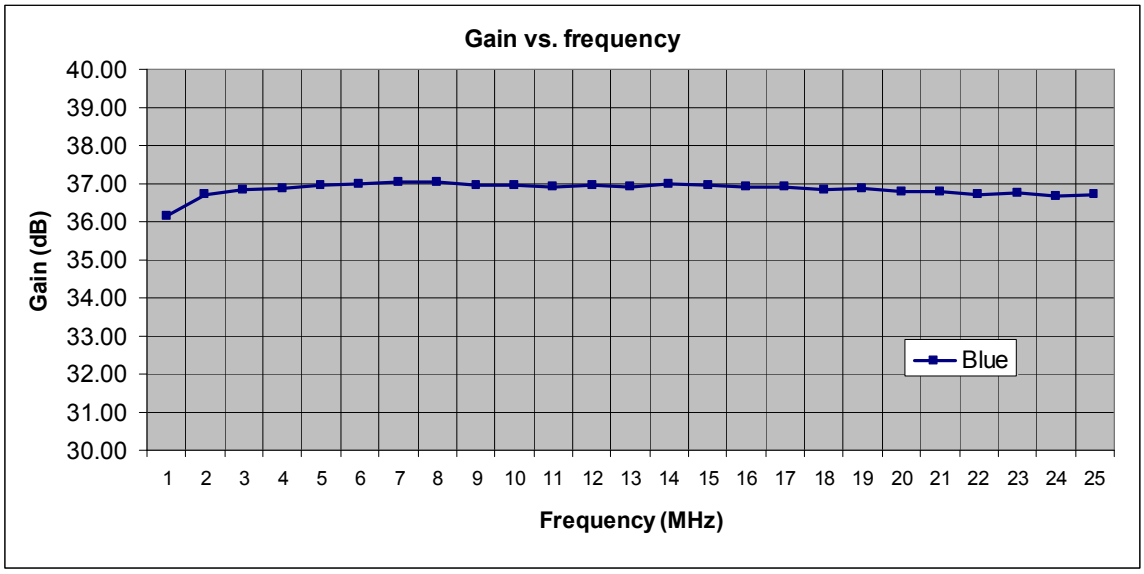


Figure 4.9: Gain at Pi=-60dBm

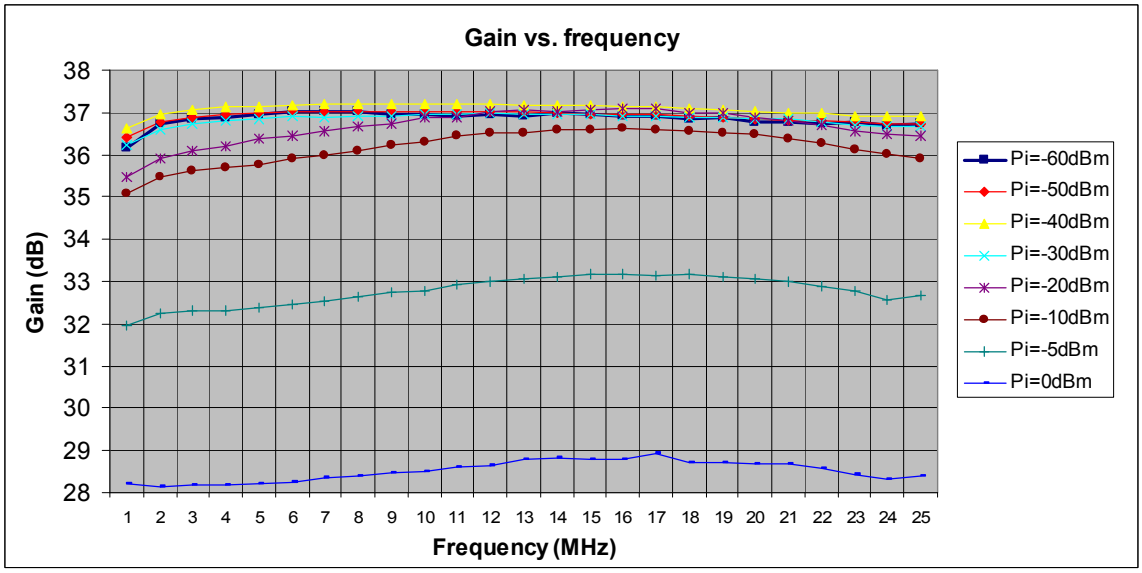


Figure 4.10: Gain with different Pi level

The two figures above show:

- Small signal gain is 37 dB. This is as expected.
- Gain is very flat at low power level, only 1db difference across 1 to 30 MHz.
- Gain flatness is still good while input power changes from -60dBm to 0dBm, max difference is only about 2 dB across the band.
- When input power reaches -10 dBm, DUT starts to saturate. Saturation is better at the middle band than at both side bands. Input 1 dB compression power is -10 dBm at 8 MHz.
- There is 8.5 dB gain compression at 8 MHz while input power is 0 dBm. Its output power is Po = G + Pi = 28.5 + 0 = 28.5 dBm. This is max saturation power.

- The DUT is robust with overdrive in conditions of 50 ohm load.
- The DUT is thermally stable even if it is hot (60-70C degree) after running several hours.
- If the DUT is hot, current is increased a little; output power is dropped a little; gain is dropped a little. But it doesn't affect overall performance.
- In summary, the boost's gain is very good.

4.3.5 Test waveform

Once gain is tested, we want to know the waveform of the output voltage at different power levels and different frequencies. The test diagram is shown below. A 40 dB ATT works as a 50 ohm load and attenuator.

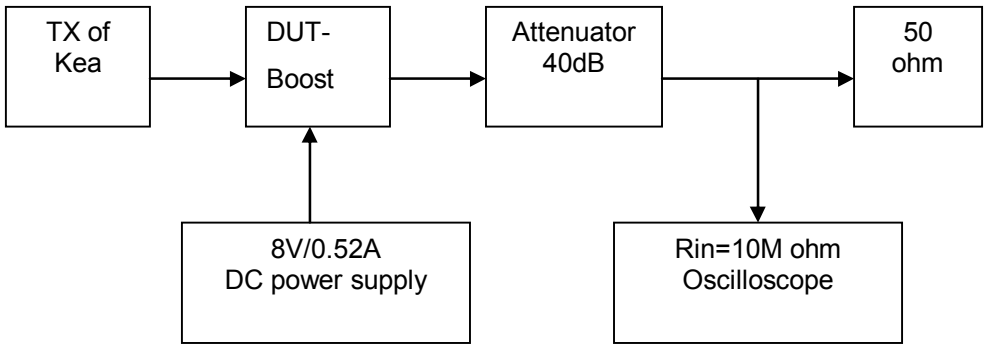


Figure 4.11: Test setting with 50 ohm load

The three figures below show the RF waveform at different power levels and frequencies.

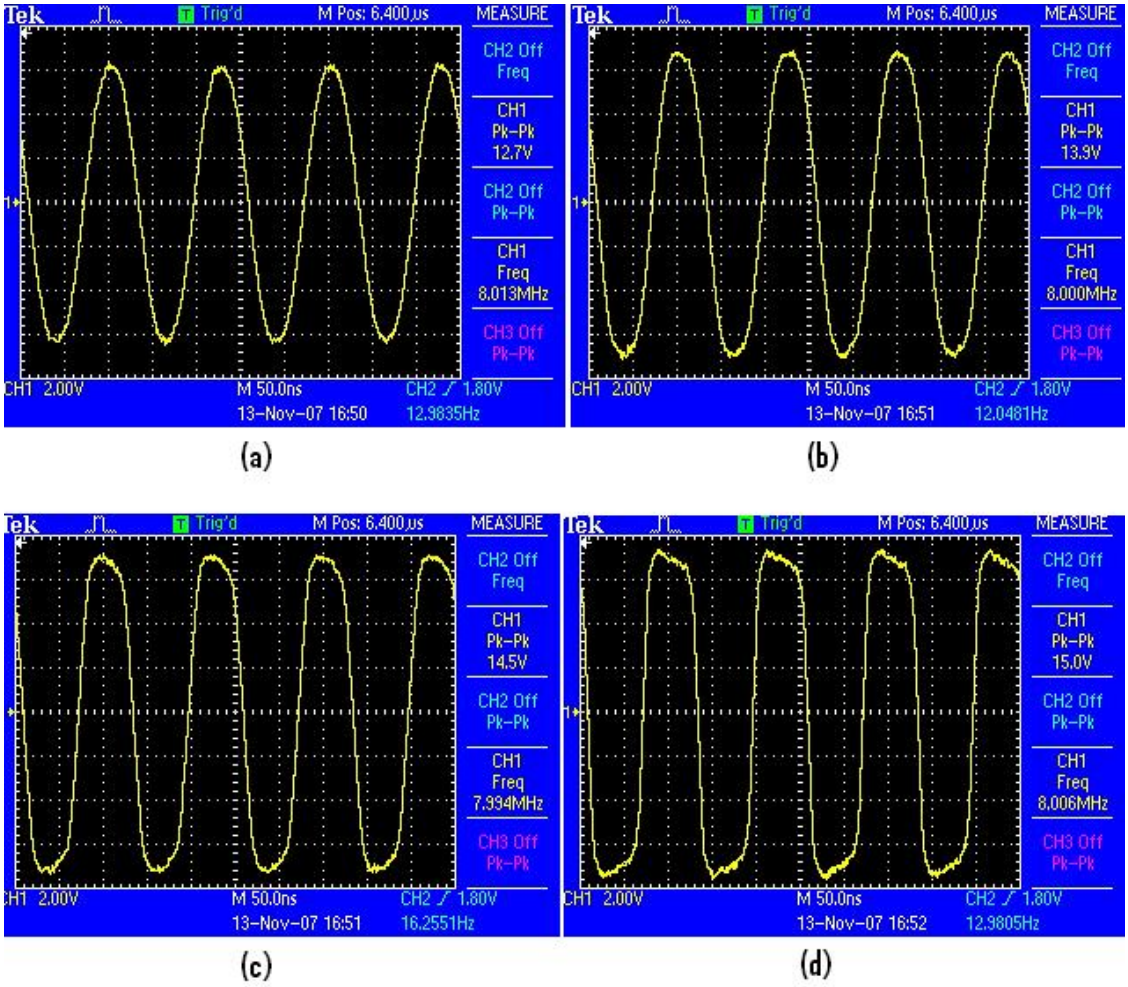


Figure 4.12: Vo on 50 ohm of Boost Rev2.0 at 8 MHz, (a) Pi=-10 dBm, (b) Pi=-8 dBm, (c) Pi=-5 dBm, (d) Pi=0 dBm

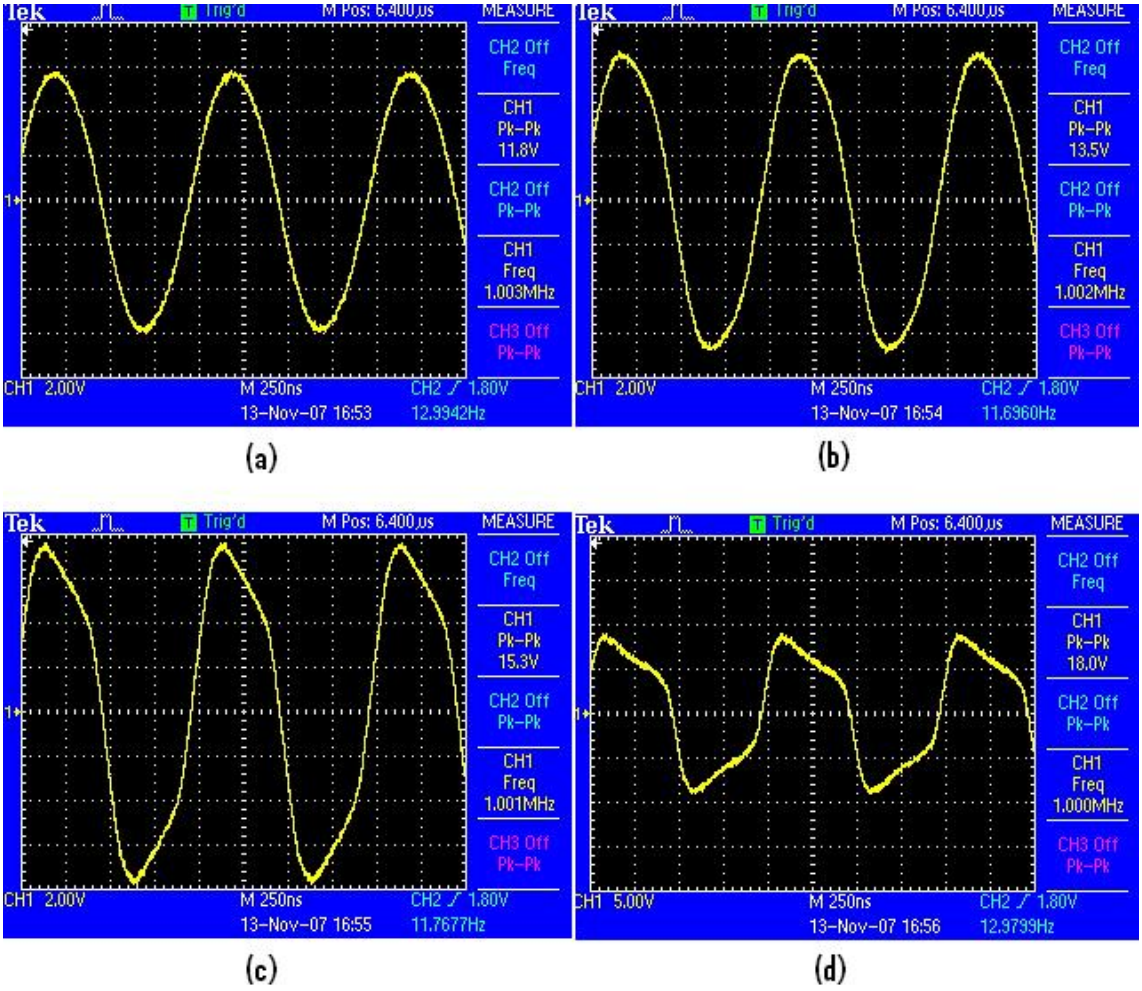


Figure 4.13: Vo on 50 ohm of Boost Rev2.0 at 1MHz, (a) Pi=-10 dBm, (b) Pi=-8 dBm, (c) Pi=-5 dBm, (d) Pi=0 dBm

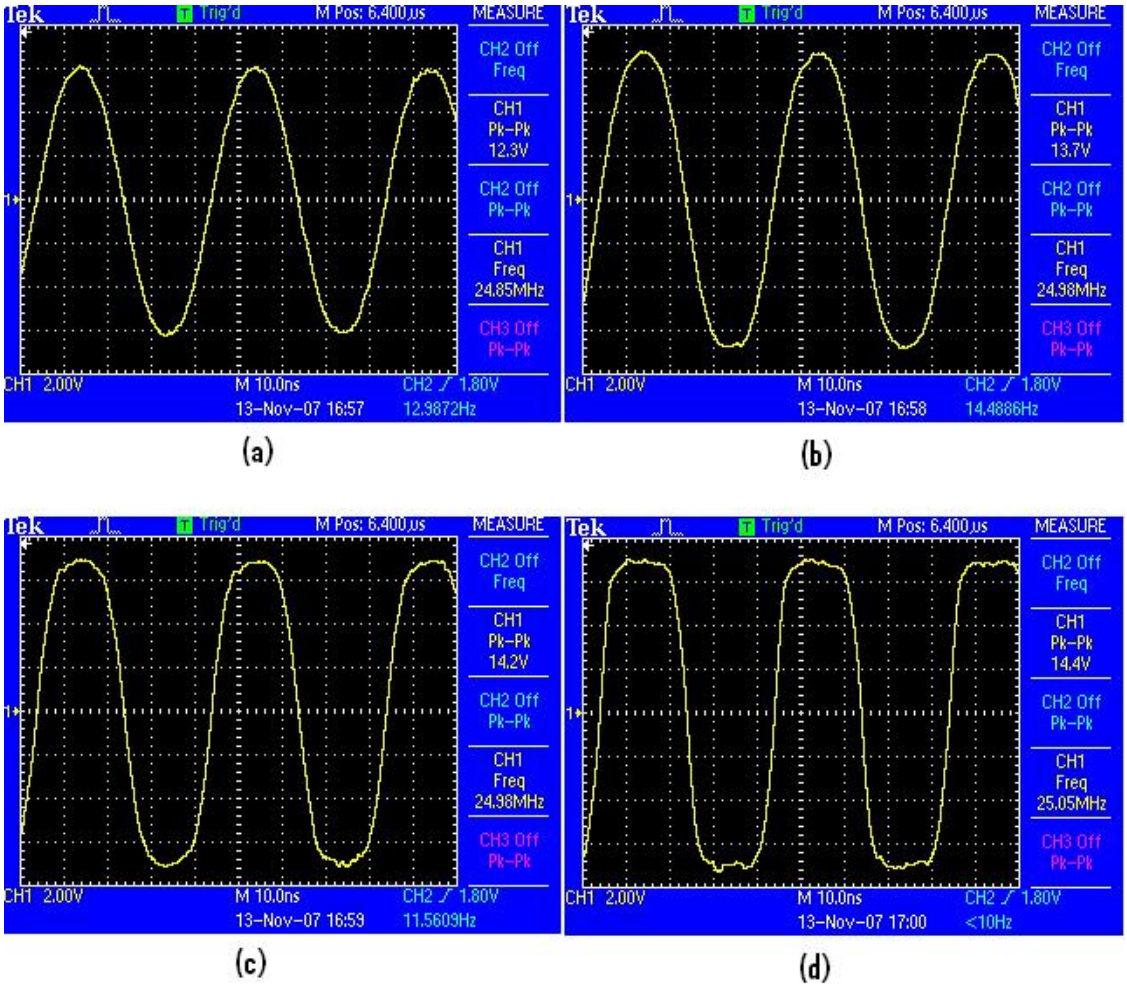


Figure 4.14: Vo on 50 ohm of Boost Rev2.0 at 25 MHz, (a) Pi=-10 dBm, (b) Pi=-8 dBm, (c) Pi=-5 dBm, (d) Pi=0 dBm

From the three figures shown above, the following can be concluded:

- Waveform is sinusoidal when input power level is less than -8 dBm.
- Waveform starts saturation when input power is over -8 dBm. Po-1 is about -8 dBm.
- Output voltage is maximum value, 13.9 Vpp, at the middle of the band (8 MHz). At both sides of the band, 1 MHz and 25 MHz, output voltage is about 13.6 Vpp.
- There is no damage on the boost when input power is overdriving boost. Maximum input power is more than 0 dBm. It is limited by maximum output power of the test system.
- Waveform is as expected.
- Next, we want to know about the envelope of the RF pulse. The ideal is a square wave. Testing is at different frequencies and different input power levels. These are shown in the two figures below.

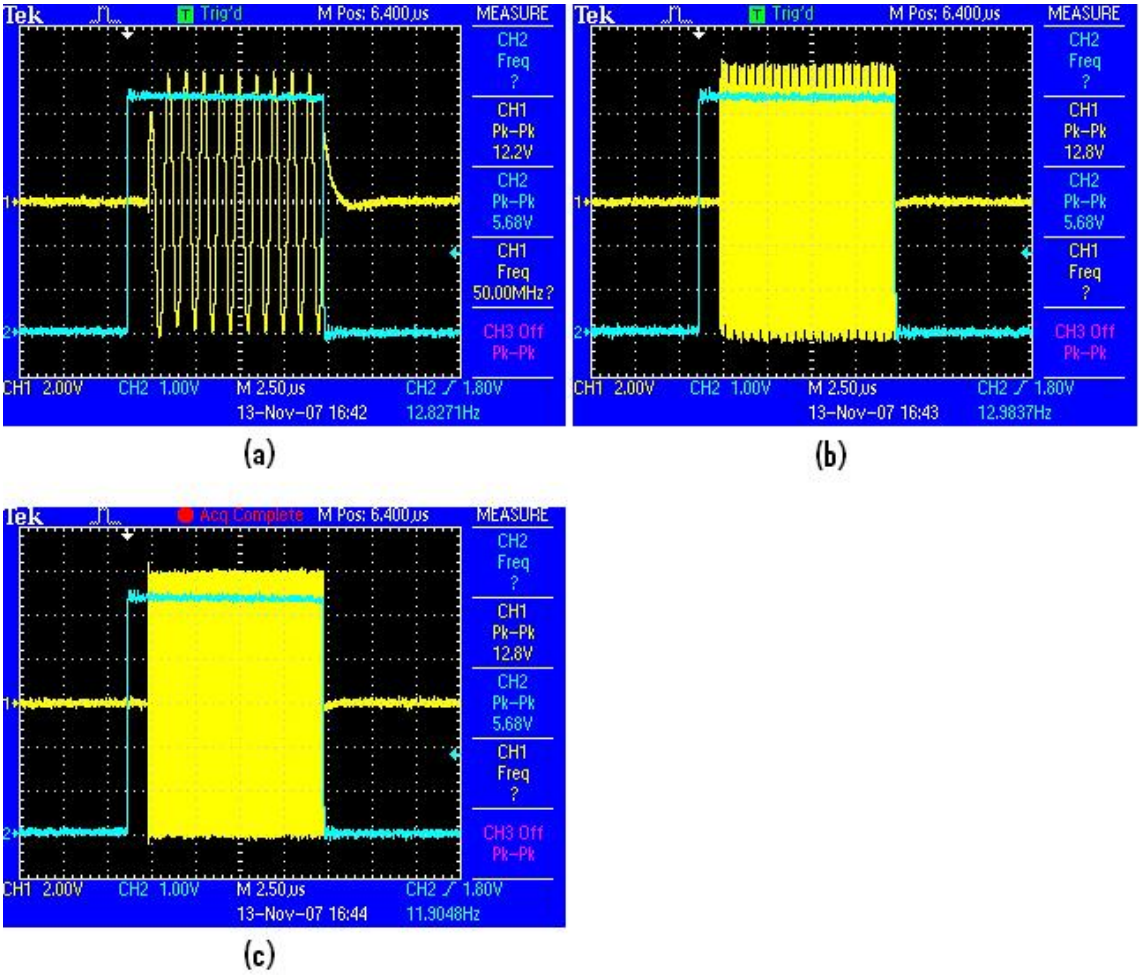


Figure 4.15: Waveform of Vo (ch1) on 50 ohm at Pi=-10 dBm, Gate blanking (ch2), (a) 1 MHz, (b) 8 MHz, (c) 25 MHz

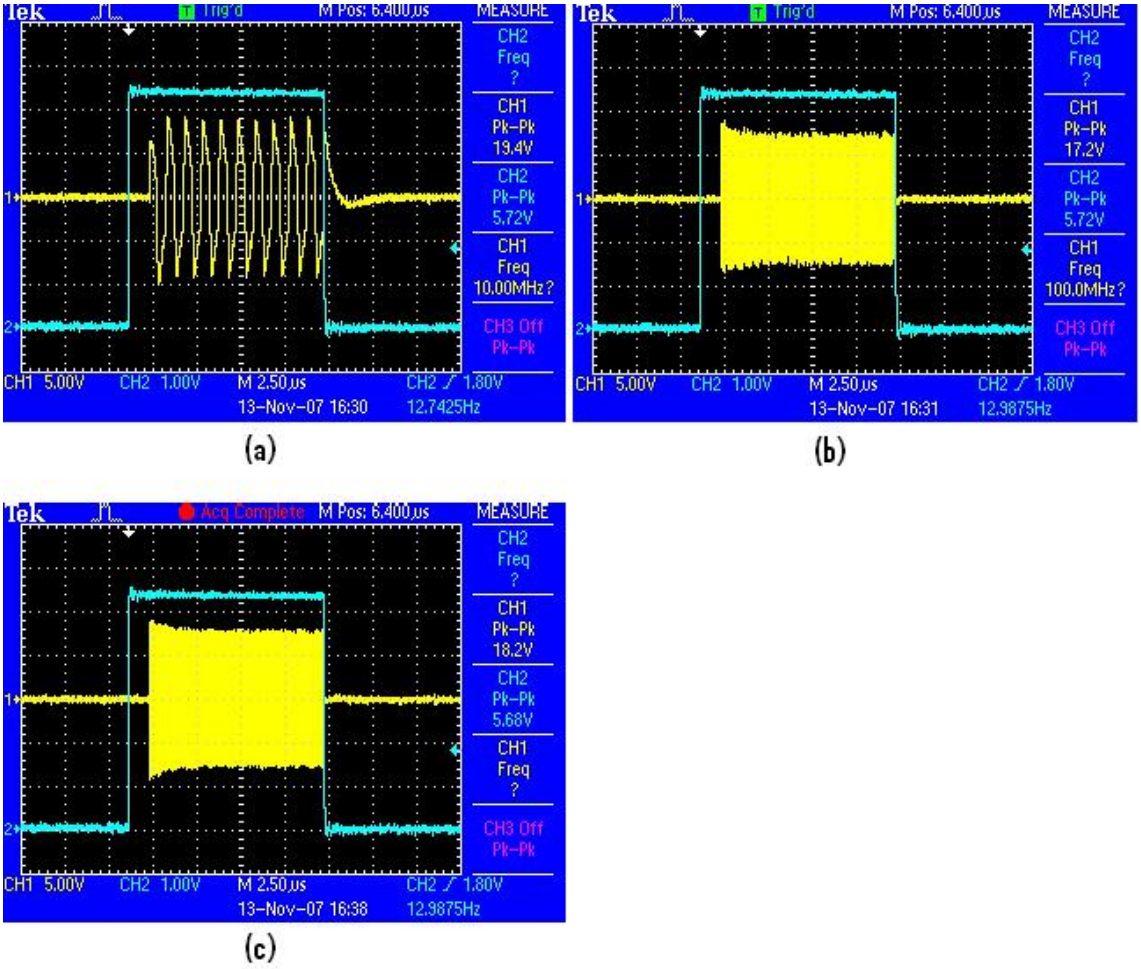


Figure 4.16: Waveform of Vo (ch1) on 50 ohm at Pi=0 dBm, Gate blanking (ch2), (a) 1 MHz, (b) 8 MHz, (c) 25 MHz

The test results above show:

- The envelope of the RF pulse is constant when frequency is changed.
- If input power is in the linear zone of boost, say -10 dBm, the envelope is an ideal square wave. If input power is in the nonlinear zone of boost, say 0 dBm, the envelope is not an ideal square wave. The amplitude is higher at the beginning of the RF pulse.
- There is no spike.

The figure below shows the detail of the waveform near the rising edge: no spike is observed.

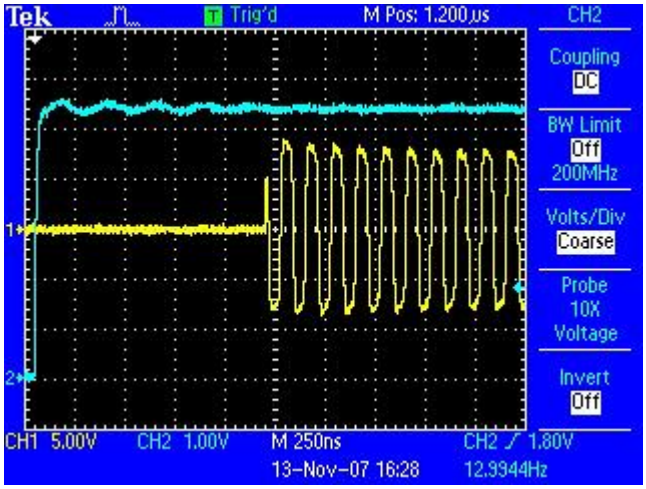


Figure 4.17: Rise edge of Vo (ch1) at 8 MHz and Pi=0 dBm, gate blanking (ch2)

On 50 ohm load, max output power is 27.5 dBm (0.56 W) at 8 MHz. This was as expected from the design.

4.3.6 Test of linearity of DUT

The performance on linearity of the DUT is measured by the curve of output power vs. input power. The ideal characteristics need to be a straight line. In practice, output power will stop increasing while input power is very high. The test procedure is to measure the output voltage while input voltage sweeps from a lower to higher level. Kea NMR spectrometer can be used as a scale network analysis to carry out this duty. Software called Amplitude sweep in Prospa has been used. To get accurate data, input and output power should be calibrated by oscilloscope. Test data is saved to a Test Template, boost linear, for further processing, analysis, displaying and storage.

Test procedure:

- Test system: Kea with Receiver, transceiver (TX and RX), controller and power supply. In this document we will refer to 'receiver +RX' as RX.
- Test software: Prospa R2.2.3
- PC with MW and Prospa.
- Connect the DUT with the test system
- Choose the test frequency
- Open the test software: Amplitude sweep. Set the step size at 100 points.
- Try to test linearity (Po vs. Pi, Gain vs. pi) of the DUT, adjust max Pi sweep level until the ratio of linear zone to non-linear is about 70% to 30% at Pi domain, or until Pi reaches its maximum level. Record the max Pi. It will be used in test below.
- Check the test system linearity without the DUT in condition of signal margin larger than 0 dB. The definition of signal margin is the difference of Via and Vib, where Via is the input signal of the receiver without the DUT, Vib is the input signal of the receiver with the DUT. Sweep to above max Pi. Adjust the Gain of receiver, input signal of the

receiver and output signal of TX to allow the test system to be linear. Save data (name L) to Test Template

- Calibrate max Vi (mVpp) at max Pi with One pulse of Prospa. Save the data to Test Template
- Set this max Vi (mVop) in software of Amplitude sweep
- Test linearity of the DUT. Set max Vi calibrated in the software before test. Save data (name L) to Test Template
- Calibrate Vo at max Pi with One pulse of Prospa. Save it to Test Template
- Test the waveform at max Pi. Choose a suitable waveform factor. Save them to the Test Template.
- Analyze the DUT linear performance. Get Po-1 data
- Repeat the steps above from 4 to 14 for other frequencies.
- Save the Test Template as the name of the DUT.
- Below is an example of a test order of term matrix for 3 frequencies. It is easy to track the test procedure if use this matrix.

Table 4.2: Test order and term matrix

Order	Term and order	Unit	2MHz	8MHz	25MHz	Notice
1	Try test DUT, linery zone	%	70	70	70	
2	Max Pi (TX=)	dBm	-5	-5	-5	
3	Check system linear		Pass	Pass	Pass	
4	Cal Vi	mVpp	364	372	358	
5	Set max Vi at SW	mVop	182	372	358	
6	Test DUT linear, Po-1	dBm	27.4	27.8	27.8	
7	Cal Vo	Vpp	15.1	14.3	14.2	
8	Record Vo waveform		19:12	19:21	19:34	13-Nov-07
9	Vo waveform factor		1.08	1,2	1.2	

The test block diagrams are shown below. The DUT means device under test. In this case the device is the boost. The signal margin is: SM=Via-Vib=40 dB-37 dB=3 dB.

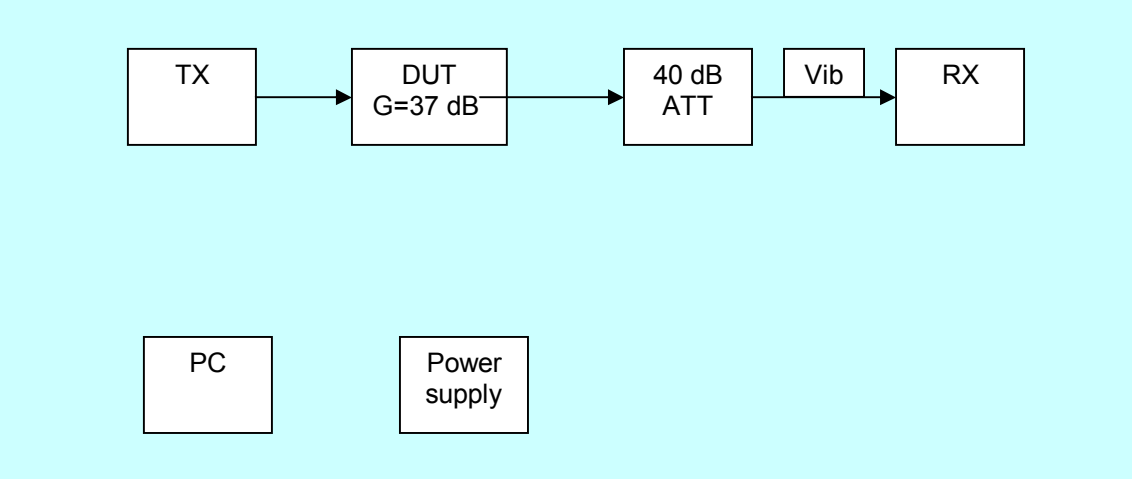


Figure 4.18: Test DUT linear

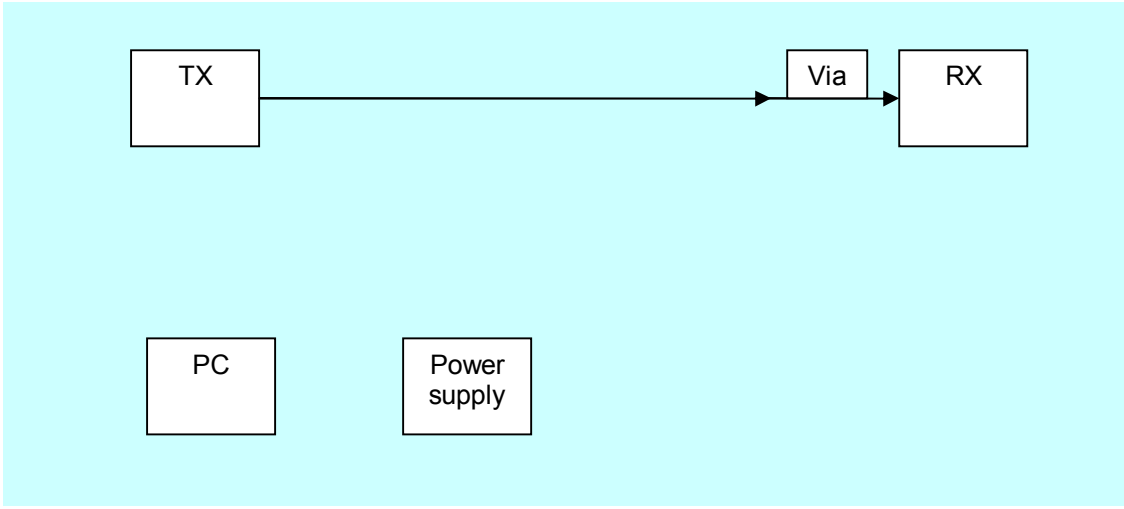


Figure 4.19: Check test system linear

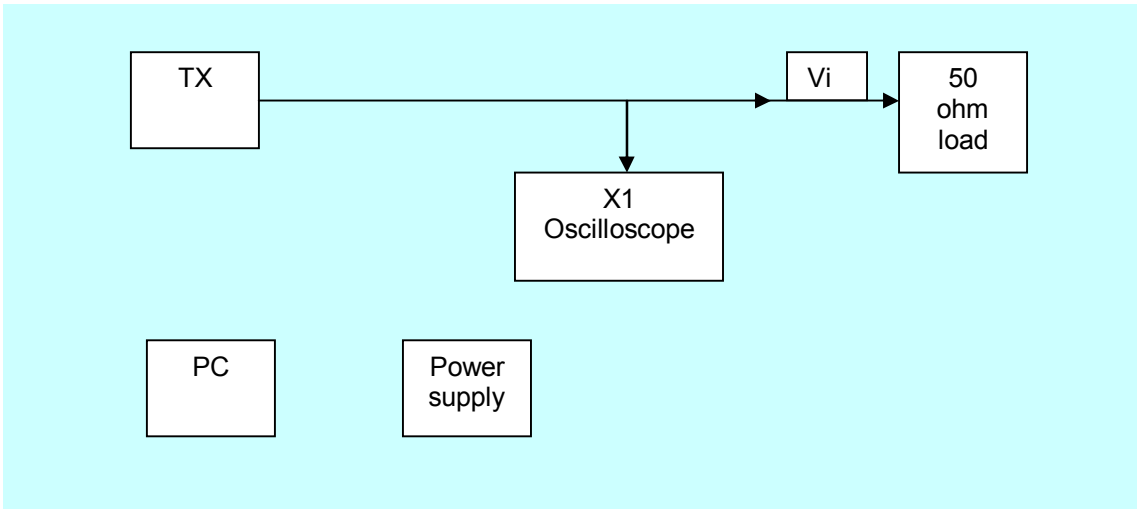


Figure 4.20: Calibration Vi

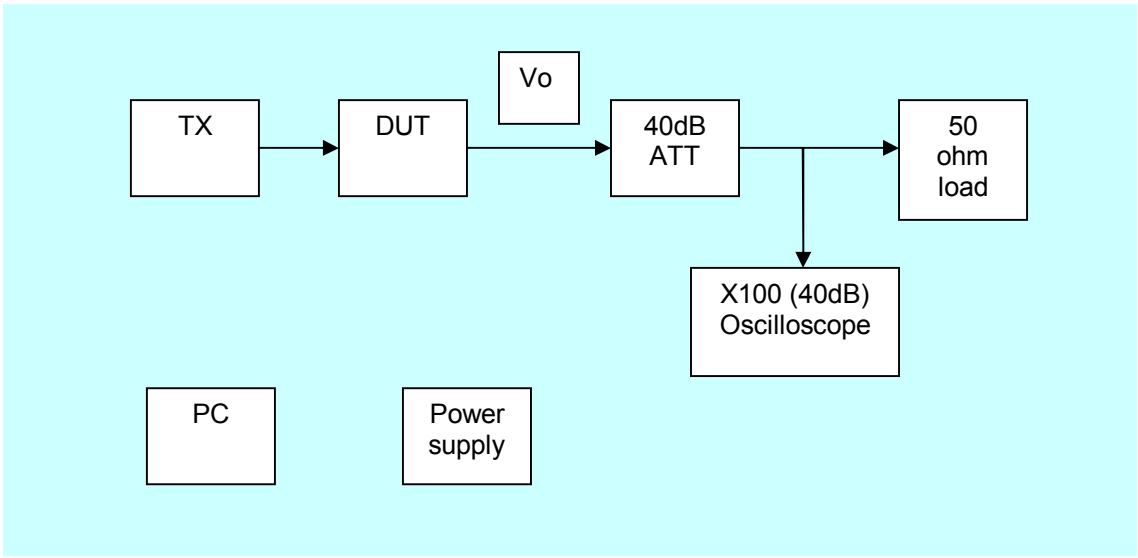


Figure 4.21: Calibration output voltage

Start the test at 8 MHz. The figure below shows that the test system is linear.

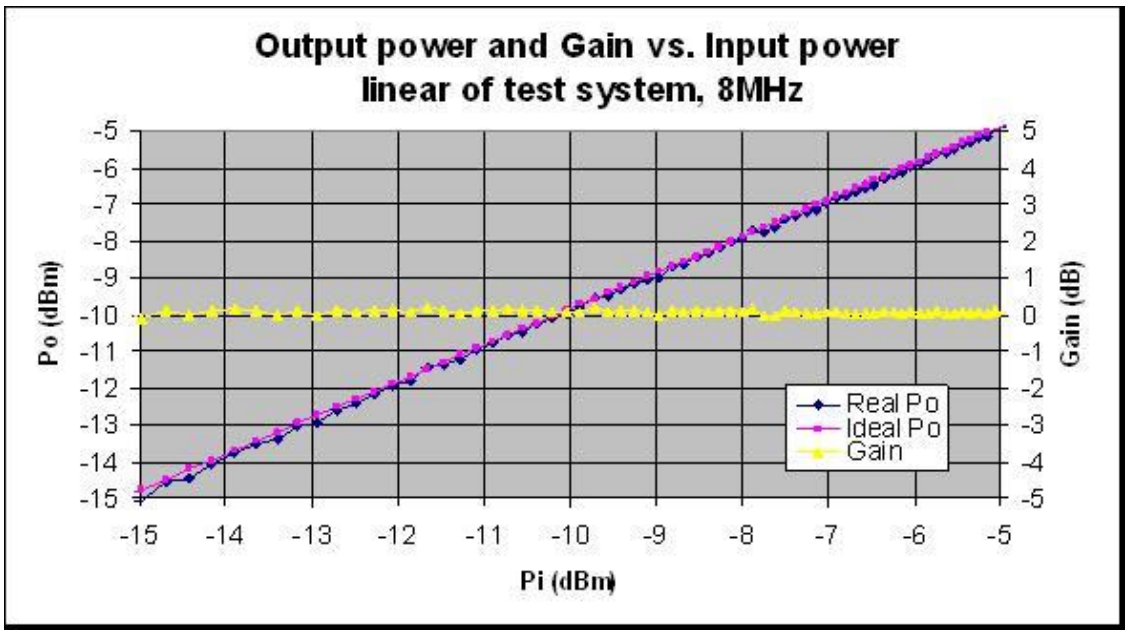


Figure 4.22: Check test system linear at 8 MHz

The figure below shows that Po-1 of the DUT is 28 dBm at 8 MHz.

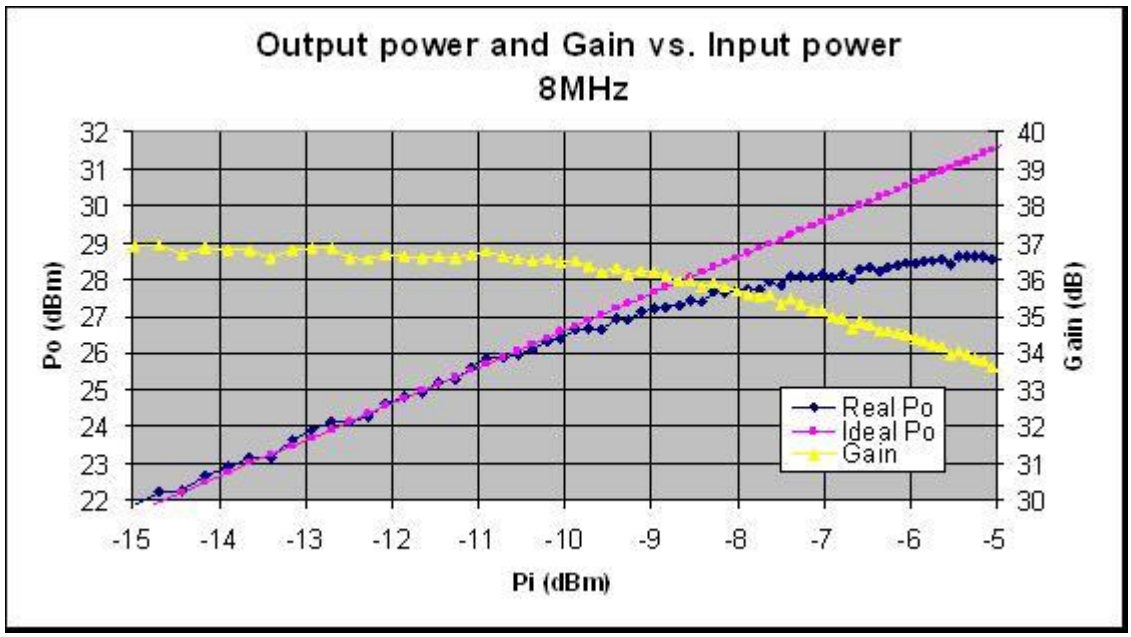


Figure 4.23: DUT linear at 8 MHz, Po-1=28 dBm

The figure below shows that the waveform is still good at max Pi-=-5 dBm, even if there is some saturation.

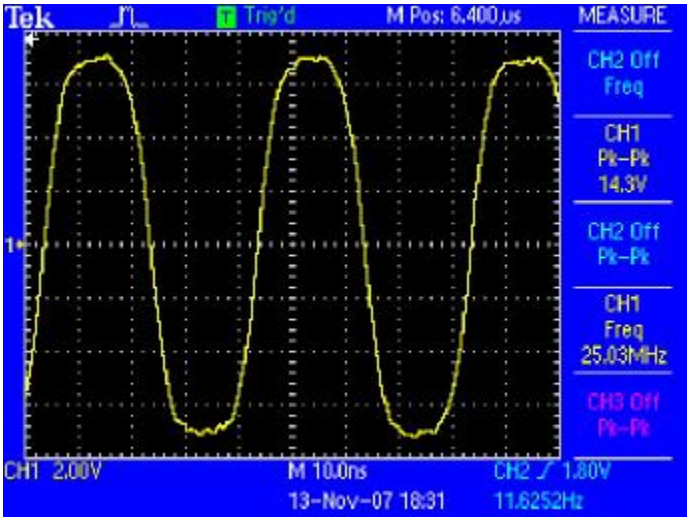


Figure 4.24: Output voltage waveform at 8 MHz and Pi=-5 dBm

In the same way, linearity and waveform of the output voltage at 2 MHz and 25 MHz are tested. Table 4.3 is a summary of the figures above.

Table 4.3: Po-1 and Gain summary

Terms	Unit	2MHz	8MHz	25MHz	Notice
Po-1	dBm	27.4	27.8	27.8	
G	dBm	36	36.7	37	
G-1	dBm	35	35.7	36	

Conclusion: Po-1 is as expected; Gain is as expected; Frequency response of gain and Po-1 is flat; These are very good results. The test setting is shown in the figure below.

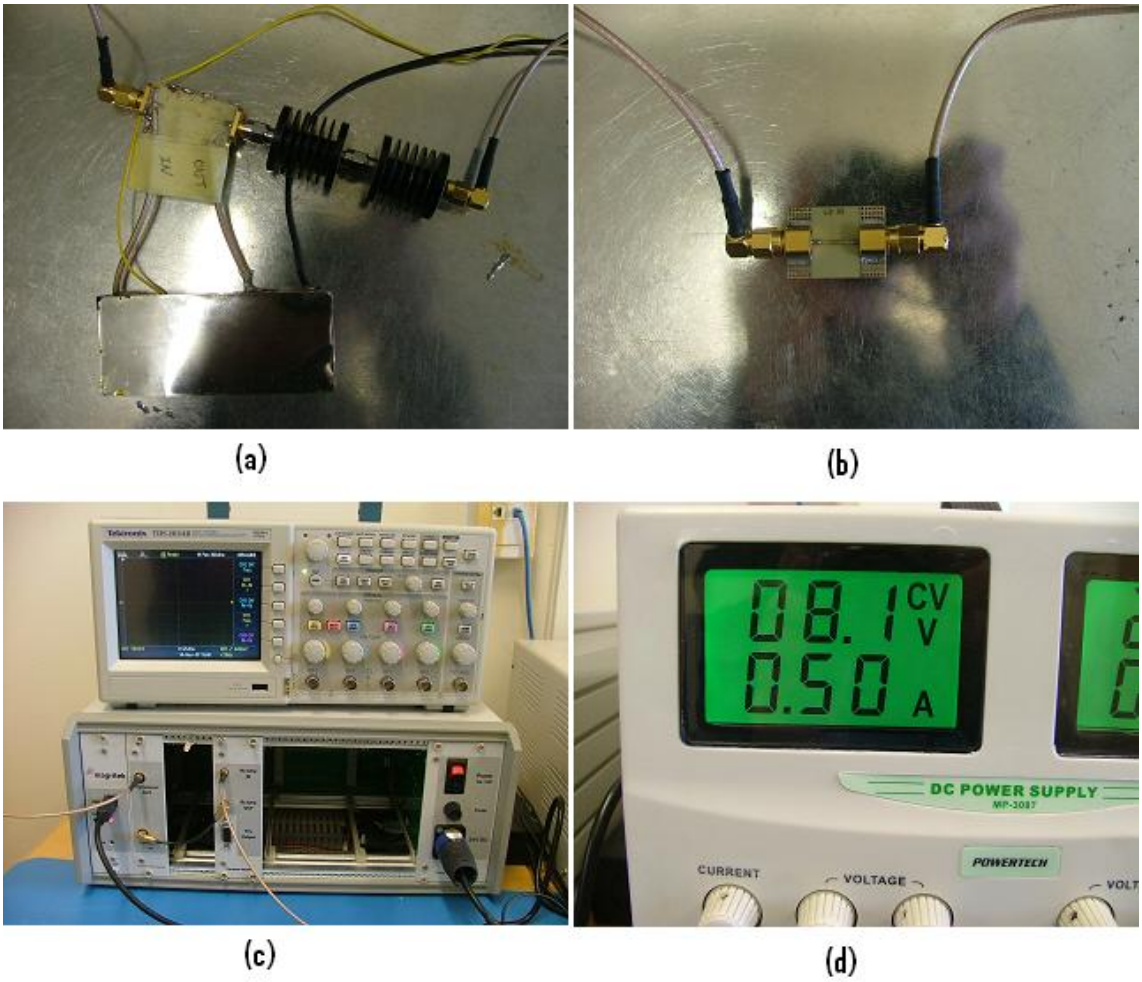


Figure 4.25: (a) DUT and 40 dB ATT, (b) Calibration input voltage, (c) Kea and Oscilloscope, (d) DC power supply and reading

4.3.7 VSWR of DUT

VSWR is a measurement of matching conditions between outside termination and the relative port of the DUT. Input VSWR is for the input port of the DUT. Output VSWR is for output port of the DUT. In practice, a Double Directional Coupler (DDC) is used to test VSWR. From it, forward voltage, fwd or Vf, and reverse voltage, rev or Vr, can been found. VSWR is;

$$S_{11} = \frac{V_r}{V_f} \tag{4.2}$$

$$inputVSWR = \frac{1 + S_{11}}{1 - S_{11}} \tag{4.3}$$

$$S_{22} = \frac{V_r}{V_f} \tag{4.4}$$

$$outputVSWR = \frac{1+S_{22}}{1-S_{22}} \quad \textbf{(4.5)}$$

Where S11 is the input reflection coefficient and S22 is the output reflection coefficient.

The test settings are shown in two figures below. ATT is an attenuator. TX and RX are part of Kea.

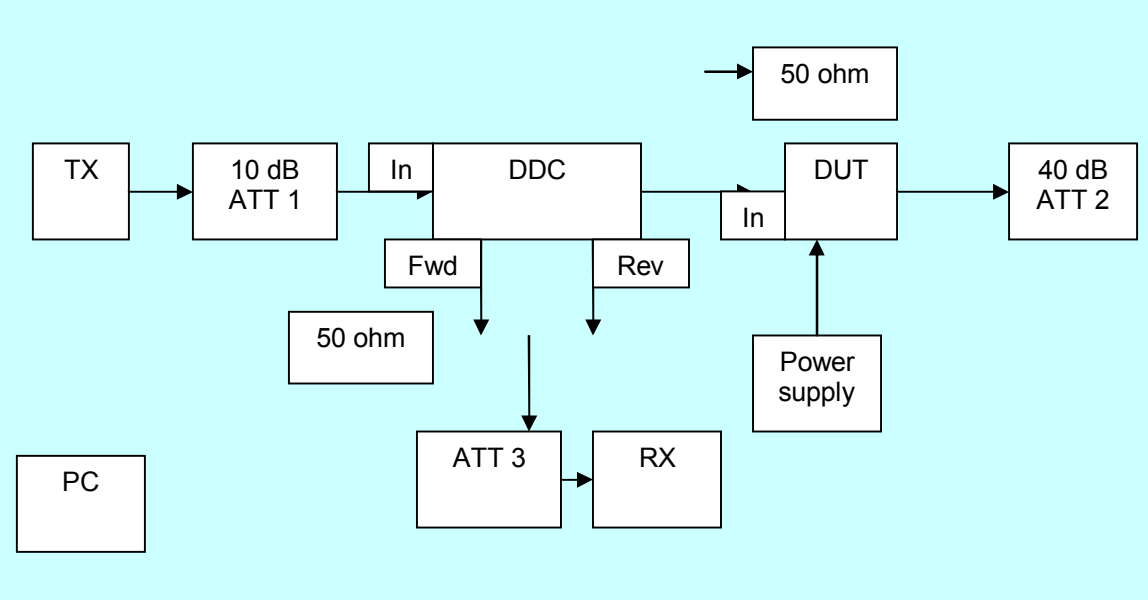


Figure 4.26: Test setting of input VSWR of DUT

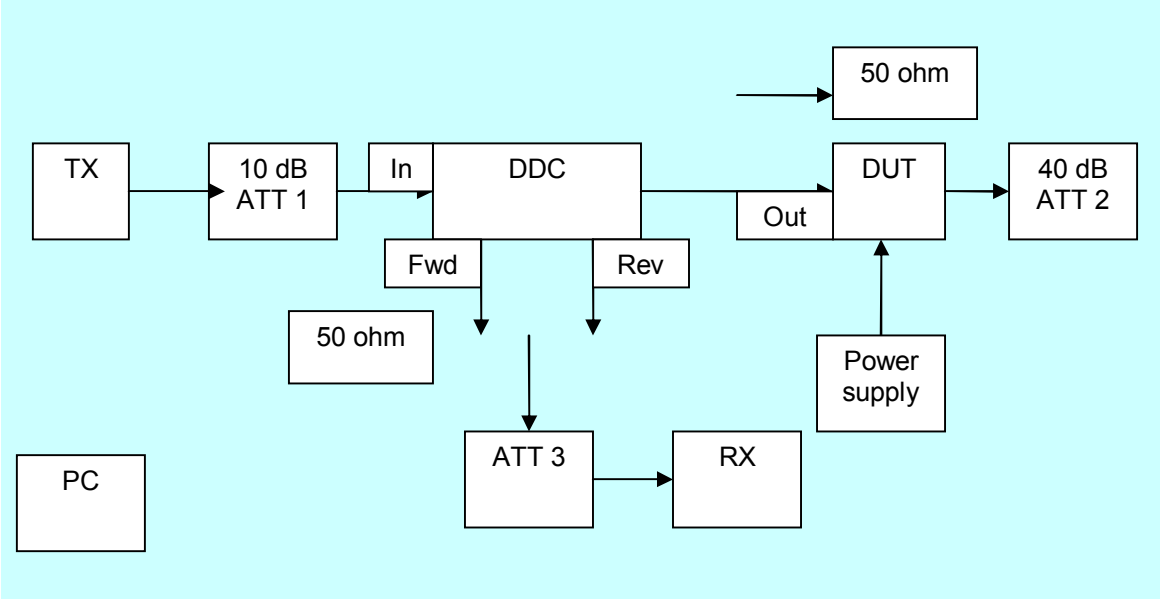


Figure 4.27: Test setting of output VSWR

Test procedure:

- Connect the DUT with the test system
- To test input VSWR, the input of the DUT is connected with the out of the DDC.
- Choose a suitable input power
- Connect the input of RX with the Fwd port of the DDC
- Open Amplitude sweep of Prospa

- Check if the test system is linear
- Adjust the gain of the receiver of Kea and ATT 3 until the test system is linear
- Connect the input of ATT 3 with Rev port of the DDC
- Check the signal level, which should be 10 dB higher than noise level. Connect the input of ATT3 to 50 ohm to test the noise level.
- Adjust the gain of the receiver of Kea and ATT3 until the above criteria are met.
- Connect the input of ATT3 to the fwd port to test Vf.
- Connect the input of ATT3 to the rev port to test Vf.
- Save Vf and Vr to the Test Template
- Remove the DUT from the output port of the DDC and put 50 ohm on it
- Repeat step 11 to step 13 to test VSWR with 50 ohm
- To test the output VSWR, connect the output of the DUT to the output of the DDC. Repeat steps 3 to 15.
- Test results are shown in the figures below. They are very good even if output VSWR is slightly higher at low frequency. This will be considered later.

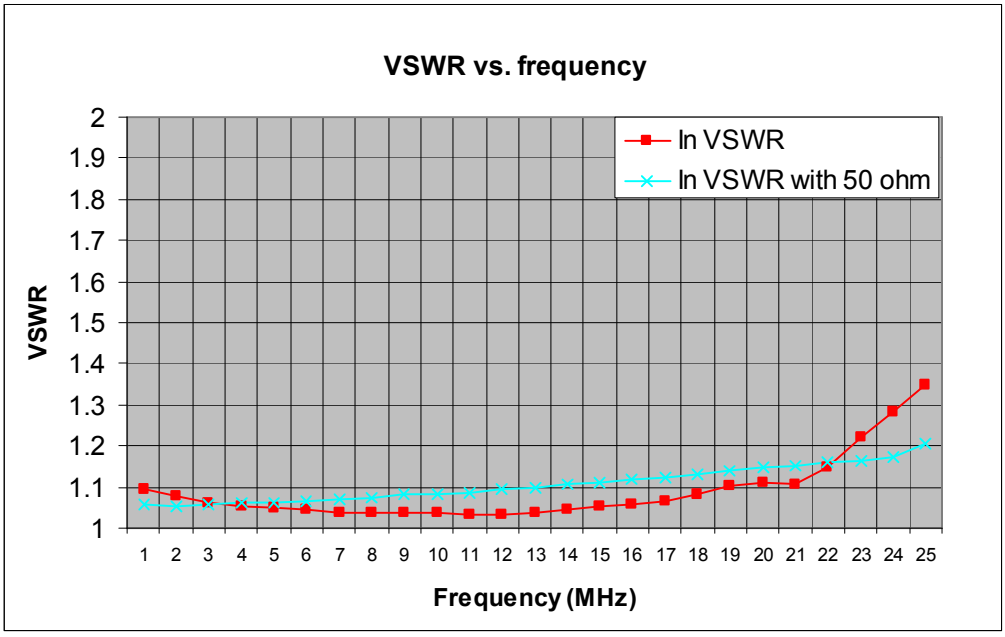


Figure 4.28: Input VSWR of DUT

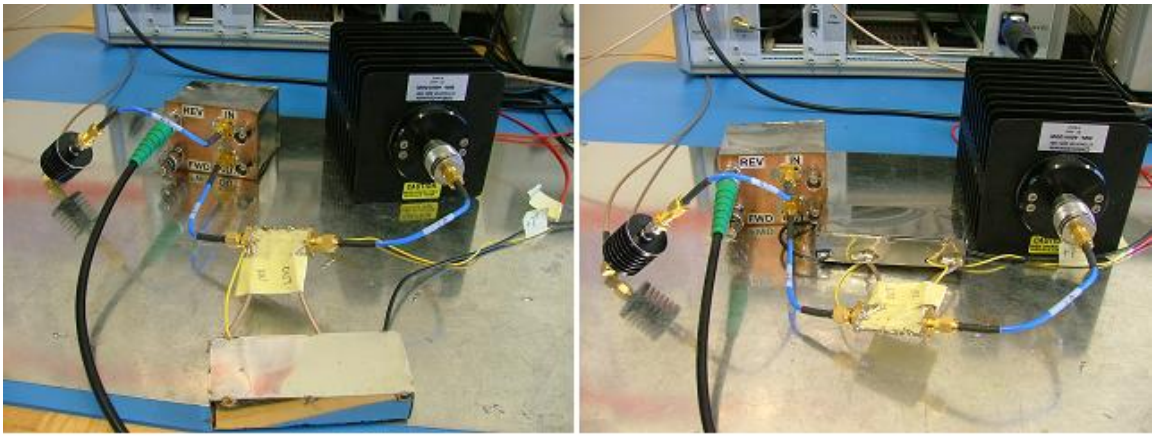


Figure 4.29: (a) Test input VSWR, (b) Test output VSWR

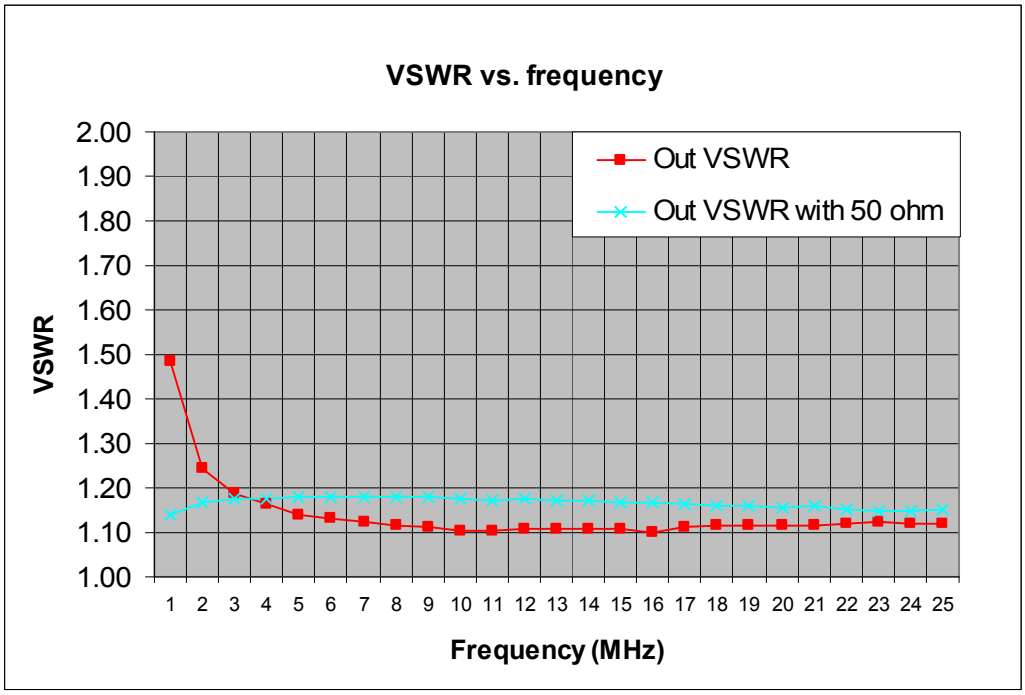


Figure 4.30: Output VSWR of DUT

4.3.8 Conclusion

The DUT (Boost Rev2.0) is good and meets requirements. Performance is:

- Gain: 37 dB
- Gain flat: 1 dB
- Frequency: 1 to 25 MHz
- Po-1: 27.5-28 dBm
- Max Po: 28.5 dBm
- Max Pi: <0 dBm

- Input VSWR: <1.1
- Output VSWR: < 1.5
- Power supply voltage: 8.0 V
- Total current: <0.52 A
- Size: 84 mmX35 mmX18 mm

4.4 Final stage and whole HPA

The power FET works near the max rate of the device. It can easily be damaged if it was set incorrectly. Use the following principle: test from one pulse to multi-pulse and from lower power to higher power.

Supply voltage and bias voltage should be at or near the recommended level. Otherwise, the risk of damaging a device will increase. For example, if voltage drops from 24 V to 12 V, the gain of the device may increase, which will increase the oscillation risk. If the gate bias voltage is too low, the amplifier status will change from Class A to Class B, which will also increase the risk of oscillation.

To get as much information as possible in case the FET fails, these test procedures are followed:

- One pulse test for G and VSWR
- Optimum Vgs for G, Po, waveform, spike and rise time
- Sweep test for G, in VSWR and out VSWR
- One pulse test for max safe Po at 50 ohm load
- Sweep test for linear curve (Po vs. Pi) to get Po-1
- Heavy duty cycle test and get Idq
- MP for Mole
- 3 dB ATT+ Mole at reduced Po
- 1.5 dB ATT+ Mole at reduced Po
- CPMG test with 1.5 dB ATT+ Mole at reduced Po

4.4.1 Schematic

The schematic diagram is shown in figure 4.31.

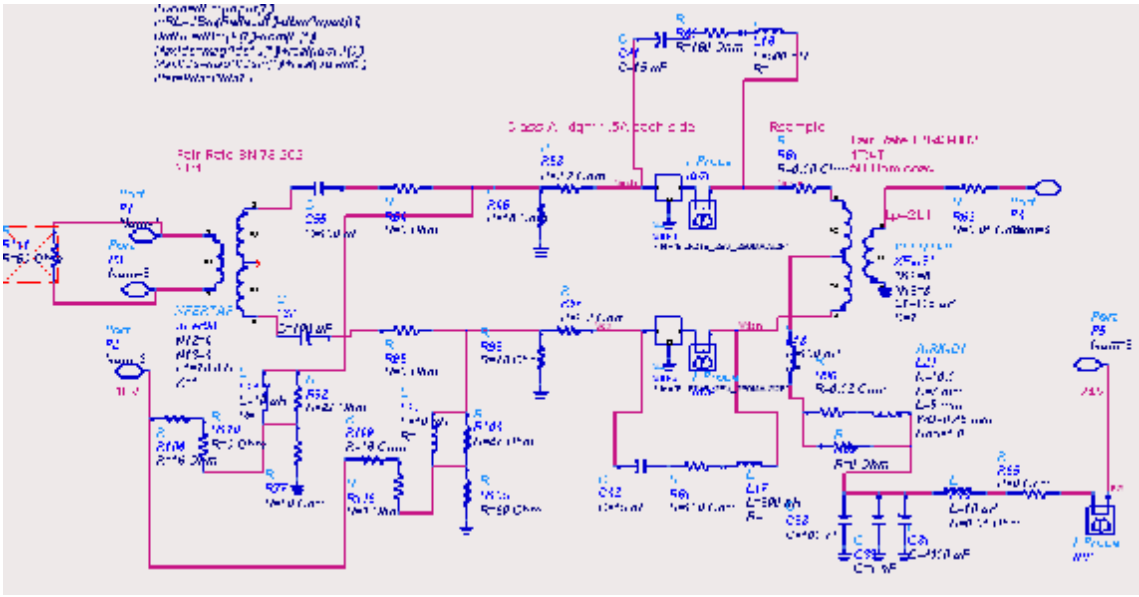


Figure 4.31: Schematic of DUT

4.4.2 Gate voltage without FET

For the safety of FET, Vgs level and waveform should be tested before FET is installed to make sure there is no spike and the level is as expected.

There are three multi-turn potentiometers (PM). One is for power supply of gate drives of both sides of the FET, Vc. One is for high side of gate bias voltage, Vgsh. One is for low side of gate bias voltage, Vgsl. If Vc is changed, Vgsh and Vgsl will change at the same time and same scale. If Vc is fixed, Vgsh or Vgsl can be tuned separately.

Set both PM of Vgs at max voltage position. Set the power supply voltage of the gate drive (Vc) to 10 V. Vgs without FET is tested as shown below.

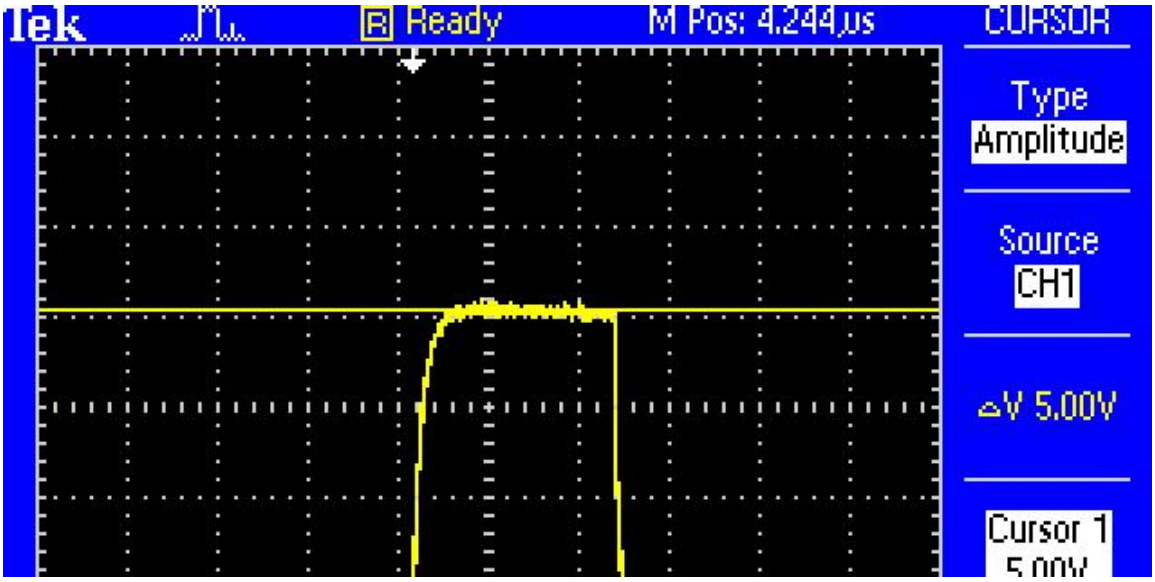


Figure 4.32: Vgs without FET, max PM position, Vc=10 V

The figure above shows no spike and the waveform is close to the ideal square shape. The peak is 5 V, which is on the high side of the gate voltage range. Pulse gate bias is ready for FET.

4.4.3 FET and shield

For safety reasons, Vc is adjusted from 10 V to 8 V before installing the FET.
After the FET is installed, then the shield plate and top covers are installed to isolate input and output. This is shown in the Figure 4.33 and the Figure 4.34.

Figure 4.33: Final stage layout

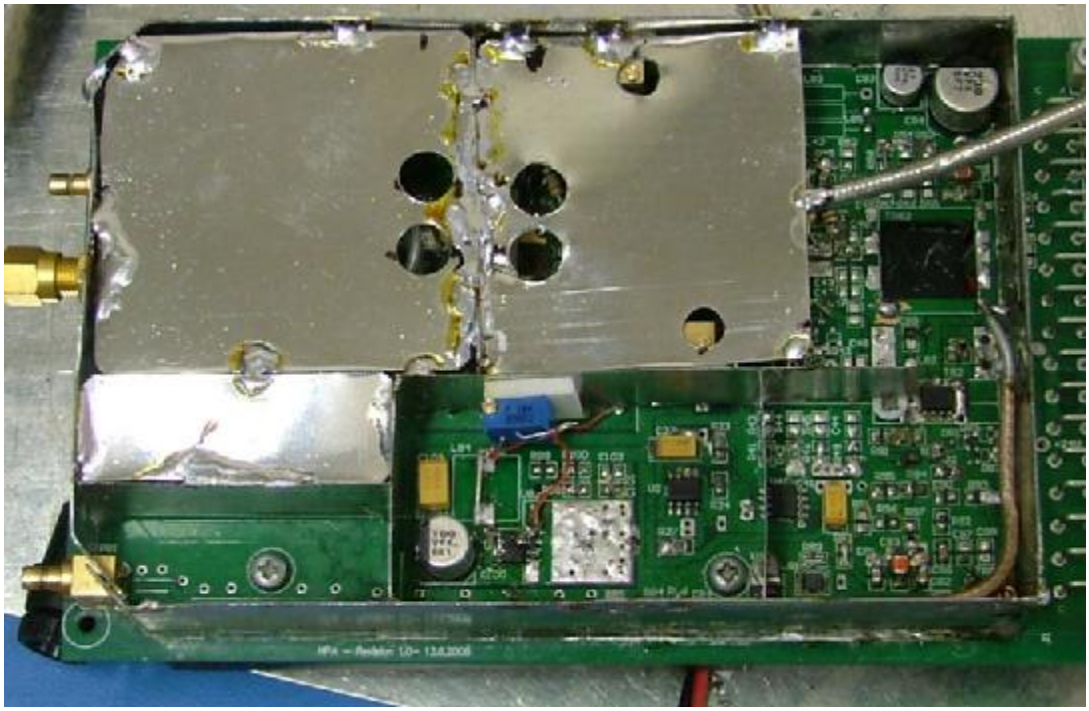


Figure 4.34: Shield of last stage

There are six holes on the covers. They are for tuning Vgs and testing Vgs and Vds of both sides. PM of Vc is on the wall of middle bottom cavity.
The final stage is ready for testing.

4.4.4 One pulse test

For any test, input and output ports should be terminated with 50 ohm load. Output load is a 50 W 40 dB attenuator (ATT) to create a reliable and powerful 50 ohm load. To test output voltage, a sample is picked from output of the 40 dB ATT of 50 W. Input voltage can be got found from the double direction coupler (DDC) or from the output of 50 W 40 dB ATT while it is connected directly with the source.
Test SW settings are as shown below.

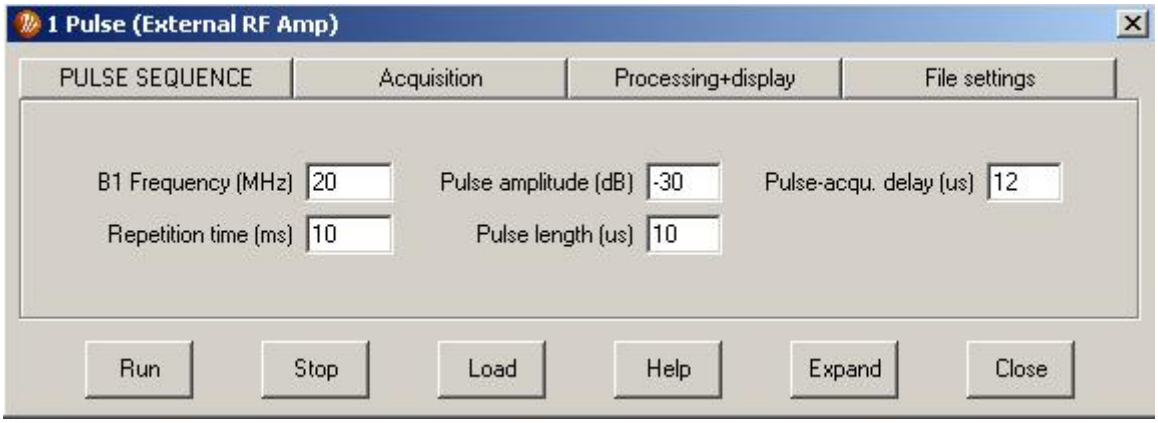


Figure 4.35: Setting, 1 of 2

In the 1 Pulse program, advance time between the gate and RF signal is fixed at 1 us. “Pulse-acqu. Delay” is for the delay between the pulse and the time to collect the NMR date. It is not for the gate and RF signal.

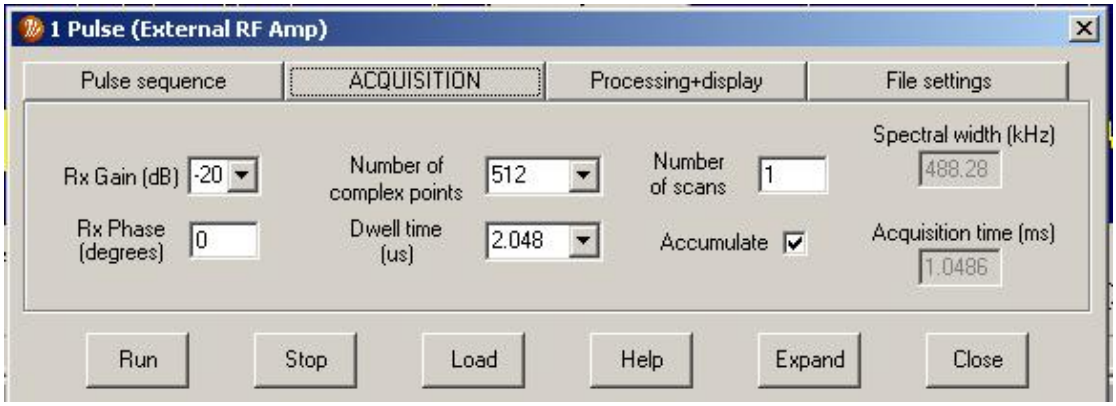


Figure 4.36: Setting, 2 of 2

Vi and Vo are tested to get gain. System setting: TX+ pre-driver (17 dB) +drive (20 dB)+ 10 dB ATT+ DDC-out+ DUT+ 40 dB ATT+ 50 ohm+ ch1 (X10), DDC-fwd/rev+50 ohm+ ch2 (X10)

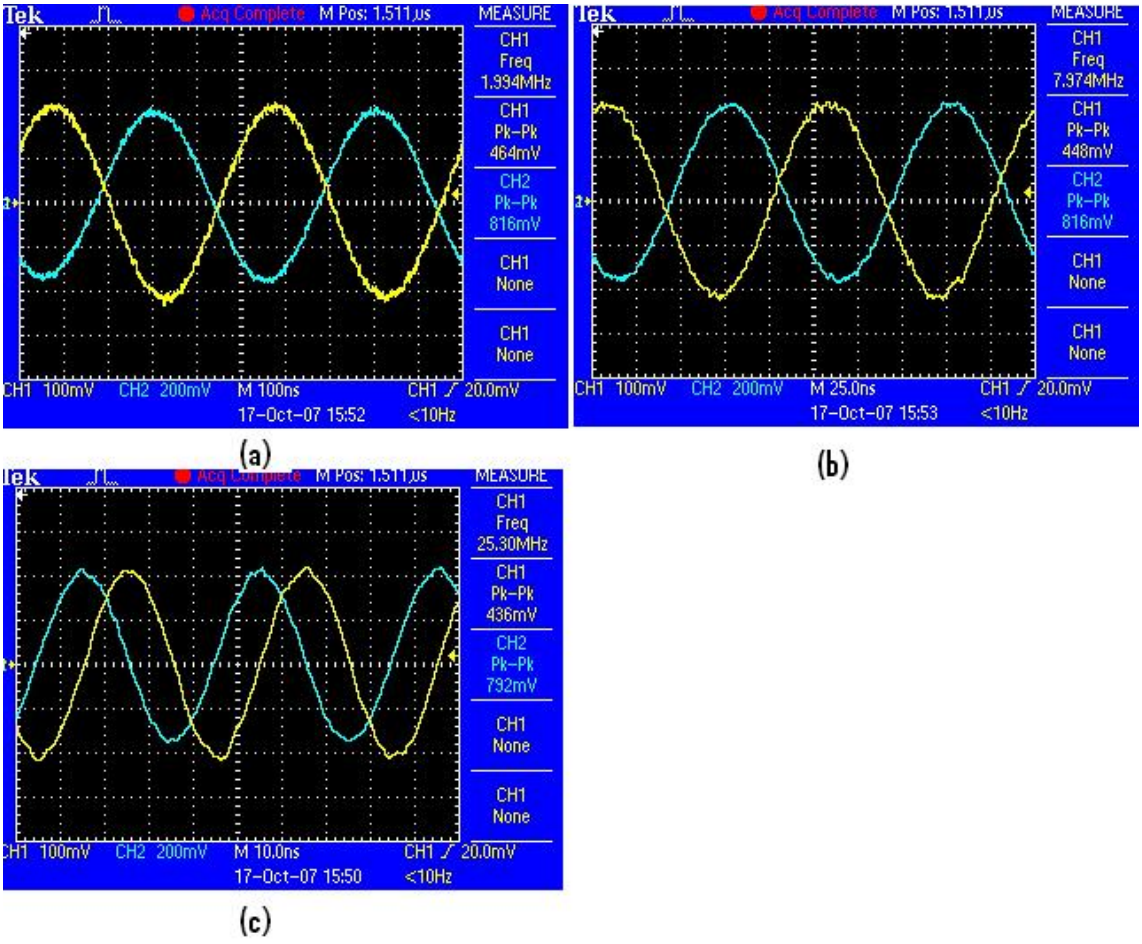


Figure 4.37: Vo (ch1X10) and Vi (ch2X10) at TX=-30, (a) 2MHz, (b) 8 MHz, (c) 25 MHz

Using above data and Vr, gain and in VSWR is produced as shown below. Gain is about 26 dB and very flat across the band. Input VSWR is very good. These results are similar to the simulation.

Table 4.4: Gain and in VSWR

Terms	Unit	2MHz	8MHz	25MHz	Notice
Read Vi	mVpp	464	448	436	
Vi scale		10	10	10	
Read Vo	mVpp	816	816	792	
Vo scale		10	10	10	
Out ATT	dB	40	40	40	
Out ATT scale		100	100	100	
Vo factor		10	10	10	
Real Vo	mVpp	8160	8160	7920	
Read Vr	mVpp	10	10	10	Limited by noise of oscilloscope
Coupling of DDC	dB	20.6	20.6	20.6	
CF of coupling	dB	0.6	0.6	0.6	
Gain	dB	**25.5**	**25.8**	**25.8**	
Reflaction		0.0216	0.0223	0.0229	
in VSWR		**1.04**	**1.05**	**1.05**	

From previous setting, in/out port of the DUT is swapped to test out VSWR. This is shown in Figure 4.38 and **Error! Reference source not found.**.

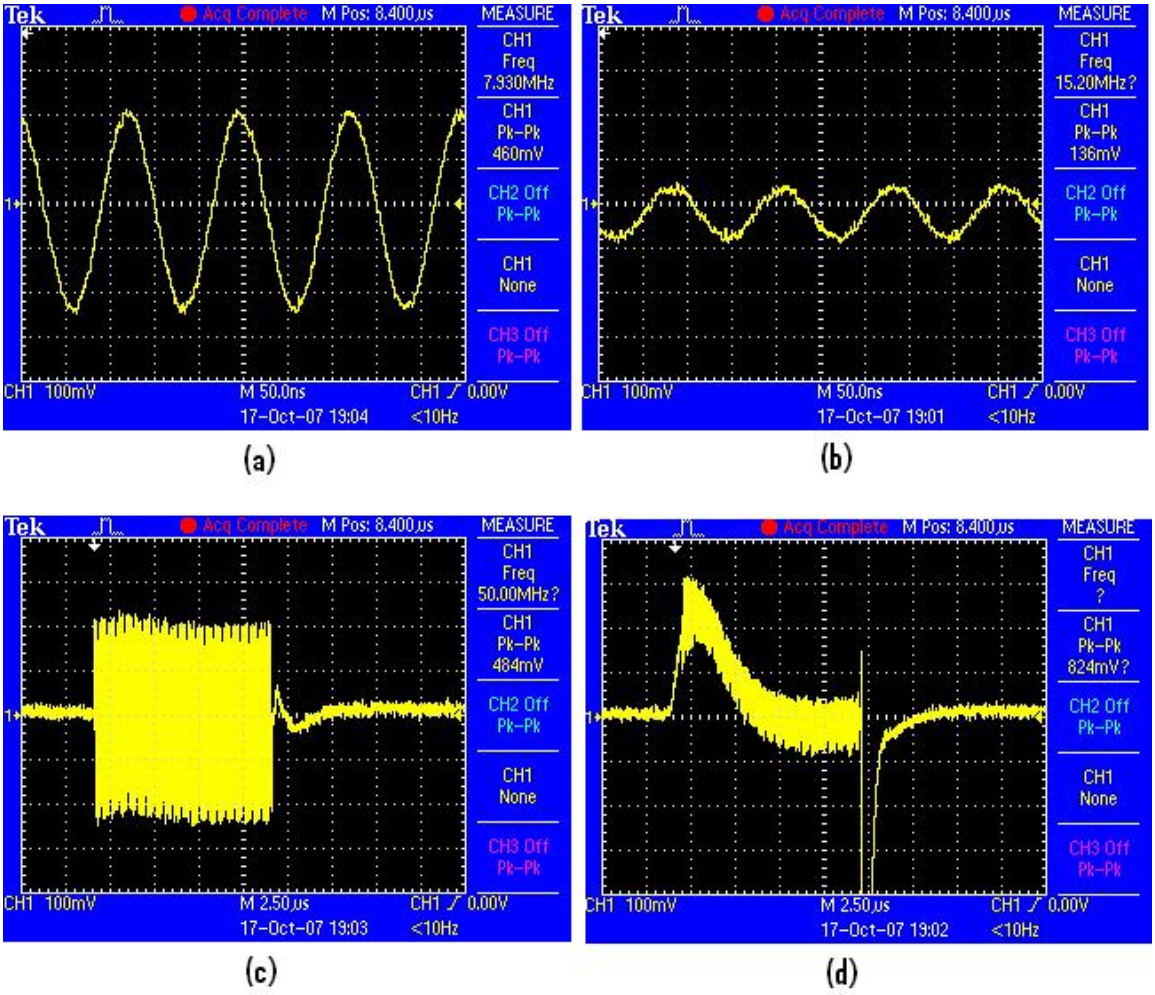


Figure 4.38: Test VSWR at 8 MHz and TX=-30, (a) Vf, (b) Vr, (c) Outline of Vf, (d) Outline of Vr

The waveform of reflection is different from forward because the total reflection is a summary of spikes caused by gate blanking and real reflection. To avoid the effect of the spikes, the Vf and Vr are taken from a stable period rather than the starting period.

Table 4.5: OutVSWR

Terms	Unit	2MHz	8MHz	25MHz	Notice
Read Vf	mVpp	480	460	468	
Read Vr		160	136	108	
Scale		10	10	10	
Reflaction		0.333	0.296	0.231	
in VSWR		**2.00**	**1.84**	**1.60**	
condition: TX=-30					

In fact, if output 40 dB ATT is viewed as a part of the probe and the scale of the probe is set as X100 (40 dB), the read voltage on the oscilloscope will be the real output voltage of the DUT. In the same way, if DDC coupling 20.6 dB is viewed as a part of the probe and the scale of the probe is set as X10 (20 dB), the read voltage from the forward port will be close to the real input voltage. The error is only 0.6 dB=20.6 dB-20 dB. The real input voltage will be the read voltage minus 0.6 dB.

The output VSWR of the DUT is good even if at a lower signal level. It means the DUT is stable. The VSWR scale is in the ideal range.

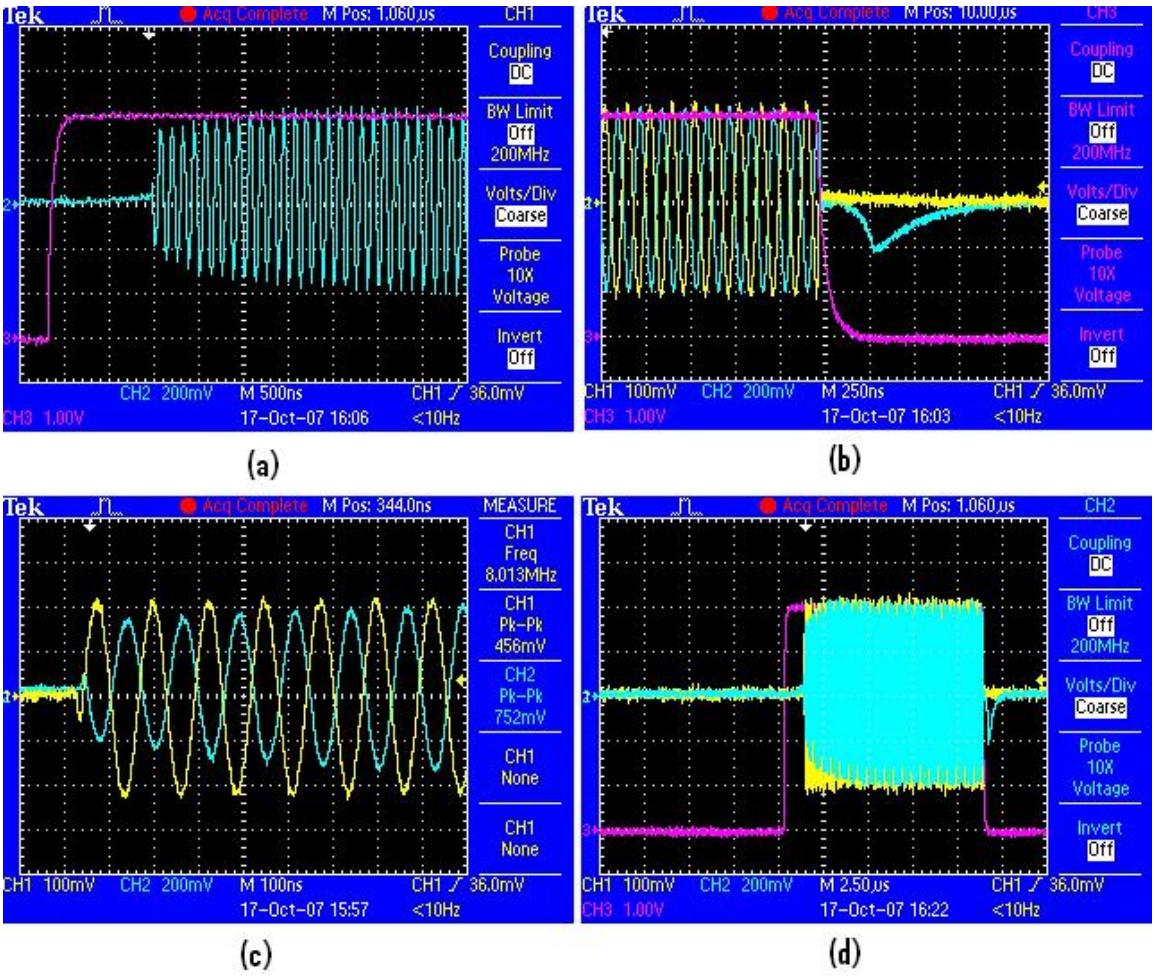


Figure 4.39 Waveform of Vi (ch1X10), Vo (ch2X10) and gate blanking (ch3), (a) Rise edge of Vo, (b) Fall edge, (c) Vi and Vo at rise edge, (d) Envelope

In Figure 4.39, the spike caused by the rising edge of the gate blanking is not seen; the spike caused by the falling edge of the gate blanking is very small; the envelope of Vo at the falling edge is an ideal square (no overshoot, no undershoot); the envelope of Vo at the rising edge is an undershoot (rise time is about 2.5 us). As initial results, these are very good.

Vc and Vgs in test is shown in Figure 4.40.

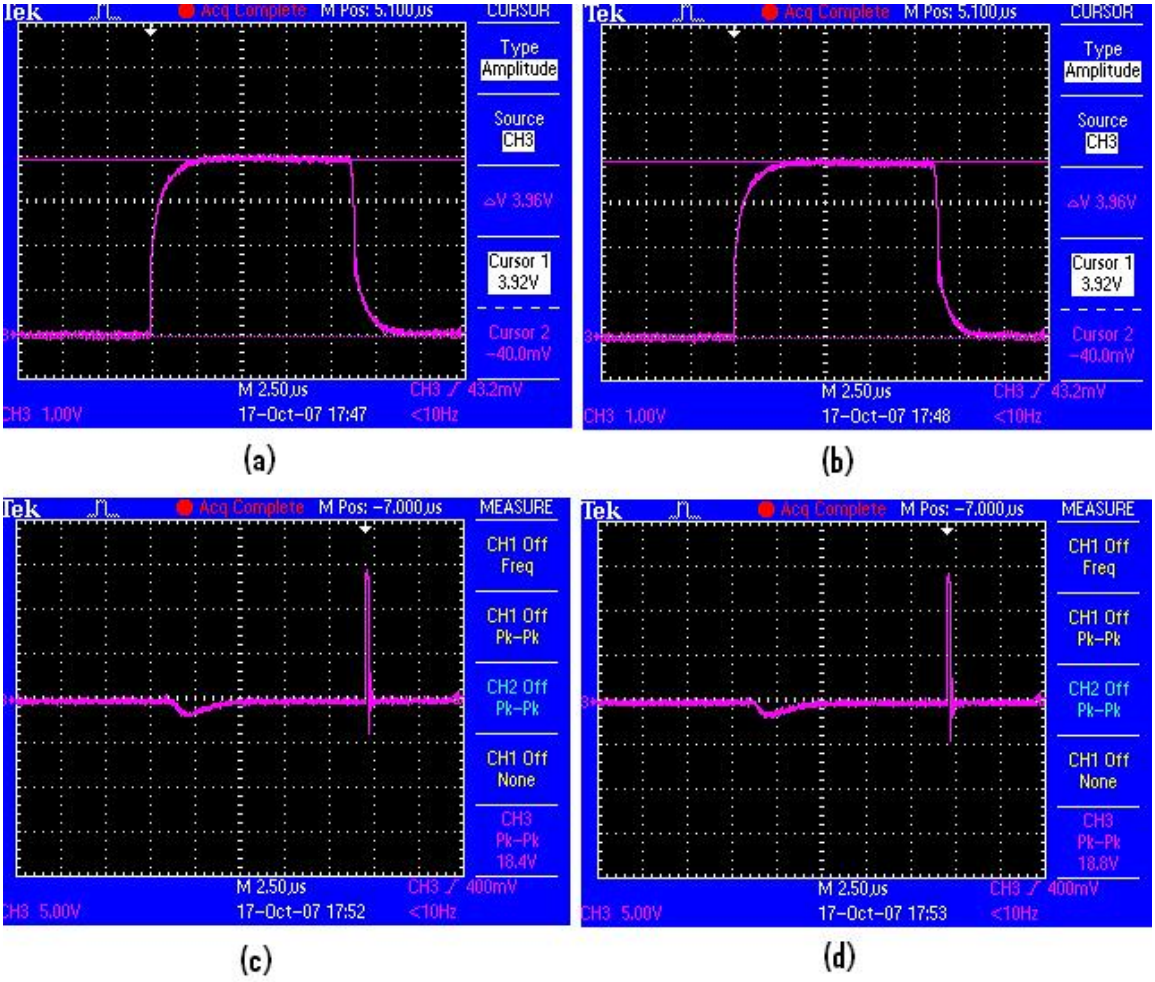


Figure 4.40: Vgs (DC) and Vds (AC) at Vc=8 V and max position of MP, (a) Vgsh, (b) Vgsl, (c) Vdsh, (d) Vdsl

The high side FET is the FET on the high side of the PCB while output of the PCB is at the left hand side and top side of PCB is up.

The Figure 4.40 shows: a. good symmetry between high and low side. b. rise time of RF envelope caused by rise time of Vgs. c. Spike of Vo (2 V) is much smaller than spike of Vds (13 V) due to cancelling effect.

Vdsl detail is shown in the Figure 4.41. This is built up by a positive voltage plus a ring down.

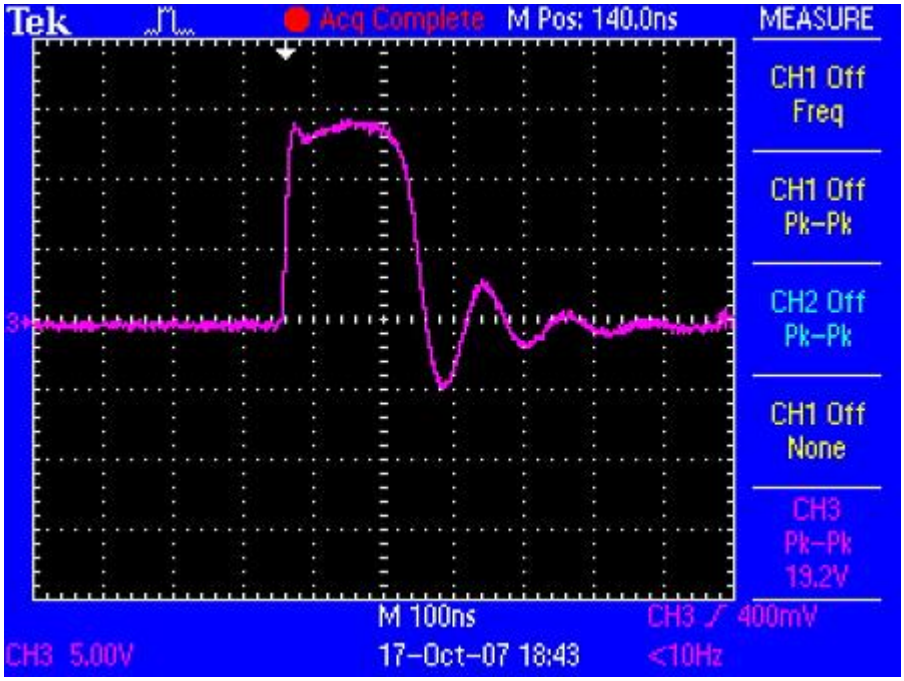


Figure 4.41: Vdsl detail

4.4.5 Optimum Vgs

The purpose of tuning DC gate voltage each side of the FET is optimum gain, output power and spike. The goal is higher output power, higher gain and lower spike.

Firstly, check Gain and Po at current Vgs condition, as shown in the Table 4.6.

Table 4.6: Waveform and Gain vs. TX

TX	In ATT	Vf	Vo	CF	Vi	G	Po	Waveform	Recoard
	dB	mVpp	Vpp	dB	Vpp	dB	W		
-30	10	44	8.24	20.6	0.453	25.2	0.17	Sinsoid	5:16:00 p.m
-25	10	75.6	14	20.6	0.779	25.1	0.49	Sinsoid	17:17
-20	10	134	24.6	20.6	1.380	25	1.5	Sinsoid	17:20
-15	10	234	44	20.6	2.410	25.2	4.8	Sinsoid	17:22
-10	10	378	69.6	20.6	3.893	25	12.1	Sinsoid	17:23
-5	10	440	84.8	20.6	4.532	25.4	18.0	Square	17:25
-20	0	428	76.8	20.6	4.408	24.8	14.7	Sinsoid	17:29
-15	0	732	118	20.6	7.540	23.9	34.8	Sinsoid	17:30
-10	0	1190	186	20.6	12.257	23.6	86.5	Square	17:32
CF=20LOG(Vi/Vf) Gain=20LOG(Vo/Vi) Po=(0.5*0.707*Vo)^2/50 One pulse 10us, 8MHz TX+Pre+drive+in ATT+in-DDC+DUT+40dB ATT+50 ohm+ch2(X100) DDC-fwd+50 ohm+ch1(X1) Vc=8V, Vgs=4V, max position MP									

The DUT is at saturation before Po reaches 150 W, which is the expected Po. Vgs is too low. Then test gain and Po with increasing DC Vgs through increasing Vc, as shown in the Table 4.7.

Table 4.7: Gain and Po vs. Vgs

TX	Vc	Vgs	In ATT	Vf	Vo	CF	Vi	G	Po	Waveform	Recoard
	V	V	dB	mVpp	Vpp	dB	Vpp	dB	W		
-10	8	4	0	1190	186	20.6	12.257	23.6	86.5	Square	18:32
-10	8.84	4.56	0	1190	246	20.6	12.257	26.1	151	Sinsoid	18:59, 19:0
-10	9.05	4.72	0	1220	260	20.6	12.566	26.3	169	Sinsoid	19:09
-10	9.21	4.8	0	1210	264	20.6	12.463	26.5	174	Sinsoid	19:21
-10	9.51	5.04	0	1190	268	20.6	12.257	26.8	180	Sinsoid	19:24
-10	9.76	5.2	0	1220	274	20.6	12.566	26.8	188	Sinsoid	19:28
-10	9.9	5.32	0	1220	272	20.6	12.566	26.7	185	Sinsoid	19:31,10:33
-10	9.49	5	0	1240	276	20.6	12.772	26.7	190	Sinsoid	19:43
CF=20LOG(Vi/Vf) Gain=20LOG(Vo/Vi) Po=(0.5*0.707*Vo)^2/50 One pulse 10us, 8MHz TX+Pre+drive+in ATT+in-DDC+DUT+40dB ATT+50 ohm+ch2(X100)											

While Vgs=5.2 V, Po and Gain reach maximum. Take Vgs=5 V for trade-off.

While first running the test in the morning, the voltage will be higher. To avoid damage to the FET, start at a lower power level, as shown in Table 4.8. This shows that the gain of the last stage is constant and output voltage is changed due to changing of input voltage. The drive stage output voltage is changed with temperature due to heating caused by voltage regulators. Keep the drive power at a constant or limit it to protect the last FET.

Table 4.8: Cold stat

	Vf	Vo	CF	Vi	G	Notice
Condition	mVpp	Vpp	dB	Vpp	dB	
First work	480	114	20.6	5	26.9	
After 10 minutes work	448	108	20.6	5	27.0	
One pulse, 10us, TX=-20, 8MHz,N=10000, Vgs=5V, Vc=9.49V						

Let us check the rise time and spike below.

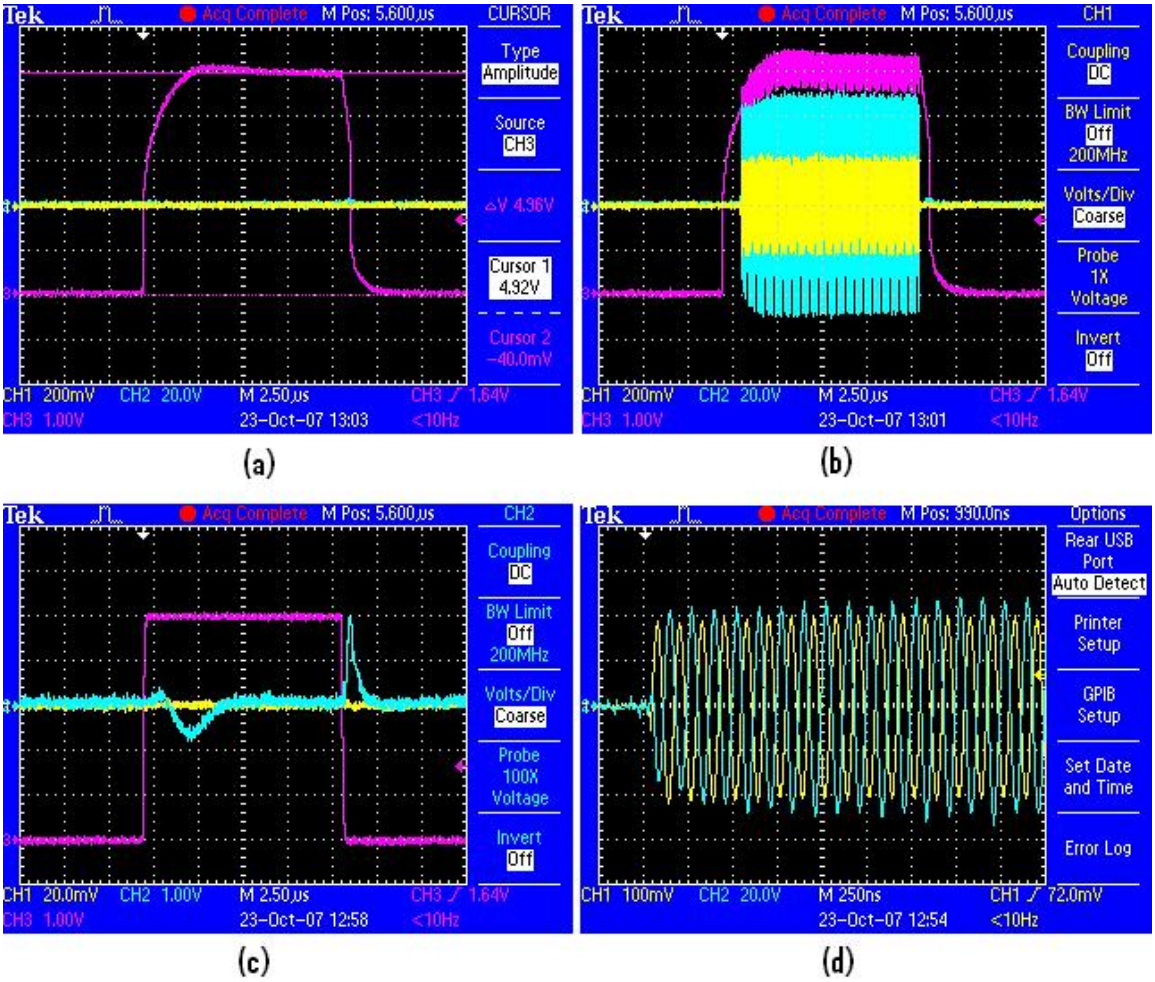


Figure 4.42: Rise time and spike at 8 MHz and TX=-20, Vf (ch1), Vo (ch2), Vgsh (ch3), (a) Vgsh, (b) Vf, Vo and Vgsh, (c) Vf, Vo and gate blanking, (d) Vf and Vo

The Figure 4.42 shows that the spike of output voltage is less than 2 V, which is very good, and rise time of output voltage is caused by rise time of Vgs, while the delay of gate blanking and RF signal is 1 us. If the delay setting is 3 us, the rise time should be 0 us. The delay is fixed in "1 Pulse" So the SW panel "Exercise the HPA" is used to change the delay, as shown below.

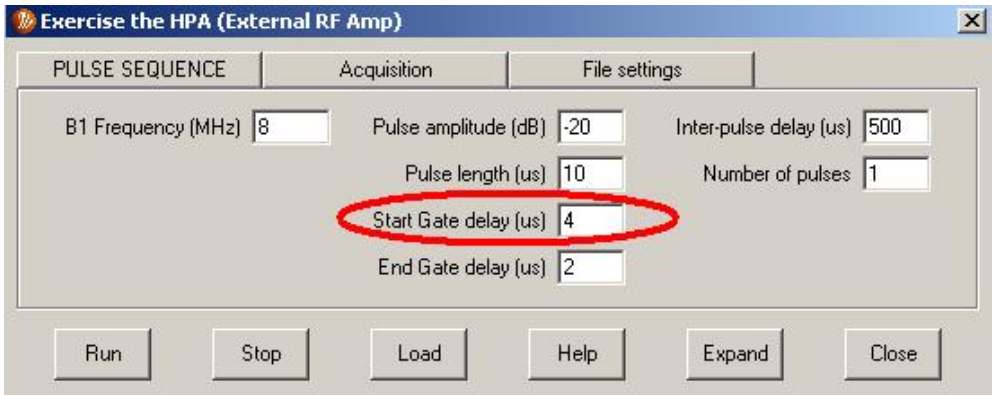


Figure 4.43: Setting delay

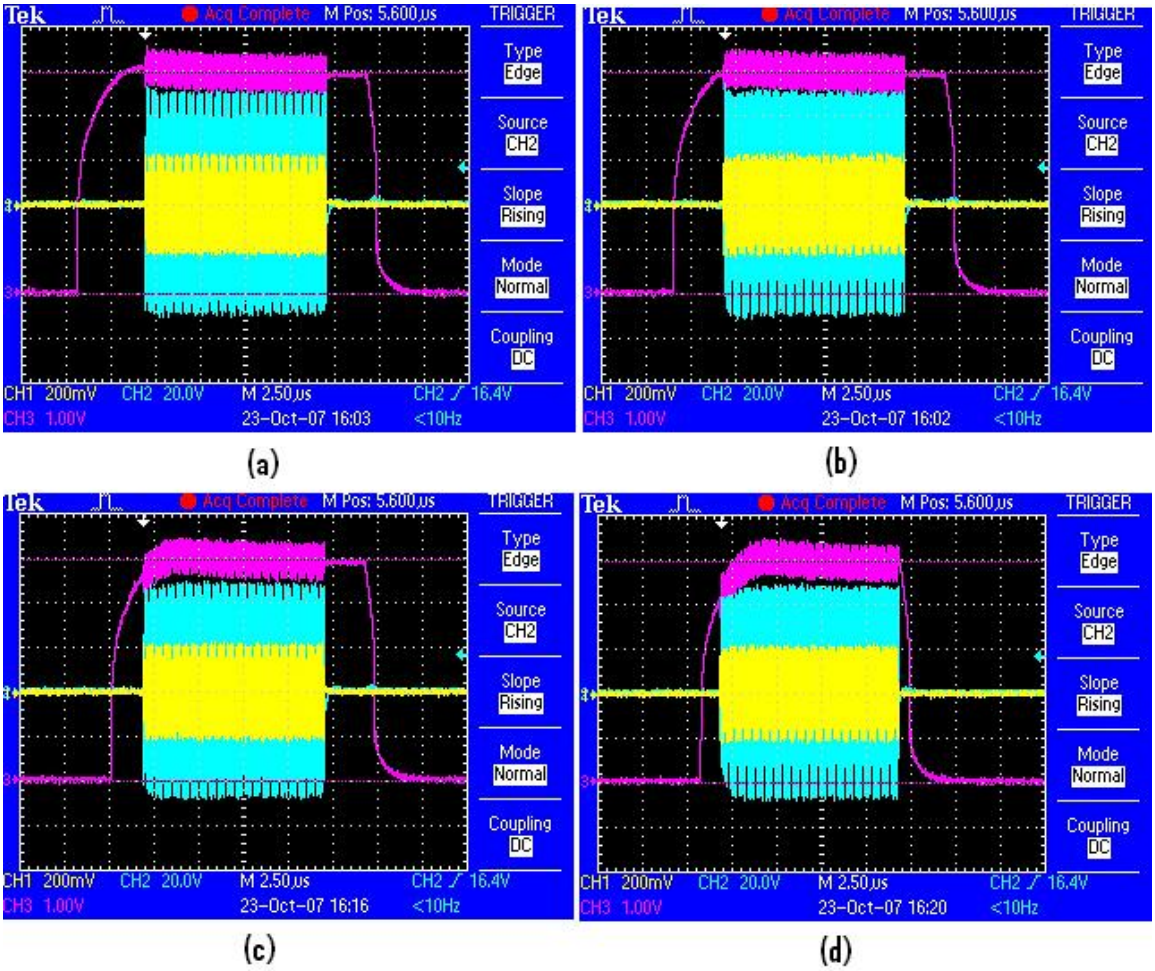


Figure 4.44: Experienced rise time and spick at 8 MHz and TX=-20, Vf (ch1), Vo (ch2), Vgsh (ch3), (a) Delay 4 us, (b) Delay 3 us, (c) Delay 2 us. (d) Delay 1 us

The Figure 4.44 shows that the experienced rise time is ideal if the delay is more than 3 us.

In summary, if the settings are Vgs=5.0 V, Vc=9.5 V and delay=3 us, then gain will be 26.5 dB, linear Po is 180 W, spike is less than 2 V and rise time is zero. Optimum Vgs is finished successfully.

4.4.6 Gain and VSWR at lower power with frequency sweep

With frequency, performance of DUT can be tested across band quickly and accuracy.

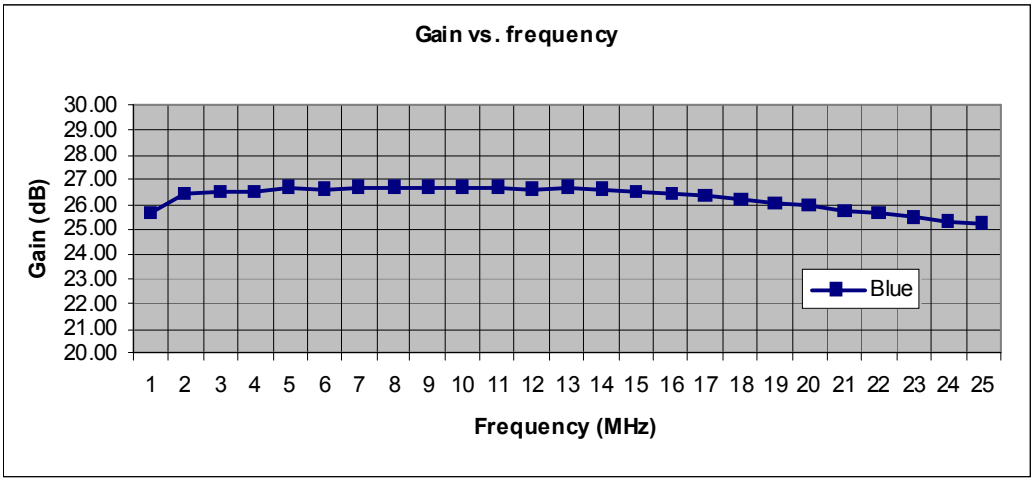


Figure 4.45: Gain

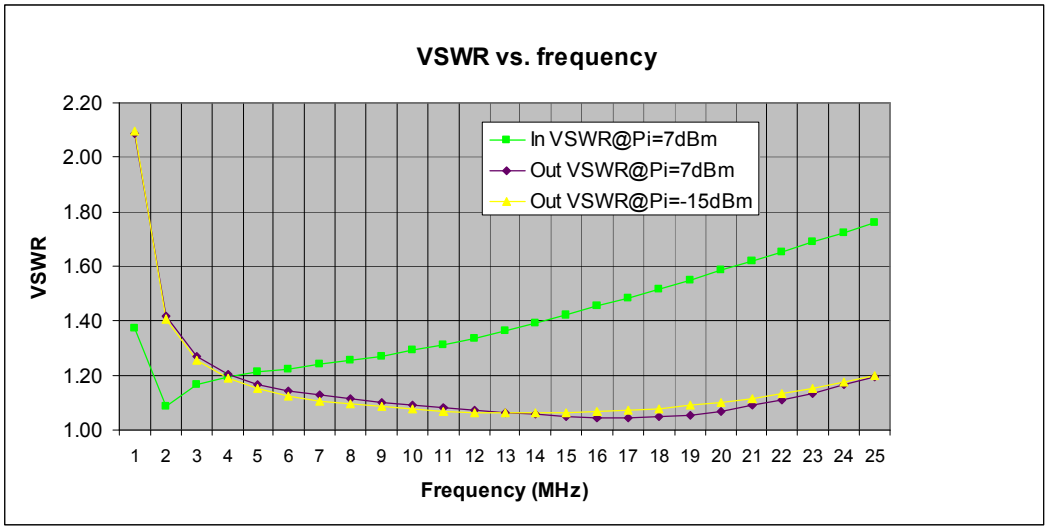


Figure 4.46: VSWR

Above figure shows: gain is about 25.2 dB to 26.7 dB. Gain flatness is 1.5 dB across the band. Input VSWR is 1.4 while frequency is lower than 14 MHz. It increases to 1.8 at 25 MHz. This is still OK. Out VSWR is lower than 1.8 while frequency is higher than 2 MHz. Out VSWR is degraded at lower frequency, which may be caused by core 61# material but it is still OK, VSWR is 2.0 at 1 MHz. If 43# material is used, it will be improved. The out VSWR is not a function of drive power. This is good.

In summary, gain, in VSWR and out VSWR are all good.

4.4.7 One pulse test for max safe Po at 50 ohm load

We want to know maximum safe output power. It is tested under 50 ohm load. Testing is under 1 pulse to avoid damage FET in case. The output power is tested while increasing input power. Table 4.9 and Figure 4.47 show output power and output waveform with different input power.

Table 4.9: Linear vs. TX

TX	In ATT	Vf	Vo	CF	Vi	Pi	Pi	G	Po	Waveform	Recoard
	dB	mVpp	Vpp	dB	Vpp	W	dBm	dB	W		
-30	0	140	30	20.6	1.44	0.005	7.16	26.4	2.249	Sinsoid	
-25	0	234	50.8	20.6	2.41	0.015	11.62	26.5	6.45	Sinsoid	
-20	0	420	90.4	20.6	4.33	0.047	16.70	26.4	20.4	Sinsoid	19:55 of 23-
-15	0	744	162	20.6	7.66	0.147	21.67	26.5	65.6	Sinsoid	
-10	0	1180	240	20.6	12.15	0.369	25.67	25.9	144.0	Sinsoid	19:57
-9	0	1260	252	20.6	12.98	0.421	26.24	25.8	158.7	M. Sine	19:58
-8	0	1300	260	20.6	13.39	0.448	26.51	25.8	168.9	M. sine	20:01
-7	0	1320	260	20.6	13.60	0.462	26.65	25.6	168.9	Square	20:03
-6	0	1340	266	20.6	13.80	0.476	26.78	25.7	176.8	Square	20:04

CF=20LOG(Vi/Vf)
Gain=20LOG(Vo/Vi)
Po=(0.5*0.707*Vo)^2/50
Exercise the HPA 10us, 8MHz
TX+Pre+drive+in ATT+in-DDC+DUT+40dB ATT+50 ohm+ch2(X100, Vo)
DDC-fwd+50 ohm+ch1(X1, Vf)
Vc=9.5V, Vgs=5V, max position MP

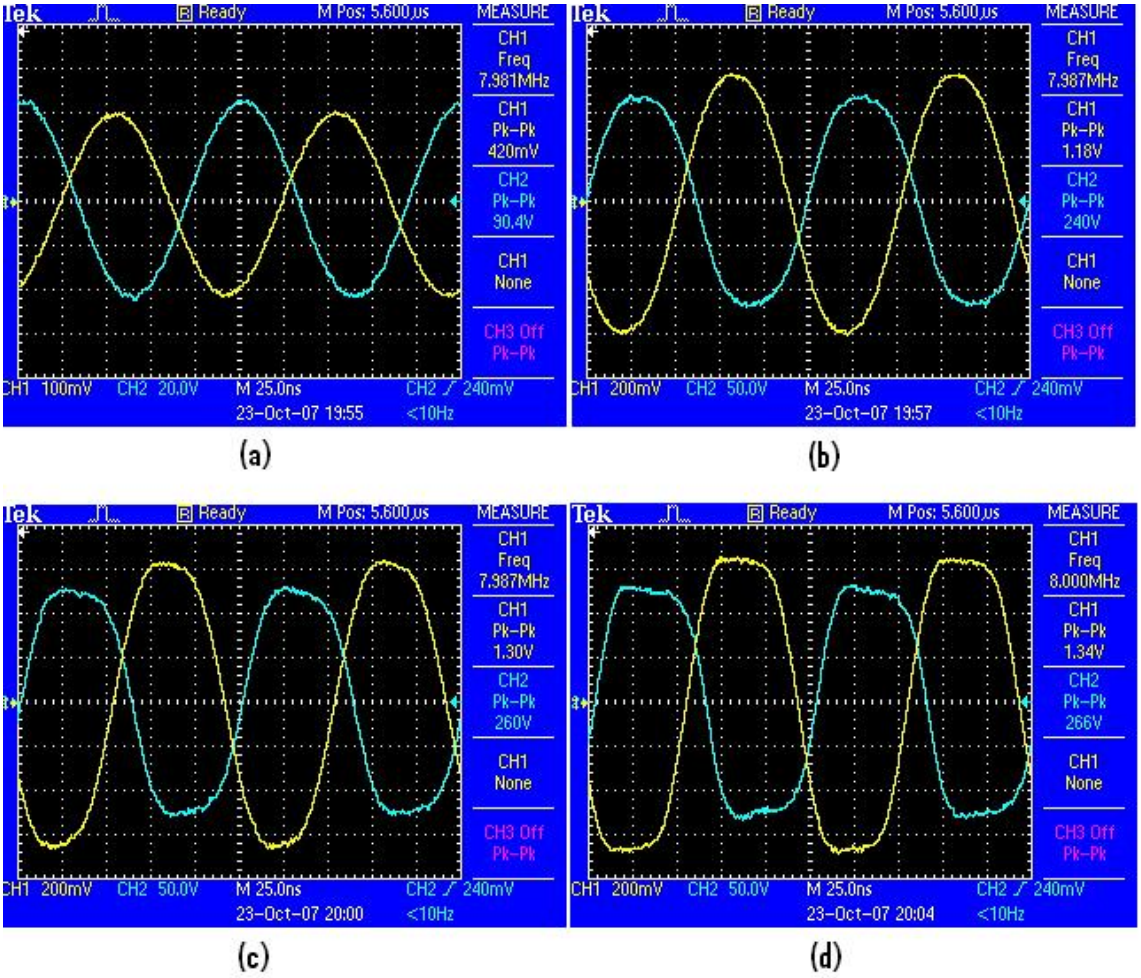


Figure 4.47:Vo (ch2) and Vf (ch1) (a) TX=-20, (b) TX=-10, (c) TX=-8, (d) TX=-6

Po reaches saturation at 170 W. The DUT is linear while TX is under -10. The DUT is still safe while TX is up to -6. The saturation is caused by the drive stage rather than the DUT.
Maximum safe output power is more than 170W. Maximum input power is more than -6 dBm.

4.4.8 Linearity test

We want to know if DUT is linear between output power and input power and where is the saturation point. The starting point of saturation is decrypted usually by 1 dB compression output power, Po-1.
Test principle and diagram is similar with one in the linear test of the drive stage.
Setting to test DUT (final stage) is as below:
Test output voltage Vo: TX of kea +Boost (pre-drive +drive) +in-DDC+DUT+40 dB ATT+50 olm+ch2 of oscilloscope (X100, Vo)
Test input voltage Vi: TX of kea +Boost (pre-drive +drive) +in-DDC+50 olm+ch2 of oscilloscope (X1, Vi)
Where DDC is a double directional coupler.
Test starting from the middle of the band, 8 MHz. Before testing the linearity of the DUT, the linearity of the test system should be checked. It is shown in the Figure 4.48. There is a little non-linearity in the system.

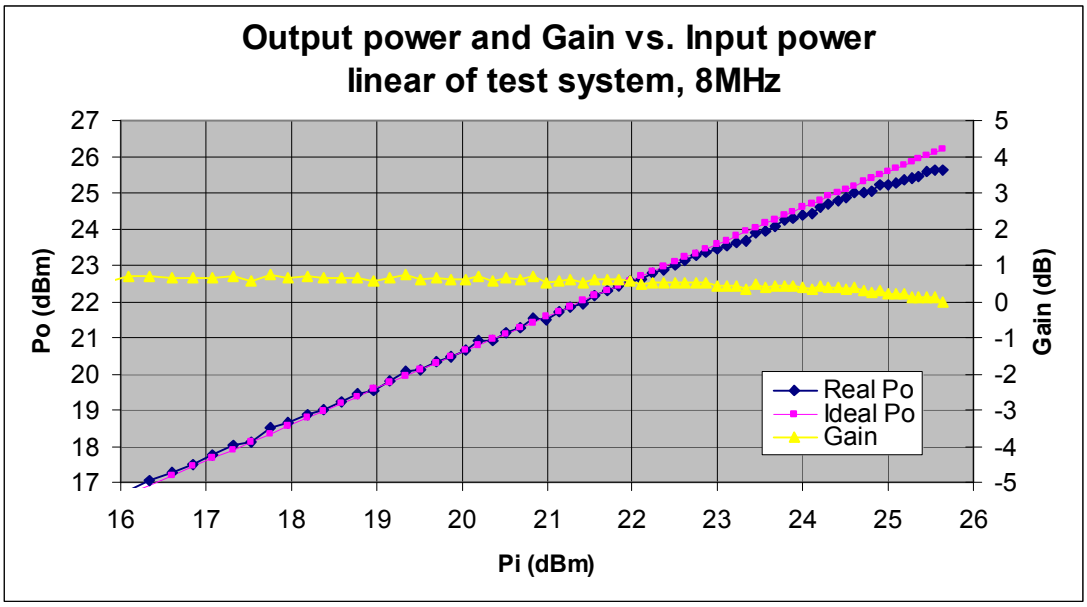


Figure 4.48: Test system linearity at 8 MHz

Then linearity of the DUT is tested. It is shown in Figure 4.49. Po-1 is 52 dBm.

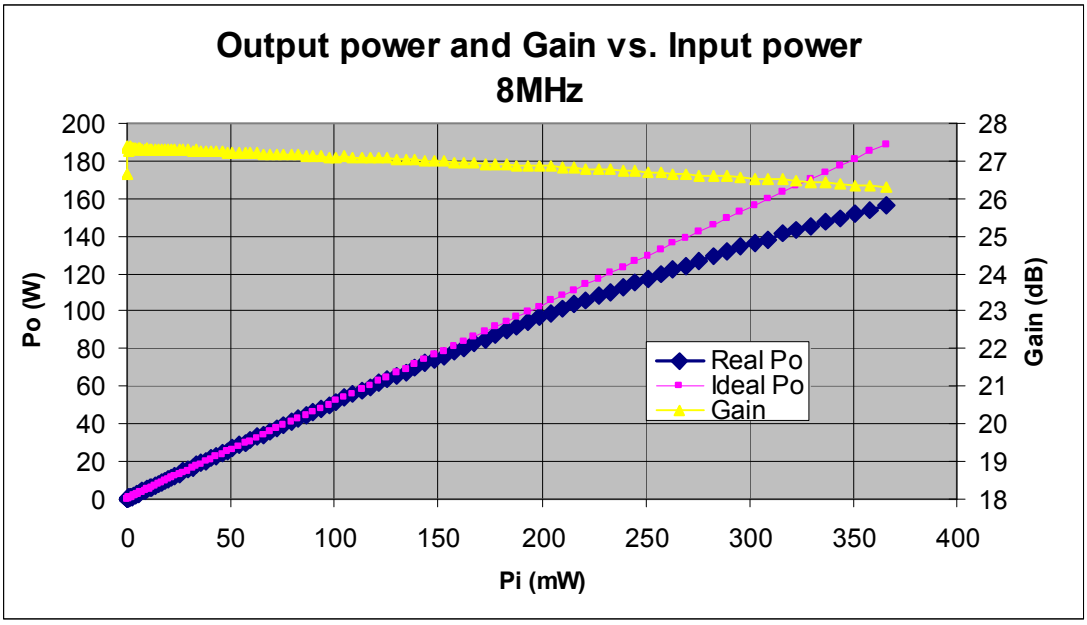


Figure 4.49: Linearity of DUT at 8MHz

In the same way, 2 MHz and 25 MHz data are gained. They are shown in the Table 4.10.

Table 4.10: Po-1 of DUT

		2 MHz	8 MHz	25 MHz
Po-1	W	158	158	107
Po-1	dBm	52	52	50.3

In fact, the real linearity of the DUT should be better. The current test system is slightly non-linear. The Table 4.11 gives the accurate linear status of the DUT.

Table 4.11: xdB compression output of DUT

xdB compression at max TX							Output of DUT			
Frequency	DUT	Total	Test system	Max TX	Pi	Gain	Po,xdB	Po,xdB	Vo,xdB	Vo,xdB
MHz	dB	dB	dB	dBm	dBm	dB	dBm	W	Vop	Vpp
2	0.2	0.9	0.7	-10	25.5	26.5	52	158	126	252
8	0.2	1	0.8	-10	25.5	26.7	52	158	126	252
25	0	3	3	-6	26.5	25.2	50.5	112	106	212
Po,dbm=10LOG(1E3Po,w) Po,w=(1e-3)10^(Po,dbm/10) Po=Vo,rms^2/R Vo,rms=(Po,wR)^0.5 Vo,rms=2^(-0.5)Vo,op Vo,op=2^0.5Vo,rms=2^0.5(Po,wR)^0.5 Vo,pp=2Vo,op										

The Table 4.11 shows:

- At 2 MHz and 8 MHz, output power is 158 W and output voltage is 252 Vpp with 0.2 dB gain compression of the DUT.
- At 25 MHz, output power is 112 W and output voltage is 212 Vpp with 0 dB gain compression of the DUT. Total non-linearity is caused by the drive stage rather than the DUT!
- Because of low gain at 25 MHz, higher Pi will be needed to test linearity status of the DUT at this frequency.

In summary, the DUT linearity is very good at the expected output power (100-200 W).

Then Waveform of output voltage is tested. It is shown in the Figure 4.50.

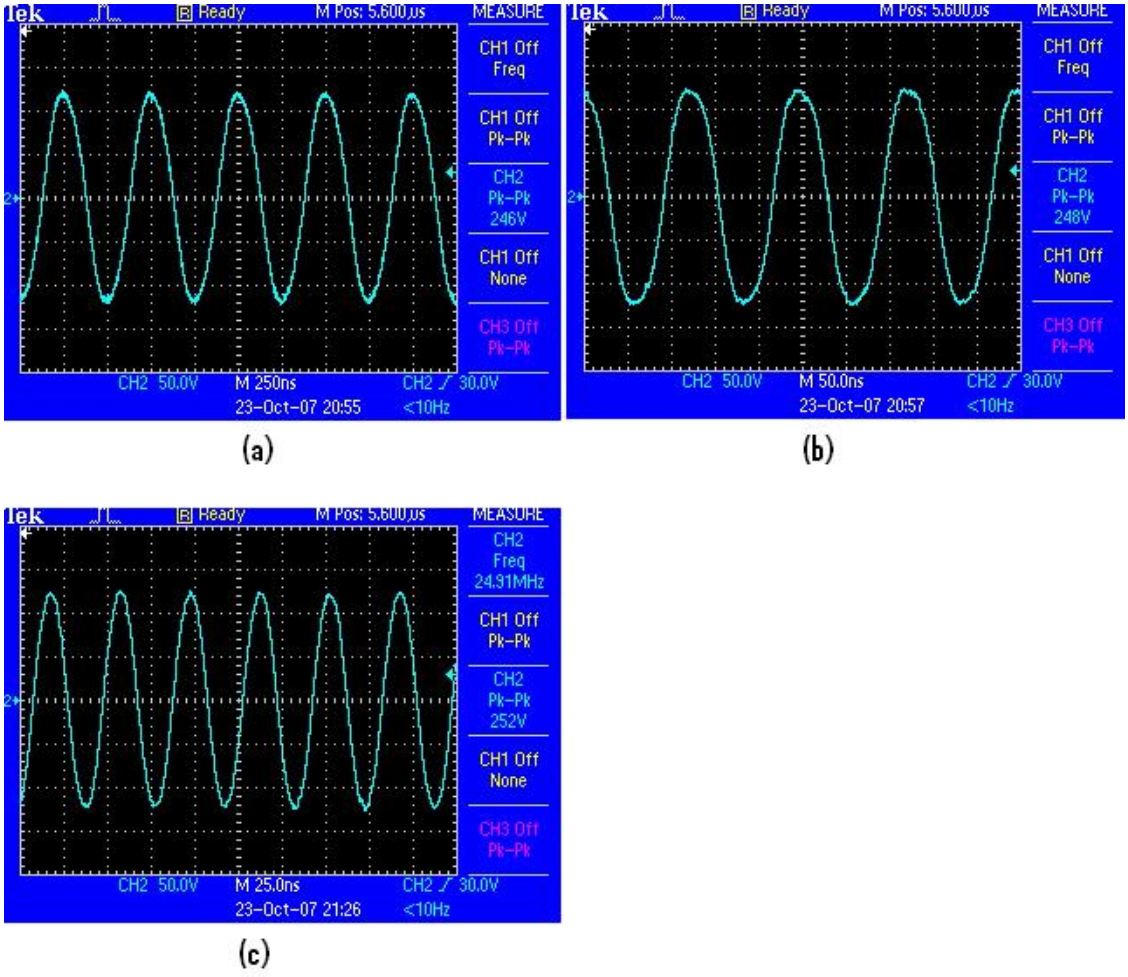


Figure 4.50: Vo at max sweep input, (a) 2 MHz, TX=-10, (b) 8 MHz, TX=-10 (c) 25 MHz, TX=-6

The Figure 4.50 shows that at Po-1, the waveform is sinusoid. It can be used in the NMR test. Sample of Input voltage Vf and output voltage Vo are tested and compared to find non-linearity of the DUT. It is shown in the figure below.

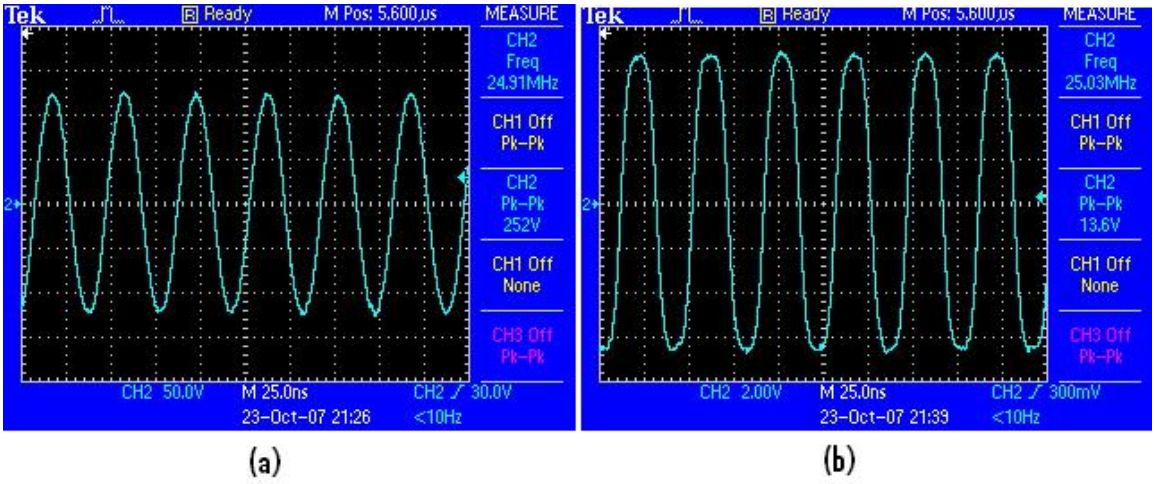


Figure 4.51: Waveform at 25MHz and max sweep input (TX=-6), (a) Vo, (b) Vf

The Figure 4.51 shows that linearity of the output is better than the input. The reason is that the DUT rejects the harmonic frequency and works as a LPF filter.

If RX of Kea is connected with an oscilloscope through a T junction, the waveform tested may be degraded while RX gain is set too high. The reason is that receiver of Kea is overdriven in this condition and gives a strange behavior.

In summary, Po-1 of the DUT is higher than 115 W across 2 to 25 MHz, which is very good. It will be improved if the drive stage is more linear.

4.4.9 Tolerance of output

In practice, we found that output power is high at first test for a day and then it dropt. It was shown in Table 4.12.

Table 4.12: Tolerance Po, G and Pi

	Freq.	TX	Vo	Vi	Pi	Pi	G	Po
	MHz	dBm	Vpp	Vpp	W	dBm	dB	W
First test in the morning	2	-10	292	13.20	0.435	26.39	26.9	213
	8	-10	262	13.40	0.449	26.52	25.8	172
	25	-6	234	14.40	0.518	27.15	24.2	137
Last test in the evening	2	-10	246	11.90	0.354	25.49	26.3	151
	8	-10	248	12.20	0.372	25.71	26.2	154
	25	-6	252	13.40	0.449	26.52	25.5	159
Gain=20LOG(Vo/Vi) Po=(0.5*0.707*Vo)^2/50 Exercise the HPA 10us, 8MHz TX+Pre+drive+in-DDC+DUT+40dB ATT+50 ohm+ch2(X100, Vo) TX+Pre+drive+in-DDC+50 ohm+ch2(X1, Vi) Vc=9.5V, Vgs=5V, max position MP SW: One pulse, 10us, Tr=10ms, data delay=12us								

In conclusion from the table above:

Output power is changed due to temperature is changed.

The temperature is changed due to DUT self-heating.

Po is changed due to changing gain of the DUT and driving power while temperature is changed. The latter is the major factor.

To get same output power, driving power of DUT should increase while temperature of DUT higher. It means that TX of Kea should increase.

4.4.10 Duty cycle test

The duty cycle test is to measure the ability of the DUT to handle continual high power.

Idq of the DUT also can be tested in this way.

The duty cycle is changed by changing the inter-pulse delay. It is shown in the figure below.

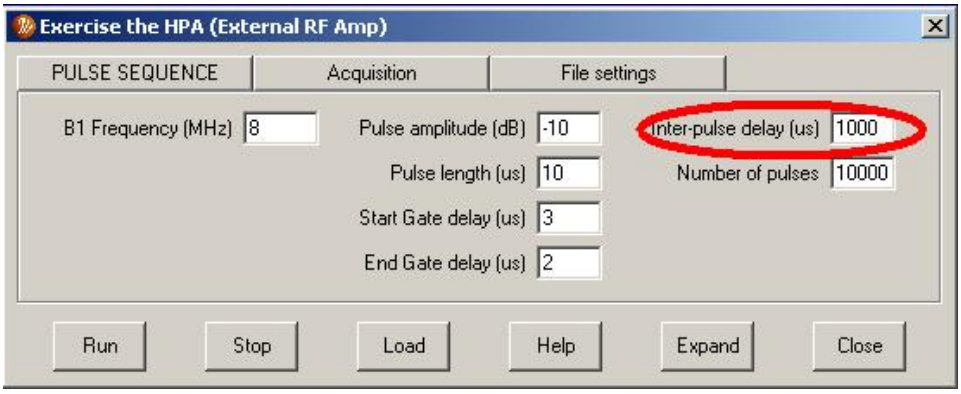


Figure 4.52: SW setting

Test setting: TX+boost+in-DDC+DUT+40 dB ATT+Coax+50 ohm+ch2(X100, Vo); DDC-pwd+50 ohm+Coax+ch1(X10, Vi), TDS2024B

PS: Topward 6303D, 24 V/3 A for DUT, 15 V/3 A for boost

To change the duty cycle, the period is changed while the pulse width is kept at 10 us. Average current, output voltage, waveform and temperature of heat sink of the DUT are monitored. The results are shown in the table and figures below.

Here, Idq is calculated from duty cycle and average current is read from PS. The formula is in the table.

Table 4.13: Vo vs. duty cycle

									Vi	Vo				
Duti cycl	Pass?	Curren	Idq ea	Temp	Pulse	Start	End	Inter-pu	Before	Before	During	After	Delta	
		A	A		us	us	us	us	Vpp	Vpp	Vpp	Vpp	Vpp	Recoard
0.00%	**Pass**	0		Cold	10	6	2	One pulse	13.4	260	260	260	0	16:57 of 24
0.10%	**Pass**	0.03	15.0	Cold	10	6	2	10000	13	252	254	252	0	
0.98%	**Pass**	0.27	13.74	Cold	10	6	2	1000	13	252	250	250	2	17:06
1.93%	**Pass**	0.54	14.0	Cold	10	6	2	500	13	250	250	254	-4	
4.59%	**Pass**	1.29	14.1	Cold	10	6	2	200	13	250	246	252	-2	17:26
0.98%	**Pass**	0.27	13.7	Cold	10	6	2	1000	13.2	250	252	254	-4	17:29
8.47%	**Pass**	2.31	13.6	Cold	10	6	2	100	13	252	242	250	2	17:33
12.82%	**Pass**	3.2	12.5	Cold	10	6	2	60	13	252	228	252	0	18:06
8.47%	**Pass**	2.31	13.6	Cold	10	6	2	100	12.8	252	242	252	0	17:39
		AVE	**13.79**							One pulse		One pulse		
TX=-10, 8MHz, No. of scan=1e4 DC=Pulse/((Start+Pulse+End+Inter-pulse delay) SW: Exercise the HPA Idq each=read I*duty Cycle														

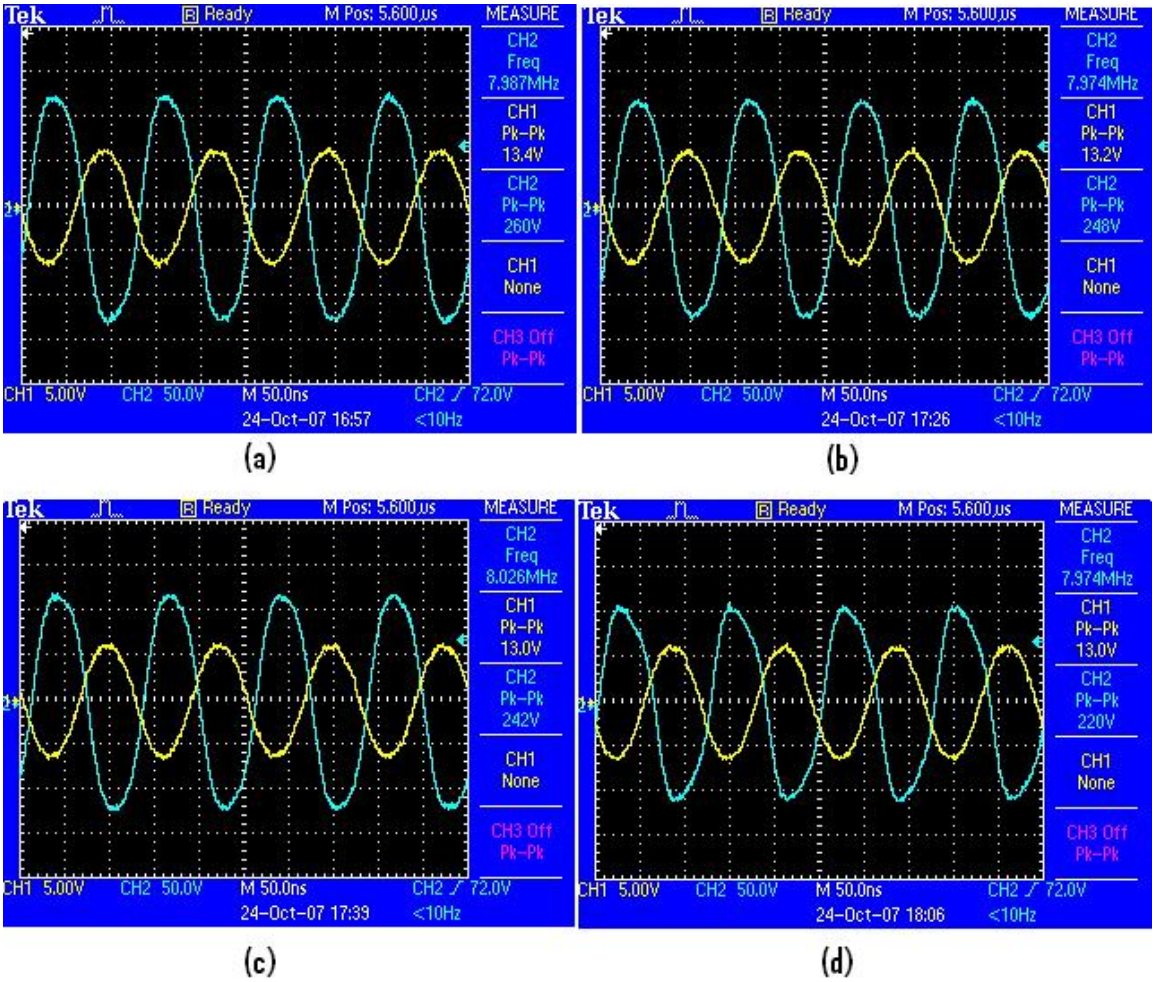


Figure 4.53: Vi (ch1) and Vo (ch2), (a) One pulse, (b) DC=4.6%, (c) DC=8.5%, (d) DC=12.8%

The table above shows:

- No voltage is degraded after each test.
- Max duty cycle tested is 12.8% it is better than specification 10%.
- Test results are repeatable.
- Vo and Idq drop is due to PS voltage dropped (24 V to 16 V) at DC=12.8%. PS current reaches max limit.
- Idq is stable and at expected level. Idq is 13.8 A each side.
- Vi is always about 13.0 V.

In summary, the duty cycle test is OK.

4.4.11 Robustness test with 3 dB ATT plus Mole

The Robust test is to test the ability of the DUT to handle the load VSWR. The output voltage of the DUT on 50 ohm load is checked before and after connecting the DUT to an NMR probe. Mole is use as an NMR probe here. Frequency is swept around the resonant frequency of the Mole to find the highest risk frequency. The test starts from lower output power to full power. An

ATT is inserted between the output of the DUT and the Mole to reduce the equivalent load VSWR of the DUT. The higher the ATT value, the lower the risk of the DUT will be. But output power will be reduced a lot if a too high value of ATT is used. The goal is to find the trade off point. The test starts from 3 dB. Test settings are as shown in the Figure 4.54. The dish with red color is the Mole.

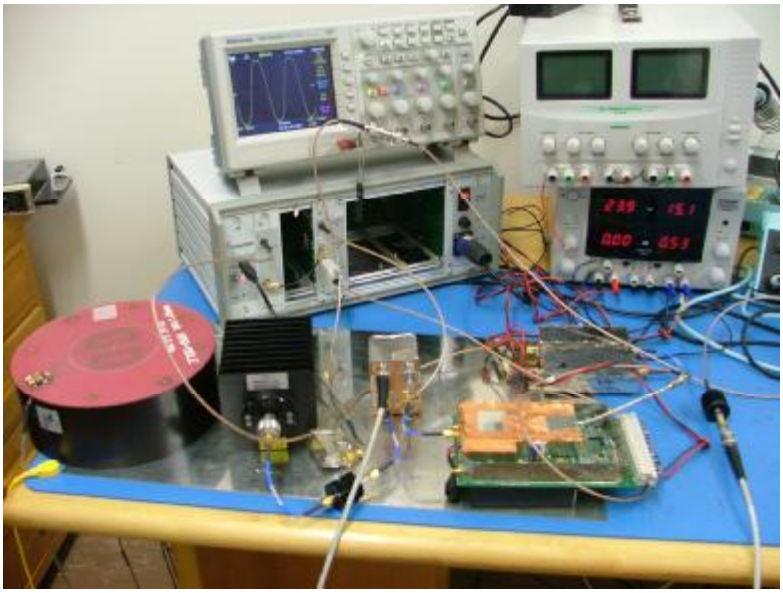


Figure 4.54: DUT and test system

Software of Prospa, called frequency sweep, is used. It is shown in the Figure 4.55.

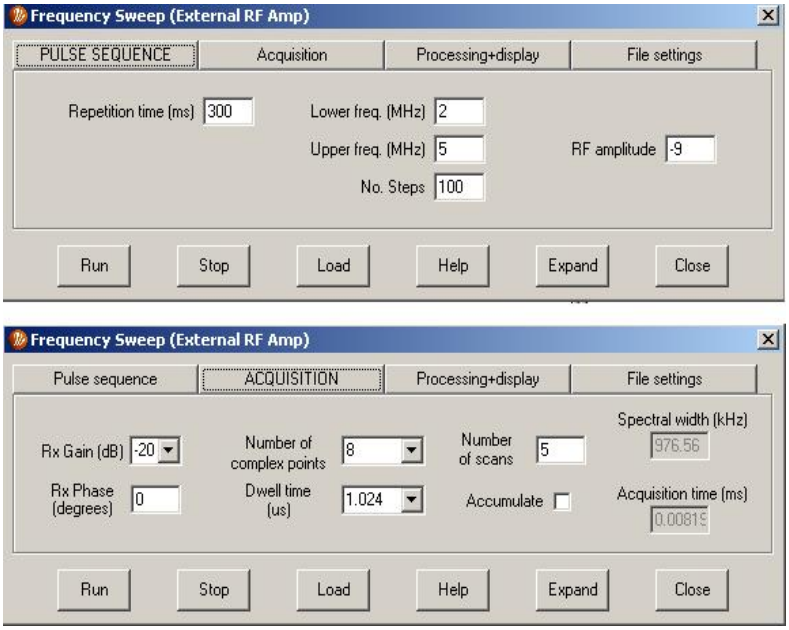


Figure 4.55: SW used and setting

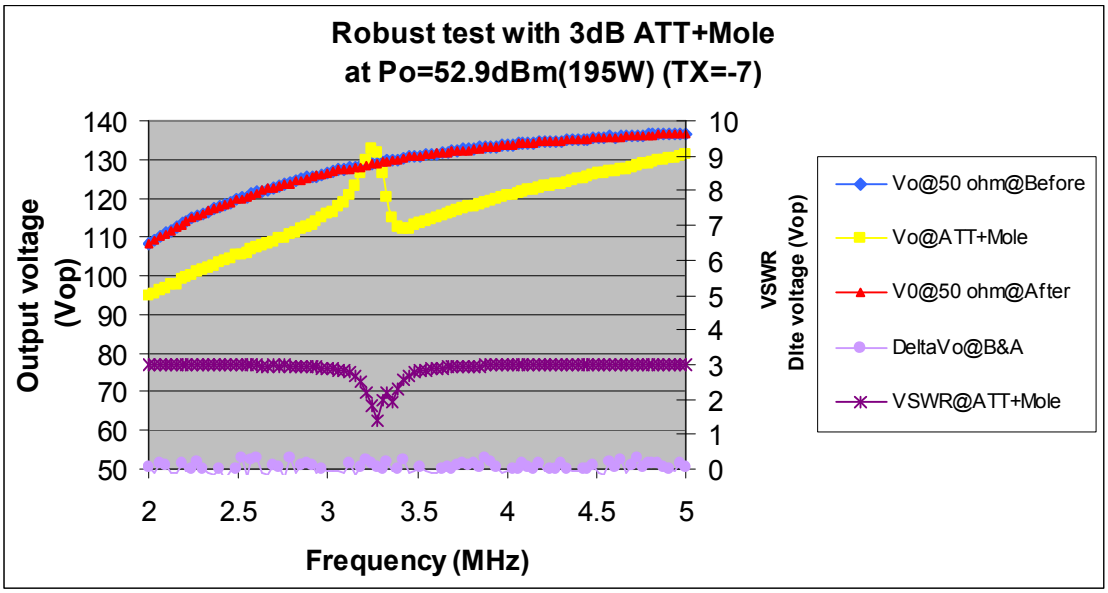


Figure 4.56: Robust test at 195 W

The figure above shows that the DUT withstands the Mole at 195 W output power if a 3 dB ATT is inserted between them. The real power on the Mole is half of 195 W. It is 97 W. Next the ATT value can be reduced further.

4.4.12 Robust test with 1.5 dB ATT plus Mole

To increase output power, the ATT value is changed from 3 dB to 1.5 dB. It will increase the risk of damaging FET.

The 1.5 dB ATT is built with three 680/10/680 ohm resistors (680 ohm, 10 ohm and 680 ohm) under pie type attenuator in a shielding box.

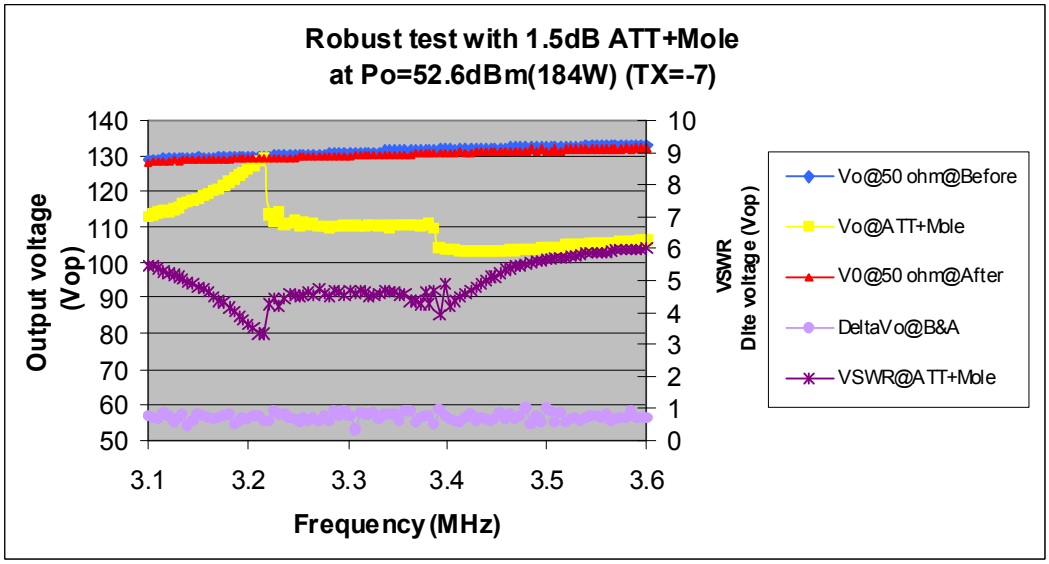


Figure 4.57: Robust test at 184 W

The figure above shows that the DUT withstands the Mole at 184 W output power if a 1.5 dB ATT is inserted between them. The real power on the Mole is 130 W. We don't want to reduce the ATT value further for safety reasons. If the ATT is 1.5 dB, the equivalent Load VSWR is less than 7:1. As we know, FET BLF248 can handle max load VSWR of 50:1. This method keeps the load VSWR of the DUT in the safe zone, so that the robustness of the HPA is guaranteed. On the other hand, 130 W output power is more than the 100 W of the specification.

If the DUT starts from a cold condition, the output voltage will be 10% higher than one at hot condition. This will affect accuracy of the robust test.

To avoid cold start effect, run 10% duty cycle with N=1e5 10 time first at TX=-15. The SW and settings are shown in the figure below.

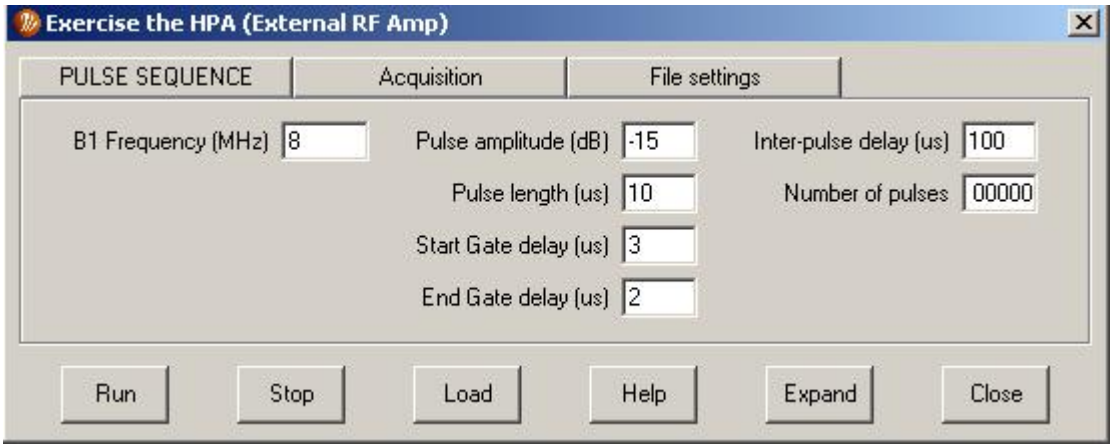


Figure 4.58: Warm up HPA setting

In summary, the HPA is robust.

4.5 NMR experiment

4.5.1 Noise of power supply vs. NMR experience

Boost is supplied by a switch mode DC-DC regulator. It converts 24 V to 8 V. It is more efficient than a linear regulator but a disadvantage is high ripple: 40-80 mVpp. As a reference, ripple of a linear regulator is about 10 to 20 mVpp. This switch mode regulator has a frequency of 100 KHz; its 20 times harmonic is 2 MHz, which falls in the operating band of HPA. The question is: does it affect NMR experience?

In theory, if the harmonic frequency is not exactly same as the echo frequency from the NMR sample, it should not affect the NMR experience.

The NMR experience was carried out with a switch mode regulator with frequency 100 KHz and ripple 60mVpp. The NMR result was compared with a linear regulator. No difference was found.

In summary, a switch mode regulator can be used in the HPA if ripple is not more than 60mVpp with 100 KHz switch frequency.

4.5.2 NMR experience

NMR experiences are carried out in Kea NMR spectrometer with this HPA. Sample is water, probe is a new Halbach. Test RF frequency is 12.3 MHz. CMPG and T1 are tested. The results shown in the Figure 4.59, Figure 4.60 and Figure 4.61 are very good.

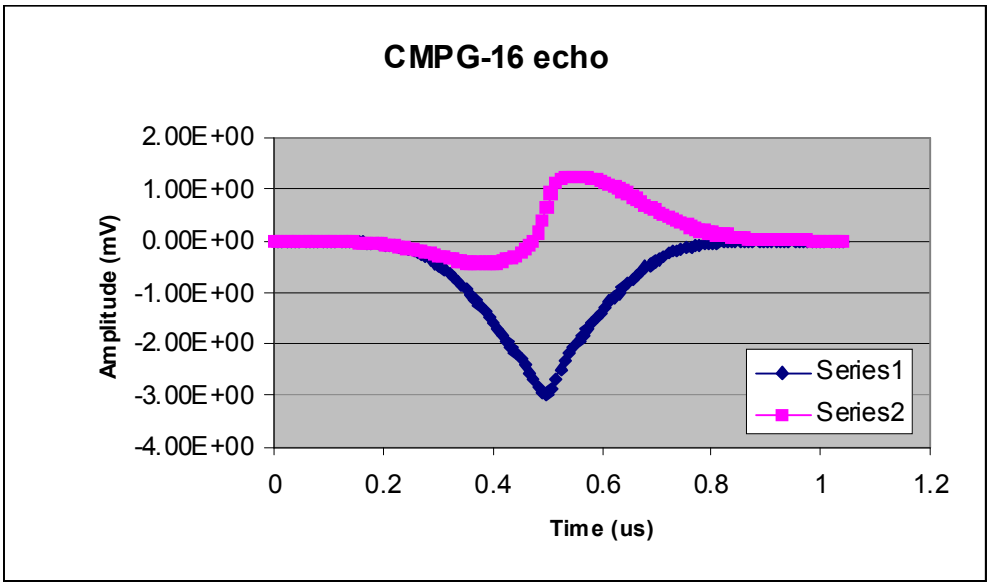


Figure 4.59: CPMG-16 echo, 12.3 MHz, new Halbach 1#, 1# HPA R3.0

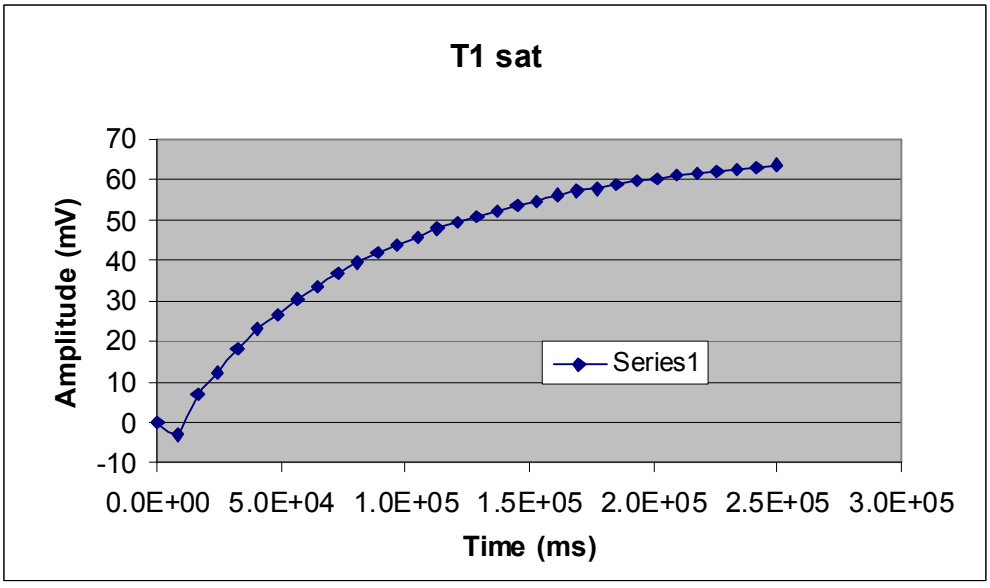


Figure 4.60: T1 sat, 12.3 MHz, new Halbach 1#, 1# HPA R3.0

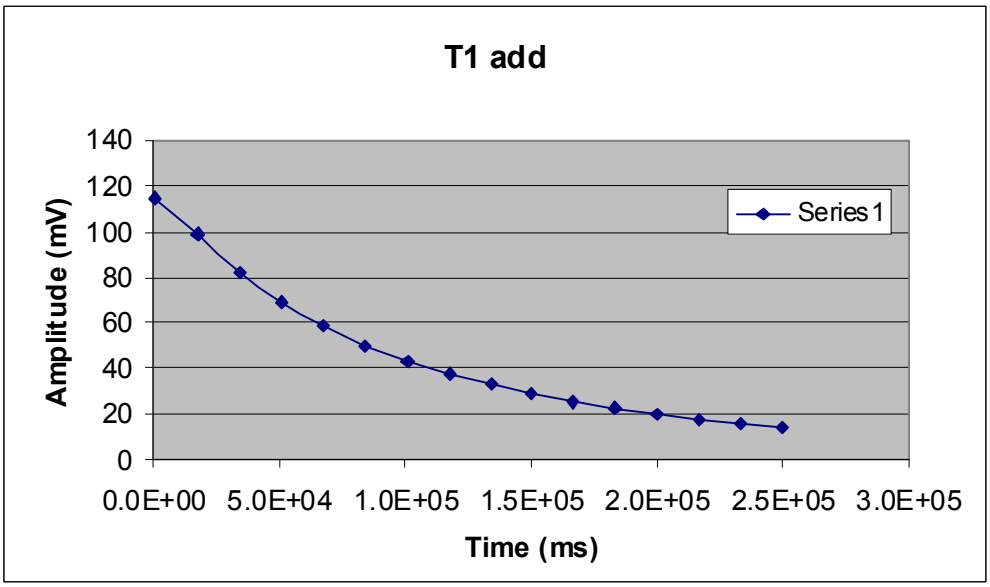


Figure 4.61: T1 add, 12.3 MHz, new Halbach 1#, 1# HPA R3.0

4.6 Summary

The test results from the sections above are very good. They are as expected and agreed with the simulation results. These test results are stable and repeatable.

5 CHAPTER FIVE

SUMMARY OF RESULTS AND DISCUSSION

5.1 Feedback

To minimize the changing of output and input impedance of the final stage and to have flat gain across the band, the negative feedback technology was used. This allows the circuit to be very stable.

A SRCL branch is crosses between the gate and drain of the FET. A resistor, an inductor and a capacitor are in series to build a SRCL branch.

The feedback level depends on resistance. The higher resistance is, the less feedback is. The capacitor is a DC block capacitor. The low side cutoff frequency of feedback depends on the value of the capacitor. When the frequency is lower than the cutoff frequency, the feedback circuit doesn't work. The frequency response of high frequency depends on the inductance. The higher inductance is, the less feedback is at high frequency.

On the other hand, feedback improves stability and gain flatness at the cost of reducing gain. 24 dB gain is a trade off between them.

Negative feedback will increase rise time because it reduces the response speed.

5.2 Hard bias and combination of hard bias and feedback

Feedback will improve stability of high frequency but it increases rise time. To improve rise time and stability at lower frequency, hard bias technology is used.

The solution of hard bias is putting a lower resistor, say 18 ohm, between the gate of the FET and ground without any DC block capacitor. It lets the impedance remain at 18 ohm when frequency is down to DC. As a reference, if a DC block capacitor is in series with a resistor, input impedance of lower frequency will be high and it will cause instability at lower frequency.

The principle behind hard bias reducing rise time is that hard bias reduces the gate voltage changes caused by negative feedback.
The principle that hard bias improves low frequency stability is that if there is no DC block capacitor, the gate impedance will remain at 18 ohm while frequency is down to DC.
So the best solution is a combination of hard bias and negative feedback.
As a result, rise time is about 2 μs with stable HPA if an 18 ohm shunt resistor is used across the gate and ground.

5.3 ATT to reduce equivalent load VSWR

To protect expensive RF power FET in the last stage, an attenuator (ATT) is inserted between the NMR probe and the output of the HPA.
The principle is that ATT works as an isolator between the HPA and the NMR probe to reduce the reflection power. For 1 dB ATT, reflection power is reduced 2 dB. For 3 dB ATT, reflection power is reduced 6 dB.
The risk of damaging the FET is a function of load VSWR. The higher the load VSWR, the higher is the risk of damaging the FET. Load VSWR should be under 10:1 for safety. 1.5 dB ATT gives max load VSWR 7:1. It protects the FET.
On the other hand, ATT reduces output power. The higher the ATT, the lower is the output power.
Trade off ATT values is 1.5 dB. It reduces 3 dB reflection power to keep output VSWR under 7:1. Output power reduces 1.5 dB. This means that if output power of the HPA is 180 W, real power on the NMR probe is 140 W.

5.4 Real NMR probe as a load of HPA

To design a stable HPA, it is not enough to use only 50 ohm as a load. A real NMR load has to be used as a load of the HPA.
The principle of designing a stable HPA is using a method of designing an oscillator to check if there is any oscillation. Because the type of load of the HPA depends on the customer, it is typically a narrow band resonator as an NMR probe rather than a 50 ohm load. Generally speaking, a resonance load gives more risk for oscillation.
At the interface of the NMR probe and output of the HPA, the load reflection coefficient and source coefficient are checked. If the product of these is -1, oscillation will occur. Otherwise the HPA is stable. In this way, the oscillation frequency will be found.
If there is an oscillation, the circuit should be modified to get rid of it. The normal way is to increase the input attenuation, increase the output attenuation of the final stage and increase negative feedback.

This check should be carried out at different frequencies across the band and with different NMR probes.

6 CHAPTER SIX

IMPROVEMENT OF DESIGN

6.1 Reduce power consumption by a pulse drive stage

The current drive stage is a CW mode amplifier. Power consumption is about 4 W. It is very important to look into different techniques to reduce its power consumption.

A solution is using pulse bias at the drive stage. If Idq is 1 A and voltage is 24 V, the power consumption is 2.4 W at 10% of the duty cycle. In this way, power consumption is a function of duty cycle. Power consumption is much lower if the duty cycle is less than 10%.

Philips BLF245B push-pull FET is a good choice for drive stage. It is easy to realize gate blanking. This is also a robust device.

If both the drive stage and the final stage use gate blanking, the total output spike comes from the final stage and the drive stage. To reduce the spike contribution of the drive stage, two approaches can be used. One is tuning its symmetry to minimize its spike. Another is using a second gate blanking control line to control the drive stage separately. Its starting time is earlier than the starting time of the final stage. Its stop time is later than the stop time of final stage. As a result, the spike of drive stage can't passed to output.

6.2 Temperature compensation in biasing

Output RF power of the HPA will drop about 10% with long period pulse. The reason is that junction temperature of the FET is increased.

The solution of keeping constant RF power is by changing the bias voltage. When junction temperature increases, the gate voltage needs to increase to compensate for output power dropped.

A temperature sensor and action circuit will be used for this purpose. The sensor should be placed at close to the FET.

6.3 LED indication

To let the customer know the status of the HPA, some LEDs on the front panel are needed. There are 4 LEDs in the current version. One is for DC power supply indication. A second one is for over temperature indication. A third one is for over drive. The fourth one is for over pulse width. For over drive indication, RF voltage detection, amplifier and some more electronic circuits are needed. For over pulse width indication, pulse width detection, amplifier circuit are needed. A sound warning device can be used to improve the warning effect. A manual reset will be used to reset the HPA to minimize the risk of damaging the HPA.

7 CHAPTER SEVEN

CONCLUSION AND FUTURE WORK

Using a portable NMR spectrometer is a very important and useful method to inspect material in a non-invasive and non-destructive way.

A portable NMR needs high power because the probes usually have a low quality factor.

In this thesis a high power pulse RF HPA is developed in an innovative way. The focus is on robustness and stability.

For robustness, there are two solutions. First rule of thumb, choose a suitable high power FET! The best frequency for the device should be one that is close to our operating frequency. A creditable device vender should also be chosen. The device should have a high max load VSWR. Second, a lower value ATT should be inserted between the NMR probe and the output of the HPA to reduce equivalent load VSWR.

For stability, Class A has been chosen; an amplifier with negative feedback is used.

For low spike, a push-pull circuit is used. Bias current is tuned for each side of the FET to allow circuit symmetry.

To protect against overloading the amplifier: ATTs are used at the input of the HPA and after the pre-drive stage. A drive stage with lower saturated power is also used.

For design technique: hard bias is used for low frequency stability. The issue of rise time and stability are solved by a combination of hard bias and feedback.

Oscillation has been checked when HPA is terminated with a NMR probe.

RF computer simulation is used in the development of the HPA design.

There is a good agreement between simulated results and experimental results.

Good NMR data is gained by using this HPA.

The HPA can be improved further by increasing the output power and reducing power consumption.

This design method can be used in an NMR HPA at other frequency bands (say 100MHz, 500MHz, or 800MHz) and higher output power (say 2KW).

Three prototypes have been built and tested. Performances of all of them are good and same. Repeatability is good. One of HPA is shown in Figure 7.1.

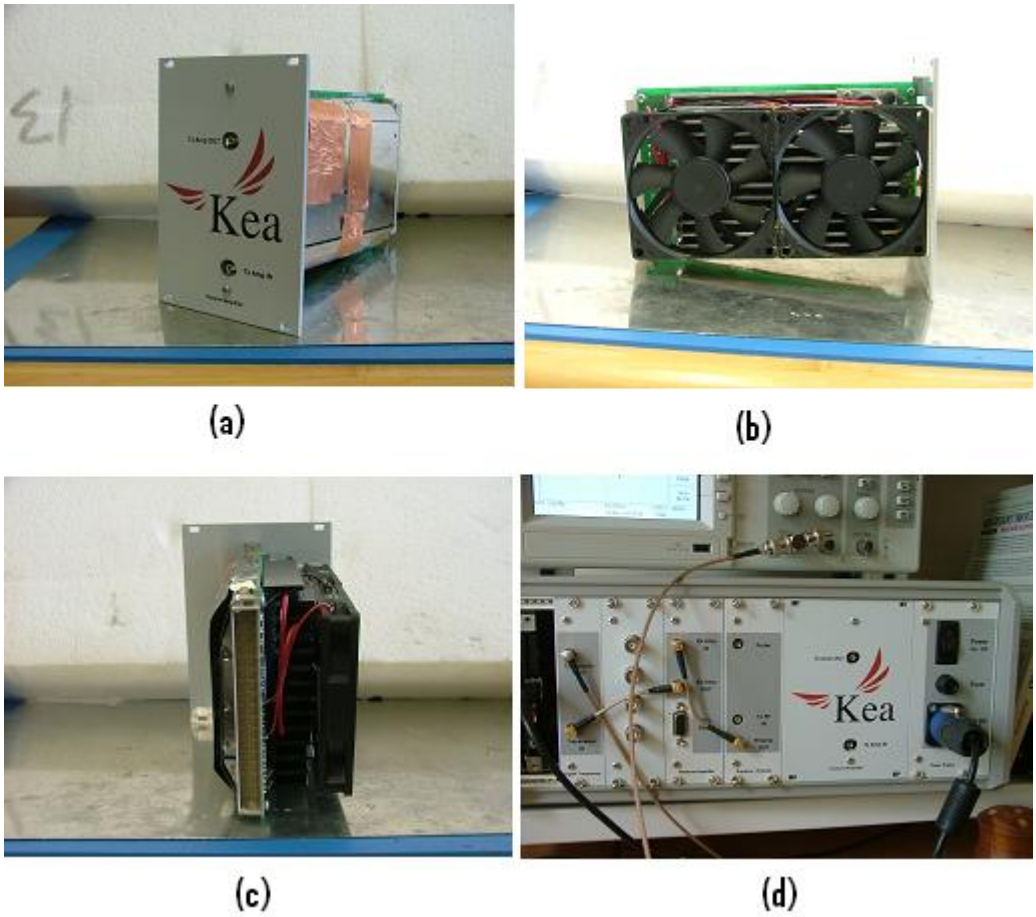


Figure 7.1: (a), (b) and (c) HPA, (d) HPA in Kea NMR spectrometer

8 REFERENCES

[1] RICHARD W. QUINE, GARETH R. EATON, SHANE DILLON, " Fast-Response VHF Pulsed 2 KW Power Amplifier", Concepts in magnetic Resonance Part B (Magnetic Resonance Engineering), Vol. 29B(4) 185-190, 2006

[2] STEVE C. CRIPPS, "RF Power Amplifiers for Wireless Communications", Norwood, MA: Artech House, P56, P179, P315, 1999

[3] Jerry Sevick, W2FMI, "Transmission Line Transformers", Atlanta, GA: Noble publishing, 1996

[4] Hewlett Packard, "HP85148A Circuit Envelope Simulator", user's manual, 1995

[5] Mike Golio, "The RF and Microwave handbook", Danvers, MA: CRC press, 2001

[6] Nick Pothecary, "Feedforward Linear Power Amplifiers", Norwood, MA: Artech House, P5, 1999

[7] Edmar Camargo, "Design of FET frequency Multipliers and harmonic Oscillators", Norwood, MA: Artech House, P37, P75, P104, 1998

[8] Peter B. Kenington, "High-Linearity RF Amplifier Design", Norwood, MA: Artech house, P91, 2000

[9] Robin Dykstra, "The development of a portable Earth's field NMR system for the study of Antarctic sea ice", A thesis for degree of Master of Science in Electronics at Massey University, Library of Massey University, 2001

[10] Ir. Dominique Schreurs, "Nonlinear measurements and modeling", 1999 IEEE MTT-S International Microwave Symposium, Nonlinear Modeling and Characterization of Microwave Devices of Workshop, 1999

[11] Pengcheng Jia, Lee-Yin Chen, Angelos Alexanian, Robert A. York, "Broad-Band High-power Amplifier using Spatial Power-combining Technique", IEEE Transactions on Microwave Theory And Techniques, Volume 51, Number 12, December 2003

[12] Roy Hejhall, “RF Small Signal Design Using Two-port Parameters”, AN215A, RF Device Data, Volume II, Motorola, 1991

[13] Glenn Young, “Microstrip Design Techniques for UHF Amplifiers”, AN548A, RF Device Data, Volume II, Motorola, 1991

[14] Lou Danley, “Mounting Stripline-opposed-emitter (SOE) Transistors”, AN555, RF Device Data, Volume II, Motorola, 1991

[15] Frederick H. Raab, “Transmitter Technology for the Second Century of Wireless”, 1999 IEEE Topical Workshop on Power Amplifiers for Wireless Communications, University of California, San Diego, 1999

[16] Walter R. Curtice, M. Ettenberg, “A Nonlinear GaAs FET Model for use in the Design of Output Circuits for power Amplifiers”, IEEE TRANSACTIONS ON Microwave Theory and Techniques, Vol. MTT-33, No. 12, December 1985

[17] Masatoshi Nakayama, “An Amplitude and phase Linearizing Technique for Linear power Amplifiers”, Microwave Journal, March 1996

[18] David Dening, “Setting Bias points for linear RF Amplifiers”, Microwave & RF, July 2002

[19] Douglas A. Teeter, jack R. East, George I. Haddad, “Use of Self Bias to Improve Power Saturation and Intermodulation Distortion in CW Class B HBT Operation”, IEEE microwave and Guided Wave Letters, Vol. 2, No 5, May 1992.

[20] Raymond Basset, “high-Power GaAs FET Device Bias Considerations”, www.fcsi.fujitsu.com

[21] Matthew Fivash, “Dissipative Filters”, Filter handbook Volume 1 – Applications, A collection from RF design, Englewood, Colorado, 1991

[22] John H. Broxon II and Douglass K. Linkhart, “Twisted-wire Transmission Lines”, RF Design, June 1990

[23] Hakan Turkoz, Yilmaz Oktay, “High-Speed microprocessor Controlled Antenna Matching init”, A Collection from RF Design, Englewood, Colorado, 1991

[24] Roderick K. Blocksome, “Predicting RF output Power From Combined Power Amplifier Modules”, A collection from RF Design, Englewood, Colorado, 1991

[25] Daniel Myer, “RF power Amplifiers in MRI”, A Collection from RF Design, Englewood, Colorado, 1991

[26] VSWR protection of Solid State RF Power Amplifiers”, A Collection from RF Design, Englewood, Colorado, 1991

[27] Helge Granberg, “Biasing Solid State Amplifiers to Linear operation”, A Collection from RF Design, Englewood, Colorado, 1991

[28] H.O. Granberg, “Good RF Construction Practices and Techniques”, A Collection from RF Design, Englewood, Colorado, 1991

[29] H.O. Granberg, “New MOSFETs Simplify High power RF Amplifier Design”, A Collection from RF design, Englewood, Colorado, 1991

[30] BLF248 Datasheet

[31] BLF245B Datasheet

[32] SR401 Datasheet

[33] L88016 Datasheet

[34] SR704 Datasheet

[35] SX601 Datasheet

[37] TC2426 gate bias drive Datasheet

[38] SGA7489 Datasheet

[39] L221P Datasheet

[40] Thermal Switch Datasheet

[41] Switch mode voltage regulator Datasheet

[42] Linear mode voltage regulator Datasheet

[43] Core BN-61-002 Datasheet, Amidon

[44] Core BN-43-202 Datasheet, Amidon

[45] Core BN-73-202 Datasheet, Amidon

[46] Core FT-37-XX Datasheet, Amidon

[47] 

[48] Hittite, NMC482ST89 datasheet, www.hittite.com

[49] Pieter L. D. Abrie, “Design of RF and Microwave Amplifiers and Oscillators”, Boston: Artech House, 1996

9 FULL FORM OF ABBREVIATED TERMS IN THE THESIS

A	
ADS	advance design system
AGC	automatic gain Control
AM	amplitude modulation
AM-AM	amplitude modulation-amplitude modulation conversion
AM-PM	amplitude modulation-phase modulation conversion
ATT	attenuator
ATTEN1	attenuator two
ATTEN2	attenuator one
B	
BJT	bipolar junction transistor
C	
CVDMOS	N-channel enhancement metal oxide semiconductor
CW	continuous wave
D	
2.5D	two and half dimension
3D	three dimension
dBm	unit for signal level, dB relative to 1 mW power
dB	decibal
DC-DC	direct current-direct current conversion
DDC	double directional coupler
DSP	digital signal processor
DC	direct current
DDS	direct digital synthesis
DUT	device under test
E	
ESD	electrostatic discharge
F	
FET	field effect transistor
Fwd	forward
G	
GB	gate blanking

GHz	billion herts
H	
HF	high frequency
HPA	high power amplify
HSL	high side limit
I	
IMD	Inter-modulation Distortion
J	
K	
Kea	the name of a kind of bird lived in New Zealand, here it is a brand name Of a kind of NMR spectrometer of Megritek Ltd
L	
Lapspec	a brand name of the portable NMR spectrometer produced by Magritek Ltd
LED	light-emitting diode
LC	inductor and capacitor
LDMOS	lateral double diffuse metal oxide semiconductor
LHS	left hand side
LNA	low noise amplifier
LSL	low side Limit
LSSP	large signal S-parameter
M	
MHz	Mega hertz
MMIC	mono microwave integrated circuit
MOSFET	metal oxide semiconductor field effect transistor
MUT	module under test
N	
NMR	nuclear magnetic resonance
P	
PP	push-pull
PRL	parallel resister and inductor
PS	power supply
PC	personal computer
PCB	printed circuit board
R	
Rev	reverse
RHS	right hand side
RL	resister load
RF	radio frequency

RX	receiver
S	
SE	single end
SiGe HBT	silicon-germanium heterojunction bipolar transistor
SPICE	simulation program with integrated circuit emphasis
SRC	series resister and capacitor
SW	software
T	
TDS2024	model number of a oscilloscope
TTL	transistor-transistor logic
TX	transmitter
V	
VHF	very-high frequency
VDMOS	vertical planar double diffused Metal oxide semiconductor
VSWR	voltage standing wave ratio