SCHOOL OF ENGINEERING AND ADVANCED TECHNOLOGY

Improved Control System for Dual Input-Dual Output DC-DC Converter

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Abstract

This thesis aims to propose a new control system of dual input dual output DC-DC converter by proposing the advanced fuzzy PID control system. The fuzzy PID controller is a type of intelligent control system being practically applying fuzzy logic theory. Compared with conventional control system, a properly designed fuzzy PID control system is more accurate, sensitive to input, robust to noise, large bandwidth, faster speed and constant oscillation. Therefore, the analysis of improved control system for dual input dual output DC-DC converter, comparison with conventional PID controller, and evaluation are the main focus of this thesis.

The improved control system for dual input dual output DC-DC converter is based on the PID control method and fuzzy logic theory. By the combination of conventional PID controller and fuzzy control theory, the advanced controller with human intelligence is produced. Fuzzy PID control method uses the present error E and EC, combined with the dynamic characteristics of controlled object and practical experience. According to the requirements and target functions, three parameters of PID controller are tuned online by fuzzy rules inference.

Simulation using MATLAB and SIMULINK and implementation with STM32f407 are presented. The optimization of improved control system for dual input dual output DC-DC converter is also studied.

Acknowledgment

There are many people whom I am very thankful to during my Master study in the past one year. They have significantly helped me in numerous ways that have enabled this thesis to be presented.

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Abbreviation List

PV	photovoltaic
PID	proportional–integral–derivative controller
FPGA	field-programmable gate array
DCS	distributed control systems
PLCs	programmable logic controllers
VSLI	very large scale integrated
PWM	pulse-width-modulated
ARM	advanced RISC machine
MCU	microprocessor control unit
ZVS	zero voltage switching
DCM	discontinuous conduction mode
ZCT	zero current transition
ZCS	zero-current-switching
EMI	electromagnetic interference
SIDO	single-inductor dual-output
DISO	dual input-single output
MIMO	multi input-multi output
SISOC	single-input single-output converter
DOC	dual-output converter
DIC	dual-input converter
MI	multi input

SQP sequential quadratic programming

CCM continuous conduction mode

GPIO general-purpose I/Os

LSIRC low-speed internal RC

LSE low-speed external

DMA direct memory access

ADC analog to digital conversion

USART universal synchronous asynchronous receiver transmitter

Chapter 1 Introduction

1.1 Research Background

Power supply is a practical technology used to build and operate electronic circuits and systems, which can be classified by the following categories as shown in Fig. 1.1. All kinds of the active electronic circuits need power supplies. Power electronics DC-DC converters is concerned with the processing electrical power using electronic devices, which have been widely used in many applications, like solar energy harvesting system, electric vehicle, biomedical implants, aircraft, satellite communication equipment, DC motor and portable electronics. In a DC-DC converter, the dc input voltage is converted into dc output voltage with a large range of magnitude, low ripple voltage, or opposite polarity. Researchers are doing research to enhance the stability, reliability, efficiency of the converters. Many topologies have been proposed to reduce the cost and components and keep these improved performances of the overall system.

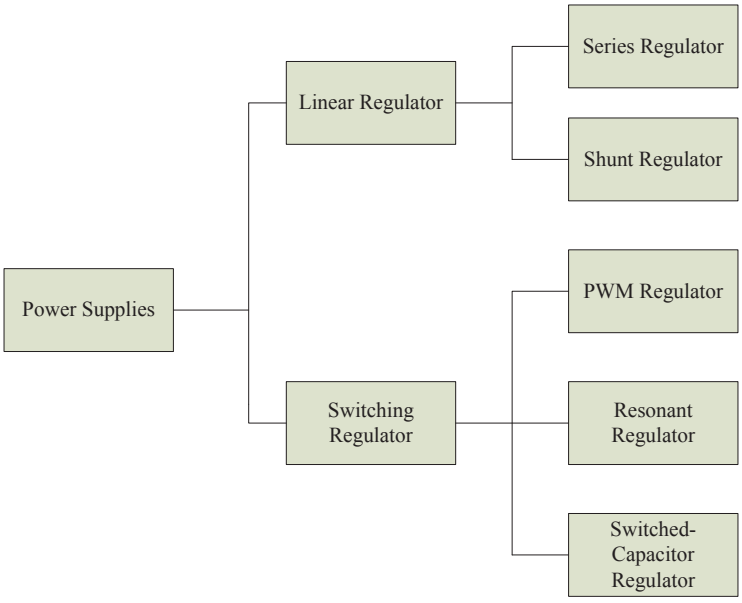

Fig. 1. 1 Classification of power supplies

The renewable energy such as photovoltaic (PV) energy and wind energy has created various electric energy sources with different electrical characteristics for the modern power system [1-

6]. In order to gain higher energy conversion efficiency, the solar cell array for PV energy prefers a parallel-connected structure to form a low-voltage source.

A lot of research [7-12] has gone to analysis, modeling, and utilizing multi-input converters in applications such as grid-connected integrated hybrid generation systems, fuel cells, micro-grid-based telecom power systems, uninterruptible power supplies, and electric and hybrid electric vehicles

1.2 Application

Nowadays, hybrid energy system is more and more popular in power electrics field, especially multi-input multi-output DC/DC converters, for they provide interface of various renewable energy sources and deliver regulated power to several loads. The energy sources like battery, fuel cells, ultra-capacitor, and renewable energy source, wind and solar photovoltaics panel (PV) can be used as input voltage source. The whole system can be more compact packaging and centralized control.

Automatic control in electrical engineering and technology is a widely used term covering a large range of industrial applications in mechanism and electrical equipment. A proportional–integral–derivative controller (PID controller) is the most practical control system in automatic controllers. PID controllers have their origins in 19th century speed governor design [13, 14]. The theoretical basis for the operation of governors was first described by James Clerk Maxwell in 1868, but it was not until 1922 that PID controllers were first developed using a theoretical analysis, by Russian American engineer Nicolas Minorsky for automatic ship steering. The Navy ultimately did not adopt the system, due to resistance by personnel. Similar work was carried out and published by several others in the 1930s. One of the earliest examples of a PID-type controller was also developed by Elmer Sperry in 1911. In recent years, electronic controllers have largely been replaced by digital controllers implemented with microcontrollers or field-programmable gate array (FPGA) [15], which implement PID algorithms. However, analog PID controllers are still used in niche applications requiring high-bandwidth and low-noise performance, such as laser-diode controllers. Most modern PID controllers in industry are

implemented in Distributed Control Systems (DCS), programmable logic controllers (PLCs) or micro digital controller. Software implementations have the advantages, because they are relatively cheap and flexible with respect to the implementation of the PID algorithm.

Applications of fuzzy logic is, automatic control system, prediction, diagnostic and advisory systems, user interface and neural language processing, domestic appliances and embedded systems, soft computing and hybrid systems with artificial neural networks, Very Large Scale Integrated (VSLI) circuit micro controller, and fuzzy expert system and fuzzy interface.

1.3 Research Methodology

1. Literature review

Review literature in this area and write summery to classified the current control methods and analyze their advantages and disadvantages.

2. Design the control system and calculate the parameters

This dual input-dual output converter includes several MOSFET in time series, so pulse-width-modulated (PWM) gate drive waveform and two feedback loops have to be well-designed. Use the improved PID controller as the compensator to ensure the stability of the output in different operating modes. The practical implementation of PID compensator with op-amp is shown in Fig. 1.2, and the total loop transfer function is,

$$G(s) = -\frac{R_3}{R_1}\frac{(1+1/s\,R_3C_3)}{(1+sR_3C_2)}\frac{(1+sR_1C_1)}{(1+sR_2C_2)} = G_{CM}\frac{(1+\omega_L/s)}{(1+s/\omega_{p1})}\frac{(1+s/\omega_z)}{1+s/\omega_{p2}} \qquad (1)$$

where, $\|G_{CM}\| = \frac{R_3}{R_1}$, $\omega_L = \frac{1}{R_3C_3}$, $\omega_z = \frac{1}{R_1C_1}$, $\omega_{p1} = \frac{1}{R_3C_2}$, $\omega_{p2} = \frac{1}{R_2C_1}$

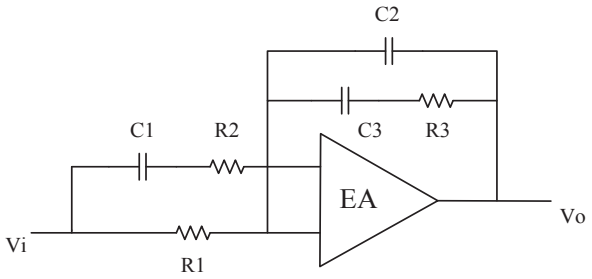

Fig. 1. 2 Practical implementation of PID compensator with op-amp

3. Simulate four different modes of controller

Use MATLAB/Simulink to simulate the whole control system and check the bode plot of gain margin and phase margin to keep control system stable. The total phase shift is less than 360° at the crossover frequency where the total gain is 1 or 0 dB.

4. Implementation

Choose suitable Advanced RISC Machine (ARM) Cortex Microprocessor Control Unit (MCU) from STM32 serial to program and build the controller according to the requirements of converter. The accuracy must within 5% and the switching frequency is 100 kHz.

5. Setting different values in practical range and test the accuracy

Record the test data to verify the accuracy and respond of the whole control system. Compare the improved controller with the conventional controller and analyze the different performance between them.

6. Writing thesis

Summarize the research progress, theoretical analysis, simulation results, programming code and hardware implementation.

1.4 Objectives of the Thesis

The objectives of the thesis are to propose the improved control system for dual-input dual-output DC/DC converter with fuzzy logic theory. Make comparisons between conventional PID control system and proposed fuzzy PID control system to analyze centralized control and get

better performance. Analysis and evaluation of the operational principles, mathematical inference, simulation, implementation by micro controller, and experimental design are also presented.

1.5 Thesis Organization

The thesis is organized in following order,

Chapter 1 presents research motivation, application, methodology, objectives, and the outline of this thesis.

Chapter 2 reviews the literature on the recent development of multi-input DC-DC converters and control systems, in terms of classification among multi-input multi-output DC-DC converter, various control algorithm and their optimization.

Chapter 3 starts with theoretical analysis of hardware circuit design, basic topology, calculation equations including four operation modes. Then it comes to the control method analysis and small signal modelling to provide an advanced control system for proposed hardware circuit.

In Chapter 4, conventional PID and fuzzy PID controller simulation for four operation modes are proposed using MATLAB. The fuzzy inference modelling is applied to achieve fuzzy PID programming. Comparison between these two controllers is made.

The implementation with STM 32 is studied in Chapter 5. Both of the conventional PID and fuzzy PID are programed and implemented to compare different performance in the dual input dual output renewable energy system.

Chapter 6 analyzes the simulation and implementation results and evaluates both of them.

Chapter 7 concludes the thesis. The major achievement is summarized. Some suggestions for future research are discussed.

Chapter 2 Literature Review

Traditionally, multiple sources are combined with the common DC bus. The separate DC-DC conversion stages are applied for individual sources, and controller has to be provided for each stages independently [16, 17]. In some cases, communication bus is also added for exchange of information between sources [18, 19], which makes the whole system more complicated and bulky.

To overcome these disadvantages, multi-input converters are proposed for their advantages of simpler circuit structure, lower cost and more controllable than several single input converters, which is shown as following Fig. 2.1 The inductor and capacitor are shared by two converters, reducing the passive components. The new topologies of different DC-DC converters aim to cost down and enhance the performance of converters like reliability, efficiency, flexibility, and modularity.

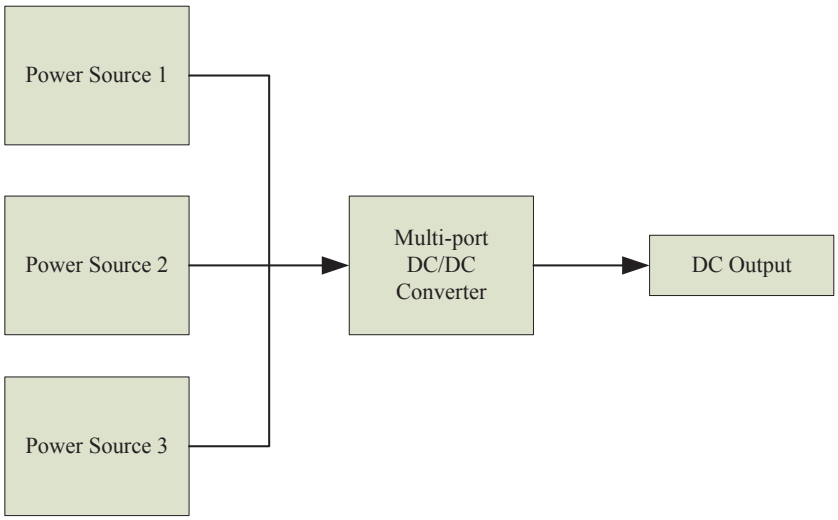

Fig. 2. 1 Structure of conventional hybrid power system

This structure can be treated as a single power converter. Because of its simplicity, convenience and less components, the multi-port converters are widely used in industrial application [20-25].

The multi-port power converter can be divided into two categories, non-isolated and isolated converters. For galvanic isolated converters, isolated transformers are incorporated. Galvanic

isolated are used in high power applications, which isolate the input from any outputs to avoid electric shock hazard and current or voltage rating of semiconductors. All isolated topologies include a transformer, and thus can produce an output of either higher or lower voltage than the input by adjusting the turn's ratio. However, the transformer makes converters bulky and costly. Non-isolated converters are used for devices that do not need galvanic isolation, which makes topologies simple and low cost. They can be used where the galvanic insulation is not required.

2.1 Multi-input Non-isolated DC-DC Converters

The conventional power conversion system combines several single-port structures. The separated DC-DC conversion stages increase the complexity and cost of the whole power system.

Multi-input DC-DC converter is widely used in various applications, like renewable energy system, hybrid vehicles, and portable electronic devices. Most electrical systems are supplied by more than one power sources. For example, PV port acts as the main source and bidirectional battery as back-up source for satisfying the output power requirement. Control systems are designed for maintaining and delivering the regulated voltage or current to load. A number of control theories were proposed. These improved control systems have better performance like efficient identification for non-linear and time-varying dynamic systems, automatically self-tuning characteristic, stability, and robust to noise and disturbance. This paper analyzes some recent development of control systems. The algorithms, methodologies, advantages and disadvantages are studied.

Multi-input PWM dc/dc converter for both high and low voltage sources can draw power from two different voltage sources simultaneously and independently. More than one of these units may be used to improve the performance and efficiency.

2.1.1 Dual Input-Single Output DC-DC Converters

In conventional approaches, two dc voltage sources are connected to two independent dc/dc

power converters to obtain two stable output voltages, and then connected to the dc bus, to provide the electric energy demanded by the load. Fig. 2.2 shows the diagram of high/low voltage sources with two individual dc/dc converters. A control switch has to be provided for each dc voltage source to act as bypass short circuit for input current of other supply. In order to cost down and simplify the topology, the dual-input dc/dc converter, as shown in Fig. 2.3 can be applied. The two dc voltage sources can be connected either in parallel or in series to form an input voltage source to transfer the desired power to the load.

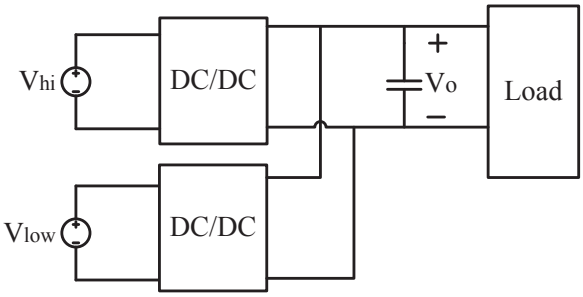

Fig. 2. 2 Structure of conventional hybrid power system

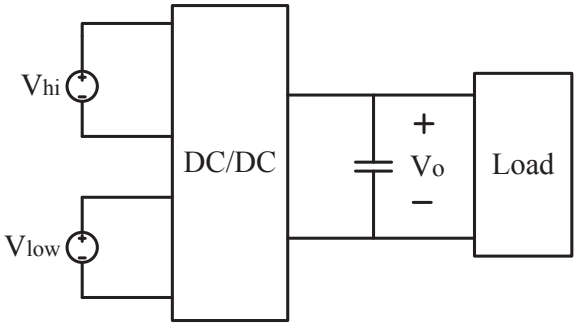

Fig. 2. 3 Structure of dual-input dc/dc converter

Because of the voltage amplitude differences between two dc sources, only one of them can be connected to the input terminal of the dc/dc converter at one time. Because of clamped voltage on the winding of the coupled transformer, the design of controller is based on the time-sharing concept. For that reason, power from different dc sources cannot be transferred to the load simultaneously.

Then, [26] proposes the multi-input dc/dc converter based on the multi-winding transformer with phase-shifted PWM control which can successfully deliver power from two dc sources to the load individually or simultaneously. However, high components cost and relatively

complicated circuit structure is the main drawbacks of the multi-input converters.

According to [27], in order to transfer power individually, each dc voltage source needs a controllable switch to provide a bypass short circuit to deliver electric energy continuously. If one of the dc sources is diminished, it is very difficult to obtain the regulated output voltage, since the input voltage variation is significant.

An innovative double-input PWM dc-dc converter for high/low voltage sources is proposed in [28, 29], which combines buck and buck-boost converter. Without the bypass short circuit, the soft-switching technology is accessible and the magnitude of the input dc voltage can be higher or lower than the one with a regulated output. The topology consists of two input sources, an output voltage, and two power switches are connected to the high-voltage source and low voltage sources respectively. There are four modes, according to the switches status. The topology and waveform are shown as Fig. 2.4 and Fig. 2.5

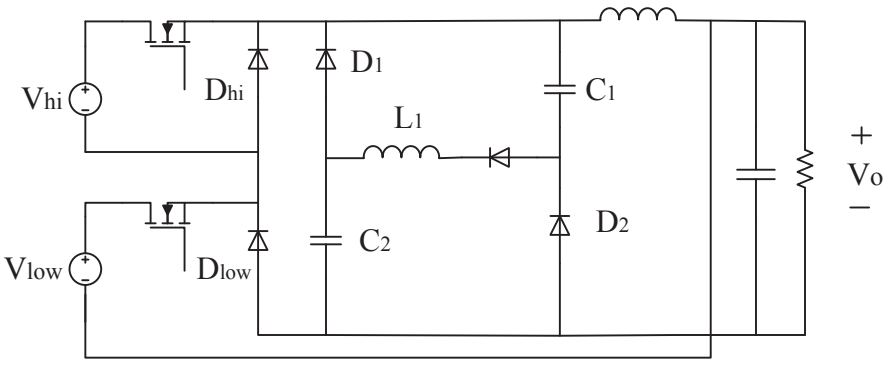

Fig. 2. 4 Structure of innovative dual-input dc/dc converter

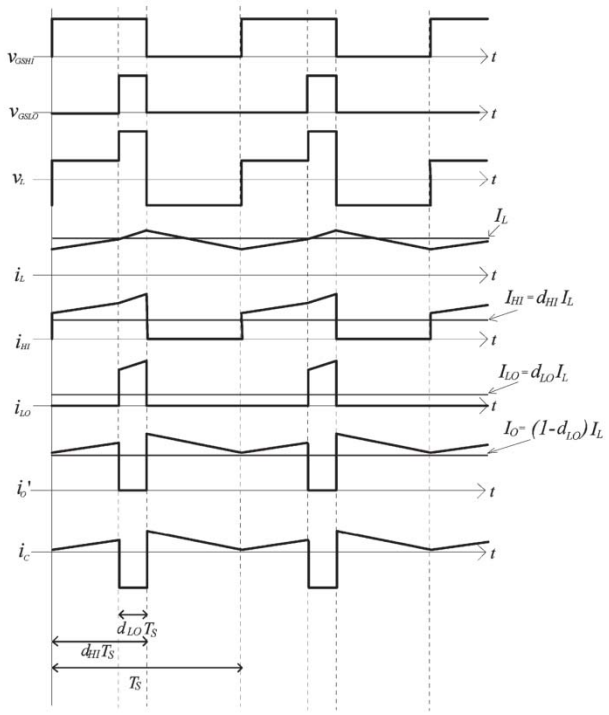

Fig. 2. 5 Waveforms of proposed dual-input dc/dc converter

Since the proposed double-input dc/dc converter has two input sources and one output with a regulated voltage, where the power for each one of them can be either controlled or undetermined, there are three different power status combination cases which can be shown in Table I.

TABLE I THREE DIFFERENT POWER STATUS COMBINATION CASES

Power Status	Case I	Case II	Case III
Low voltage source	undetermined	controlled	controlled
High voltage source	controlled	undetermined	controlled
Load	controlled	controlled	undetermined

Among the proposed topologies, the multi-input converters presented in [30-33]are useful for combining some energy sources, whose power capacity and voltage levels are different to obtain regulated output voltage. The limitation of these topologies is that only one power source is allowed to transfer energy to the load at a time to prevent power coupling effects.

A new topology for dc-dc converter topology is advanced from double input to n-numbered input buck-boost converter in [34, 35] as shown in Fig. 2.6 and Fig. 2.7. It simplifies the structure of converter with fewer components. The proposed topology is capable of energy

diversification among different energy sources with different voltage-current characteristics while achieving low part number and bidirectional operational. It has the advantage that positive output voltage without any additional transformer is capable of bidirectional operation and operates as buck, boost, and buck-boost modes separately, compared to previous multi-input converter. However, it can only operate single direction and only one source can be used to deliver power to load at a time. This topology contains many components which increase the cost, and lead to conduction loss which may decrease the efficiency.

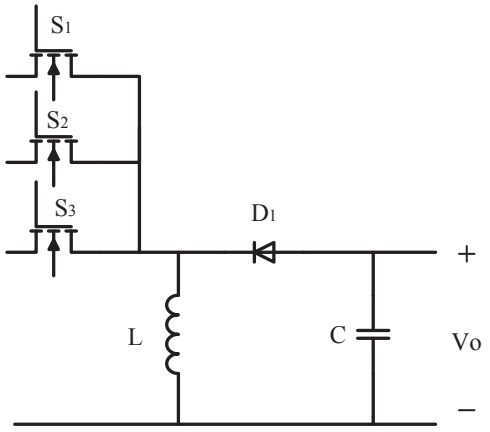

Fig. 2. 6 Structure of n-numbered input dc/dc converter

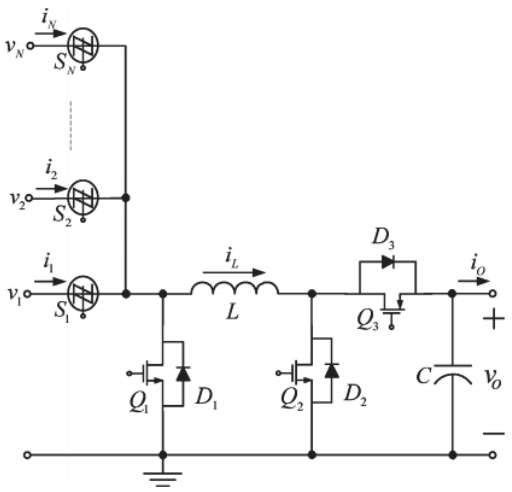

Fig. 2. 7 Topology of unidirectional multi-input buck-buck converter

In order to guarantee load leveling, assuring braking energy recovery and good performances in transient operations, a new conversion structure for bidirectional interfacing of two dc

voltage sources with a higher voltage dc-link has presented [23]. Only three controllable switches in this topology are needed. The limit of this structure is that the sum of the two dc voltages must be lower or equal than the motor drive dc-link voltage. Even though the switching loss is reduced by decrease the number of controllable switches, the overall efficiency of converter is reduced by reverse recovery current as shown in Fig.2.8 and its relationship is shown in Fig.2.9.

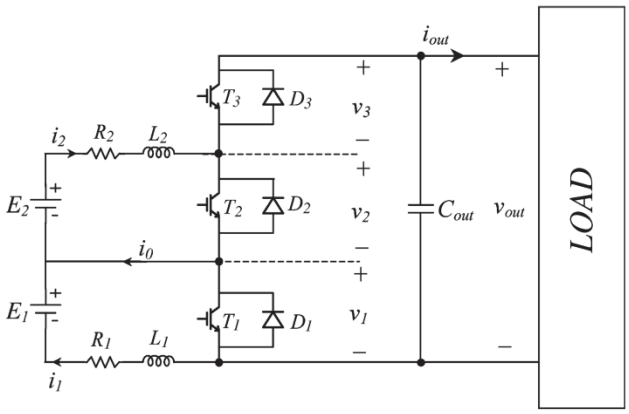

Fig. 2. 8 New boost converter structure

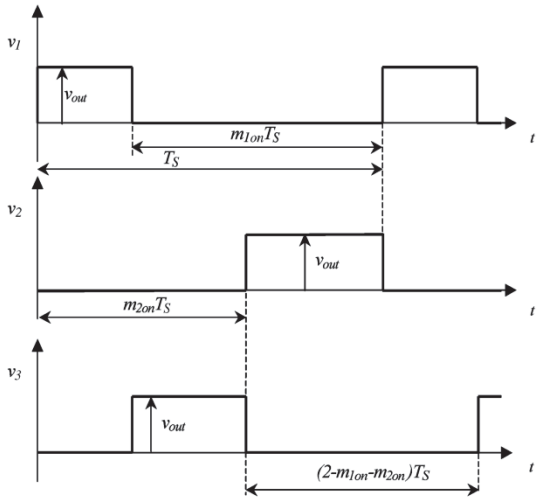

Fig. 2. 9 Relationship between v_1, v_2, v_3 voltages and switch on-duty ratios

A new designed zero voltage switching (ZVS) multi-input converter is proposed to solve efficiency problem in [36]. The converter uses the current sources directly to both inputs and based on the series-connected input circuits and the PWM control signals, the switching loss can be greatly reduced in dual power supply state. This converter can be operated in two modes

and convert two power sources with different voltages to a stable dc-bus voltage. The overall efficiency in both of the single and dual power supply states is higher than 93.8%. Because the auxiliary inductor series connected with a Schottky diode operated in the discontinuous conduction mode (DCM) is utilized for achieving turn on high efficiency ZVS of all switches, as shown in Fig.2.10 and its relationship in both single and dual operation modes are shown in Fig.2.11 and Fig.2.12.

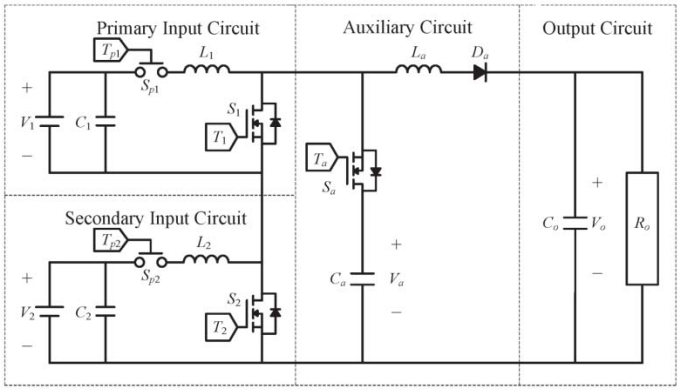

Fig. 2. 10 Circuit topology of high-efficiency multi-input converter

Fig.2.10

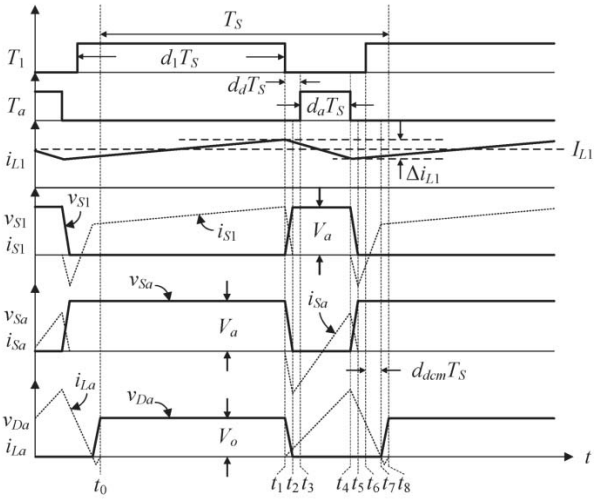

Fig. 2. 11 Characteristic waveforms in single-power-supply state

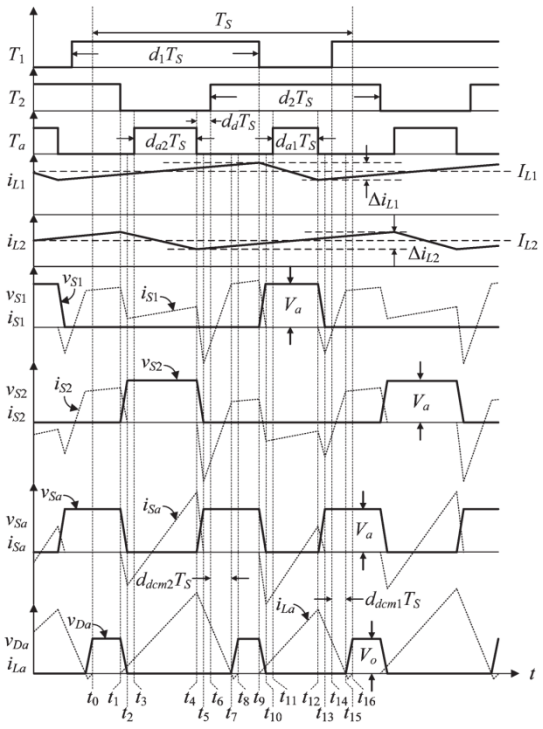

Fig. 2. 12 Characteristic waveforms in dual-power-supply state

The efficiency is increasing in the proposed zero current transition (ZCT) PWM dc-dc converters, without additional current stress and conduction loss on the main switch during the resonance period of the auxiliary cell in [37]. Adding the ZCT technique into boost converter can significantly decreases the conduction loss and current stress. The auxiliary cell is made of a resonant inductor, a resonant capacitor, an auxiliary switch and an auxiliary diode in parallel with the main switch and the zero-current-switching (ZCS) ranges of the main and the auxiliary switch are entirely achieved by operating the auxiliary cell. The efficiency is more than 95% and can be used in high voltage application. However, it still contains some electromagnetic interference (EMI) problems if it is used in non-isolated situation. The topology is shown as Fig. 2.13.

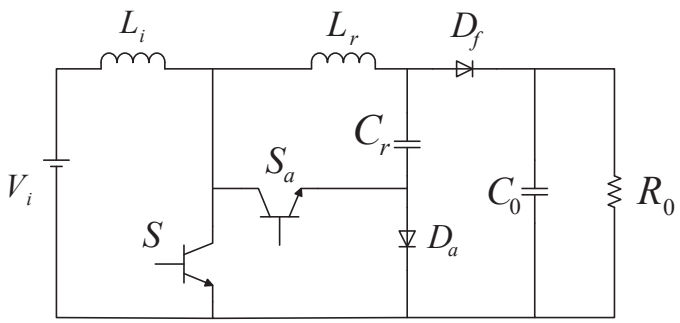

Fig. 2. 13 The PWM dc-dc boost converter with ZCT cell

2.1.2 Single Input-Dual Output DC-DC Converters

Single-inductor dual-output (SIDO) non-isolated DC-DC converters in [38] have been widely used in low power portable devices, like cell phones, cameras, and hand-held electronic devices, because of its simplicity and low cost. Because of the area and cost, each DC-DC converter uses one inductor is not practical, the idea that several converters share the same inductor has been proposed to solve these problems. The circuit structure is show in Fig. 2.14. The operation of SIDO converters can be divided into two modes: discontinuous conduction mode (DCM) and continuous conduction mode (CCM), depending on the inductor current waveform. The most critical feature is the inductor that stores and transfers magnetic energy to the load and converts to electrostatic energy stored in capacitor.

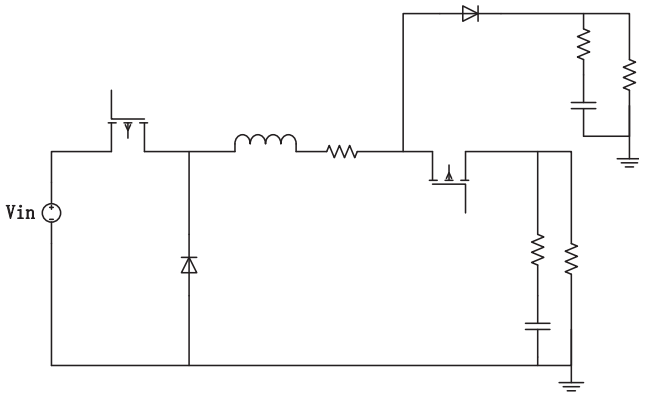

Fig. 2. 14 Topology of SIDO non-isolated DC-DC converter

In portable applications, using multiple supply voltages for different function block has been proposed in [39]. In this case, the buck converter consists of several independent converters as many as the required outputs. However, it will increase the overall cost and make the circuit bulky and complicated. To solve this problem, a new SIDO buck converter is presented [40], which uses only one external inductor to provide dual independent output voltages ranging from 1.2V to the power supply with the maximum output current 200mA.The efficiency is as high as 93.3%. The diagram is shown in Fig. 2.15.

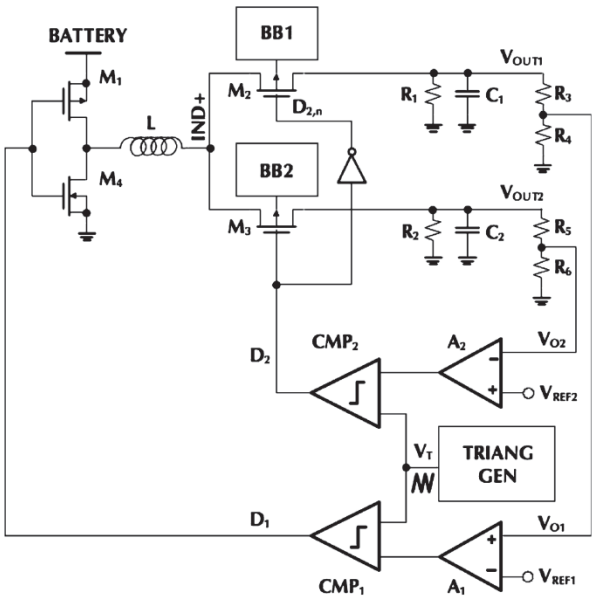

Fig. 2. 15 Circuit structure of SIDO converter

As large as 1.4A current SIDO converter with a wide input supply voltage range has been proposed in [41]. To keep long lifetime of batteries and provide stable supply voltage, the power management system is critical. The suitable control of a double feedback loop enables the single inductor sharing between two outputs with low output voltages errors and limited load regulation. The SIDO configurations of buck, boost, and buck-boost converters have two additional load switches for two outputs as shown in Fig. 2.16, 2.17, 2.18.

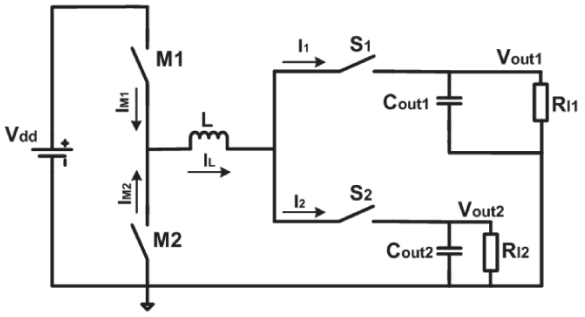

Fig. 2. 16 DC-DC SIDO buck converter

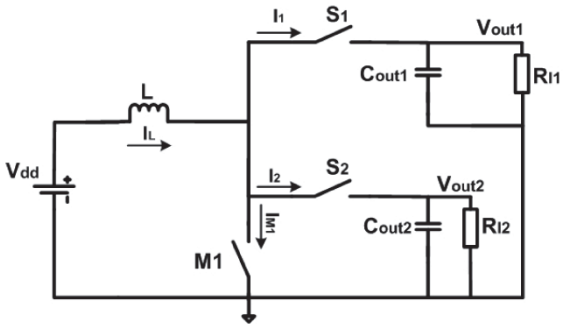

Fig. 2. 17 DC-DC SIDO boost converter

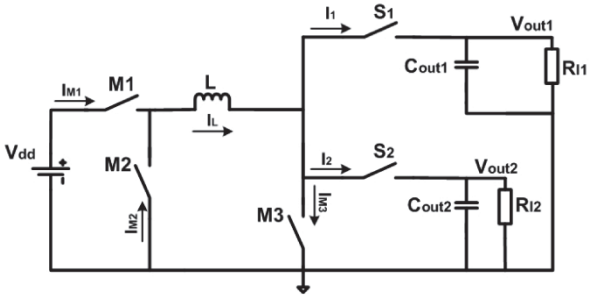

Fig. 2. 18 DC-DC SIDO buck-boost converter

2.1.3 Multi Input-Multi Output DC-DC Converters

Recently, the combination of several power sources and energy storage units of power system (photo voltaic panels, fuel cells, wind turbines, batteries, and ultra-capacitors) has been widely used in industrial applications. The multi input-multi output DC-DC converters have advantages of compact structure and higher efficiency, unify management among the ports. Analysis the power flow and work states reveals that a three-port converter can be treated as a dual-output converter from the main source and as a dual-input converter from the load,

respectively. Three port converter features small size and low cost with high efficiency and high power density in [42] as shown in Fig. 2.19 and Fig. 2.20.

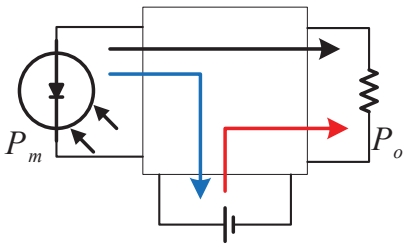

Fig. 2. 19 The power flow in a three-port converter

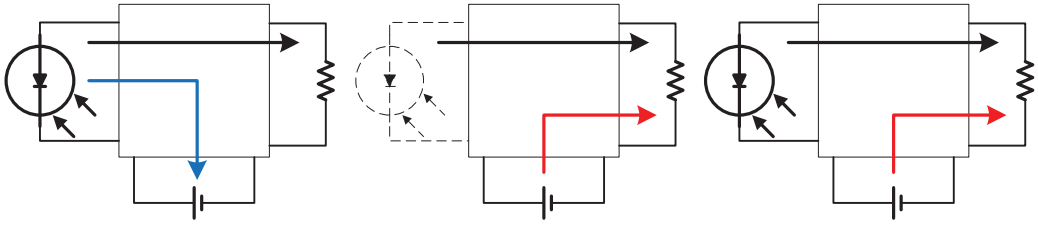

Fig. 2. 20 Power flow of three-port converters when: (a) $P_m > P_o$ (b) $P_m < P_o$ (c) $P_m = 0$

The new topology for multi-input multi-output buck-boost DC-DC converter based on the combination of matrix and buck-boost converters to interface efficiently between DC loads and various DC power sources in a micro grid is proposed in [43]. The switches in this circuit are unidirectional controllable switches, compounds of IGBT transistor in series with a diode and switches are connected in the same input source horizontally and the same output vertically like a matrix structure. There is no limit to the number of inputs and outputs of this topology as Fig. 2.21 shows.

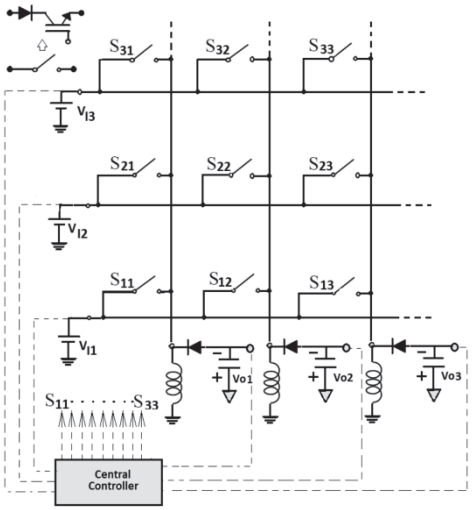

Fig. 2. 21 Topology of proposed multi-input multi-output buck-boost converter

The proposed novel non-isolated three-port converter has one PV port, one bidirectional battery port and one load port [44] in Fig. 2.22. Single stage power conversion between any two of the three ports is achieved. This circuit is architected by one unidirectional buck and one bidirectional boost. The inductor L_2 and switch S_3 are shared in different switching period resulting in minimizing cost and weight. There are three working states, dual-input, dual-output, and single-input single-output.

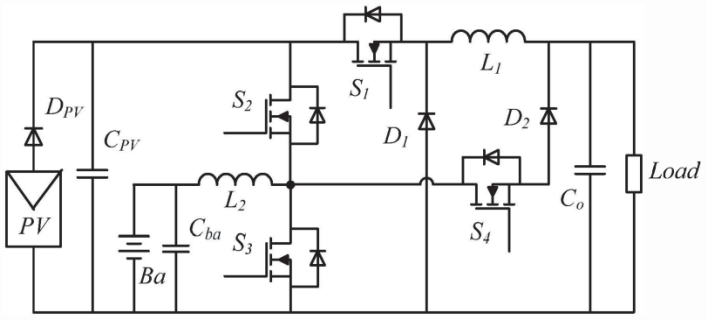

Fig. 2. 22 Topology of proposed multi-input multi-output buck-boost converter

The family of non-isolated three-port converters for power system can be divided into two categories, the combination of dual-output converter (DOC) And single-input single-output converter (SISOC), dual-input converter (DIC) and single-input single-output converter (SISOC) in [45, 46], which analyze the power flow and work states of three-port converters. The diagram of the family is shown as Fig. 2.23.

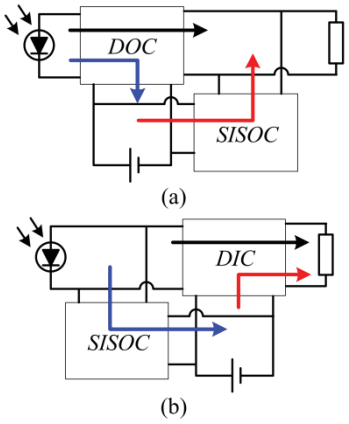

Fig. 2. 23 Structure of non-isolated three-port converter derived from combination of (a) DOC and SISOC, (b) DIC and SISOC

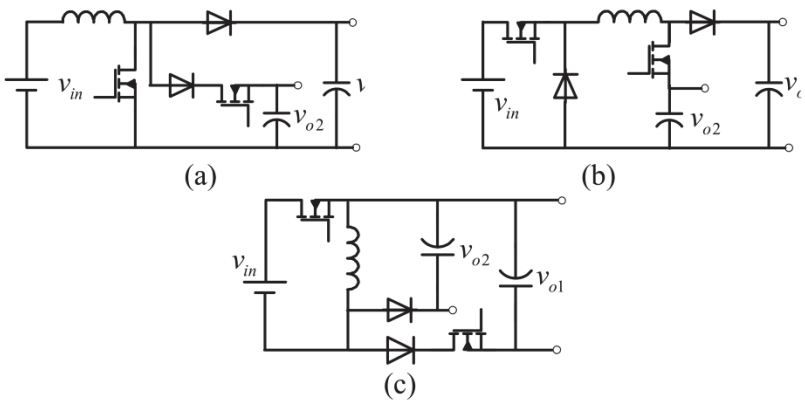

Fig. 2. 24 Topology of non-isolated three-port converter

2.2 Multi-input Isolated DC-DC Converters

There are many research on multi-input isolated DC/DC converter have been presented [11, 31, 47-53]. To overcome the limitations of the proposed converters, researchers at Nagasaki University, Japan [54], developed an MI converter that utilized a transformer in which there is a separate winding for each input. The converter also accommodated multiple outputs by using multiple secondary windings. Any input can provide energy to any output, and there is electrical isolation among all inputs and outputs. However, the transformer core must be suitably large to accommodate all of these windings, and if only one output is required, this advantage is partially mitigated.

2.3 Feedback Control System and Proportional-Integral-Derivative Controllers

The output voltage of dc-dc converter should be able to be regulated within a specific range in response to changes in the output load and the input voltages[55]. The regulation is achieved by using a negative feedback system. Negative feedback applies for reducing the fluctuations in the output, which may cause by the input of other disturbance. The conventional voltage regulator with negative feedback consists of a dc-dc converter, a feedback network, a reference voltage and a control circuit including an error amplifier as shown in Fig. 2.25. Feedback

network monitors the output voltage and reduces the error signal.

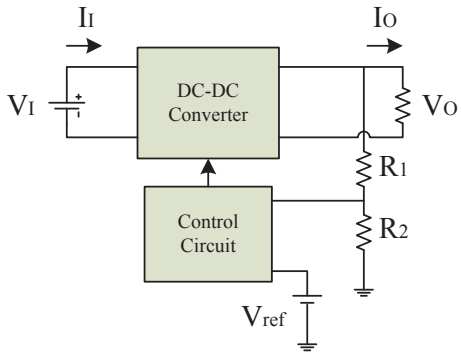

Fig. 2. 25 Structure of negative feedback control

The switching regulators can be classified by voltage mode and current mode controlled switching regulators in as shown in Fig. 2.26. The advantages of voltage-mode control are (a) a single feedback loop is easier to design and analyze, (b) a large-amplitude ramp waveform provides good noise margin for a stable modulation process, (c) a low-impedance power output provides better cross-regulation for multiple output supplies. However, the disadvantages of voltage mode regulator are slow response for any change can be sensed and correct by feedback loop, complicated compensation and output filter. The current mode regulator has advantages immediately response to line voltage, simple compensation and high gain bandwidth, easily adding multiple power units. The disadvantages are the difficult structure of two feedback loops, unstable loop without slope compensation, and noise inserted into the control loop. The ultimate aim of closed-loop feedback control system is to maintain sufficient stability margin.

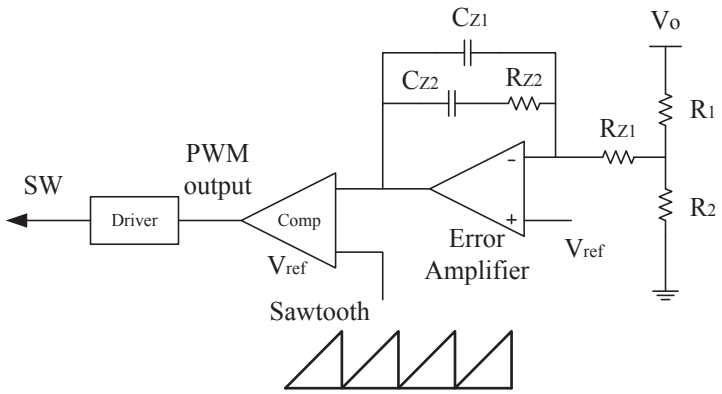

Fig. 2. 26 Voltage mode regulator for dc-dc converter

Another control method is current mode control. With current programmed control, the peak

transistor switch current replaces the duty cycle as the converter's control input. The merits of current mode control is simple dynamics, robust, the protection of transistor switch from excessive current, and mitigation of transistor saturation problem in full-bridge or push-pull converters. And the disadvantages are its susceptibility to noise.

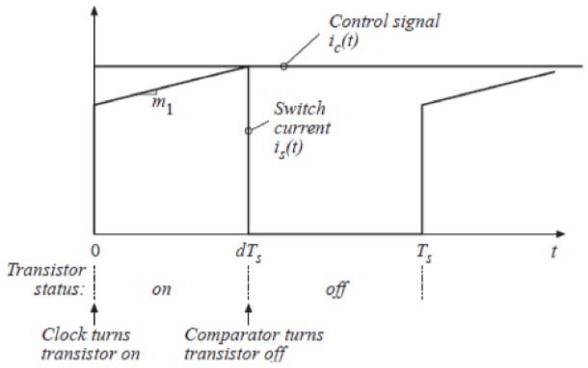

Fig. 2. 27 Current mode regulator for dc-dc converter

For the oscillation $D > 0.5$, the ratio between m_1 and m_2 under steady state, the first interval is

$$i_L(dT_s) = i_c = i_L(0) + m_1 dT_s \tag{2}$$

The solve for duty cycle is

$$d = \frac{i_c - i_L(0)}{m_1 T_s} \tag{3}$$

The second interval is

$$i_L(T_s) = i_L(dT_s) - m_2 d' T_s = i_L(0) + m_1 dT_s - m_2 d' T_s \tag{4}$$

In the steady state,

$$0 = M_1 DT_s - M_2 D' T_s \tag{5}$$

$$\frac{M_2}{M_1} = \frac{D}{D'} \tag{6}$$

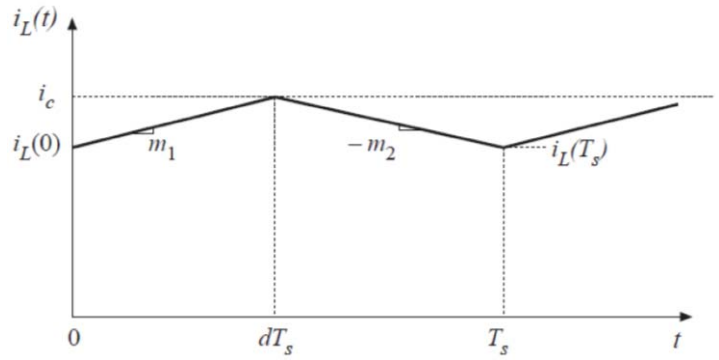

Fig. 2. 28 Waveform of the inductor

When a small perturbation $\hat{i}_L(0)$ is introduced at $t=0$, it is desired to determine the size of the perturbation after n cycles is

$$i_L(nT_s)=(-\frac{m_2}{m_1})^n i_L(0) \tag{7}$$

The figure below shows a case for $\hat{i}_L(0)>0$ and $\hat{d}<0$ with constant m_1 and m_2.

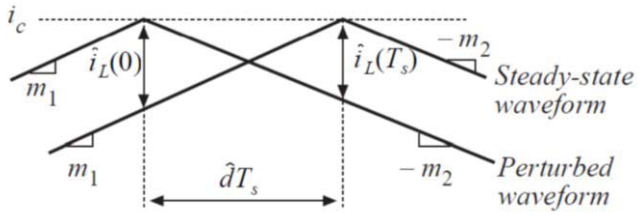

Fig. 2. 29 Waveform of a case for $\hat{i}_L(0)>0$ and $\hat{d}<0$ with constant m_1 and m_2

If the converter operates close to the steady-state operating point, then $m_2/m_1 \approx M_2/M_1 = D/D'$, and after n cycles,

$$i_L(nT_s)=(-\frac{m_2}{m_1})^n i_L(0) \approx (-\frac{M_2}{M_1})^n i_L(0) = (-\frac{D}{D'})^n i_L(0) \tag{8}$$

Or,

$$\left|\hat{i}_L(nT_s)\right| \to \begin{cases} 0 \\ \infty \end{cases} when \begin{matrix} \left|-\frac{D}{D'}\right| < 1 \\ \left|-\frac{D}{D'}\right| > 1 \end{matrix} \tag{9}$$

Therefore, for the stable operation of the current programmed controller in the presence of the disturbances, the quiescent duty cycle should be kept $D < 0.5$.

In most industrial control system, proportional-integral-derivative (PID) algorithm and its growing algorithms are widely used, because of its simplicity, efficiency and feedback loop. It consists of three parameters, proportional factor, integral factor and derivative factor. Proportional value depends on present errors. Integral value depends on accumulation of past errors. Derivative value is a prediction of further errors. PID control algorithm is a process of deviation controlling. The advantages of PID controller are simple structure, easy tuning, and robust performance in a wide range of operational conditions. Moreover, PID controller can describe system dynamic characteristics properly in [56].

When the structure or parameters of controlled object is not accurate, or when the accurate mathematic model cannot be established, other technologies of control theory is hardly applied. PID controller is suitable for these kinds of situations.

When a conventional PID is tuned, three parameters K_p , K_i and K_d are required. The PID algorithm is,

$$u(t) = K_p e(t) + K_i \int_0^t e(\tau) d\tau + K_d \frac{d}{dt} e(t) \tag{10}$$

K_p is used to tune the rise time. K_d is used to reduce the overshoot and setting time. K_i is used to eliminate the steady-state error. u is the control signal. $e(t)$ is the control error, which equals to $e(t) = r_{in}(t) - r_{out}(t)$

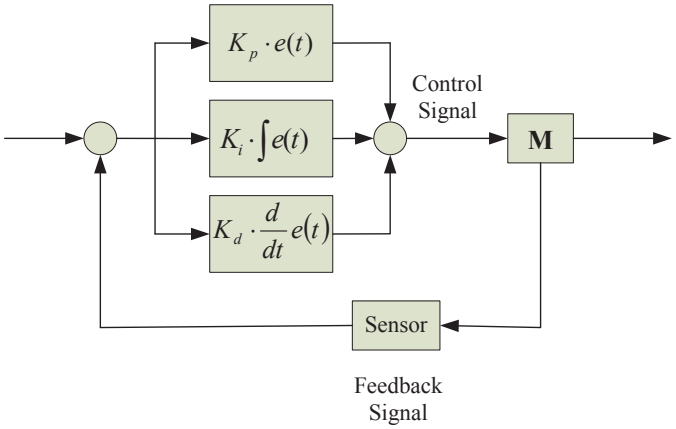

Fig. 2. 30 Structure of conventional PID controller

TABLE II COMPARISON AMONG TUNING PARAMETERS OF CONVENTIONAL PID CONTROLLER

	Rise Time	**Overshoot**	**Settling Time**	**Steady-State Error**	**Stability**
$K_p \uparrow$	↓	↑	small↑	↓	Degrade
$K_i \uparrow$	small↓	↑	↑	large↓	Degrade
$K_d \uparrow$	small↓	↓	↓	Minor Change	Improve

2.4 Advanced PID Controllers

2.4.1 Increment PID algorithm

In order to increase the stability of whole system, the increment PID algorithm is proposed in [57-61]. Firstly, the PID continuous system has to discrete in order to implement by microcontroller. Integral factors are accumulated instead of integration. Derivative factors express as a slope rather than derivation. It can be described with the well-known discrete equations as follows,

$$u(k) = K_p(err(k) + \frac{T}{T_i}\sum err(j) + \frac{T_d}{T}(err(k) - err(k-1))) \\ = K_p(err(k) + K_i\sum err(j) + K_d err(k) - err(k-1))) \quad (11)$$

Also, the increment function is as follows,

$$\Delta u(k) = K_p(err(k) - err(k-1) + K_i err(k) + K_d err(k) - 2err(k-1) + err(k-2)) \quad (12)$$

According to the above formula, the final result of increment PID is only related to the recent three deviations, which will improve the stability of whole system. The final output is $u(k) + \Delta u(k)$. If the noise signal added into one of the factors, it will not affect the accuracy of the whole system.

2.4.2 Integral-separation PID algorithm

The conventional PID control method does not consider the dead-time problem and upper/lower limits. For that reason, when the status of control system changes dramatically (just starts, about to finishes or has to be changed the setting values dramatically), the output of control system will generate large deviation, which will result in accumulation of PID integral factors. It will lead to parameters of controlled object beyond the control tuning range of processor, which will lead to large overshooting, even oscillation of the whole system.

In order to solve this problem, integral separation PID is proposed in [62-64]. When there is a big difference between controlled object output value and reference value, integral factor does not work. When controlled object output value approaches to reference value, integral factor control is introduced for eliminate static error, and improve the accuracy. The time period of reaching the steady-state will be significantly decreased.

2.4.3 Integral anti-windup PID algorithm

The problem of integral saturation occurred in industrial application of PID controller, which is most common phenomenon the control system. The integral saturation means that if there is

the same kind of deviation, integral factor will lead to the output of PID controller accumulate and increase to a maximum limitation. If the output of controller $u(k)$ continues increasing over the normal operation range, it will enter the saturation region. During this period of time, the processor cannot respond to bias deviation immediately and stay in the limitation region. It takes a long time to recover to normal situation. This phenomenon is called integral saturation. In case of this phenomenon, the integral anti-windup algorithm is proposed in [65-68]. The principle of this algorithm is to determine whether last output $u(k-1)$ has exceeded the limit range before calculate the current output $u(k)$.

When $u(k-1) > u_{\max}$, the control system only accumulates negative deviation. When $u(k-1) < u_{\min}$, the control system only accumulates positive deviation. This algorithm can effectively avoid the controlled object stay in the saturation region for a long time.

2.4.4 Gradient PID algorithm

However, in order to improve output accuracy, the gradient PID algorithm is proposed in [69-71]. The integral factor express as following formula,

$$\int_0^t e(t)dt = \sum_{i=0}^{k} \frac{e(i)+e(i-1)}{2}T \tag{13}$$

The function of integral factor is to eliminate the residual errors. In order to decrease residual error and increase the accuracy of operating precision, the rectangular integration can be changed to trapezoidal integration. So the algorithm is,

$$u(k) = K_p(err(k) + \sum_{i=0}^{k} \frac{err(i)+err(i-1)}{2}T + K_d err(k) - err(k-1))) \tag{14}$$

2.4.5 Single-input Fuzzy PID algorithm

Single input fuzzy PID is a kind of intelligence PID in [72-75]. In the conventional PID control

algorithm [76], integral parameter K_i is a constant value. So during the control process, the increment of integral is fixed. However, when deviation is larger than reference value, integral factor should be decreased or even inactive. When deviation is smaller than reference value, integral factor should be increased. The large integral coefficient will lead to over-tuning or even integral saturation. The small integral coefficient cannot eliminate static error in a short time. So the principle of Single input fuzzy PID algorithm is to change the accumulation rate of integral factor responding to deviation error. The final integral factor is $K_i \times index$ by adding a proportional value to integral coefficient $index$.

However, PID controller is not good enough for complex systems. When the three parameters K_p , K_d , K_i are calculated and determined, the whole control process can be hardly changed. In the practical situation, PID controller cannot obtain the optimum efficiency in complex systems like time-varying system and non-linear systems.

2.4.6 Fuzzy Logic Control System

To overcome the problems of conventional PID controller, intelligent PID algorithm is proposed [77-82]. The intelligent PID control method combines intelligent control with conventional PID control. This design concept is using expert system, fuzzy control and neural network technologies to introduce human intelligence into controller design for complex system like nonlinear system and time-varying system. It does not depend on the accurate mathematic model or structure. Robustness to variable parameters make system achieves optimum performance.

The control system based on fuzzy logic, a mathematical system that analyzes analog input value in terms of logical variables that take on continuous values between 0 and 1 in [83]. It simulates human intelligence and human thinking process. The feedback value can be used to predict the achievable performance of PID controllers tuned by fuzzy rules formula as shown in Fig. 2.29.

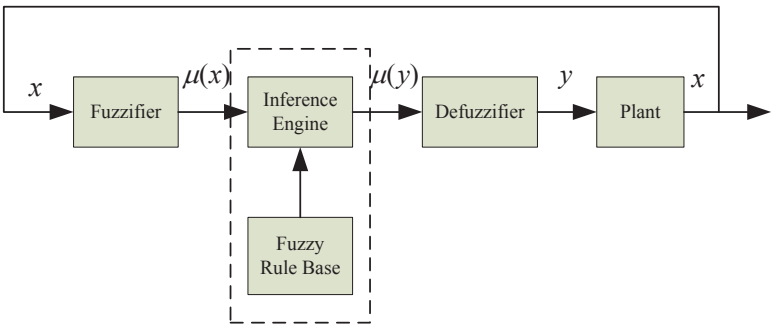

Fig. 2. 31 Diagram of fuzzy logic control method

The most difficult part for expert system is parameters tuning. For processor control models, parameters tuning can be acquired by calculation, whereas for some processor the accuracy requirement is not very high, parameters tuning can be acquired by experimental trial and error method.

However, in the practical control system, most of them are nonlinear systems or uncertain model system. If the accuracy requirements of control system are very high, it is difficult for neural network to design proper algorithm.

Fuzzy logic and expert logic are designed for the necessity of this requirement. The above advanced PID algorithms are special cases of expert system. For example, if the deviation is large enough, the control system should remove integral term. This idea of logic determination is expert system.

They propose a method on how to choose the type of fuzzy controller among PI, PD, and PID, suitable for the controlled plant and the design principle of the fuzzy PID controller. PD mode is used in the case of large error to speed up response, whereas the PI mode is applied for small error conditions to eliminate the steady-state offset. Examples are given for time-delay system, high-order system and nonlinear system.

A fuzzy logic controller can improve control performance especially for high order linear or non-linear system. For time-varying and nonlinear system, their flexibility and stability will be greatly improved, because of the non-linear characteristic of fuzzy PID controller in [84-91].

Fuzzy PID control algorithm is fuzzy logic algorithms application used in parameters tuning of PID controller. The fuzzy logic control usually works with input signals of the system error e

and the change rate de in the error. The system error is defined as the difference between the set point $r(k)$ and the plant output $y(k)$ at the moment k , or

$$e(k) = r(k) - y(k) \tag{15}$$

Hence the change rate in the error de at the moment k will be:

$$de(k) = e(k) - e(k-1) \tag{16}$$

The fuzzy PID controller can use as a third input signal the sum of the system error δe or the acceleration error d^2e ,which are calculated using the equations:

$$\delta e(k) = \sum_{i=1}^{k} e(i) \tag{17}$$

$$d^2e(k) = e(k) - 2e(k-1) + e(k-2) \tag{18}$$

It is known from digital control theory, that the most frequently used digital PID control algorithm

For positioning type PID controller:

$$u(k) = k_p e(k) + k_i \delta e(k) + k_d de(k) \tag{19}$$

For velocity type PID controller:

$$\Delta u(k) = k_p de(k) + k_i e(k) + k_d d^2 e(k) \tag{20}$$

Where $k_i = k_p \frac{T_k}{T_i}$, $k_d = k_p \frac{T_d}{T_k}$, T_k is the sample time of the discrete system, T_i is the integral time constant of the conventional controller, T_d is the differential time constant, k_p is the proportional gain, $u(k)$ is the output control action and $\Delta u(k)$ is the incremental action.

The final control action for the second controller can be calculated according to the previous value of the control output $u(k-1)$ as follows,

$$u(k) = u(k-1) + \Delta u(k) \tag{21}$$

A fuzzy PID controller based on Sugeono's fuzzy technique wit fuzzy neural implementation, which obtain three-term fuzzy PID controller similar to the conventional digital PID controller

in [92, 93]. It can be classified by two categories, one is velocity type fuzzy PID controller, and the other is the positioning type fuzzy PID controller. The antecedent part of the applied fuzzy rules contains a linear function, similar to the discrete equation of the corresponding conventional PID controller. X_1, X_2, X_3 are the input nodes in the first layer connected to the fuzzification μ modules in the second layer. The R modules from the third layer interpret the fuzzy rules and give their output to the μ_n modules in the fourth layer related to the control action u_F that is formed by the output U node in the fifth layer, which is shown in Fig. 2.30. The node in the layer two are term nodes, which act as membership functions to represent the terms of the respective linguistic variables. The structure enables adaptation of the controller properties according to the changing process parameters and environment.

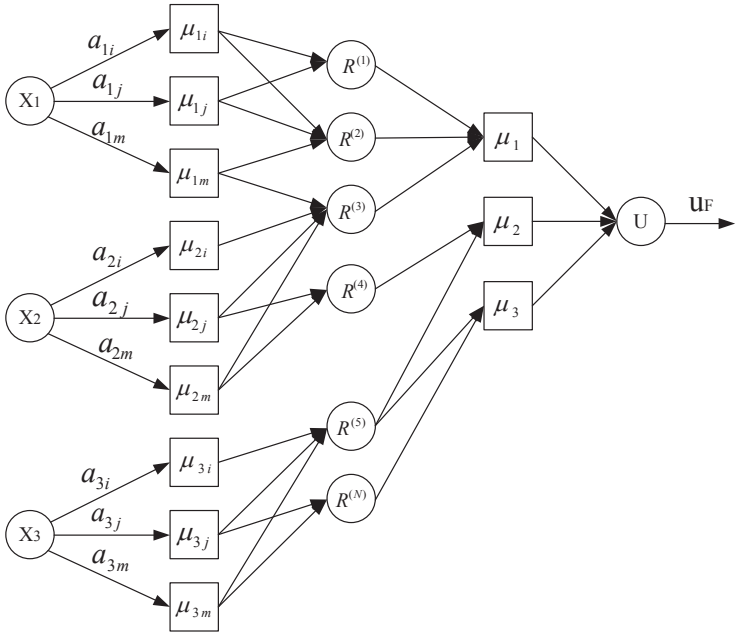

Fig. 2. 32 The structure of the proposed fuzzy-neural PID controller

Firstly, the selected fuzzy PID controller is designed to have the same control property with corresponding PID controller because the parameters of its control rules base are calculated according to tuned parameters of PID controller. Then parameters of this fuzzy rule base of fuzzy PID controller are tuned by sequential quadratic programming (SQP) algorithm. The tuned control surface is nonlinear corresponding to the property of controlled plants, which is shown in Fig. 2.31.

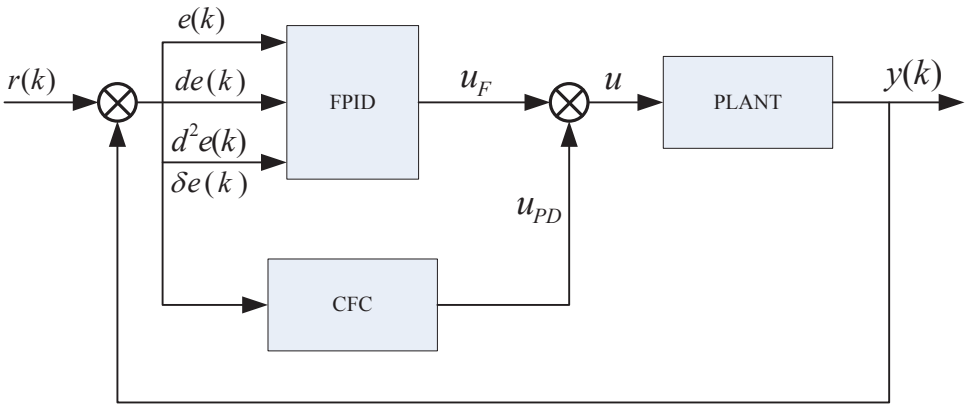

Fig. 2. 33 The structure of the control system with the proposed fuzzy PID controller

There are two types of parameters for fuzzy PID controllers. One is the scaling factors; the other is the fuzzy rule base. If we use the linear defuzzification algorithm with two inputs partitioned into uniformly distributed fuzzy regions, and if we choose suitable scaling factors and fuzzy rule base, a linear-like fuzzy control surface can be generated by linearly defined control rules in simplified inference method. The structure of fuzzy self-adaptive PID controller is shown in Fig. 2.32.

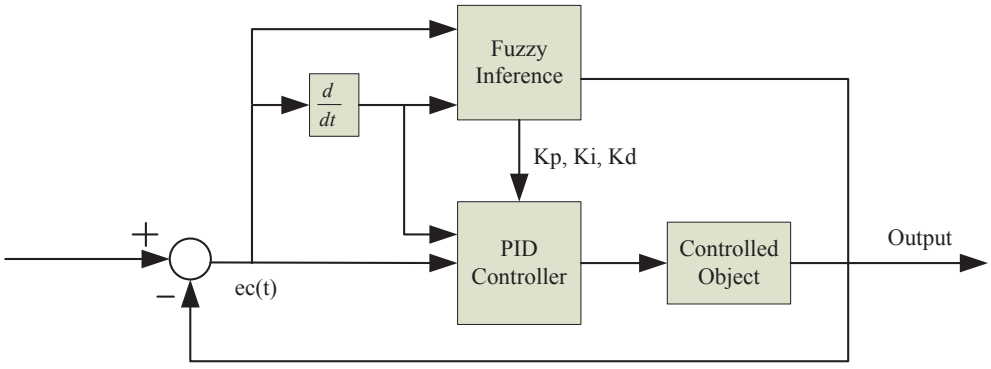

Fig. 2. 34 The structure of fuzzy self-adaptive PID controller

The input of fuzzy self-adaptive PID controller is error e and error variation ec .Determine fuzzy relation graph between three parameters K_p , K_d , K_i of conventional PID and error e and error variation $e(t)$. According to the principle of fuzzy logic control method, revising three parameters online to ensure dynamic and static performance of the controlled object.

The fuzzy self-adaptive PID controller design steps are as follows,

(a) system analysis, to determine input and output variable and structure of controller

(b) Define the field of input and output variable, subjection function, setting control rules, determine defuzzification method.

(c) Simulation and testing. Either offline simulation or online real-time measurement. The offline simulation can be finished by software. There is no need to compose hardware system to verify its performance

(d) Compare the performance of control methods through simulation to decide the optimal control logic.

(e) Tuning the parameters of fuzzy controller, through changing controlled object characteristic parameters to verify the self-adaptive performance

However, the fuzzy PID controller still has following demerits,

1. The design of fuzzy control still has systematic problem, which is difficult to control complicated system.

2. The fuzzy control rules and subjection function, which is design method of the system are based on experience

3. Simple information of fuzzy processing will lead to decrease of control accuracy and dynamic quality. Improving accuracy will need to increase quantitative series inevitably, which lead to expand the searching scope, decrease speed of decision-making, even cannot achieve real-time control function.

4. Stability and robustness of fuzzy control system need further research

Fuzzy control technology lacks a design theory on fuzzy controllers. Many fuzzy controllers have been constructed, instead of systematically designed, case by case using the trial and error method guided by designers, experiences on fuzzy control.

Chapter 3 Theoretical Analysis of Improved Controller on Multi-input Converter

3.1 Hardware Circuit Analysis

Multi-input multi-output power converters are widely used in various applications like hybrid electric vehicles, fuel cells, and micro gird. However, the above-mentioned multi-port converters have several disadvantages as follows: (1) they cannot power up the load simultaneously or individually. (2) They have no storage devices for storing extra available energy when both of two power sources work together. (3) Storage device increases the cost. (4) Single input source for multiple output supplies. (5) Battery charging circuit cannot be controlled.

A new single inductor dual-input dual output dc-dc buck converter for the standalone hybrid power system is presented [94-96]. The circuit has two unidirectional ports, one bidirectional port for storage device and one output port. This converter can solve the above issues with high efficiency, less components, controllable storage device, and delivery independently and simultaneously. The topology is shown as Fig. 3.1.

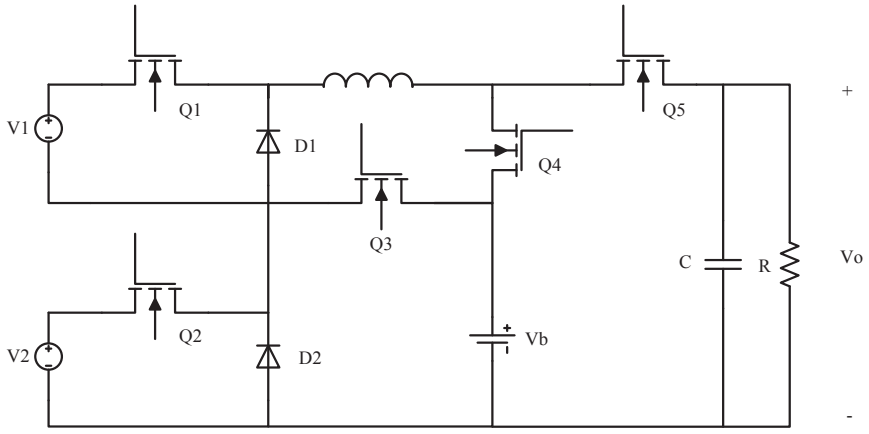

Fig. 3. 1 Structure of Dual-input Dual-output DC-DC Buck Converter

In the dual-input dual-output dc-dc buck converter, there are two input sources V_1, V_2, single inductor L draws current from both two sources individually and simultaneously, two diodes D_1, D_2, R is the load, and five switches Q_1, Q_2, Q_3, Q_4, Q_5, which responsible for power flow control. D_1 D_2 are used for conducting complementary to the switches Q_1, Q_2. Q_3 and Q_4 are responsible for battery charging and discharging circuit. The switch Q_5 regulates the output voltage.

The principle of circuit operation and analysis are based on the following assumptions,

1. All switches are assumed to be ideal forward conducting reverse blocking.
2. Capacitor C is large enough to ensure the output voltage V_O stable.
3. $V_1, V_2, V_b > V_O$.

The four modes of operation analysis are as follows,

A. Dual Input Mode

This mode is further divided into two sub modes,

(a) Both power sources V_1 and V_2 supply the load

In this mode, both power sources V_1 and V_2 supply the load, and the equivalent circuit is shown in Fig. 3.2. It is a dual input buck converter in this mode. Because the battery is not available in this mode, the Q_3 and Q_4 switch off.

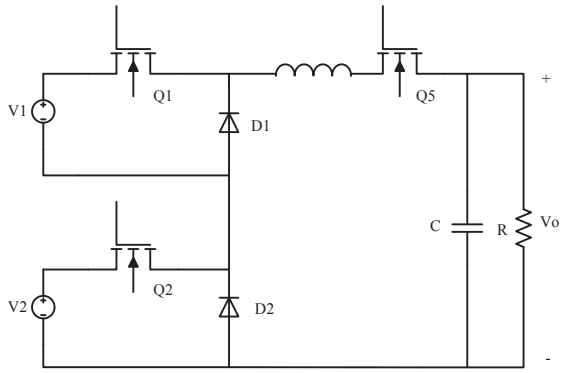

Fig. 3. 2 Structure of Dual-input Dual-output DC-DC Buck Converter

Based on the duty cycle of this sub mode, there are four switching states during the time period T. The inductor current in response to time in each state can be referred by the following equations,

$$\frac{di_L(t_1)}{dt} = \frac{V_1 - V_O}{L} \tag{22}$$

$$\frac{di_L(t_2)}{dt} = \frac{(V_1 + V_2) - V_O}{L} \tag{23}$$

$$\frac{di_L(t_3)}{dt} = \frac{V_2 - V_O}{L} \tag{24}$$

$$\frac{di_L(t_4)}{dt} = \frac{-V_O}{L} \tag{25}$$

In these equations, V_1 and V_2 are input source1 and input source 2, respectively. V_O is the output voltage, and L is the inductance. The output voltage in CCM can be represent as,

$$V_O = V_1 d_1 + V_2 d_2 \tag{26}$$

The key waveforms are shown in Fig. 3.3.

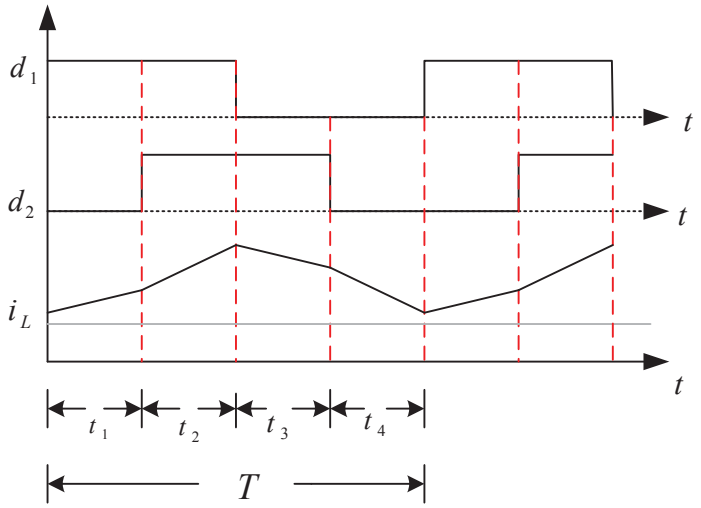

Fig. 3. 3 Waveforms of dual-input mode

(b) V_1 and V_b supply the load

In this sub mode, V_2 is not available to power up the load so the Q_2 switches off, and the battery discharge in this mode instead of V_2 as another power source. V_1 and V_b act as two power source to supply the load when the output voltage is lower than the value of V_1 and V_b .The equivalent circuit is shown in Fig. 3.4. Q_4 switches on and Q_3 remains switches off. The output voltage in CCM can be represent as,

$$V_O = V_1 d_1 + V_b d_4 \tag{27}$$

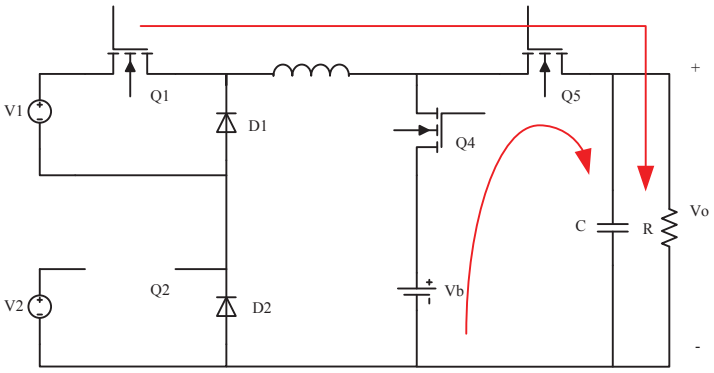

Fig. 3. 4 Power flow analysis of Dual-input Dual-output DC-DC Buck Converter

B. Dual Output Mode

When the voltage of the two input sources is higher than output voltage, a part of energy is used to charge the rechargeable battery. Both input source V_1 and V_2 are available to power the load and charge the battery. In this operation, the converter works in dual output mode. The equivalent circuit is shown in Fig. 3.5.

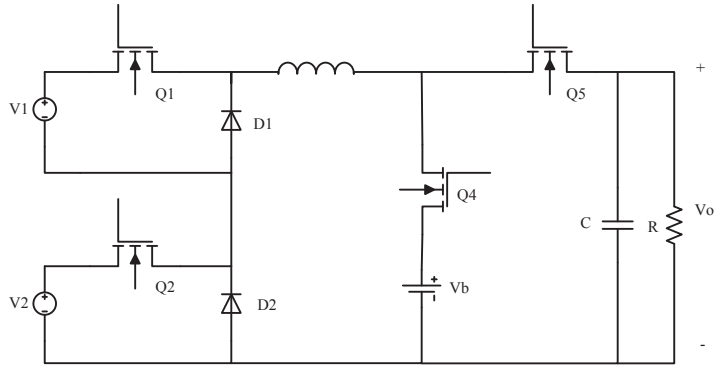

Fig. 3. 5 Equivalent circuit of Dual-input Dual-output DC-DC Buck Converter

The CCM operation in this mode can be divided into several sub modes according to the duty cycle of switches Q_1, Q_2, and Q_5. If $d_1 = d_2$, then d_3 maybe greater than, less than or equals to d_1 and d_2. In dual output mode, Q_4 switches on and Q_3 switches off until the battery is fully charged. The inductor current in response to time in each state can be referred by the following equations,

$$\frac{di_L(t_1)}{dt} = \frac{(V_1 + V_2) - V_{O1} - V_{O2}}{L} \tag{28}$$

$$\frac{di_L(t_2)}{dt} = \frac{(V_1 + V_2) - V_{O2}}{L} \tag{29}$$

$$\frac{di_L(t_3)}{dt} = \frac{-V_{O2}}{L} \tag{30}$$

In these equations, V_{O1} is the output voltage of the load and V_{O2} is the voltage to charge the battery. The waveforms during the period of time and t_1, t_2, t_3 are shown in Fig. 3.6.

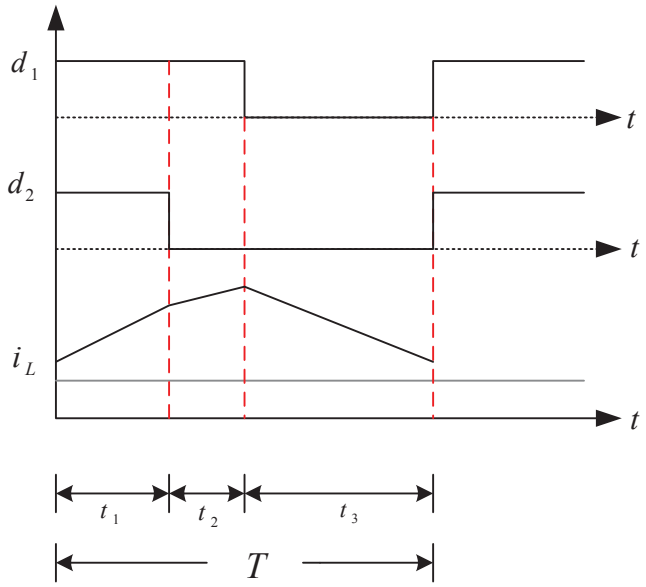

Fig. 3. 6 Waveforms of dual-output mode

C. Single Input Single Output Mode

Only one of the power sources (V_1 , V_2 or V_b) is working as input source. It acts as the conventional buck converter, which is shown in Fig. 3.7.

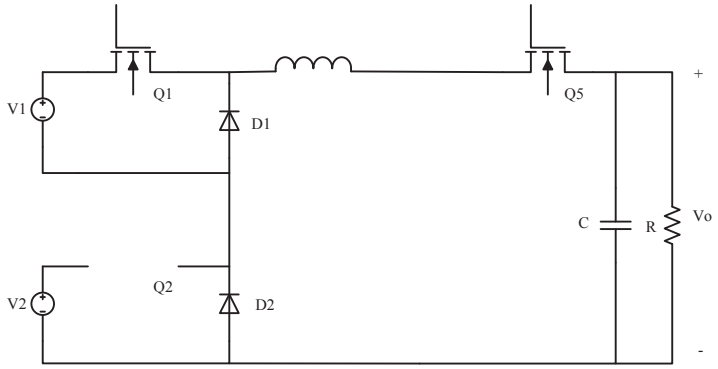

Fig. 3. 7 Equivalent circuit of SISO converter

3.2 Control Method Analysis

Controller is one which compares controlled values with the desired values and has a function to correct the deviation produced. It can be classified into two categories, voltage mode control and current mode control [97].

Voltage mode control has been used for many years in industrial applications. The major characteristics of voltage mode control is that the single voltage feedback path with pulse width modulation performed by comparing the voltage error signal with a constant ramp waveform as shown in Fig. 3.8.

The advantage of voltage mode control is as follows:

1. Simplicity for its single feedback loop.
2. Stability. The large-amplitude ramp provides stable modulation process and small noise.
3. Low-impedance power output provides better cross-regulation for multiple output supplies.

The disadvantage of voltage mode control is as follows:

1. Slow response because any change in line or load will be sensed as an output change and corrected by feedback loop.
2. Two poles to the control loop are required, a dominant-pole low frequency roll-off at the error amplifier, and an added zero I the compensation.

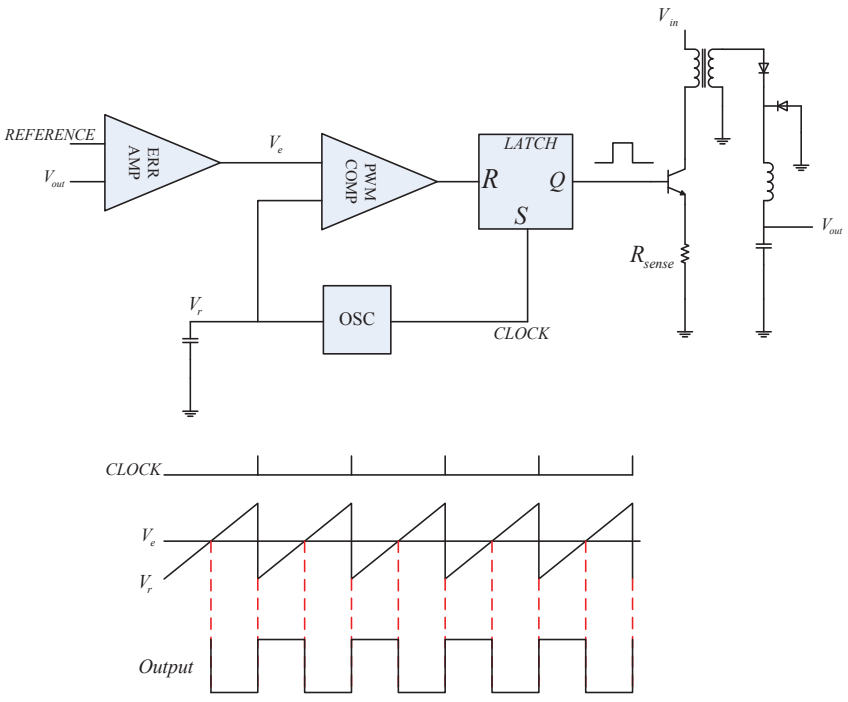

Fig. 3. 8 Diagram of Voltage Mode Control

The above-mentioned disadvantages are alleviated by current mode control. The operation principle can be seen in Fig. 3.9. It uses the oscillator as a fixed-frequency clock and ramp waveform is replaced with the signal derived from output inductor current. The advantages of current mode control are,

1. Respond immediately to line voltage change and eliminate the delay response and gain variation with changes in input voltage, because the inductor current rises with a slope determined by $V_{in} - V_{out}$.

2. Since the error amplifier is now used to command an output current rather than voltage, the effect of the output inductor is minimized and the filter offers a single pole to feedback loop. It makes a simple compensation and a high gain bandwidth than voltage mode control.

3. The inherent pulse by pulse current is limited by clamping the command from the error amplifier, and the ease of providing load sharing when multiple power units are in parallel.

The disadvantage of current mode control is as follows:

1. Two feedback loops that makes circuit complex.

2. Slope compensation is needed to keep circuit stable when duty cycle is higher than 50%

3. Resonances in power stage will insert noise into the control loop since the control modulation is based on the signal derived from output current.

4. Troublesome noise source is the leading edge current spike typically caused by transformer winding capacitance and output filter recovery current.

5. With the control loop forcing a current drive, load regulation is worse and coupled inductors are required to get acceptable cross-regulation with multiple outputs.

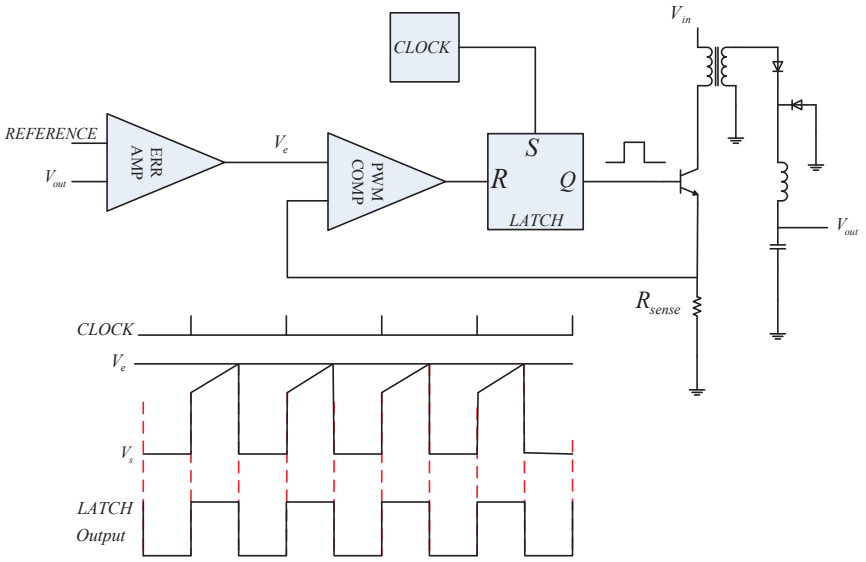

Fig. 3. 9 Diagram of Current Mode Control

Consider the use of current-mode control if:

1. The power supply output is to be a current source or very high output voltage.
2. The fastest dynamic response is needed with a given switching frequency.
3. The application is for a DC/DC converter where the input voltage variation is relatively constrained.
4. Modular applications where parallel ability with load sharing is required.
5. In push-pull circuits where transformer fluxes balancing is important.
6. In low-cost applications requiring the absolute fewest components.

Consider voltage-mode control (with feed-forward) if:

1. There are wide input line and/or output load variations possible.
2. Particularly with low line - light load conditions where the current ramp slope is too shallow for stable PWM operation.
3. High power and/or noisy applications where noise on the current waveform would be difficult to control.
4. Multiple output voltages are needed with relatively good cross-regulation.

5. Saturable reactor controllers are to be used as auxiliary secondary-side regulators.

6. Applications where the complexities of dual feedback loops and/or slope compensation is to be avoided

Pulse-width-modulation converters rely on the theory of non-linear three-terminal switches, which is similar to linear amplifier circuits.

Multivariable control system is a kind of system with more than one control loop are known as multi input multi output (MIMO) or multivariable control system. The controller generates the duty cycles for switches to regulate the output voltage, distributes input power over two input sources, which is shown in Fig. 3.10.

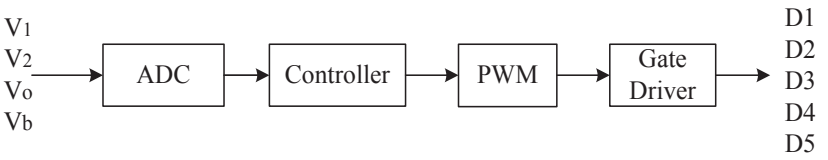

Fig. 3. 10 Diagram of Control system

It is designed for four different operations and controls the internal energy flow of the DIDO converter. The normal buck DC-DC converter negative feedback control system is shown in Fig. 3.11.

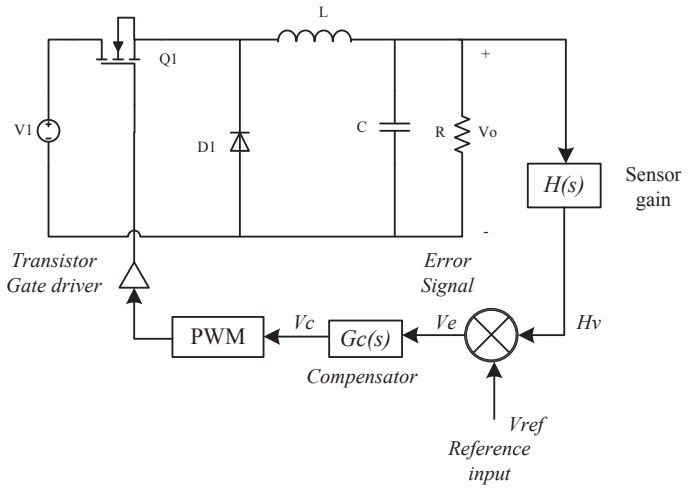

Fig. 3. 11 Basic structure of feedback system for switching regulators

Requirements of a good control system are,

1. Accuracy: defines the limits of the errors when the instrument is used in normal operating conditions. To increase accuracy of any control system, error detector should be present in control system.
2. Sensitivity: a control system should be sensitive to the input only.
3. Noise: a good control system should be able to reduce the noise.
4. Bandwidth: bandwidth should be as large as possible for frequency response of good control system.
5. Speed: a good control system possesses high speed. The transient period for such system is very small.
6. Oscillations: a small numbers of oscillation or constant oscillation of output made system stable.

3.2.1 PID Controller

PID controllers date to 1890s governor design. PID controllers were subsequently developed in automatic ship steering. One of the earliest examples of a PID type controller was developed by Elmer Sperry in 1911 [98].

The first published theoretical analysis of a PID controller was by Russian American engineer Nicolas Minorsky in 1922 [99]. In the early history of automatic process control the PID controller was implemented as a mechanical device. These mechanical controllers used a lever, spring and a mass and were often energized by compressed air. These pneumatic controllers were once the industry standard.

PID controller is a genetic control loop feedback mechanism widely used in industrial control systems. It calculates an “error” values as the difference between a measured process variable and a desired set-point. The PID controller algorithm involves three separate constant parameters, and is accordingly sometimes called three-term control [78].

Designing a PID controller,

1. Obtain an open-loop response and determine what needs to be improved
2. Add a proportional control to improve the rise time
3. Add a derivative control to improve the overshoot
4. Add an integral control to eliminate the steady-state error
5. Adjust each of K_p, K_i, K_d until you obtain a desired overall response

3.2.2 Fuzzy Logic Analysis

Fuzzy logic is a kind of flexible machine learning technique and a multi valued logic, which allows intermediate values to be defined. The basic idea is to mimic the logic of human thought that provides an inference mechanism which can interpret and execute commands. Fuzzy systems are suitable for uncertain or approximate reasoning. Be-valued logic only has two possible values as 0 or 1, yes or no, right or wrong. Fuzzy logic can be multi valued like yes, not, not so much, a little bit, etc. There are several concepts of fuzzy logic system,

- Fuzzy sets are sets whose elements have degrees of membership. Fuzzy sets were introduced simultaneously by Lotfi A. Zadeh [100] and Dieter Klaua in 1965 [101] as an extension of the classical notion of set. In classical set theory, the membership of elements in a set is assessed in binary terms according to a bivalent condition. An element either belongs or does not belong to the set.
- Membership function is maps elements of a fuzzy set to real numbered values in the interval 0 to 1. The curve representing the mathematical function is a membership function that determines the degree of belonging of member x to the fuzzy set T. There are many different fuzzy functions, Quasi-fuzzy membership function, Triangular fuzzy membership function, Trapezoidal fuzzy membership function.
- Fuzzification is a process of transforming crisp input values into linguistic values. The steps of fuzzification is,

1. Input values are translated into linguistic concepts, which are represented by fuzzy set.
2. Membership functions are applied to the measurements and the degree of membership is determined.

- Defuzzification converts the fuzzy values into crisp value. There are several methods to defuzzify, like Max-membership method, Centroid method, and Weighted average method.
- Fuzzy rules are expressed in the form, “IF variable IS set THEN action”.

The characteristics of fuzzy logic are,

1. Exact reasoning is viewed as a limiting case of approximate reasoning.
2. Everything is a matter of degree.
3. Knowledge is interpreted as a collection of elastic or equivalently fuzzy constraints on a collection of variables.
4. Inference is viewed as a process of propagating elastic constraints.
5. Any logical system can be fuzzfied.

Fuzzy control system is based on fuzzy logic. The process of designing fuzzy control system can be described using following steps,

1. Identify the principal input, output and process tasks.
2. Identify linguistic variables used and define fuzzy sets and memberships accordingly.
3. Use these fuzzy sets and linguistic variables to form procedural rules.
4. Determine the defuzzification method.
5. Test the system and modify if necessary.

3.2.3 Fuzzy PID Control System

Intelligent control is a class of control techniques that use various artificial intelligence computing approaches like neural networks, Bayesian probability, fuzzy logic, machine learning, evolutionary computation and genetic algorithms [102]. After the development of fuzzy logic, the important application of it was developed in control method and it is defined as fuzzy PID control system. It is the combination and application of fuzzy logic theory and linear PID controller. It provides significant improvement on controllers due to its non-linear performance. The design of fuzzy PID control system remains a challenging area that requires approaches in solving non-linear tuning issues when captures the noise and output variations.

The principle of fuzzy PID control system is that they convert the error between the measured and controlled values and the reference values into a command, which is applied to the actuator of a process.

The purpose of design the fuzzy PID controller is to develop all processes and increases its control quality with high efficiency of energy conversion and better description and performance of non-linear model.

The methodology to design a fuzzy PID controller is in [103], the tuning is made using a graphical analytical analysis based on the input-output transfer characteristics of the fuzzy block, the linear characteristic of the fuzzy block around the origin and the usage of the gain in origin obtained as an origin limit of the variable gain of the fuzzy block. Transfer functions and equivalence relations between controller's parameters are obtained for the common structures of the PID fuzzy controllers, and algorithms of equivalence are presented.

The basic structure of fuzzy controllers with dynamics is shown in Fig. 3.12.

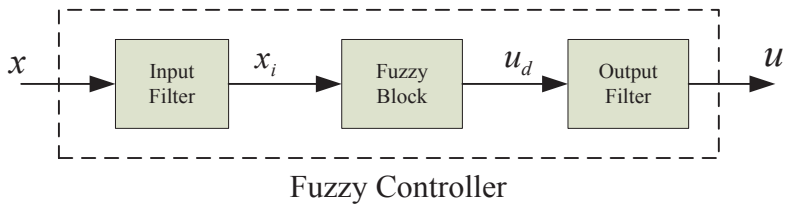

Fig. 3. 12 The diagram of a fuzzy controller with dynamics

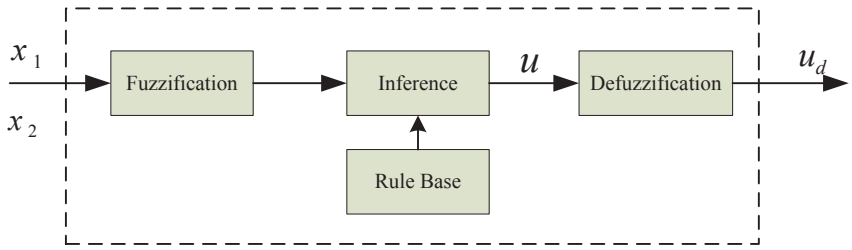

Fig. 3. 13 The detail structure of a fuzzy block

The fuzzy PID has no clear definition as linear system does. It is a kind of mathematical relation using inference with many base rules, based on linguistic variable and practical experience. The fuzzy block consists of three parts, fuzzification, inference and defuzzificaion as shown in Fig. 3.13. The fuzzy logic principles operate as inference.

The fuzzy controller has two input variables x_1 , x_2 and one output variable u . The input variables are taken from the control system. The inference interface of the fuzzy block releases a treatment by linguistic variables of the input variables, obtained by the filtration of the controller input variables. For the linguistic treatment, a definition with membership functions of the input variable is needed. In the interior of fuzzy block, the linguistic variables are linked by rules that are taking account of the static and dynamic behaviour of the control system and also they are taking account of the limitations imposed to the controlled process. After the inference we obtain fuzzy information for the output variable. The defuzzification is used because the actuator that follows the controller must be commanded with a crisp value u_d . The command variable u furnished by the fuzzy controller is obtained by filtering the defuzzified variable u_d . The output variable of the controller is the command input for the process. The fuzzification, inference, and the defuzzification bring a nonlinear behaviour of the fuzzy block. The nonlinear behaviour of the fuzzy block is transmitted also to the fuzzy PID controllers. By an adequate choosing of the input and output filter, different structures of the fuzzy controllers with imposed dynamics as, PI, PD, and PID dynamics.

The structure of fuzzy PID controller is shown in Fig 3.14.

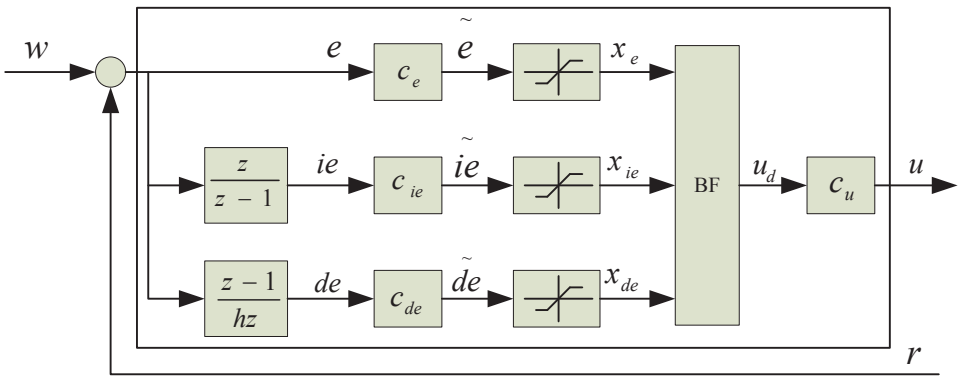

Fig. 3. 14 The simulation diagram of fuzzy PID controller

The deviation and integration is made at the input of the fuzzy block, on the error e. The fuzzy block has three input variables x_e, x_{ie}, and x_{de}. The transfer function of the PID controller is obtained considering a linearization of the fuzzy block BF around the origin, for $x_e = 0$, $x_{ie} = 0$, $x_{de} = 0$, and $u_d = 0$ with a relation of the following form,

$$u_d = K_0(x_e + x_{ie} + x_{de}) \tag{31}$$

A relation, as the fuzzy block from the PID controller, which has three input variable is describes as follows,

$$K_{BF}(x_t; x_{de}, x_{ie} = 0) = \frac{u_d}{x_t}, x_t \neq 0 \tag{32}$$

Where,

$$x_t = x_e + x_{ie} + x_{de} \tag{33}$$

The value K_0 is the limit value in origin of the characteristics of the function,

$$K_0 = \lim_{x_t \to 0} K_{BF}(x_t; x_{de}, x_{ie} = 0) \tag{34}$$

Taking account of the correction made on the fuzzy block with the incremental coefficient c_u, the characteristic of the fuzzy block corrected and liberalized around the origin is given by the relation,

$$u = c_u K_0(x_e + x_{ie} + x_{de}) \tag{35}$$

We are denoting,

$$\tilde{c}_u = c_u K_0 \tag{36}$$

For the fuzzy controller, RF-PID, with the fuzzy block BF liberalized, the following input-output relation in the z domain can be written,

$$u(z) = c_u[x_e(z) + \tilde{x}_{ie}(z) + x_{de}(z)] = \tilde{c}_u[c_e + c_{ie}\frac{z}{z-1} + c_{de}\frac{z-1}{hz}]e(z) \tag{37}$$

With these observations, the transfer function of the fuzzy PID controller becomes,

$$H_{RF}(z) = \frac{u(z)}{e(z)} = \tilde{c}_u(c_e + c_{ie}\frac{z}{z-1} + c_{de}\frac{z-1}{hz}) \tag{38}$$

For the linear PID controller, the following relation for the transfer function is considered,

$$H_{RG}(s) = K_{RG}(1 + T_D s + \frac{1}{T_I s}) \tag{39}$$

1. Linearization

Assuming the multi-input single-output transfer characteristic is,

$$u_d = f_{FB}(x_e, x_{de}), x_e, x_{de} \in [-a, a] \tag{40}$$

And the single-input single-output transfer characteristic is as following equation, and the x_{de} is a parameter.

$$u_d = f_e(x_e, x_{de}), x_e \in [-a, a] \tag{41}$$

A new variable can be introduced for analysis,

$$x_t = x_e + x_{de} \tag{42}$$

So the family of transfer characteristics can be represented as,

$$u_d = f_t(x_t, x_{de}), x \in [-2a, 2a] \tag{43}$$

With x_{de} , the frequency function can be translated to parameter function, which can be determined by the transfer impedance. So, the characteristics of fuzzy block variable gain is,

$$K_{BF}(x_t, x_{de}) = f_t(x_t, x_{de}) / x_t, x_t \neq 0 \tag{44}$$

In conclusion, the multi-input single-output characteristics can be described as,

$$u_d = f_{FB}(x_e, x_{de}) = K_{FB}(x_e, x_{de}) = K_{FB}(x_t, x_{de}) * x_t \tag{45}$$

For instance, the relationship among x_e, x_{de} and u_d is based on the rule base (3×3),

$$K_0 = \lim_{x_e \to 0} K_{BF}(x_t; x_{de}), x_{de} = 0 \tag{46}$$

And the relationship is shown in the table,

TABLE III THE RELATIONSHIP AMONG PARAMETERS OF FUZZY BLOCK

u_d		x_e		
		NB	ZO	PB
x_{de}	NB	NB	NB	ZO
	ZO	NB	ZO	PB
	PB	ZO	PB	PB

2. Anti-wind up circuit

For the digital fuzzy PID controller, anti-wind up circuit is necessary. For the PID controller with integration at the output, an equivalent anti-wind up circuit is applied. The structure is shown as Fig. 3.15.

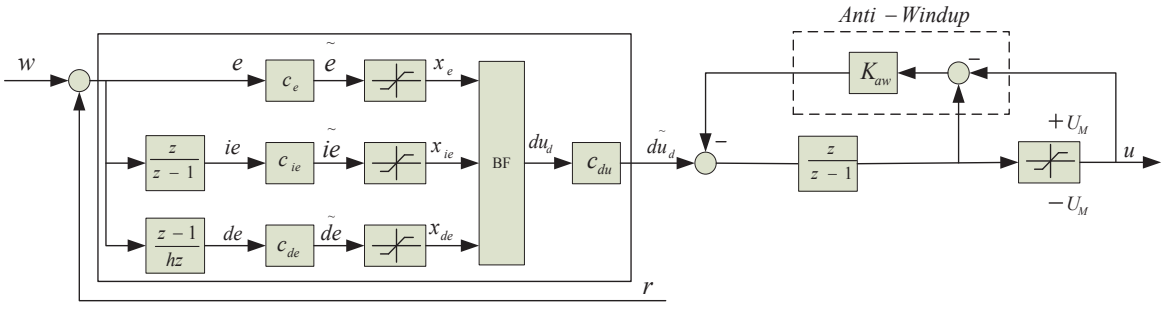

Fig. 3. 15 The Structure of Anti-wind up Fuzzy PID Controller

The feedback loop is designed with anti-windup circuit and the output needs to be limited between the period of $-U_M$ and $+U_M$.

3. Correction of the fuzzy block

The correction circuit is necessary in order to modify the input-output transfer characteristics and quasi-fuzzy controller results. The structure is shown as Fig. 3.16.

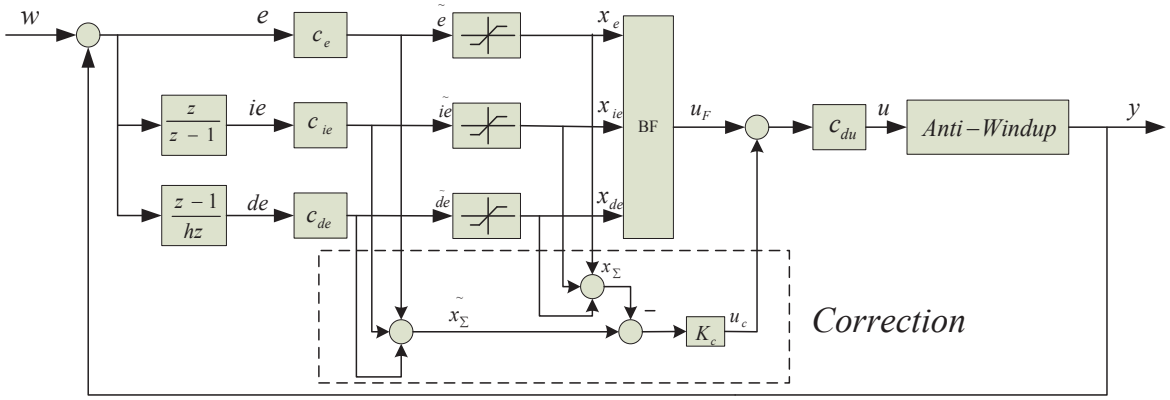

Fig. 3. 16 The Structure of Anti-wind up Fuzzy PID Controller with Correction Circuit

The above-shown equation of correction circuit is nonlinear and is as follows,

$$u_c = K_c[(\tilde{e}+\tilde{de})-(e+de)] \tag{47}$$

4. Pseudo equivalence of the fuzzy PID controller

In fuzzy PID controller, the quasi-continual equation is,

$$H_{RF}(s)=\frac{u(s)}{e(s)}=H_{RF}(z)\Big|_{z=\frac{1+sh/2}{1-sh/2}}=\tilde{c}_u(c_e+c_{ie}/2)[1+\frac{c_{ie}}{h(c_e+c_{ie}/2)}+\frac{c_{de}}{c_e+c_{ie}/2}s] \tag{48}$$

From the identification of the coefficients, the following relations of tuning are,

$$K_{RG}=\tilde{c}_u(c_e+c_{ie}/2) \tag{49}$$

$$T_I=\frac{h(c_e+c_{ie}/2)}{c_{ie}} \tag{50}$$

$$T_D = \frac{c_{de}}{c_e + c_{ie}/2} \tag{51}$$

From the above equations, the expressions of scaling coefficients are,

$$c_e = \left(\frac{T_I}{h} - \frac{1}{2}\right)\frac{hK_{RG}}{\tilde{c}_u T_I} \tag{52}$$

$$c_{ie} = \frac{hK_{RG}}{\tilde{c}_u T_I} \tag{53}$$

$$c_{de} = \frac{K_{RG}}{\tilde{c}_u} T_D \tag{54}$$

3.3 Small Signal Modeling

Small signal modelling is the common analytical techniques in electronics engineering, which is using the approximate behavior of electronic circuits containing nonlinear components with linear equations [104].

The procedure of small signal modeling is as follows,

1. Establish the time-domain differential equations of components like inductors and capacitors in power stage
2. Average state space of equations, which means to calculate the average value in one periodic switching cycle.
3. Introduce the perturbation to equations.
4. Linear equations and get the small signal model.

3.3.1 State-space Average Method

The state-space average method is a kind of mathematical model of power converter as a set of input, output, and variables related to first-order differential equations to represent the hardware

circuit and controller [105].

In this part, a state space average model and its procedure for hardware topology are presented as follows,

1. Draw the linear switched circuit model for each state of the switching converter.
2. Write state equations for each switched circuit model using Kichhoff's voltage and current laws.
3. Averaging the state-space equation using the duty ratio.
4. Perturb the averaged state equation to yield steady-state (DC) and dynamic (AC) terms and eliminate the product of any AC terms
5. Transform the AC equations into S-domain to solve for transfer function.

This model used to design the accurate and robust controller for the hardware circuits, which can satisfy the stability and reliability of the control requirement and obtain the best performance of the controller. In modeling, the components like capacitors, inductors, switches and diodes are non-ideal, so the disturbances are considered.

State space averaging method is used to analyze the components of the converter, which is as follows,

$$\vec{K}\frac{d\vec{x(t)}}{dt} = \vec{A}\vec{x}(t) + \vec{B}\vec{u}(t) \tag{55}$$

$$\vec{y}(t) = \vec{C}\vec{x}(t) + \vec{E}\vec{u}(t) \tag{56}$$

State variable $x(t)$ includes inductor current, capacitor voltage, and other components, which can be represented as follows,

$$\vec{x}(t) = \begin{bmatrix} x_1(t) \\ x_2(t) \\ \cdots\cdots \end{bmatrix}, \frac{d\vec{x(t)}}{dt} = \begin{bmatrix} \frac{dx_1(t)}{dt} \\ \frac{dx_2(t)}{dt} \\ \cdots\cdots \\ \end{bmatrix} \tag{57}$$

$u(t)$ is the converter input $v_g(t)$. $y(t)$ is the output vector. Coefficient matrix includes capacitance, inductance, and mutual inductance. Output variable $y(t)$ is linear combination of input independent source and state variables. A, B, C, E are constant matrix.

State-space average method applies for inductance and capacitance. The inductor characteristic equation is

$$L\frac{di_L}{dt} = v_L(t) \tag{58}$$

Its differential form is,

$$Ldi_L(t) = v_L(t) \tag{59}$$

The integration of above equation in a period is,

$$\int_t^{t+T_s} dt = \frac{1}{L}\int_t^{t+T_s} v_L(\tau)dt \tag{60}$$

$$i(t+T_s) - i(t) = \frac{1}{L}T_s\left\langle v_L(t)\right\rangle_{T_s} \tag{61}$$

$$L\frac{i(t+T_s)-i(t)}{T_s} = \left\langle v_L(t)\right\rangle_{T_s} \tag{62}$$

The above equations prove that the change of inductor current is directly proportional to the average value of inductor voltage in a switching period. From the Euler formula, we can obtain,

$$\begin{aligned}
&\frac{d\left\langle i(t)\right\rangle_{T_s}}{dt} \\
&= \frac{d}{dt}[\frac{1}{T_s}\int_t^{t+T_s} i(\tau)d\tau] \\
&= \frac{1}{T_s}\frac{d}{dt}\left[\int_t^0 i(\tau)d\tau + \int_0^{t+T_s} i(\tau)d\tau\right] \\
&= \frac{i(t+T_s)-i(t)}{T_s}
\end{aligned} \tag{63}$$

From equation (58) and (63), the conclusion is,

$$L\frac{d\left\langle i(t)\right\rangle_{T_s}}{dt} = \left\langle v_L(t)\right\rangle_{T_s} \tag{64}$$

The average values of voltage and current components in a switching period also satisfy the

characteristic equation of inductor.

In the steady state, according to the voltage-second balance, the average value of inductor voltage is zero, which is represented as $\langle v_L(t)\rangle_{T_s} = 0$. From equation (64), $L\dfrac{d\langle i(t)\rangle_{T_s}}{dt} = 0$, which means the average value of inductor current $\langle i(t)\rangle_{T_s}$ is a constant value. However, its waveform of instantaneous value is nearly a triangle wave.

Same method to describe the characteristic of capacitor is

$$C\frac{d\langle v_C(t)\rangle_{T_s}}{dt} = \langle i_C(t)\rangle_{T_s} \tag{65}$$

In the steady state, according to the charge balance principle, the average current of capacitor is zero, which can be described as the following equation,

$$\langle i_C(t)\rangle_{T_s} = 0 \tag{66}$$

From the equation (66),

$$C\frac{d\langle v_C(t)\rangle_{T_s}}{dt} = 0 \tag{67}$$

Capacitor voltage in a switching period $\langle v_C(t)\rangle_{T_s}$ is a constant value. Its waveform of instantaneous value is also nearly a triangle wave.

3.3.2 Large-signal Model

The simple buck converter is used as the example to describe two different operation modes. One is ON state when the switch turns on, and the other is OFF state, when the switch turns off. These two statuses are shown in Fig. 3.17.

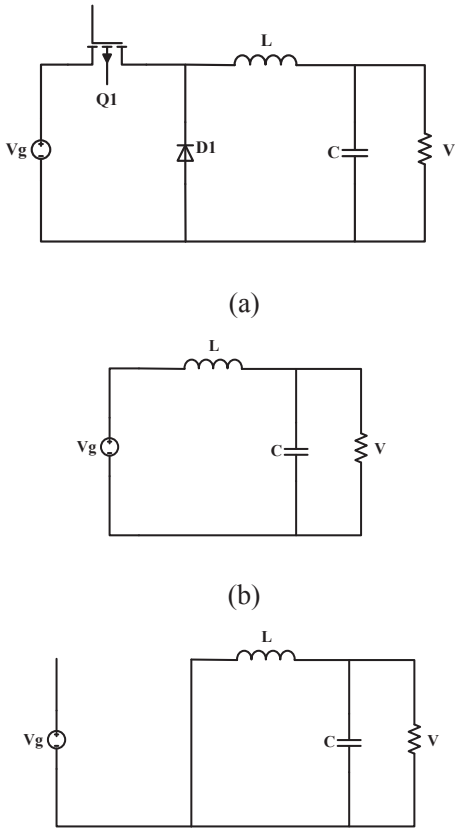

Fig. 3. 17 Buck converter and its ideal equivalent circuit (a) Circuit (b) Equivalent circuit when the switch is ON. (c) Equivalent circuit when the switch is OFF.

When the switch is ON, in the period of $\left[t, t+dT_s\right]$, the voltage of inductor is,

$$v_L(t) = L\frac{di(t)}{dt} = v_g(t) - v(t) \tag{68}$$

The current of inductor is,

$$i_c(t) = C\frac{dv(t)}{dt} = -v(t) \tag{69}$$

When the switch is OFF, in the period of $\left[t+dT_s, t+T_s\right]$, the voltage of inductor is,

$$v_L(t) = L\frac{di(t)}{dt} = -v(t) \tag{70}$$

The current of inductor is,

$$i_c(t) = C\frac{dv(t)}{dt} = i(t) - \frac{v(t)}{R} \tag{71}$$

According to the calculation above, idealized current and voltage waveform can be shown as Fig 3.18.

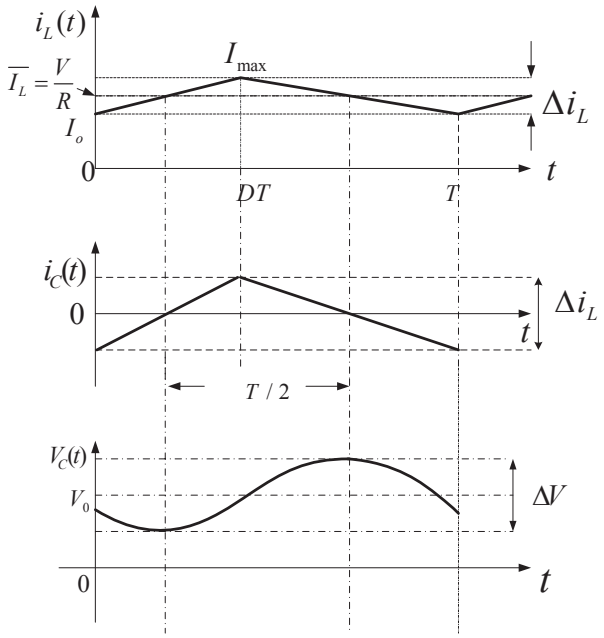

Fig. 3. 18 Idealized current and voltage waveform of buck converter

The average voltage value in a period is,

$$\left\langle v_L(t)\right\rangle_{T_s} = \frac{1}{T_s}\int_t^{t+T_s} v_L(t)dt = \frac{1}{T_s}\left[\int_t^{t+DT_s} v_L(t)dt + \int_{t+DT_s}^{t+T_s} v_L(t)dt\right] \tag{72}$$

$$\left\langle v_L(t)\right\rangle_{T_s} = \frac{1}{T_s}\left[\int_t^{t+DT_s} [v_g(t)-v(t)]dt - \int_{t+DT_s}^{t+T_s} v(t)dt\right] = (V_g - V)D - V(1-D)$$

(73)

If the input voltage $v_g(t)$ is continuous and has little variation in a switching period, the $v_g(t)$ in the interval $[t, t+dT_s]$ is approximate to the average value $\left\langle v_g(t)\right\rangle_{T_s}$, which can be represented as follow equation,

$$\int_t^{t+dT_s} v_g(\tau)d\tau \approx \int_t^{t+dT_s} \left\langle v_g(\tau)\right\rangle_{T_s} dt = \left\langle v_g(t)-v(t)\right\rangle_{T_s} dT_s \tag{74}$$

Similarly, because the output voltage $v(t)$ is continuous and has little variation in a switching period, the $v(t)$ in the interval $[t+dT_s, t+T_s]$ is approximate to the average value $\left\langle v(t)\right\rangle_{T_s}$, which is shown as the following equation,

$$\int_{t+dT_s}^{t+T_s} v(\tau)d\tau \approx \int_{t+dT_s}^{t+T_s} \left\langle v(\tau)\right\rangle_{T_s} d\tau = -\left\langle v(t)\right\rangle_{T_s} (1-d)T_s \tag{75}$$

According to the characteristic equation of inductor, it can be represented as follows,

$$L\frac{\langle di(t)\rangle_{T_s}}{dt}=d(t)\langle v_g(t)-v(t)\rangle_{T_s}-d'(t)\langle v(t)\rangle_{T_s} \tag{76}$$

The average current is controlled by the change of duty cycle $d(t)$. Input voltage will affect the line regulation and output will affect the load regulation. Through close loop feedback controller, these parameters will be significantly improved.

Approximate straight-line the inductor current to deduct the current equation. When switch is ON, the equation is,

$$i(dT_s)=i(0)+(dT_s)\left[\frac{\langle v_g(t)\rangle_{T_s}}{L}\right] \tag{77}$$

When switch is OFF, the equation is,

$$i(T_s)=i(dT_s)+(d'T_s)\left[\frac{\langle v(t)\rangle_{T_s}}{L}\right] \tag{78}$$

So, the $i(T_s)$ is,

$$i(T_s)=i(0)+\frac{T_s}{L}[d(t)\langle v_g(t)\rangle_{T_s}+d'(t)\langle v(t)\rangle_{T_s}] \tag{79}$$

Similarly, the current and voltage of capacitor is,

$$\langle i_C(t)\rangle_{T_s}=d(t)\frac{\langle v(t)\rangle_{T_s}}{R}+d'(t)(\langle i(t)\rangle_{T_s}-\frac{\langle v(t)\rangle_{T_s}}{R}) \tag{80}$$

Because,

$$i_g(t)=\begin{cases} i(t) & 0<t<dT_s \\ 0 & dT_s<t<T_s \end{cases} \tag{81}$$

$$\langle i_g(t)\rangle_{T_s}\approx d(t)\langle i(t)\rangle_{T_s} \tag{82}$$

In conclusion, state-space average equation of the buck converter in a switching period is,

$$\begin{cases} L\dfrac{\langle di(t)\rangle_{T_s}}{dt}=d(t)\langle v_g(t)-v(t)\rangle_{T_s}-d'(t)\langle v(t)\rangle_{T_s} \\ C\dfrac{d\langle v(t)\rangle_{T_s}}{dt}=d(t)\dfrac{\langle v(t)\rangle_{T_s}}{R}+d'(t)(\langle i(t)\rangle_{T_s}-\dfrac{\langle v(t)\rangle_{T_s}}{R}) \end{cases} \tag{83}$$

3.3.3 Linearization and Small Signal AC Equivalent Circuit

The average value equation of input current in a switching period is,

$$\left\langle i_g(t)\right\rangle_{T_s} = d(t)\left\langle i(t)\right\rangle_{T_s} \tag{84}$$

If the buck converter operates at quiescent point, steady state duty cycle is $d(t) = D$, input voltage $\left\langle v_g(t)\right\rangle_{T_s}$, inductor current $\left\langle i(t)\right\rangle_{T_s}$, capacitor voltage $\left\langle v(t)\right\rangle_{T_s}$ and input current $\left\langle i_g(t)\right\rangle_{T_s}$ are V_g, I, V and I_g.

According to the inductor current equation (83), the voltage-second balance equation is, $\left\langle v_L(t)\right\rangle_{T_s} = L\dfrac{\left\langle di(t)\right\rangle_{T_s}}{dt} = 0$, the duty cycle is $d(t) = D$.They are steady values, so the calculation result is,

$$DV_g = V \tag{85}$$

Same theory, according to capacitor voltage equation (83) and charge balance principle, the equation is $\left\langle i_C(t)\right\rangle_{T_s} = C\dfrac{\left\langle dv(t)\right\rangle_{T_s}}{dt} = 0$, the duty cycle is $d(t) = D$ and they are steady values, the calculation result is,

$$I = \frac{V}{R}\left(\frac{D'-D}{D'}\right) \tag{86}$$

According to average value equation of input current, we can obtain the equation, $\left\langle i_g(t)\right\rangle_{T_s} = d(t)\left\langle i(t)\right\rangle_{T_s}$, and duty cycle is $d(t) = D$. They are all steady values, the calculation result is,

$$I_g = DI \tag{87}$$

Disturbance injection method can be used to design the small signal dynamic model. If the input voltage and duty cycle have little perturbations near the quiescent point, which can be expressed as follows,

$$\left\langle v_g(t)\right\rangle_{T_s} = V_g + \hat{v}_g(t) \tag{88}$$

$$d(t) = D + \hat{d}(t) \tag{89}$$

It will arouse perturbations of state variables and input current, which are,

$$\left\langle i(t)\right\rangle_{T_s} = I + \hat{i}(t) \tag{90}$$

$$\left\langle v(t)\right\rangle_{T_s} = V + \hat{v}(t) \tag{91}$$

$$\left\langle i_g(t)\right\rangle_{T_s} = I_g + \hat{i}_g(t) \tag{92}$$

As a result, the state space averaging equation of inductor current is,

$$L\frac{d[I+\hat{i}(t)]}{dt} = [D+\hat{d}(t)][V_g+\hat{v}_g(t)-V-\hat{v}(t)]+[D'-\hat{d}(t)][V+\hat{v}(t)]$$
$$= \underbrace{DV_g - DV + D'V}_{DC} + \underbrace{D\hat{v}_g(t)+\hat{d}(t)V_g + D'\hat{v}(t)+\hat{d}(t)V - D\hat{v}(t)-V\hat{d}(t)}_{First-order-AC} + \underbrace{\hat{d}(t)\hat{v}_g(t)+2\hat{d}(t)\hat{v}(t)}_{Second-order-AC}$$

(93)

Because $\frac{dI}{dt}=0$, $DV_g = V$, and second-order factor is much smaller than first-order factor, the second-order factors are negligible. So the calculation result is linear ordinary differential equation with constant coefficients as follows,

$$L\frac{d\hat{i}(t)}{dt} = D\hat{v}_g(t)+\hat{d}(t)V_g + D'\hat{v}(t)+\hat{d}(t)V - D\hat{v}(t)-V\hat{d}(t) \tag{94}$$

Similarly, the state space averaging equation of capacitor voltage is,

$$C\frac{d[V+\hat{v}(t)]}{dt} = [D+\hat{d}(t)]\frac{V+\hat{v}(t)}{R}+[D'-\hat{d}(t)][I+\hat{i}(t)-\frac{V+\hat{v}(t)}{R}]$$
$$= \underbrace{\frac{V}{R}D + D'I + \frac{VD'}{R}}_{DC} + \underbrace{\frac{D}{R}\hat{v}(t)+D'\hat{i}(t)+\frac{V}{R}\hat{d}(t)-\frac{D'}{R}\hat{v}(t)-I\hat{d}(t)+\frac{V}{R}\hat{d}(t)}_{First-order-AC} + \underbrace{\frac{2}{R}\hat{d}(t)\hat{v}(t)-\hat{d}(t)\hat{i}(t)}_{Second-order-AC}$$

(95)

Because $\frac{dV}{dt}=0$, $I=\frac{V}{R}(\frac{D'-D}{D'})$, and second-order factor is much smaller than first-order factor, the second-order factors are negligible. So the calculation result is linear ordinary differential equation with constant coefficients as follows,

$$C\frac{d\hat{v}(t)}{dt}=\frac{D}{R}\hat{v}(t)+D'\hat{i}(t)+\frac{V}{R}\hat{d}(t)-\frac{D'}{R}\hat{v}(t)-I\hat{d}(t)+\frac{V}{R}\hat{d}(t) \tag{96}$$

According to average value equation of input current, the input current with perturbation is,

$$I_g+\hat{i}_g(t)=[D+\hat{d}(t)]+[I+\hat{i}(t)] \tag{97}$$

Also, the nonlinear second-order factor is negligible, and the final equation is,

$$\hat{i}_g(t)=D\hat{i}(t)+I\hat{d}(t) \tag{98}$$

In conclusion, the small signal ac model is,

$$\begin{cases} L\dfrac{d\hat{i}(t)}{dt}=D\hat{v}_g(t)+\hat{d}(t)V_g+D'\hat{v}(t)+\hat{d}(t)V-D\hat{v}(t)-V\hat{d}(t) \\ C\dfrac{d\hat{v}(t)}{dt}=\dfrac{D}{R}\hat{v}(t)+D'\hat{i}(t)+\dfrac{V}{R}\hat{d}(t)-\dfrac{D'}{R}\hat{v}(t)-I\hat{d}(t)+\dfrac{V}{R}\hat{d}(t) \\ \hat{i}_g(t)=D\hat{i}(t)+I\hat{d}(t) \end{cases} \tag{99}$$

According to the above equations, small signal ac equivalent circuit is shown in Fig. 3.19.

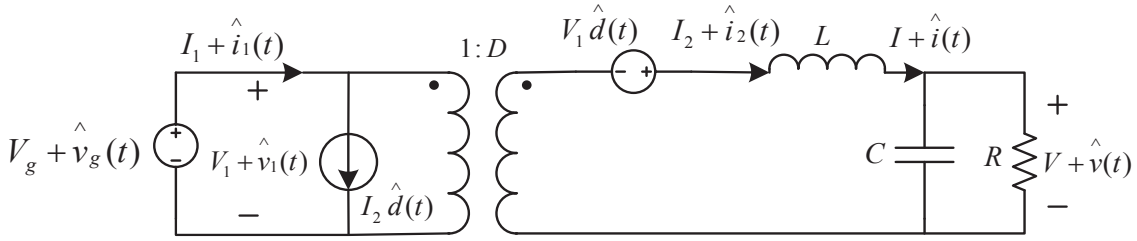

Fig. 3. 19 Small signal ac equivalent circuit

3.3.4 Transfer Function

According to the above equations, small signal ac equivalent circuit is shown in Fig. 3.20 and 3.21.

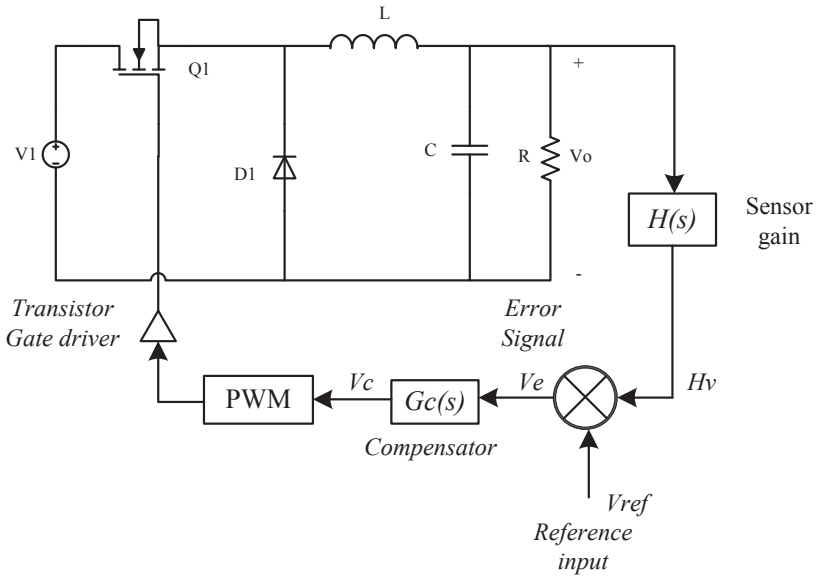

Fig. 3. 20 Buck DC/DC converter feedback control system

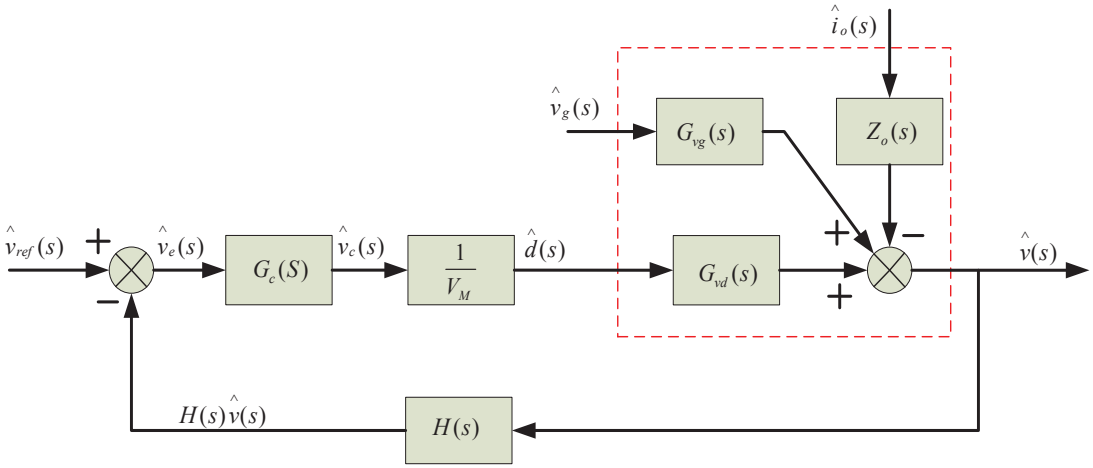

Fig. 3. 21 Linearized Buck DC/DC converter feedback control system diagram

The buck converter linearization model is expressed as follow formula,

$$\hat{v}(s) = G_{vd}(s)\hat{d}(s) + G_{vg}(s)\hat{v}_g(s) + Z_o(s)\hat{i}_o(s) \tag{100}$$

$\hat{v}(s)$ is the output voltage of Buck converter. $\hat{d}(s)$ is the duty cycle of PWM modulator. $\hat{v}_g(s)$ is the input voltage of buck converter. $\hat{i}_o(s)$ is load current of buck converter.

Without feedback control, the influence of input voltage disturbance to output voltage is,

$$G_{vg}(s) = \frac{\hat{v}(s)}{\hat{v}_g(s)} \tag{101}$$

when $\hat{d}(s)=0$, $\hat{i}_o(s)=0$.

The influence of load variation to output voltage is,

$$Z_o(s)=\frac{\hat{v}(s)}{\hat{i}_o(s)} \tag{102}$$

when $\hat{d}(s)=0$, $\hat{v}_g(s)=0$.

The transfer function from duty cycle to output voltage is,

$$G_{vd}(s)=\frac{\hat{v}(s)}{\hat{d}(s)} \tag{103}$$

when $\hat{i}_o(s)=0$, $\hat{v}_g(s)=0$.

When feedback control is introduced, the output voltage is,

$$\hat{v}(s)=\hat{v}_{ref}\frac{T}{H(1+T)}+\hat{v}_g\frac{G_{vg}}{1+T}+\hat{i}_o\frac{Z_o}{1+T} \tag{104}$$

T is the gain of circuit, and $T=H(s)G_c(s)G_{vd}(s)/V_M$.

As the result of above equation, the influence of input voltage disturbance to output voltage is,

$$\frac{\hat{v}}{\hat{v}_g}=\frac{G_{vg}(s)}{1+T} \tag{105}$$

when $\hat{d}(s)=0$, $\hat{i}_o(s)=0$

Transfer function of input voltage to output voltage is,

$$G_{vg}(s)=\left.\frac{\hat{v}(s)}{\hat{v}_g(s)}\right|_{\hat{d}(s)=0}=M(D)H_e(s)=\frac{D}{1+s\frac{L}{R}+s^2LC} \tag{106}$$

$M(D)$ is input/output voltage transfer ratio, $H_e(s)$ is transfer function of low-pass filter, $H_e(s)=\frac{v(s)}{v_t(s)}$.

Transfer function of controller to output voltage is,

$$G_{vd}(s)=\frac{\hat{v}(s)}{\hat{d}(s)}\bigg|_{\hat{v}_g(s)=0}=e(s)M(D)H_e(s)=\frac{V}{D}\frac{1}{1+s\frac{L}{R}+s^2LC} \tag{107}$$

The second-order system model is,

$$G(s)=\frac{1}{1+2\zeta\frac{s}{\omega_0}+\frac{s^2}{\omega_0{}^2}}=\frac{1}{1+\frac{s}{Q\omega_0}+\frac{s^2}{\omega_0{}^2}} \tag{108}$$

$$Q=R\sqrt{\frac{C}{L}},\omega_0=\frac{1}{\sqrt{LC}} \tag{109}$$

3.3.5 The Model of PWM Modulator

DC/DC converter is controlled by variation of duty cycle. The modulator can change control voltage $v_c(t)$ to the pulse series of duty cycle $\hat{d}(t)$. The average output of PWM modulator $\delta(t)$ is $\langle\delta(t)\rangle_{T_s}$,

$$\langle\delta(t)\rangle_{T_s}=\frac{1}{T_s}\int_t^{t+T_s}\delta(\tau)=d(t) \tag{110}$$

$$d(t)=\frac{\langle v_c(t)\rangle_{T_s}}{V_M}\quad,0\le v_c(t)\le V_M \tag{111}$$

Introducing disturbance, the equation is,

$$\langle v_c(t)\rangle_{T_s}=V_c+\hat{v}_c(t) \tag{112}$$

$$d(t)=D+\hat{d}(t) \tag{113}$$

$$D+\hat{d}(t)=\frac{V_c+\hat{v}_c(t)}{V_M} \tag{114}$$

So, the dc equation and ac small signal equation are,

$$D=\frac{V_c}{V_M} \tag{115}$$

$$\hat{d}(t) = \frac{\hat{v}_c(t)}{V_M} \tag{116}$$

3.3.6 Feedback Controller Design

The transfer function of close-loop feedback controller is,

$$G(s) = \frac{C(s)}{R(s)} = \frac{a_m s^m + a_{m-1} s^{m-1} + \ldots + a_1 s + a_0}{b_n s^n + b_{n-1} s^{n-1} + \ldots + b_1 s + b_0} \tag{117}$$

$R(s)$ is the input of system, $C(s)$ is the output of system, $G(s)$ is the Laplace transformation of the ratio between the output and input. The transfer function can be factorized by the following form, in order to analyze the zero points and poles.

$$G(s) = \frac{K'(s-Z_1)(s-Z_2)\ldots(s-Z_m)}{s^i(s-P_1)(s-P_2)\ldots(s-P_n)} = \frac{K(1+T_1 s)(1+T_2 s)\ldots(1+T_m s)}{s^i(1+T_a s)(1+T_b s)\ldots(1+T_n s)} \tag{118}$$

$$\begin{aligned} G(j\omega) &= \left|G(j\omega)\right| \angle G(j\omega) = G(s)\Big|_{s=j\omega} \\ &= \frac{K(1+T_1 j\omega)(1+T_2 j\omega)\ldots(1+T_m j\omega)}{s^i(1+T_a j\omega)(1+T_b j\omega)\ldots(1+T_n j\omega)} \end{aligned} \tag{119}$$

The whole system can be described by frequency characteristics, and the diagram is shown in Fig.3.22,

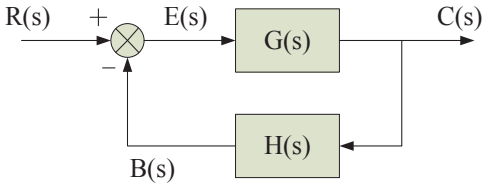

Fig. 3. 22 Close-loop control system diagram

In this diagram, the output $C(s)$ processes through $H(s)$ and obtains feedback signal $B(s)$. $B(s)$ deducts reference signal $R(s)$ is error signal $E(s)$. $E(s)$ processes though the controller $G(s)$ and obtain the output signal $C(s)$

$$C(s) = G(s)E(s) \tag{120}$$
$$B(s) = H(s)C(s) \tag{121}$$
$$E(s) = R(s) - B(s) \tag{122}$$
$$C(s) = G(s)R(s) - G(s)H(s)C(s) \tag{123}$$

$$\frac{C(s)}{R(s)} = \frac{G(s)}{1+G(s)H(s)} \tag{124}$$

$$F(s) = 1+G(s)H(s) = 0 \tag{125}$$

$F(s)$ is the Eigen equation of close-loop control system. $G(s)H(s)$ is called loop gain function, which equals to,

$$G(s)H(s) = G_c(s)G_m(s)G_{vd}(s)H(s) = G_c(s)G_o(s) \tag{126}$$

$$G_o(s) = G_m(s)G_{vd}(s)H(s) \tag{127}$$

The equation (5.11) is the system without compensation network. $G_m(s)$ is the transfer function of PWM modulator . $G_{vd}(s)$ is the transfer function from duty cycle to output voltage . $H(s)$ is feedback voltage divider network.

The transfer function of PWM modulator $G_m(s)$ is,

$$G_m(s) = \frac{\hat{d}(s)}{\hat{V}_c(s)} = \frac{1}{V_M} \tag{128}$$

The feedback voltage divider network $H(s)$ is,

$$H(s) = \frac{B(s)}{V(s)} = \frac{R_2}{R_1+R_2} \tag{129}$$

From the above equations, the loop gain without compensation network can be defined as,

$$G_o(s) = G_m(s)G_{vd}(s)H(s) = G_{vd}(s)\frac{1}{V_M}\frac{R_2}{R_1+R_2} \tag{130}$$

$$G_{vd}(s) = \frac{\hat{V}_o(s)}{\hat{d}(s)} = \frac{V_o}{D}\frac{1}{1+s\frac{L}{R}+s^2LC} \tag{131}$$

$$G_o(s) = G_m(s)G_{vd}(s)H(s) = \frac{R_2}{R_1+R_2}\frac{V_o}{DV_m}\frac{1}{1+s\frac{L}{R}+s^2LC} \tag{132}$$

3.4 Compensator Design

In all switching regulators, the output voltage $v(t)$ is a function of the input line voltage $v_g(t)$, the duty cycle $d(t)$, the load current $i_{load}(t)$, and the circuit element values. The controller is needed to compensate for input voltage variations, load current variations, tolerance in the values of circuit elements. It is desired to obtain a constant output voltage $v(t) = V$ in spite of the presence of disturbances to do this feedback control is required.

The conditions for instability are judged by gain margin and phase margin.

- Phase margin is the amount by which the total phase shift is less than 360° at the crossover frequency where the total gain is 1 or 0 dB.
- Gain margin is the amount by which the total gain is less than 1 or 0 dB at the frequency where the total phase shift is 360°.

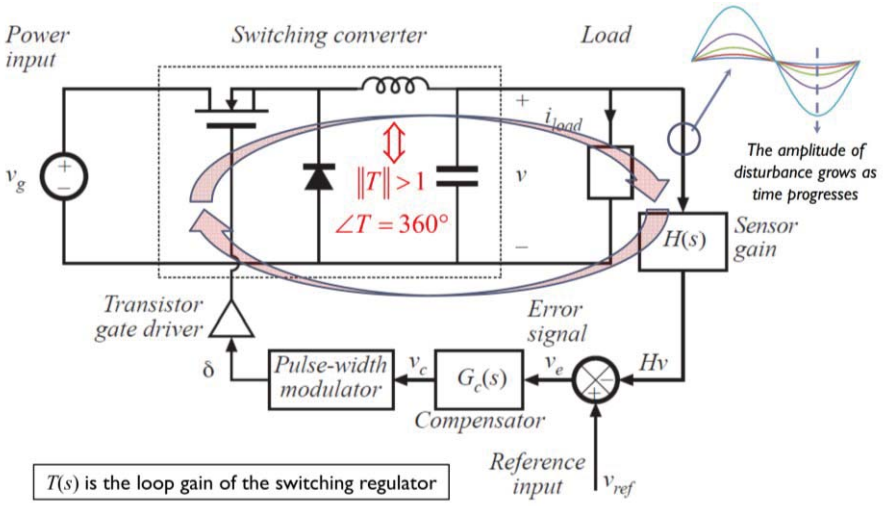

Fig. 3. 23 Condition for instability

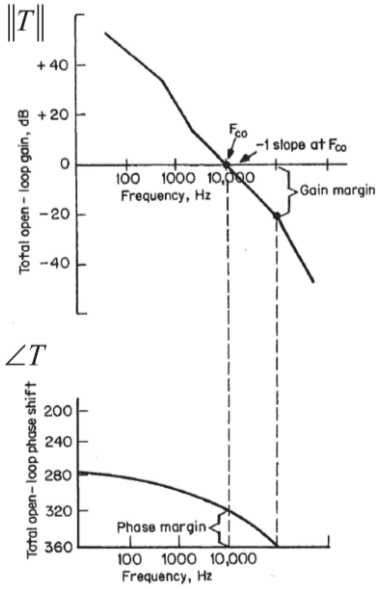

Fig. 3. 24 Phase margin and gain margin for stable system

The phase margin and gain margin are shown in Bode plots, which is a plot of the magnitude and phase of a transfer function or other complex-valued quantity versus frequency. Magnitude in decibels (dB) and phase in degrees ($^\circ$) are plotted versus frequency on semi-log scale. The magnitude of a complex-valued quantity A can be expressed as one of these forms,

$$\|A\|_{dB} = 20\log_{10}\left(\|A\|\right) \tag{133}$$

$$\|A\|_{dB\Omega} = 20\log_{10}\left(\|A\| / R_{base}\right) \tag{134}$$

$$\|A\|_{dB\mu V} = 20\log_{10}\left(\|A\| / V_{base}\right) \tag{135}$$

$$\|A\|_{dB\mu A} = 20\log_{10}\left(\|A\| / I_{base}\right) \tag{136}$$

The base value V_{base}, R_{base}, and I_{base} must be specified. A frequency encountered form of A when analyzing switching regulators is,

$$\|A\| = (\frac{f}{f_0})^n \Rightarrow \|A\|_{dB} = 20\log_{10}(\frac{f}{f_0})^n = 20n\log_{10}(\frac{f}{f_0}) \tag{137}$$

The unit increase of $\log_{10}(f)$ corresponds to a factor of 10, or one decade, increase in frequency. For example, a pure integrator, in the form of the pole at the origin is,

$$G(s)=\frac{1}{(\frac{s}{\omega_o})}\Rightarrow\|G\|_{dB}=20\log_{10}(\frac{f}{f_0})^{-1}=-20\log_{10}(\frac{f}{f_0}) \tag{138}$$

There are several Bode plots designed methods, single pole response, single zero response, right halt-plane zero, frequency inversion, second-order or quadratic pole response.

The shaping of $T(s)$ is achieved by appropriately designing the compensator network $G_c(s)$. Compensator network is used to shape the loop gain $T(s)$ and hence the closed-loop transfer functions of switching regulators in order to meet some performance specifications,

- Effect of load current variations

  This is used to limit the maximum allowable closed-loop output impedance

- Effect of input voltage variations

  This is used to limit the maximum allowable closed-loop line to output transfer function. And a typical case is to suppress the amplitude of variations at the second harmonic of the ac line frequency (100Hz or 120Hz)

- Transient response time

  This requires a sufficiently high crossover frequency

- Overshoot and ringing

  This requires an adequate phase margin

Lead proportional-plus-derivative (PD) compensator is used to improve phase margin. It is applied in system originally containing a two-pole response. To extend the bandwidth of the feedback loop while maintaining an acceptable phase margin, and $G_c(s)$ can be expressed as follows,

$$G_c(s)=G_{c0}\frac{(1+\frac{s}{\omega_z})}{(1+\frac{s}{\omega_p})} \tag{139}$$

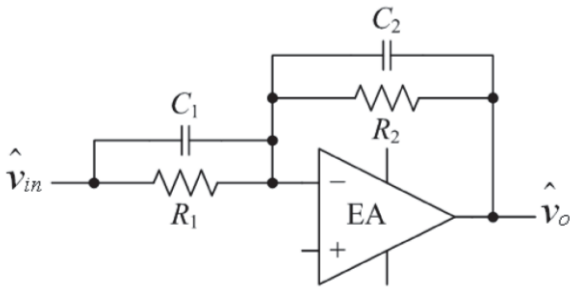

Fig. 3. 25 Structure of lead PD compensator

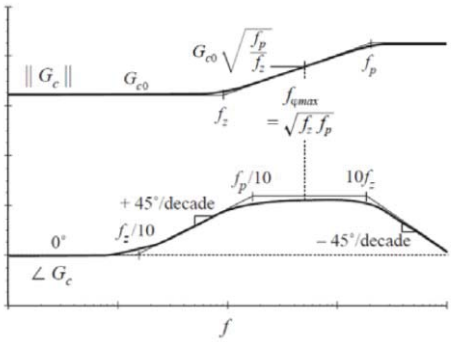

Fig. 3. 26 Phase margin and gain margin of PD compensator network

To obtain the maximum improvement in phase margin, the frequency $f_{\varphi\max}$ should coincide with the loop gain's crossover frequency f_c . This requires the placement of f_z and f_p at,

$$f_z = f_c\sqrt{\frac{1-\sin\theta}{1+\sin\theta}} \tag{140}$$

$$f_p = f_c\sqrt{\frac{1+\sin\theta}{1-\sin\theta}} \tag{141}$$

Where, $\theta = \angle G_c(f_{\varphi\max})$

When it is desired to avoid changing the crossover frequency, the magnitude of the compensator gain is chosen to be unity at the loop gain's crossover frequency $f_c = f_{\varphi\max}$,

$$\left\|G_c(f_{\phi\max})\right\| = G_{c0}\sqrt{\frac{f_p}{f_z}} = 1 \Rightarrow G_{c0} = \sqrt{\frac{f_z}{f_p}} \tag{142}$$

Therefore, the practical implementation of lead PD compensator with op-amp is,

$$\frac{\hat{v}_o}{\hat{v}_{in}} = -\frac{R_2}{R_1}\cdot\frac{(1+sR_1C_1)}{(1+sR_2C_2)} = G_{c0}\frac{(1+s/\omega_z)}{(1+s/\omega_p)} \tag{143}$$

with, $\|G_{c0}\| = \frac{R_2}{R_1}$, $\omega_z = \frac{1}{R_1C_1}$, $\omega_p = \frac{1}{R_2C_2}$

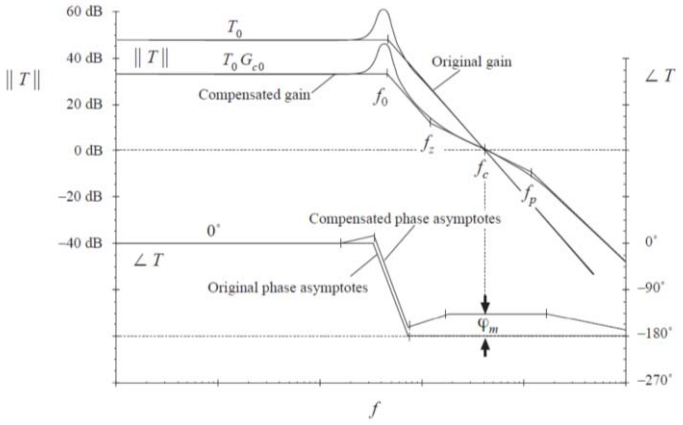

Fig. 3. 27 T(s) crosses 0 dB at -40 dB/decade

Lag proportional-plus-integral (PI) compensator is a type of compensator used to increase the low-frequency loop gain. It is especially effective for systems originally containing a single pole. If f_L is sufficiently lower than the loop crossover frequency f_c, the phase margin is unchanged.

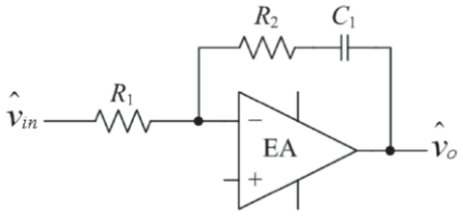

Fig. 3. 28 Structure of lag PI compensator

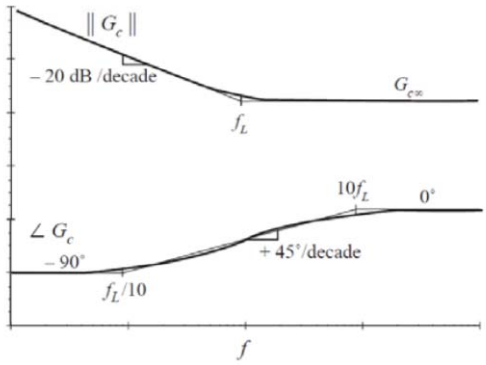

Fig. 3. 29 Phase margin and gain margin of PI compensator network

The compensator high-frequency $G_{c\infty}$ is chosen to obtain the desired crossover frequency f_c. For systems containing a single pole, it can be approximated the compensated loop gain by its high-frequency asymptote near the crossover frequency f_c,

$$T(s) = G_c(s)T_u(s) = G_{c\infty}(1+\frac{\omega_L}{s})\cdot T_{u0}(\frac{1}{1+s/\omega_0}) \approx \frac{G_{c\infty}T_{u0}}{f/f_0} \tag{144}$$

for f , $f_0 >> f_L$.

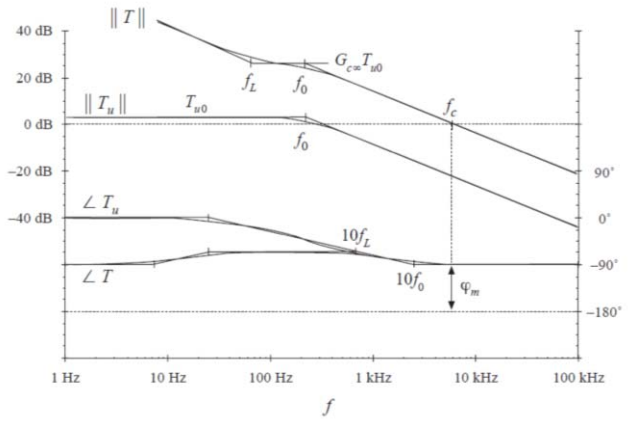

Fig. 3. 30 T(s) crosses 0 dB at -40 dB/decade

1At the crossover frequency $f = f_c$, the loop gain has unity magnitude, so the compensator gain $G_{c\infty}$ as,

$$\frac{G_{c\infty}T_{u0}}{(f_c/f_0)}=1\Rightarrow G_{c\infty}=\frac{f_c}{T_{u0}f_0} \tag{145}$$

The practical implementation of lag PI compensator with op-amp is,

$$\frac{\hat{v}_o}{\hat{v}_{in}}=-\frac{R_2}{R_1}\cdot\frac{(1+sR_1C_1)}{(1+sR_2C_2)}=G_{c\infty}\frac{(1+s/\omega_L)}{s/\omega_L} \tag{146}$$

with, $\|G_{c\infty}\|=\frac{R_2}{R_1}$, $\omega_L=\frac{1}{R_1C_1}$, $\omega_p=\frac{1}{R_2C_2}$

Combined the advantages of lag PI and lead PD compensator, proportional-integral-derivative (PID) compensator is proposed to obtain wide bandwidth of feedback loop and zero steady-state error. The high-frequency poles at f_{p1} and f_{p2} cause the gain to roll off at high frequencies to prevent the switching ripple from disrupting the operation of the pulse width modulator.

$$G_c(s)=G_{cm}\frac{(1+\frac{\omega_L}{s})(1+\frac{s}{\omega_z})}{(1+\frac{s}{\omega_{p1}})(1+\frac{s}{\omega_{p2}})} \tag{147}$$

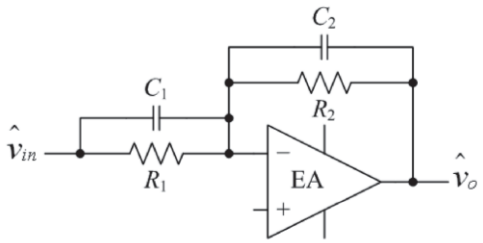

Fig. 3. 31 Structure of PID compensator

The practical implementation of PID compensator with op-amp is,

$$\frac{\hat{v}_o}{\hat{v}_{in}}=-\frac{R_3}{R_1}\cdot\frac{(1+1/sR_3C_3)}{(1+sR_3C_3)}\cdot\frac{(1+sR_1C_1)}{1+sR_2C_1}=G_{cm}\frac{(1+\omega_L/s)}{(1+s/\omega_{p1})}\cdot\frac{(1+s/\omega_z)}{(1+s/\omega_{p2})} \tag{148}$$

With $\|G_{cm}\|=\frac{R_3}{R_1}$, $\omega_L=\frac{1}{R_3C_3}$, $\omega_z=\frac{1}{R_1C_1}$, $\omega_{p1}=\frac{1}{R_3C_2}$, $\omega_{p2}=\frac{1}{R_2C_1}$

The advantage of this method is there are many degrees of freedom with PID control, so we

limit the scope by choosing $C_3 >> C_2$, $R_1 >> R_2$. The specifications of designed PID compensator are crossover frequency ≤ 5 kHz, the peak overshoot $\leq 16\%$, and phase margin $\geq 52°$. As the above requirements, the functions are as follows,

$$G_{vd}(s) = \frac{V}{D}\frac{1}{1+s\frac{L}{R}+s^2LC} \tag{149}$$

$$G_{vg}(s) = D\frac{1}{1+s\frac{L}{R}+s^2LC} \tag{150}$$

The standard form is,

$$G_{vd}(s) = G_{d0}\frac{1}{1+\frac{Ls}{Q_0\omega_0}+(\frac{s}{\omega_0})^2} \tag{151}$$

$$G_{vg}(s) = G_{g0}\frac{1}{1+\frac{s}{Q_0\omega_0}+\left(\frac{s}{\omega_0}\right)^2} \tag{152}$$

The salient features are,

$$G_{d0} = \frac{V}{D} \tag{153}$$

$$f_0 = \frac{\omega_0}{2\pi} = \frac{1}{2\pi\sqrt{LC}} \tag{154}$$

$$Q_0 = R\sqrt{\frac{C}{L}} \tag{155}$$

The output impedance is,

$$Z_{out}(s) = R\left\|\frac{1}{sC}\right\|sL = \frac{sL}{1+s\frac{L}{R}+s^2LC} \tag{156}$$

The total open-loop gain is,

$$T(s) = G_c(s)(\frac{1}{V_M})G_{vd}(s)H(s) = \frac{G_c(s)H(s)}{V_M}\frac{V}{D}\frac{1}{1+\frac{s}{Q_0\omega_0}+(\frac{s}{\omega_0})^2} = T_{u0}$$

(157)

With $G_c = 1$, the loop gain is,

$$T_u(s) = T_{u0} \frac{1}{1 + \frac{s}{Q_0 \omega_0} + (\frac{s}{\omega_0})^2} \tag{158}$$

$$T_{u0} = \frac{HV}{DV_M} \tag{159}$$

The uncompensated loop gain $T_u(s)$ has phase of approximately $-180°$ at the desired crossover frequency f_c. Compensated loop gain $T(s) = G_c(S)T_u(s)$ with lead compensator only is,

$$T(s) = T_{u0} G_{c0} \frac{(1 + \frac{s}{\omega_z})}{(1 + \frac{s}{\omega_p})(1 + \frac{s}{Q_0 \omega_0} + (\frac{s}{\omega_0})^2)} \tag{160}$$

Including lag compensator is,

$$G_c(s) = G_{cm} \frac{(1 + \frac{s}{\omega_z})(1 + \frac{\omega_L}{s})}{(1 + \frac{s}{\omega_p})} \tag{161}$$

The inverted zero to PD compensator is added without changing dc gain or corner frequencies. In order to keep the phase margin unchanged, $f_L = f_c / 10$.

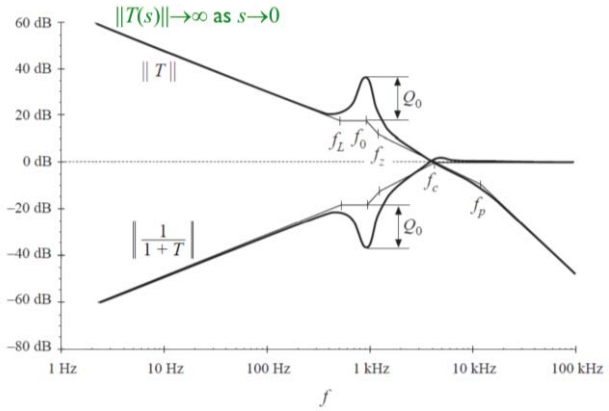

Fig. 3. 32 Compensated loop gain T(s) with lead-lag PID compensator network

Chapter 4 Simulation

4.1 MATLAB and SIMULINK

Millions of engineers and scientists worldwide use MATLAB to analyze and design the systems and products. MATLAB is in automobile active safety systems, interplanetary spacecraft, health monitoring devices, smart power grids, and LTE cellular networks. It is used for machine learning, signal processing, image processing, computer vision, communications, computational finance, control design, robotics, and much more.

4.2 Conventional PID Controller Simulation

The purpose of analyze this chapter is to tune PID controllers, develop it based on the most general structure of Mamdani type [106] of fuzzy systems, and improve the quality of the control systems. Proportional-integral-derivative controller is widely used in industrial area, because of its stability, robust performance, and simplicity. The design of PID controller needs three factors, proportional gain, integral value, and derivative value, which is shown in Fig. 4.1. Proportional gain depends on present errors, integral factor depends on accumulation of past errors, and derivative factor is a prediction of further errors. K_p is used for decreasing the rise time, K_i is used for reducing the overshoot and setting time, and K_d is used for eliminating the steady-state errors.

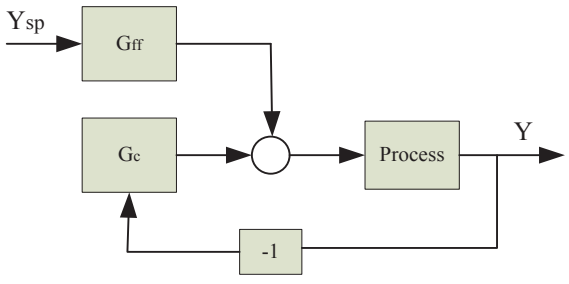

Fig. 4. 1 Diagram of PID control method

The calculation procedure of fuzzy PID is as follows,

$$u(x) = K_p \cdot e(t) + \frac{1}{T_i}\int e(t)dt + T_D \frac{d}{dt}e(t) \tag{162}$$

$$e(t) = r_{in}(t) \text{-} r_{out}(t) \tag{163}$$

$$e(t) = bysp(t) - y(t) \tag{164}$$

$$G_{ff} = K_p \left[b + \frac{1}{sT_i} + T_d \right] \tag{165}$$

$$U(s) = \left[K_p + \frac{K_i}{s} + K_d s \right] E(s) \tag{166}$$

There are four characteristics to evaluate the performance of PID controller, rise time, overshoot time, setting time steady state error, when tuning and calculating three factors. The requirements of PID controller is trying to minimize the rise time, overshoot time, and setting time, and limit the steady state error within 1%. The merits of PID controller are simple structure, stability, reliability, convenience for tuning.

Drawbacks of PID controller are that PID is not good enough for non-linear and complex systems. When parameters are calculated, the whole control process can be hardly changed. In the practical situation, parameter change always happens, so PID controller cannot obtain the optimum efficiency, especially in complex systems. When the structure or parameters of controlled object is not accurate, or when the accurate mathematic model cannot be established, other technologies of control theory is hardly being applied. In this situation, the most suitable control method is PID controller.

The structure and parameters of system controller can only be determined by experience and tuning. In this situation, PID control method is the most convenient technology. It means if we cannot mathematically describe a model and controlled object or cannot accurately measure parameters of the whole system, the best choice is to use PID controller. Tuning is the process of finding appropriate parameters for the PID controller, and it determines the overall performance of control loop. The steps to tune PID controller is as follows,

1. Set the T_i = infinity and $T_d = 0$.

2. Set the gain $K_p = 0$

3. Increase the K_p value until there are sustained oscillations in the control system.

4. The P value should be set to the half of that value

5. Increase I until any offset is corrected in sufficient time for the process

The transfer function of PID controller is,

$$G_c = K_p + K_i / s + K_d s \tag{167}$$

The equivalent equation is,

$$G_c = K_p \left[1 + \frac{1}{sT_i} + T_d \right] \tag{168}$$

Where, $T_i = K_p / K_i$, $T_d = K_d / K_p$

The discrete time equivalent equation is given as,

$$u(k) = K_p \cdot e(k) + K_i T_s \sum_{i=1}^{n} e(i) + \frac{K_d}{T_s} \Delta e(k) \tag{169}$$

$u(k)$ is the control signal, $e(k)$ is the error between the reference setting and actual output. And $\Delta e(k) \overset{\Delta}{=} e(k) - e(k-1)$. The factors can be tuned in order to produce various response curves.

There are several steps to simulate conventional PID controller,

1. Modelling the hardware circuit using PWM waveform generators (without controller) to test the hardware model as shown in Fig 4.2.

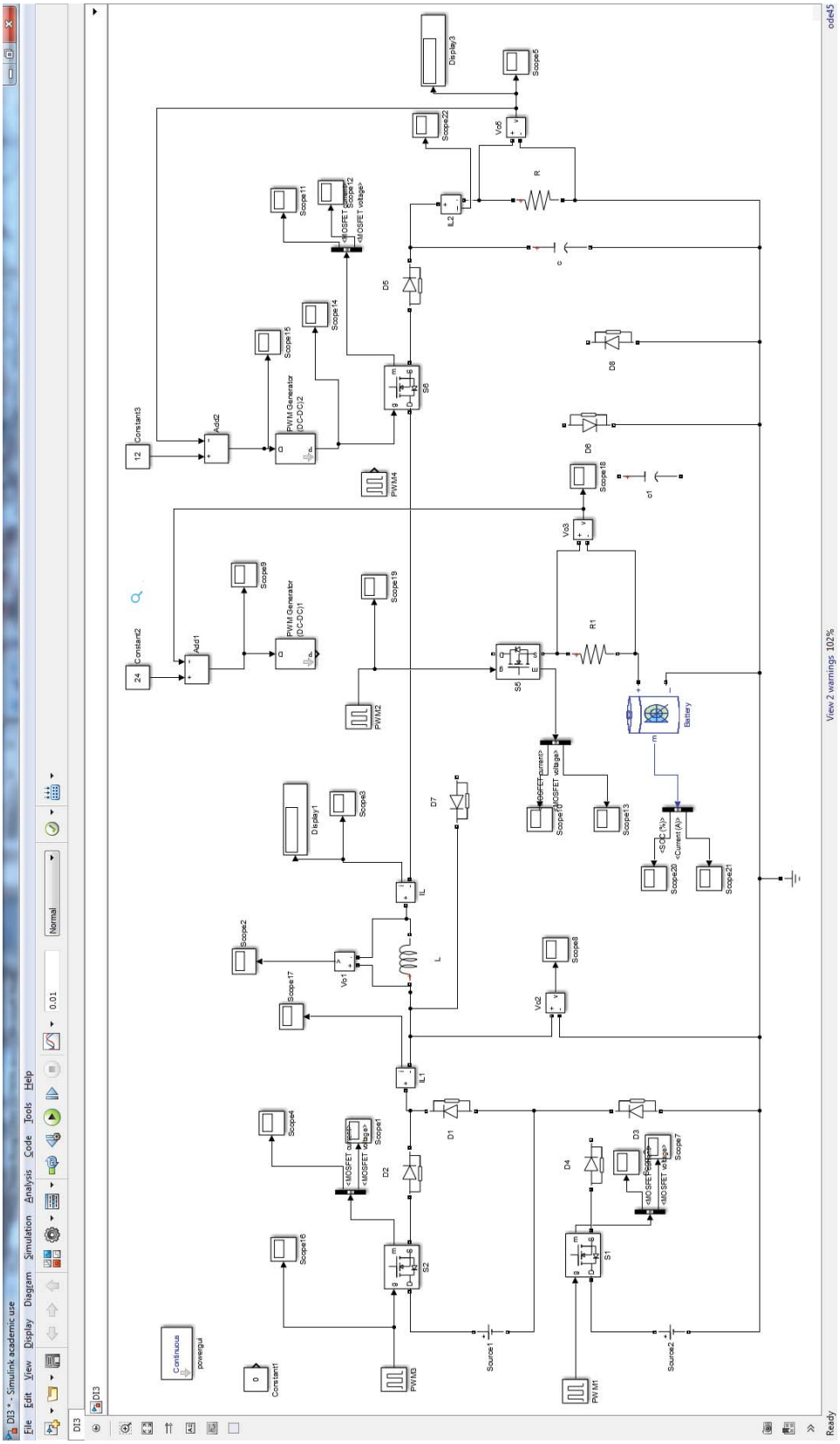

Fig. 4. 2 Hardware circuit modelling

2. Modelling the hardware circuit using Simulink for four operation modes, single input single output, dual input single output, and dual input with battery, as shown in the following Fig. 4.3 to Fig. 4.5.

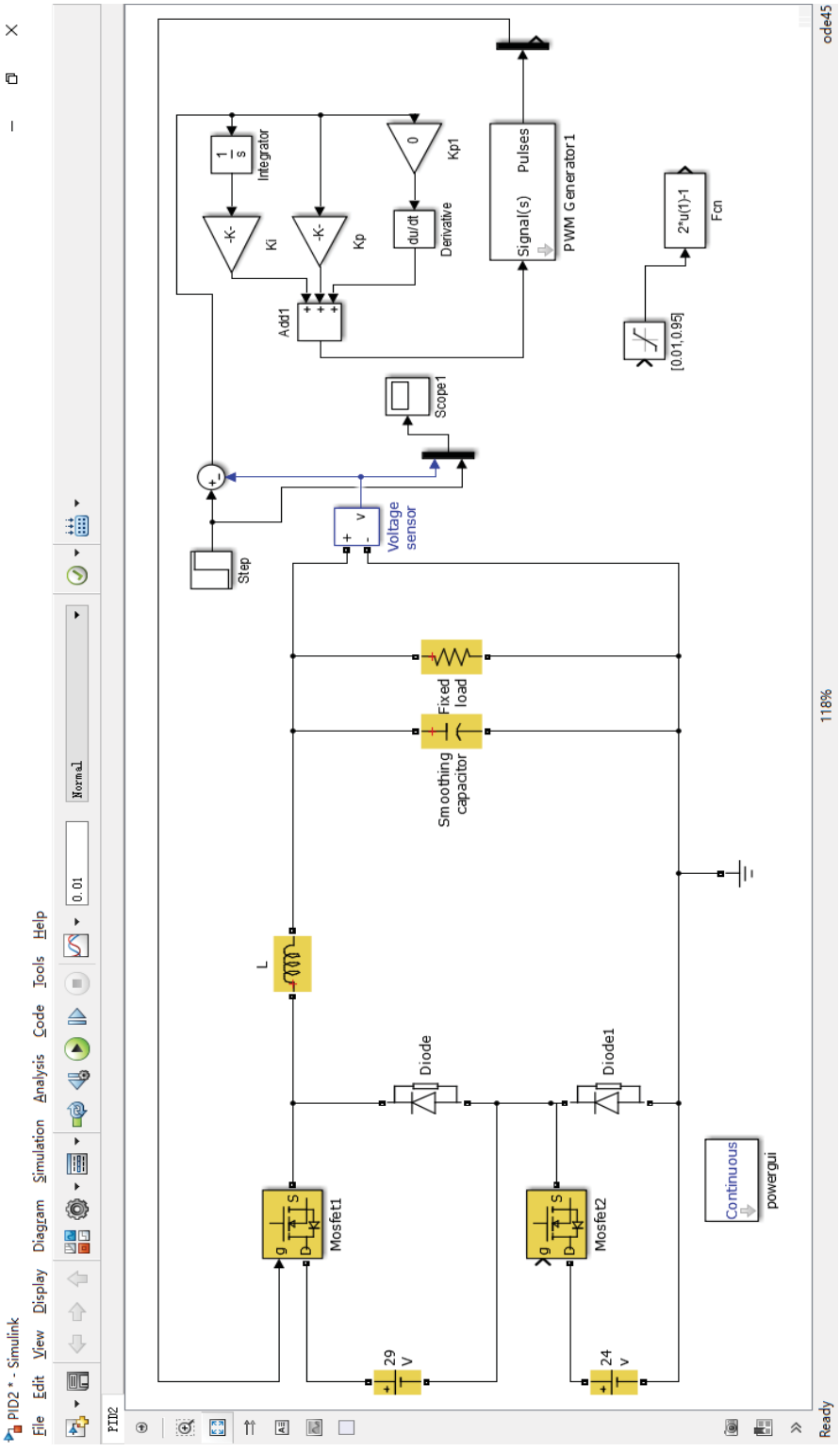

Fig. 4. 3 Single-input single-output simulation

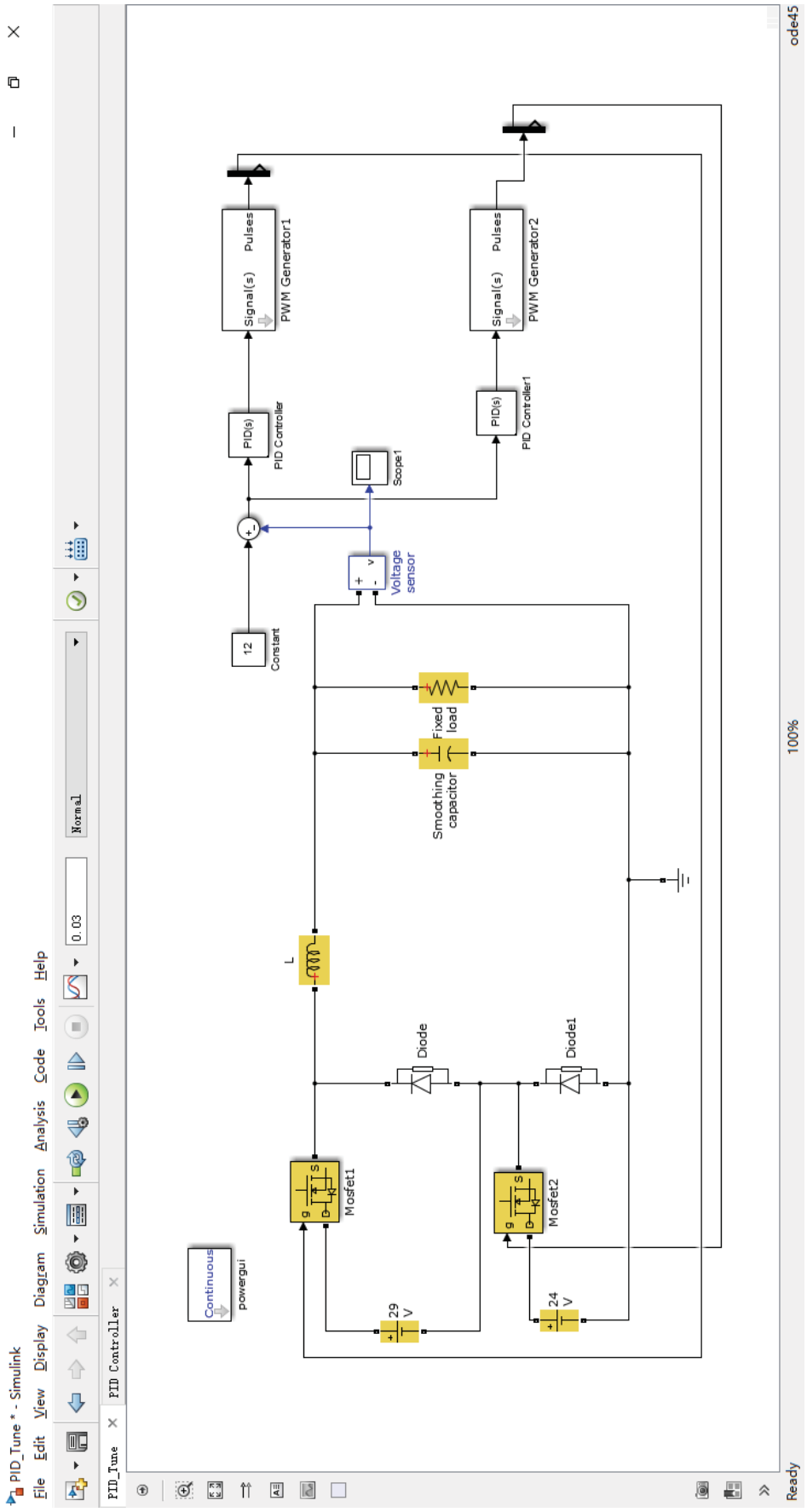

Fig. 4. 4 Dual-input single output simulation

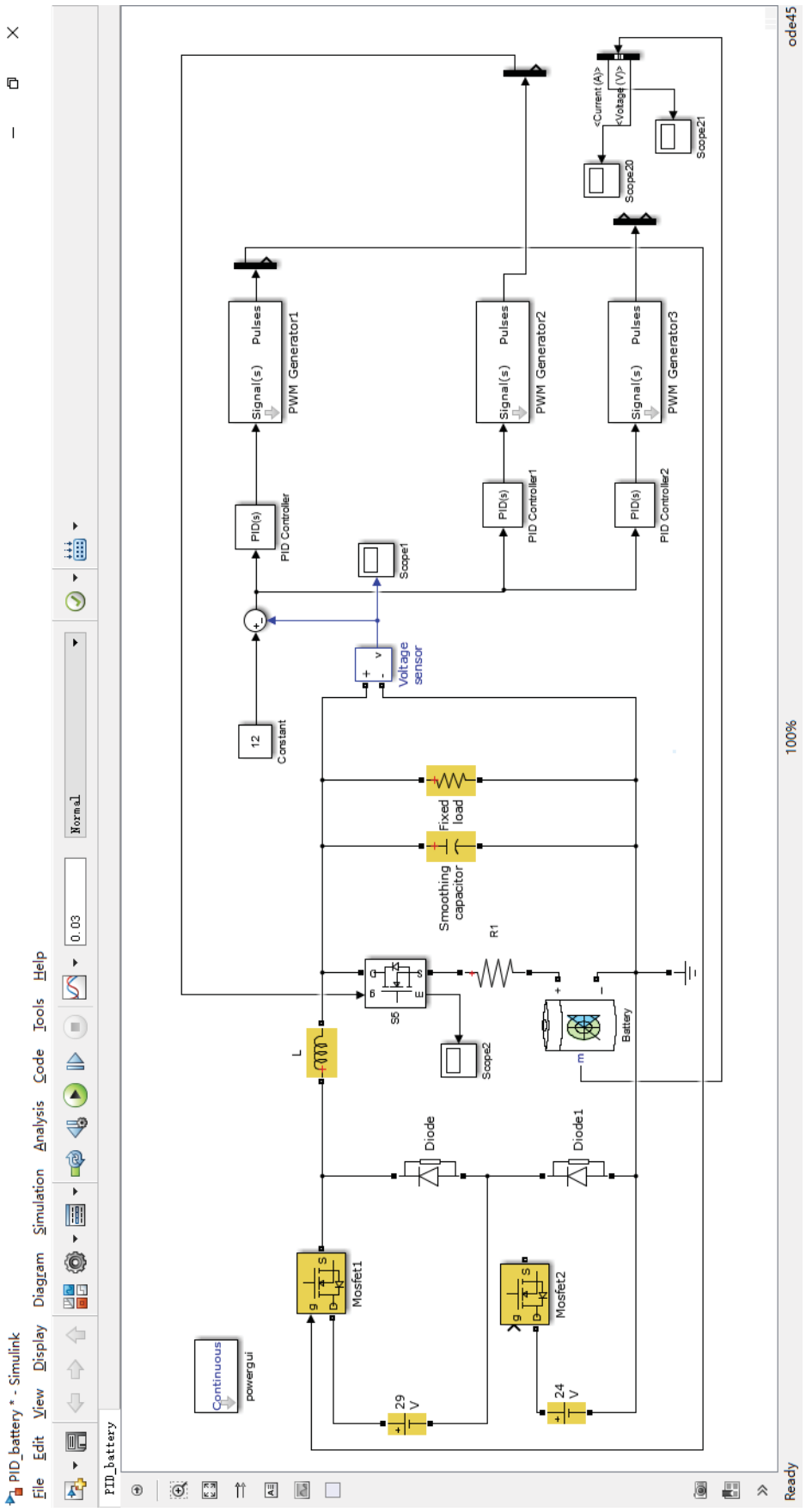

Fig. 4. 5 Dual-input with battery simulation

3. Setting the components parameters

TABLE IV THE PARAMETERS USED FOR SIMULATION

Components	Value
Input voltage 1	29 V
Input voltage 2	24 V
Output voltage	12V
Inductance	100 μH
Capacitance	220 μF
Switches	MOSFET
Switching Frequency	100 kHz

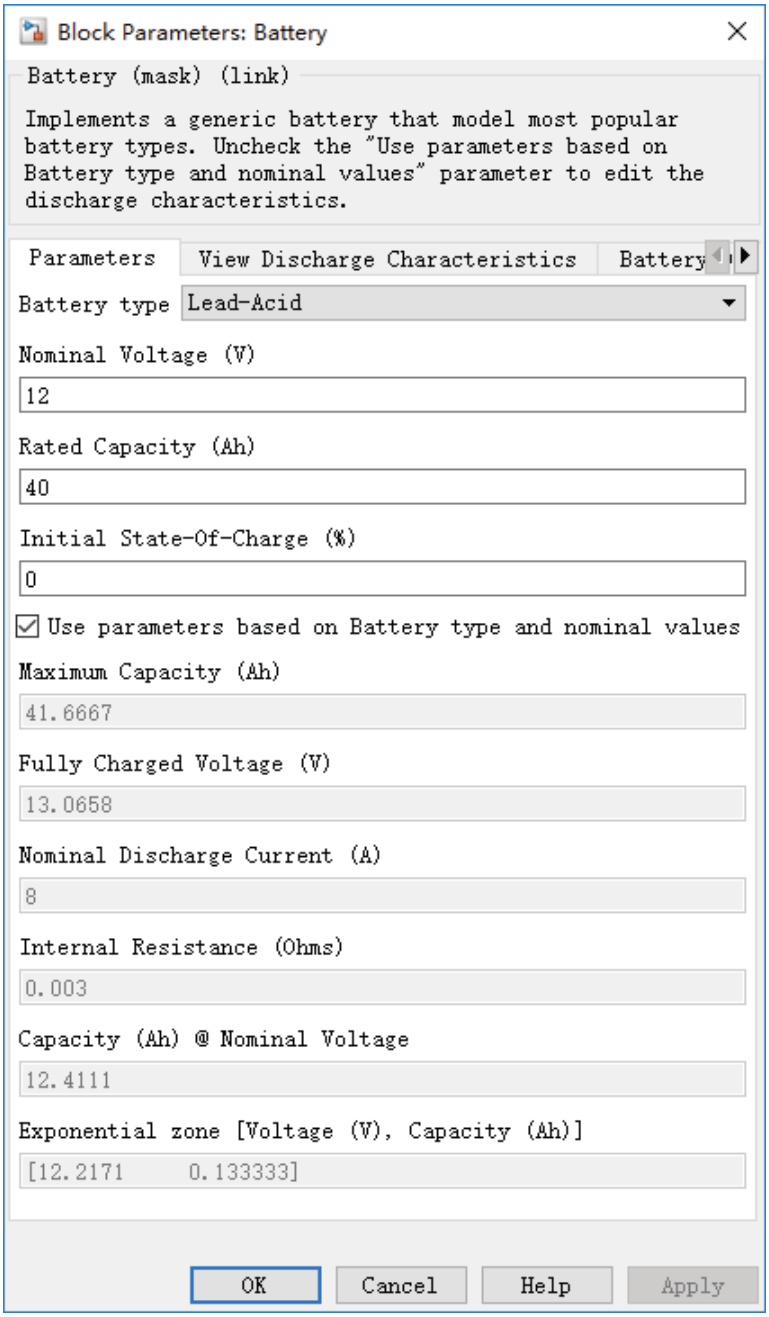

Fig. 4. 6 Parameters applied for battery

4. Setting the values of three PID factors

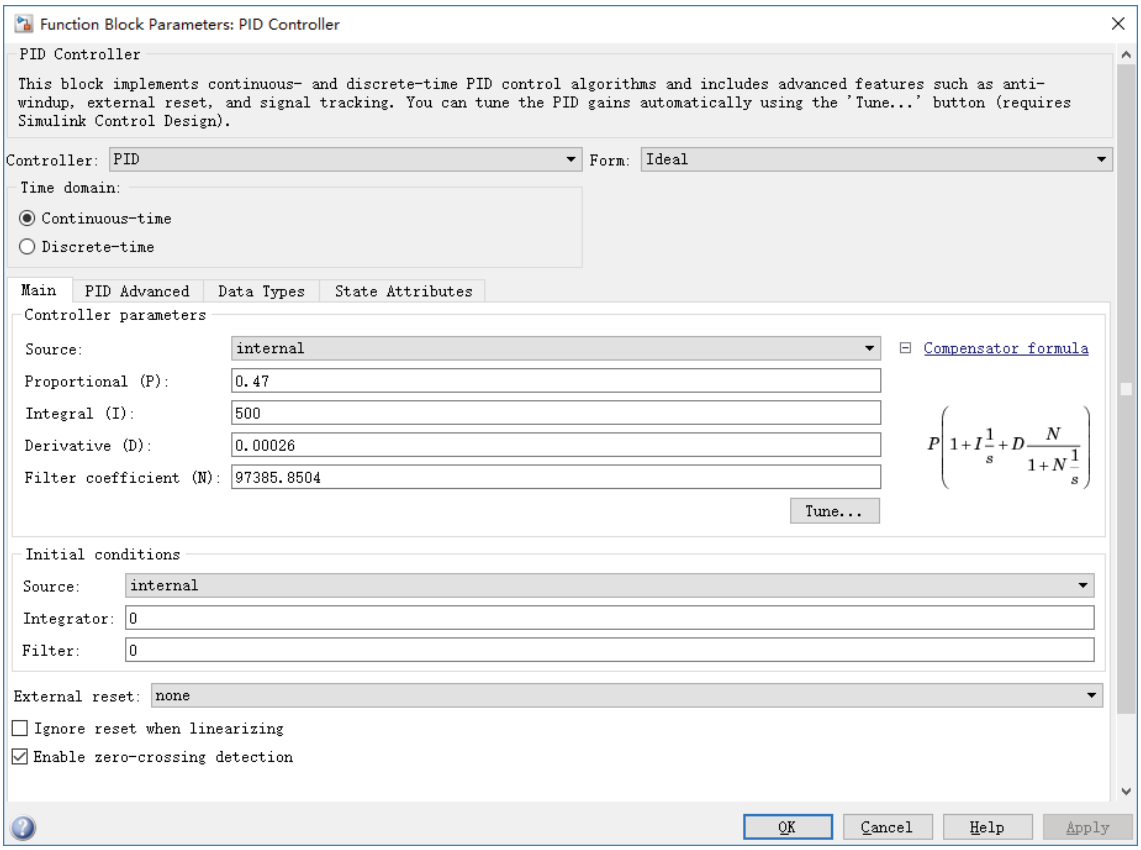

Fig. 4. 7 Parameters used for conventional PID control simulation

5. The key waveforms

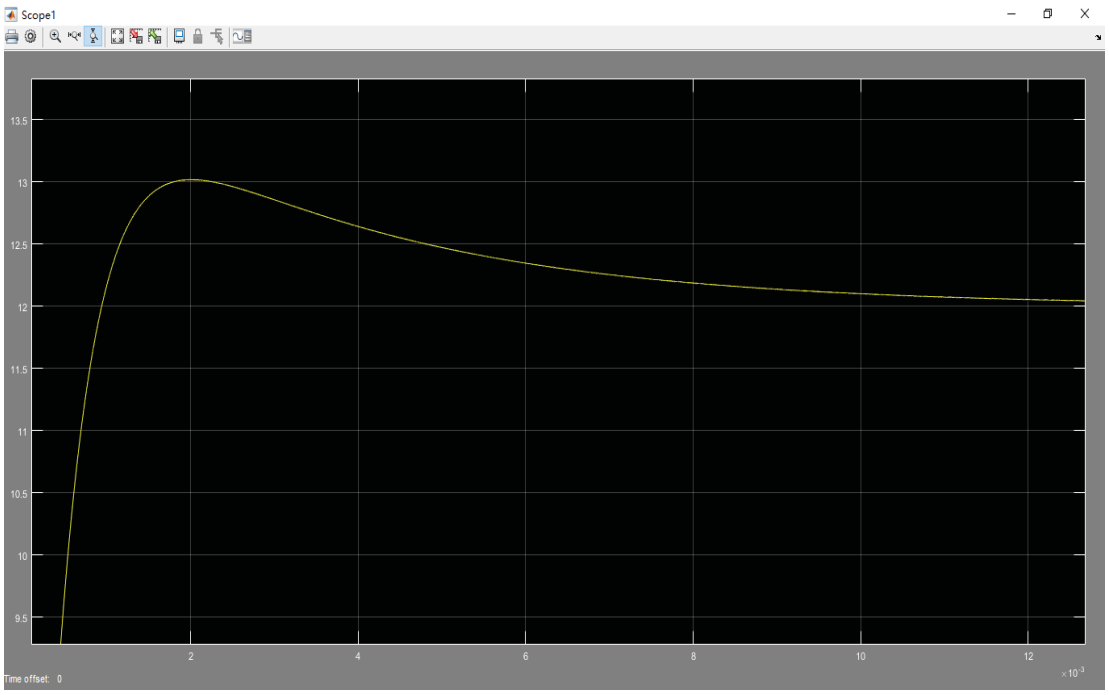

Fig. 4. 8 Output voltage v_{out} ($0.5\,V\,/\,div$, time scale: $2\,ms\,/\,div$) of single-input single-output mode

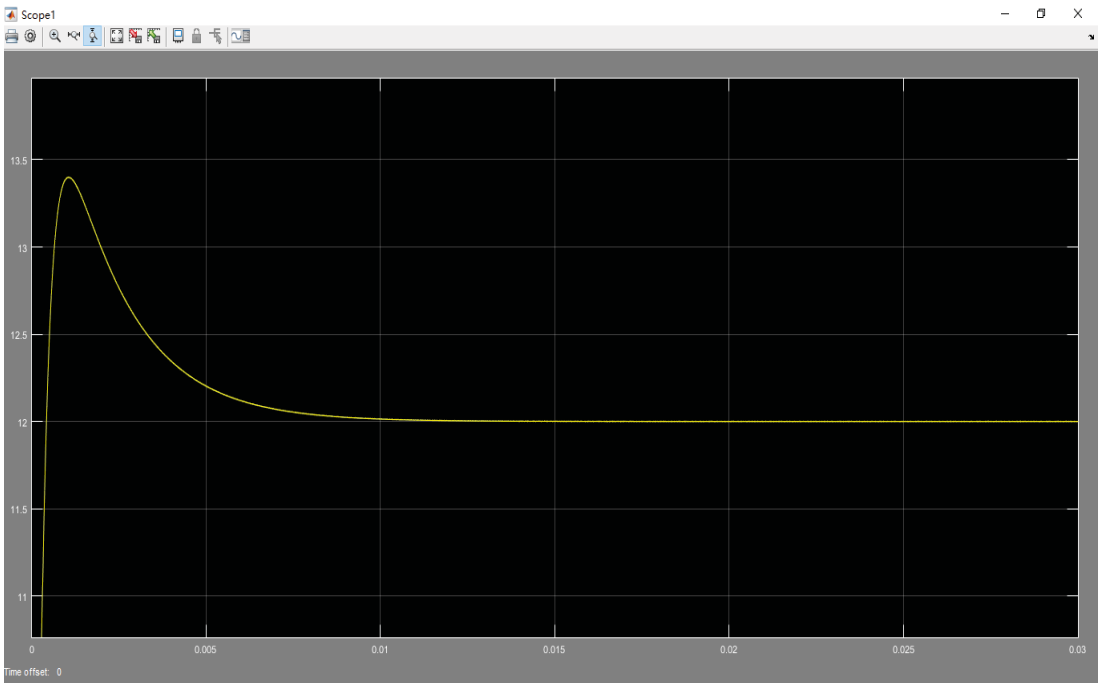

Fig. 4. 9 Output voltage v_{out} ($0.5\,V\,/\,div$, time scale: $5\,ms\,/\,div$) of dual-input single-output mode

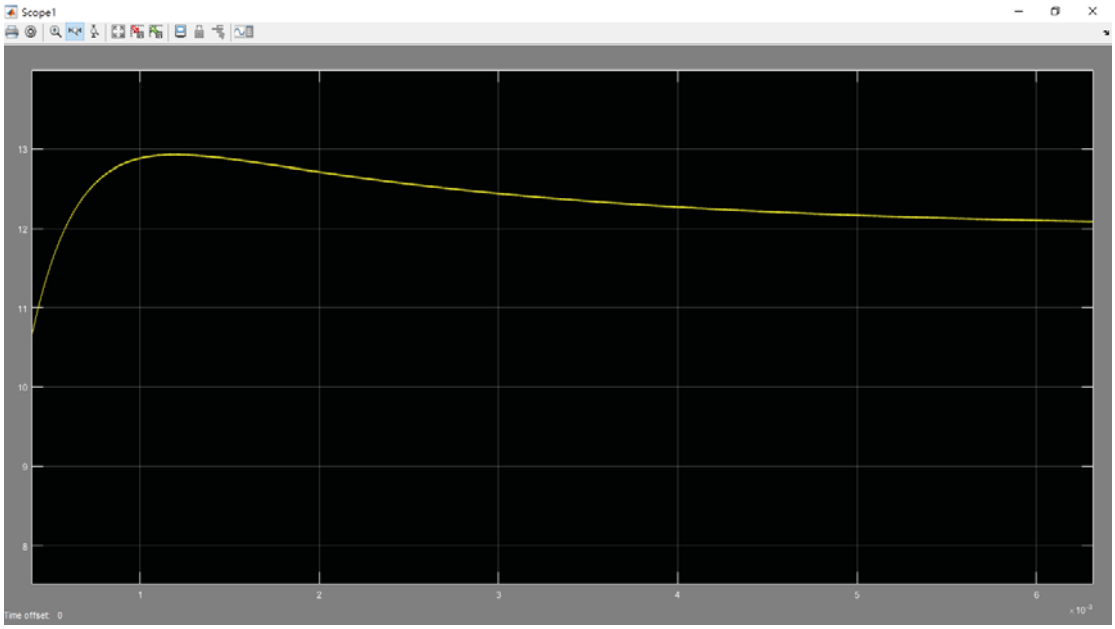

Fig. 4. 10 Output voltage v_{out} ($0.5\,V/div$, time scale: $1\,ms/div$) of dual-input dual-output mode with battery

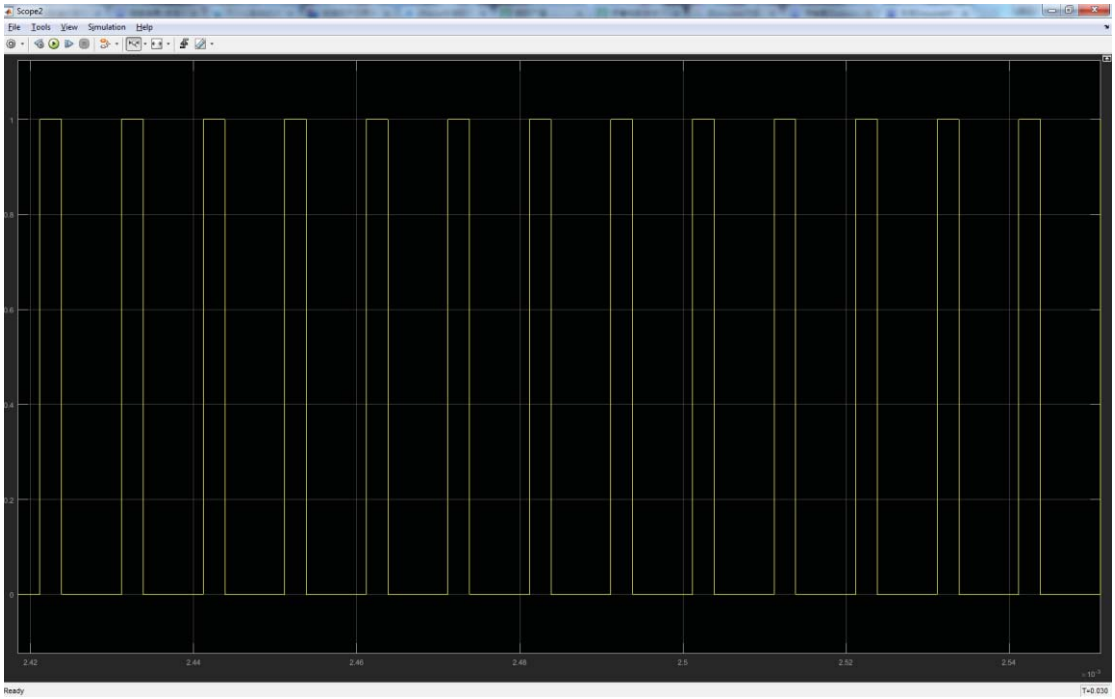

Fig. 4. 11 Drive signal v_{gate} ($0.2\,V/div$, time scale: $0.1\,\mu s/div$) for power switch

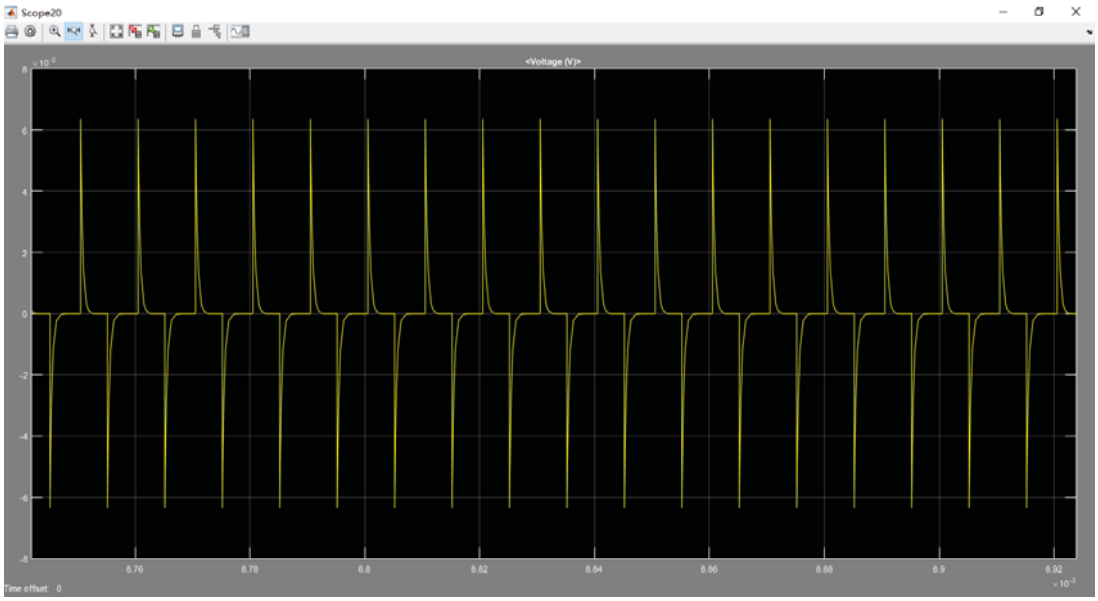

Fig. 4. 12 Battery voltage $v_{battery}$ (2 mV / div , time scale: 0.1 μs / div)

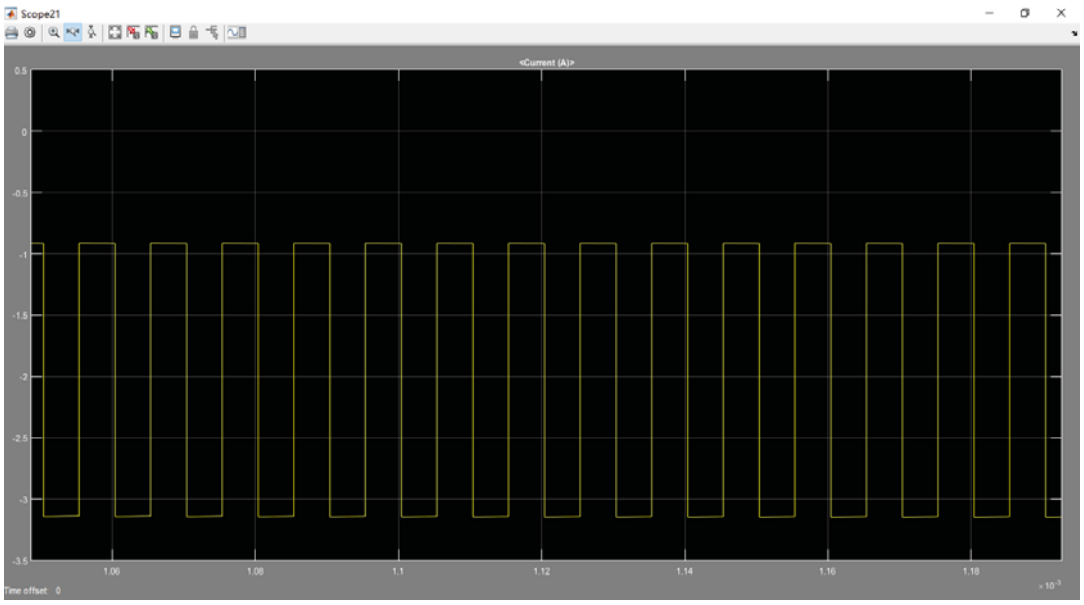

Fig. 4. 13 Battery current $i_{battery}$ (0.5 A / div , time scale: 0.2 μs / div)

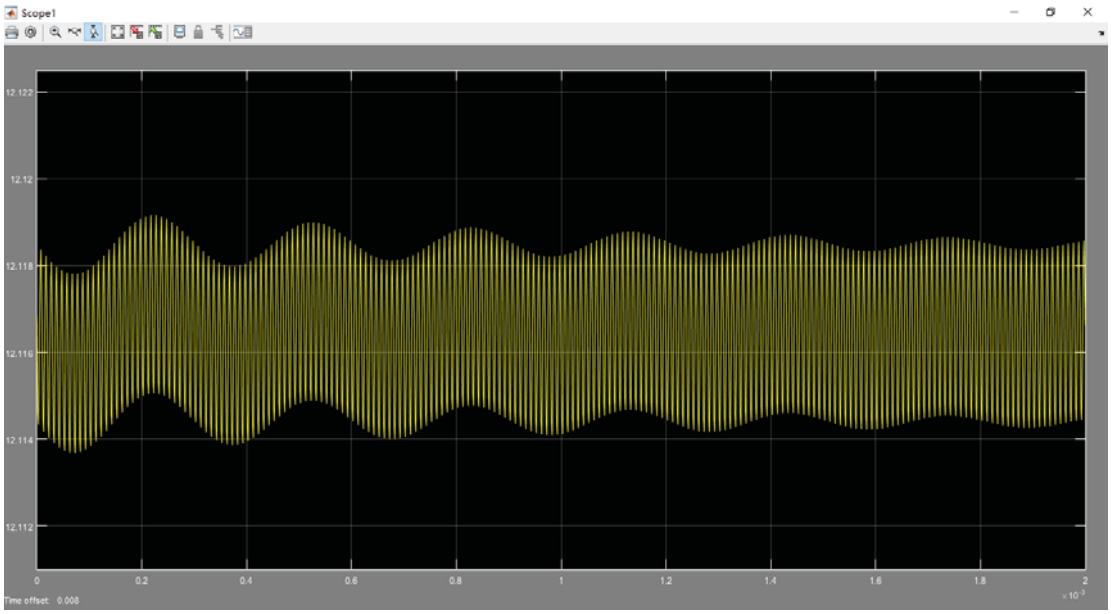

Fig. 4. 14 Amplified stable output voltage v_{out} (2 mV/div, time scale: 0.2 ms / div)

4.3 Fuzzy PID Controller Simulation

This part describes the development of process control of fuzzy scheduling scheme of PID controller. Fuzzy logic rules are applied for determining the controller parameters and reasoning procedures based on error signal and difference.

The intelligent PID control method is combined intelligent control with traditional PID control. This design concept is using expert system (ES), fuzzy control, and neural network technologies to introduce human intelligence into controller design in the form of nonlinear control, which makes the system, achieve the optimum performance. It does not dependent on the accurate mathematic model and the structure and parameter of controller. Good robustness to variable parameter of the whole system is achieved.

Fuzzy PID is a kind of intelligent PID controller. In the fuzzy controller, the linguistic description of human expertise in process is presented as fuzzy rules or fuzzy relations. It is based on inference mechanism related to measured responses. However, they have no clear structure of PID controllers. Fuzzy logic can be considered as a nonlinear PID controller with parameters determined by online error signal and time derivatives and difference.

Fuzzy PID control method uses the present error E and EC, combined with the dynamic characteristics of controlled object and practical experience. According to the requirements and target function, three parameters of PID controller are tuned online by fuzzy rules inference. It has more advantages than traditional PID control in practical situation. Fig.4.2 shows the approach to apply fuzzy rules and reasoning procedures to generate factors of fuzzy PID controller.

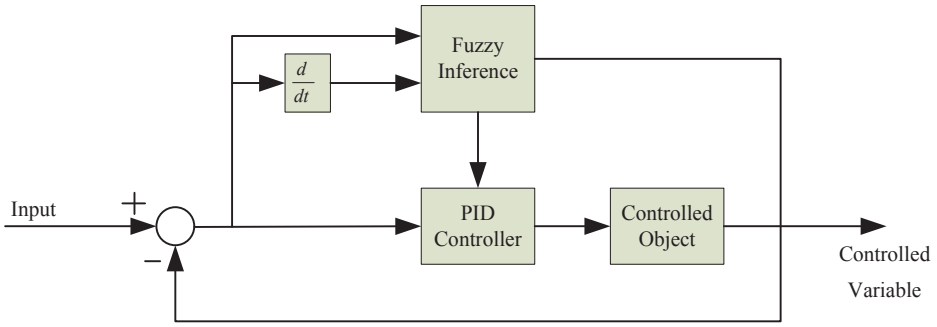

Fig. 4. 15 Fuzzy PID controller diagram

The factors K_p, K_i and K_d are limited in the ranges $[K_{p,\min}, K_{p,\max}]$, $[K_{i,\min}, K_{i,\max}]$, $[K_{d,\min}, K_{d,\max}]$, respectively. The K_p and K_d are normalized into the range between minus three and three by the linear functions as follows,

$$K_p' = (K_p - K_{p,\min}) / (K_{p,\max} - K_{p,\min}) \tag{170}$$

$$K_d' = (K_d - K_{d,\min}) / (K_{d,\max} - K_{d,\min}) \tag{171}$$

The three factors of PID are determined by the difference between current error $e(k)$ and first difference $\Delta e(k)$. The integral time constant is determined by derivative reference value, which is,

$$T_i = \alpha T_d \tag{172}$$

And the integral factor is,

$$K_i = K_p / (\alpha T_d) = K_p^2 / (\alpha K_d) \tag{173}$$

The variations K_p, K_d and α are determined by a set of fuzzy rules of the specific form,

If $e(k)$ is A_i and $\Delta e(k)$ is B_i, then $K_p^{'}$ is C_i, $K_d^{'}$ is D_i, and $\alpha = \alpha_i (1 = 1,2,3,\cdots,m)$

The membership functions of fuzzy sets A_i, B_i, C_i, D_i for $e(k)$ and $\Delta e(k)$ are shown as following figure,

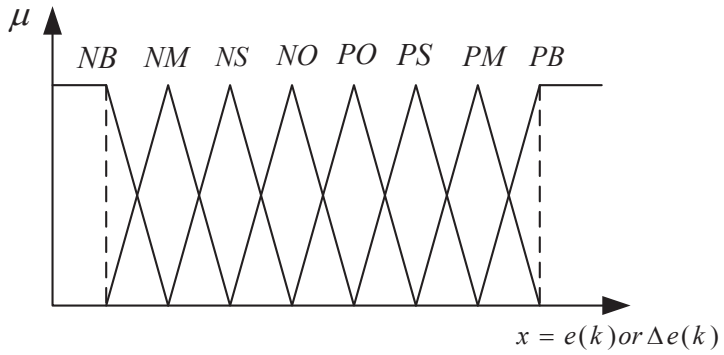

Fig. 4. 16 Membership function

In this figure, B represents big, S represents small, M represents medium, PO represents approximately positive zero, NO represents approximately negative zero. P represents positive, and N represents negative. The requirement of designed controller is shown as following plots,

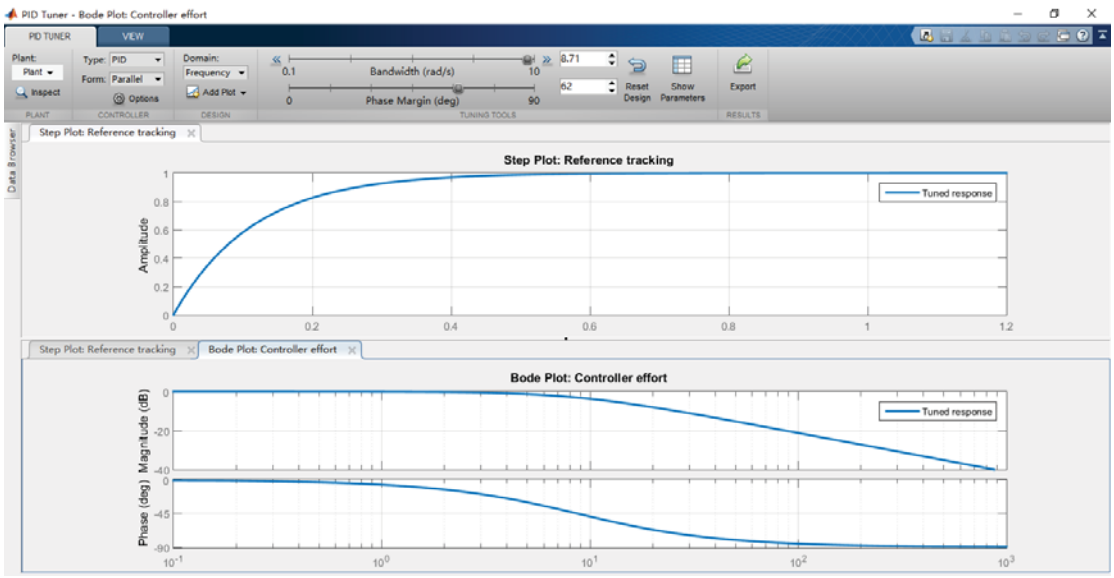

Fig. 4. 17 The Bode plots of stable control system

Defuzzification equations are,

$$K_p^{'} = \sum_{i=1}^{m} \mu_i K_{p,i}^{'} \tag{174}$$

$$K_d^{'} = \sum_{i=1}^{m} \mu_i K_{d,i}^{'} \tag{175}$$

$$\alpha = \sum_{i=1}^{m} \mu_i \alpha_i \tag{176}$$

The fuzzy set A_i gives the value to $e(k)$ and B_i gives the value to $\Delta e(k)$.

There are several steps to simulate Fuzzy PID controller,

1. Modelling the hardware circuit using Simulink for different operation modes, dual input single output, and single input single output, as shown in the following Fig. 4.18.

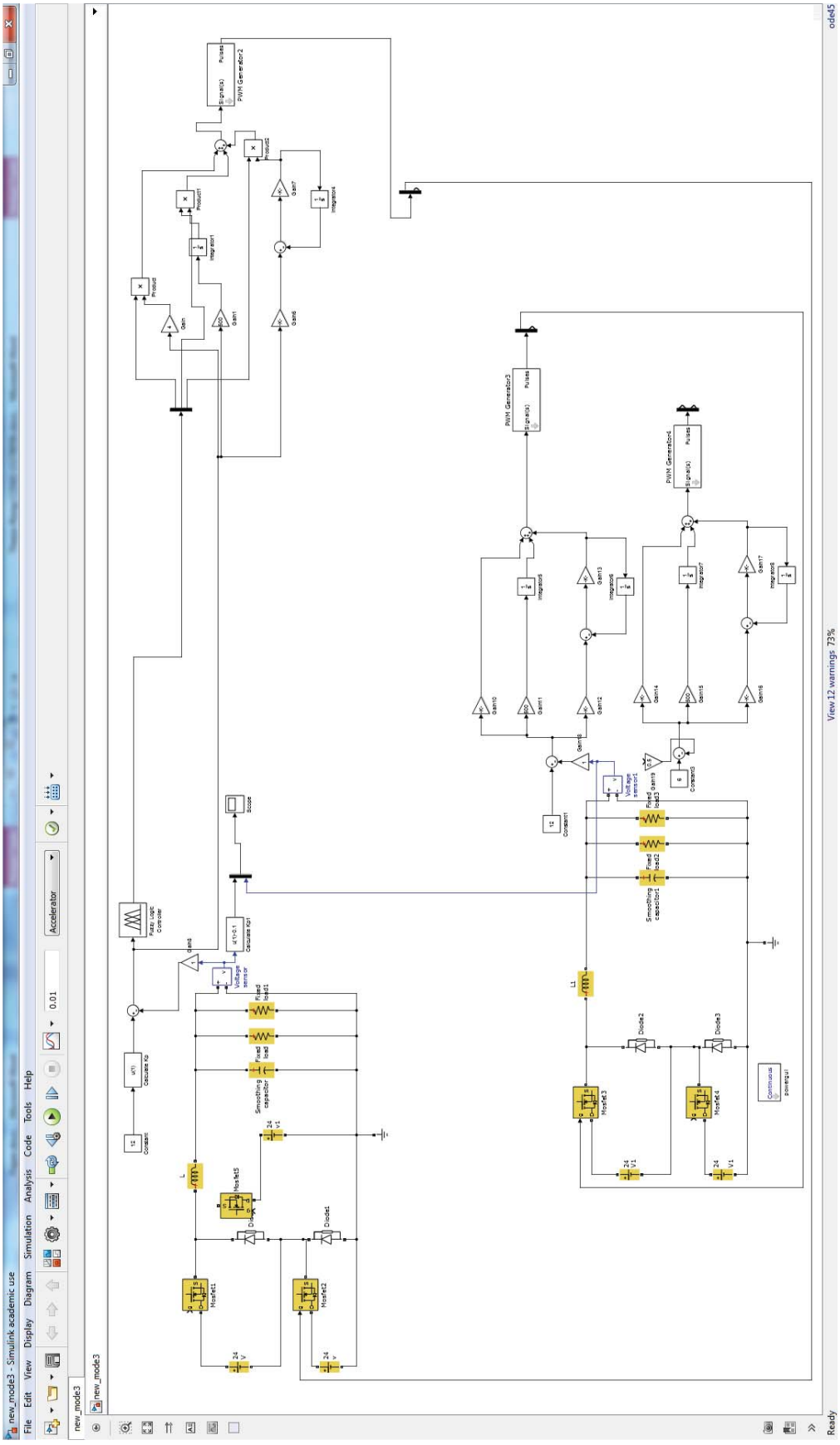

Fig. 4. 18 Fuzzy PID controller modeling for single-input mode

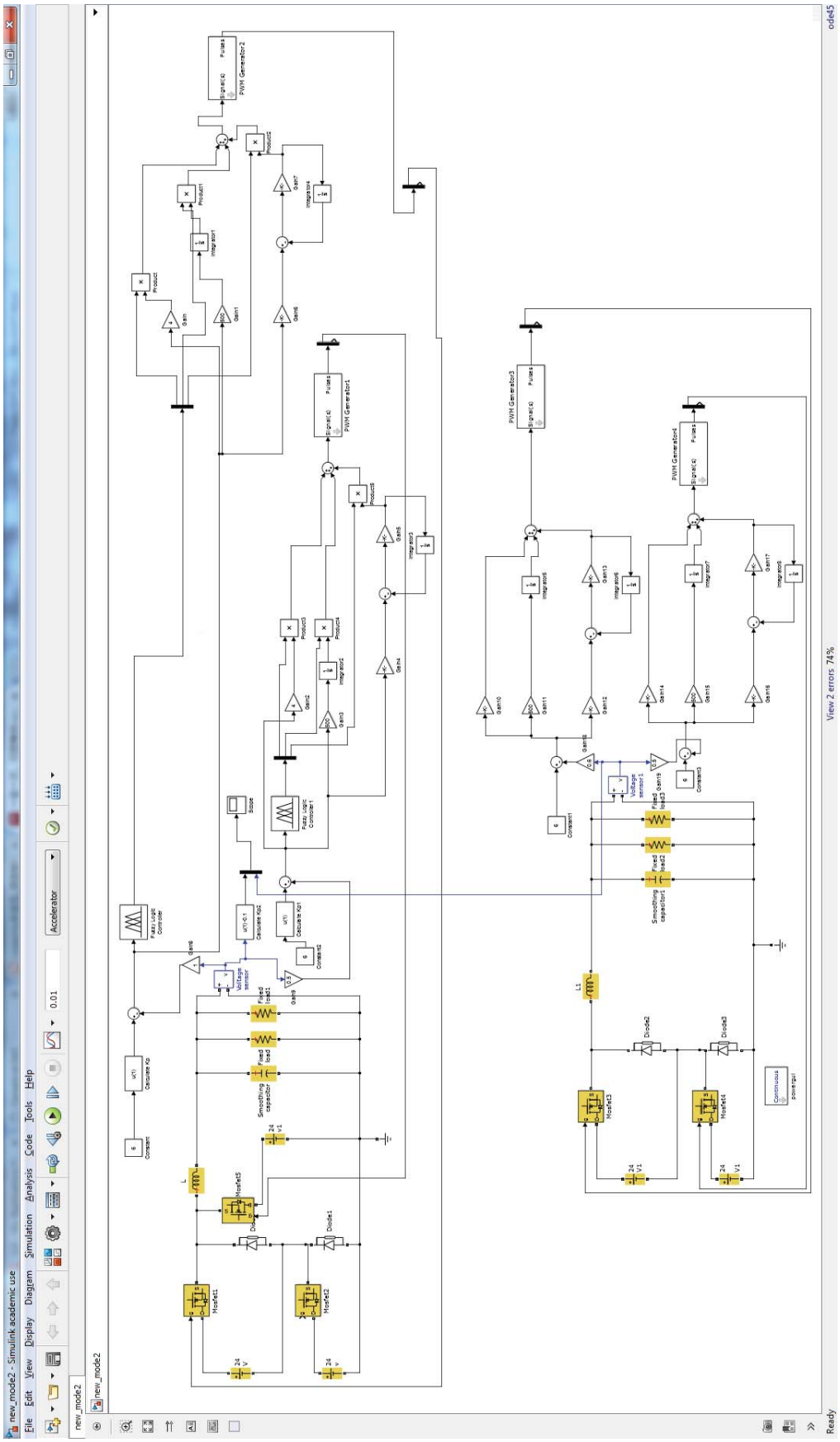

Fig. 4. 19 Fuzzy PID controller modeling for dual-input mode

2. Programming and setting fuzzy membership functions to optimize the performance of controller for single input mode. This mode is used for single input single output mode. $e(k)$ is the calculating error, $\Delta e(k)$ is the error changing rate of the system, and Cu is the self-tuning output membership function.

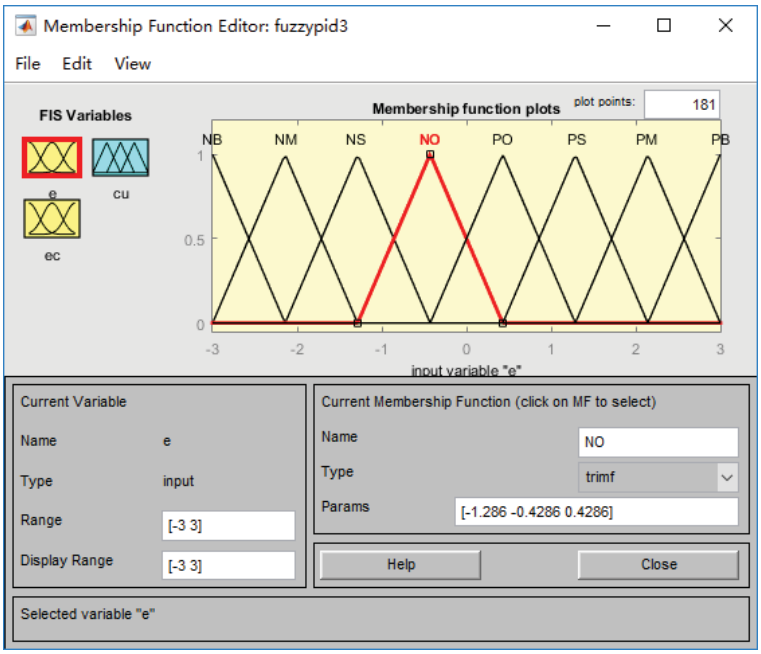

Fig. 4. 20 Membership function plots for $e(k)$

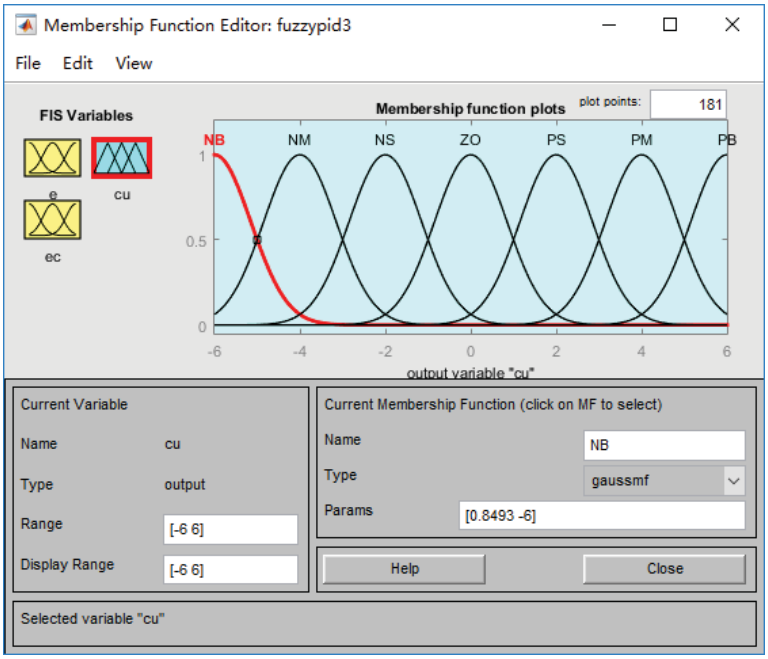

Fig. 4. 21 Membership function plots for Cu

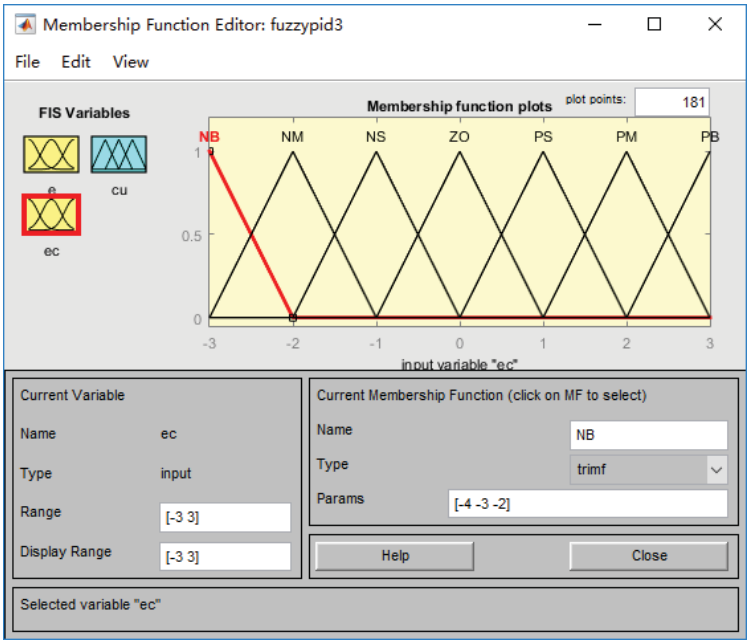

Fig. 4. 22 Membership function plots for $\Delta e(k)$

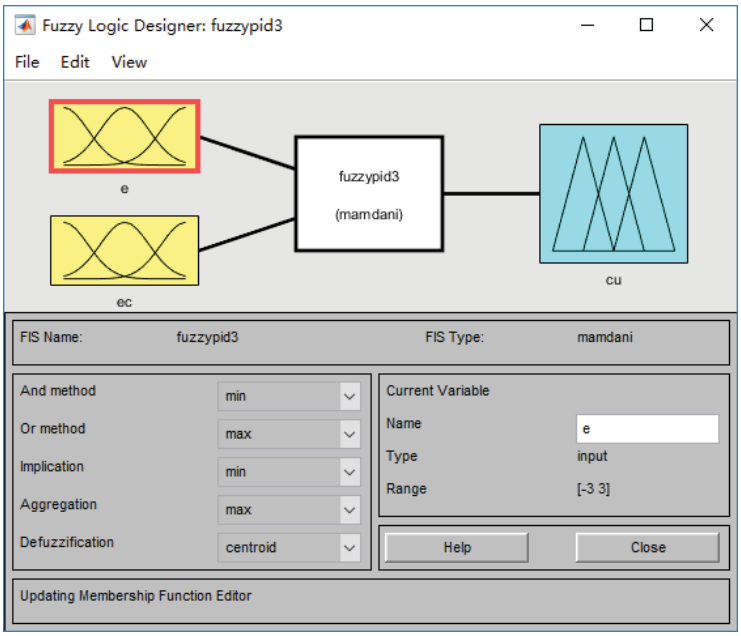

Fig. 4. 23 Membership function editor for the single input mode corresponding relationship and parameters

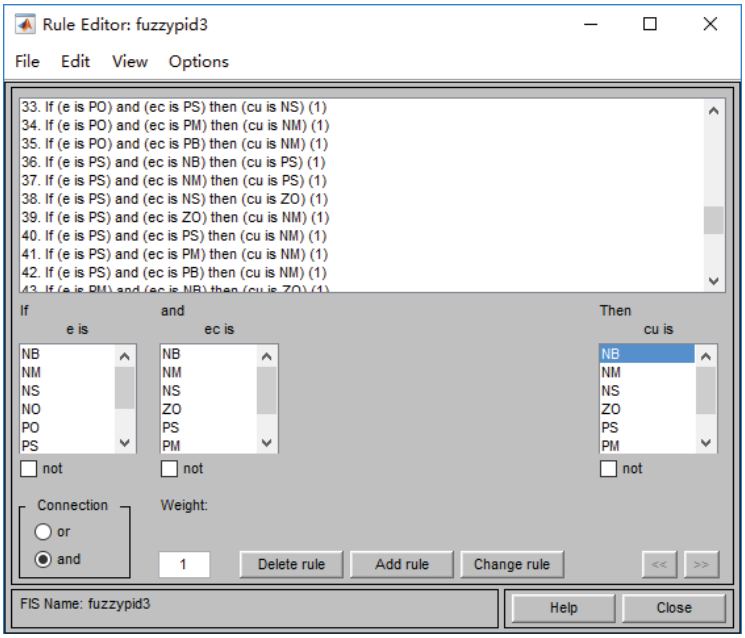

Fig. 4. 24 Basic rules of fuzzy PID controller for single input mode converter

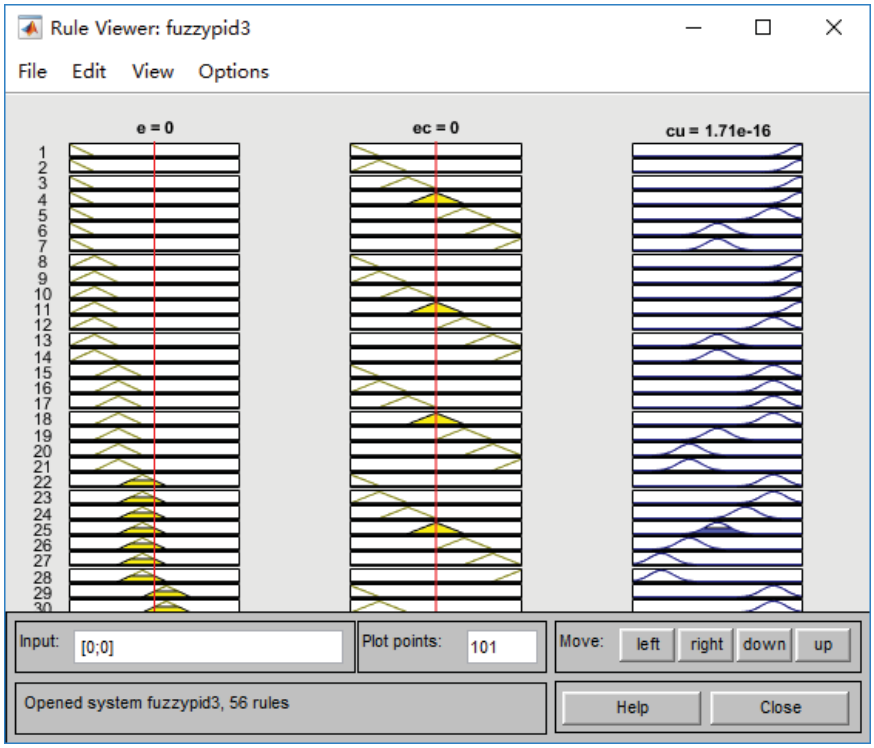

Fig. 4. 25 Fuzzy rules viewer in MATLAB for single input mode

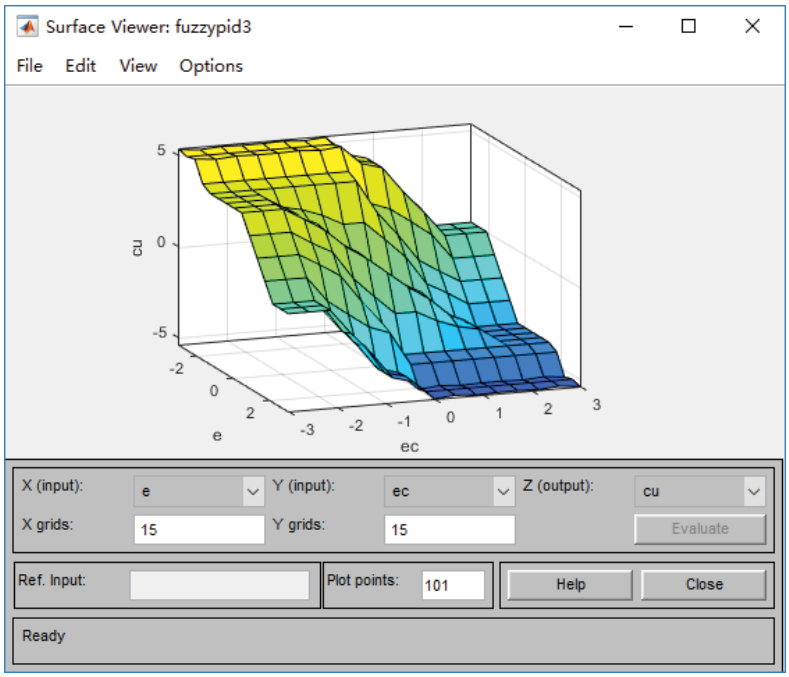

Fig. 4. 26 Fuzzy rules 3D surface for single input mode of fuzzy PID controller

The following table is the detail corresponding fuzzy inference system for adaptive calculating error and error changing rate.

TABLE V FUZZY INFERENCE SYSTEM FOR ADAPTIVE OUTPUT

	$\Delta e(k)$							
$e(k)$	$\mu(k)$	NB	NM	NS	ZO	PS	PM	PB
	NB	PB	PB	PB	PB	PM	ZO	ZO
	NM	PB	PB	PB	PB	PM	ZO	ZO
	NS	PM	PM	PM	PM	ZO	NS	NS
	ZO	PM	PM	PS	ZO	NS	NM	NM
	PS	PS	PS	ZO	NM	NM	NM	NM
	PM	ZO	ZO	NM	NB	NB	NB	NB
	PB	ZO	ZO	NM	NB	NB	NB	NB

3. Import data and parameters into MATLAB workspace and read the determined fuzzy

inference system documents. Setting the fuzzification type is Mamdani, and the defuzzification type is centroid.

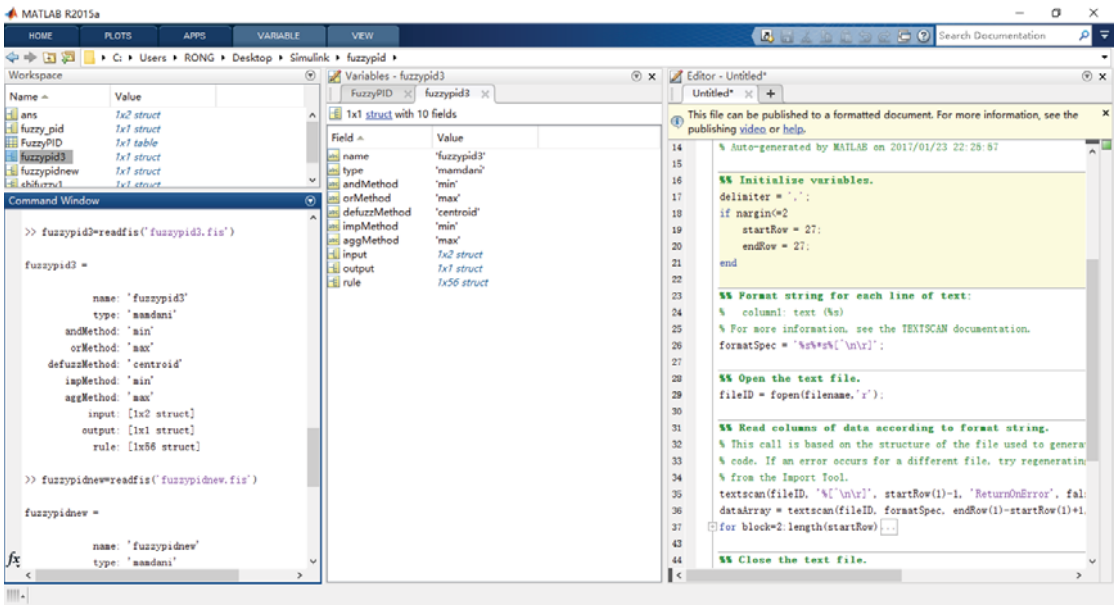

Fig. 4. 27 MATLAB Workspace of fuzzy inference system for single input mode

4. Programming and setting fuzzy membership functions to optimize the performance of controller for dual input mode. The qualitative relationship between control error and error changing rate and three control factors of PID controller are shown as following figures. The K_{pp}, K_{ip}, and K_{dp} are change of K_p, K_i, and K_d respectively.

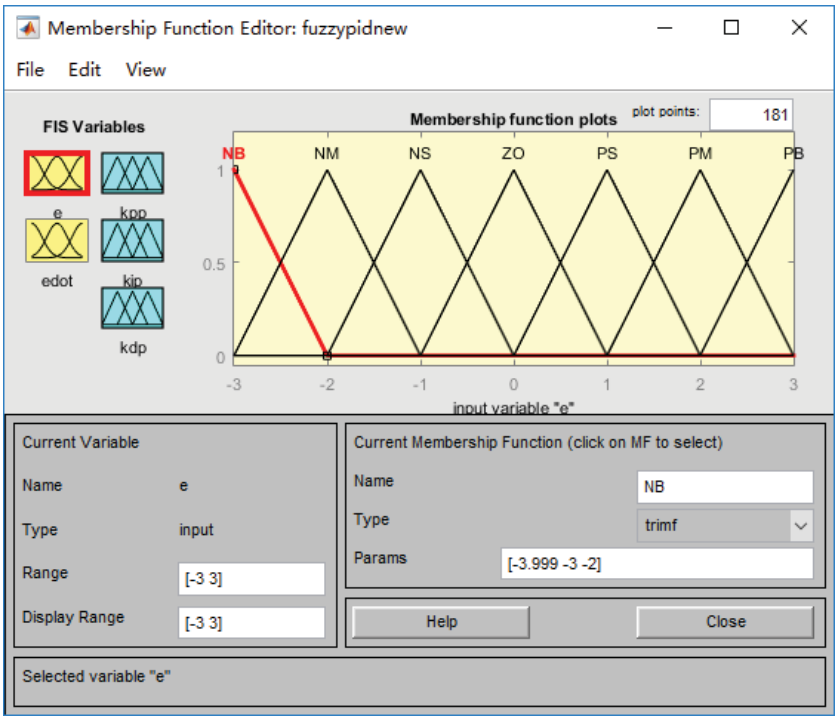

Fig. 4. 28 Membership function plots for $e(k)$

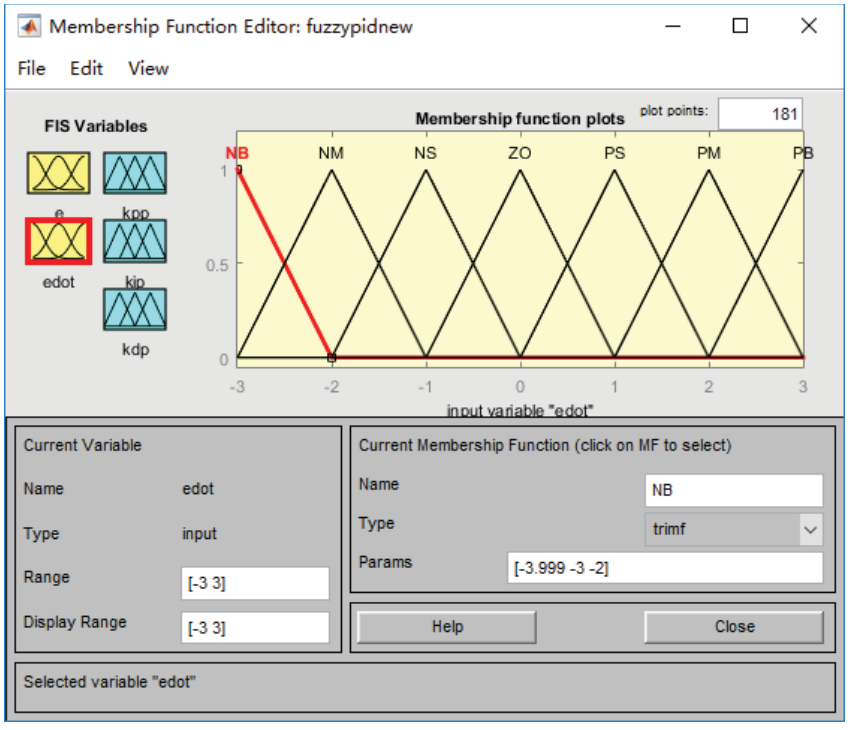

Fig. 4. 29 Membership function plots for $\Delta e(k)$

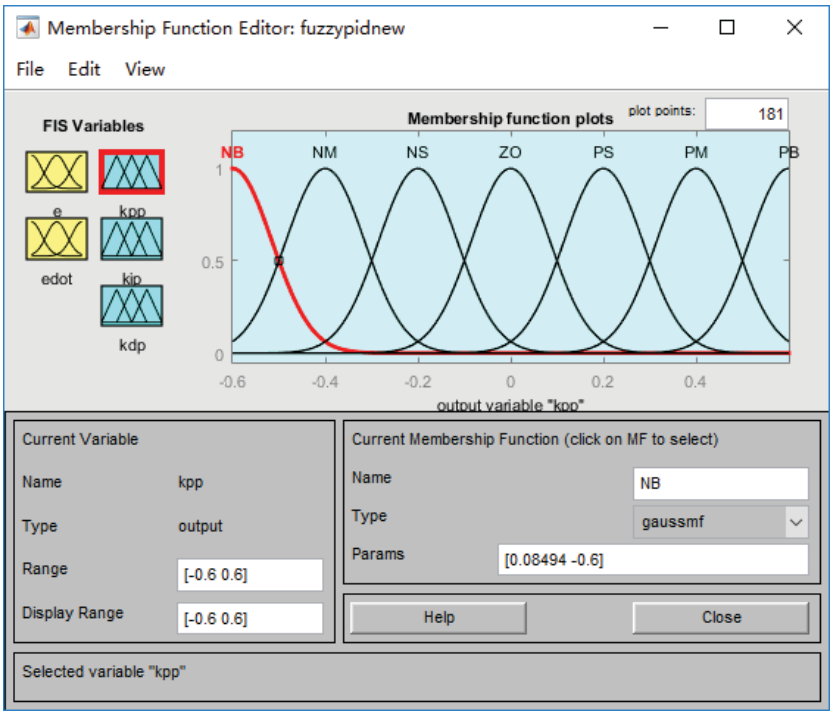

Fig. 4. 30 Membership function plots for K_{pp}

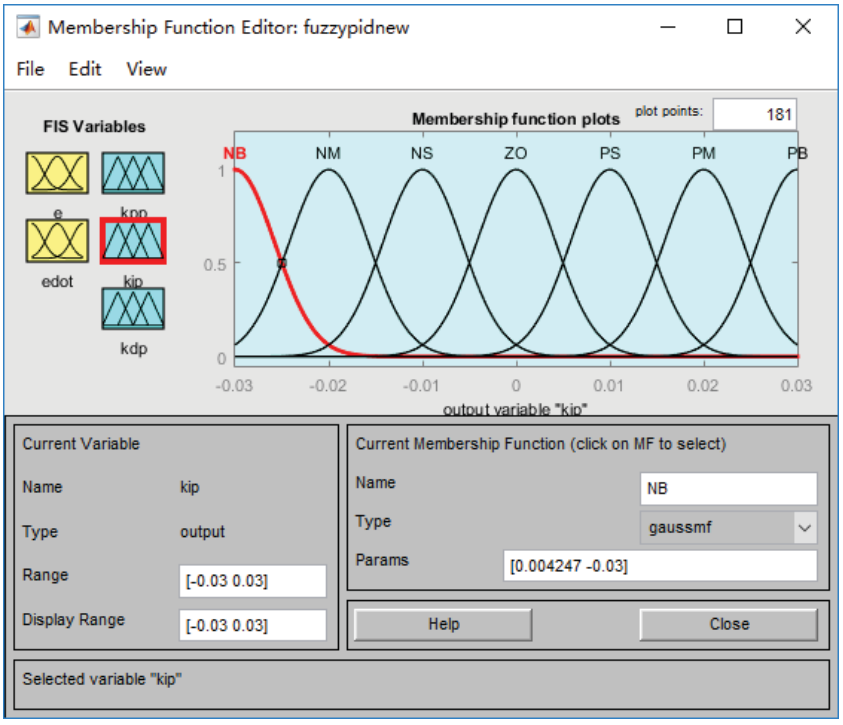

Fig. 4. 31 Membership function plots for K_{ip}

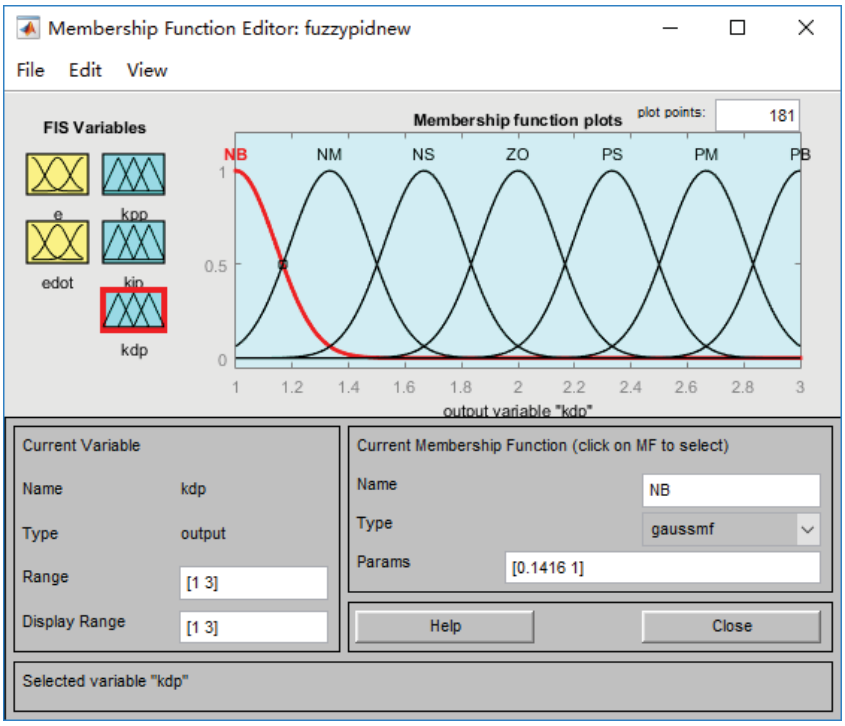

Fig. 4. 32 Membership function plots for K_{dp}

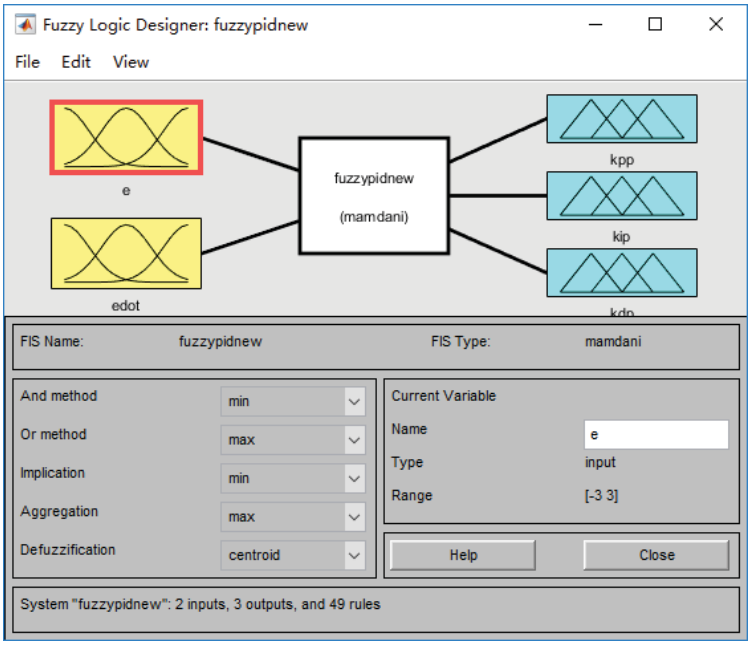

Fig. 4. 33 Membership function editor for the dual input mode corresponding relationship and parameters

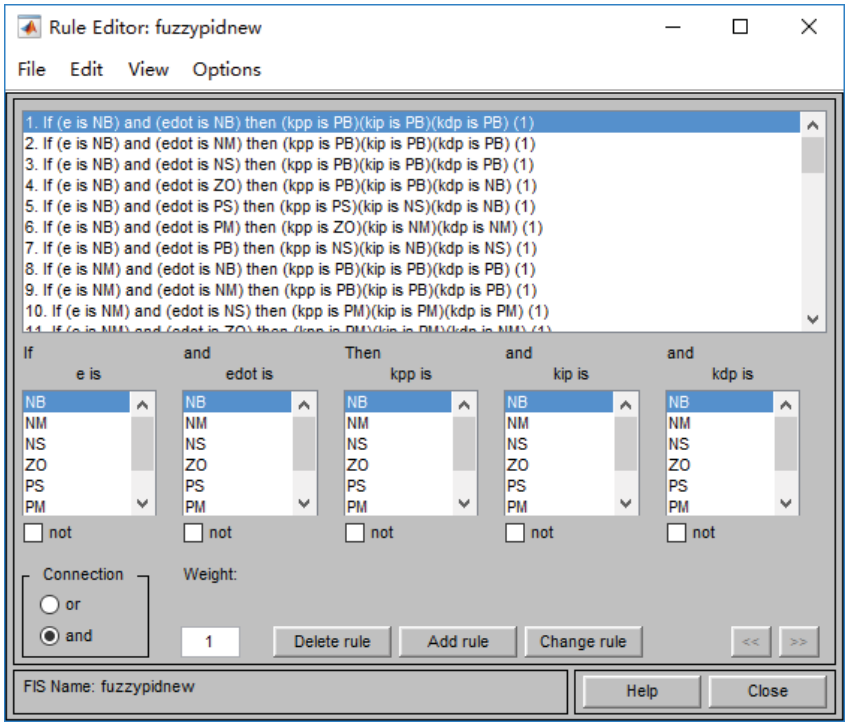

Fig. 4. 34 Basic rules of fuzzy PID controller for dual input converter

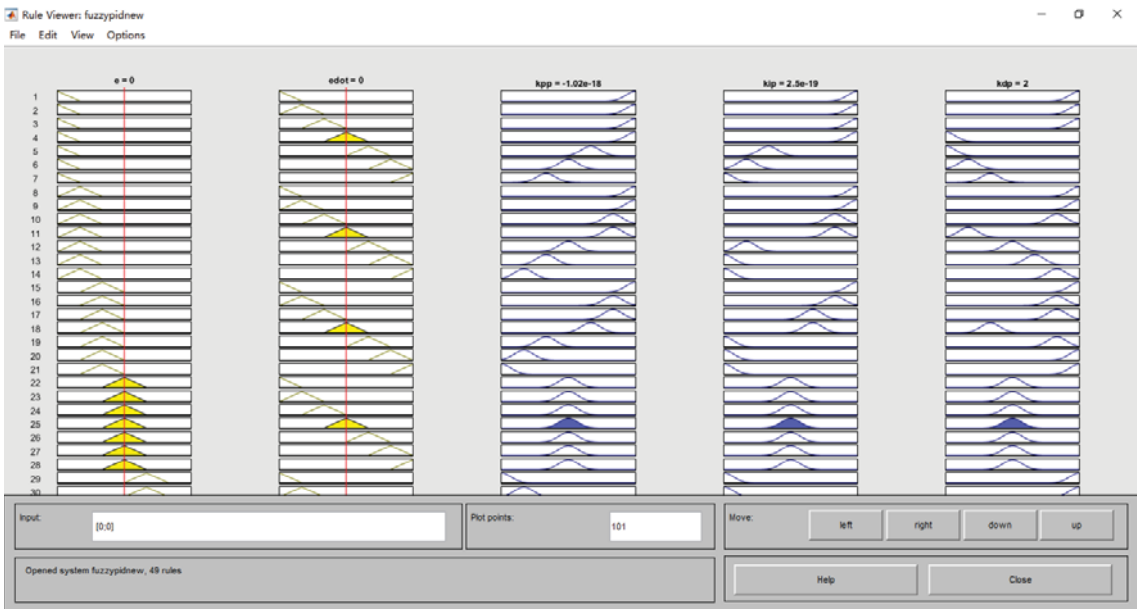

Fig. 4. 35 Fuzzy rules viewer in MATLAB for dual input mode

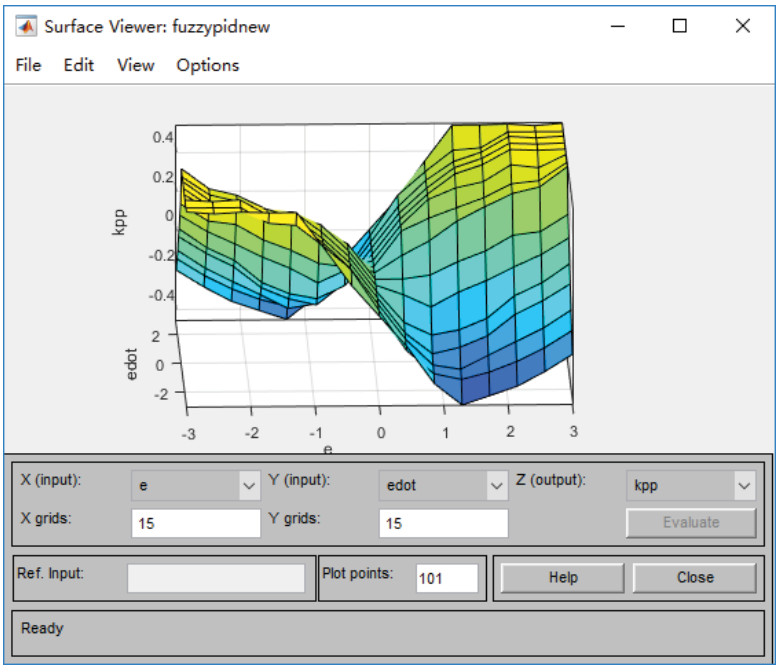

Fig. 4. 36 Fuzzy rules 3D surface for dual input mode of fuzzy PID controller

The core of designed fuzzy controller is the knowledge of technology and engineering, personal summarized and practical operation experience. Establishing the proper fuzzy rules as following tables of three factors K_p , K_i ,and K_d .

TABLE VI THE FUZZY RULES FOR PROPORTIONAL GAIN

		$\Delta e(k)$						
$e(k)$	K_p	NB	NM	NS	ZO	PS	PM	PB
	NB	PB	PB	PB	PB	PS	ZO	NS
	NM	PB	PB	PM	PM	ZO	NS	NM
	NS	PB	PM	PM	PS	NS	NM	NB
	ZO	ZO	ZO	ZO	ZO	ZO	ZO	ZO
	PS	NB	NM	NS	PS	PM	PM	PB
	PM	NM	NS	ZO	PM	PB	PB	PB
	PB	NS	ZO	PS	PB	PB	PB	PB

TABLE VII THE FUZZY RULES FOR INTEGRAL GAIN

	$\Delta e(k)$							
	K_i	NB	NM	NS	ZO	PS	PM	PB
$e(k)$	NB	PB	PB	PB	PB	NS	NM	NB
	NM	PB	PB	PM	PM	NM	NB	NB
	NS	PB	PM	PS	PS	NB	NB	NB
	ZO	ZO	ZO	ZO	ZO	ZO	ZO	ZO
	PS	NB	NB	NB	PS	PS	PM	PB
	PM	NB	NB	NM	PM	PB	PB	PB
	PB	NB	NM	NS	PB	PB	PB	PB

TABLE VIII THE FUZZY RULES FOR DERIVATIVE GAIN

	$\Delta e(k)$							
	K_d	NB	NM	NS	ZO	PS	PM	PB
$e(k)$	NB	PB	PB	PB	NB	NB	NM	NS
	NM	PB	PB	PM	NM	ZO	PS	PM
	NS	PB	PM	PM	NS	PM	PB	PB
	ZO	ZO	ZO	ZO	ZO	ZO	ZO	ZO
	PS	PB	PB	PM	NS	PM	PM	PB
	PM	PM	PS	ZO	NM	PM	PB	PB
	PB	NS	NM	NB	NB	PB	PB	PB

5. Import data and parameters into MATLAB workspace and read the determined fuzzy

inference system documents. Setting the fuzzification type is Mamdani, and the defuzzification type is centroid. The two input variations are $e(k)$ and $\Delta e(k)$, and the three output variations are K_{pp}, K_{ip}, and K_{dp}.

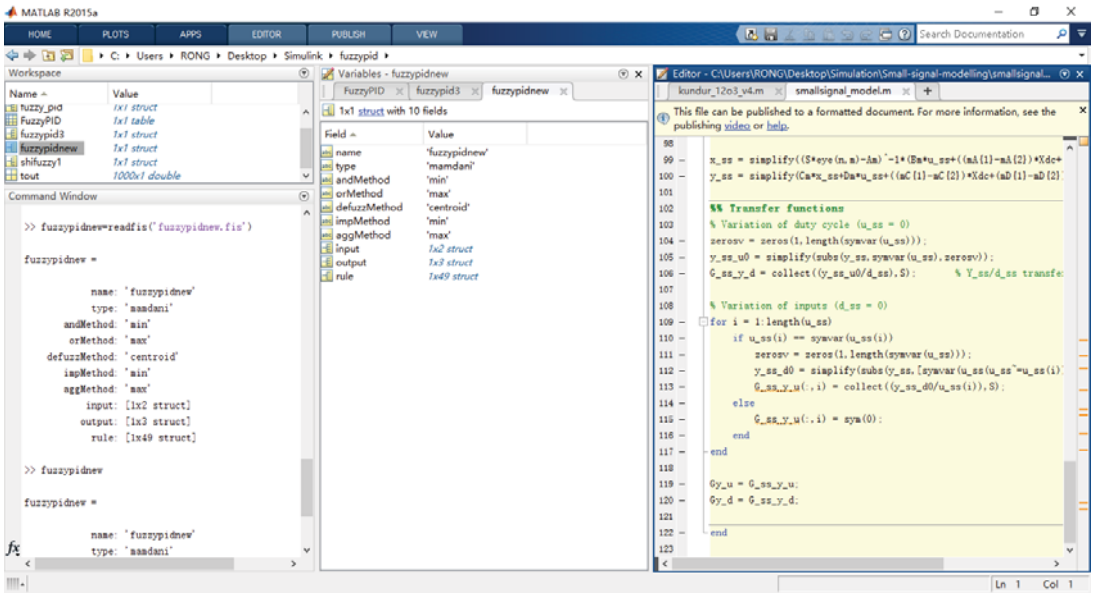

Fig. 4. 37 MATLAB Workspace of fuzzy inference system for dual input mode

4.2.1 Operation Models Simulation

The operation model simulation and comparison between fuzzy PID and conventional PID controller is shown as following figures 4.38, 4.39 and 4.40 with SIMULINK. The pink waveform is the output voltage controlled by conventional PID, v_{PIDout}, and the yellow waveform is the output voltage controlled by fuzzy PID controller, $v_{FuzzyPIDout}$.

- Single input single output mode

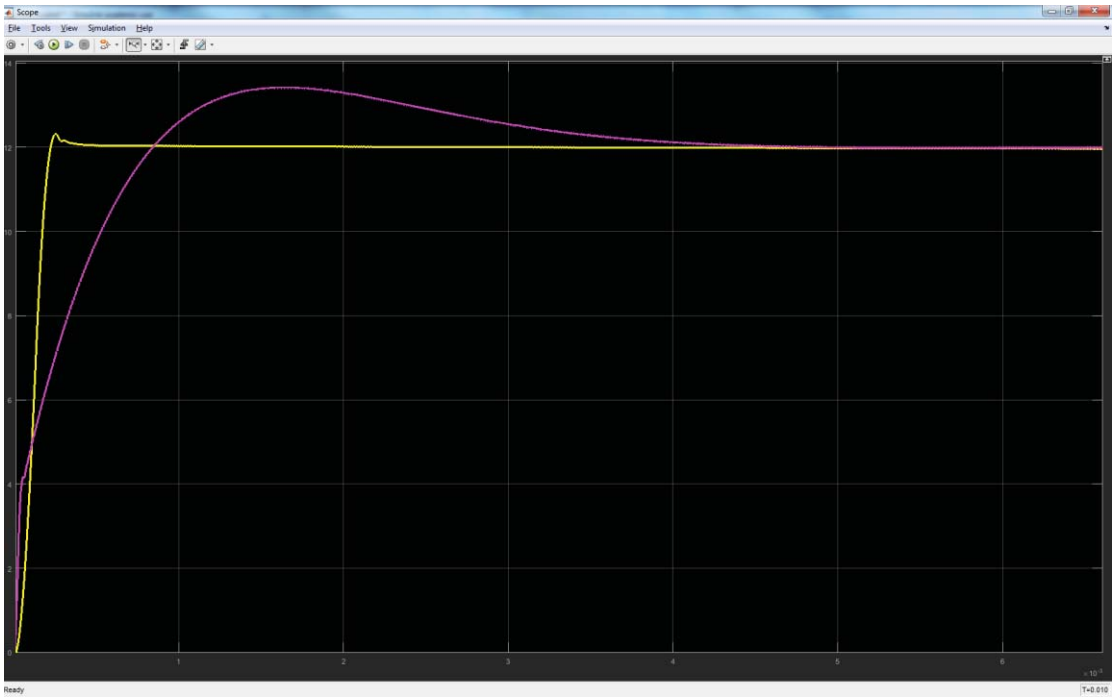

Fig. 4. 38 Two output voltages v_{PIDout} (pink) and $v_{FuzzyPIDout}$ (yellow) ($2\,V/div$, time scale: 1 ms/div) in single-input single-output mode

- Dual input single output mode

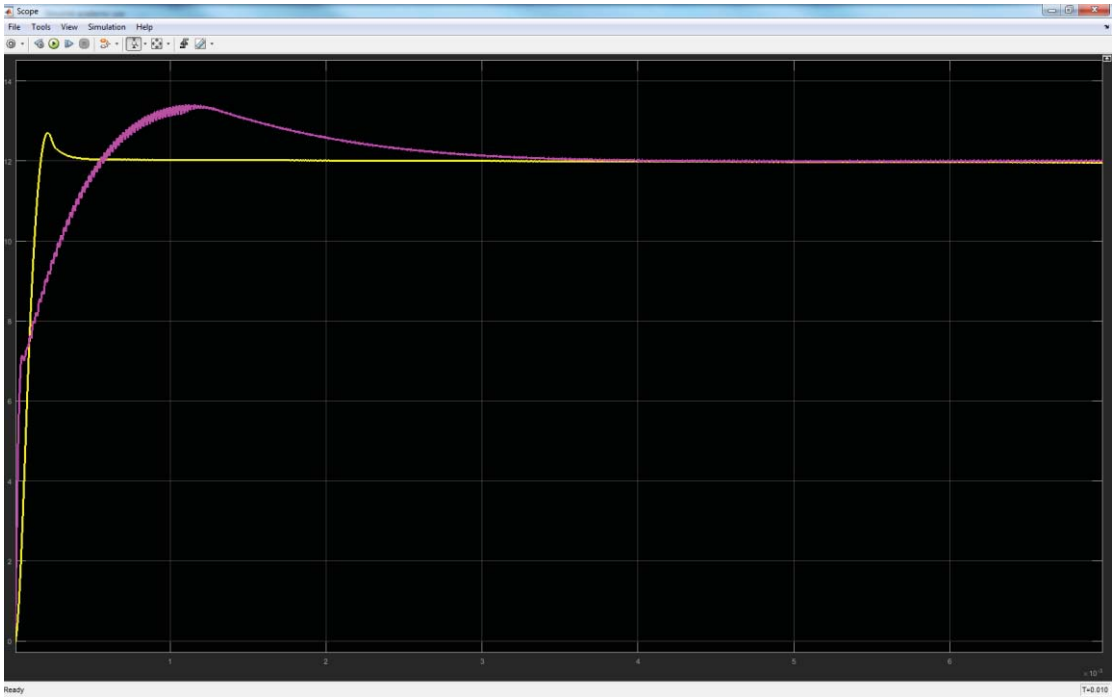

Fig. 4. 39 Two output voltages v_{PIDout} (pink) and $v_{FuzzyPIDout}$ (yellow)($2\,V/div$, time scale: 1 ms/div) in dual-input single-output mode

- Dual input with battery mode

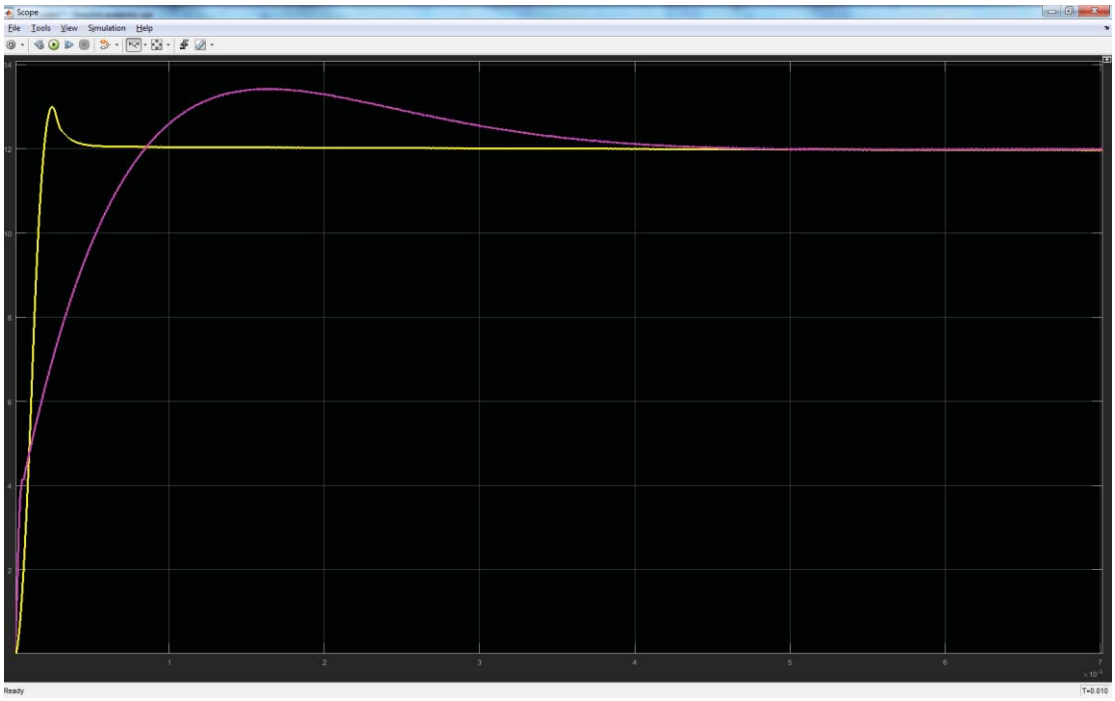

Fig. 4. 40 Two output voltages v_{PIDout} (pink) and $v_{FuzzyPIDout}$ (yellow) (2 V / div , time scale: 1 ms / div) in dual-input with battery mode

4.2.2 Comparison and Analysis

The setting range of calculating error $e(k)$ is [-3, 3], the error changing rate of the system $\Delta e(k)$ is [-3, 3] in Fig. 4.41, and the self-tuning output membership function Cu is [-6, 6]. The change of K_p is K_{pp}, and its range is [-0.6, 0.6]. The change of K_i is K_{ip}, and its range is [-0.03, 0.03]. K_{dp} is the change of K_d and its range is [1, 3].

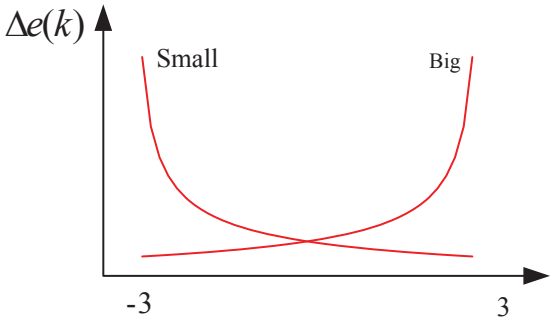

Fig. 4. 41 The range of $\Delta e(k)$

Amplify the output voltage waveform when it tends to stable. It is obvious that the yellow waveform, which is controlled by fuzzy PID is more quickly approach to the setting value, more stable, and its accuracy is better than the output controlled by conventional PID controller, which are shown in Fig. 4.42 and 4.43.

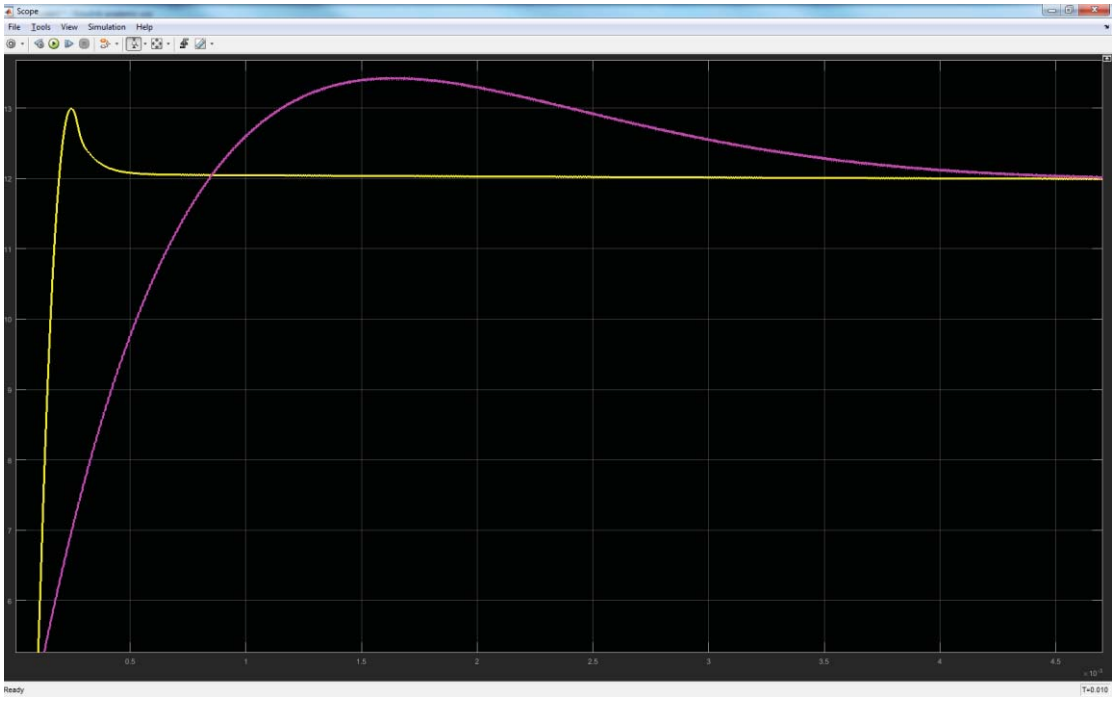

Fig. 4. 42 Two output voltages v_{PIDout} (pink) and $v_{FuzzyPIDout}$ (yellow) ($1\,V/div$, time scale: $0.5\,ms/div$) tend to stable

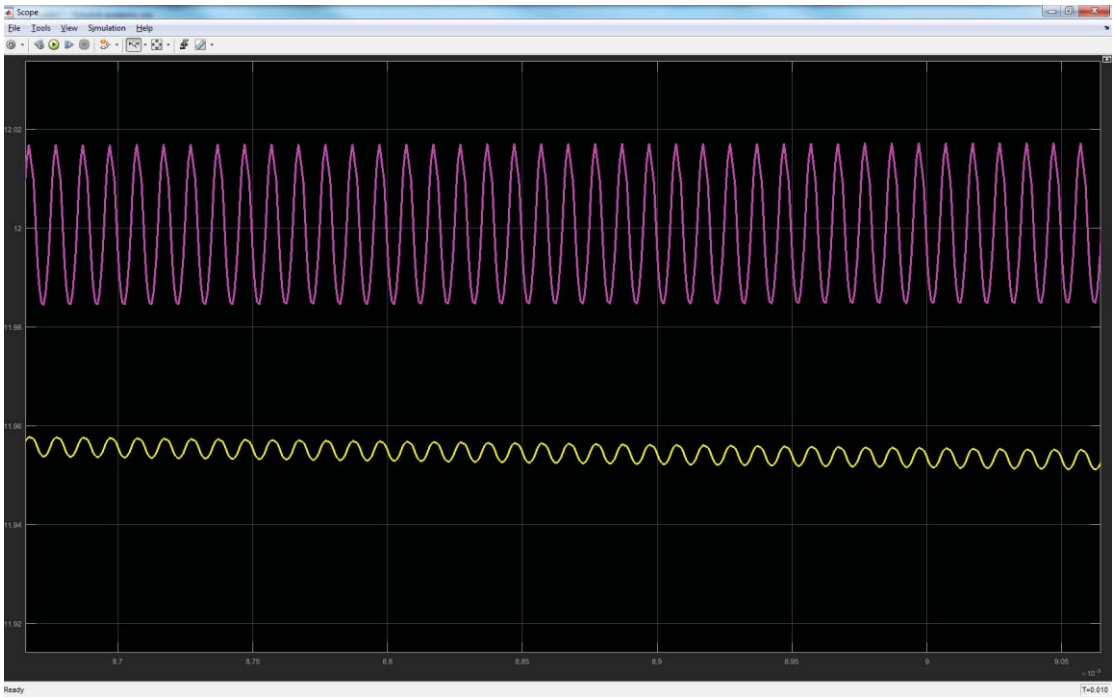

Fig. 4. 43 Two stable output voltages v_{PIDout} (pink) and $v_{FuzzyPIDout}$ (yellow) ($0.02\,V/div$, time scale: $0.05\,ms/div$)

Chapter 5 Implementation

5.1 Introduction of STM32f407

The inner core is based on high-performance 32-bit ARM Cortex M4 CPU with FPU adaptive real-time accelerator, which is shown in Fig. 5.1. It incorporates high-speed embedded memories. The extensive range of enhanced I/O and peripherals connected to two APB buses, three AHB buses and a 32-bit multi-AHB bus matrix. All devices offer three 12-bit ADCs, two general-purpose 32-bit timers, and advanced communication interface. Its frequency is up to 168MHz. The advantages of STM32f4 applied for the dual-input dual-output dc/dc converter are:

1. Advanced peripherals:

2. Up to 1 M byte of Flash memory

3. Low power operation

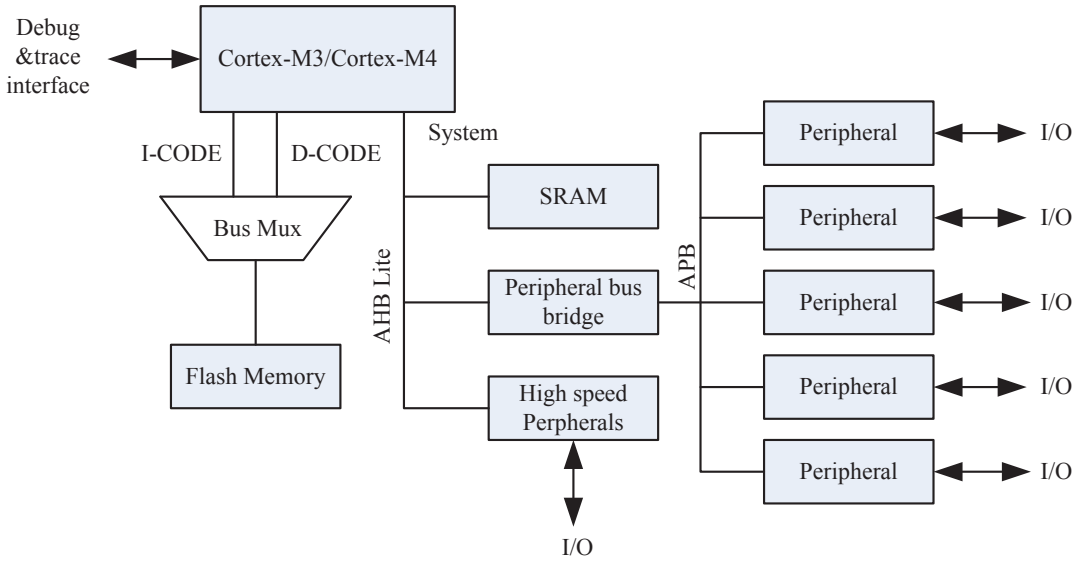

Fig. 5. 1 Diagram of 32-bit ARM Cortex M4 CPU

There are eight masters, Cortex®-M4 with FPU core I-bus, D-bus and S-bus, DMA1 memory bus, DMA2 memory bus, DMA2 peripheral bus, Ethernet DMA bus, USB OTG HS DMA bus.

And seven slaves, Internal Flash memory I Code bus, Internal Flash memory D Code bus, Main internal SRAM1 (112 KB), Auxiliary internal SRAM2 (16 KB), AHB1 peripherals including AHB to APB bridges and APB peripherals, AHB2 peripherals, FSMC.

Several main functions are introduced in details,

1. General-purpose I/Os (GPIO)

Each general-purpose I/O port has four 32-bit configuration registers (GPIOx_MODER, GPIOx_OTYPER, GPIOx_OSPEEDR and GPIOx_PUPDR), two 32-bit data registers (GPIOx_IDR and GPIOx_ODR), a 32-bit set/reset register (GPIOx_BSRR), a 32-bit locking register (GPIOx_LCKR) and two 32-bit alternate function selection register (GPIOx_AFRH and GPIOx_AFRL).

The main features of GPIO, which is shown in Fig. 5.2.

- Up to 16 I/Os under control
- Output states: push-pull or open drain + pull-up/down
- Output data from output data register (GPIOx_ODR) or peripheral (alternate function output)
- Speed selection for each I/O
- Input states: floating, pull-up/down, analog
- Input data to input data register (GPIOx_IDR) or peripheral (alternate function input)
- Bit set and reset register (GPIOx_BSRR) for bitwise write access to GPIOx_ODR
- Locking mechanism (GPIOx_LCKR) provided to freeze the I/O configuration
- Analog function
- Alternate function input/output selection registers (at most 16 AFs per I/O)
- Fast toggle capable of changing every two clock cycles
- Highly flexible pin multiplexing allows the use of I/O pins as GPIOs or as one of several

peripheral functions

Subject to the specific hardware characteristics of each I/O port listed in the datasheet, each port bit of the general-purpose I/O (GPIO) ports can be individually configured by software in several modes:

- Input floating
- Input pull-up
- Input-pull-down
- Analog
- Output open-drain with pull-up or pull-down capability
- Output push-pull with pull-up or pull-down capability
- Alternate function push-pull with pull-up or pull-down capability
- Alternate function open-drain with pull-up or pull-down capability General-purpose I/Os (GPIO) RM0090

Each I/O port bit is freely programmable, however, the I/O port registers have to be accessed as 32-bit words, half-words or bytes. The purpose of the GPIOx_BSRR register is to allow atomic read/modify accesses to any of the GPIO registers. In this way, there is no risk of an IRQ occurring between the read and the modify access.

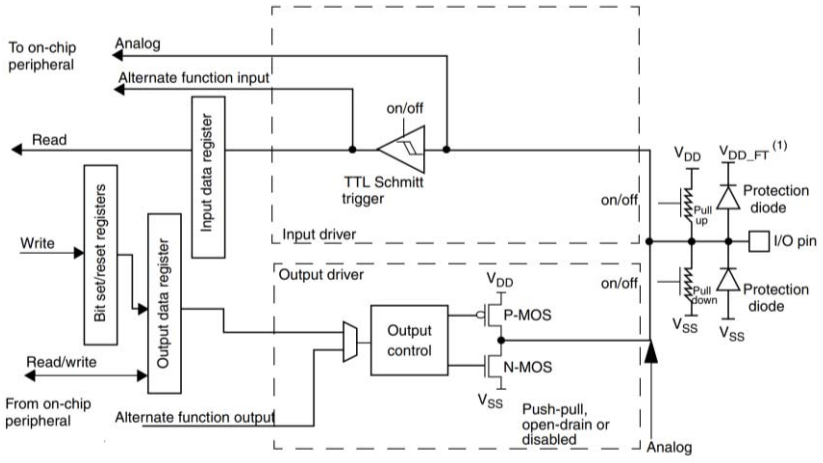

Fig. 5. 2 Basic structure of a five-volt tolerant I/O port bit

2. Clock

Three different clock sources can be used to drive the system clock (SYSCLK), HSI oscillator clock, HSE oscillator clock, Main PLL (PLL) clock.

The devices have the two following secondary clock sources:

• 32 kHz low-speed internal RC (LSI RC) which drives the independent watchdog and, optionally, the RTC used for Auto-wakeup from the Stop/Standby mode.

• 32.768 kHz low-speed external crystal (LSE crystal) which optionally drives the RTC clock (RTCCLK)

Each clock source can be switched on or off independently when it is not used, to optimize power consumption. The clock tree is shown in Fig. 5.3.

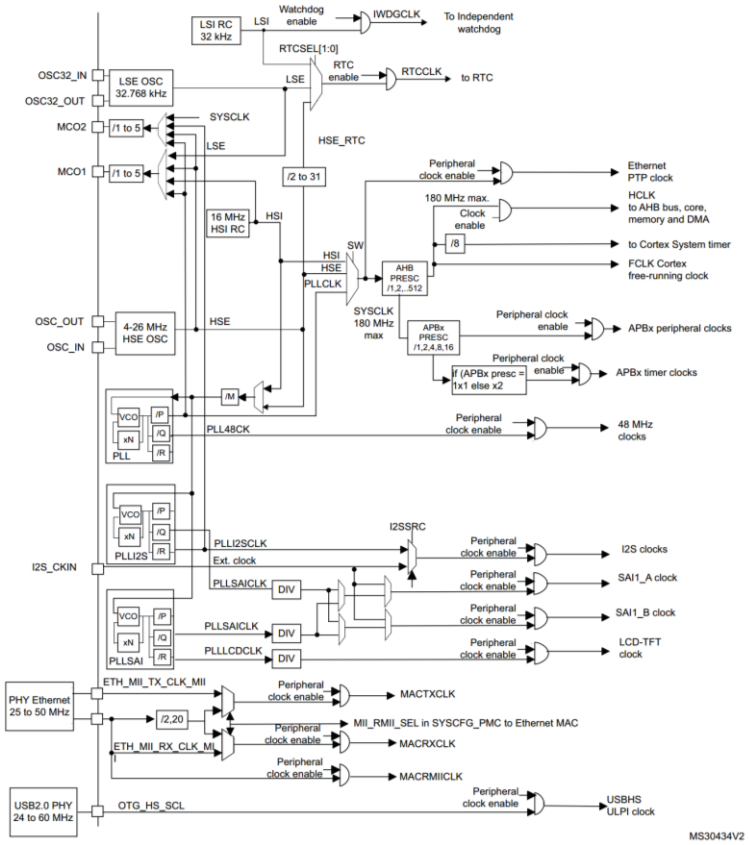

Fig. 5. 3 Structure of clock tree

3. Direct memory access (DMA)

Direct memory access (DMA) is used in order to provide high-speed data transfer between

peripherals and memory and between memory and memory. Data can be quickly moved by DMA without any CPU action. This keeps CPU resources free for other operations. The DMA controller combines a powerful dual AHB master bus architecture with independent FIFO to optimize the bandwidth of the system, based on complex bus matrix architecture and its structure is shown in Fig. 5.4.

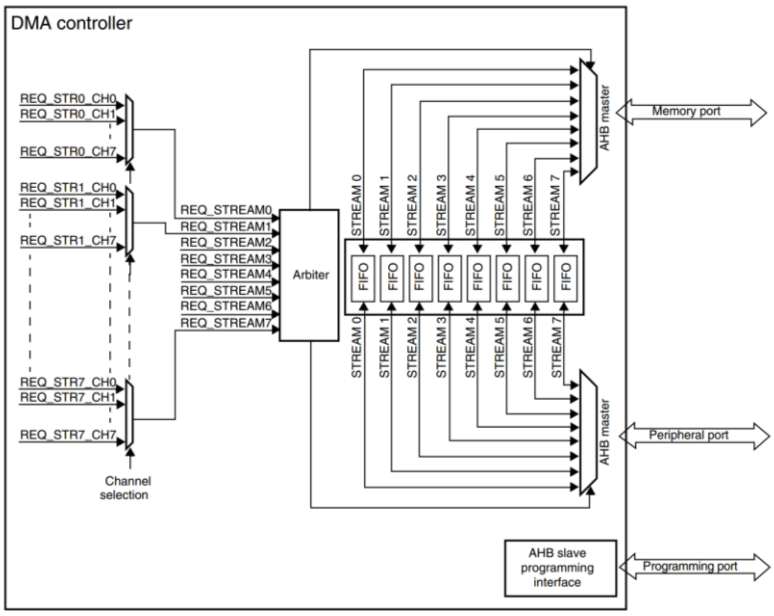

Fig. 5. 4 Structure of DMA controller

The two DMA controllers have 16 streams in total (8 for each controller), each dedicated to managing memory access requests from one or more peripherals. Each stream can have up to 8 channels (requests) in total. And each has an arbiter for handling the priority between DMA requests.

The main DMA features are:

• Dual AHB master bus architecture, one dedicated to memory accesses and one dedicated to peripheral accesses

• AHB slave programming interface supporting only 32-bit accesses

• 8 streams for each DMA controller, up to 8 channels (requests) per stream

• Four-word depth 32 first-in, first-out memory buffers (FIFOs) per stream, that can be used in FIFO mode or direct mode:

– FIFO mode: with threshold level software selectable between 1/4, 1/2 or 3/4 of the FIFO size

– Direct mode

Each DMA request immediately initiates a transfer from/to the memory. When it is configured in direct mode (FIFO disabled), to transfer data in memory-to peripheral mode, the DMA preloads only one data from the memory to the internal FIFO to ensure an immediate data transfer as soon as a DMA request is triggered by a peripheral.

• Each stream can be configured by hardware to be:

– a regular channel that supports peripheral-to-memory, memory-to-peripheral and memory-to-memory transfers

– a double buffer channel that also supports double buffering on the memory side

• Each of the 8 streams are connected to dedicated hardware DMA channels (requests)

• Priorities between DMA stream requests are software-programmable (4 levels consisting of very high, high, medium, low) or hardware in case of equality (request 0 has priority over request 1, etc.)

• Each stream also supports software trigger for memory-to-memory transfers (only available for the DMA2 controller)

• Each stream request can be selected among up to 8 possible channel requests. This selection is software-configurable and allows several peripherals to initiate DMA requests

• The number of data items to be transferred can be managed either by the DMA controller or by the peripheral:

– DMA flow controller: the number of data items to be transferred is software programmable from 1 to 65535

– Peripheral flow controller: the number of data items to be transferred is unknown and controlled by the source or the destination peripheral that signals the end of the transfer by hardware

• Independent source and destination transfer width (byte, half-word, word): when the data widths of the source and destination are not equal, the DMA automatically packs/unpacks the necessary transfers to optimize the bandwidth. This feature is only available in FIFO mode

• Incrementing or non-incrementing addressing for source and destination

• Supports incremental burst transfers of 4, 8 or 16 beats. The size of the burst is software-configurable, usually equal to half the FIFO size of the peripheral

• Each stream supports circular buffer management

• 5 event flags (DMA Half Transfer, DMA Transfer complete, DMA Transfer Error, DMA FIFO Error, Direct Mode Error) logically ORed together in a single interrupt request for each stream

The DMA controller performs direct memory transfer: as an AHB master, it can take the control of the AHB bus matrix to initiate AHB transactions. It can carry out the following transactions:

• peripheral-to-memory

• memory-to-peripheral

• memory-to-memory

The DMA controller provides two AHB master ports: the AHB memory port, intended to be connected to memories and the AHB peripheral port, intended to be connected to peripherals. However, to allow memory-to-memory transfers, the AHB peripheral port must also have access to the memories. The AHB slave port is used to program the DMA controller (it supports only 32-bit accesses)

4. Analog to digital conversion

The 12-bit ADC is a successive approximation analog-to-digital converter, and its diagram is shown in Fig. 5.5. It has up to 19 multiplexed channels allowing it to measure signals from 16 external sources, two internal sources, and the VBAT channel. The A/D conversion of the channels can be performed in single, continuous, scan or discontinuous mode. The result of the ADC is stored into a left or right-aligned 16-bit data register.

The analog watchdog feature allows the application to detect if the input voltage goes beyond the user-defined, higher or lower thresholds.

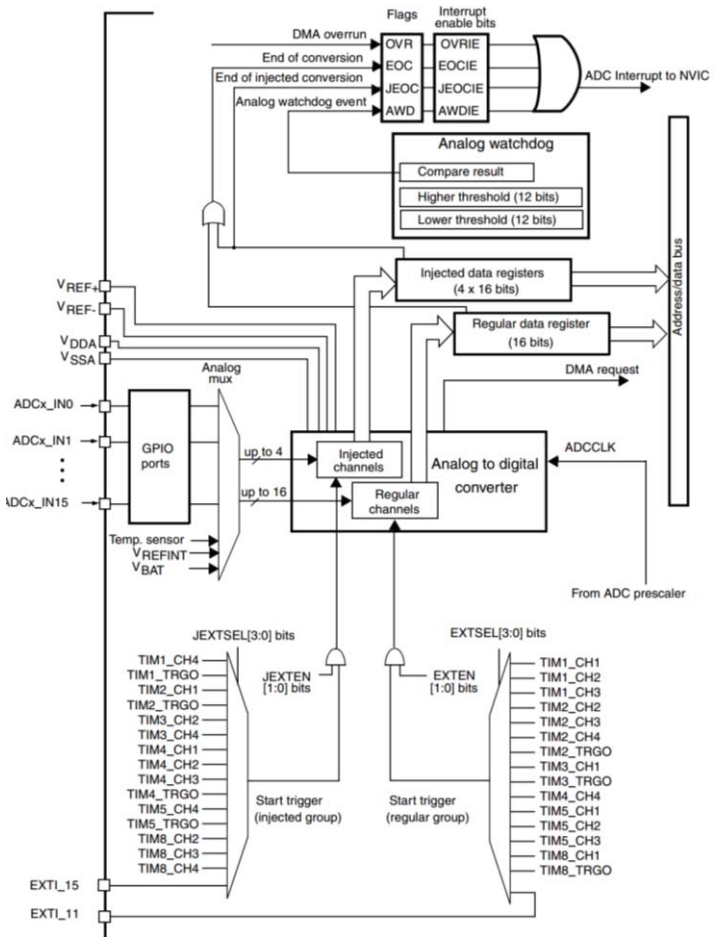

Fig. 5. 5 Single ADC block diagram

ADC main features are,

- 12-bit, 10-bit, 8-bit or 6-bit configurable resolution
- Interrupt generation at the end of conversion, end of injected conversion, and in case of analog watchdog or overrun events
- Single and continuous conversion modes
- Scan mode for automatic conversion of channel 0 to channel ‘n’
- Data alignment with in-built data coherency
- Channel-wise programmable sampling time

- External trigger option with configurable polarity for both regular and injected conversions
- Discontinuous mode
- Dual/Triple mode (on devices with 2 ADCs or more)
- Configurable DMA data storage in Dual/Triple ADC mode
- Configurable delay between conversions in Dual/Triple interleaved mode
- ADC conversion type (refer to the datasheets)
- ADC supply requirements: 2.4 V to 3.6 V at full speed and down to 1.8 V at slower speed
- ADC input range: VREF– ≤ VIN ≤ VREF+
- DMA request generation during regular channel conversion

The ADC features two clock schemes:

- Clock for the analog circuitry: ADCCLK, common to all ADCs

This clock is generated from the APB2 clock divided by a programmable prescaler that allows the ADC to work at fPCLK2/2, /4, /6 or /8. Refer to the datasheets for the maximum value of ADCCLK.

- Clock for the digital interface (used for registers read/write access)

This clock is equal to the APB2 clock. The digital interface clock can be enabled/disabled individually for each ADC through the RCC APB2 peripheral clock enable register (RCC_APB2ENR)

5. Universal synchronous asynchronous receiver transmitter (USART)

The universal synchronous asynchronous receiver transmitter (USART) offers a flexible means of full-duplex data exchange with external equipment requiring an industry standard NRZ asynchronous serial data format. The USART offers a very wide range of baud rates using a fractional baud rate generator. It supports synchronous one-way communication and half-duplex single wire communication. It also supports the LIN (local interconnection network), Smartcard Protocol and IrDA (infrared data association) SIR ENDEC specifications, and

modem operations (CTS/RTS). It allows multiprocessor communication. High speed data communication is possible by using the DMA for multi-buffer configuration. The block diagram is shown in Fig. 5.6

The interface is externally connected to another device by three pins (see Figure 296). Any USART bidirectional communication requires a minimum of two pins: Receive Data In (RX) and Transmit Data Out (TX):

RX: Receive Data Input is the serial data input. Oversampling techniques are used for data recovery by discriminating between valid incoming data and noise.

TX: Transmit Data Output. When the transmitter is disabled, the output pin returns to its I/O port configuration. When the transmitter is enabled and nothing is to be transmitted, the TX pin is at high level. In single-wire and smartcard modes, this I/O is used to transmit and receive the data (at USART level, data are then received on SW_RX).

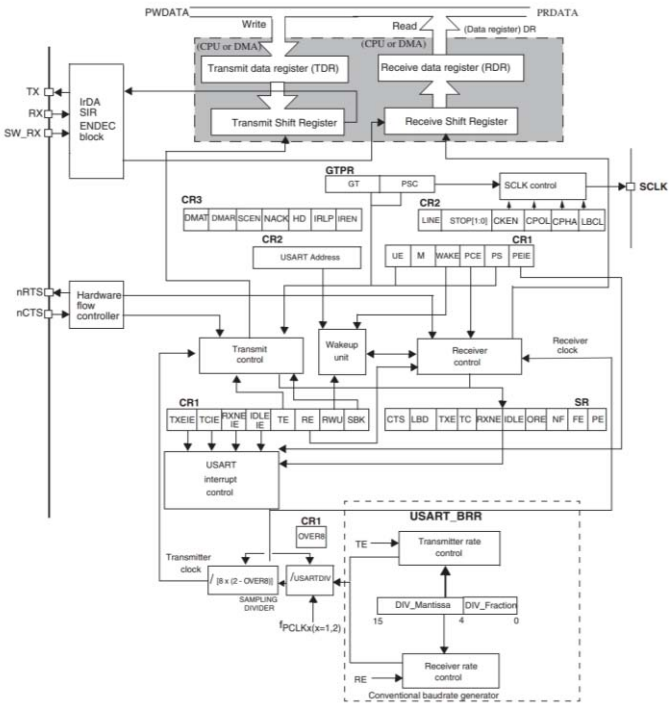

Fig. 5. 6 USART block diagram

6. General-purpose timer

The general-purpose timers consist of a 16-bit or 32-bit auto-reload counter driven by a

programmable pre-scaler. They may be used for a variety of purposes, including measuring the pulse lengths of input signals (input capture) or generating output waveforms (output compare and PWM). Pulse lengths and waveform periods can be modulated from a few microseconds to several milliseconds using the timer pre-scaler and the RCC clock controller pre-scalers. The timers are completely independent, and do not share any resources. They can be synchronized together as shown in Fig. 5.7.

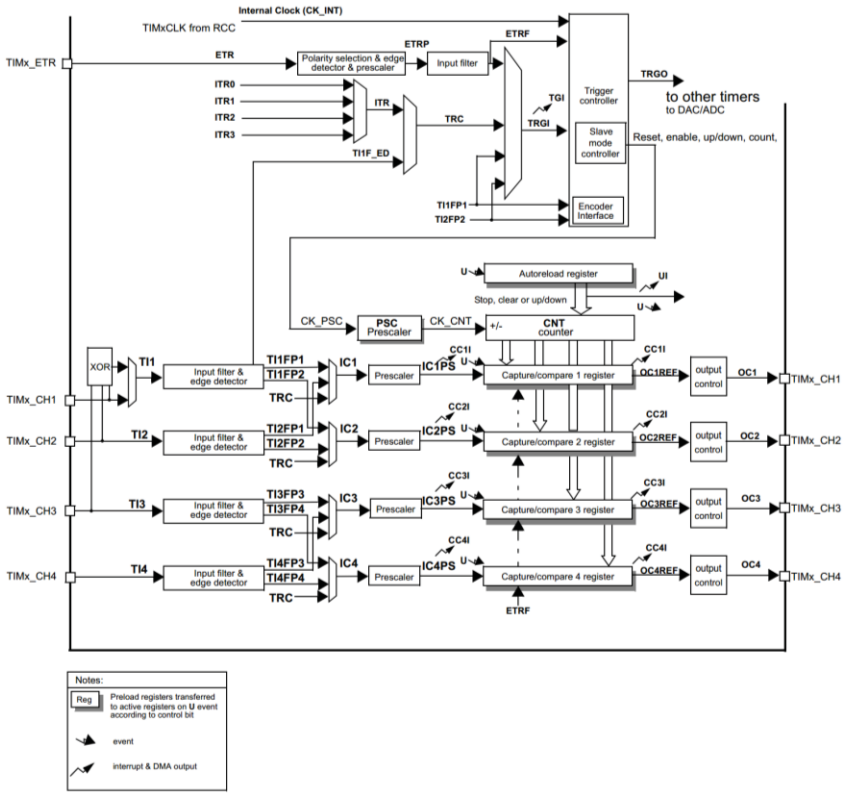

Fig. 5. 7 General purpose timer block diagram

General-purpose TIMx timer features include:

- 16-bit (TIM3 and TIM4) or 32-bit (TIM2 and TIM5) up, down, up/down auto-reload counter.
- 16-bit programmable pre-scaler used to divide (also “on the fly”) the counter clock frequency by any factor between 1 and 65536.
- Up to 4 independent channels for, Input capture, output compare, PWM generation (Edge- and Center-aligned modes), one-pulse mode output.
- Synchronization circuit to control the timer with external signals and to interconnect several

timers.

- Interrupt/DMA generation on the following events:

- Update: counter overflow/underflow, counter initialization (by software or internal/external trigger)

- Trigger event (counter start, stop, initialization or count by internal/external trigger)

- Input capture

- Output compare

- Supports incremental (quadrature) encoder and hall-sensor circuitry for positioning purposes.

- Trigger input for external clock or cycle-by-cycle current management.

5.2 Experimental Steps

Programming STM32f407 as the controller with C language is used to verify the fuzzy PID control method. The experimental steps are as follows,

1. Initialized the equipment (oscilloscope, multi-meter, signal generator, laptop, power sources, STM32f407, hardware circuit). The signal generator generates a special square waveform to drive MOSFET and achieve a constant output voltage to verify the hardware works well.

2. Line the hardware with micro controller. For STM32, it generates two PWM outputs as gates drive waveforms and one input to generate the error signal. Sampling the output voltage and using ADC function to convert the voltage signals to digital signals. The sampling frequency is 10 kHz. For oscillator, there are two channels to test the output voltage and PWM waveform separately. The multi-meter is used to measure input voltage and the large range of output voltage. Laptop is connected to STM32 to download finished program. The following figure 5.8 shows the connected hardware.

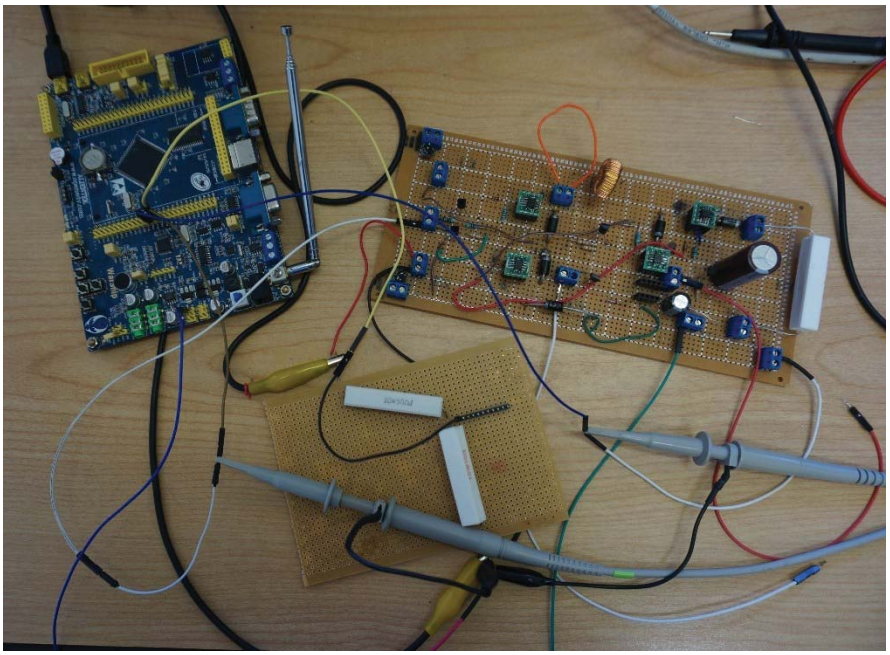

Fig. 5. 8 The connected hardware including converter and controller

3. Download the program from computer by the software named Fly MCU to STM32. There are several resources we need to use, GPIO, TIMER, ADC, USART, DMA, and PWM to be used for realizing the whole controller functions. The following figure is the internal operation process of micro controller unit (MCU) programmer.

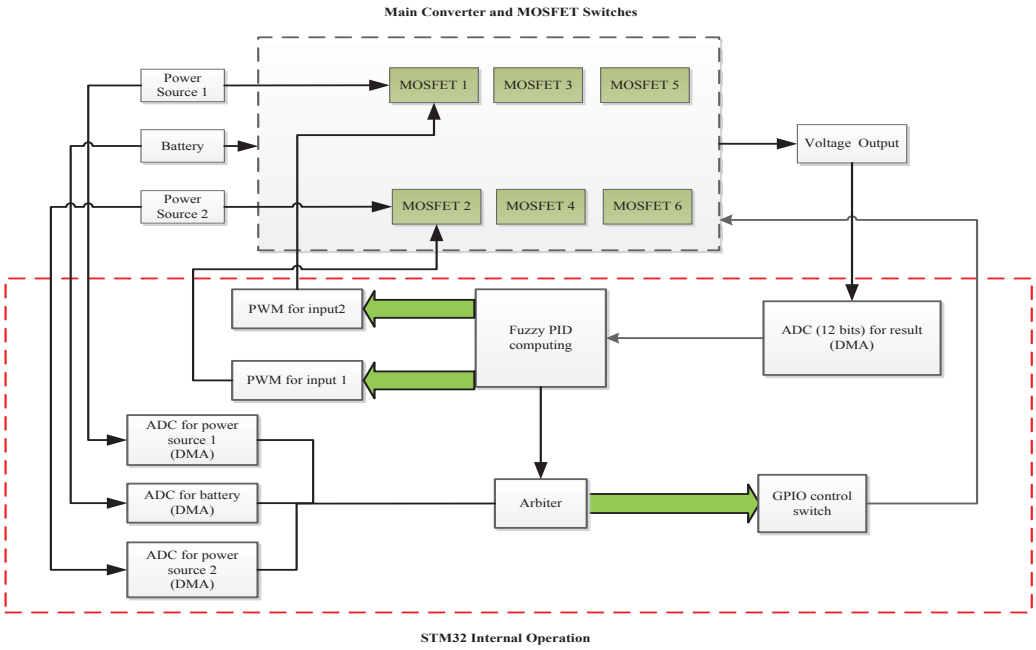

Fig. 5. 9 The STM32 internal operation diagram

4. Choose different reference voltage and input voltage to test the performance of improved controller. The reference voltage is changing from 1.0 V to 4.0 V. The input voltage is changing from 3.0 V to 8.5 V. Measured the output voltage and duty cycle with oscilloscope to verify the experimental results. Check the ADC values from USART interface.

5. Measured the output voltage with multi-meter and compared them with oscilloscope measured values. Because the maximum range of MCU is limited to 5.0 V, voltage divider is necessary for sampling feedback voltage. The branch voltage is half of the output voltage, so the oscilloscope measured voltage is multiplied by two equals to the output voltage.

5.3 Experimental Results

The experimental results are shown in following tables. The reference voltage is 1.0V, 2.0V, 2.3V, 2.5V, 2.7V, 3.0V, 3.5V, 4.0V. The input voltage range is from 3.0V to 8.5V. Duty cycle and oscilloscope voltage are displayed by oscilloscope. Output voltage is measured by multi-meter. The ADC values are displayed by computer interface. Keeping the reference voltage constant, changing the input voltage from 3.0V to 8.5V and recording the output voltage, ADC

value, duty cycle, and oscilloscope display. The output voltage should not change too much according to the variation of input voltage, which is closed to reference voltage.

TABLE IX THE EXPERIMENTAL RESULTS OF SETTING REFERENCE VOLTAGE IS 1.0V

Reference Voltage: 1.0 V				
Input Voltage (V)	Output Voltage (V)	ADC (USART)	Duty Cycle	Oscilloscope
3.0	0.884	0.495	61.00%	464.4 mV
3.5	0.879	0.482	27.99%	461.2 mV
4.0	0.878	0.489	15.00%	470.7 mV
4.5	0.894	0.496	9.00%	469.6 mV
5.0	0.895	0.492	7.00%	462.4 mV
5.5	0.842	0.459	5.95%	439.0 mV
6.0	0.840	0.464	3.99%	454.7 mV
6.5	0.926	0.511	3.99%	487.2 mV
7.0	0.848	0.469	3.00%	443.3 mV
7.5	0.950	0.527	3.00%	499.4 mV
8.0	0.847	0.468	2.00%	446.0mV

TABLE X THE EXPERIMENTAL RESULTS OF SETTING REFERENCE VOLTAGE IS 2.0V

Reference Voltage: 2.0 V				
Input Voltage (V)	Output Voltage (V)	ADC (USART)	Duty Cycle	Oscilloscope
4.5	1.78	0.98	48.000%	963.4mV
5.0	1.79	0.99	32.997%	960.0mV
5.5	1.76	0.98	16.001%	976.8mV
6.0	1.79	1.00	12.000%	968.4mV
6.5	1.77	0.98	10.001%	971.6mV
7.0	1.74	0.96	8.996%	1024mV
7.5	1.77	0.98	7.000%	955.7mV
8.0	1.74	1.07	4.000%	923.5mV

TABLE XI THE EXPERIMENTAL RESULTS OF SETTING REFERENCE VOLTAGE IS 2.3V

Reference Voltage: 2.3 V				
Input Voltage (V)	Output Voltage (V)	ADC (USART)	Duty Cycle	Oscilloscope
4.5	2.03	1.12	69.002%	1.0680V
5.0	2.00	1.12	32.997%	1.1140V
5.5	2.00	1.12	17.00%	1.15V
6.0	2.03	1.12	14.01%	1.0991V
6.5	2.07	1.14	10.99%	1.1117V
7.0	1.96	1.08	9.00%	1.0669V
7.5	1.99	1.100	8.00%	1.0870V
8.0	1.99	1.10	7.00%	1.0788V

TABLE XII THE EXPERIMENTAL RESULTS OF SETTING REFERENCE VOLTAGE IS 2.5V

Reference Voltage: 2.5 V				
Input Voltage (V)	Output Voltage (V)	ADC (USART)	Duty Cycle	Oscilloscope
4.5	2.49	1.37	88.99%	1.1836V
5.0	2.25	1.23	47.00%	1.2122V
5.5	2.29	1.23	23.99%	1.2120V
6.0	2.26	1.19	18.01%	1.2167V
6.5	2.31	1.24	14.00%	1.2019V
7.0	2.30	1.26	11.00%	1.1919V
7.5	2.31	1.24	10.00%	1.2202V
8.0	2.27	1.21	9.00%	1.2686V

TABLE XIII THE EXPERIMENTAL RESULTS OF SETTING REFERENCE VOLTAGE IS 2.7V

Reference Voltage: 2.7 V				
Input Voltage (V)	Output Voltage (V)	ADC (USART)	Duty Cycle	Oscilloscope
5.0	2.37	1.290	79.00%	1.2910V
5.5	2.38	1.320	30.00%	1.3052V
6.0	2.38	1.328	20.00%	1.3002V
6.5	2.37	1.316	16.01%	1.3336V
7.0	2.37	1.315	13.00%	1.3253V
7.5	2.31	1.360	11.00%	1.3335V
8.0	2.37	1.320	9.01%	1.3045V

TABLE XIV THE EXPERIMENTAL RESULTS OF SETTING REFERENCE VOLTAGE IS 3.0V

Reference Voltage: 3.0 V				
Input Voltage (V)	Output Voltage (V)	ADC (USART)	Duty Cycle	Oscilloscope
5.5	2.643	1.460	54.00%	1.4543V
6.0	2.650	1.474	29.00%	1.4602V
6.5	2.662	1.479	20.00%	1.4601V
7.0	2.682	1.486	15.00%	1.4646V
7.5	2.649	1.494	12.99%	1.4749V
8.0	2.678	1.482	11.00%	1.4610V

TABLE XV THE EXPERIMENTAL RESULTS OF SETTING REFERENCE VOLTAGE IS 3.5V

Reference Voltage: 3.5 V				
Input Voltage (V)	Output Voltage (V)	ADC (USART)	Duty Cycle	Oscilloscope
6.0	3.10	1.716	46.00%	1.6932V
6.5	3.12	1.72	27.00%	1.7105V
7.0	3.14	1.72	21.00%	1.7286V
7.5	3.12	1.72	15.99%	1.6889V
8.0	3.13	1.73	15.00%	1.7019V
8.5	3.15	1.74	14.00%	1.7124V

TABLE XVI THE EXPERIMENTAL RESULTS OF SETTING REFERENCE VOLTAGE IS 4.0V

Reference Voltage: 4.0 V				
Input Voltage (V)	Output Voltage (V)	ADC (USART)	Duty Cycle	Oscilloscope
6.5	3.55	1.96	51.00%	1.9451V
7.0	3.56	1.97	30.00%	1.9511V
7.5	3.57	1.97	22.00%	1.9471V
8.0	3.58	1.98	18.00%	1.9588V
8.5	3.55	1.95	15.00%	1.9253V

The following figures are the experimental results measured by oscilloscope. When the input voltage is 7V and reference voltage is 3.5V, the fuzzy PID and conventional PID key waveforms are as shown in Fig. 5.10 and Fig. 5.11.

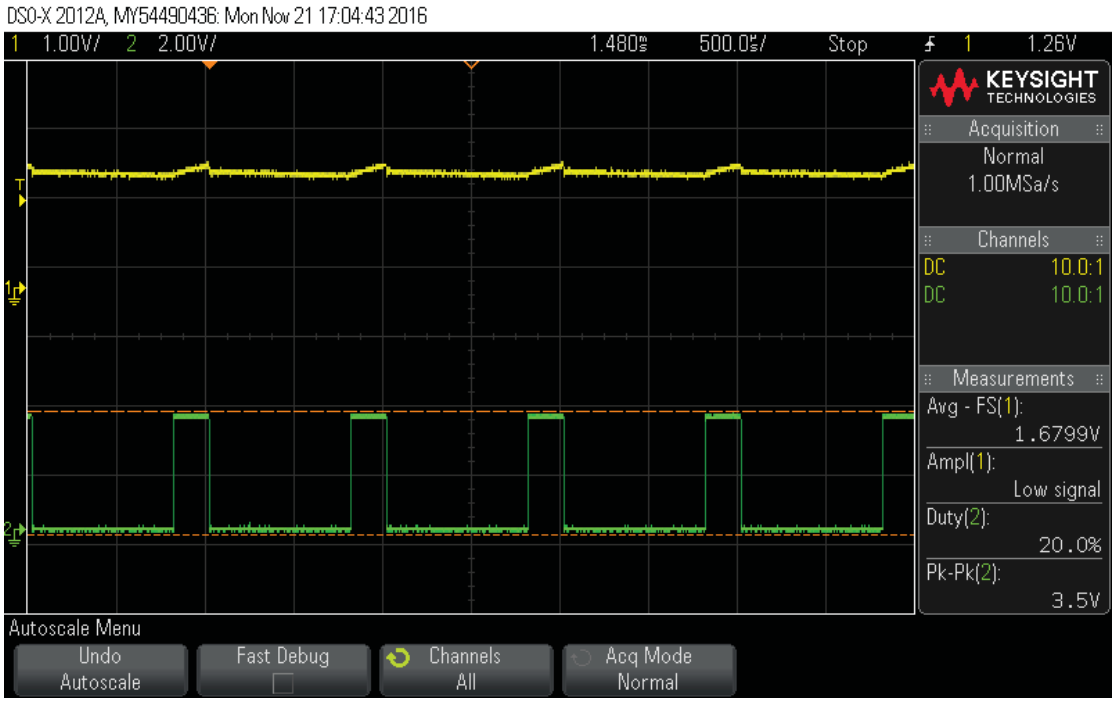

Fig. 5. 10 Output voltage (yellow) and duty cycle (green) in dual input mode controlled by fuzzy PID with 7V input

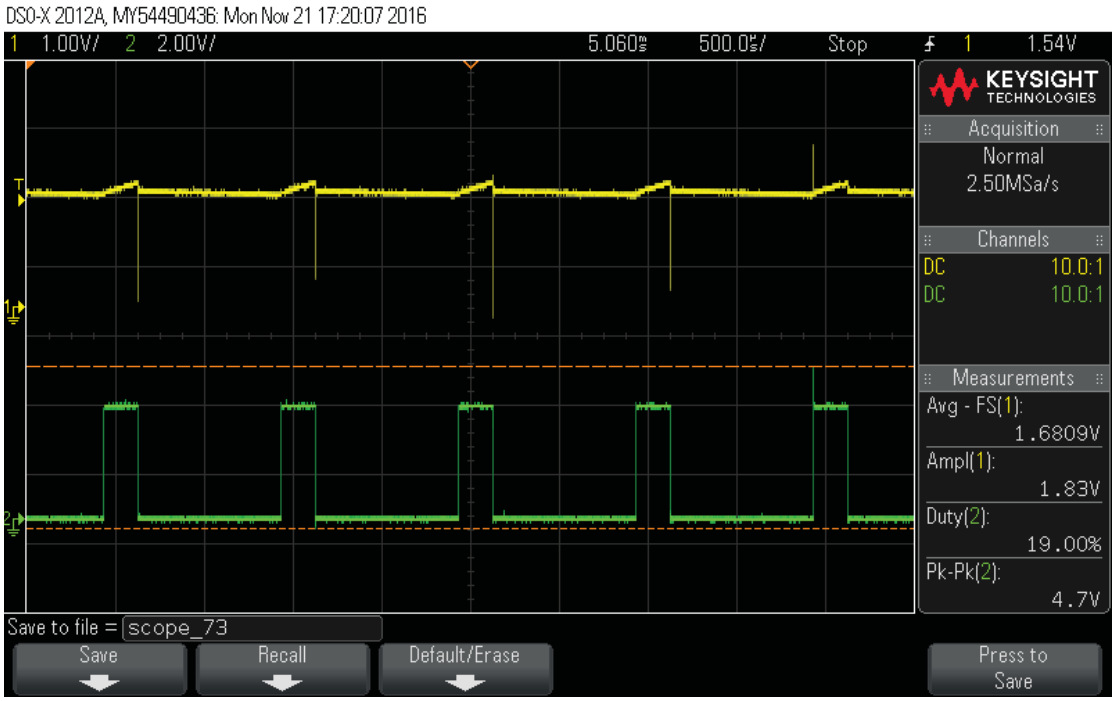

Fig. 5. 11 Output voltage (yellow) and duty cycle (green) in dual input mode controlled by conventional PID with 7V input

When the input voltage is 6V and reference voltage is 2V, the fuzzy PID and conventional PID key waveforms are as shown in Fig. 5.12 and Fig. 5.13.

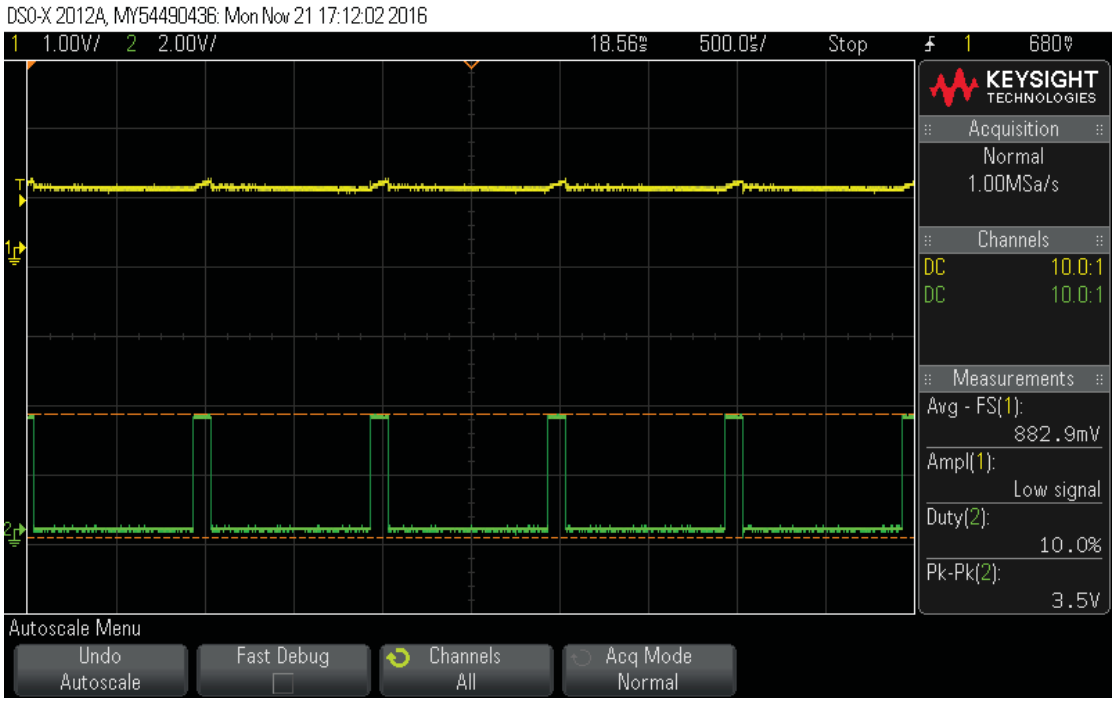

Fig. 5. 12 Output voltage (yellow) and duty cycle (green) in dual input mode controlled by fuzzy PID with 6V input

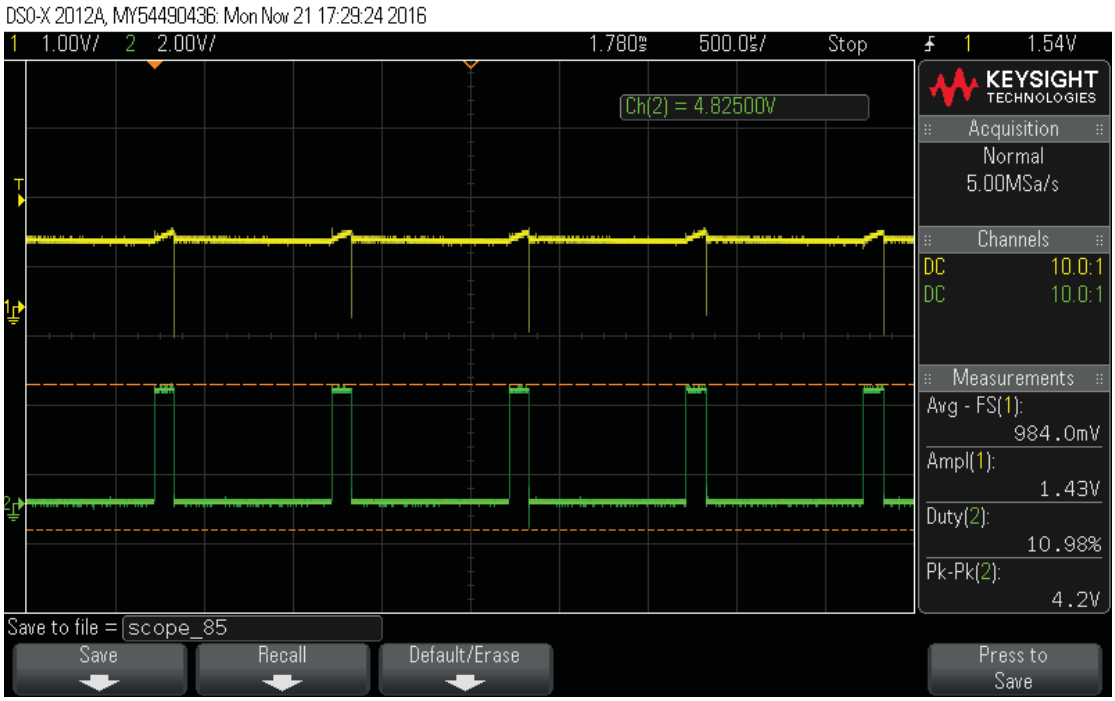

Fig. 5. 13 Output voltage (yellow) and duty cycle (green) in dual input mode controlled by conventional PID with 6V input

When the input voltage is 5V and reference voltage is 2V, the fuzzy PID and conventional PID key waveforms are as shown in Fig. 5.14 and Fig. 5.15.

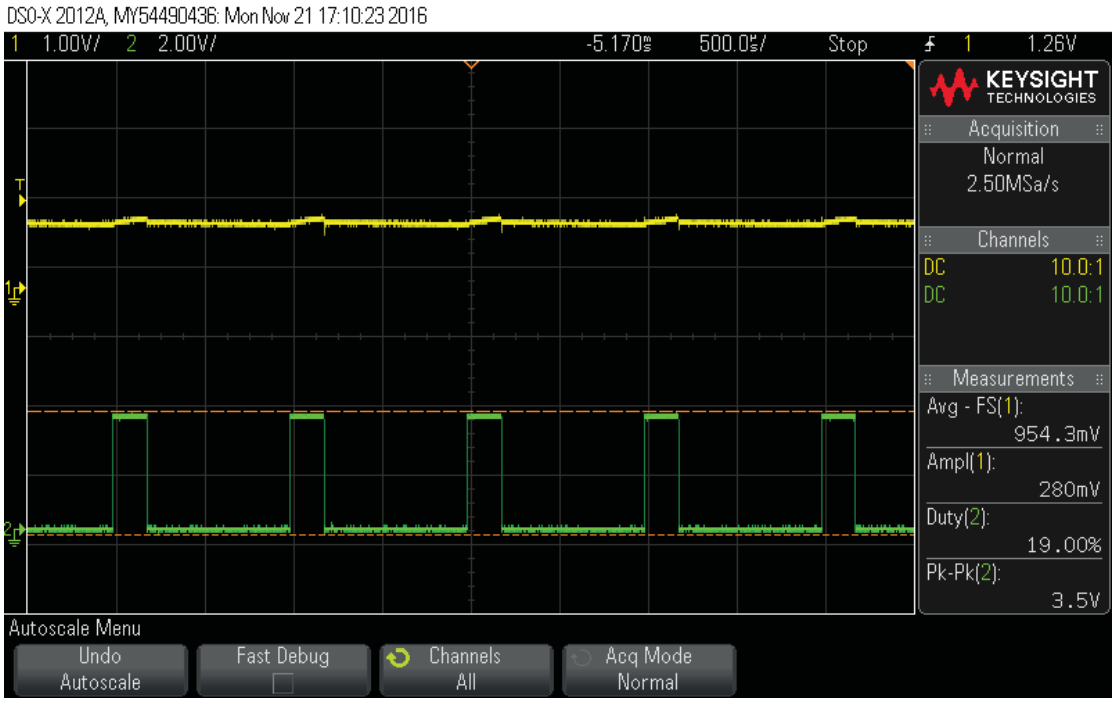

Fig. 5. 14 Output voltage (yellow) and duty cycle (green) in dual input mode controlled by fuzzy PID with 2V input

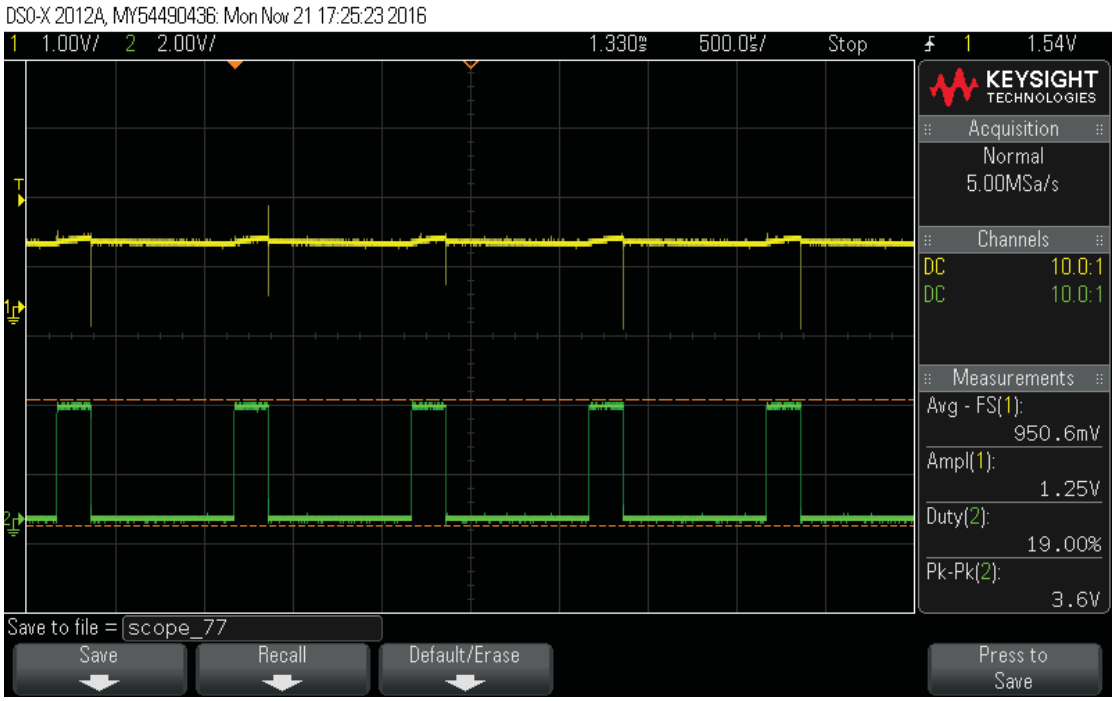

Fig. 5. 15 Output voltage (yellow) and duty cycle (green) in dual input mode controlled by conventional PID with 2V input

Chapter 6 Evaluation

6.1 Results Analysis

Result analysis from the aspects of accuracy, sensitivity, noise, speed, and oscillations has been carried put in this section.

For example, when the input voltage is 6V and the reference voltage is 2V, the amplified waveforms shown in Fig 6.1 and 6.2 would reveal some differences in the performances in the two control methods. An analysis for the two cases is provided below.

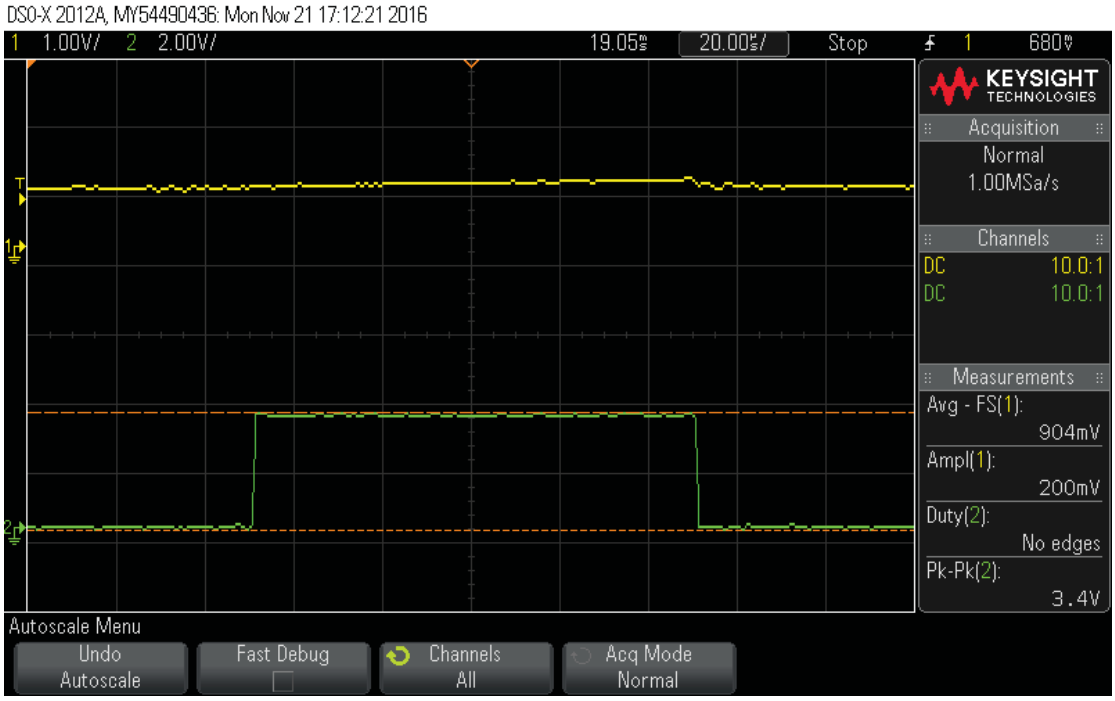

Fig. 6. 1 Output voltage (yellow) and duty cycle (green) in dual input mode with fuzzy PID controller

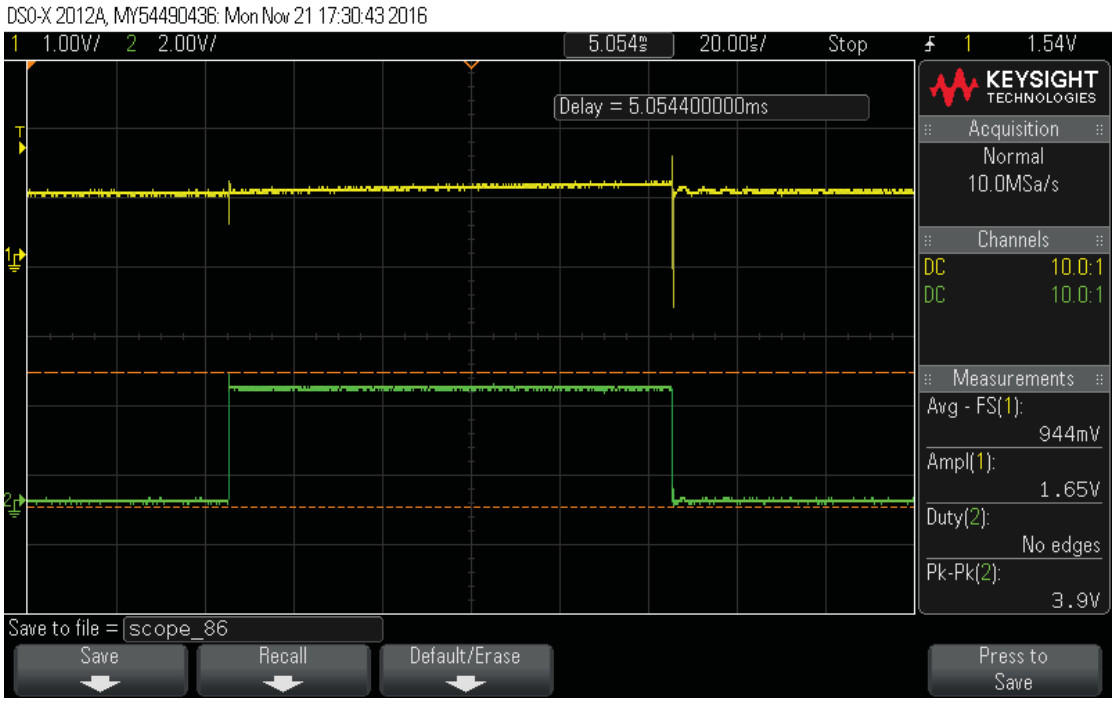

Fig. 6. 2 Output voltage (yellow) and duty cycle (green) in dual input mode with conventional PID controller

From the above figures, the output and duty cycle of fuzzy PID is more stable and robust to noise than conventional PID. The oscilloscope display the output voltage amplitude is 200mV and the peak to peak voltage of the duty cycle is 3.4V, which is controlled by fuzzy PID. Whereas the oscilloscope displays the output voltage amplitude is 1.65V and the peak to peak voltage of the duty cycle is 3.9V, which is controlled by conventional PID. So obviously, the fuzzy PID controller performance of accuracy, sensitivity, robustness to noise, low oscillation and response speed is much better than conventional PID controller.

The disadvantages of conventional PID are shown by following figures, the rising edge and failing edge controlled by conventional PID controller. The reference voltage is 2V and input voltage is 6V. These figures are amplified for showing the instability of conventional PID controller. The output voltage significantly varies in response to the duty cycle variation. However, performance will be apparently improved by fuzzy PID controller, which will be discussed later in next part.

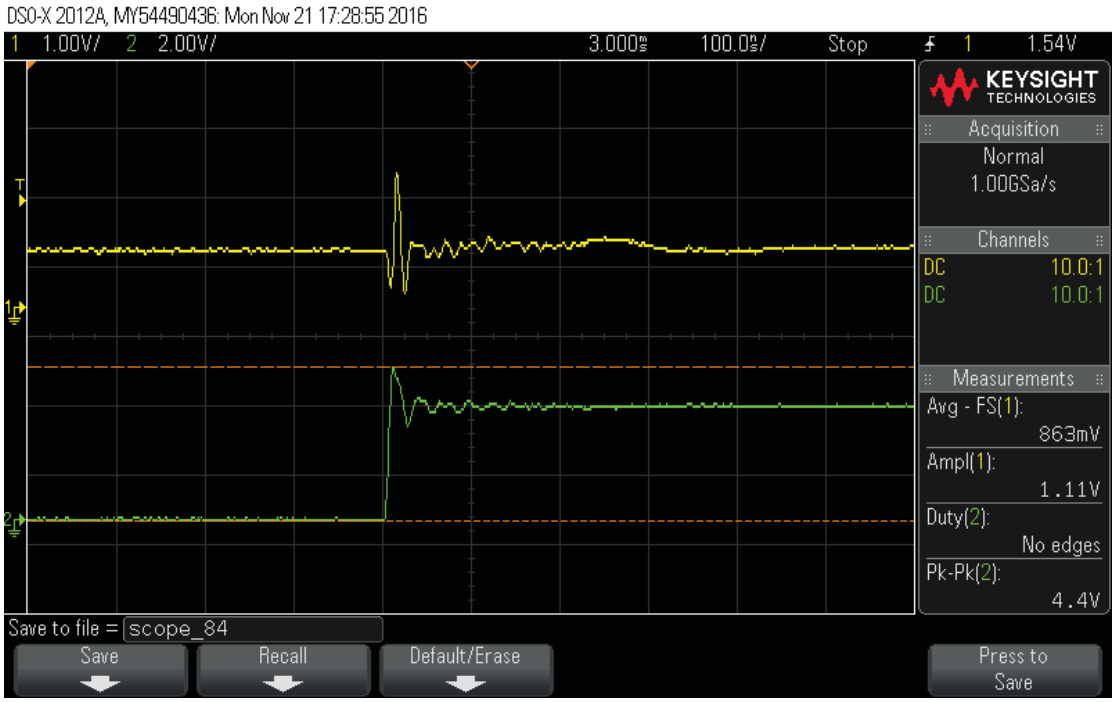

Fig. 6. 3 Duty cycle rising edge (green) and corresponding output voltage (yellow) of conventional PID system with 6V the input voltage

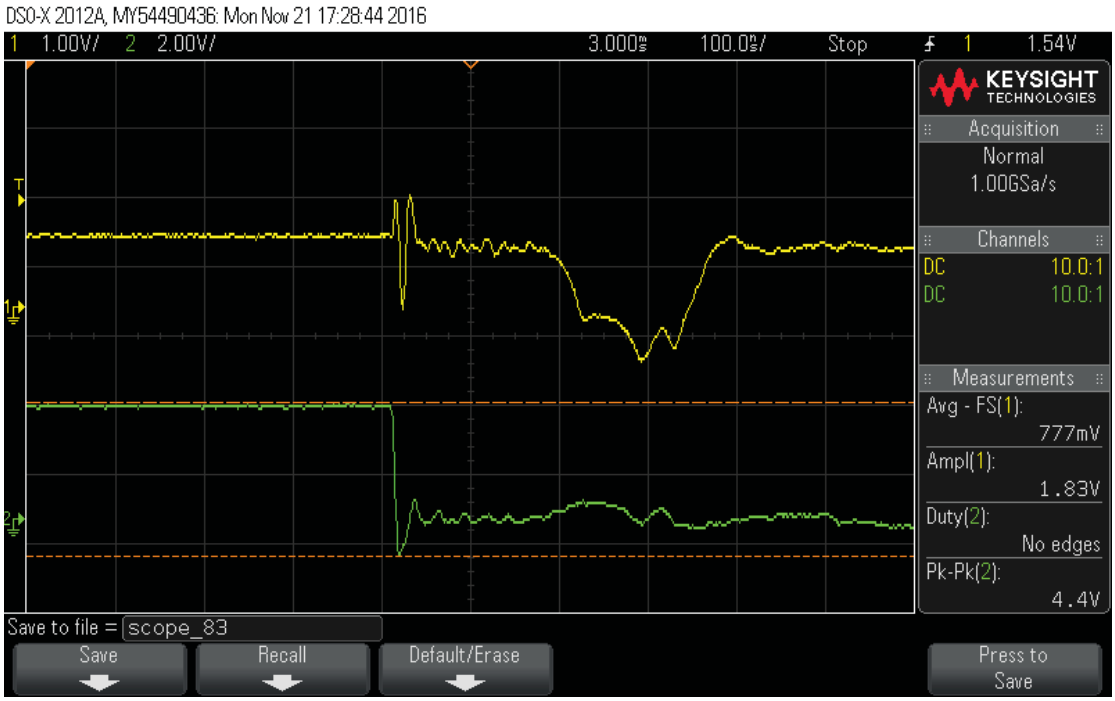

Fig. 6. 4 Duty cycle failing edge (green) and corresponding output voltage (yellow) of conventional PID system with 6V the input voltage

6.2 Comparison

The comparison between conventional PID and fuzzy PID is among several aspects [107]. The figure of these aspects is shown in Fig. 6.5.

- Rise time:

  The time is taken by changing signal from a specified low value to a specified high value. These values may be expressed as ratios or, equivalently, as percentages with respect to a given reference value. In analog or digital electronics, these percentages are commonly the 10% and 90% of the anticipated output.

- Overshoot

Overshoot is the occurrence of a signal or function exceeding its target. The overshoot will occur several times before it tends to stable.

- Steady-state error

  Because a non-zero error is required to drive it, a proportional controller generally operates with a so-called steady-state error. Steady-state error is proportional to the process gain and inversely proportional to proportional gain. It may be mitigated by adding a compensating bias term to the set-point or output, or corrected dynamically by adding an integral term.

- Settling time:

  The time elapsed from the application of an ideal instantaneous step input to the time at which the amplifier output has entered and remained within a specified error band. Settling time includes a very brief propagation delay, plus the time required for the output to slew to the vicinity of the final value, recover from the overload condition associated with slew, and finally settle to within the specified error.

- Stability

  The output will stay bounded for any bounded input for a long time.

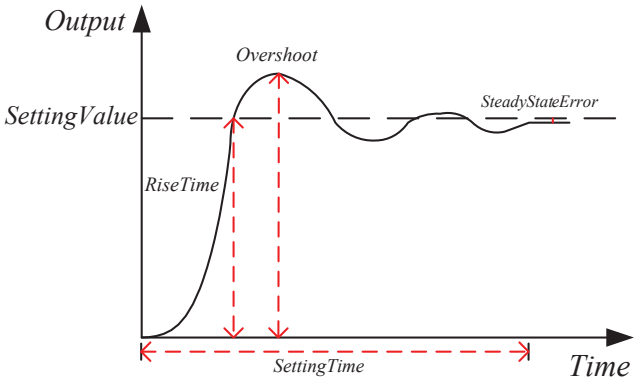

Fig. 6. 5 Aspects to evaluate a control system

The following figures are output comparison between proposed fuzzy PID and conventional PID controller. There are three groups' comparisons. The first group is amplified rising edge and failing edge of duty cycle, when the reference voltage is 3.5V and input voltage is 6V. The second group is amplified rising edge and failing edge of duty cycle, when the reference voltage is 3.5V and input voltage is 7V. The third group is amplified rising edge and failing edge of duty cycle, when the reference voltage is 2.0V and input voltage is 5V.

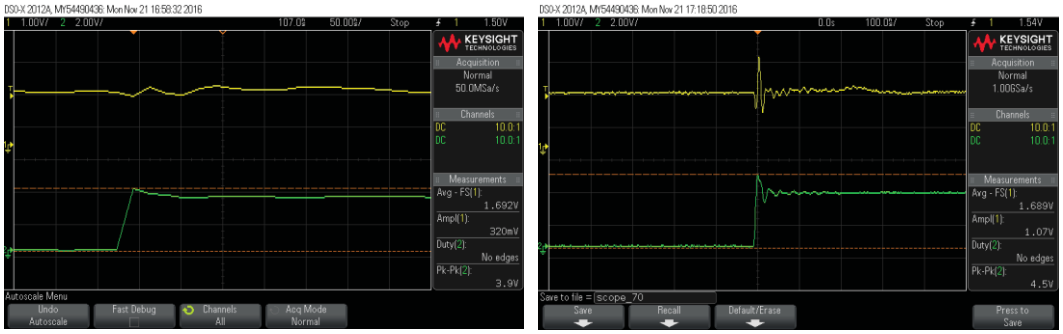

Fig. 6. 6 Rising edge of duty cycle controlled by fuzzy PID (left) and conventional PID (right) with 6V input and 3.5V reference

Fig. 6. 7 Failing edge of duty cycle controlled by fuzzy PID (left) and conventional PID (right) with 6V input and 3.5V reference

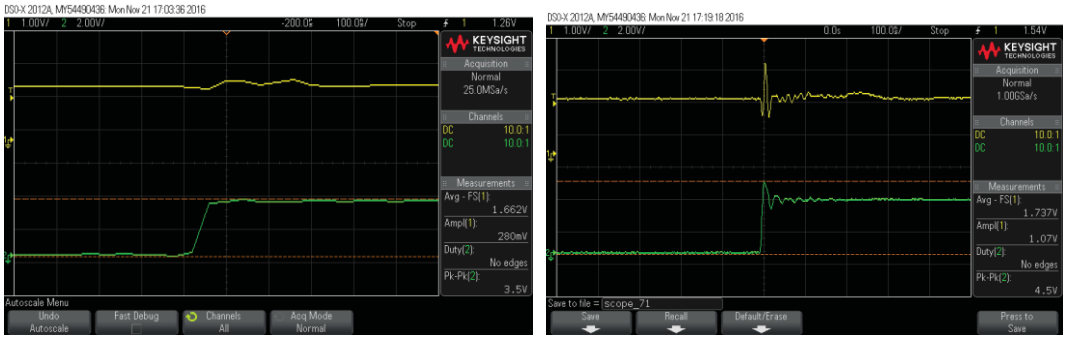

Fig. 6. 8 Rising edge of duty cycle controlled by fuzzy PID (left) and conventional PID (right) with 7V input and 3.5V reference

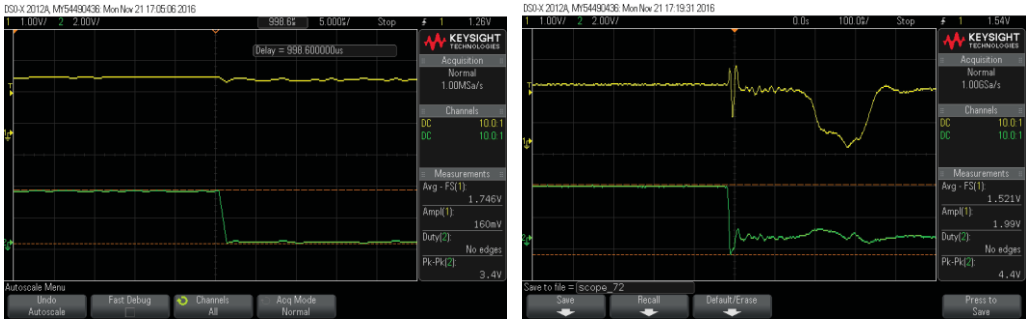

Fig. 6. 9 Failing edge of duty cycle controlled by fuzzy PID (left) and conventional PID (right) with 7V input and 3.5V reference

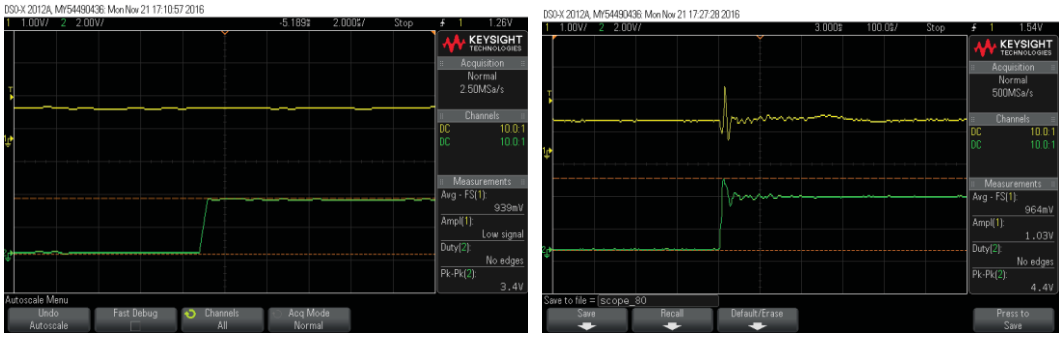

Fig. 6. 10 Rising edge of duty cycle controlled by fuzzy PID (left) and conventional PID (right) with 5V input and 2.0V reference

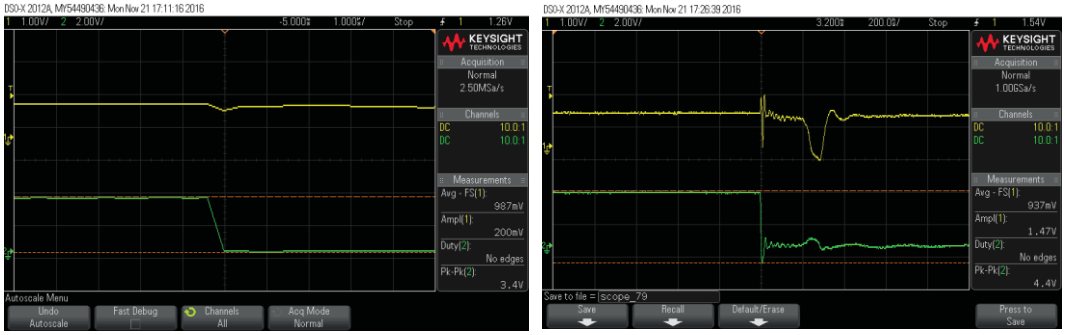

Fig. 6. 11 Failing edge of duty cycle controlled by fuzzy PID (left) and conventional PID (right) with 5V input and 2.0V reference

Chapter 7 Conclusion and Future Possibilities

The objectives of the research are to develop an improved control system for dual-input dual-output DC/DC converter with fuzzy logic theory. Comparisons between conventional PID control system and proposed fuzzy PID control system are made. In conclusion, the improved fuzzy control system is more centralized control and has better performance than conventional PID controller. Analysis and evaluation of the operational principles, mathematical inference, simulation, implementation by STM32f407, and experimental design are also presented.

The project has required a large amount of work to be completed.

First of all, the hardware circuit needs to be improved because switching power supplies have output ripple inevitable, which may cause the inaccuracy and instability of the whole system. Printed Circuit Board (PCB) is necessary for the hardware design, because the well-designed PCB board is helpful to avoid most of the noise.

Secondly, algorithm can be optimized by adding Kalman filtering [108] for reducing the noise produced by control system. The Kalman filter uses a system's dynamics model, known control inputs to system, and multiple sequential measurements to form an estimate of the system's varying quantities that is better than the estimate obtained by using only one measurement alone.

Thirdly, there are still some limitations of the proposed fuzzy control system,

1. Fuzzy systems lack the capability of machine learning as well as neural network type pattern recognition.
2. Verification and validation of a fuzzy knowledge based system require extensive testing with hardware
3. Determining exact fuzzy ruled and membership functions is a hard task and need to be continuously optimized.
4. Stability is an important concern for fuzzy control

The above-mentioned problems are the future work need to be improved for better performance of the proposed control system.

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Appendix

Codes for implementation with STM32f407, using C programming language

- Codes for Main.c

```
#include "led.h"
#include "delay.h"
#include "key.h"
#include "sys.h"
#include "usart.h"
#include "timer.h"
#include "adc.h"
#include "pid.h"
#include "stm32f10x_adc.h"
#include "math.h"
float Get_Vol(u8 ch, u16 times);
u16 VolToPWM(float Vol);
float temp_adc = 0;
#define REFVOL 2.0
 int main(void)
 {
      //float temp_adc = 0;
      float temp_vol = 0;
        u16 PWM;
        u16 i=1;
      delay_init();                    //
      uart_init(9600);        //
      LED_Init();                          //
      TIM3_PWM_Init(100-1,719);         //10khz
   PID_Init(0.01,0.4,0.2);
      Adc_Init();
```

```
    while(1)
    {
        /*printf("the ouput vol is %f\n",Get_Vol(ADC_Channel_2,20));
        delay_ms(4000);
        printf("the input vol is %f\n",Get_Vol(ADC_Channel_3,20));
        delay_ms(4000);*/

          temp_adc = Get_Vol(ADC_Channel_2,20);
          printf("the voltage is %f\n", temp_adc);
          //delay_ms(5000);

              temp_vol = PID_realized(REFVOL,temp_vol);
            printf("the temp_vol is %f",temp_vol);

              PWM = VolToPWM(temp_vol);
        printf("the PWM is %d\n",PWM);

          TIM_SetCompare1(TIM3, PWM);
       TIM_SetCompare2(TIM3, PWM);

        }

        }

float Get_Vol(u8 ch, u16 times)
{
   u16 adcx;
    float temp=0.00;
    adcx =    Get_Adc_Average(ch, times);
```

```
    temp = (float)adcx/4096*3.3;
        return temp;


}

u16 VolToPWM(float Vol)
{
    float PWM_Value;

    PWM_Value = (Vol * 100)/(Get_Vol(ADC_Channel_3,20)*6);
    return (u16)(fabs(PWM_Value));
}
```

- Codes for Timer.c

```
#include "timer.h"
#include "led.h"
#include "usart.h"

void TIM3_Int_Init(u16 arr,u16 psc)
{
        TIM_TimeBaseInitTypeDef    TIM_TimeBaseStructure;
        NVIC_InitTypeDef NVIC_InitStructure;

        RCC_APB1PeriphClockCmd(RCC_APB1Periph_TIM3, ENABLE); //

        TIM_TimeBaseStructure.TIM_Period = arr;    ¼ÆÊýµ½5000Îª500ms
        TIM_TimeBaseStructure.TIM_Prescaler=psc;
        TIM_TimeBaseStructure.TIM_ClockDivision = 0;
```

```
    TDTS = Tck_tim
    TIM_TimeBaseStructure.TIM_CounterMode = TIM_CounterMode_Up;
    TIM_TimeBaseInit(TIM3, &TIM_TimeBaseStructure);
    TIM_ITConfig(TIM3,TIM_IT_Update,ENABLE );

    NVIC_InitStructure.NVIC_IRQChannel = TIM3_IRQn;  //TIM3
    NVIC_InitStructure.NVIC_IRQChannelPreemptionPriority = 0;
    NVIC_InitStructure.NVIC_IRQChannelSubPriority = 3;  //
    NVIC_InitStructure.NVIC_IRQChannelCmd = ENABLE; //
    NVIC_Init(&NVIC_InitStructure);
    TIM_Cmd(TIM3, ENABLE);  //

}
void TIM3_IRQHandler(void)
{
    if (TIM_GetITStatus(TIM3, TIM_IT_Update) != RESET)
        {
        TIM_ClearITPendingBit(TIM3, TIM_IT_Update  );
        LED1=!LED1;
        }
}

void TIM3_PWM_Init(u16 arr,u16 psc)
{
    GPIO_InitTypeDef GPIO_InitStructure;
    TIM_TimeBaseInitTypeDef  TIM_TimeBaseStructure;
    TIM_OCInitTypeDef  TIM_OCInitStructure;

    RCC_APB1PeriphClockCmd(RCC_APB1Periph_TIM3, ENABLE);
    RCC_APB2PeriphClockCmd(RCC_APB2Periph_GPIOA|RCC_APB2Periph_AFIO,
```

```
ENABLE);

    GPIO_InitStructure.GPIO_Pin = GPIO_Pin_6|GPIO_Pin_7; //TIM_CH2
    GPIO_InitStructure.GPIO_Mode = GPIO_Mode_AF_PP;    //¸´ÓÃÍÆÍìÊä³ö
    GPIO_InitStructure.GPIO_Speed = GPIO_Speed_50MHz;
    GPIO_Init(GPIOA, &GPIO_InitStructure);//³õÊ¼»¯GPIO

    TIM_TimeBaseStructure.TIM_Period = arr;
    TIM_TimeBaseStructure.TIM_Prescaler =psc;
    TIM_TimeBaseStructure.TIM_ClockDivision = 0; //ÉèÖÃÊ±ÖÓ·Ö,î:TDTS = Tck_tim
    TIM_TimeBaseStructure.TIM_CounterMode=TIM_CounterMode_Up;
    TIM_TimeBaseInit(TIM3,&TIM_TimeBaseStructure);
    TIM_OCInitStructure.TIM_OCMode=TIM_OCMode_PWM1;
    TIM_OCInitStructure.TIM_OutputState = TIM_OutputState_Enable;
    TIM_OCInitStructure.TIM_OCPolarity=TIM_OCPolarity_High;
    TIM_OC1Init(TIM3, &TIM_OCInitStructure);
    TIM_OC2Init(TIM3, &TIM_OCInitStructure);
    TIM_OC1PreloadConfig(TIM3, TIM_OCPreload_Enable);
    TIM_OC2PreloadConfig(TIM3, TIM_OCPreload_Enable);
    TIM_Cmd(TIM3, ENABLE);    /
}
```

- Codes for adc.c

```
#include "adc.h"
 #include "delay.h"
 #include "stm32f10x_adc.h"
void    Adc_Init(void)
{
    ADC_InitTypeDef ADC_InitStructure;
    GPIO_InitTypeDef GPIO_InitStructure;
```

```
    RCC_APB2PeriphClockCmd(RCC_APB2Periph_GPIOA    |RCC_APB2Periph_ADC1
    , ENABLE );

    RCC_ADCCLKConfig(RCC_PCLK2_Div6);
    GPIO_InitStructure.GPIO_Pin = GPIO_Pin_2|GPIO_Pin_3;
    GPIO_InitStructure.GPIO_Mode = GPIO_Mode_AIN;
    GPIO_Init(GPIOA, &GPIO_InitStructure);

    ADC_DeInit(ADC1);
    ADC_InitStructure.ADC_Mode = ADC_Mode_Independent;
    ADC_InitStructure.ADC_ScanConvMode = DISABLE;
    ADC_InitStructure.ADC_ContinuousConvMode = DISABLE;
    ADC_InitStructure.ADC_ExternalTrigConv = ADC_ExternalTrigConv_None;
    ADC_InitStructure.ADC_DataAlign = ADC_DataAlign_Right;
    ADC_InitStructure.ADC_NbrOfChannel = 1;
    ADC_Init(ADC1, &ADC_InitStructure);
    ADC_Cmd(ADC1, ENABLE);
    ADC_ResetCalibration(ADC1);

    while(ADC_GetResetCalibrationStatus(ADC1));
    ADC_StartCalibration(ADC1);
    while(ADC_GetCalibrationStatus(ADC1));

//  ADC_SoftwareStartConvCmd(ADC1, ENABLE);

}
u16 Get_Adc(u8 ch)
{
    ADC_RegularChannelConfig(ADC1, ch, 1, ADC_SampleTime_239Cycles5 );
```

```
    ADC_SoftwareStartConvCmd(ADC1, ENABLE);
    while(!ADC_GetFlagStatus(ADC1, ADC_FLAG_EOC ));
    return ADC_GetConversionValue(ADC1);
}

u16 Get_Adc_Average(u8 ch,u8 times)
{
    u32 temp_val=0;
    u8 t;
    for(t=0;t<times;t++)
    {
        temp_val+=Get_Adc(ch);
        delay_ms(5);
    }
    return temp_val/times;
}
```

- Codes for pid.c

```
#include "sys.h"
#include "delay.h"
#include "pid.h"
#include "math.h"
pid PID_Vol;

void PID_Init(float kd, float kp, float ki)
 {
    PID_Vol.err = 0.0;
    PID_Vol.err_last = 0.0;
    PID_Vol.Integral = 0;
      PID_Vol.kd = kd;
```

```
    PID_Vol.kp = kp;
        PID_Vol.ki = ki;
        PID_Vol.SetVol = 0;
    PID_Vol.Vol = 0;
    PID_Vol.ActualVol = 0;

 }

float PID_realized(float Vol_Typical, float Vol_actual)
 {
        float Voltage_Out_Put;
    //PID_Vol.SetVol = Vol_Typical;
      // PID_Vol.ActualVol = Vol_actual;
        PID_Vol.err = Vol_Typical - Vol_actual;
    PID_Vol.Integral += PID_Vol.err;

        PID_Vol.Vol = PID_Vol.kp * PID_Vol.err + PID_Vol.Integral *PID_Vol.ki + PID_Vol.kd
*(PID_Vol.err - PID_Vol.err_last);
    PID_Vol.err_last = PID_Vol.err;
        PID_Vol.ActualVol    = PID_Vol.Vol;

        return PID_Vol.Vol;
}
```

- Codes for delay.c

```
#include "delay.h"
#include "sys.h"

#if SYSTEM_SUPPORT_UCOS
#include "includes.h"
```

```
#endif
//////////////////////////////////////////////////////////////////////////////////

static u8  fac_us=0;
static u16 fac_ms=0;
#ifdef OS_CRITICAL_METHOD
void SysTick_Handler(void)
{
    OSIntEnter();
    OSTimeTick();
    OSIntExit();
}
#endif

void delay_init()
{

#ifdef OS_CRITICAL_METHOD
    u32 reload;
#endif
    SysTick_CLKSourceConfig(SysTick_CLKSource_HCLK_Div8);
    fac_us=SystemCoreClock/8000000;

#ifdef OS_CRITICAL_METHOD
    reload=SystemCoreClock/8000000;
    reload*=1000000/OS_TICKS_PER_SEC;

    fac_ms=1000/OS_TICKS_PER_SEC;
    SysTick->CTRL|=SysTick_CTRL_TICKINT_Msk;
    SysTick->LOAD=reload;
```

```
    SysTick->CTRL|=SysTick_CTRL_ENABLE_Msk;
#else
    fac_ms=(u16)fac_us*1000;/
#endif
}

#ifdef OS_CRITICAL_METHOD
void delay_us(u32 nus)
{
    u32 ticks;
    u32 told,tnow,tcnt=0;
    u32 reload=SysTick->LOAD;
    ticks=nus*fac_us;
    tcnt=0;
    told=SysTick->VAL;
    while(1)
    {
        tnow=SysTick->VAL;
        if(tnow!=told)
        {
            if(tnow<told)tcnt+=told-tnow;
            else tcnt+=reload-tnow+told;
            told=tnow;
            if(tcnt>=ticks)break;
        }
    };
}
void delay_ms(u16 nms)
{
    if(OSRunning==TRUE)
```

```
    {
        if(nms>=fac_ms)
        {
            OSTimeDly(nms/fac_ms);//
        }
        nms%=fac_ms;
    }
    delay_us((u32)(nms*1000));
}
#else.
void delay_us(u32 nus)
{
    u32 temp;
    SysTick->LOAD=nus*fac_us;
    SysTick->VAL=0x00;
    SysTick->CTRL|=SysTick_CTRL_ENABLE_Msk ;
    do
    {
        temp=SysTick->CTRL;
    }
    while(temp&0x01&&!(temp&(1<<16)));
    SysTick->CTRL&=~SysTick_CTRL_ENABLE_Msk;
    SysTick->VAL =0X00;
}
void delay_ms(u16 nms)
{
    u32 temp;
    SysTick->LOAD=(u32)nms*fac_ms;
    SysTick->VAL =0x00;
    SysTick->CTRL|=SysTick_CTRL_ENABLE_Msk ;
```

```
    do
    {
        temp=SysTick->CTRL;
    }
    while(temp&0x01&&!(temp&(1<<16)));
    SysTick->CTRL&=~SysTick_CTRL_ENABLE_Msk;
    SysTick->VAL =0X00;
}
#endif
```

- Codes for usart.c

```
#include "sys.h"
#include "usart.h"
#if SYSTEM_SUPPORT_UCOS
#include "includes.h"
#endif

#if 1
#pragma import(__use_no_semihosting)
struct __FILE
{
    int handle;
};

FILE __stdout;
_sys_exit(int x)
{
    x = x;
}
int fputc(int ch, FILE *f)
```

```
{
	while((USART1->SR&0X40)==0);
	USART1->DR = (u8) ch;
	return ch;
}
#endif

#if EN_USART1_RX
u8 USART_RX_BUF[USART_REC_LEN];
u16 USART_RX_STA=0;

void uart_init(u32 bound){
	GPIO_InitTypeDef GPIO_InitStructure;
	USART_InitTypeDef USART_InitStructure;
	NVIC_InitTypeDef NVIC_InitStructure;

	RCC_APB2PeriphClockCmd(RCC_APB2Periph_USART1|RCC_APB2Periph_GPIOA,
ENABLE);
	USART_DeInit(USART1);
	 //USART1_TX	PA.9
	GPIO_InitStructure.GPIO_Pin = GPIO_Pin_9; //PA.9
	GPIO_InitStructure.GPIO_Speed = GPIO_Speed_50MHz;
	GPIO_InitStructure.GPIO_Mode = GPIO_Mode_AF_PP;
	GPIO_Init(GPIOA, &GPIO_InitStructure);

	//USART1_RX		PA.10
	GPIO_InitStructure.GPIO_Pin = GPIO_Pin_10;
	GPIO_InitStructure.GPIO_Mode = GPIO_Mode_IN_FLOATING;
	GPIO_Init(GPIOA, &GPIO_InitStructure);
```

```
	NVIC_InitStructure.NVIC_IRQChannel = USART1_IRQn;
	NVIC_InitStructure.NVIC_IRQChannelPreemptionPriority=3 ;
	NVIC_InitStructure.NVIC_IRQChannelSubPriority = 3;
	NVIC_InitStructure.NVIC_IRQChannelCmd = ENABLE;
	NVIC_Init(&NVIC_InitStructure);
	USART_InitStructure.USART_BaudRate = bound;//Ò»°ãÉèÖÃÎª9600;
	USART_InitStructure.USART_WordLength= USART_WordLength_8b;
	USART_InitStructure.USART_StopBits = USART_StopBits_1;
	USART_InitStructure.USART_Parity = USART_Parity_No;
	USART_InitStructure.USART_HardwareFlowControl=USART_HardwareFlowControl_
None;
	USART_InitStructure.USART_Mode = USART_Mode_Rx | USART_Mode_Tx;

	USART_Init(USART1, &USART_InitStructure);
	USART_ITConfig(USART1, USART_IT_RXNE, ENABLE);
	USART_Cmd(USART1, ENABLE);
}

void USART1_IRQHandler(void)
	{
	u8 Res;
#ifdef OS_TICKS_PER_SEC
	OSIntEnter();
#endif
	if(USART_GetITStatus(USART1, USART_IT_RXNE) != RESET)
		{
		Res =USART_ReceiveData(USART1);//(USART1->DR);

		if((USART_RX_STA&0x8000)==0)
			{
```

```
                if(USART_RX_STA&0x4000)
                    {
                    if(Res!=0x0a)USART_RX_STA=0;
                    else USART_RX_STA|=0x8000;
                    }
                else
                    {
                    if(Res==0x0d)USART_RX_STA|=0x4000;
                    else
                        {
                        USART_RX_BUF[USART_RX_STA&0X3FFF]=Res ;
                        USART_RX_STA++;
                        if(USART_RX_STA>(USART_REC_LEN-1))USART_RX_STA=0;
                        }
                    }
                }
        }
#ifdef OS_TICKS_PER_SEC
OSIntExit();
#endif
}
#endif
```