NANO-METRIC OPTIMISED CMOS RF RECEIVER FRONT-END COMPONENTS FOR UHF RFID READERS

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JIE (JACK) LI

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ABSTRACT

Nano-metric Optimised CMOS RF Receiver Front-end Components for UHF RFID Readers

Jie (Jack) Li
Doctor of Philosophy in Engineering – School of Engineering and Technology
Massey University, Auckland, New Zealand

As the capabilities of wireless hand-held devices continue to increase, more pressure is placed on the performance of RF transceiver front-ends. The primary objective of this research is to investigate optimal methods of implementing a receiver front-end with reduced power dissipation, reduced design complexity and minimised cost. This design will be implemented on CMOS technology due to its advantages in system integration and low-cost mass production.

This thesis presents the optimisation of a CMOS RF receiver front-end components design for 866 MHz UHF RFID readers. The completed receiver front-end was fabricated on an IBM 130nm CMOS process. Circuit-level techniques were employed to reduce chip size and power consumption while providing enhanced performance. The inclusion of the finite drain-source conductance g_{ds} effect improves the nano-metric design optimisation algorithm. Simulated results and experimental data are presented that demonstrate the RF receiver design with low power dissipation and low noise while providing high performance.

Low-noise amplifiers using a power-constrained simultaneous noise and input matching (PCSNIM) technique are presented first. In contrast to previously published narrow-band LNA designs, the proposed design methodology includes the finite drain-source conductance of devices, thus achieving simultaneous impedance and minimum noise matching at the very low power drain of 1.6mW from a 1V supply. The LNA delivers a power gain (S21) of 17dB, a reverse isolation (S12) of -34dB and an input power

reflection (S11@866 MHz) of -30dB. It has a minimum pass-band NF of around 2dB and a 3rd order input referred intercept point (IIP3) of -16dBm.

A low noise mixer is also presented utilising the PCSNIM topology with current bleeding techniques. This design is proposed to replace the conventional Gilbert cell mixer that usually exhibits a high noise figure. The proposed mixer has demonstrated the ability to scale to the targeted 130nm process and meets design requirement at the required operating frequency. It has a power conversion gain of 14.5dB, DSB noise figure of 8.7dB DSB and an IIP3 of -5.1dBM. The mixer core itself only consumes 6mW from a 1.2V supply and the complete test circuit consumes 10mW with a balun at each port.

Finally, a voltage controlled oscillator (VCO) is presented. A quadrature VCO (QVCO) structure is selected to overcome the image rejection issue. Since the main goal for this work is to design a low power receiver front-end, a folded-cascode topology is employed to enable the QVCO to operate under 1V power supply. The proposed VCO has a phase noise of -140dBc/Hz at 3-MHz offset from the carrier with only 5mW of power dissipation. This gives a FoM value of -181dBc/Hz that compares favourably to recently published designs.

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Dedicated to my parents

DECLARATION

The author declares that this is his own work except where due acknowledgement has been given. It is being submitted for the PhD in Engineering to Massey University, New Zealand.

This thesis describes the research carried out by the author at the School of Engineering, Massey University, New Zealand from February 2007 to February 2011, supervised by Dr. Rezaul Hasan.

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DEFINITIONS AND ABBREVIATIONS

3G	Third Generation
AC	Alternating Current
ADS	Agilent's Advanced Design System program
AM	Amplitude Modulation
BB	Baseband
BiCMOS	Bipolar-Complementary Metal Oxide Semiconductor
BJT	Bipolar Junction Transistor
CAD	Computer Aided Design
CMOS	Complementary Metal Oxide Semiconductor
CG	Common-gate
CP	Compression Point
DAC	Digital to Analog Converter
DC	Direct Current
DRC	Design Rule Check
DSP	Digital Signal Processing
DUT	Device / Die Under Test
EDGE	Enhanced Data rates for GSM Evolution
ESD	Electrostatic Discharge
F	Noise factor
FFT	Fast Fourier Transform
FM	Frequency Modulation
FSK	Frequency Shift Keying
GaAs	Gallium Arsenide
GDSII	Gerber Data Stream Information Interchange
GHz	Gigahertz
GPRS	General Packet Radio Service
GPS	Global Positioning System
GSM	Global System for Mobile Communications
Hz	Hertz

HF	High Frequency
I/O	Input-Output
IC	Integrated Circuit
IEEE	The Institute of Electrical and Electronics Engineers, Inc.
IF	Intermediate Frequency
IIP3	Input Third Order Intercept Point
IM	Inter-modulation
IM3	Third Order Inter-modulation
IP2	Second Order Intercept Point
IP3	Third Order Intercept Point
ISF	Impulse Sensitivity Function
I/Q	In phase-Quadrature phase
KCL	Kirchoff Current Law
KVL	Kirchoff Voltage Law
LAN	Local Area Network
LC	Inductor-Capacitor
LF	Low Frequency
LNA	Low-Noise Amplifier
LO	Local Oscillator
LPF	Low Pass Filter
LSB	Lower Sideband
LTI	Linear Time-Invariant
LTV	Linear Time Varying
LVS	Layout versus Schematic
MIMO	Multiple Input – Multiple Output
MCM	Multi Carrier Modulation
MOS	Metal Oxide Semiconductor
NF	Noise Figure
OFDM	Orthogonal Frequency Division Multiplexing
P1dB	1-dB Gain Compression Measurement
PA	Power Amplifier
PGS	Patterned Ground Shield
PSK	Phase Shift Keying
PSRR	Power Supply Rejection Ratio

PSS	Periodic Steady State
Q	Quality Factor
QAM	Quadrature Amplitude Modulation
QPSK	Quadrature Phase Shift Keying
QVCO	Quadrature Voltage Controlled Oscillator
RF	Radio Frequency
RFIC	Radio Frequency Integrated Circuit
RFID	Radio Frequency Identification
Rx	Receiver
SAW	Surface Acoustic Wave
SCM	Single Carrier Modulation
SNR	Signal to Noise Ratio
SoC	System on Chip
SSB	Single Sideband
Tx	Transmitter
UHF	Ultra-high Frequency
UMTS	Universal Mobile Telecommunications System
USB	Upper Sideband
UWB	Ultra Wide Band
VCO	Voltage Controlled Oscillator
VGA	Variable Gain Amplifier
VNA	Vector Network Analyser
WCDMA	Wideband Code Division Multiple Access
WLAN	Wireless Local Area Network
WPAN	Wireless Personal Area Networks
XDB	Gain Compression

CHAPTER 1: INTRODUCTION

Applications for wireless communication technology have multiplied in the last few decades. Substantial research and commercial products have been produced for applications in the fields of cellular phones, WLANs and GPS. In the meantime, the growing demand for IC-based RF products encourages compact, multi-functional, low-power and high performance design. This trend will continue in the foreseeable future as System-on-Chip (SoC) products continue to increase in complexity.

Complementary metal–oxide–semiconductor (CMOS) manufacturing processes hold the dominant position in RF device production due to a combination of low cost, area-efficient deep-submicron scales and high cut-off frequency f_T. When compared with other technologies such as Gallium arsenide (GaAs), High electron mobility transistor (HEMT), Heterojunction bipolar transistor (HBT) and Bipolar junction transistor (BJT), CMOS processes also offer the advantage of higher levels of system integration and reduced power consumption which are important criteria for modern SoC RF solutions. Passive components such as inductors and capacitors, which are essential in RF design, can also be integrated into modern CMOS technologies.

In the RF receiver system, “front-end” is a generic term for all the receiver blocks between the antenna and the intermediate frequency (IF) stage. In super-heterodyne architectures, the receiver blocks consist of matching circuits between successive stages (including buffer and balun), band-pass filters (BPF), low noise amplifiers (LNA), down-converter mixers and voltage controlled oscillators (VCO).

While performing broadband characterisation, accurate modelling of MOSFET noise is a critical and challenging issue for RF receiver front-end designs, particularly with short channel MOSFETs. The design methodology aims to minimise the impact of noise on the complete integrated SoC.

1.1 Research Challenges

Operating frequencies in the GHz range is a challenge for CMOS-based RF receiver front-ends as the transistors and some lumped elements are pushed to their physical frequency limits. This may impact system linearity by introducing undesired coupling and skin effects in both active and passive components. Accurate modellings of these components are therefore essential for RF design. Model parameters of interest include high frequency characteristics, process-induced parameter variation, device noise sources, as well as corner effect definitions. Accurate RF models require device characterisation over a wide range of operating parameters. The detailed design methodology for RF transceiver front-end components involves understanding each component's specification to determine transistor sizes, associated parasitic passive components, design of impedance matching circuitry, physical circuit layout and test set-up for characterisation of the fabricated designs.

1.2 Research Objectives

In this thesis, the design techniques for each front-end component are explored to provide an optimised design solution for a RFID receiver. The objectives for this thesis are as follows:

1. Thoroughly review relevant knowledge and publications on design techniques for implementing state-of-the-art transceiver front-end blocks for UHF RFID systems. Analyse the shortcomings in existing design methodologies. Investigate opportunities for further improvement and development.

2. Develop improved methodologies for circuit design based on Research Objective 1. Implement the IC design and simulation software to meet targeted design specifications.

3. Evaluate system performance at both the schematic and layout design stages. Fabricate initial design for the measurement of system performance. Compare these

results with recently published designs to provide recommendations and insights into the direction for future work on IC-based RF systems.

1.3 Contributions to Knowledge

The research described in subsequent chapters of this thesis makes original contributions to knowledge in the field of RF receiver front-end design for RFID applications by:

1. Investigating and discussing front-end block and system design and analysing challenges for existing systems and recently published designs.

2. Introducing finite transistor drain-source conductance into the system design methodologies, thereby simultaneous optimise the noise, impedance matching and power dissipation for LNAs and mixers design.

3. Combining different techniques and topologies into each RF front-end block design to improve the overall system performance in selectivity, sensitivity and power dissipation

1.4 Thesis Outline

In Chapter 2, an overview of the RF receiver structure is discussed including each key component of the front-end block. Low-noise amplifiers are studied first as they not only amplify the incoming RF signal but also contribute most of the noise. The mixer located between the RF and IF sections is then discussed; particularly, the constraints of port-to-port isolations, conversion gain and linearity. The features of VCOs are introduced next, of which phase noise and quadrature signals are two important design characteristics. A balun is also implemented to perform hybrid (or inverted) signal transformation between successive components.

In Chapter 3, the design methodologies for each RF receiver front-end component are discussed. The implementations based on these methodologies are performed in Chapter 4.

The performances of the front-end components are analysed, simulated and tested in Chapter 5. Chapter 6 summarizes the research outcomes of this thesis. Challenges and issues arising from this research are discussed next and the possible directions of future research are described at the end.

CHAPTER 2: LITERATURE REVIEW

Designing an analogue integrated circuit is inextricably tied to the implemented manufacturing process. Critical device characteristics change between different technology processes, transistor dimensions and supply voltages. Circuit techniques that work well on one process generation are often superseded on the next. RFID technology, with the useful applications in automatic detection and identification of people, objects and animals, is certainly no exception to this trend.

This chapter reviews the history and development of RFID technologies. Simultaneously, performance of published topologies along with proposed RFID system architectures are discussed and evaluated. With the rapid growth in demand for RFID applications, especially for UHF RFID systems, significant research efforts have been dedicated to the fabrication of single SoC RFID receiver in the last decade. Several proposed architectures are evaluated based on their performance. Some state-of-the-art front-end designs published recently are also analysed in this chapter. Key components, such as low noise amplifiers (LNA), mixers, voltage controlled oscillators (VCO) and so on, are studied to develop a design strategy that balances gain, input impedance, linearity, isolation, sensitivity, noise performance and power consumption. This chapter concludes with research and suggests the feasibility of implementing a single Soc RFID receiver front-end operated at the ultra-high frequency (UHF) band which meets the international standards.

2.1 RFID Systems

2.1.1 History of RFID Systems

The modern systems of wireless communication are associated with several well-known names such as Maxwell, Hertz, Marconi, Lodge, Tesla, de Forest, Fessenden and so on

[1]. In terms of modern wireless systems, they not only deal with signal processing, electric field theory, and the development of circuit designs based on theory; they also deal with advance information and control theory. Radio frequency identification (RFID) wireless telecommunication development is still at its infancy. However, RFID has begun to highlight its importance in our daily life within the last decade. With the advantage of the capability of identifying more than one item simultaneously without human involvement, RFID is expected to replace barcodes.

Like any other wireless system, RFID is based on the theory of electromagnetism and radio waves developed in 19th century [2]. The concept of using radio frequencies to reflect waves from objects goes as far back as 1888 to experiments conducted by Heinrich Hertz[3]. Radar was invented in 1922 based on this concept. However, the early radar system had a fatal defect in that it could not determine the type of incoming aircraft and its origin. During World War II, Britain used the IFF (Identify Friend or Foe) system to identify friendly aircrafts but not hostile ones. Since RFID is the combination of radio broadcast technology and radar, it is not unexpected that the convergence of these two radio disciplines and the concept of RFID occurred on the heels of the development of radar. RFID technology was used for the first time within the transponders of RAF planes to differentiate alliance's aircraft from the enemy's. The debut of the new technology was a success. In the late 1960s, the U.S. Government began using RFID to tag and monitor nuclear and other hazardous materials[4].

History shows it does not take long for a new technology to spread from military into commercial applications. The first RFID card for access controls was developed in the laboratory in 1972 and had spread to the public sector in 1977. Other early major uses of RFID were in livestock identification and toll collection systems in the 1980s[4]. The success of toll collection system across the U.S. was considered as one of the major breakthroughs of RFID applications. In the mid of 1990s, Massachusetts Institute of Technology (MIT) introduced RFID technology into robotics for items recognition and response. The Auto-ID Centre[5] was co-founded at MIT in 1999 to develop the concept of using RFID as a networked technology as the Internet became the most powerful resource supplier. The Auto-ID Labs at MIT and other universities around the world continued contributing large amount of research on Electronic Product Code (EPC) technologies and proposed the Class 0 and Class 1 protocols which was later

approved by EPCglobal organization as EPC standards. In 2004, EPCglobal developed a new global standard that was more closely aligned with ISO standards, the second-generation protocol (Gen 2) [6]. Figure 2-1 shows a Class 1 Gen 1 tag with antenna using UHF 865 MHz from GAO RFID Inc[7].

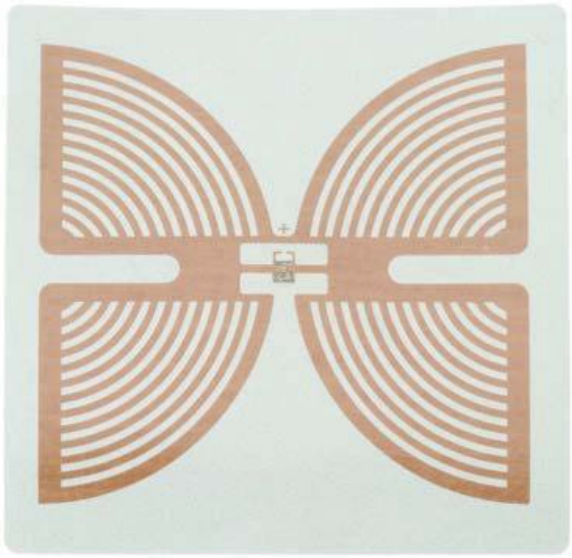


Figure 2-1: Class 1 Gen 1 tag (butterfly style) [7]

2.1.2 RFID Systems' Components

RFID systems may consist of several elements: tags, tag readers, antennas, tag programming stations, the computer network used to connect the readers, middleware and enterprise logic software [8]. As shown in Figure 2-2, a typical working scenario of RFID technology involves a reader communicating with a tag that holds digital information on a microchip. The microchip is used for storing data which can only be a unique numeric identifier (ID) or an "object". The "object" could add several attributes such as type of asset, the date of manufacture, a description of product or shipment information. Some middleware may be used to increase data accuracy and reduce noise and several software applications, such as Enterprise Resource Planning (EPR) system[9], Laboratory Information Management (LIMS) Systems[10] or Customer Relationship Management (CRM) system[11], may also be used to manage and track the data.

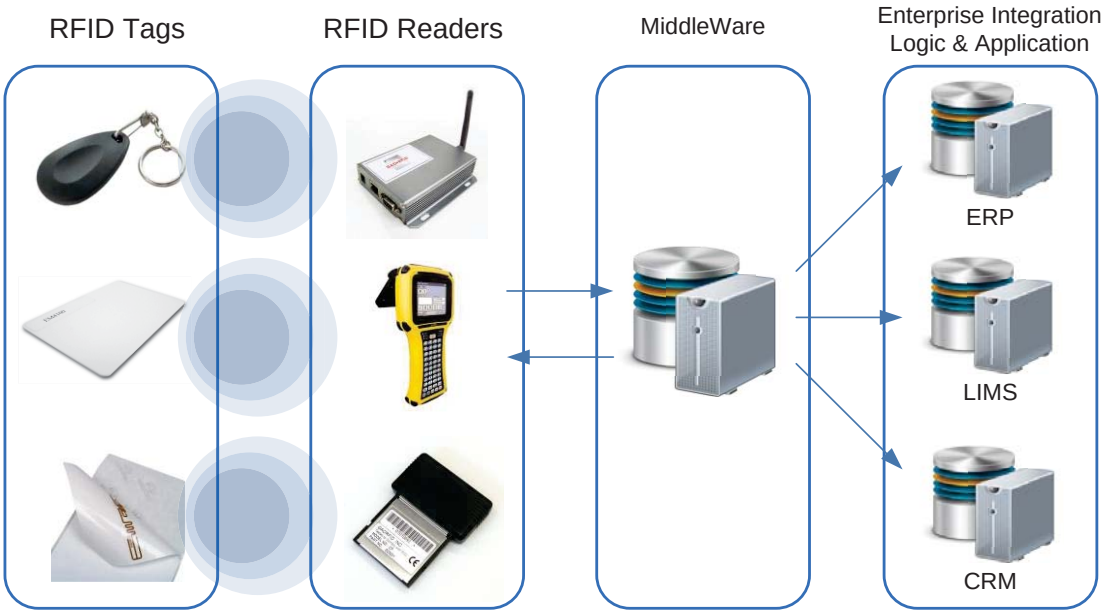


Figure 2-2: Demonstration of typical RFID systems

According to the power source, RFID tags are classified as active tag, passive tag and semi-passive tag. A tag that has a transmitter to send back information rather than reflecting a signal back from the reader is defined as an active tag. An active tag requires a battery to transmit the signal to the reader. Therefore, an active tag could operate over a range up to a few hundred meters. The shortcoming of the active tag is its cost and large power consumption. A typical application of an active tag is in tracking expensive items over longer read ranges, e.g. shipping containers, rail cars, road toll booths, and asset management applications [12].

In contrast, passive tags do not have their own power supply; rather, they rely on the reader's RF power to turn on the tag. The reader's RF signal's electromagnetic energy is converted into electricity by the passive tag's antenna, which turns on the tag's microchip and powers the tag's transmission. The microchip in the tag is powered up and able to operate and transmit the stored information. Backscatter is a method of communication between passive tags and readers by reflecting the signals from the reader at the same frequency back to it. Transferring of energy from one circuit to another via the mutual inductance between the circuits is defined as inductive coupling. In a passive RFID system, the reader antenna and the tag antenna form a magnetic field using inductive coupling which means the tag receives energy from the magnetic field

and this energy is used by the RFID microchip to supply transmitting power for the tag antenna[12].

Similar to the active tags that use battery power for generating the RFID tag's signal, semi-passive tags also utilise a battery. However, the battery only used to power the tag's microcontroller. The semi-passive tags stay in "sleep" mode until they are "woken up", or activated by a signal from the reader. The advantages of semi-passive tag include conserving battery life and increasing the reflected ratio that would directly enhance the working range[12].

Readers are defined as the devices used to communicate with RFID tags. A reader has one or more antennas which transmit radio waves and receive signals back from the tags. The reader system will be discussed in following chapters.

Antennae are either used to transmit or receive a tag or reader's signal and are designed to transform current into electromagnetic radiation, or vice versa. In RFID applications, antennae consist of two general types: inductive antennae that use magnetic coupling; and dipole antennae that use radioactively coupling [13]. Inductive antennas are commonly found in low- and high-frequency applications but are also used in ultra-high-frequency (UHF) near-field tags. Most UHF and microwave tags use variants of the dipole antennae radioactively coupled to the reader antenna, typically a patch antenna or a Yagi-Uda antenna [14, 15]. These types of antennae use a centre-fed element for transmitting or receiving radio frequency energy.

2.1.3 RFID Regulations and Standards

There are several parties involved in the development and definition of RFID technologies including International Organisation of Standardisation (ISO), EPCglobal, European Telecommunications Standards Institute (ETSI) and Federal Communications Commission (FCC). Those RFID standards were proposed to deal with the air interface protocol, data content structure, communication conformance and applications. Moreover, countries also vary the standard based on their frequency band and range.

For instance, ISO 14223/1[16] is used for animals and advanced transponders, ISO 14443 is applied as the basis of RFID-enabled passports and ISO15693 is widely employed for non-contact smart payment and credit cards. Among all standards, the most likely to undergo international standardisation is the EPCglobal[17] standardization framework.

EPCglobal is working mostly for passive RFID and the EPC in the identification of many items in the supply chain for companies worldwide. They are more likely to focus on the carrier data content of the physical object, the infrastructure performance of RFID system and the data exchange standards. In 2003, EPCglobal defined the Class 0 and Class 1 protocols for two tag air interfaces. A new protocol, the Class 1 Generation 2 interface (Gen 2), was created to overcome most problems experienced with Class 0 and Class 1 tags. The Auto-ID Centre developed and established the protocols to communicate between different classes of tags and also approved by EPCglobal. Each class of these tags changes over time, but below is what was originally proposed.

Class 1: a simple, passive, read-only backscatter tag with one-time, field-programmable non-volatile memory

Class 2: a passive backscatter tag with up to 65 KB of read-write memory

Class 3: a semi-passive backscatter tag, with up to 65 KB read-write memory essentially, a Class 2 tag with a built-in battery to support increased read range

Class 4: an active tag that uses a built-in battery to run the microchip's circuitry and to power a transmitter that broadcasts a signal to a reader

Class 5: an active RFID tag that can communicate with other Class 5 tags and/or other devices (i.e. can act as a reader)

Some standards were made regarding its technical parameters. For example, ISO 18000 is a series of ISO standards for the air interface protocol used in RFID for tracking goods in the supply chain. They cover the major frequencies used in RFID systems around the world. Thus the EPC Gen2 standard was also adopted with minor modifications as ISO 18000-6C in 2006. The ISO 18000 is listed as following:

18000–1: Generic parameters for air interfaces for globally accepted frequencies

18000–2: Air interface for below 135 KHz

18000–3: Air interface for 13.56 MHz

18000–4: Air interface for 2.45 GHz

18000–5: Air interface for 5.8 GHz

18000–6: Air interface for 860 MHz to 930 MHz

18000–7: Air interface at 433.92 MHz

2.1.4 Applications of RFID Systems

There are several frequencies in the electromagnetic spectrum, which includes audio (under 25 kHz), Infrared ($10^{12} - 10^{14}$Hz), visible light ($10^{14} - 10^{15}$ Hz), and x-rays ($10^{15} - 10^{22}$ Hz) frequencies. Radio frequencies are also within the electromagnetic spectrum operated from 3 kHz to 300 GHz, as shown in Figure 2-3. With respect to RFID, LF tags operate at 125 kHz or 134 kHz, HF tags typically operate at 13.56 MHz, and UHF tags operate at 433 MHz and 860 - 960MHz. The frequency categories and passive RFID system frequencies' characteristics are tabulated in Table 2-1.

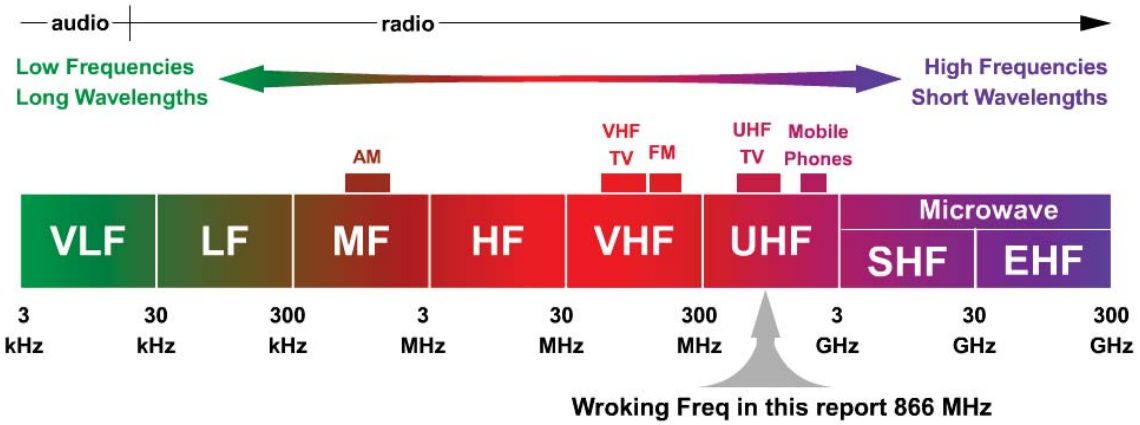


Figure 2-3: Radio spectrum divided by ranges of frequencies[18, 19]

Table 2-1: (Passive) RFID Frequency Bands and Characteristics

Frequency Band	Typical RFID Frequencies	Coupling Meth.	Communication Range	Data Rate	Maturity	Reader Cost
LF	125–135 kHz	Inductive	< 0.3 m	<1kbit/s	Very Mature	Low
HF	13.56 MHz	Inductive	< 1.2 m	≈25 kbit/s	Established	Medium
UHF	433 MHz or 860–956 MHz	Backscatter	< 100 m < 10m	≈30 kbit/s	New	High
Microwave	2.45 GHz	Backscatter	<10m	≈100 kbit/s	In Development	Very High
	5.8 GHz	Backscatter	<10m	<100 kbit/s	Future Development	Very High

According to their working frequency and distance range, RFID system can be used for automatic toll collection, personal and vehicle access control, library management, security, equipment and storage tracking, payment and other retail out outlet and a wide range of other applications[4, 12].

Even within a frequency band, the communication range varies widely depending on antenna design, system power, transponder power consumption and receiver (RX) sensitivity. Among all these parameters, range, memory size and security features, have been considered as the three selection keys to RFID applications [20]. Especially, the UHF RFID systems are gaining worldwide momentum due to its longer read distance (up to 10 m), larger information storage and faster data rate up to 640 kbps [21, 22]. On the other hand, the higher operating frequency scales down the size of antennae, which is beneficial for high integration. Some of the generally RFID applications are listed below:

Product tracking:	Library book tracking from 2004 [4]
Inventory systems:	The suppliers of Walt-Mart Limited is required to apply RFID label in 2006 [23]
Passports:	New E-passport of US is officially issued from Feb 2008
Transportation Payment:	Calypso international standard are used globally for toll-road system and parking system [24]
Automotive:	Car keys and parts since 1990
Animal identification:	Livestock tracking [4]

Human implants:	Implants for interacting with robotics and paying system in 1998 [25]
Remote sensor:	Broadcast telemetry back to a base station inducing sensing of road conditions by implanted beacons, weather reports and noise level monitoring
Precise locationing:	Wirama[26] has used Gen2 passive RFID by retailers to quickly obtain precise, shelf-level location information about their inventory

2.2 Receiver Architecture Analysis

2.2.1 Receiver Architecture Analysis in RF systems

Since the RFID receiver front-end design is the main research goal of this thesis, a brief overview of existing RF receiver architecture is carried out here. The suitability of a particular receiver topology relies on many parameters. Jeffery [27] summarized following key characteristics:

Sensitivity	defines the weakest signal level that a receiver can detect and is usually determined by the various noise sources in the receiver.
Selectivity	represents the ability of the receiver to detect the desired signal and reject all others.
Stability	indicates the lack of change in the receiver gain and operating frequency with temperature, time, voltage, etc.
Dynamic range	is the difference in power between the weakest signal that the receiver can detect and the strongest signal that can be supported (either in-band or out-of- band) on the receiver without detrimental effects.
Spurious response	is a receiver's freedom from interference due to internally generated spurious signals or to their interaction with external signals.

Starting from the simplest topology, the single conversion receiver topologies (see Figure 2-4 (a) and (b)) are used in low-power applications due to only a single mixing stage is needed to convert the signal to baseband (or near baseband) and are classified as either direct conversion, homodyne, or zero-IF receivers. Since mixers utilise the largest proportion of the receivers' power, architectures with only one conversion stage offer good power consumption with respect to the entire receiver. As seen in Figure 2-4 (b), the in-phase/quadrature (I/Q) down-conversion with frequency-modulation is used to avoid the overlap between the upper and lower sidebands, which contain different information. Hence, this I/Q structure is well employed in many recent RF receiver front-ends [28-30].

In the case of homodyne Receiver, the LPF after the mixer is an active filter rather than passive LC filter, as the passive component tend to be extremely large at baseband frequency. The drawbacks of an active filter include increased noise, increased power dissipation, and worse linearity. Furthermore, since down-converted baseband extends to the DC level, extraneous offset voltages can also corrupt and saturate following stages.

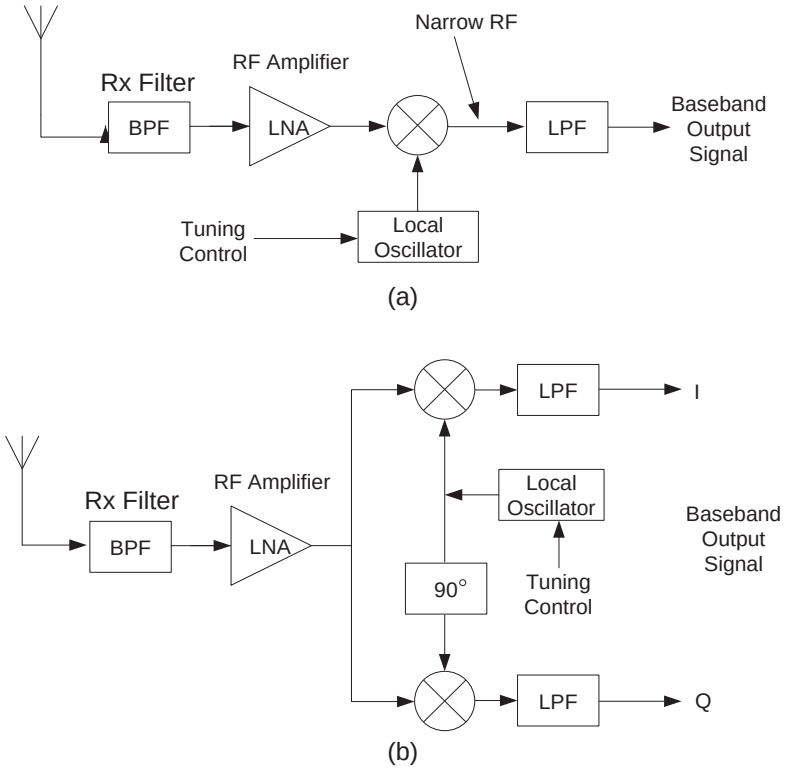


Figure 2-4: (a) Typical Single-conversion receiver with binary phase-shift keying (BFSK) and amplitude modulation (AM) and (b) single-conversion receiver with frequency modulation (FM) and phase modulation (PM) [31]

The LO leakage can cause the mixer to down-convert a received version of itself (known as self-mixing), which results in a large DC bias at the mixer output. High port-to-port isolation between the LO and input to the mixer or other components is very important but difficult to achieve. A non-ideal I and Q down-conversion may result in a warping of the received RF signal constellation diagram for a quadrature phase-shift keying (QPSK) signal, as shown in Figure 2-5. I and Q mismatch in quadrature mixing can be caused by either self-mixing DC bias in I and Q output or any gain and phase error from LO. Figure 2-5 demonstrates several non-idea mixing processes that seriously impact the phase constellation diagram.

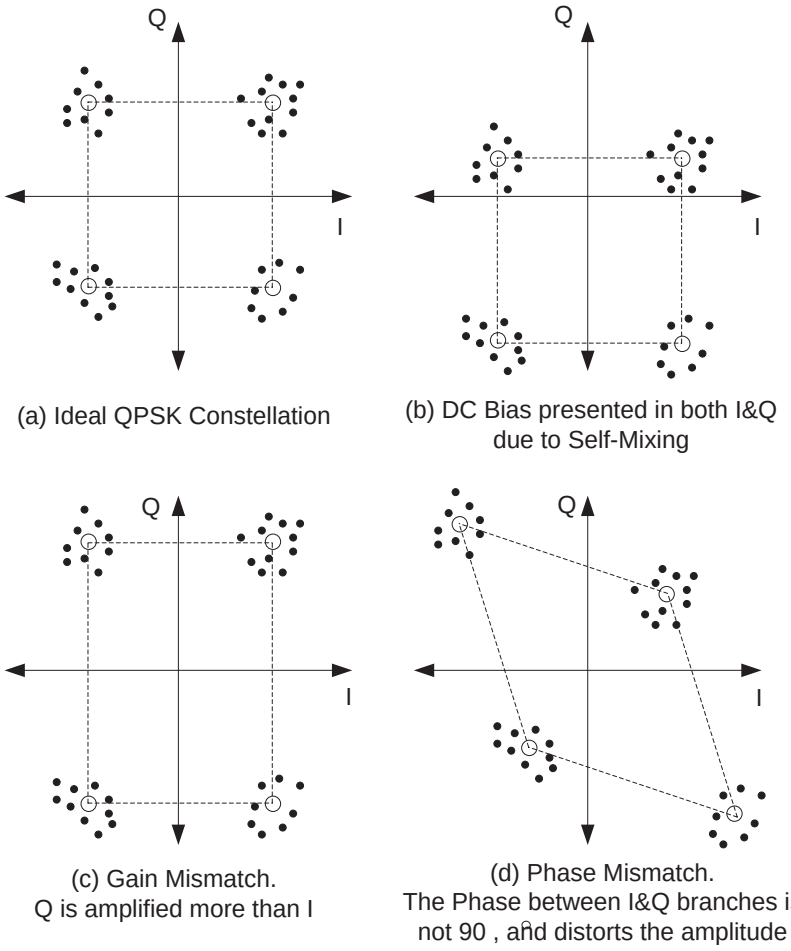


Figure 2-5:Impact on constellation due to non-ideal mixing process[27]

Furthermore, at the mixer stage, not only the signal is down-converted, but also a portion of the image signal (ω_{IM}) is down-converted, which will overlap on the top of the desired translated signal. This effect is demonstrated in Figure 2-6. The typical

drawback for this is not only the additional undesired signal but also the extra image noise (3dB more if they are equal).

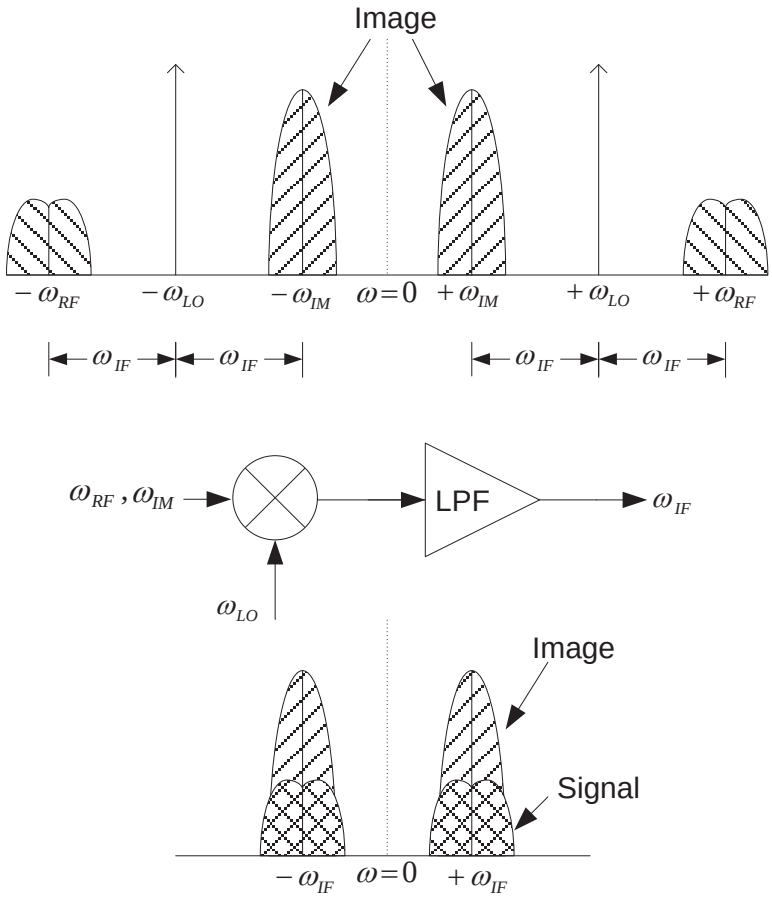


Figure 2-6: Problem of image in the heterodyne receiver.

One solution of avoiding image overlap is to apply an image reject filter (IRF) after the LNA[32]. The block diagram of this technique is illustrated in Figure 2-7. A well selected ω_{IF} can provide substantial rejection of image signal (ω_{IM}). However, a high Q IRF is required if the ω_{IF} is large, resulting to a larger loss with the filter. Therefore, it is important that IRF filter loss should not exceed a certain limit (a typical LNA provide a gain of approximate 10-16 dB) and finding the balance of the trade-off between image rejection effect and signal value level of IF. Moreover, a channel selection filter (CSF) stage may be used after mixer to avoid any unexpected interfere signal (ω_{INT}). With a large ω_{IF}, the Q value of CSF must be also larger enough to cause substantial suppression of ω_{INT} and this could be difficult to approach. Furthermore, the secondary harmonics of mixer input signal ($(\omega_{RF}+\omega_{LO})/2$) and ω_{LO} will create two possible signal expected ω_{IF} and an unexpected half-IF inference signal$\omega_{IF}/2$.

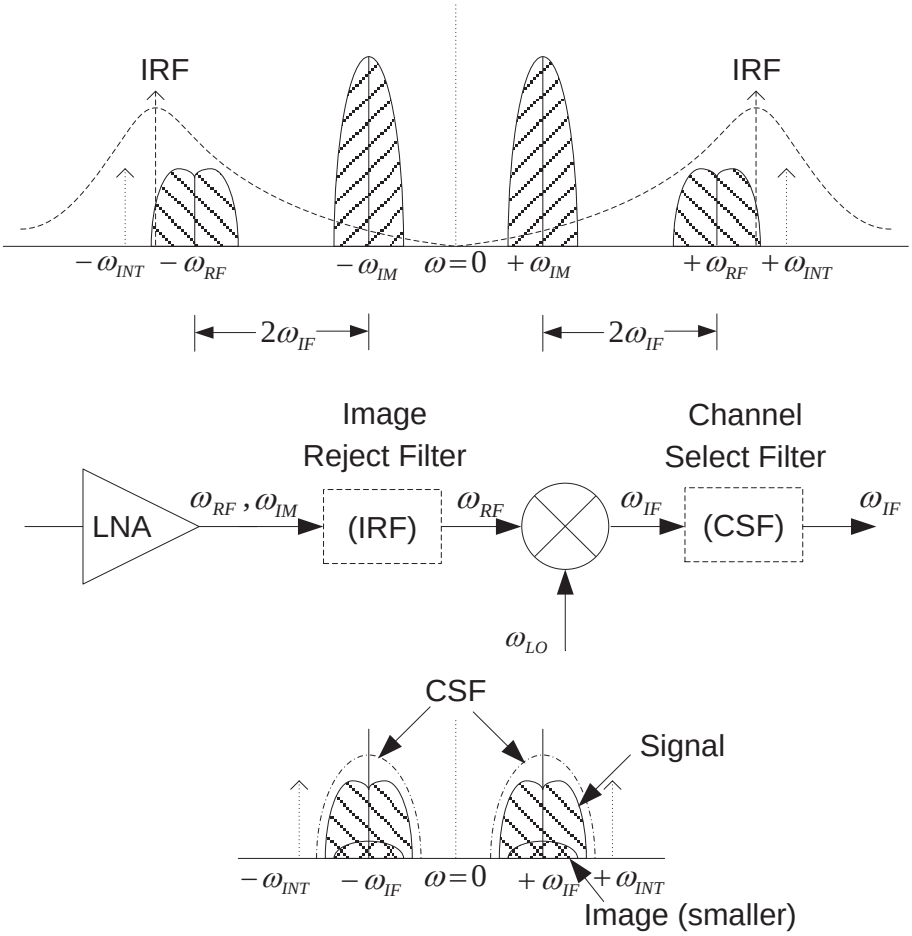


Figure 2-7: Image reject filter and channel select filter applied in RF front-ends [32]

In some cases, it may be more convenient to down-convert the signal to some lower intermediate frequency instead of directly to baseband. The heterodyne receiver topology is based on this principle and dominates most RF analogue front-end applications [33]. The heterodyne receiver works by shifting the incoming signal frequency to an IF that is fixed and independent of the desired signal's centre frequency.

Rather than employing the heterodyne principle to demodulate defined signal directly, Armstrong [34] proposed converting the incoming high-frequency RF signal into one at a lower frequency, where high gain and selectivity could be obtained with relative ease. This signal, known as the IF, was then demodulated after filtering and amplification in order to possess enough sensitivity comparing with the atmospheric noise in the Amplitude modulation (AM) broadcast band. This topology is known as "superheterodyne", as shown in Figure 2-8. It has been refined continuously in the following decades to employ in almost every modern receiver, ranging from portable

radios to radar sets. Since it requires two stages of signal mixing, it is also called dual-conversion superheterodyne receiver (or dual-IF receiver). This topology shown in Figure 2-8 employs two stages of down-conversion that offers relaxed filtering requirements compared to a single-conversion receiver, which improves the filter quality factor (since the centre frequency of the signal is lower after the first stage of down-conversion) and as a result it reduces the ratio of centre frequency to filter bandwidth. However, the additional mixer and LO results in higher power consumption, extra circuit size occupation, and increased costs due to the second filter, which may exist off-chip due to its lower operating frequency occasionally.

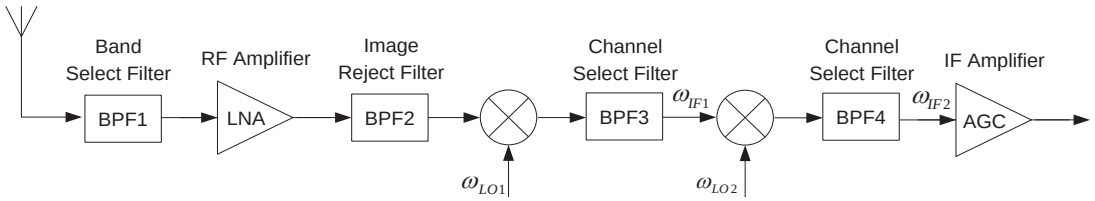


Figure 2-8: Superheterodyne (Dual-IF) receiver's topology

Another image rejection method utilizes a single-side band (SSB) from IF frequency converting. This approach is implemented by in-phase / quadrature-phase (I/Q) down-conversion, such as the Hartley or Weaver mixing process. The Hartley modulation provides a SSB signal with phasing to suppress the unwanted sideband as illustrated in Figure 2-9 (a). Two original RF signals, mutually 90° out of phase are generated and further modulated and separated with carrier frequency LO that are also 90° I/Q out of phase with each other. A lower or upper sideband signal representing the image signal and desired signal is achieved in either adding or subtracting the signals. However, large range of frequencies shifting is sometimes difficult to achieve. Another variation, the Weaver modulation [35] uses only LPF and quadrature mixers, as shown in Figure 2-9 (b). In Weaver's method, the interested RF band is first translated into the zero baseband, conceptually by modulating a complex exponential $\exp(j\omega t)$ with frequency. This signal is modulated with quadrature mixer stage and further filtered by LPF to remove the undesired sideband that is not centred at zero. This SSB complex signal is later on up-converted to the real desired signal frequency band by another pair of quadrature mixers. However, the requirement of two stages of mixers and filters will also result in larger power consumption.

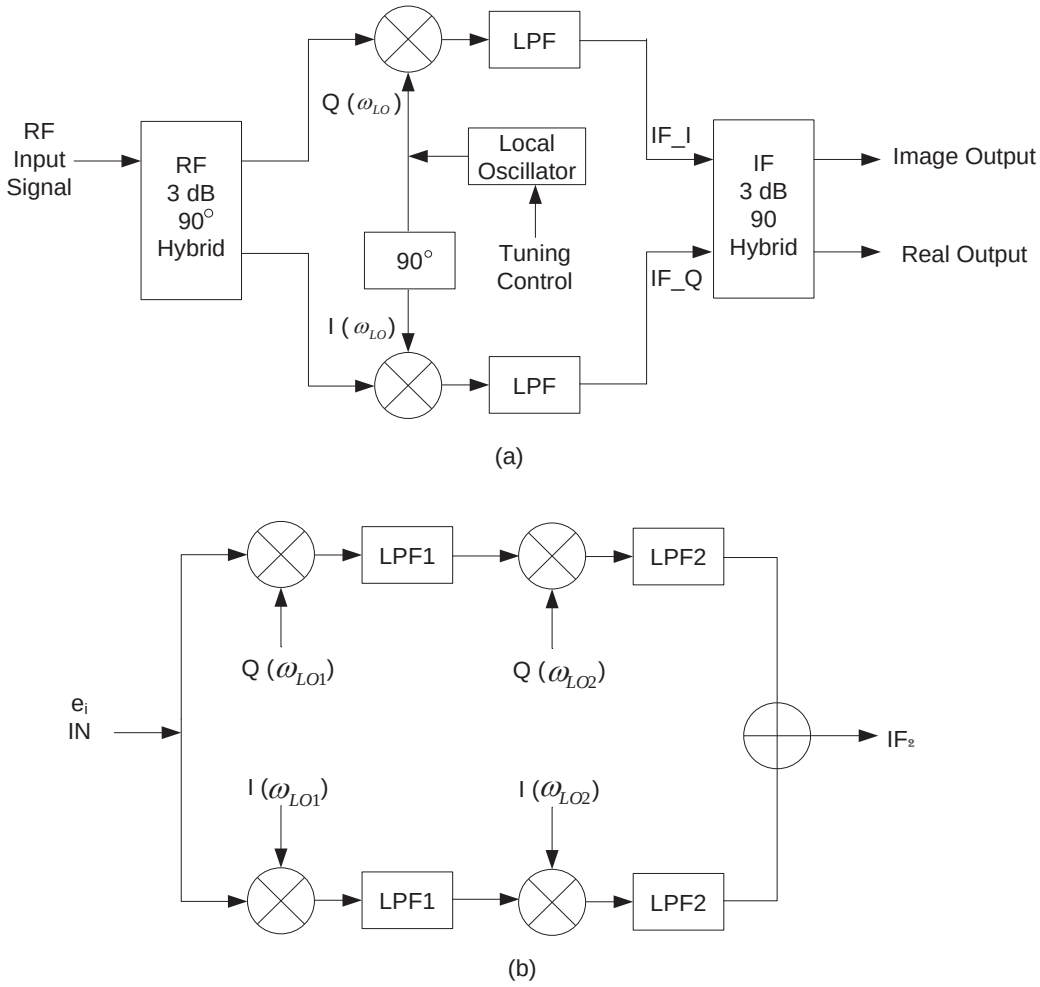


Figure 2-9: (a) Hartley modulation and (b) Weaver modulation architectures

A mixer with image rejection ratio around 20 dB is considered a good design since the noise figure contribution of the image frequency is below 0.1 dB[36]; however, the high rejection always accompanies a trade-off between phase or gain imbalance.

The simpler the RF chain, the more predictable its response will be after retuning of the signal. The choice of a single or double conversion receiver depends on a number of factors including channel spacing, frequency plan, spurious response and total gain. In general, the smaller the channel spacing, the more attractive the double conversion receiver becomes because of its ability to narrowly filter the desired signal. These above topologies can also be adopted in RFID receiver design since they are achieving the same purpose.

2.2.2 System Architecture for RFID Receiver Front-End

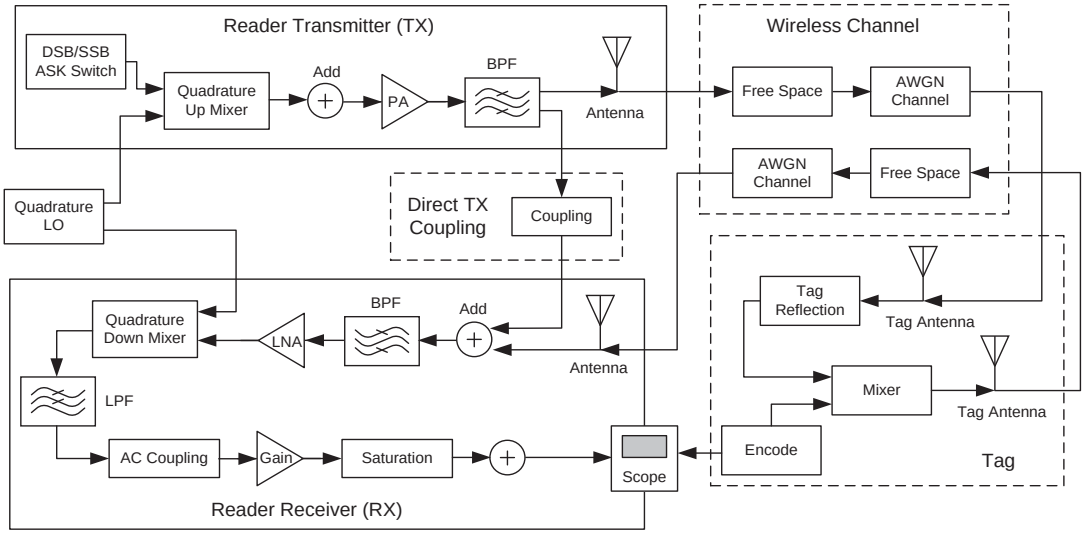


Figure 2-10: The simulation environment of return link (Reader, Wireless channel and Tag) [37]

A simulation environment of complete return link of RFID reader, including the wireless channel and the tag, is illustrated in Figure 2-10. The transmitter sends a continuous carrier to power up the tag. The free space pass-loss is modelled for the distance between reader, tag and the noise source models in an AWGN channel. Another source of receiving power is the direct coupling from TX to RX. It is modelled by a proper gain and phase delay. The tag is modelled by coding method, antenna gain and percent of reflection by using the backscatter method. The receiver arm includes BPF, LNA, Mixer, AC coupling, channel select filter and the variable gain stage. The working procedures of the receiver are opposite to the transmitter. The completed simulation results can be presented by using different modulation and encoding types in transmitter from Jin and Cheng's paper[37].

In terms of practical implementation, a single-chip reader is feasible for UHF RFID since the higher operating frequency results in a smaller size of antennas and passive components. Among various solutions, the standard CMOS technology and the direct-conversion architecture are popular methods represented in reduced cost, low power consumption, and improved the level of integration. In passive UHF RFID system the

design is much more challenging. Tags are expected to be as "simple" as possible and its operating power is limited. These requirements will lead to increase in design complexity and performance of the receiver.

In passive UHF RFID system, the tags are powered from the reader. If the tag is the corresponding one, the communication link between the reader and the tag will be established. Then the reader sends the DSB/SSB/PR-ASK modulated signal to command the tag and subsequently transmits the continuous-wave (CW) signal to ensure the tag remains energised.

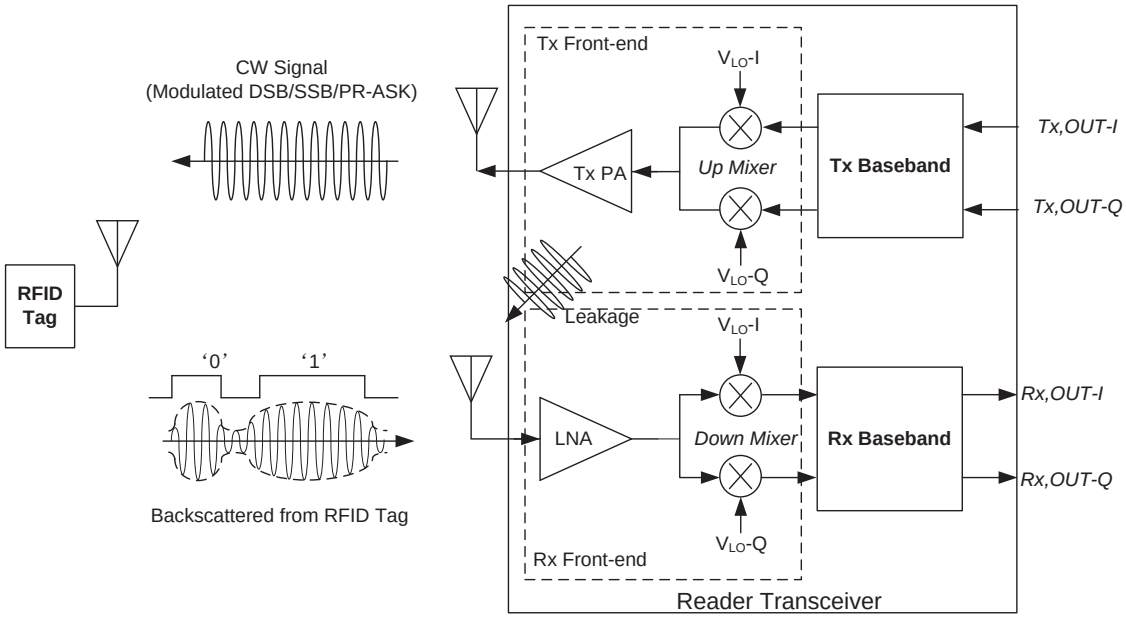


Figure 2-11: The front-end block of a typical RFID Reader[12]

However, limited isolation between transmitter (Tx) and receiver (Rx) can cause a leaking problem. Leaked signal from a transmitter can saturate the receiver, hence inducing severe noise performance degradation or even blocking the expected signal from the tags. In general, this DC leakage signal (self-jammer) from transmitter is much larger (over 10dBm) than the wanted signal from tags (down to -80dBm) [38]. Therefore, the RF front-end of the reader needs to have extremely high linearity to handle the carrier leakage problem and the trade-off between linearity and noise figure becomes the greatest challenge for RFID reader receiver.

Several methods have been proposed to remove the DC leakage [39-42]. A self-jammer cancellation circuit with off-chip capacitors is employed in [39] to remove the DC leakage. It achieves sufficient linearity and good sensitivity in the presence of large leakages. However, it is based on the SiGe BiCMOS and requires a 5 V supply voltage. The use of off-chip capacitors to handle the DC leakage results in large power consumption up to 1.5 W. However, the fully differential I/Q receiver structure requires four off-chip capacitors and eight pins in the package.

Another scheme, reported in [40], used a front-end structure that consists of a passive mixer without LNA to achieve high linearity. However, the NF and receiver sensitivity, as functions of time, deteriorated significantly. In contrast, a LNA was partially employed in [43] to prevent the demodulator from saturation during listen-before-talk (LBT) mode, with a trade-off of degrading the receiver sensitivity and the dynamic range of the receiver. In [44, 45], on-chip intelligent canceller (carrier suppression) is used to counteract the leakage carrier from Tx to Rx but at the cost of larger size and additional calibration control[42].

Recently, on-chip DC offset correction circuits (DCOC) have gained popularity due to their linearity and sensitivity without removing the LNA[38, 43]. This kind of architecture consists of an LNA, a passive down-conversion mixer, a baseband programmable gain amplifier (PGA) and a few low pass filters (LPF). Direct conversion (Zero-IF) architecture is selected to overcome the carrier leakage problem. Since the LO frequency equals to RF input carrier frequency, the received signals are mixed down to the baseband and the carrier leakage components is converted to DC that can be removed by AC-coupling. The passive mixers are commonly chosen to offer higher linearity to avoid the in-band blocker from carrier leakage. In the baseband, quadrature I/Q paths cooperate with four PGA to provide a wide gain control range. The baseband low pass filter is an active-RC filter with a programmable 3-dB bandwidth from 100 kHz to 1.6 MHz depending on the different Rx data rate. However, the settling time of the on-chip DCOC circuit might become longer when the DC leakage is larger. In [38], an on-chip SC circuit was proposed with quickly time-varying cut-off frequency and on-chip DCOC circuit to kill the DC leakage. However, like any other direct-conversion receivers, the baseband analogue modules are still susceptible to the DC offset, especially in CMOS technology.

In addition, the I/Q direct-conversion Rx structure is preferred to eliminate the zero-effect in terms of UHF RFID applications for different phase delay from variable operation distance [46]. The limited LO phase noise performance would significantly exacerbate Rx input noise floor and the transmit-to-receiver turnaround time.

Therefore, in this thesis, an active highly linear RF front-end is designed to provide good trade-offs between power consumption, linearity, noise and sensitivity for achieving optimal performance.

2.3 Low Noise Amplifiers Design

Being the first block in the receiver front-end chain, the LNA plays a significant role in overall NF of the receiver that determines the system sensitivity and bit-error rate. Various kinds of LNAs are available for different applications, such as narrow band, multiple bands and wide-band LNAs.

For a single-band amplifier, a cascode common-source (CS) with inductive degeneration amplifier topology is mostly used in narrow band LNA design [47-51]. Apart from the advantage of good isolation between ports, the inductive degeneration part is used to generate the real part to match the LNA input to the preceding antenna or filter, as shown in Figure 2-12 (a). By choosing appropriate L_s, this real term can be made equal to 50 Ω. However, the downside of inductive degeneration technique is that L_s will degrade NF with shunt-input resistor. The cascode configuration can be used to enhance the stability and reverse-isolation of the amplifier. The conventional common-gate (CG) LNA is also adopted in LNA design due to its inherent wideband operating performance, good linearity and good I/O isolation property[52]. However, the parasitic components of the transistor in CG LNA will result in higher noise figure and higher power consumption problems that will require sophisticated input matching network and extra noise figure cancellation techniques [53-55].

In order to operate the LNA at low-power implementations, one extra capacitor C_{ex} is employed, as shown in Figure 2-12 (b). This additional capacitor, in parallel with transistor gate-drain capacitor C_{gs}, reduces the inductive degeneration term. This approach is defined as the power constrained simultaneous noise and input matching (PCSNIM) technique [56], which is used in most of modern LNA designs. At the same time, turning the topology into folded-cascode structure can further reduce the power consumption[57]; however, the trade off is the degradation of power gain and linearity.

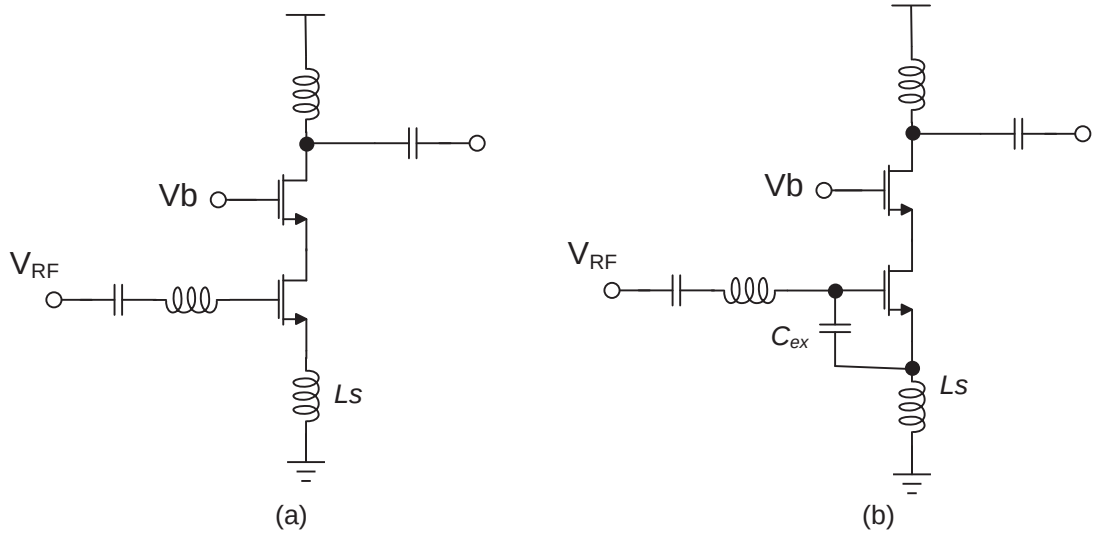


Figure 2-12: (a) CS with inductive degeneration (b) PCSNIM technique with additional capacitor C_{ex}

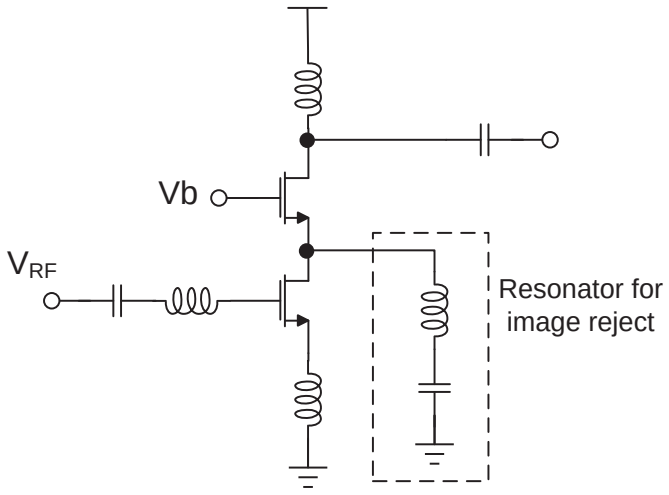


Figure 2-13: Schematic circuit of an Image-reject LNA

One of the issues related to a super-heterodyne receiver is its image signal. Although an image-reject mixer can be implemented for image rejection, practical systems require higher amounts of image rejection in each stage. Instead of applying an image-reject filter stage after the LNA stage in a super-heterodyne receiver, an LNA with notch filter structure is implemented, as shown in Figure 2-13[58, 59]. In order to have the ability of filtering images at the right frequency, a varactor is usually used in parallel to the inductor. However, this design requires extra inductors and occupies larger die area or even requires off-chip components as the image can appear at much lower frequency.

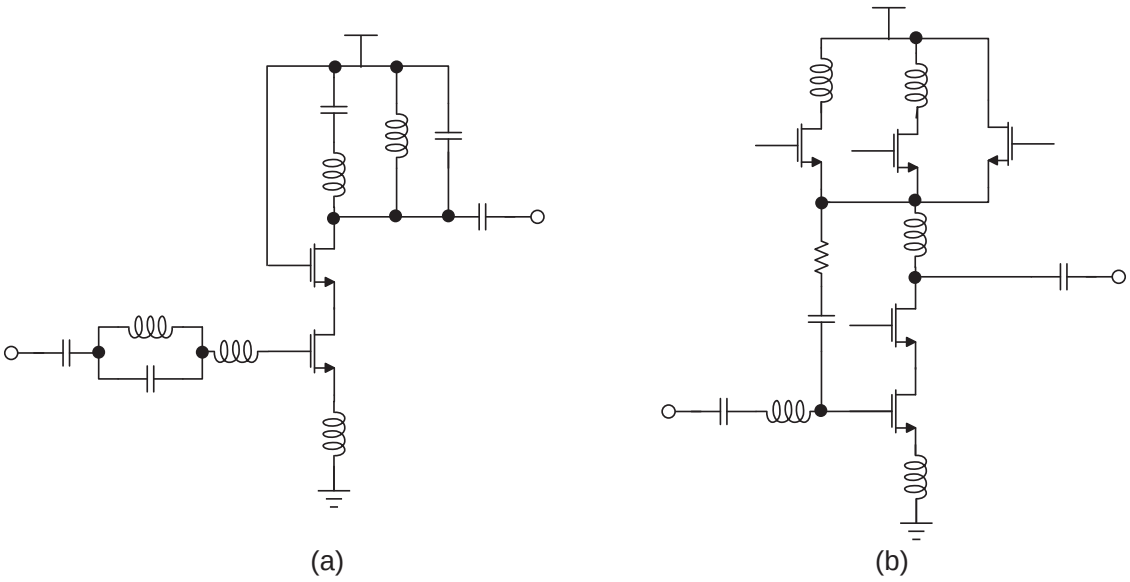


Figure 2-14: Multi-band circuit architecture with (a) concurrent input tuning matching and (b) Feedback loop by selectable outputs loads

With the increasing number of wireless standards, the need for multi-standard transceivers also increases. Therefore, in the future, a wireless transceiver chip, especially in RFID, must cover several bands under different ISO standards, or even ultra-wide band (UWB), which has come under intense attention recently since higher bandwidth means the higher data rate. Conventional ways of designing dual band LNA rely on the input matching networks that can be tuned at more than one resonant frequency [60-64], as shown in Figure 2-14 (a). Such a structure can be implemented based on the Bipolar CMOS SiGe technologies for higher frequencies [65]. Although switching between bands improves a transceiver's versatility, it still has its limitation when more than one band needs to be received simultaneously.

Recently, feedback loops (see Figure 2-14(b)) have been used in multi-band applications [30, 63, 66-69]. The feedback loop's gain varies with output transistor as it switches between different output loads. Shunt positive feedback loop provides enhanced current gain to improve noise figure and variable gain and tuneable load are used to meet the different standards. There are some designs [70] that combine common-source and common-gate amplifier for both narrow band and wide band applications. However, this structure requires complicated switchable input and output matching networks that are not very feasible for practical applications.

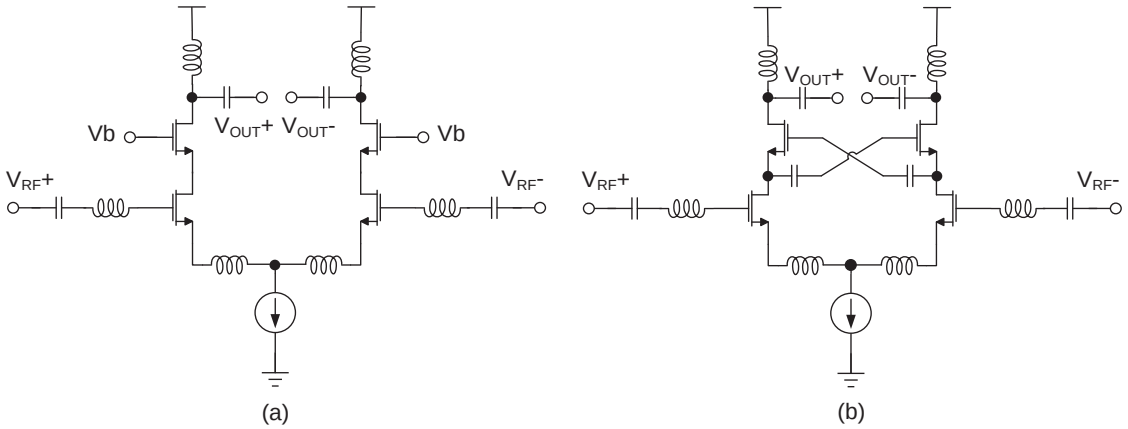


Figure 2-15: (a) Conventional CSCG differential LNA topology (b) CSCG differential LNA with capacitive cross-coupling technique

Differential circuits are an important part of integrated circuit design because they offer several important advantages over single-ended circuits. First, a differential LNA offers a stable reference point in contrast to a single-ended LNA. A single-ended LNA treats the on-chip ground as its reference point, which may not be very reliable due to the presence of parasitic resistance and capacitance. In practice, the parasitic components could be unpredictable due to the packaging, temperature and production process variations. With a differential LNA, in contrast to a single-ended LNA, the measured results of one half-circuit are always taken with respect to the other half-circuit. This minimises the chance of getting unexpected results. Another significant and relevant benefit of using a differential circuit is noise reduction. Provided the noise source at the input of the amplifier is distributed equally between two signal paths, the noise will not be amplified by the same gain factor as the input signals. Figure 2-15 (a) demonstrates a conventional differential LNA topology. The capacitive cross-coupling technique used

in Figure 2-15 (b) for CG stage can partially cancel the noise contribution of the CG transistor at the output [53, 71]. Additional inductors can be added at the drain of the CS transistor to cancel the effect of the parasitic capacitance, thus improving the noise and linearity performance at the cost of larger area for the extra on-chip inductors [59, 72]. Furthermore, differential amplifier also improves the linearity of the amplifier.

In terms of RFID LNA design, meeting the standard frequency band is a critical requirement. There are considerable researches into CMOS LNA design at 900 MHz [73-76]. The 866 MHz for ISO 18000–6c is employed for UHF RFID in Europe, Africa and New Zealand. Low power dissipation (at the lowest possible supply voltage) is a RFID hand-held reader design criterion, synthesised by trade-offs between gains, NF, input / out impedance matching and high linearity. Voltage supply under 1 V for RFID has not been reported so far. In the following chapter, the discussion of the complete design and optimization of a low-power 866 MHz CMOS CSCG cascode LNA using an enhanced PCSNIM technique is carried out. Unlike most previous optimization techniques, the effect of finite output conductance (g_{ds}) has been included in this design and analysis, which results in additional performance improvements. At deep nanometric device geometries, g_{ds} becomes reasonably comparable to the device trans-conductance (g_m), particularly for low-power LNA designs. Hence, the analysis for classical design techniques needs re-evaluation and this has been carried out in the upcoming chapters.

2.4 Baluns / Phase Splitters Design

Baluns (or phase splitters) are fundamental components required in microwave designs, converting between unbalanced (single-ended) and balanced (differential) signals. The signal generated in each line has identical amplitude but with 180° phase difference. In RFIC baluns design, they can be either passive or active. Mostly, baluns are designed for the goals of better isolation, impedance matching, balanced / unbalanced transformation and lower noise interaction in between the ports [77].

Passive balun can be formed by wire-wound transformer, lumped elements or microstrip transmission lines. Classical wire-wound transformer (or centre-tapped secondary winding) are available, covering frequencies from a few kHz to beyond 2GHz[78]. However, comparing with the printed or lumped element baluns, wire-would transformers are more expensive for industrial applications. Lumped elements baluns are based on the insertion phase, where a low pass filter lags the insertion phase through a high pass filter, and is ideal for narrow band designs. A simple example of an L-C lumped balun is shown in Figure 2-16. In order to overcome the cost and productivity disadvantage of using discreet lumped balun, a RF integrated passive device (IPD) is expected to be used due to its improvements in linearity and noise performance [79]. It is expected that RF IPD use will become the trend for SIP and SOC design. However, the "inductors overcommitted" in the design network still occupy large on chip space comparing with most of the active baluns.

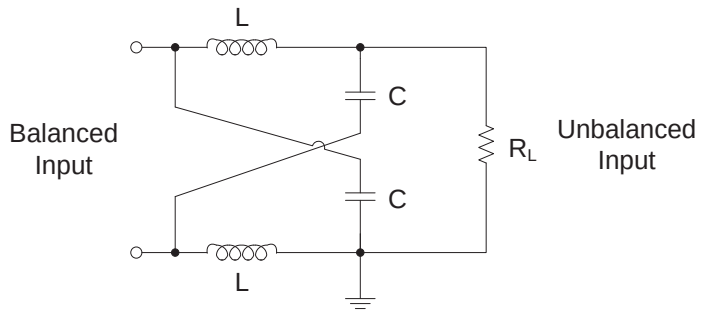


Figure 2-16: Schematic diagram of an L-C lumped balun.

Another type of popular passive balun is designed by microstrip lines, which has the advantage of being inexpensive, as they are on the printed circuit board (PCB) or microwave integrated circuit (MIC) substrate. The simplest structure is the coupled line (or parallel-line) balun [80] as shown in Figure 2-17(a). In order to increase the bandwidths over few hundred hertz, a more practical approach is to use multiple coupled lines as shown in Figure 2-17 (b) or to adopt a broad-side (or parallel plate) coupler topology, as shown in Figure 2-17 (c). An improvement on the parallel-line balun is a printed version of the "Marchand Balun" [81], which is derived from the co-axial balun, as shown in Figure 2-17 (d). Furthermore, this is more tolerant to low even mode impedance (low coupling ratio) than the parallel line balun and has a wider bandwidth. As with the parallel line balun, improved performance is obtained if

multiple planar sections are used or if a broadside coupling topology is adopted [82, 83]. On the other hand, adding extra tapping of the balanced resonator of the baluns can minimise the size [84]. However, the biggest drawback of using these printed baluns at lower RF frequencies is their large size. As with the parallel line and Marchand baluns, the use of broadside, rather than edge coupling, will yield tighter coupling and improved performance.

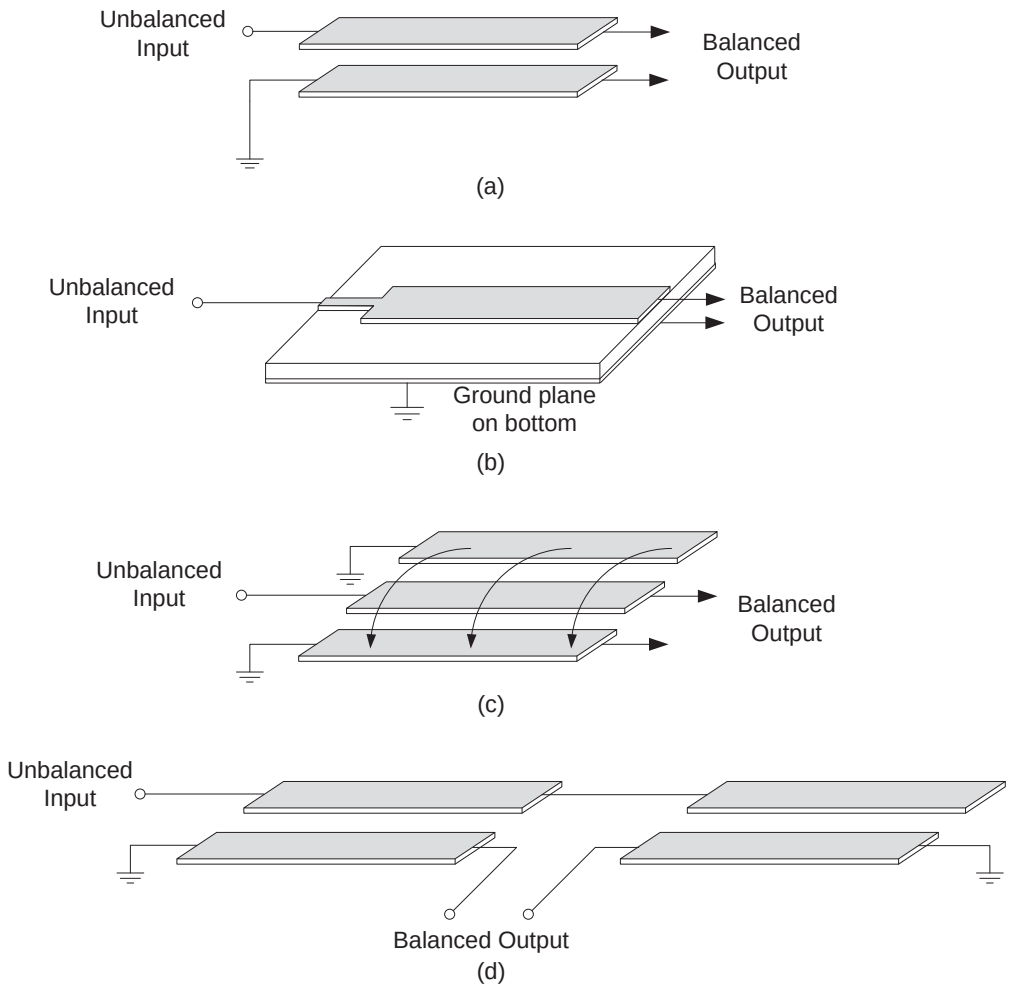


Figure 2-17: (a) Simple coupled line balun, (b) multiple coupled lines balun, (c) broadside coupler lines balun and (d) Marchand balun

Even though printed and lumped baluns can work reasonably well in a wide range of frequencies, the cost for lumped components and microstrip lines in RFIC is still too expensive (due to their larger physical size at lower frequencies). Moreover, most external baluns also increase extra gain and cause noise figure degeneration. In terms of active balun, there are three main topologies normally employed in lower microwave

frequencies: single FET circuits, common-gate common-source (CGCS) circuits and differential amplifier circuits, as shown in Figure 2-18.

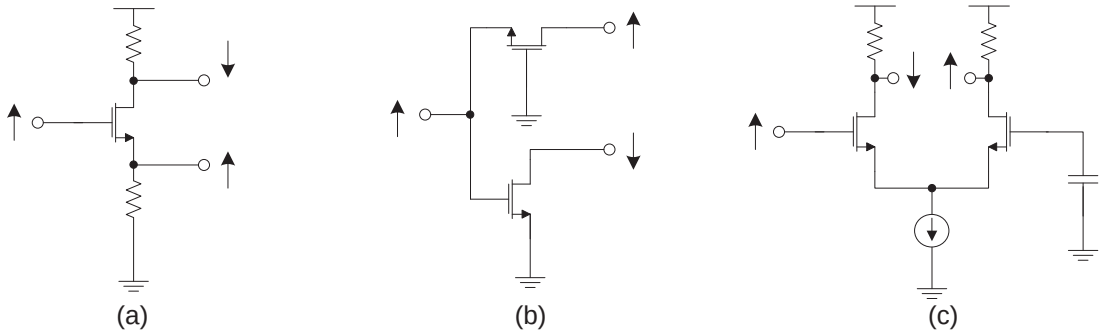


Figure 2-18: Active balun topologies: (a) single FET (b) CGCS (c) differential amplifier

In common-source single FET baluns, the output signals at the drain and source will be out of phase by 180° and have equal amplitude as the signals enter the gate. However, the parasitic capacitance of the FET makes it difficult for the common-source FET to achieve the required phase difference for wideband and high-frequency application [85]. In order to work beyond 1 GHz, a sophisticated imbalance cancellation technique, by cross-connecting the outputs from basic single FET stage, can be used to improve the performance[86]. However, the trade-off is the increase in circuit complexity, die area and DC current. The CGCS topology focuses more on low power consumption and adequate isolation. However, it does not have low phase error performance in broadband applications due to the parasitic effects. Therefore, in order to provide equal amplitudes split with 180° phase difference, the correct AC coupling capacitance and bypass capacitance are imperative [87, 88]. One additional common-gate FETs can be connected in series to the CGCS structure, under certain conditions to improve the broadband characteristics [89].

Differential amplifier topology is the most commonly balun topology due to its capability of providing high gain and consists of a differential stage with one of the two inputs grounded [77, 90-95]. However, the leakage signal to the current source will cause phase and gain imbalances. In addition, the over-driven voltage of the differential amplifier will also decrease the headroom of the output signals. Hence, the output amplitude difference can be 2dB or the phase difference can be poorer than 174°, within

a frequency range from dc to 6 GHz [77]. The active current source can be replaced by an inductor to increase the impedance at high frequencies for narrow band applications; however, this topology is not suitable for RF communication applications where the frequencies are below 2GHz because extremely large on-chip spiral inductors will be required. In many cases for a wider frequency range, a large biasing resistor is used to keep the output signals balanced. However, it creates a large voltage drop at high current. At a high frequency, when a large biasing transistor is needed for high current and high linearity, the parasitic capacitance will reduce the current source impedance and affect the output signal balance. A parallel LC band stop resonator can be inserted between source and current source to increase the impedance looking into current source at resonant frequency without creating additional DC voltage drop [91, 92]. Besides improving the virtual ground, it also isolates the common mode noise from the circuit operation. The output signals tend to be unbalanced due to the impedance attenuated at high frequency. There exist few compensation methods to overcome this unbalanced frequency issue [77, 90].

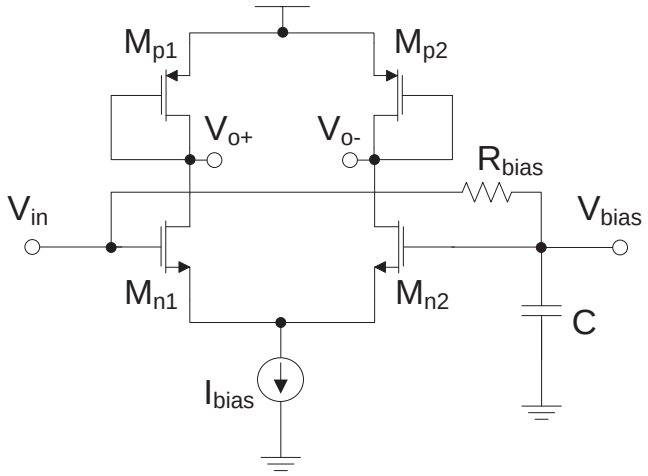


Figure 2-19: Simplified improved balun topology using second CS stage and output RC compensation circuit.

A second CS pair stage [96, 97] can alternatively be utilised to enhance the high frequency common-mode rejection ratio (CMRR) that is defined as the ratio between differential-mode gain and common-mode gain. Although the operating frequency is improved to cover 0.2 - 20GHz, the drawback of the design is the large power consumption of up to 166mW. A better solution is proposed in [98], where introducing

a common-mode resistor improves the amplitude balance and phase error up to 24 GHz with a power consumption of 10mA. Furthermore, a capacitor/RC network is usually used in the phase compensation to keep a phase margin, as shown in Figure 2-19. A phase compensator subtracts out an amount of phase shift from a signal that is equal to the amount of phase shift added by switching one or more additional amplifier stages into the amplification signal path. Unfortunately, the RC network heavily reduces the input impedance of the circuit and affects the output swing if the gate voltage of the common gate stage is not a perfect ground. This is difficult to overcome due to the bond-wire and bond pad parasitic capacitor.

In considering the compromises between electrical specifications, robustness, portability, autonomy and importantly, ease of mass production, size and costs in complete receiver design, a monolithic active balun is preferred. Sometimes, an unbalanced signal is preferred due to its higher immunity to common-mode noise, rejection of the parasitic couplings and increased dynamic range. The typical application is a conventional active balun, which is added to the output load of LNA circuit in GPS applications [99-102]. Due to the better high frequency performance, SiGe BiCMOS technology is preferred in this expedient structure [94, 95]. In terms of RFID receiver design, it is necessary to convert from a single-ended input signal to a differential input signal. The balun offers the optional freedom for the design as the differential LNA can also be employed. In the following chapter, the performance of merit between differential and singled-end LNA with active balun is discussed in order to determine the optimal solution for the RFID receiver front-end application.

2.5 Mixers Design

Mixers are non-linear devices and are used to translate radio frequency in the front-end of the receiver. The output signal from an ideal mixer should be an exact replica of the input RF signal. However, in practice, the non-linearity of the mixer will distort the output signal. The non-linearity in the active devices will further cause spurious response (or out-of-band interferers' rejection) issues [31]. Moreover, the noise analysis in the mixer is not as straight forward as in the LNA because of the frequency

translation. The noise at the image frequency could be converted and added into the RF noise, known as “noise folding”[103] The noise components near the no-ideal LO harmonics are also mixed and translated to IF, which could further affect the noise figure. Both the noise performance (noise cancelation techniques) and out-of-band interferers’ rejection are critical for receiver design because they both limit the boundary of the system’s sensitivity. To get the highest performance from the mixer we must make the RF to IF path as linear as possible, minimising the noise generated and minimise the switching time of the LO switch.

Either passive or active mixers can be utilised according to the design specifications. In general, passive types usually have advantages in structure simplicity, no DC power requirement, extra high operating frequency and better performance in linearity compared with active types [104]. However, the high conversion losses, induced high noise figures, and lower bandwidth limit the practical applications in modern RF design. The growth of CMOS technology also pushes the transistor-based active mixer into mainstream microwave application design.

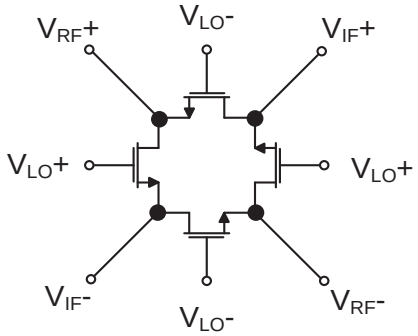


Figure 2-20: Schematic of a passive ring mixer.

The passive mixer yields higher linearity, simple architecture and no DC consumptions. As shown in Figure 2-20, a four-FET switch mixer can be used as a double-balanced up-conversion mixer that allows outputs tied together to select a single sideband [105]. However, it has no conversion gain and needs more LO power to pump these switches. Moreover, the VCO must follow with a buffer stage that provides more power to drive the passive mixer. Besides, the isolations among ports are usually much poorer compared with an active mixer.

A single-ended mixer is the simplest active mixer. Figure 2-21 (a) and (b) show two typical single FET configurations[106]. The "pinch-off" of transistor in gate-pumped configuration expresses a large non-linearity in saturation mode, thus a small change in V_{gs} leads to a large change in g_m. In this case, the isolation between RF and LO ports are very poor and proper separation between the ports is required. An improved isolation can be approached in drain-pumped configuration since the RF and LO ports feed in different ports, but it is still limited by C_{gs}. The non-linearity is still pronounced due to the transistor being biased at saturation mode [107]. Based on the drain-pumped mixer principle, the dual-gate FET (cascode) of Figure 2-21 (c) can be adopted to provide improved LO-RF isolation and low power consumption. The top transistor acts as both a common-gate amplifier and a source-follower for the bottom transistor to perform the mixing. However, beside the desired mixing signal, a wide range of out-of-band interferer components are also generated from those mixers. Furthermore, external high Q filters are required for the ports filtering.

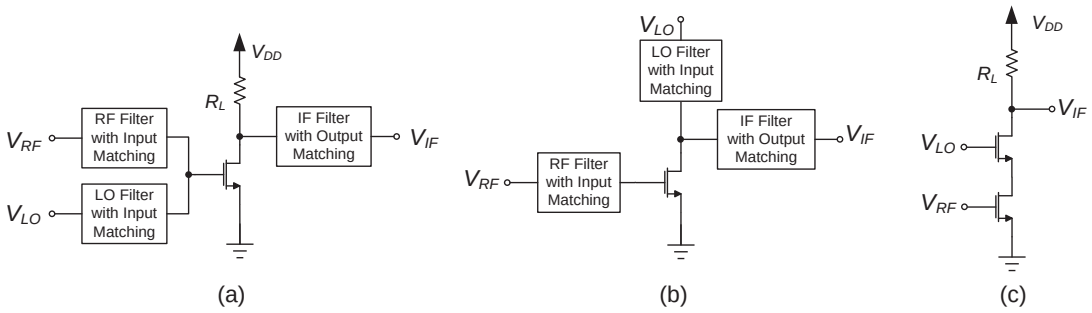


Figure 2-21: (a) Gate-pumped Single FET (b) drain-pumped Single FET and (c) Dual-gate FET mixer

Another critical parameter for the mixer is its port-to-port isolation. A single-balanced mixer is later proposed to have similar structure to dual-gate FET mixer. The current trans-conducted from the bottom transistor switches alternately to the LO pair branches. This differential switching pair equivalent working diagram is demonstrated in Figure 2-22. Even if the LO-to-RF isolation is improved, the LO-to IF isolation issue still exists. The odd-order LO harmonic components still appearing in the output need to be filter out. Nevertheless, both common-source trans-conductor and differential pair (acting as a virtual ground to the LO signal) provide good isolation between RF and LO. Thus it is still applied in some receiver systems [108-110].

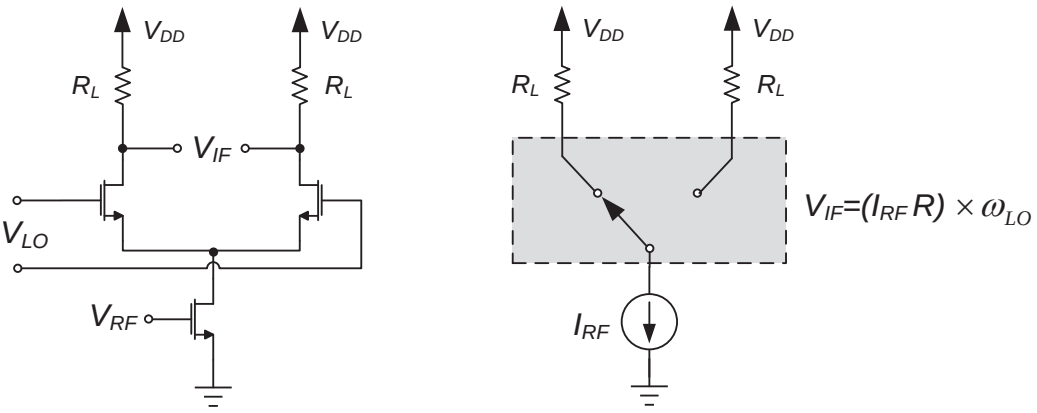


Figure 2-22: Single-balanced FET mixer and its switching equivalent diagram

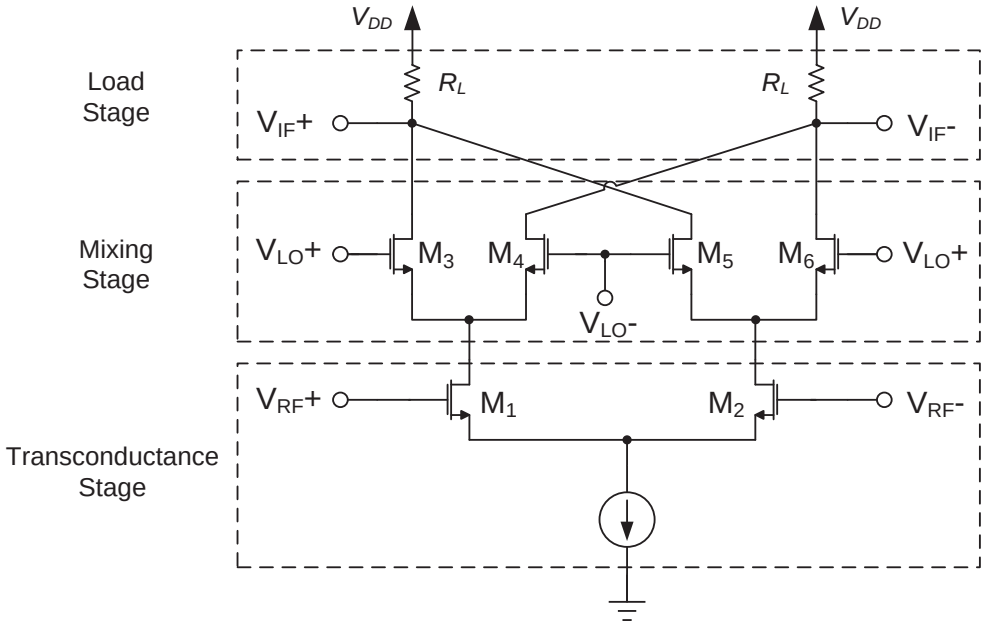


Figure 2-23: Typical Gilbert mixer

A double-balanced mixer is introduced to inherit the advantage of the single-balanced mixer and overcome its weakness. One of the most well-known double-balanced active mixer is the Gilbert cell mixer shown in Figure 2-23 [111]. The high conversion gain, compact structure and high isolation of the Gilbert mixer makes it the backbone of most of mixers used nowadays. The balanced mixing stage allows the LO signal to be cancelled while the IF signal appears differentially at the output. Consequently, a high LO-to-IF isolation can be achieved. The overall Gilbert mixer linearity is controlled by the trans-conductance stage only if the LO-driven transistors act as good switches.

In most of the RFID receiver front-end designs, passive mixers are preferred as they have higher linearity. Furthermore, the requirement of post-mixer amplifiers (PMA) with additional compensation gain will also introduce extra noise and stage signal delay. Active mixers that can offer better performance in isolation and conversion gain by replacing the conventional mixer with the PMA are investigated in following chapter.

2.6 Voltage Controlled Oscillators Design

In the transceiver design, the local oscillator (LO) provides carrier signals for signal conversion in front-end. As mentioned earlier, this process of frequency conversion is also called heterodyning. Oscillators are usually embedded as part of the phase-locked system. A voltage-controlled oscillator (VCO) has gained its dominance in oscillator design due to its flexible frequency tuning ability. In terms of waveform generation trends, oscillators can be classified as either the harmonic oscillator or the relaxation oscillator[112].

Ideal harmonic oscillators produce linear periodic sinusoidal output. A typical form of a harmonic oscillator is a feedback loop consisting of an amplifier and filter. The inherent noise is filtered and re-amplified until it resembles the desired signal. As such a circuit has no input while sustaining the output indefinitely, and a negative resistance or positive feedback system is used to form an oscillator. Almost all the well-known oscillators, such as the Colpitts oscillator[113], Hartley oscillator[114], Clap oscillator [115] and so on, are used in the feedback system with a LC harmonic resonate circuit. In contrast, a relaxation oscillator produces a non-sinusoidal output and contains nonlinear components. The active components (transistors) periodically discharge the energy stored in a capacitor or inductor to cause the disturbed changes of the output waveform. Ring oscillators are an extremely popular member, since they are derived from digital-like building blocks. Even they occasionally have inferior phase noise for a given level of power consumption compared to harmonic tuned oscillators; their relatively large tuning range and simplicity are attractive enough for many applications. However, relaxation oscillators are rarely used in high-performance transceivers because they generate signals of inadequate spectral purity[31].

The simplest LC circuit resembles a resonant “mass-spring” system. The active device joins the system to overcome the harmonic damping effect. Most of the tuned harmonic oscillators are named by those who first develop the topologies, but as seen in Figure 2-24, these designs appear more or less similar to the unified description. In the Colpitts oscillator, a capacitive voltage divider off the tank provides feedback to the amplifier. A sketch of the root locus shows the feedback is positive with a band pass filter. Rather than a tapped capacitor, a tapped inductor for feedback is implemented in the Hartley oscillator. The Clapp oscillator is a modified version of Colpitts’ oscillator, with a series LC replacing the single inductor. It offers an additional tap on the capacitive diver chain that allows an excessive voltage swing across the inductor. Among these topologies, the Colpitts is certainly the most commonly used topology due to its excellent phase noise performance. Crystal oscillators are later derived from the above LC structure to provide more stable and accurate tuning frequency.

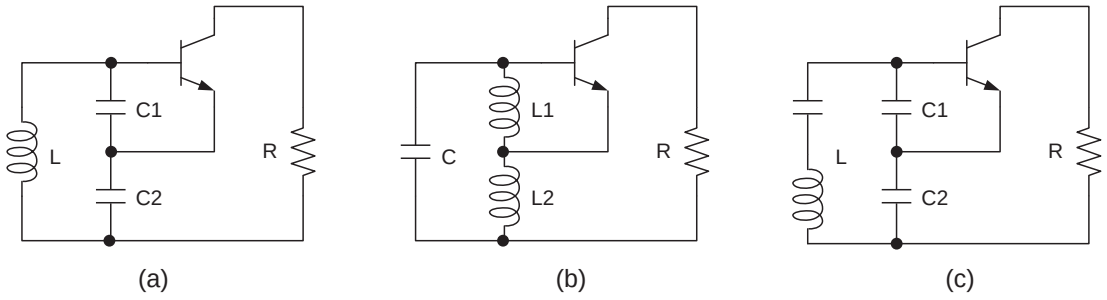


Figure 2-24: (a) Colpitts oscillator (b) Hartley oscillator and (c) Clapp oscillator

In the last decade, the differential cross-coupled LC oscillators have gained in popularity as they produce a more practical negative resistance, as shown in Figure 2-25 (a)[116-118]. The symmetrically half-circuit implied a negative resistor that is essentially identical from above equivalent circuits. A variable MOS capacitor is commonly used nowadays for extra tuning capability of the oscillator, as shown in Figure 2-25 (b) [119]. The current reusing complementary cross-coupled topology used in Figure 2-26 was proposed afterwards to overcome the voltage swing limit issue [120, 121], but with higher power consumption.

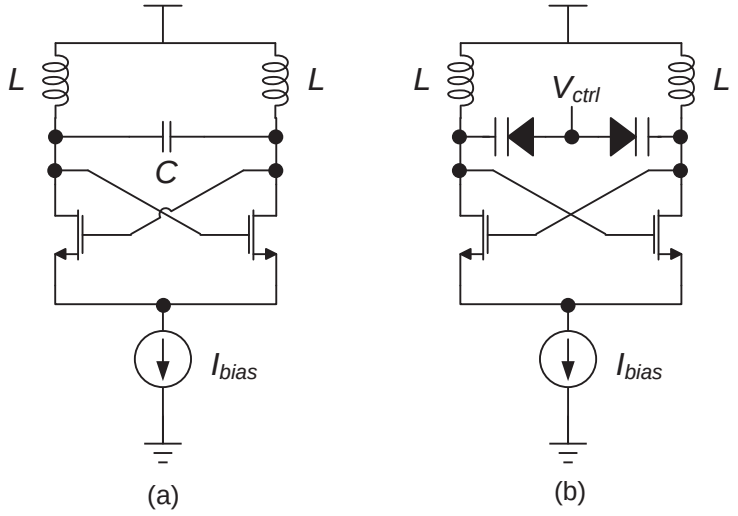


Figure 2-25: (a) Simple differential negative resistance oscillator and (b) Voltage-controlled negative resistance oscillator.

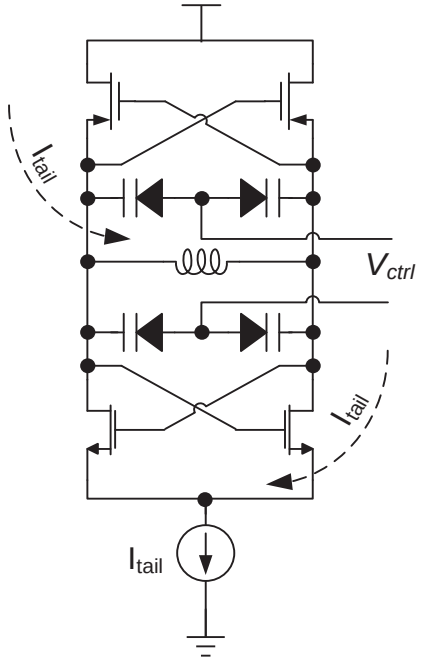


Figure 2-26: Current reusing complementary VCO topology

As discussed earlier, quadrature output is required for images rejection application. An oscillator architecture that naturally provides quadrature output uses a pair of integrators in a feedback loop. The Original (QVCO) was based on the cross-coupling of two differential LC VCOs [121-123]. This structure has coupling transistors and switch transistor in parallel that has poor phase-noise behaviour, as shown in Figure 2-27 (a). In order to improve the phase noise, the cross-coupling transistors were later placed in series with switch transistor rather than in parallel [29, 124, 125]. The structure with the

coupling transistor on the top of the switch transistor is known as a top-series QVCO (TS-QVCO), as shown in Figure 2-27 (b). Alternatively, a bottom-series QVCO (BS-QVCO) has the coupling transistor at the bottom as illustrated in Figure 2-27 (c). Simulations show that the BS-QVCO has better phase noise and higher phase error than the parallel QVCO and TS-QVCO[126].

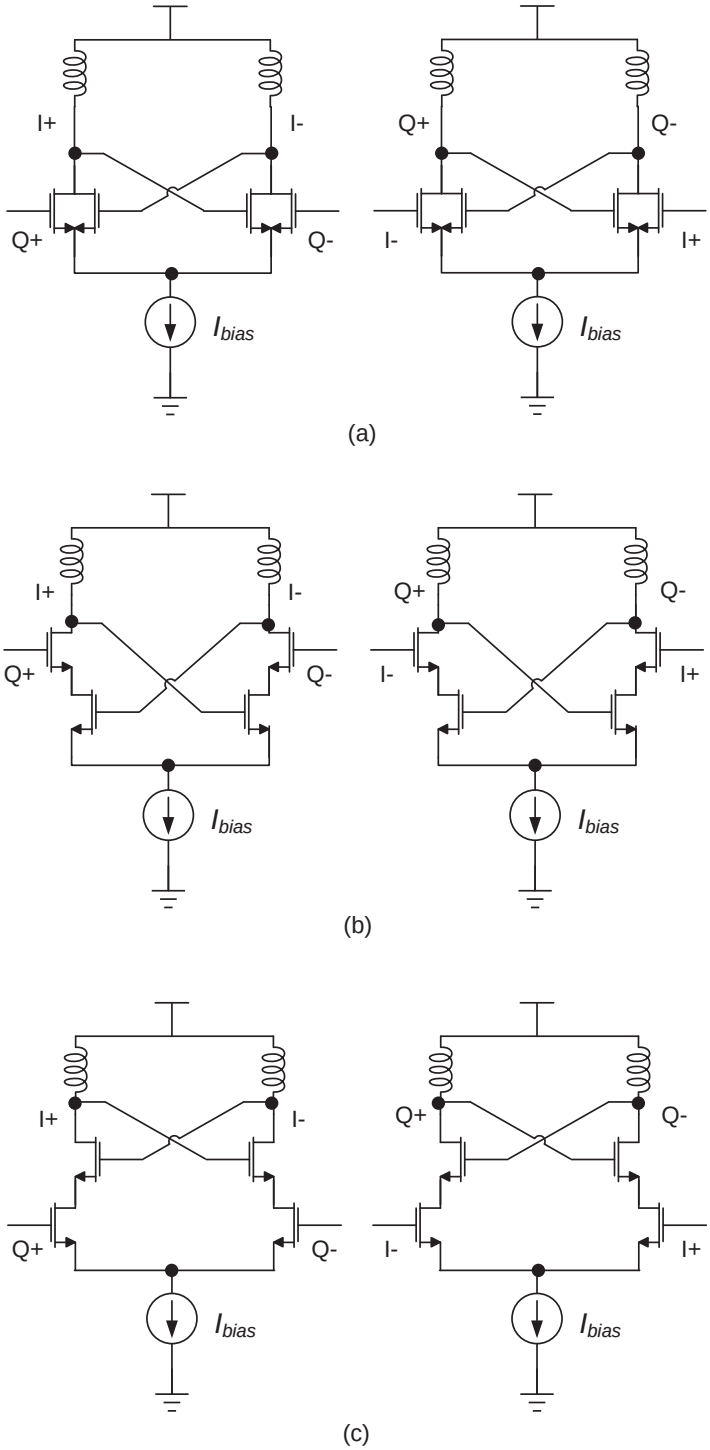


Figure 2-27: Schematic of (a) parallel QVCO (b) top-series QVCO[124] (c) bottom-series QVCO[126].

Since the telescopic cascode structure along with the tail current source constrains the voltage headroom, these topologies are not very suitable for today's deeply scaled power supplies, especially with symmetrical structures [127, 128]. They consume more power due to the stacking of the symmetrical coupling transistors in series with the switch transistors that generate negative resistance. Even low-voltage operation involving transformer coupling has been investigated [129]; it generally requires a large bias current through a single tail device, resulting in severe bandwidth versus headroom trade-off. The current reusing technique along with back-gate coupling uses less power but requires two extra bias voltages for optimal back-gate biasing[130]. VCO design with folded-cascode topology was introduced in 2010 with the advantages of requiring low power supplies and low power dissipation[131]. This topology will be investigated in the following chapter, where detailed analysis and simulation results will be presented and the topology's advantages and disadvantages will be discussed. In the meanwhile, the definition of phase noise and its numerical expression is reviewed for selection of better solution in an RFID receiver front-end.

2.7 Summary

RFID receivers require robust front-end topologies that can offer good linearity, low noise, image rejection and sensitivity. The continuous decrease in minimum feature size of CMOS technology has enabled the integration of more sophisticated single on-chip front-end blocks. Low power application becomes the mainstream in RFID design requirements.

In each individual blocks in RFID receiver front-end, investigation and analysis should be carried out to determine the optimal performance for each critical parameters. The g_{ds} should be taken into considerations in short-channel CMOS technology to construct a more accurate model for front-end system analysis and performance optimization. Either a single-ended LNA (with active balun) or differential LNA can be adopted in the front-end blocks but with proper assessment and evaluation. Active mixers can be used to replace passive mixers and PMA stage to gain extra freedom and

simplicity for the system. A tuneable low voltage CMOS quadrature VCO design can be performed for RFID application to be free from frequency ambiguity.

CHAPTER 3: DESIGN METHODOLOGY

In the previous chapter, an overview of the history of RFID development and the RFID system provided a broad understanding of how each front-end component functioned. The purpose in this chapter is to find the best solution for each system block that would optimise the overall system performance.

The performance criteria and design parameters are presented. Upon the analysis and evaluation of existing design methodology, the opportunities of improvement are identified and discussed. Lastly, novel circuit topologies and analysis techniques are used to achieve the optimum solution, which is presented.

3.1 Design Performance Criteria and Design Parameters

The key characteristics for RFID front-end design takes into consideration sensitivity, selectivity, stability, dynamic range and spurious response. These criteria characteristics are represented in detailed evaluation and specifications of each parameter. An overview and description for these design criteria is carried out below to give a better understanding for further design methodology.

3.1.1 Receiver Sensitivity

Sensitivity is defined as the minimum signal level at the receiver input such that there is a sufficient signal-to-noise power ratio (SNR) at the receiver output for a given application. The sensitivity of a system is usually specified in dBm (decibels relative to one mill watt), along with reference impedance. The overall sensitivity is directly impacted by the noise from individual blocks in the receiver as well as the gain distribution of the receiver chain.

Noise

Noise factor, denoted as F, is a figure of merit for noise produced by the LNAs and mixers. It compares the output noise power generated by the component to the thermal noise of an input source resistor (50Ω) at standard room temperature $T_0 = 290°K$. A general definition for noise factor is formulized as [31]:

$$F = \frac{Total\ Output\ Noise\ Power}{Output\ Noise\ Power\ due\ to\ Input\ Source} \quad (3\text{-}1)$$

Alternatively, the general definition can also be explained [132] as the ratio of the signal-to-noise (S/N) power ratio (SNR) at the input and the output of the system in the following format:

$$F = \frac{SNR_i}{SNR_o} = \frac{S_i/N_i}{S_o/N_o} \quad (3\text{-}2)$$

$$SNR = \frac{P_{signal}}{P_{noise}} = \left(\frac{A_{signal}}{A_{noise}}\right)^2 \quad (3\text{-}3)$$

where P is average power and A is root mean square (RMS) amplitude. The SNR value at the IF (or RF) port need to be specified for either single sideband (SSB) or double sideband (DSB). In SSB, it is assumed that the only noise present is from the expected signal frequency and not the image frequency. In DSB both sidebands are available thus it has twice as much power available at the IF port compared to the SSB signal. As a result, its conversion loss is 3dB less than that of an SSB signal. In receiver front-end design, it is important to identify either SSB noise or DSB noise.

Besides noise factor itself, noise figure and noise temperature are another two figures of merit appearing in literature frequently. Noise figure (NF) is simply the noise factor (F) expressed in decibels.

$$NF(dB) = 10 * log_{10}(F) \quad (3\text{-}4)$$

Since the noise contributes in increasing the temperature, noise temperature T_N can also be used for describing the noise performance of the amplifiers, which relates to the noise factor as follows:

$$T_N = 290 * (F - 1) \quad (3\text{-}5)$$

From the general noise factor definition in equation (3-1), the noise figure for the entire receiver front-end can be represented by Friis formula as[132]:

$$F_{total} = \frac{SNR_i}{SNR_o} = 1 + (F_1 - 1) + \frac{(F_2 - 1)}{A_1} + \cdots + \frac{(F_n - 1)}{A_1 \cdots A_{n-1}} \quad (3\text{-}6)$$

Where, A_i is the available output power gain of each block in the receiver, which is evaluated with the output impedance of the preceding block. This formula demonstrates that the noise from each stage is attenuated, while the first few stages contribute the most critical noise for the whole system. This explains why LNA dominates the entire receiver sensitivity and the importance of designing a LNA with low *NF* and high gain. The sensitivity of a receiver can be expressed in a format relative to noise floor and the required SNR at the input as follows:

$$Sensitivity\ (dBm) = SNR_{in}(dB) + NoiseFloor(dBm) + 10\,log(BW)\,(dB) \quad (3\text{-}7)$$

where BW is the bandwidth of the communication channel.

In oscillator design, one more type of noise, known as phase noise, is defined as the random phase variation in the VCO's output. Substantial phase noise could corrupt the desired signal at the receiver. In a homodyne receiver, the noise close to the carrier phase is mainly composed of flicker noise and is only generated by the active devices. The phase noise is measured from 1 KHz off the carrier to several MHz off the carrier in a 1-Hz bandwidth. Phase noise is also defined as the ratio of the output power divided by the noise power at a specified value and expressed in dBc/Hz. It is a type of cyclostationary noise and is closely related to jitter. The integrated phase noise (expressed in degrees) can be converted to jitter (expressed in second) using following formula:

$$Jitter = \frac{Phase\ Error}{360 \cdot f} \tag{3-8}$$

Phase noise is the crucial measurement parameter in an oscillator design. Oscillator phase noise often includes low frequency flicker noise and white noise. The detail of identifying phase noise for VCO is carried out later in this chapter.

Gain

The Gain of an amplifier can be either represented as voltage gain or power gain. In a typical receiver, the power levels at the antenna are around -120dBm and this signal can be further degraded in the presence of the physical obstructions and environment medium. Therefore, the main function of an amplifier (such as LNA) is to provide enough available gain for signal processing in subsequent stages. Friis equations demonstrate that when the gain at the first stage is large enough, the noise of the subsequent stages are reduced.

In a mixer, the conversion gain (CG) is used instead and defined as the ratio (in dB) between the IF signal and the RF signal. It can be represented in a format of either voltage (or current) or power conversion gain. Following expression is one way of representing the conversion gain in voltage syntax for a down-converting mixer ($\omega_{RF} - \omega_{LO}$):

$$CG = \frac{\frac{1}{2} A_{LO}(t) A_{RF}(t)}{A_{RF}(t)} = \frac{A_{LO}(t)}{2} \tag{3-9}$$

where A are root mean square (RMS) amplitudes for local oscillator and RF signal. The conversion gain of a mixer could exceed 1 in some active mixers if it is represented in power gain form. The magnitude of the power conversion gain is proportional to the square of the voltage conversion gain. Therefore, an active mixer can amplify the signal in mixing. However, the noise figure and linearity are also critical performance parameters for design considerations. That would explain why in some circumstances, passive mixers are also used even if they have conversion gain loss.

3.1.2 Receiver Selectivity

Receiver selectivity is a performance measure of the ability to separate the desired signal from those unexpected interfering signals at the input. It is especially critical for RFID applications since the desired signal is usually weak comparing to those strong interfering signals in adjacent channels. Different to sensitivity, the selectivity is not represented in any quantitative measure at circuit level. The physical layer is usually used to represent the sensitivity in the form of nonlinearity, and phase noise.

As mentioned in the previous chapter, strong interference jammer (blocker) signal can significantly degrade the receiver performance by presenting in mixing itself with the desired signal in direct-conversion or low-IF/Zero-IF receiver. This is defined as its nonlinearity, which will further induce high phase noise from the local oscillator after mixing with the jammer signal. The out-of-band jammers can be easily attenuated and filtered out by the band-selecting filter. However, the in-band blockers usually cause a lot of problems in practical receiver design. A well designed mixer with high linearity and port-to-port isolation is necessary to overcome these problems.

Linearity

Since active RF devices are ultimately non-linear in operation, linearity or inter-modulation distortion is one of the most significant figures of merit in an RF device. The device could generate an undesirable spurious signal while driven by a large RF input signal and the linearity of the device defines how many spurious signals are generated by the device.

An amplifier (or mixer) maintains a constant gain at a low power level input signal. However, when driven with a large enough power level, the amplifier goes into saturation and its gain starts to roll-off. The 1dB compression point (P1dB) is a figure of merit for output power, which indicates the power level that causes the gain to drop by 1 dB from its small signal value. In other words, a higher compression point means higher output power. The Figure 3-1 shows two ways of defining 1dB compression point: (a) the gain vs. input/output power gain and (b) the input power gain versus output power

gain plot. Occasionally, two or three dB compression points (P2dB and P3dB) are also employed in amplifier design.

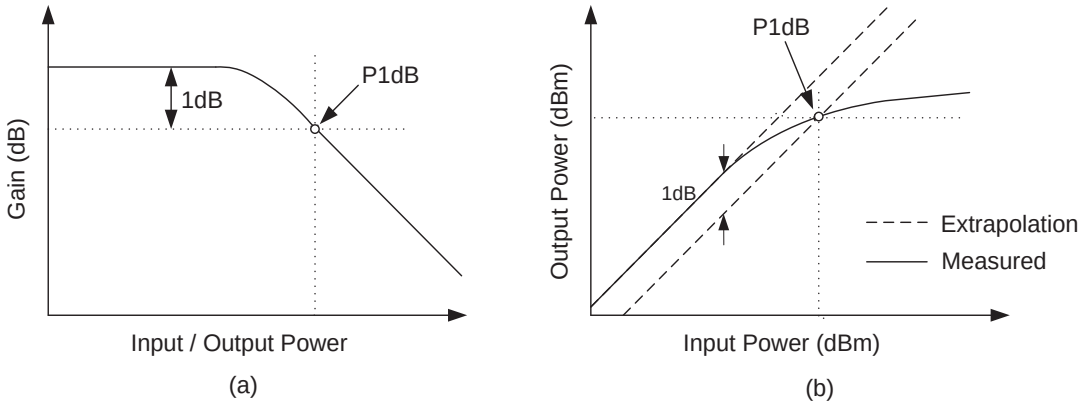


Figure 3-1:(a) Gain compression plot and (b) input power gain vs. output power gain plot

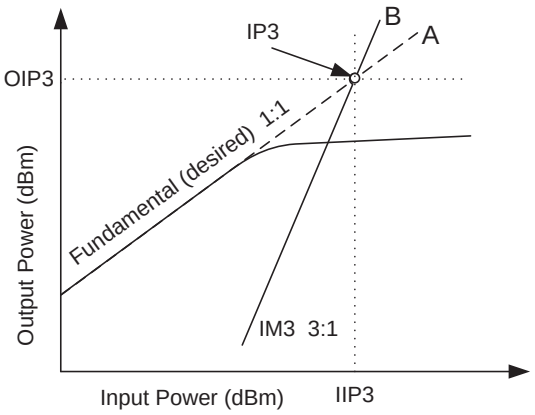


Figure 3-2: IP3 is the hypothetical interception of fundamental signal power response curve A and IM3 power response curve B

Second-order intercept point (IP2) and third-order intercept point (IP3) are another two figures of merit for linearity that quantifies the second-order or third-order distortion. IP3 is commonly tested with two fundamental sinusoid input tones with a small frequency difference. The idea of this intercept point is based on inter-modulation products as the device nonlinearity can be modelled using a low-order polynomial. Because the amplifier is not perfectly linear, the output of the amplifier also produces two third-order inter-modulation (IM3) products from desired signals. The IM3 distortion products could be very close in frequency to the desired signals and they

cannot be removed easily by filtering. In order to reduce third order distortion products, the IP3 specification must be increased. Hence, a higher IP3 means better linearity and less distortion. The intercept point can be obtained graphically by plotting the output power versus the input power. Represented in mathematical terms, IP3 is a theoretical input power point at which the fundamental and third-order distortion output lines are intercepted, as shown in Figure 3-2. Curve "A" here represents the linearly amplified output power versus input power for the desired fundamental signal and curve B stands for the nonlinear product third-order distortion output power (IM3) versus input power. The slope of curve B is three times steeper and theoretically intersects curve A. The hypothetical input power at this point is the input IP3 (IIP3) and the output power is the OIP3 respectively.

3.1.3 Scattering parameters

Scattering parameters or S-parameters describes the electrical behaviours of linear multiple ports network under various steady state stimuli. Instead of applying open or short circuit conditions to characterize a linear network in Y- and Z-parameters, S-parameters matches directly with loaded terminations, hence they are much facilitated and easier to apply at high signal frequencies. Most electrical properties of the network of components can be expressed using S-parameters, such as gain, return loss, voltage standing wave ratio (VSWR), reflection coefficient (isolation) and amplifier stability. S-parameters are preferred at RF and microwave frequencies, where signal power and energy considerations are more easily quantified than currents and voltages. S-parameters change with the measurement frequency and the characteristic impedance of the system. S-parameters are usually represented in matrix format.

In a generic multi-port network with port n, the associated S-parameter definition is in terms of incident and reflected "power waves", a_n and b_n respectively. In typical two-port network, the scattering matrix can be represented as:

$$\begin{bmatrix} b_1 \\ b_2 \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \end{bmatrix} \qquad (3\text{-}10)$$

The incident and reflected waves a_1, a_2, b_1 and b_2 are defined in terms of voltage and current with a real-valued positive reference impedance Z_0 as follows:

$$\begin{bmatrix} a_1 = \dfrac{V_1 + Z_0 I_1}{2\sqrt{Z_0}} & a_2 = \dfrac{V_1 + Z_0(-I_2)}{2\sqrt{Z_0}} \\ b_1 = \dfrac{V_1 - Z_0 I_1}{2\sqrt{Z_0}} & b_2 = \dfrac{V_1 - Z_0(-I_2)}{2\sqrt{Z_0}} \end{bmatrix} \quad (3\text{-}11)$$

Hence, individual S-parameters can be represented with the incident and reflected power waves when each port is terminated individually with a load identical to the system impedance as follows:

$$\begin{bmatrix} S_{11} = \dfrac{b_1}{a_1} = \dfrac{\mathrm{V}_1^-}{\mathrm{V}_1^+} & S_{21} = \dfrac{b_2}{a_1} = \dfrac{\mathrm{V}_2^-}{\mathrm{V}_1^+} \\ S_{12} = \dfrac{b_1}{a_2} = \dfrac{\mathrm{V}_1^-}{\mathrm{V}_2^+} & S_{22} = \dfrac{b_2}{a_2} = \dfrac{\mathrm{V}_2^-}{\mathrm{V}_2^+} \end{bmatrix} \quad (3\text{-}12)$$

From the above derived formula, S_{11} stands for the input port voltage reflection coefficient, S_{12} is the reverse voltage gain that also represents port-to-port isolation, S_{21} is the forward voltage gain that also evaluated as gain for the device and S_{22} can be identified as the output port voltage reflection coefficient. Hence, when $Z_L = Z_0$, no reflected waves from the load lead $a_2 = 0$ and left only reflection coefficient S_{11} and forward voltage gain S_{21} (also known as transmission coefficient).

In describing the stability conditions of an amplifier in terms of S-parameters, the following definitions of constants are often used:

$$\Delta = S_{11}S_{22} - S_{12}S_{21} \quad (3\text{-}13)$$

and defining unconditional stability by the Rollet stability factor (K) as [133]

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}S_{21}|} \quad (3\text{-}14)$$

The condition of unconditional stability is achieved when K is greater than 1 and $|\Delta|$ is smaller than 1.

3.1.4 Frequency Pushing and Pulling Effect

The frequency pushing effect is defined as the variation of the oscillator's output frequency due to the change in the power supply. At a specific tuning voltage, the frequency change due to the power supply change yields the frequency pushing. The value of frequency pushing may vary at different tuning voltages. Therefore, an unreliable power source may degrade phase noise as well. In order to improve the power supply rejection ratio, low-dropout linear regulators (LDOs) are preferred [134].

Frequency pulling is a measure of frequency change due to a non-ideal load at output. The changes of output impedance may also lead to unstable oscillator performance. Measurement of the frequency pulling can be achieved by noting the frequency change caused by a load having a nominal 12dB return loss with all possible phases. The frequency pulling should be minimised, especially in cases where power stages are close to the VCO and short pulses might affect the output frequency. Buffer stages after VCO output may reduce the pulling effect [135].

3.2 Architectural and Specification Considerations

As in the Weaver architecture, a low-IF architecture inherits many of the attributes of a homodyne receiver, but it has lower sensitivity to DC offsets and higher $\frac{1}{f}$ noise. The trade-off, however, reappears as the image rejection issue. If the goal for the receiver design is to avoid the use of expensive filters, then the burden of image rejection can only be solved by using suitable architecture. The Weaver architecture, which has the ability to resolve the difference between negative and positive frequencies, also endows it with the ability to resolve the difference between a signal and its image.

Although the direct-conversion receiver architecture has many drawbacks, it has still gained popularity in RFID system due to the improvement in IC technologies. Well controlled and suppressed IC technologies enable its possibility in discrete implementation. Since direct-conversion receiver architecture directly converts RF to baseband, the DCR employs only LPF for filtering out unwanted interference and no image rejection filter is required. Moreover, LPF and one stage of LO has also reduced the architecture complexity (BPF design in superheterodyne is much more complex compare to LPF) and power consumption of the system.

Likewise, in order to approach low power consumption and simple circuit structure, the active mixer is employed as passive ring mixer and post-mixer amplifier (PMA). Even though an active mixer has worse linearity when compared to a passive mixer, it performs better in isolation and has better conversion gain. In addition, the extra PMA stage will introduce extra noise and signal processing delay.

A down-converted band in direct-conversion receiver architecture also faces some serious problems that require further discussion. Since the signals are down-converted to baseband, any DC offset voltages can corrupt the signal. Large DC voltage can affect the bias voltage of the transistors and further degrade the performance of other stages. In RF front-end blocks, LO leakage often occurs when there is an imperfect isolation among the LO port, IF port and the RF port. The feed-through from capacitive and substrate coupling will heavily degrade the performance between LNA and mixer. This offset problem can be more severe and unpredictable if the LO is provided externally, which will introduce additional bond-wire coupling. The LO leakage signal will feed-through the mixer and subsequently mixed with the desired LO signal, causing a “self-mixing” issue. The dc term generated by self-mixing can saturate the front-end stages in the receiver or even leak to the antenna since LNA and mixer have limited reverse isolation capability. This leakage problem could further contaminate itself or nearby receivers to become “self-jammer” [38]. A similar situation could also occur the other way around from mixer input to LO port, known as interferer leakage. Therefore, maintaining high isolation between ports and high linearity for LNA, mixer and VCO are the major concerns in further design.

Down-converted signal after the mixer is usually feeble and very sensitive to any noise. Especially, the signal of interest at zero-IF frequency is susceptible to the flicker noise (also known as $1/f$ noise). A closer investigation regarding noise behaviour around baseband frequency should be carried out. A relatively high gain in the RF range is desirable in the later design considerations. Therefore, an active mixer is preferred to passive mixer in this design to achieve higher gain.

In baseband, the even-order distortion in homodyne structure becomes critical enough to be taken into consideration. The second-order intercept point (IP2) should remain at a high value to overcome the distortion problem. Applying capacitive degeneration and ac coupling techniques in the mixer design can improve even-order linearity. Differential mixer topologies are less susceptible to the even-order distortion and will be employed in later designs. Unfortunately, this problem may not be alleviated in the LNA stage since single-ended LNA is required to work with antenna and duplex filter in a typical single-ended system. Converting the single output to a differential signal may require extra blocks such as baluns and lead to additional power consumption. Unfortunately, a transformer is avoided at high frequency since it generates high losses as a consequence of a higher noise figure [136]. Therefore, optimizing the trade-offs between power consumption, system simplification, performance in system design and evaluation for different structures should be carried out in detail.

In this work, each block operates in UHF range at 866 MHz frequency. The LNA and mixers design should provide a high voltage or conversion gain (>12dB) and low noise figure (<2.5dB for LNA and <6dB for mixer) at this operating frequency. Since the direct-conversion receiver architecture is applied here, the VCO is required to generate the same oscillating frequency (866MHz) and low phase noise (<120 @ 3MHz). The supply voltage and power dissipation are also critical for the design consideration and aim to remain as low as possible.

In the following sections, each block of the RFID front-end is investigated in detail with respect to both design methodology and circuit topology to overcome design problems. To evaluate overall performance, more than one possible solution is described. At the same time, derivation of accurate models for each component was done in order to optimise overall performance. Figure 3-3 demonstrates the direct-conversion receiver

architecture with image-reject mixers that are employed in this thesis for the UHF RFID receiver front-end.

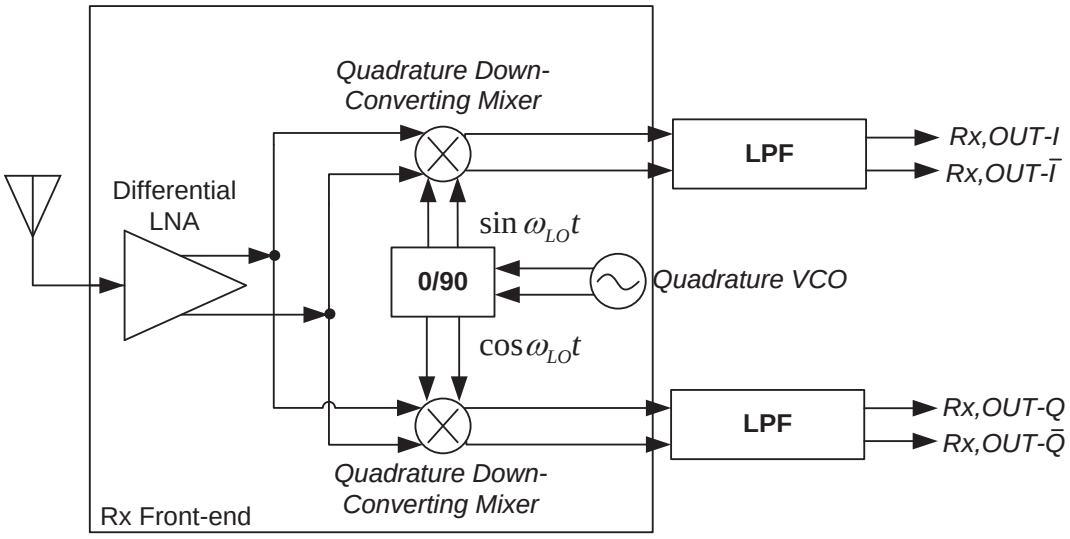


Figure 3-3: Proposed Direct-conversion receiver architecture in this thesis for RFID receiver front-end.

3.3 LNA Design Topologies and Methodologies

The noise in general can be defined as "everything except the desired signal"[31]. Apart from those artificial noise sources, such as AC signal noise, the noise sources in technical terms are described as those irreducible sources of noise from a device, in particular, the MOS transistor in this research. One of the major challenges for the LNA design is to understand the noise modelling as the sensitive performance of an RF system are limited by noise. Therefore, the defining and measuring of noise are becoming a significant part of semiconductor device characterization and SPICE modelling.

3.3.1 Noise Sources and Noise Modelling in MOS transistor

Due to the stronger skin effect in surface mechanism, the performances of noise in the MOSFET transistor are worse compared to the bipolar transistors. These deficiencies

are demonstrated in different sources of noise varying with different frequency bands. The short-channel effects, such as velocity saturation and hot electrons in particular, become apparent along with the shrinking of the channel length in MOSFET's technology. Hence, the classical drain current thermal noise model in MOS transistor is no longer applicable. In particular in MOSFETs, the flicker noise ($1/f$ noise) exhibits its corner frequency between tens of KHz to a few MHz. This will result in the phase noise increase in the RF circuits, such as in the VCOs. The drain current thermal noise in MOS transistor is another major noise source due to the random thermal motion of the charge carriers. Furthermore, excess noise from induced gate current will contribute most of the noise from one tenth of f_T. These two types of noise are usually the major noise source for RF application considerations [137]. Hence, these three main noise sources will form bathtub-shaped characteristics over the frequency. Figure 3-4 illustrates the approximate noise figure characteristic of a MOS transistor over the frequency connect to 50Ω source impedance. A precise noise model under high frequency for MOS transistor is necessary for modern RF front-end design[31].

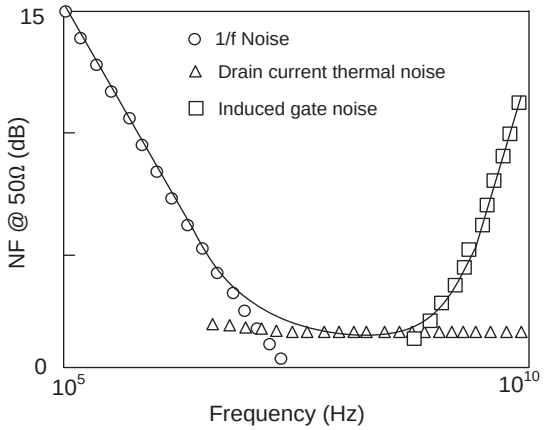


Figure 3-4: Noise figure of a MOS transistor with impedance matching (50Ω)[138]

Thermal Noise

Johnson [139, 140] first discovered and measured the noise in resistors and his colleague Nyquist [141] explained them as a consequence of random Brownian motion of thermally-excited charged electron in a conductor. Thermal noise of a resistor is quite often represented by either available noise power (P_{NA}) or noise power spectrum in square voltage or in square current ($\overline{e_n^2}$ or $\overline{i_n^2}$) as following:

$$P_{NA} = kT\Delta f \quad (3\text{-}15)$$

$$\overline{e_n^2} = 4kTR\Delta f \quad (3\text{-}16)$$

$$\overline{i_n^2} = \frac{4kT\Delta f}{R} = 4kTG\Delta f \quad (3\text{-}17)$$

where k is Boltzmann's constant (about 1.38×10^{-23} J/K), T is absolute temperature in Kelvin and Δf is the noise equivalent brick-wall bandwidth in hertz. Based on the definition, the only way to minimise the thermal noise is to keep the temperature as low as possible and limiting the brick-wall bandwidth. Therefore, the parasitic resistance of all practical capacitors and inductors generate thermal noise.

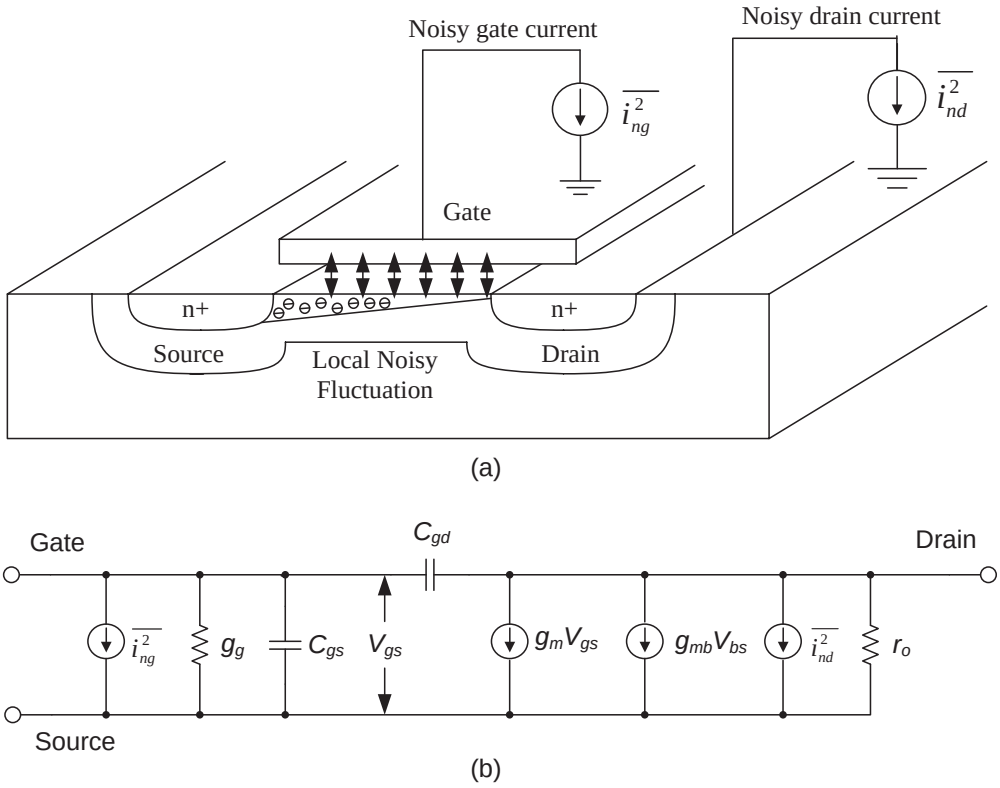


Figure 3-5: (a) Drain current noise and induced gate noise in MOSFET devices and (b) its small-signal equivalent circuit with noise source

MOS transistors also exhibit thermal noise because they are based on modulated voltage-controlled resistors capacitive-coupled to the gate. Hence, both drain current and induced gate current generate noise, as shown in Figure 3-5. Van der Ziel deduced

following expression for the drain current noise, induced gate noise and their cross-correlation coefficient for MOS transistor [142]:

$$\overline{i_{nd}^2} = 4kT\gamma g_{d0}\Delta f \quad (3\text{-}18)$$

$$\overline{i_{ng}^2} = 4kT\delta g_g \Delta f \quad (3\text{-}19)$$

$$g_g = \frac{\omega^2 C_{gs}^2}{5 g_{d0}} \quad (3\text{-}20)$$

$$\mathrm{c} \equiv \frac{\overline{i_{ng} \cdot i_{nd}^*}}{\sqrt{\overline{i_{ng}^2} \cdot \overline{i_{nd}^2}}} \quad (3\text{-}21)$$

here, g_{d0} and g_g are the drain-source conductance when $V_{DS} = 0$ and real part of the gate-to-source admittance respectively. The parameters γ and δ are bias dependent coefficients. Drain current noise coefficient γ has a value of 1 when $V_{DS} = 0$ and the value decreases to approximate 0.6 in saturation for long-channel MOSFETs[142] [143]. Van der Ziel [142] also caclulated the value of 4/3 for the gate noise coefficient δ in long-channel devices. Short-channel MOSFET devices have larger drain current comparing to the long-channel devices due to shorter channel length, stronger crosswise magnetic field induction. Hence, hot electrons in the channel are speeded up to increase the collision opportunity. The cross-correlation coefficient c has a theoretical value $-j0.395$ for long-channel transistor and this value reduced lower than 0.2 for short-channel device [137].

Shot Noise

This type of electronic noise occurs when a finite number of energy-carrying particles are small enough to trigger a detectable data fluctuation in a measurement. It requires a potential barrier over the carriers, which indicates that the linear devices do not generate this kind of noise. Thus shot noise only contributes when there is DC gate leakage current exist in MOSFET devices. Fortunately, this value is usually small enough to be negligible in RF design.[143]

Flicker Noise ($1/f$ noise)

Johnson made the first electronic system for observing noise [144] and he detected a "mystical" but ubiquitous noise, called flicker noise. Since its spectral density increases

unlimitedly with decreasing frequency, this noise is also known as $1/f$ noise. Unlike thermal and shot noise, the model for this ubiquitous noise contains various empirical parameters shown as:

$$\overline{N^2} = \frac{K}{f^n}\Delta f \qquad (3\text{-}22)$$

In this expression, $\overline{N^2}$ can be either current noise $\overline{i_n^2}$ or voltage noise $\overline{v_n^2}$, K represents an empirical parameter that usually depends on the device or bias and n equals to unity in most cases.

Flicker noise is significantly more notable in MOSFET devices than in bipolar devices since it is very sensitive to surface devices than bulk devices, or more precisely, to the charge trapping phenomena. Some types of defects and certain impurities can randomly trap and release charges at the Si/SiO_2 interface. In MOSFETs, flicker noise is defined as:

$$\overline{i_n^2} = \frac{K}{f}\cdot\frac{g_m^2}{WLC_{ox}^2}\cdot\Delta f \approx \frac{K}{f}\cdot\omega_T^2\cdot A\cdot\Delta f \qquad (3\text{-}23)$$

where A is the area of the gate and K is a device-specific constant. From the model expression, in order to reduce the noise term for a fixed trans-conductance g_m, larger transistor (gate area A) and a thinner dielectric is preferred. Noticeably, flicker noise does not only affect the application performance at low-frequency, but also serious impact in phase noise due to the upconversion.

Parasitic Noise Components

Another similar white noise (bandwidth dependent) called shot noise was defined by Schottky in 1918 [145] as:

$$\overline{i_n^2} = 2qI_{DC}\Delta f \qquad (3\text{-}24)$$

Intrinsic noise measuring requires de-embedding procedure since the parasitic components sometime significantly influence the noise performance in the measurement stage. The parasitic noises for the DUT implicate components from bonding pad, gate poly resistance, subtract resistance and etc.

Classical Two-Port Noise Theory

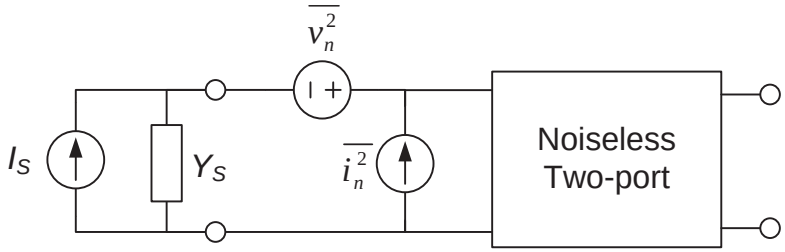


Figure 3-6: Equivalent circuit model for a typical noisy two-port

Based on the detailed noise models of the CMOS transistor, a two-port system can be developed from a macroscopic perspective. A noisy two-port model (as shown in Figure 3-6) can greatly simplify the analysis and lead to the acquisition of useful design insight for the following chapter. Since all the noise sources are input-referred, the expression for noise factor is therefore given by

$$F = \frac{\overline{i_s^2} + \overline{|i_n^2 + Y_s v_n^2|^2}}{\overline{i_s^2}} = \frac{\overline{i_s^2} + \overline{|i_u^2 + (Y_c + Y_s) v_n^2|^2}}{\overline{i_s^2}} = 1 + \frac{i_u^2 + (Y_c + Y_s) v_n^2}{\overline{i_s^2}} \qquad (3\text{-}25)$$

where i_c is the part of noise current i_n that is correlated with v_n, which is defined as $i_c = Y_c\, v_n$, while i_u is the part of i_n that is uncorrelated. This noise factors contains three independent noise sources as follows:

$$R_n = \frac{\overline{e_n^2}}{4kT\Delta f} \qquad (3\text{-}26)$$

$$G_u = \frac{\overline{i_u^2}}{4kT\Delta f} \qquad (3\text{-}27)$$

$$G_s = \frac{\overline{i_s^2}}{4kT\Delta f} \qquad (3\text{-}28)$$

$$Y_c = \frac{i_c}{e_n} = G_c + jB_c \qquad (3\text{-}29)$$

Thus, the noise factor is now written in terms of these parameters as:

$$F = 1 + \frac{G_u + |Y_c + Y_s|^2 R_n}{G_s} = 1 + \frac{G_u + [(G_c + G_s)^2 + (B_c + B_s)^2] R_n}{G_s} \quad (3\text{-}30)$$

The optimal admittance from above equation can be approached when the source conductance and source susceptance cancel each other and this yields [31]:

$$B_c = -B_s = B_{opt} \quad (3\text{-}31)$$

$$G_s = \sqrt{\frac{G_u}{R_n} + G_c^2} = G_{opt} \quad (3\text{-}32)$$

This optimal condition can be used to calculate the minimum noise figure as:

$$F_{min} = 1 + 2R_n\left(G_{opt} + G_c\right) \quad (3\text{-}33)$$

Consequently, the general expression for noise figure now can be represented with F_{min} term as [31]:

$$F = F_{min} + \frac{R_n}{G_s}\left[\left(G_s - G_{opt}\right)^2 + \left(B_s - B_{opt}\right)^2\right] \quad (3\text{-}34)$$

3.3.2 LNA Design with NF and Input Matching Considerations

In general LNA design, the topology considerations pursue both minimum NF and optimum input impedance matching simultaneously. The impedance matching is important in LNA design because the matching of antenna impedance enable the maximum RF power delivery and minimum reflections. The classical noise matching (CNM) topology deduced from conversion common-source (CS) amplifier [57, 146] is shown in Figure 3-7(a). In this technique, the LNA is designed for minimum NF F_{min} by presenting the optimum noise impedance Z_{opt} . This is achieved by adding a

matching circuit between the source and the input of the amplifier. However, due to the inherent mismatch between Z_{opt} and Z_{in}^{*} (where Z_{in}^{*} is the complex conjugate of the amplifier input impedance), the amplifier can experience a significant gain mismatch at the input. Therefore, the CNM technique typically requires a compromise between the gain and noise performance. The simplified small-signal equivalent circuit in Figure 3-7 (b) neglects the terminals parasitic resistances, gate-drain capacitance, drain-source capacitance and transistor conductance. The noise analytical model represented in this equivalent circuit includes the intrinsic transistor noise current $\overline{i_{nd}^2}$ for the mean-squared channel (drain) thermal noise current as defined in equation (3-18) and $\overline{i_{ng}^2}$ for the mean-squared induced gate thermal noise current as represented in equation (3-19). Besides deducing the noise parameters from the two-port noise theory in equation (3-26), (3-27), (3-28) and (3-29), the noise parameters for the amplifier can be expressed as [31]:

$$R_n^{\circ} = \frac{\gamma}{\alpha} \cdot \frac{1}{g_m} \tag{3-35}$$

$$Y_{opt}^{\circ} = \alpha\omega C_{gs}\sqrt{\frac{\delta}{5\gamma}(1-|c|^2)} - sC_{gs}\left(1-\alpha|c|\sqrt{\frac{\delta}{5\gamma}}\right) \tag{3-36}$$

$$F_{min}^{\circ} = 1 + \frac{2}{\sqrt{5}}\frac{\omega}{\omega_T}\sqrt{\gamma\delta(1-|c|^2)} \tag{3-37}$$

where R_n° represents the noise resistance, Y_{opt}° is the optimum noise admittance and F_{min}° is the minimum noise factor, respectively. The cut-off frequency ω_T equals to g_m/C_{gs} and parameter $\alpha = g_m/g_{d0}$ is unity for long-channel devices and decreases when channel length scales down.

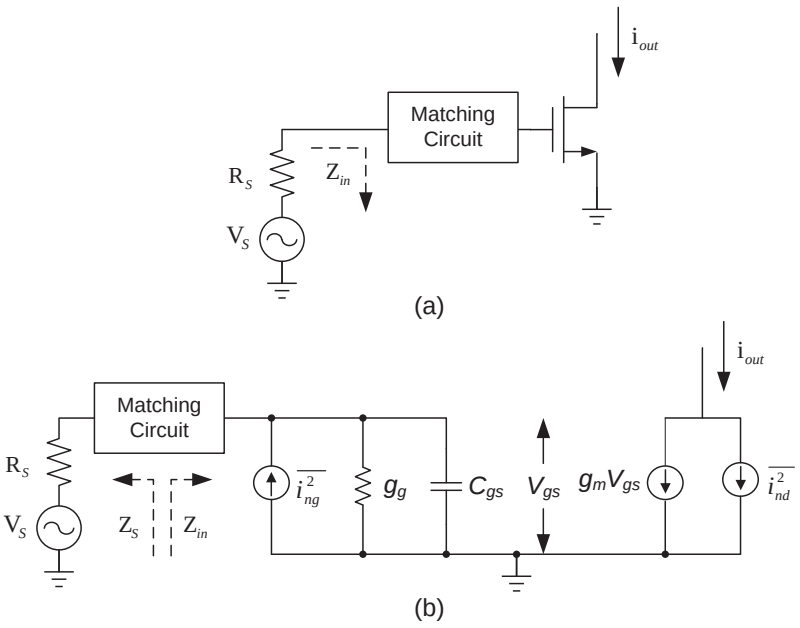


Figure 3-7: (a) Schematic of a CS LNA topology adopted to apply the CNM technique and (b) its small-signal equivalent circuit

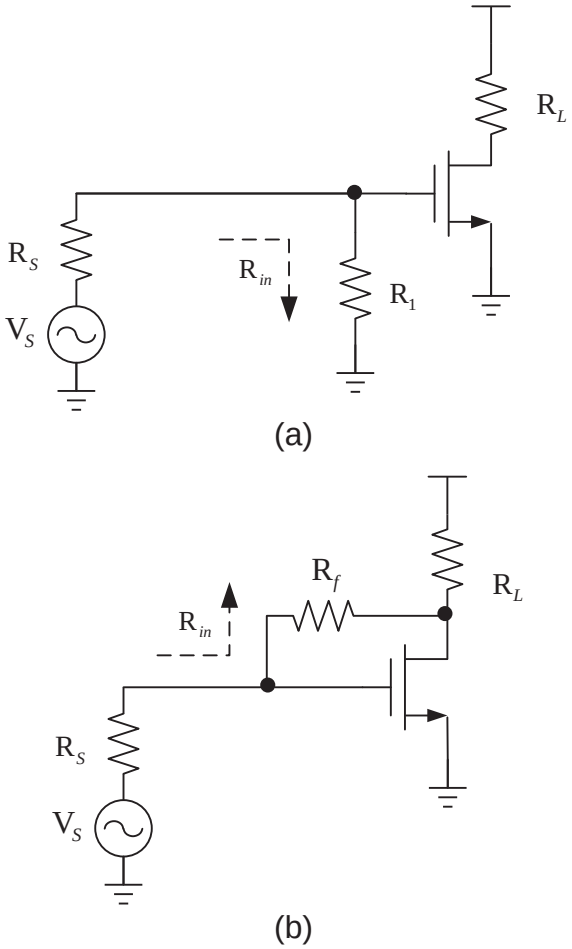


Figure 3-8: (a) Directly resistive termination matching topology and (b) shunt-series feedback matching topology

A typical input impedance (X) of the LNA should be 50Ω. However, the input admittance ($Y = \frac{1}{X}$) in equation (3-36) is purely capacitive ($Y_{opt}^{\circ} = j\omega C_{gs}$), which is inherently different from the noise matching condition in both real and imaginary parts. Thus, it becomes a challenge to match the signal source without large degradation of noise performance. In practical implementation, the most straightforward method is directly resistive termination matching to source impedance, as shown in Figure 3-8(a). The matching bandwidth is therefore determined by the input capacitance of the MOS transistor and can approach a few gigahertz of bandwidth for wide-band application. However, this matching resistor R_1 generates its own thermal noise and halves the desired signal as voltage divider. These two properties therefore aggravate the noise factor and are thus not practically suitable in low noise application. Shunt-series feedback is another method to achieve input matching. This topology, demonstrated in Figure 3-8(b), does not attenuate the signal like resistive termination matching. The input impedance R_{in} is determined by load impedanceR_L, feedback impedance R_f and transistor trans-conductor g_m as:

$$R_{in} = \frac{R_L + R_f}{1 + g_m R_L} \qquad (3\text{-}38)$$

This expression provides more than one degree of freedom for matching possibility and becomes an attractive choice for multi-band and wideband LNA design [63, 68, 69]. However, it still contributes its own thermal noise and this can significantly affect the overall noise performance in the system. In the trade-off of approaching lower noise, large power dissipation is necessary. As an example in [68], even if the latest 90nm technology is adopted, the single-ended LNA consumes 42mW power in order to satisfy the practical noise figure level. Thus, CNM structure cannot attain both input matching and minimum NF simultaneously.

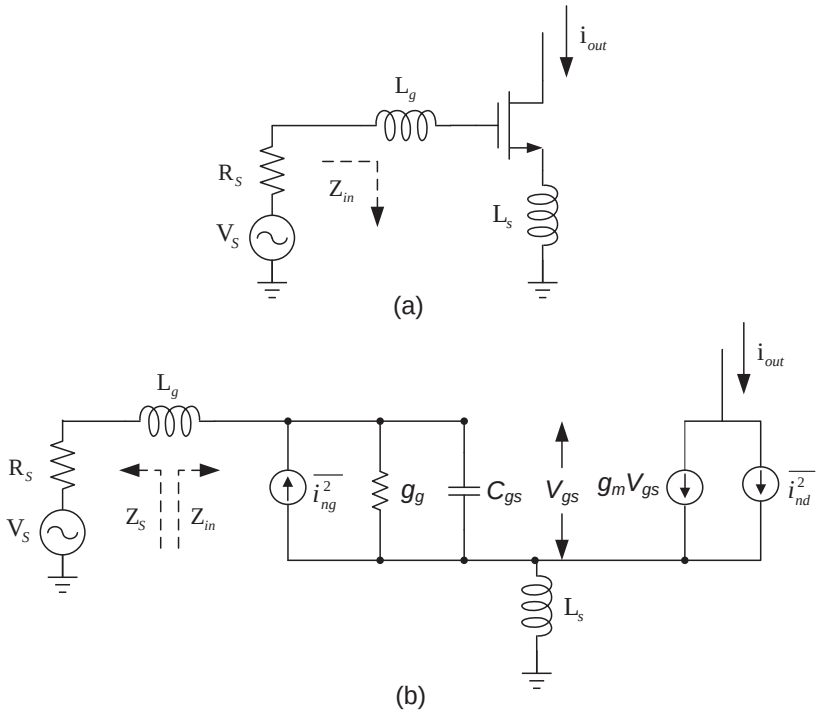


Figure 3-9: (a) Schematic of a CS LNA topology adopted to apply the SNIM technique and (b) its small-signal equivalent circuit

Instead of adding extra noise to the system, an inductive source degeneration matching configuration provides a perfect match with a source degeneration inductor L_s and external matching inductor L_g. This topology is nowadays widely used for narrow-band application and is known as simultaneous noise and input matching (SNIM), as shown in Figure 3-9(a) [57, 146]. The same analysis is carried out with its small-signal equivalent circuit in Figure 3-9 (b). The noise parameters can be acquired after a tedious derivation given by [57, 147, 148]:

$$F = 1 + \frac{1}{g_m^2 R_s}\left\{\gamma g_{d0}\left\{\left[1 + s^2 C_{gs}\left(L_g + L_s\right)\left(1 - \alpha|c|\sqrt{\frac{\delta}{5\gamma}}\right)\right]^2 - \left[\left(sC_{gs}R_s\right)\left(1 - \alpha|c|\sqrt{\frac{\delta}{5\gamma}}\right)\right]^2\right\} - \frac{\alpha\delta}{5}(1 - |c|^2)g_m\left(sC_{gs}\right)^2\left[R_s^2 - s^2\left(L_g + L_s\right)^2\right]\right\} \quad (3\text{-}39)$$

$$R_n = R_n^\circ = \frac{\gamma}{\alpha} \cdot \frac{1}{g_m} \tag{3-40}$$

$$Z_{opt} = Z_{opt}^\circ - sL_s \tag{3-41}$$

$$F_{min} = F_{min}^\circ = 1 + \frac{2}{\sqrt{5}} \frac{\omega}{\omega_T} \sqrt{\gamma\delta(1-|c|^2)} \tag{3-42}$$

The optimum noise impedance and transistor size can be calculated to meet the minimum NF given by[31]:

$$Z_{opt}^\circ = \frac{1}{Y_{opt}^\circ} \frac{\alpha\sqrt{\frac{\delta}{5\gamma}(1-|c|^2)} + j\left(1-\alpha|c|\sqrt{\frac{\delta}{5\gamma}}\right)}{\omega C_{gs}\left[\frac{\alpha^2\delta}{5\gamma}(1-|c|^2) + \left(1-\alpha|c|\sqrt{\frac{\delta}{5\gamma}}\right)^2\right]} \tag{3-43}$$

$$W_{opt} = \frac{3}{2} \frac{1}{\omega L C_{ox} R_S Q_{opt}} \approx \frac{1}{3\omega L C_{ox} R_S} \tag{3-44}$$

$$Q_{opt} = |c|\sqrt{\frac{5\gamma}{\delta}}\left[1 + \sqrt{1 + \frac{3}{|c|^2}\left(1 + \frac{\delta}{5\gamma}\right)}\right] \tag{3-45}$$

Comparing the noise parameters with superscripted zeros for the amplifier without degeneration, the parameters R_n and F_{min} remains the same as given in equation (3-35) and (3-37). Furthermore, the impedance looking through the input source can be expressed as:

$$Z_{in} = j\omega L_s + \frac{1}{j\omega C_{gs}} + \omega_T L_s \tag{3-46}$$

At the resonance frequency, where the inductance impedance cancels the capacitance impedance C_{gd}, equation (3-46) leaves only the last term and therefore is expressed by:

$$Z_{in}(\omega_0) = \omega_T L_s \tag{3-47}$$

$$\omega_0 = \frac{1}{\sqrt{(L_g + L_s)C_{gs}}} \tag{3-48}$$

The inductance term ($\omega_T L_s$) left in this expression indicates that there is no additional noise. With the additional L_s, the SNIM technique can achieve power and noise match at any value of Z_s. The quality factor derived from the equivalent model in Figure 3-4 (b) can be expressed as:

$$Q = \frac{\omega C_{gs}}{R_S} \tag{3-49}$$

3.3.3 LNA Design with Power Constraint

As mentioned previously, a choice is usually made between the optimal noise and input impedance matching. However, in practical design, in order to approach the desired lower noise performance, a noise figure expression with power consumption consideration must explicitly be taken into account. The SNIM can satisfy any desired power dissipation but with a worse noise performance. The power-constrained simultaneous noise and input matching (PCSNIM) technique (see Figure 3-10) has been used in recent LNA topology designs [57, 147, 148], and introduces an extra capacitor C_{ex}.

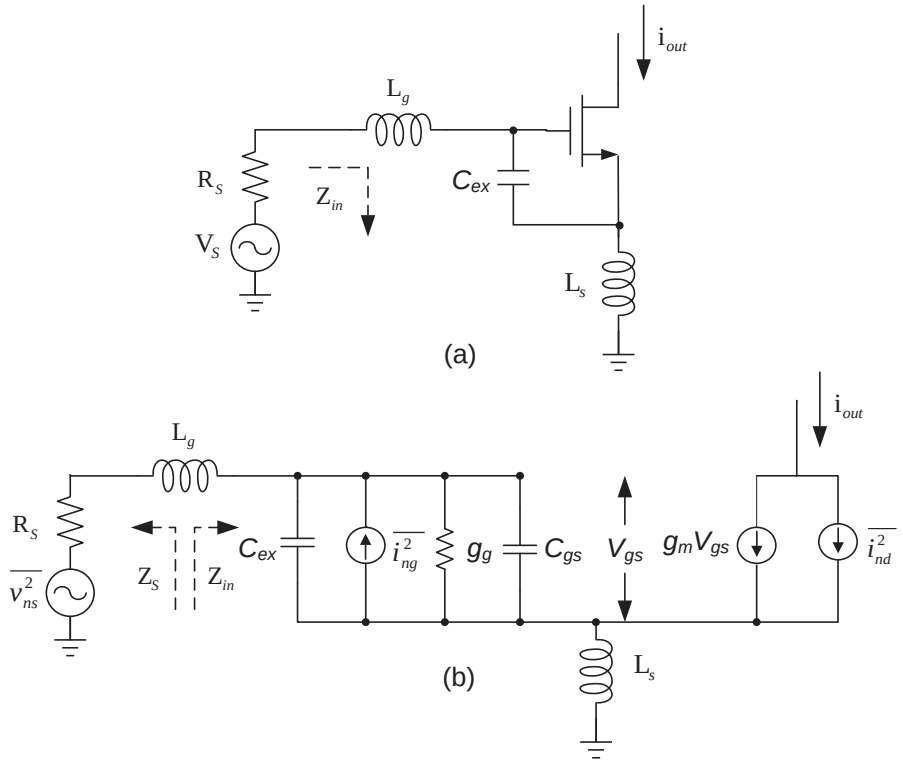


Figure 3-10: (a) Schematic of a CS LNA topology adopted to apply the PCSNIM technique and (b) its small-signal equivalent circuit

From equation (3-18) and (3-19), the induced gate noise current can be expressed as:

$$\overline{i_{ng}^2} = 4kT\delta_{eff}\frac{\omega^2 C_t^2}{5g_{d0}}\Delta f \tag{3-50}$$

where $\delta_{eff} = \delta\left(C_{gs}^2/C_t^2\right)$ and $C_t = C_{gs} + C_{ex}$. Following the same derivation, the noise factor for this topology is given by [57, 147, 148]:

$$F = 1 + \frac{1}{g_m^2 R_s}\left\{\gamma g_{d0}\left\{\left[1 + s^2 C_t\left(L_g + L_s\right)\left(1 - \alpha|c|\sqrt{\frac{\delta}{5\gamma}}\right)\right]^2 - \left[\left(sC_t R_s\right)\left(1 - \alpha|c|\sqrt{\frac{\delta}{5\gamma}}\right)\right]^2\right\} - \frac{\alpha\delta}{5}(1 - |c|^2)g_m(sC_t)^2\left[R_s^2 - s^2\left(L_g + L_s\right)^2\right]\right\} \tag{3-51}$$

$$R_n = R_n^\circ = \frac{\gamma}{\alpha}\cdot\frac{1}{g_m} \tag{3-52}$$

$$Z_{opt} = Z_{opt}^* - j\omega L_s \tag{3-53}$$

$$F_{min} = F_{min}^\circ = 1 + \frac{2}{\sqrt{5}}\frac{\omega}{\omega_T^*}\sqrt{\gamma\delta(1 - |c|^2)} \tag{3-54}$$

The noise parameter expressions R_n, Z_{opt} and F_{min} are not affected by the additional C_{ex} [57], but varied in Z_{opt}^* and ω_T^* given by:

$$Z_{opt}^* = \frac{\alpha\sqrt{\frac{\delta}{5\gamma}(1 - |c|^2)} + j\left(\frac{C_t}{C_{gs}} - \alpha|c|\sqrt{\frac{\delta}{5\gamma}}\right)}{\omega C_{gs}\left[\frac{\alpha^2\delta}{5\gamma}(1 - |c|^2) + \left(\frac{C_t}{C_{gs}} - \alpha|c|\sqrt{\frac{\delta}{5\gamma}}\right)^2\right]} \tag{3-55}$$

$$\omega_T^* = \frac{g_m}{C_t} \tag{3-56}$$

The input resistance can be rewritten as:

$$Z_{in} = j\omega\left(L_g + L_s\right) + \frac{1}{j\omega C_t} + \omega_T^* L_s \tag{3-57}$$

Consequently, the conditions that satisfy $Z_{opt} = Z_{in}$ and matching with the source impedance Z_S can be expressed as follows:

$$\mathrm{Re}\left[Z_{opt}\right] = \mathrm{Re}[Z_S] = \frac{\alpha\sqrt{\frac{\delta}{5\gamma}(1-|c|^2)}}{\omega C_{gs}\left[\frac{\alpha^2\delta}{5\gamma}(1-|c|^2) + \left(\frac{C_t}{C_{gs}} - \alpha|c|\sqrt{\frac{\delta}{5\gamma}}\right)^2\right]} \tag{3-58}$$

$$\mathrm{Im}\left[Z_{opt}\right] = \mathrm{Im}[Z_S] = \frac{j\left(\frac{C_t}{C_{gs}} - \alpha|c|\sqrt{\frac{\delta}{5\gamma}}\right)}{\omega C_{gs}\left[\frac{\alpha^2\delta}{5\gamma}(1-|c|^2) + \left(\frac{C_t}{C_{gs}} - \alpha|c|\sqrt{\frac{\delta}{5\gamma}}\right)^2\right]} - j\omega L_s \tag{3-59}$$

$$Re[Z_{in}] = Re[Z_S] = g_m\frac{L_s}{C_t} \tag{3-60}$$

$$\mathrm{Im}[Z_{in}] = -\mathrm{Im}[Z_S] = j\omega L_s + \frac{1}{j\omega C_t} \tag{3-61}$$

Therefore, for the given value of L_s, the imaginary value of the optimum noise impedance automatically becomes approximately equal to that of the input impedance with an opposite sign. The four indeterminate value V_{gs}, W, C_{gs}, L_s and C_{ex} provide arbitrary value of Z_S by fixing one of the design parameters value. This proves that with the additional capacitor C_{ex}, the PCSNIM can achieve any level of power dissipation compared with SNIM [57].

At the same time, L_s is given by following approximated relation:

$$L_s \approx \frac{\alpha\sqrt{\frac{\delta}{5\gamma}(1-|c|^2)}}{\omega\omega_T^* C_t} \tag{3-62}$$

Since a large value of L_s will significantly increase $F_{\min}$ [149], the required L_s from this deduced equation can be reduced because of the additional C_{ex} compared to SNIM.

3.3.4 Design with Finite Device Conductance for Low Power

The above derivations enable the possibility of approaching low power design for LNA. However, most of the derivations for NF and gain are based on neglecting the effects of finite transistor channel conductance (g_{ds}) and distributed gate resistance (R_g) [143, 150]. In following steps, all the components are taken into design consideration and the entire process is carried out again. The inductive source degenerated telescopic cascode topology is employed here since it has the advantage of current reusing and hence it consumes less bias current than the folded cascode topology, as shown in Figure 3-11[57]. An improved PCSNIM technique is adopted here for this telescopic cascode LNA's noise optimisation. The effect of the finite device conductance $g_{ds}(= 1/r_0)$, due to the deeply scaled short channel length, is included in this design optimization. With regard to the input impedance matching at resonance in equation (3-57), another expression for Z_{in} is given by:

$$Z_{in} \approx g_{m1}\frac{L_s}{C_t}\frac{g_{m2}}{g_{ds1}+g_{m2}} \qquad (3\text{-}63)$$

where g_{ds1} is the output conductance of M_1, while g_{m1} and g_{m2} are the trans-conductance of the cascode transistors M_1 and M_2, respectively.

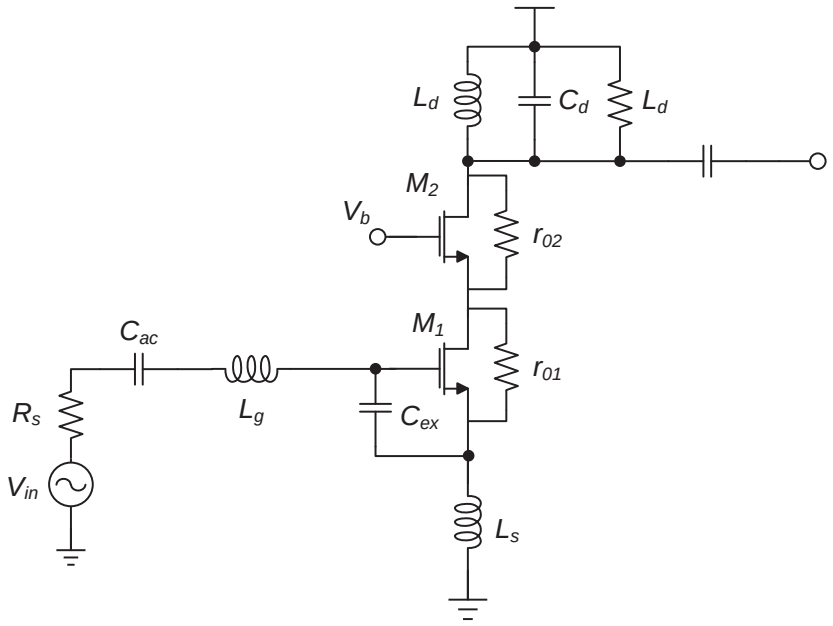


Figure 3-11: Proposed narrow-band circuit LNA topology for RFID front-end.

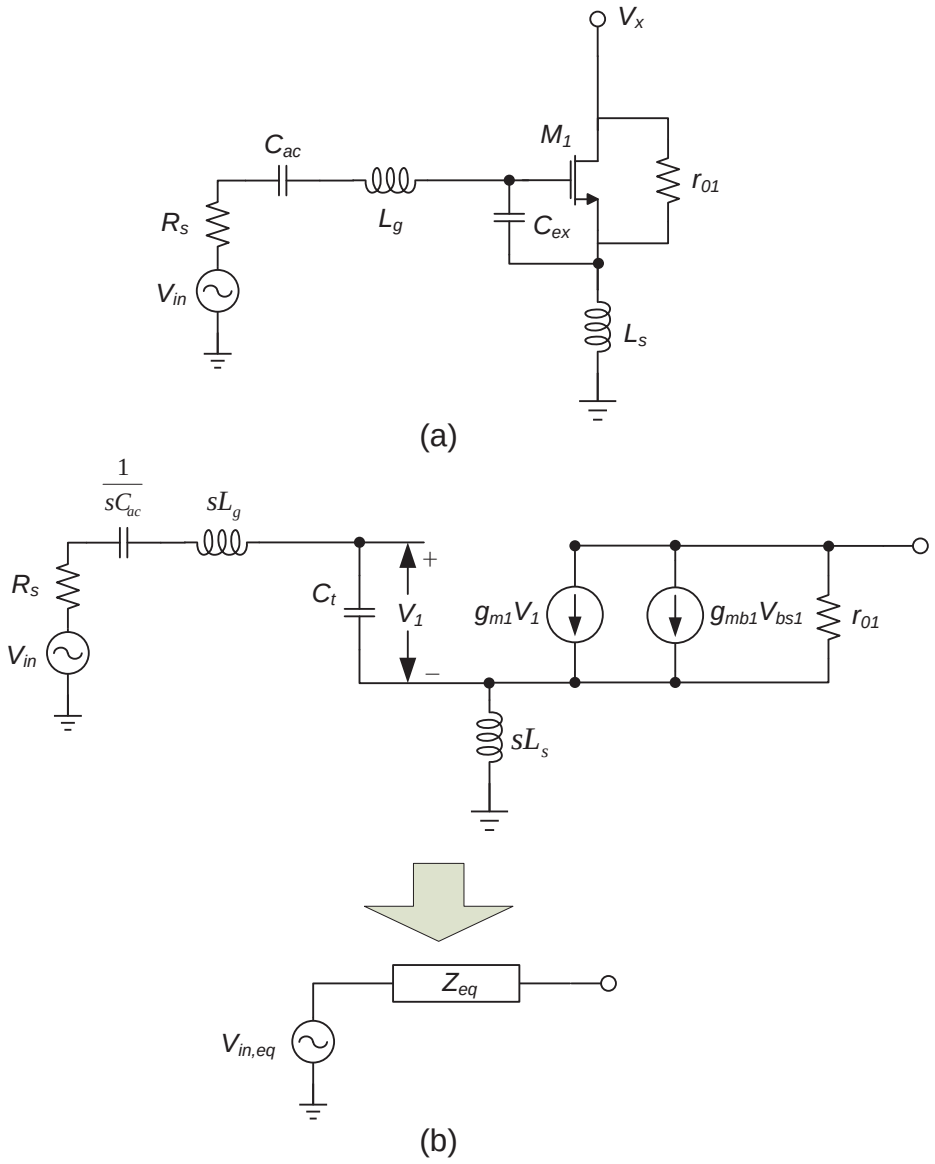


Figure 3-12: (a) Schematic of the CS LNA topology adopted to apply the PCSNIM technique and (b) its Thevenin equivalent circuit.

In order to evaluate the effect of g_{ds}, expressions for voltage gain and noise are necessary. The voltage gain for this topology can be calculated by applying the Thevenin equivalent circuit for the CS stage with M_1. As shown in Figure 3-12(b), the expression for equivalent output voltage $V_{in,eq}$ when it is in open circuit condition is given by:

$$V_1 = \frac{V_{in}}{sC_t\left[R_S + R_{ge} + R_{Lg} + R_{Ls} + s\left(L_s + L_g\right)\right]} \qquad (3\text{-}64)$$

$$V_{in.eq} = (R_{Ls} + sL_s) \cdot sC_t V_1$$

$$V_{in.eq} = \frac{R_{Ls} + sL_s}{R_S + R_{ge} + R_{Lg} + R_{Ls} + s(L_s + L_g)} \cdot V_{in} \tag{3-65}$$

here the R_{Lg} is the series resistance of the gate inductor, R_{Ls} is the series resistance of the source inductor and R_{ge} is an equivalent gate resistance due to the addition of C_e. For simplicity, the gate resistance R_g is not marked in the Figure 3-13. A detail derivation for finding the expression for R_{ge} is explained in Appendix 8-2. The expression shows that R_{ge} is smaller than the original gate resistance R_g of the transistor M_1, which is given by:

$$R_{ge} = R_g \frac{C_{gs1}^2}{C_t^2} \tag{3-66}$$

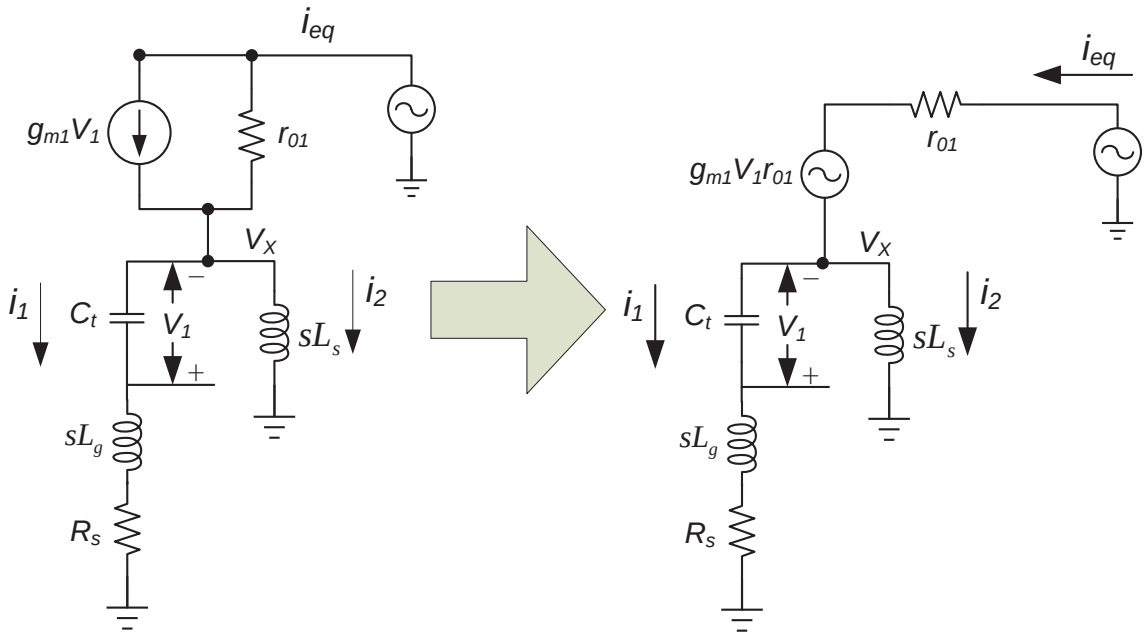


Figure 3-13: (a) The Thevenin equivalent circuit for finding $Z_{in.eq}$

The Thevenin equivalent output current is found when the output terminals are shorted. Alternatively, the voltage source V_{in} can be replaced with short circuits to calculate the equivalent resistance $Z_{in.eq}$ as demonstrated in Figure 3-14. Since $Z_{in.eq} = V_{eq} / i_{eq}$, $i_{eq} = i_1 + i_2$ and $i_1 = sC_tV_1$, therefore we have:

$$V_X = sC_tV_1\left(R_S + R_{ge} + R_{Lg} + sL_g + \frac{1}{sC_t}\right) \qquad (3\text{-}67)$$
$$= \left(\, i_{eq} - sC_tV_1\right)(R_{Ls} + sL_s) = V_{eq} - \, i_{eq}r_{01} + g_{m1}V_1r_{01}$$

Rearranging this equation give us:

$$Z_{in.eq} = \frac{V_{eq}}{i_{eq}} = (R_{Ls} + sL_s + r_{01}) \qquad (3\text{-}68)$$
$$- \frac{(R_{Ls} + sL_s)[g_{m1}r_{01} + sC_t(R_{Ls} + sL_s)]}{sC_t\left(R_S + R_{ge} + R_{Lg} + sL_g + \frac{1}{sC_t} + R_{Ls} + sL_s\right)}$$

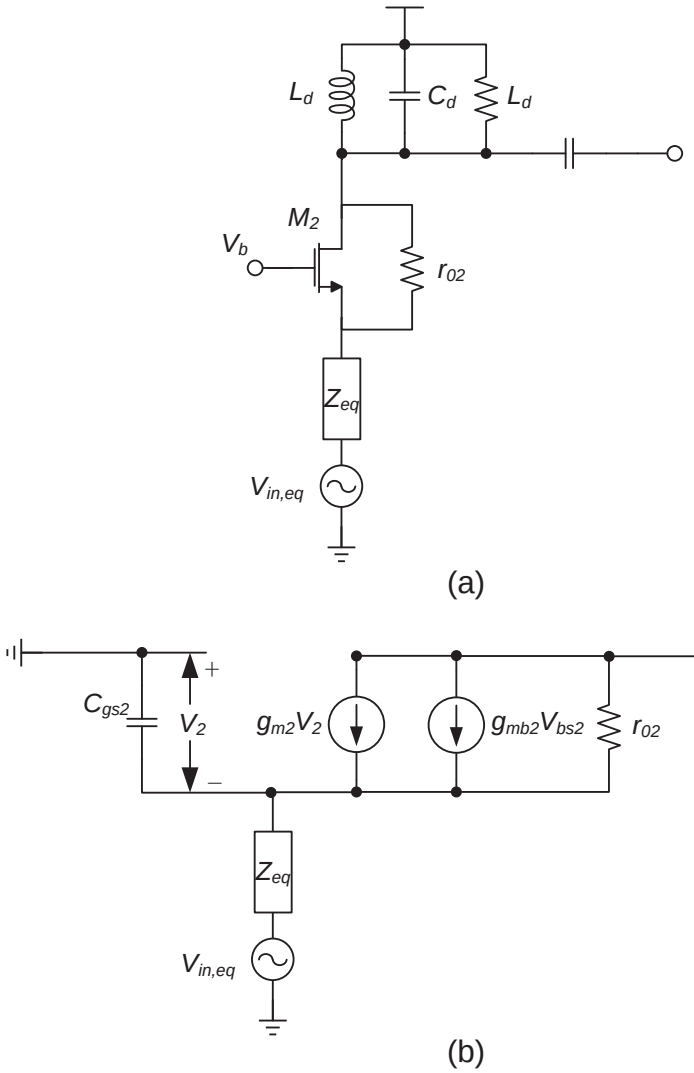


Figure 3-14: (a) Schematic of the CS stage with equivalent input impedance and voltage source and (b) its small signal equivalent circuit.

Redrawing the cascode topology at the CG stage with equivalent input source and finite output resistance, the circuit is demonstrated in Figure 3-14 (a). From its small-signal equivalent circuit in Figure 3-14 (b), noting that the current flowing through $Z_{in.eq}$ is equal to $-V_{out}/Z_d$ and here the load impedance Z_d is formed by a RLC tank tuned at resonance frequency, which equals to $\frac{1}{sC_d}\Big\| sL_d \| R_d$. Tracking with current flow direction, following expression can be achieved as:

$$V_2 - \frac{V_{out}}{Z_d} Z_{in.eq} + V_{in.eq} = 0 \tag{3-69}$$

Furthermore, the current through r_{02} is equal to $-V_{out}/Z_d - (g_{m2} + g_{mb2})V_2$, therefore V_{out} can be rewritten by:

$$V_{out} = -\left[\frac{V_{out}}{Z_d} + (g_{m2} + g_{mb2})V_2\right] r_{02} - \frac{V_{out}}{Z_d} Z_{in.eq} + V_{in.eq} \tag{3-70}$$

Upon the substitution for V_2 from Equation 1-32 and 1-33, the expression reduces to:

$$\frac{V_{out}}{V_{in.eq}} \approx \frac{(g_{m2} + g_{mb2})r_{02} + 1}{r_{02} + [(g_{m2} + g_{mb2})r_{02} + 1]Z_{in.eq} + Z_d} \cdot Z_d \tag{3-71}$$

The total gain for the completed cascode CS CG topology is given by:

$$\frac{V_{out}}{V_{in}} \frac{g_{m2}r_{02} + 1}{r_{02} + g_{m2}r_{02}Z_{in.eq} + Z_{in.eq} + Z_d} \cdot Z_d \cdot \frac{sL_s}{R_S + R_{ge} + R_{Lg} + R_{Ls} + s(L_s + L_g)} \tag{3-72}$$

Assuming both transistors in saturation with same transistor width and length will give $r_{02} \approx r_{01}$, $g_{m2} \approx g_{m1}$, $g_{m2}r_{02} \gg 1$ and $g_m \gg g_{mb}$. The above equation can be further simplified as:

$$\frac{V_{out}}{V_{in}} \approx G_m Z_{out} \tag{3-73}$$

$$\frac{\left[g_{m1}+\frac{(sC_t+g_{m1})(R_{Ls}+sL_s)}{r_{01}+R_{Ls}+sL_s}\right]\cdot Z_d}{\left[1+sC_t\left[R_S+R_{ge}+R_{Lg}+R_{Ls}+s\left(L_s+L_g\right)\right]+\frac{(sC_t+g_{m1})r_{01}(R_{Ls}+sL_s)}{r_{01}+R_{Ls}+sL_s}\right]}$$

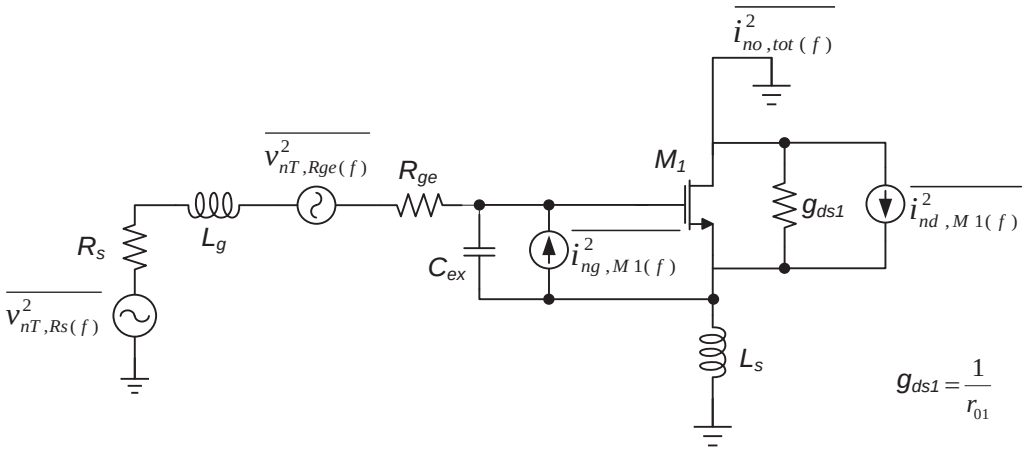


Figure 3-15: Proposed noise inserted circuit diagram for noise model

Figure 3-15 shows the noise inserted circuit diagram of the RFID LNA front-end, which accounts for the major noise components contributing to the short circuit output noise current at the drain of M_1. Thermal noise of resistors, along with drain current noise and induced gate noise, contribute significant noise components in the LNA circuit. The technique based on determining the short circuit output noise current power at the drain of M_1 was used for the noise analysis. In this method the output load is shorted since the noise factor is defined as the ratio of the total mean-squared output noise current due to all the noise sources to the input source only. As the noise factor mostly depends on the front-end noise sources farthest from the output load, almost the same value of noise factor is obtained by using this technique without the extra calculation, compared to the output noise current with load. Hence, the noise factor of the front-end noise sources using this short circuit output noise current method, are added to obtain the overall frequency behaviour of the NF, which is given by:

$$F = 1+\frac{\alpha\delta}{5}\frac{s^2C_{gs1}^2}{R_s g_{m1}}\frac{A^2-B^2}{(r_{01}^2-s^2L_s^2)D^2}+\frac{\gamma g_{m1}}{\alpha R_s}\frac{r_{01}^2C}{D^2} + 2|c|\frac{sC_{gs1}r_{01}}{R_s D^2}\sqrt{\frac{\delta\gamma}{5}\frac{A^2-B^2C}{(r_{01}^2-s^2L_s^2)}} \qquad (3\text{-}74)$$

$$A = g_{m1} r_{01}^2 R_s + s^2 L_s \left[L_s + g_{m1} r_{01} \left(L_g + L_s \right) \right] \quad (3\text{-}75)$$

$$B = s r_{01} \left[L_s (1 + R_s g_{m1}) + g_{m1} r_{01} \left(L_g + L_s \right) \right] \quad (3\text{-}76)$$

$$C = \left[1 + s^2 C_t \left(L_g + L_s \right) \right]^2 - s^2 C_t^2 R_s^2 \quad (3\text{-}77)$$

$$D = s C_t (s L_s + g_{m1} r_{01} / s C_t) \quad (3\text{-}78)$$

This expression includes device drain-source conductance g_{ds} that provides a more accurate estimate of the noise factor.

3.3.5 Design of Baluns for Differential Approach

It is clear that power consumption performance consideration encourages single-ended architecture, but in this case, the package parasitic components become much more important in affecting the overall performance. This problem is not impossible to solve, but it adds another level of risk that must be fully comprehended before selecting the input stage architecture. A matching network case study is presented in chapter III by applying a microstrip transmission line externally. The simulation's result is investigated in order to define the trade-offs between its critical performance parameters.

Practical communication transceiver applications utilise differential signals, whereas antenna connectivity is single-ended. Therefore, balun circuits needs to be employed to transform between the singled-ends and differential forms. Nowadays, these devices are more likely implemented on-chip since off-chip solutions are much more expensive operating at micro-millimetre wave frequencies. The GaAs MESFET balun proposed by Ma et al. in 1998 [77] used an asymmetrical feedback LCR network to improve differential pair phase-splitting performance to within $\pm 1 dB$ difference in amplitude and $\pm 1°$ phase difference. This kind of structure has a limitation on wide band performance since its resonance is highly dependent on circuit parasitic components, which also rely on supply voltage and the biasing point of the circuit. Nevertheless, it fits perfectly for narrow-band application. The details of implementing this balun are discussed in the Chapter 4.

3.4 Mixer Design Topologies and Methodologies

Active mixers are able to provide higher conversion gain at the cost of a higher noise figure and lower bandwidth compared to passive mixers. Conversion gain is critical in receiver design because it reduces the number of amplifiers after the mixer.

3.4.1 The Conventional Gilbert Mixer Structure

Active mixers are amplitude-nonlinear above a certain input level resulting in a gain compression characteristic. Most mixers have the 1dB compression point specified at the input, such as the signal-tone input signal level at which the output of the mixer has fallen 1dB below the expected output level. For a typical double balanced mixer, this figure is approximately 6dB below the LO power level. The 1dB compression point gives rise to the dynamic range of the mixer, which is the difference between the 1dB compression and the minimum discernible signal (MDS – this is dependent on the noise floor of the device).

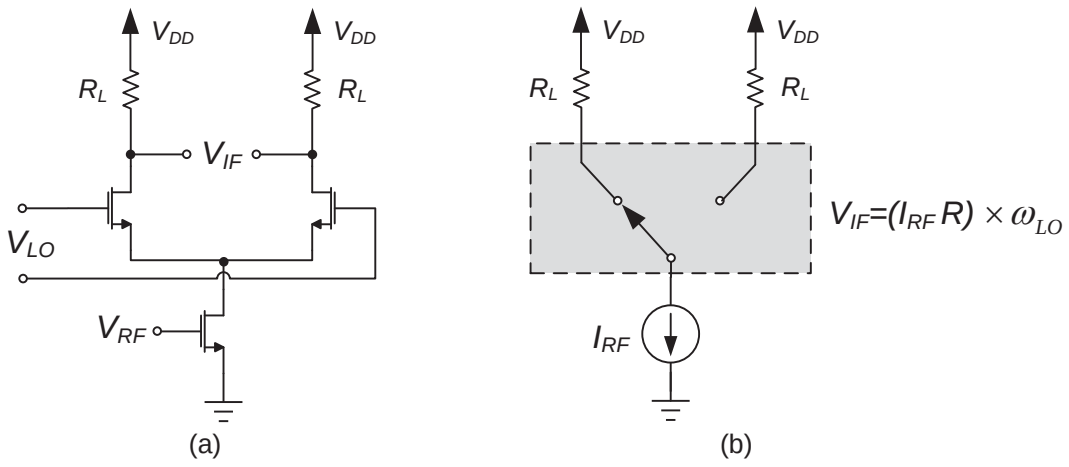


Figure 3-16: Single-balanced FET mixer (a) topology and (b) its switching equivalent circuit

In order to provide better isolation between LO-to-RF and RF-to-IF, a single-balanced mixer is proposed in Figure 3-16. Similar to the dual-gate FET mixer, the bottom

transistor is the trans-conductor that converts the incoming RF voltage into current. Large LO signals drive the current from the trans-conductor into the pair branches alternately. The tail RF current is multiplied by a square-wave from LO. This current domain mixing action is known as current-commutating mixer. The ideal square-wave under switching action can be represented as:

$$f_{square\ wave}(t) = \frac{4}{\pi}cos(\omega_{LO}t) - \frac{4}{3\pi}cos(3\omega_{LO}t) + \frac{4}{5\pi}cos(5\omega_{LO}t) \qquad (3\text{-}79)$$

The common-mode signals generated by the differential switching pair cancels the even-order harmonic components. Therefore, the current through the IF load is:

$$I_{IF} = [I_{DC} - g_m V_{RF} cos(\omega_{RF}t)] f_{square\ wave}(t)$$
$$= \frac{4}{\pi} I_{DC} cos(\omega_{LO}t) - \frac{2}{\pi} g_m V_{RF}[cos(\omega_{RF} - \omega_{LO})t + cos(\omega_{RF} + \omega_{LO})t] + \cdots \qquad (3\text{-}80)$$

Hence, the mixer trans-conductance is therefore given by:

$$G_c = \frac{2}{\pi} g_m \qquad (3\text{-}81)$$

From equations 3-80 and 3-81, it can be observed that the LO-to-IF still has the isolation issue as the switching-pair modulates the DC current with the LO and thus there is no LO noise rejection. The odd-order LO harmonic components still appear in the output that we need to filter out. Nevertheless, both the common-source trans-conductor and differential pair, which acts as a virtual ground to the LO signal provides good isolation between RF and LO. It is thus applied in some receiver systems [108-110].

Since a single-balanced FET mixer has the drawbacks of low LO-to-IF isolation and being sensitive to supply fluctuation, the Gilbert cell mixer was proposed in 1960s and quickly dominated CMOS receiver design. The Gilbert cell mixer's high conversion gain, compact structure, and high isolations make it the backbone of most of mixers we have today.

A typical Gilbert mixer consists of several stages, as presented in Figure 3-17. The trans-conductance stage, formed by transistors M_1 and M_2, converts differential RF input voltage into RF current. Similar to the single-balanced mixer, the RF current is further multiplied by a square-wave LO signal in the mixing stage. The balanced mixing stage enables the LO signal to be cancelled while the IF signal appears differentially at the output. Consequently, a high LO-to-IF isolation can be achieved.

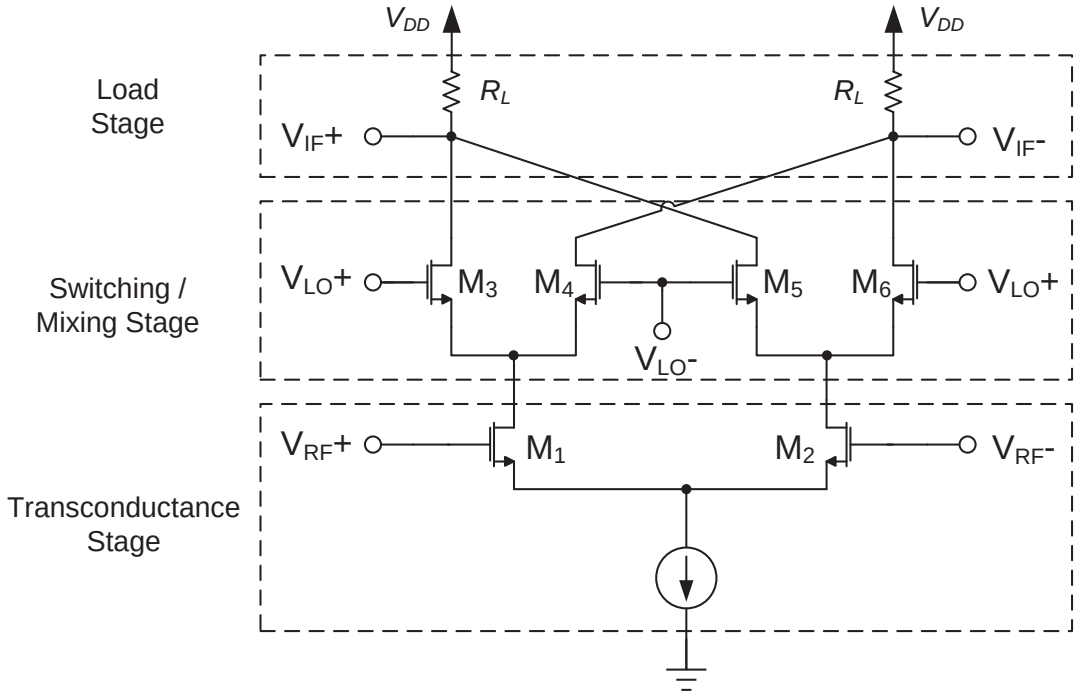


Figure 3-17: Conventional Gilbert mixer topology

RF signals are as shown in $V_{RF\pm}(\mathrm{t}) = \pm V_{RF} cos(\omega_{RF} t)$ and LO signals are shown as

$$V_{LO\pm}(t) = \pm V_{LO} cos(\omega_{LO} t) \quad (3\text{-}82)$$

RF voltage signals transfer to current signals as presented as:

$$I_{M1} = I_{DC} + g_{m1} V_{RF} cos(\omega_{RF} t) \quad (3\text{-}83)$$

$$I_{M2} = I_{DC} - g_{m2} V_{RF} cos(\omega_{RF} t) \quad (3\text{-}84)$$

Therefore, the output IF current is now expressed as if $g_{m1} = g_{m2}$:

$$I_{IF} = I_{IF+} - I_{IF1} = (I_{M3} + I_{M5}) - (I_{M4} + I_{M6}) = (I_{M3} - I_{M4}) - (I_{M6} - I_{M5})$$
$$= I_{M1} \times f_{square\ wave}(t) - I_{M2} \times f_{square\ wave}(t) = (I_{M1} - I_{M2}) \times f_{square\ wave}(t)$$
$$= 2g_m V_{RF} cos(\omega_{RF} t) \times f_{square\ wave}(t) \quad (3\text{-}85)$$

Separate $f_{square\ wave}(t)$ with Fourier series as above and neglect higher harmonics, we obtain:

$$I_{IF} = I_{IF+} - I_{IF1} \approx \frac{4}{\pi} g_m V_{RF} [cos(\omega_{RF} - \omega_{LO})t + cos(\omega_{RF} + \omega_{LO})t] \quad (3\text{-}86)$$

Therefore, the voltage conversion gain can be represented with a load resistor as:

$$G_c = \frac{2}{\pi} g_m R_L \quad (3\text{-}87)$$

The overall Gilbert mixer linearity is controlled by the trans-conductance stage if the LO-driven transistors act as good switches. However, the switching process from the trans-conductance stage also contributes most of the noise in the Gilbert mixer and some modifications are necessary to overcome this noise issue.

3.4.2 Noise and Noise Reduction Techniques in Gilbert Mixer Design

Unlike in the LNAs, the noise figure definition in the mixer is often confused due to the existence of the image signals. The image signal and the expected signal are also called sidebands in mixers. The SSB is assumed to be the only noise from the expected signal frequency and not the image frequency, but the DSB evaluates both sidebands as a result of twice as much power available at the IF port compared to the SSB signal.

However, the intuitive view of the noise in the mixer includes both the flicker and the thermal noise dominating the separate frequency bands as is the situation in LNAs. At low frequency, the flicker noise at the trans-conductors appears in down-conversion mixing, which translates the flicker noise to ω_{LO} and its harmonics. Due to the

mismatch of the switching, small amount of flicker noise appears in the output without frequency translation. In addition, the IF loads will also contribute a certain amount of flicker noise. Therefore, PMOS load is preferred in some designs since it has less flicker noise as compared to an NMOS load[151]. Even if the switches perform perfect switching at the zero-crossing, the noise voltage that is superimposed onto the ω_{LO} signal affects the switching time[152]. The flicker noise will add current impulses with amplitude of $2I$ at a frequency $2\omega_{LO}$ with a pulse train of random widths change in switching time Δt. The average value of the output current over one LO period (T_{LO}) is

$$i_{o,n} = \frac{2}{T_{LO}} \times 2I \times \Delta t = 4I \frac{v_n}{ST_{LO}} \tag{3-88}$$

Where, S is the slope of the LO at the zero-crossing. From the expression, it is clear that the switch flicker noise appears at the output without any frequency translation and it decreases when the slope increases and/or the bias current decreases. The zero-crossing modulation, Δt, depends on the low-frequency noise v_n and the voltage slope S can be increased by enlarging the LO power. Secondly, increasing the gate area of transistor in the mixing stage can also reduce the v_n.

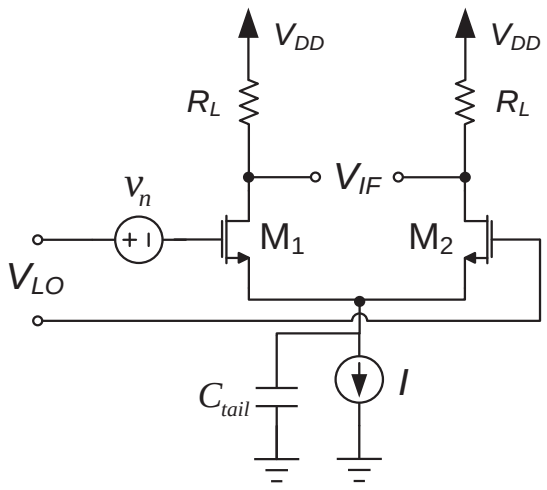


Figure 3-18: Single-balanced mixer with switch noise

From an indirect point of view, the output flicker noise appears via another mechanism, which depends on the LO frequency and the circuit tail capacitor C_{tail} [152]. C_{tail} is

charged up exponentially by the noise voltage during half of the cycle with the same frequency as LO. The output noise current therefore can be expressed as:

$$i_{o,n} = \frac{2C_{tail}}{T_{LO}} \cdot v_n \cdot \frac{(\omega_{LO} C_{tail})^2}{g_m{}^2 + (\omega_{LO} C_{tail})^2} \quad (3\text{-}89)$$

Therefore, when tail capacitance dominates, flicker noise can be reduced by using larger switching transistors, which have large LO power. If the capacitance is dominated by the switching trans-conductor's junction (g_m) capacitance, larger switch size can lower the flicker noise.

At high frequency, the noise still involves the same three source from the switches, the IF loads and the trans-conductors. The thermal noise of the switches can be referred to as the differential. The sampling function of impulse train can be given by

$$p(\omega_{LO} t) = \sum_n G_m \left(t - \frac{nT_{LO}}{2} \right) \quad (3\text{-}90)$$

where switching trans-conductance G_m have a period twice of the LO frequency, since there are two zero-crossing over at each LO cycle. The mixer output current thus yields to

$$i_{o,n} = p(\omega_{LO} t) \cdot v_n(t) \quad (3\text{-}91)$$

which appears as white noise and cyclostationary characteristic. When the LO waveform is a sine-wave with slope S equal to twice of LO amplitude (A_{LO}), the power spectral density of the noise current at the output due to one switch is

$$\overline{|i_{o,n}|^2} = 4kT\gamma \frac{I}{\pi A_{LO}} \quad (3\text{-}92)$$

Expression 3-92's output is dependent on the bias current and LO amplitude and demonstrates that there is no effect of switch size when C_{tail} is negligible. In Practical applications, large C_{tail} does affect the gain of the mixer at high frequency.

Nevertheless, it increases the noise figure since direct translation causes the drain noise current flow into a finite C_{tail} impedance when only one switch is "on". Furthermore, the thermal noise of the trans-conductors around each odd order harmonic of the LO signal translates to IF similar to the RF signal [153]. Noticeably, the thermal noise around the even order harmonic is cancelled out in balanced topology. Therefore, the Gilbert mixers produce large amount of noise.

A number of different techniques are proposed to reduce both the flicker noise and the thermal noise. As discussed, the switches contribute most of the flicker noise; therefore, in order to reduce flicker noise of the switches, both large LO power and low overdrive voltage can be used. The current bleeding techniques are widely adopted for Gilbert mixers to maintain high conversion gain and minimum bias current for the mixing stage [154-158]. The current bleeding is also known as charge-injection method that provides extra current for the trans-conductance stage, as shown in Figure 3-19. Most of the RF signal will be forced into entering switching pairs since current source has large output impedance. However, the drawback of the current source is an increment in the tail capacitance, which amplifies the flicker noise indirectly. This issue has been discussed and resolved in the literature [155, 156]. The same method of using inductor degenerated topology in LNA design can be applied here by resonating out the tail capacitance to reduce the flicker noise. Therefore, the current bleeding technique and inductor degenerated topology is often used simultaneously to reduce overall flicker noise and enhance conversion gain for the mixer.

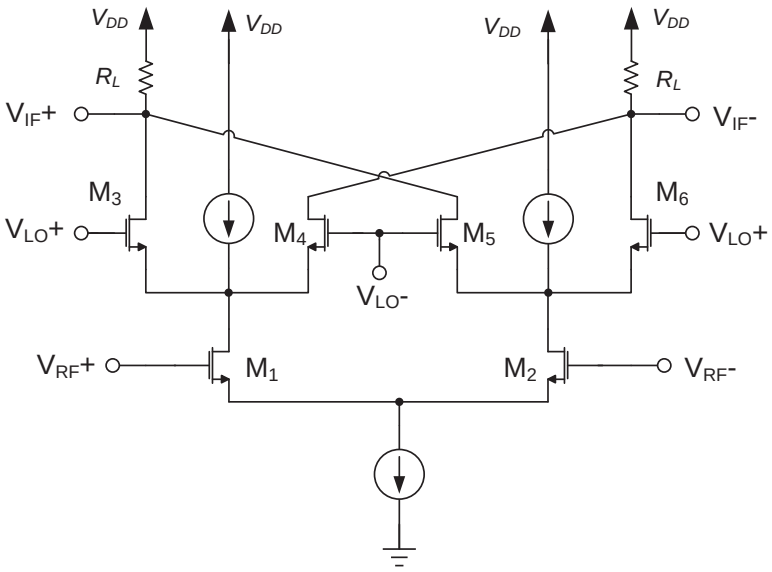


Figure 3-19: Gilbert mixer with current bleeding technique

In terms of the thermal noise, trans-conductors contribute the majority of it. Thus, this noise can be reduced significantly by replacing the trans-conductors with the proposed LNA's topology, as discussed previously. Current bleeding technique also reduces the noise contribution of the switching stage since the DC current gets smaller.

3.4.3 Low Power and Low Noise Design in Gilbert Mixer Design

The proposed topology uses both current bleeding technique and PCSNIM techniques as illustrated in Figure 3-20. This topology can reduce the current in the mixing stage and resonate out the large tail capacitance. Current bleeding and PCSNIM techniques provide freedom of control at low power dissipation and low noise figure at operating frequency.

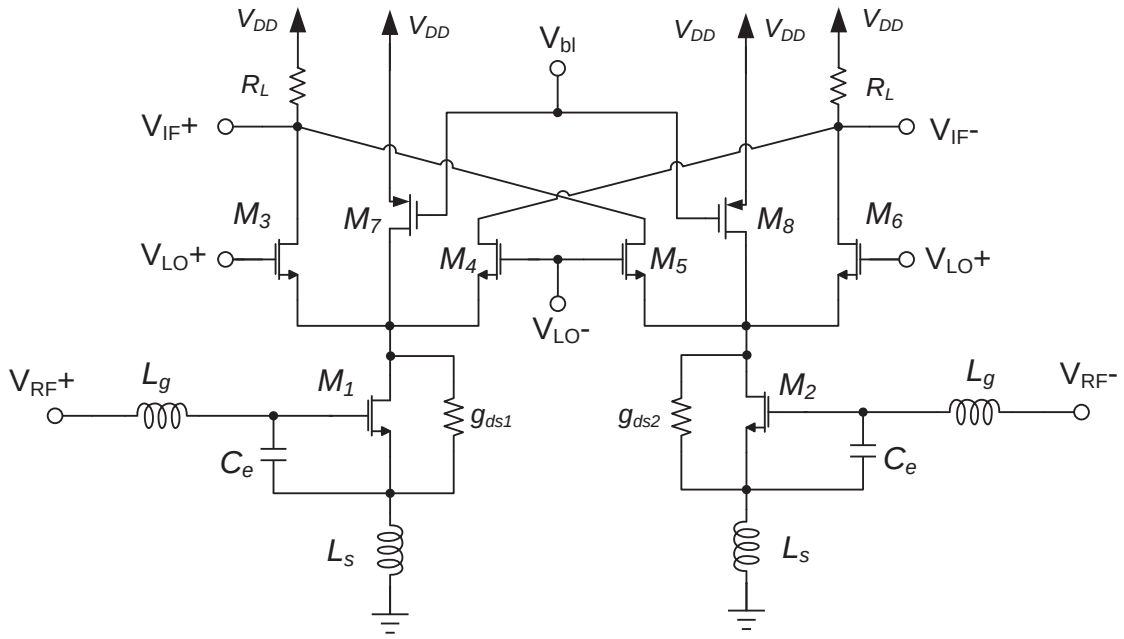


Figure 3-20: Proposed low-noise mixer

The current-reuse bleeding technique here improves the conversion gain and linearity. The PMOS transistors M_7 and M_8 are used as the bleeding current sources. The conversion gain improves as the bleeding ratio increases because of efficient LO

switching and increased trans-conductance in the drive stage. As the bleeding ratio increases, the drain-source voltage of the input transistor M_1 increases and the input transistor obtain higher drain voltage leading to higher linearity [154, 159]. In order to maximise the gain, most of the DC current needed for the low noise trans-conductance stage is driven by the current bleeding PMOS.

To achieve low power consumption, the trans-conductance stage is replaced with PCSNIM LNA, which has finite g_{ds} and reduces the trans-conductance's transistors size. Although this approach will trade at the cost of increased gate and source inductor sizes, which must be kept as small as possible to maximise the Q value. Since the Q factor in standard CMOS technology is not very high, the PCSNIM's reduction in power consumption consequently increases the inductor sizes to unreasonable on-chip implementation sizes. The involvement of g_{ds} brings a certain freedom for lower power consideration. Furthermore, the PCSNIM technique also reduces the size of the PMOS transistors M_7 and M_8 since heavy bleeding is no longer required.

Since the noise figure will have similar behaviour as the proposed LNA, the earlier tedious derivation is not repeated here. The detailed implementation will be explained in the Section 4.2.

3.4.4 Single-sideband Quadrature Mixer Design

When a mixer is used in frequency translation, output signals have spectral components at the sum and difference frequencies as explained in equation (3-85). A SSB mixer is preferred since it removes the unwanted side-band and prevents it from interfering with other transmissions and image signal. Moreover, either the lower sideband or the upper sideband can be selected by exchanging the in-phase (I) and quadrature-phase (Q) inputs. This procedure can be explained by the Hartley architecture in Figure 3-21 (a) and its graphical analysis in Figure 3-21 (b). In general terms, two periodic waveforms whose phase difference is 1/4 of their output period are said to have a quadrature phase relationship. A composite signal described by its envelope-and-phase form can be decomposed to an equivalent quadrature carrier (I and Q) form as:

$$V_{sig} = I(t) \cdot sin(2\pi ft) + Q(t) \cdot cos(2\pi ft) \quad (3\text{-}93)$$

where

$$I(t) = A(t) \cdot cos[\emptyset(t)] \quad (3\text{-}94)$$

and

$$Q(t) = A(t) \cdot sin[\emptyset(t)] \quad (3\text{-}95)$$

where $A(t)$ and $\emptyset(t)$ represent the amplitude and phase modulation for the carrier signal. The component $Q(t)$ that is in the same phase with the original carrier is reffered to as the in-phase component. The other component $I(t)$, which is always 90° out of phase to $Q(t)$ is referred as the quadrature component. In a quadrature system, the mixing is performed with both I and Q LO signal, generating two IF signals also in I and Q format.

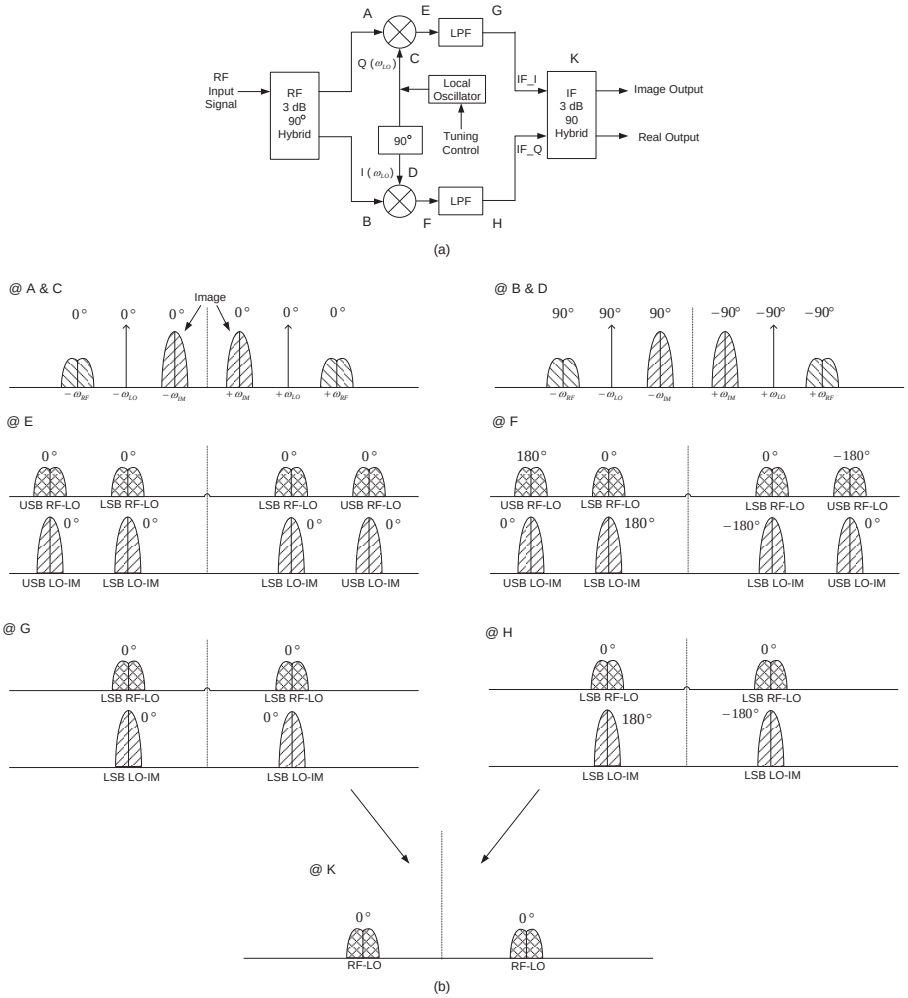


Figure 3-21: (a) Single-sideband Frequency Translation in Hartley architecture and (b) its graphical analysis of Spectrum demonstration cancellation of USB and Image-rejection.

The noise figure for the quadrature mixer is contributed from both of the image band and the signal band. With ideal switching, the noise from the mixing stage is often negligible. Therefore, the total output-referred noise of a system using a pair of conventional Gilbert mixer and the quadrature mixer yields to [160, 161]:

$$\overline{v_n^2} = 16kTR_L\left[\frac{16}{3\pi^2}g_{m,RF}R_L + 1\right] \quad (3\text{-}96)$$

$$\overline{v_{nq}^2} = 16kTR_L\left[\frac{4}{3\pi^2}\left(g_{m,RF} + g_{m,LO}\right)R_L + 1\right] \quad (3\text{-}97)$$

From the above expression, the noise performance of the quadrature mixer shows the advantage in trans-conductor terms but a flaw in the mixing stage. They will have similar noise performance when the overdrive voltage of the trans-conductor transistors is equal to the average overdrive voltage of the mixing stage transistors. When mixing stage transistors are small enough to minimise the LO drive power dissipation, the noise performance of the quadrature mixer is improved relative to a conventional Gilbert mixer. The completed proposed quadrature mixer design with PCSNIM, finite g_{ds} and current bleeding techniques is presented in Figure 3-22.

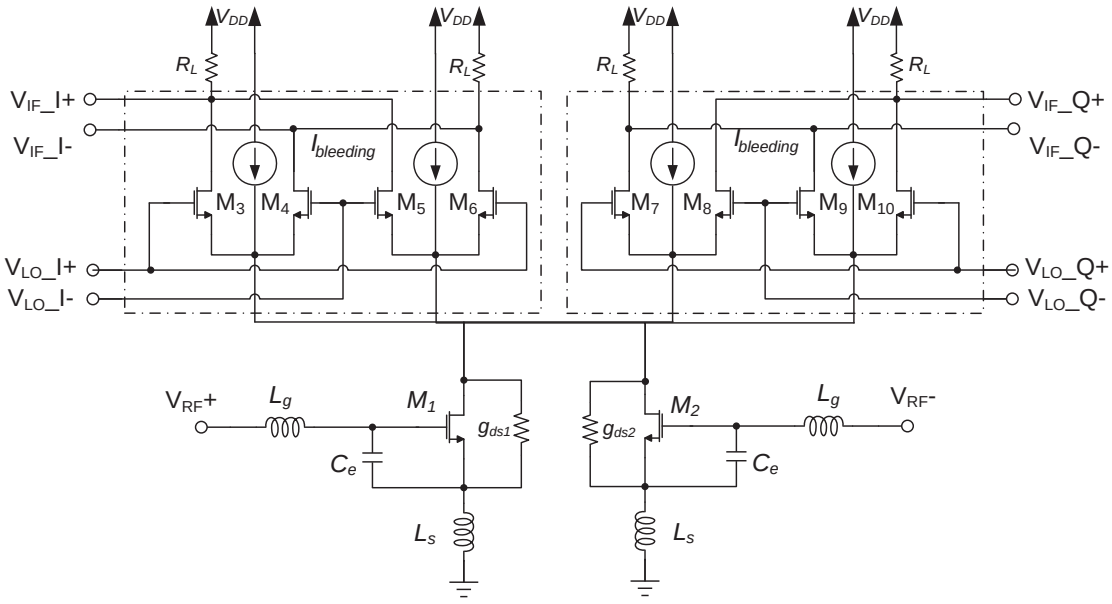


Figure 3-22: Proposed low-noise quadrature Gilbert mixer

3.5 VCO Design Topologies and Methodologies

Voltage control oscillator (VCO) consumes significant power in a receiver's front end. Therefore, balancing the trade-off among the power consumption, tuning range, tuning gain and phase noise is the key indicator of a good VCO design. The important elements that determine the phase noise of an oscillator are the material, transistor's flicker noise corner frequency, the loaded Q of the resonator and the final signal to noise ratio [31, 118, 120].

However, VCOs are difficult to implement in SoC due to the temperature and process variations of the active components. Any unexpected fluctuations at the output of VCO can express jitter and phase noise [118, 162]. They will directly impact on the system performance since timing accuracy is important for phase alignment and the signal-to-noise ratio can be highly degraded when frequency is translated. Therefore, a good performance VCO should also have low phase noise and high frequency stability.

Most common VOC circuits, e.g. [113, 115, 123], are based on the Colpitts and Clapp oscillators. Compared to other type of oscillators, the Colpitts and Clapp VOCs suffer higher levels of jitter due to lower Q-factor, but have the advantages of no off-chip components, e.g. crystal, and larger tuning ranges. Ideally, an oscillator is a perfectly lossless resonant circuit; however, lossless passive components are impossible to realise. In order to overcome the energy loss issue, practical oscillators can be designed by using the finite Q of practical resonators with power compensation of active elements. A structure on Figure 3-23 is constructed to form a negative impedance converter (NIC). It can be achieved with a simple op-amp circuit that employs both positive and negative feedback. If ideal op-amp behaviour is assumed, the input impedance can be easy obtained as follows:

$$Z_{in} = \frac{Z_f}{1 - A} \qquad (3\text{-}98)$$

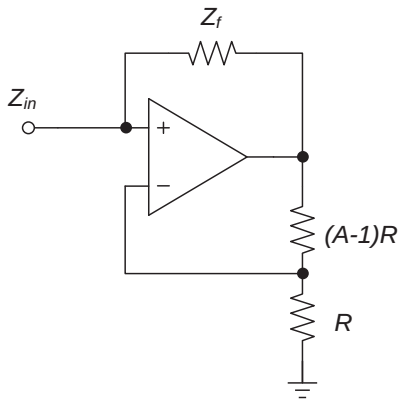


Figure 3-23: Feedback System formed by a negative impedance converter (NIC) and its system diagram

If the closed-loop gain is equal to two, then feedback impedance gives an algebraic inverse of the input impedance. Put differently, if the feedback impedance is a pure positive resistance then the input impedance will be a purely negative resistance. This negative resistance may be used to offset the positive resistance of all practical resonators to produce an oscillator. Finally, those popular oscillator configurations (e.g. Colpitts, Pierce, Clapp, etc.) may themselves be viewed as negative resistance resonators.

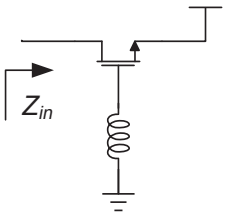


Figure 3-24: a NIC formed by a common-gate configuration with inductance attached to the gate.

A more practical negative resistance is easily obtained by exploiting the MOSFET parasitic effect. As shown in Figure 3-24, a common-gate configuration with inductance in the gate can cause a negative resistance to appear at the source terminal. If C_{gd} is negligible, then Z_{in} has a negative real part when frequencies are greater than the resonant frequency of the inductor and C_{gs}. For frequencies larger than the resonant frequency but smaller than ω_T, the real part of Z_{in} is approximated by:

$$R_{in} \approx -\frac{\omega^2 L}{\omega_T} = -\frac{\omega}{\omega_T}|Z_L| \qquad (3\text{-}99)$$

3.5.1 LC tank Voltage Controlled Oscillators

Since this circuit can easily achieve a negative resistance, its application is very extensive. The LC tank voltage controlled oscillator recurred in recently applications use a cross-coupled differential pair to achieve negative resistance, as shown in Figure 3-25(a) [116, 163, 164]. Arguably the most common RFID oscillator type, the LC VCO has outstanding high frequency phase noise and jitter performance. Two cross-coupled transistors produce the negative resistance $\frac{1}{g_m}$. Inductor and capacitances act as LC tank and the oscillating frequency can be easily obtained as $\omega_0 = \frac{1}{\sqrt{L_p C}}$, where $L_p = L_S\left(1 + \frac{1}{Q^2}\right)$. Hence, the value of negative resistance provided by the cross-coupled NMOS transistor is equal to $-R_P = -Q\omega_0 L_p$

In order to tune the frequency more precisely, the capacitance is often replaced by a varactor, as shown in Figure 3-25(b). Varactors are also widely applied in phase shifters, tuneable filters, and PLLs' design. Improving the tuning-control linearity of varactors enhances the PLLs' phase shifting and consistence of loop dynamics accuracy. The implementation for the varactor is carried out in following chapter.

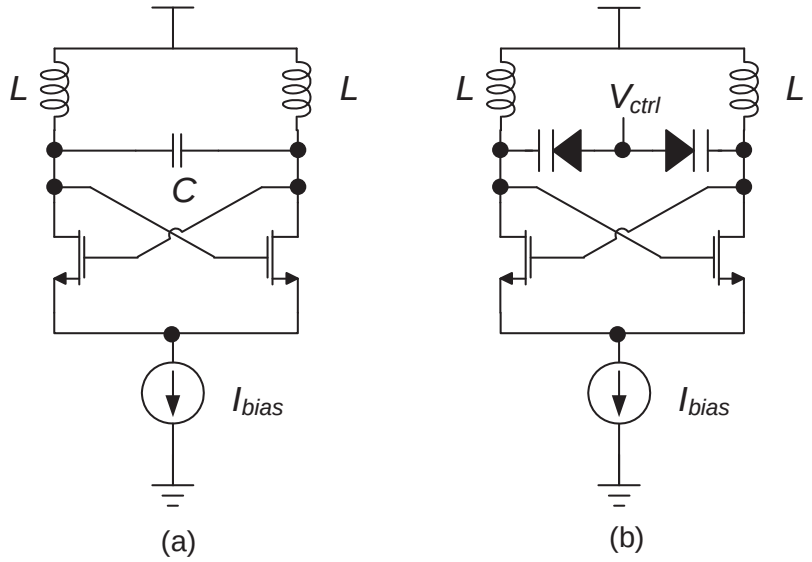


Figure 3-25: (a) Conventional cross-coupled differential LC VCO topology and (b) precisely LC tank tuning improvement with varactors.

Although possessing ideal phase and jitter performance, the use of inductors in the LC VCO has several disadvantages, which result in large area occupation, high power consumption, and relatively small tuning range in VLSI design.

3.5.2 Quadrature VCO Design with Low Power Consideration

Implementation of narrow-band RF architectures using image-reject mixer requires accurate quadrature voltage-controlled oscillator (QVCO) signals at a tuneable frequency range. Quadrature inaccuracies lead to gain and phase errors and further lead to residual image in the down-converted base-band signal for mixers. The LC VCO acts an ideal candidate for such an application due to its inherently low quadrature error and phase-noise behaviour.

As in the block diagram shown in Figure 3-26, the combination of a direct connection and inverting connection forces the two VCOs to oscillate in quadrature mode. The three topologies for approaching QVCO discussed in Chapter 2 also follows the same architecture and model, as shown in Figure 3-27.

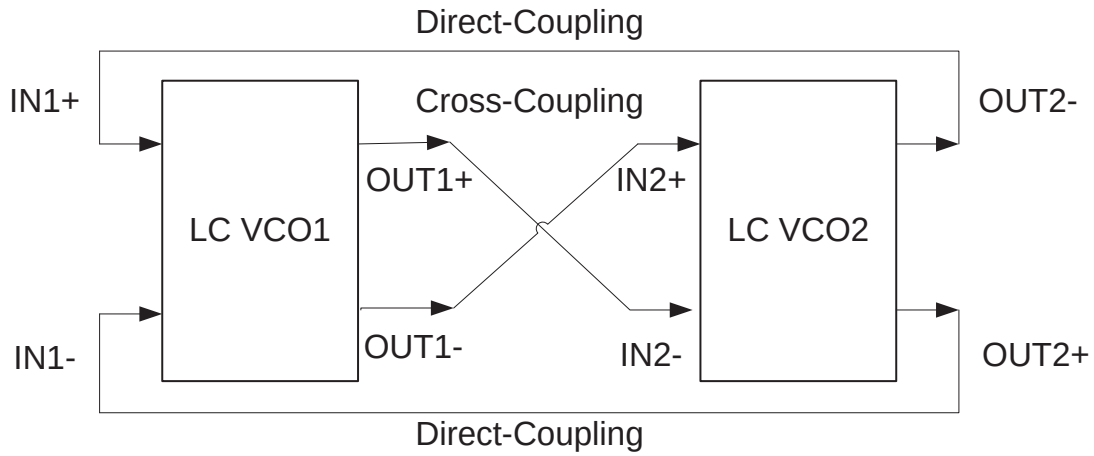


Figure 3-26: Block diagram and signal phases for QVCO

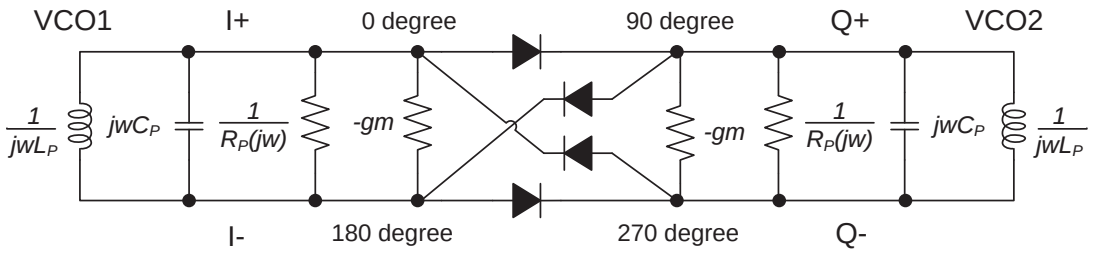


Figure 3-27: Simple model of the LC quadrature VCO

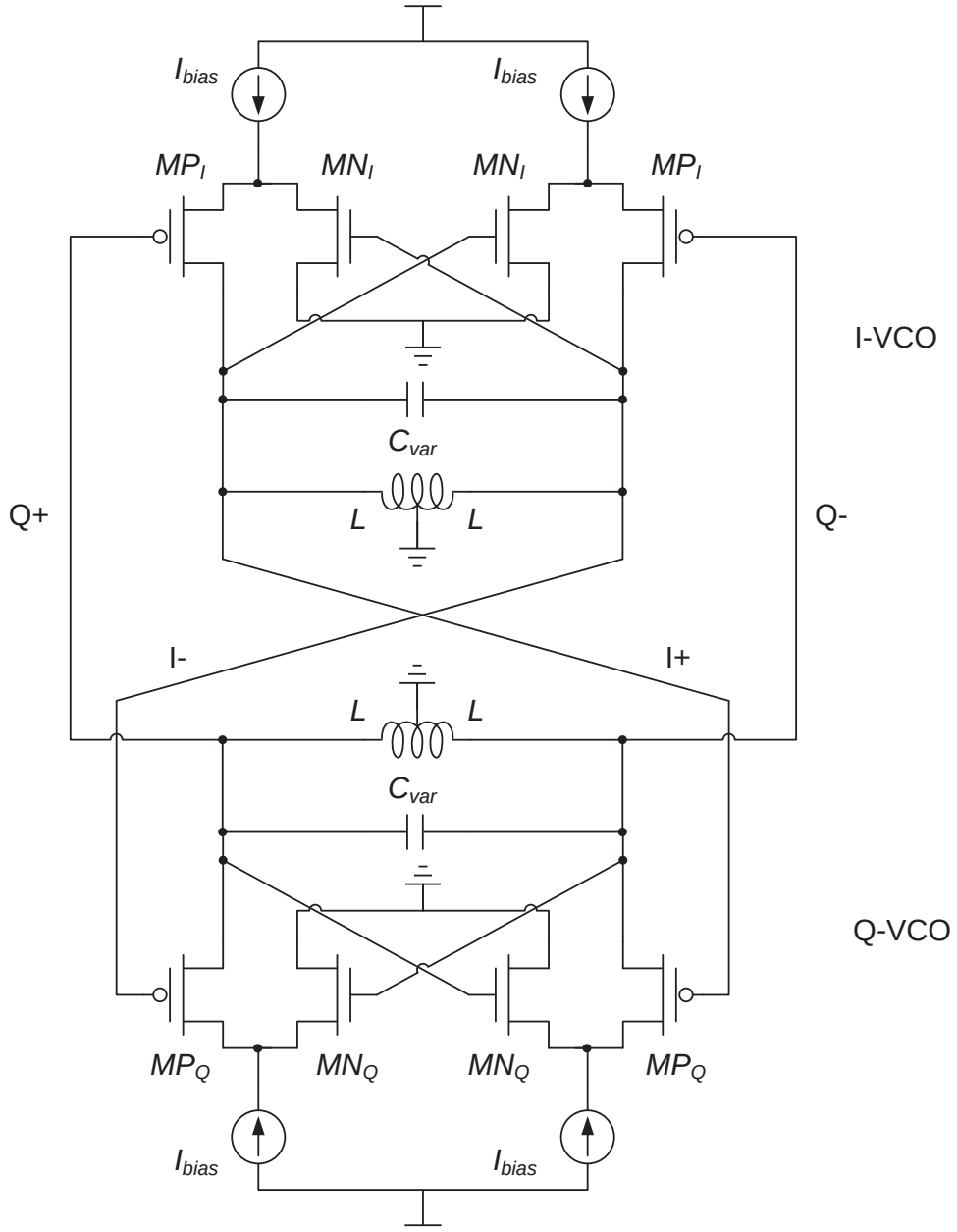


Figure 3-28: Proposed Low-voltage folded-cascode QVCO topology

PMOS folded cascode structure is used in the proposed topology to provide the mutual input excitations (couplings) for the quadrature generation. Figure 3-28 shows the circuit diagram of the proposed low-voltage folded cascode QVCO topology. The tail NMOS current source of the VCO-core positive feedback latch is eliminated to provide additional voltage headroom. Hence, it enjoys the advantage of oscillation under highly scaled supply voltage condition. Noise due to the tail current source is also avoided to bring further performance improvement[165]. In addition to the phase noise reducing effect of cascode structure [125], the inherent low-noise behaviour of the PMOS device (lower hot carrier induced drain current noise [137]) in this proposed folded-cascode structure would further reduce the phase noise contributions introduced by the coupling device. Furthermore, this structure uses a grounded centre-tapped inductor for the LC tank instead of the supply centre-tapped inductor in most of the QVCO design. This provides the advantage of reduced power supply noise that can greatly affect the linearity of cohabiting data-converters in a lower-voltage mixed signal VLSI chip. One of the additional benefits of this topology is the reduction of leakage currents into the standard p-substrate, which was connected to the ground as well. Therefore, this topology is less prone to self-resonance compared to most other topologies with floating or supply centre-tapped inductors.

3.5.3 QVCO with Low Phase Noise Consideration

The noise performance of a mixer is strongly affected by noise in the LO signal. Therefore, most of the oscillators are embedded in phase-locked loops (PLL) to control their frequency and reduce their phase noise. However, oscillators could still produce enough variation in the phase of their output to affect the performance of the transceiver. Thus, it is important to minimise the phase noise produced by the oscillator. Nonlinear oscillators naturally produce high levels of phase noise due to its perturbation term in the periodic steady-state response. The following equations show the decomposition of the noise response into amplitude and phase variations as:

$$V(t) = X(t) + \Delta X(t) = V_0\left[1 + \frac{\alpha(t)}{V_0}\right] sin[2\pi v_0 t + \emptyset(t)] \qquad (3\text{-}100)$$

or

$$v(t) = x(t) + \Delta x(t) = [1 + \alpha(t)]x\left[t + \frac{1}{2\pi}\frac{\emptyset(t)}{f_0}\right] \quad (3\text{-}101)$$

where $x(t)$ and $\Delta x(t)$ represents the unperturbed and perturbed solution in the response respectively, $\alpha(t)$ represents amplitude variations or amplitude modulation of the signal, $\emptyset(t)$ represents the phase fluctuations modulating the ideal linear phase change of the signal and f_0 is the oscillation frequency.

The phase noise itself is typically quantified in terms of the relative single-sideband SSB noise spectral density $L(f_m)$ (in dBc/Hz), which is given by [118]:

$$L(f_m) = 10log\left(\frac{N_{0,SSB}(f_m)}{P_{LO}}\right) = 10log\left[\frac{2kT}{P_{LO}}\left(\frac{f_0}{2Qf_m}\right)^2\right] \quad (3\text{-}102)$$

where f_m (or Δf) is the frequency offset relative to the oscillator frequency, $N_{0,SSB}(f_m)$ represents the phase noise power spectral density in a SSB at the offset frequency f_m, P_{LO} is the oscillator (carrier) power level, f_0 is the centre frequency of the oscillator and Q is the tank inductor quality factor. The equation (3-102) indicates that phase noise improves as both the oscillator power and Q increase at a given offset.

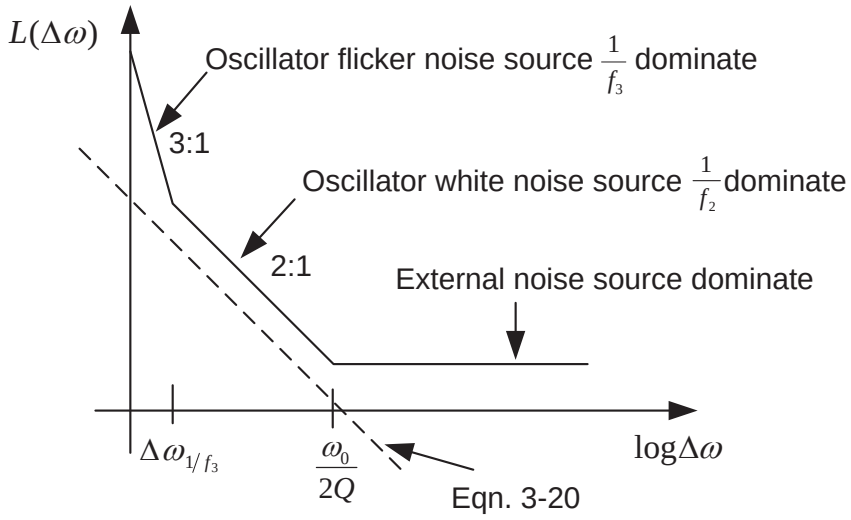


Figure 3-29: Typical Phase Noise Curve for an Oscillator

However, the equation (3-102) cannot accurately account for the practical frequency spectrum analysis of the VCO phase noise because of the additional noise sources such as active device noise, MOS flicker noise, white noise and other injected circuit noise. Moreover, the LC tank will also cause a large deviation in filtering from the resonant centre frequency. Leeson [166] claimed that a typical oscillator phase noise consists of three different regions: oscillator flicker noise sources dominated region $\frac{1}{f^3}$ at small offsets, oscillator white noise sources dominated region $\frac{1}{f^2}$ and a constant noise floor spread to higher frequency offsets from external noise sources, as shown in Figure 3-29. Therefore, a more accurate modification to equation (3-102) in $\Delta\omega$ format is given by Leeson [166] as:

$$L(\Delta\omega) = 10 \cdot log\left\{\frac{2FkT}{P_{LO}}\left[1 + \left(\frac{\omega_0}{2Q\Delta\omega}\right)^2\right] \cdot \left(1 + \frac{\Delta\omega_{1/f^3}}{|\Delta\omega|}\right)\right\} \qquad (3\text{-}103)$$

This modification equation involves a factor F to account for the increased noise in the $\frac{1}{f^2}\left(=\frac{1}{\Delta\omega^2}\right)$ region, an additive factor of unity to account for the noise floor and a multiplicative factor to provide a $\frac{1}{f^3}\left(=\frac{1}{|\Delta\omega|^3}\right)$ behaviour at sufficient small offset frequencies. Even though the modified equation provides a better qualitative model for phase noise behaviour, it still requires an empirical fitting parameter F and $|\Delta\omega|^3$ that must be determined from measurements, diminishing the predictive power of the phase noise equation. Furthermore, the noise values at corner frequencies between $\frac{1}{\Delta\omega^2}$ and $\frac{1}{|\Delta\omega|^3}$ often are not consistent with practical measurements [118, 162]. It is noted worthy to mention that the frequency at which the noise flattens out does not always equal to half of the resonator bandwidth $\omega_0/2Q$.

Both the ideal oscillator model and the Leeson model suggest that the increase in resonator Q and signal power will reduce phase noise. However, enlarging the Q value by active circuits is usually accompanied by increment in F as well since active devices contribute noises of their own. Also these models rely on a number of impractical assumptions: the linearity and time invariance.

Rather than using a linear time-invariant (LTI) phase noise model in the LC oscillator, the analytical model proposed by Hajimiri and Lee [118, 162] used a linear time varying (LTV) model that yielded a more accurate estimate of the overall phase noise. An impulse sensitivity function (ISF) is introduced to account for the time varying phase error. This function is a dimensionless, frequency-independent and amplitude-independent. The excess phase $\phi(t)$ is given by [118, 162]:

$$\phi(t) = \int_{-\infty}^{\infty} h_{\phi}(t,\tau)\, i(\tau) d\tau = \frac{1}{q_{max}} \int_{-\infty}^{t} \Gamma(\omega_0 \tau)\, i(\tau) d\tau \qquad (3\text{-}104)$$

where $h_{\phi}(x)$ and $\Gamma(x)$ represent impulse response and ISF, t and τ represents observation time and impulse occurrence time. After applying the Fourier expansion and integration, the above equation becomes:

$$\phi(t) = \frac{1}{q_{max}} \left[\frac{c_0}{2} \int_{-\infty}^{t} i(\tau) d\tau + \sum_{n=1}^{\infty} c_n \int_{-\infty}^{t} i(\tau) cos(n\omega_0 \tau) d\tau \right] \qquad (3\text{-}105)$$

The Fourier coefficients c_n are real and the phase (θ_n) of harmonics of ISF is ignored with the assumption that the noise components are uncorrelated. The q_{max} is the maximum charge displacement across the capacitance at the oscillator internal node. Injecting a sinusoidal current of frequency near an integer multiple m(=n) of the oscillation frequency to equation (3-105) gives a more useful phase spectrum expression that consists of two equal sidebands at $\pm\Delta\omega$ as:

$$\phi(t) \approx \frac{I_m c_m sin(\Delta\omega t)}{2 q_{max}\, \Delta\omega} \qquad (3\text{-}106)$$

In order to find the spectrum of the output voltage of the oscillator, the conversion of phase to voltage is obtained by involving the phase modulation of a sinusoid in output. The relationship is verified experimentally for equation (3-106) where two equal-power sidebands symmetrically disposed about the carrier as [118, 162]:

$$P_{SBC}(\Delta\omega) \approx 10 \cdot log\left[\frac{I_m c_m}{2q_{max}\,\Delta\omega}\right]^2 \quad (3\text{-}107)$$

This equation can be further extended to the general case into a white noise source as [120]:

$$P_{SBC}(\Delta\omega) \approx 10 \cdot log\left(\frac{\frac{\overline{i_n^2}}{\Delta f}\sum_{m=0}^{\infty} c_m^2}{4q_{max}^2\,\Delta\omega^2}\right) \quad (3\text{-}108)$$

Equation (3-107) and (3-108) implies the noises at both upward and downward frequencies are translated into the noise near the carrier. Noise near dc $\frac{1}{f}$ is up-converted and multiplied by coefficient c_0 to become $\frac{1}{f^3}$ noise near the carrier. Noise near the carrier remains in the same region but weighted by c_1 and white noise near higher integer multiples of the carrier is down-converted into $\frac{1}{f^2}$ region. It becomes clear that minimizing the various coefficients c_n and ISF will minimise the phase noise.

The spectrum in the $\frac{1}{f^2}$ region may be expressed from Parseval's theorem as:

$$L(\Delta\omega) = 10 \cdot log\left(\frac{\frac{\overline{i_n^2}}{\Delta f} \cdot \Gamma_{rms}^2}{2q_{max}^2\,\Delta\omega^2}\right) \quad (3\text{-}109)$$

where Γ_{rms} is the rms value of the ISF. The way to reduce the phase noise at all frequencies now depends on Γ_{rms}. It is notable that no empirical parameters are present in this new spectrum equation for $\frac{1}{f^2}$ region. Furthermore, this new LTV model can also use to analyse the phase spectrum in $\frac{1}{f^3}$ region as:

$$L(\Delta\omega) = 10 \cdot log\left(\frac{\frac{\overline{i_n^2}}{\Delta f} \cdot c_0^2}{8q_{max}^2\,\Delta\omega^2} \cdot \frac{\omega_{1/f}}{\Delta\omega}\right) \quad (3\text{-}110)$$

with $\frac{1}{f^3}$ corner frequency

$$\Delta\omega_{1/f^3} = \omega_{1/f} \cdot \frac{c_0^2}{4\Gamma_{rms}^2} = \omega_{1/f} \left(\frac{\Gamma_{dc}}{\Gamma_{rms}}\right)^2 \quad (3\text{-}111)$$

In addition to the time varying system, the influence of cyclostationary noise sources should also be taken into consideration. A typical example is the drain current noise $4KT\gamma g_{d0}$. It is cyclostationary in nature since g_{d0} depends on the noise bias current, which periodically fluctuates with the change in the overdrive of the MOSFET devices. Therefore, the cyclostationary noise can be treated as a stationary noise source and still fit into the foregoing conclusions.

In determining the various factors that will influence oscillator noise, the conditions for making a good oscillator can be satisfied. In the first place, both the signal power and resonator Q should be maximised for both LTI and LTV models. Secondly, an active device is necessary to compensate for tank loss with minimum noise input. ISF indicate there are sensitive and insensitive moments in an oscillation cycle. The best moment for an active device to return energy to the tank should occur all at once when ISF is at its minimum value. Hence, the transistors in an ideal LC oscillator should remain off and only deliver an impulse of current at the peak of each signal cycle. The final concern for a good oscillator design is to have a symmetrical property, which has small Γ_{dc} for minimizing the up-conversion of $\frac{1}{f}$ noise. A circuit topology in the following section is accomplished to include all these considerations in a practical oscillator design.

In addition to the symmetry concerns in LTV theory, a symmetrical negative resistance oscillator configuration is well explained. As shown in Figure 3-28, the noise in the two symmetrical half-circuit is partially correlated. By appropriately selecting the relative widths of the PMOS and NMOS devices, the dc value of the ISF (Γ_{dc}) for each half-circuit can be minimised and therefore minimising the up-conversion of $\frac{1}{f}$ noise. The symmetrical manner of this structure reduces the $\frac{1}{f}$ corner frequency to an exceptional low value. Furthermore, the arrangement of four transistors allows better signal swings,

which will also account for the improvement in phase noise behaviour. [116, 120, 167] experimentally proved a low phase noise of -121dBc/Hz at an offset of 600 kHz at 1.8 GHz, which can be obtained with low-Q on-chip spiral inductors (around 3-5) and 6mW of power consumption in a 0.25μm CMOS technology.

Considering the specific aspect of the proposed QVCO topology, the use of cascode topology in conjunction with PMOS coupling considerably reduces the effect of any injected circuit noise from the power supply, thus reducing the phase noise in the $\frac{1}{f^3}$ region of the overall phase noise spectrum. In accordance with LTV analytical model, all the white noise components near integer multiples of the QVCO frequency fold into phase noise near the oscillator in the $\frac{1}{f^2}$ region. The low frequency MOSFET flicker noise is also up-converted into close-in phase noise in the $\frac{1}{f^3} (= \frac{1}{|\Delta\omega|^3})$ region. Furthermore, the removal of the tail current source helps in reducing the number of $\frac{1}{f}$ noise source in this QVCO design, thus reducing noise in the $\frac{1}{f^3}$ region. However, the drawback of this structure compared with a conventional symmetrical negative resistance structure is the reduction of signal headroom and swing in a trade-off for the lower power consumption.

3.6 Summary

The performance measurements of the RF receiver front-end components have been evaluated in terms of its sensitivity, selectivity, spurious response, dynamic range and stability, which present themselves in the form of low cost, power consumption, noise performance, and high linearity and levels of integration. The system's architecture's design has been determined to balance these trade-offs. Direct-conversion receiver architecture is applied in this thesis due to its power consumption, system simplification and general performance. Quadrature topology is used to overcome the image problem.

Several opportunities for improvement have been identified for each front-end block. In LNA design, finite g_{ds} is introduced along with the PCSNIM technique to provide more

precise analytical model for noise performance, as well as additional degree of freedom on design consideration. The same topology is also employed for mixer design. Combining the LNA into mixer trans-conductance term can improve noise performance and power consumption. Along with quadrature topology and current-bleeding technique, the proposed mixer compares favourably to a conventional Gilbert mixer. VCO use folded-cascode topology to shrink down its voltage supply while keeping most of other performance measurements constant. The use of cascode topology in conjunction with PMOS coupling folded in QVCO can also reduce the phase noise in both $\frac{1}{f}$ and $\frac{1}{f^3}$ regions.

Circuit schematics to implement these design improvements have been presented and verified. Chapter 4 will describe the design implementations in detail to turn these schematics into a functional system.

CHAPTER 4: DESIGN IMPLEMENTATION

This chapter presents a detailed analysis of the design trade-offs consideration between the front-end RF receiver's design parameters, as well as the proposed circuit diagrams and relative components.

The introduction of 130nm fabrication technology has significantly improved the IC's thermal and power dissipation (TDP) and die size; enabling more integration on single silicon or a complete SOC. Even though there are some advanced fabrication technologies with smaller transistor size are available from foundry, they will have impact in the output impedance and the g_{ds} value of the transistors, which will result in lower gain and larger noise. Especially for LNA and mixer designs, smaller transistor size will also degenerate the input matching circuit that requires large inductor to match. This will be presented in the large induced thermal noise to the system. Moreover, the fabrication cost using 130nm is also much affordable compare to other advanced technologies to us.

The chapter's remaining sections focus on performance optimization and tuning of the UHF RFID at substrate level. RFIC design involves the consideration of parasitic effects that is present in MOSFET and a parametric selection of passive components for the front-end of a radio receiver; improper design would significantly affect the overall system performance and signal-to-noise ratio (SNR), hence an increase in noise figure especially in the high frequency range.

4.1 Design Implementation of the Low Noise Amplifier

4.1.1 The Basic Cascode Common-Source Amplifier

The cascode common-source (CS) amplifier provides high voltage gain for the LNA in high frequency range (see Figure 4-2(a)). Assuming $g_m = g_{d0}$ in a long channel device, the approximate noise factor of this simple amplifier is expressed as[31]:

$$F_{LNA} \approx 1 + \frac{\gamma}{g_m \cdot R_s} \tag{4-1}$$

The CS amplifier will provide reasonably high voltage gain with load resistor R_d. A degeneration resistor R_s is connected to the source to improve linearity of the amplifier. However, the present internal capacitance between the gate and drain (C_{gd}) will restrict its frequency response. This is represented as a small-signal circuit model in Figure 4-2(b). Miller's Theorem shows that the capacitance C_{gd} can be transformed into input capacitance as $C_{gd}(1 - A_v)$ and output capacitance as $C_{gd}\left(1 - \frac{1}{A_v}\right)$. The equivalent input capacitance is large and phase-shifted by $\frac{\pi}{2}$ radian due to high voltage gain A_v, which results in a pole at a lower frequency given by [31]:

$$p_{high} = \frac{1}{R_{in} \cdot C_{gs} || \left[C_{gd}(1 - A_v)\right]} = \frac{1}{R_{in}\left(C_{gs} + C_{gd} A_v\right)} \tag{4-2}$$

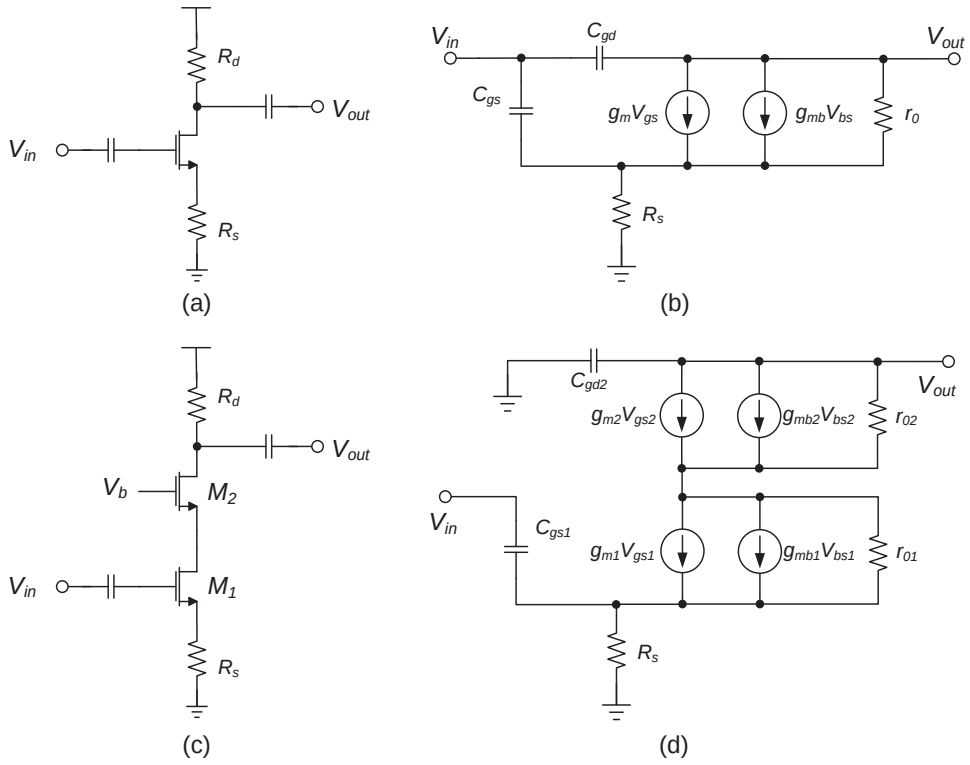


Figure 4-1: (a) Common-Source Amplifier and (b) its Small-signal CS circuit; (c) Cascode CS-CG Amplifier and (d) its Small-Signal Cascode Circuit

The cascode configuration in Figure 4-2(c) is often employed for signal processing with high-frequency (HF) components in order to reduce the Miller effect. In the small-signal equivalent circuit (Figure 4-2(d)), the gate of the CG stage will short to ground at AC, which will ground the internal capacitor C_{gd}. The Miller capacitance is reduced due to a negative feedback. When inductor L_d is attached to the cascode transistor's drain, oscillation in M_1 is created and the system resonates when the circuit's impedance is at a minimum or maximum for a series or parallel circuit, respectively; thus forming a band-pass filter, which produces input at a higher frequency. Although this configuration significantly improves the frequency response, it degrades the amplifier linearity due to the stacking of two transistors in series, and introduces undesirable noise power to the system. This factor is usually ignored in most of the RF journals as it produces insignificant noise injection at the input stage [31, 57]. However in deep sub-micron technology, this factor can no longer be ignored as it comprises more than 40% of noise injection, hence it is taken into account in this discussion [168].

The quality factor derived from the equivalent model in Figure 4-2 (d) is as below:

$$Q = \frac{\omega C_{gs}}{R_S} \tag{4-3}$$

At the resonance frequency, the voltage amplitude through the C_{gs} is approximately Q times the voltage across the input terminal. Hence the effective trans-conductance would be Q times the input transistor trans-conductance. This will also increase the voltage gain by the same factor. In view of these, the CS-CG configuration is usually adopted in narrow-band applications due to its input impedance is treated as a series RLC network with the finite Q.

The MOSFET trans-conductance would also increase the transistor unity gain frequency f_T, also known as cut-off frequency in amplifier design. f_T is defined as the frequency when the gain of the device (or transistor) equals to unity and it is often used in measuring the speed of the device. For instance the transistor unity gain is defined as:

$$f_T \approx \frac{g_m}{2\pi C_g} \tag{4-4}$$

where the gate capacitor $C_g = C_{gd} + C_{gd}$. A higher transistor unity frequency f_T usually implies a higher frequency range of operation, which is desirable. Typically, f_T should be five times more than the operating frequency of the devices in practical application.

4.1.2 Noise and Power Constrained Techniques

Previous sections' discussion of the CS-CG concludes that inductive source degeneration serves as a suitable front-end amplifier since it does not inject too much noise into the system. The degeneration inductor L_s is used to replace R_s in Figure 4-3. This additional inductor is attached with another inductor connected to the gate to provide resonance tuning. Figure 4-4(a) and (b) demonstrate the effect of L_s in tuning the performance of LNA [168]. The Smith Chart in Figure 4-4(a) illustrates an independent trajectories between the optimum noise matching condition Z_{opt} and the power matching condition when L_s is increased. The point in which the two trajectories intersect is therefore the optimal noise figure. This emphasizes the importance of accurate input impedance characterization in optimizing noise performance. As the input impedance Z_{in} is also dependant on L_s, therefore by varying the L_s, Z_{in} can be tuned to matched different impedances, as shown in Figure 4-5.

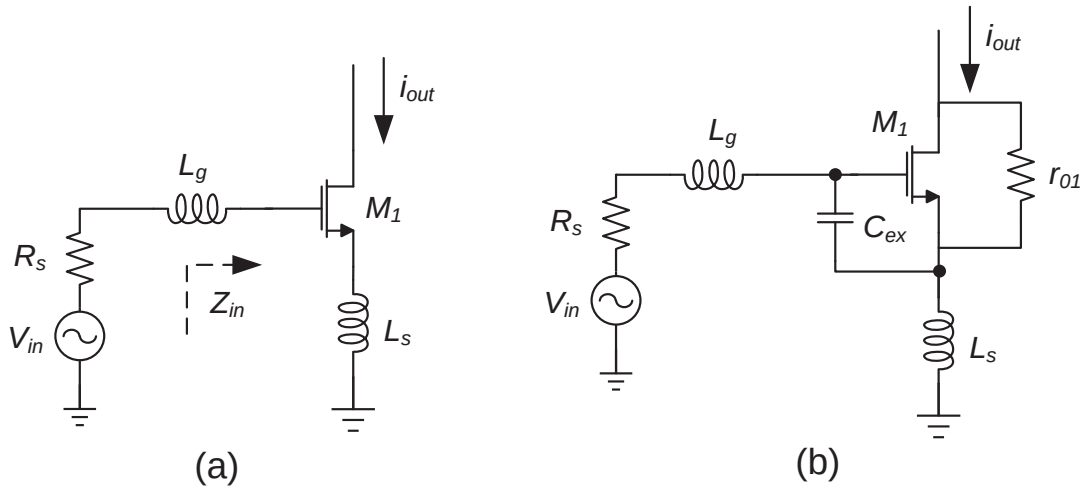


Figure 4-2: (a) Inductive source degeneration topology and (b) with extra capacitance and g_{ds} consideration for design in LNA

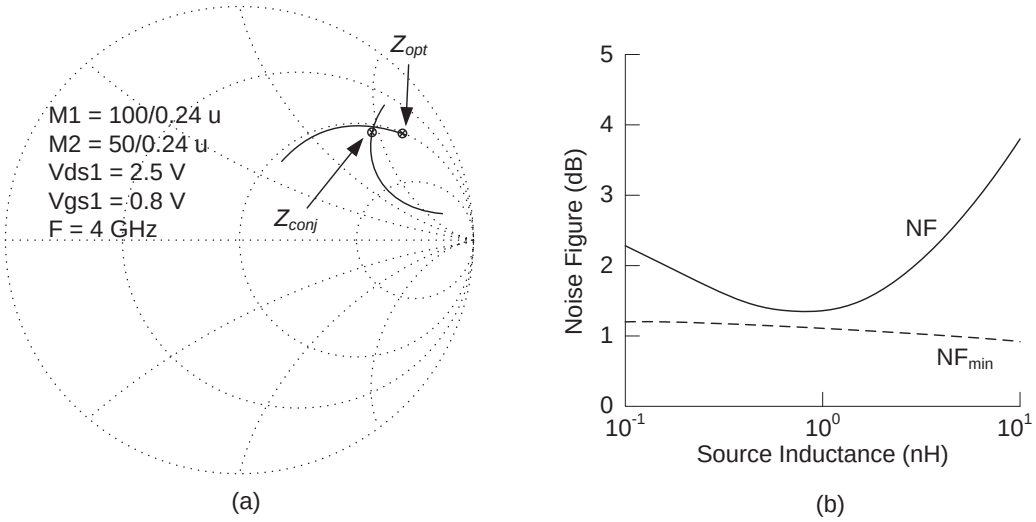


Figure 4-3: The noise performance relative in $\boldsymbol{L_s}$ changing representing in (a) Smith Chart of optimum source impedance and (b) its noise figure performance

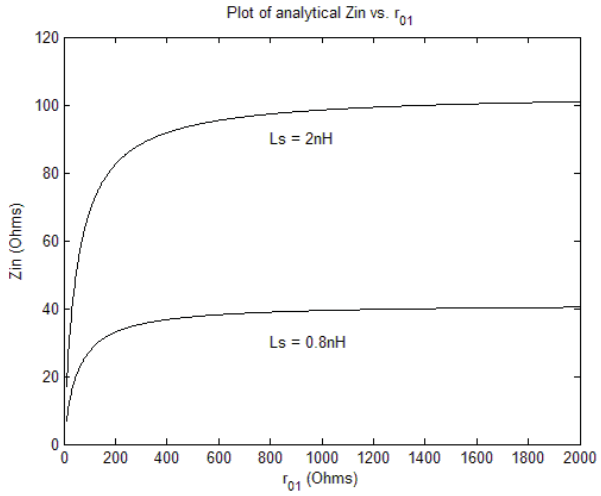


Figure 4-4: Zin is varying due to the degeneration inductor value

There are several challenges in the implementation of a UHF RF front-end receiver with deep-submicron CMOS process, e.g. the C_{gs} of the M_1 would be very small (such that a large inductor L_g and L_s would be required for the matching). One solution would be to attach L_g off-chip. This, however, will result in a large resistance, which combined with the gate resistance would generate a large amount of additional thermal noise. PCSNIM topology applies extra degree of freedom by attaching an extra capacitor C_{ex} parallel to C_{gs} to overcome this problem.

This extra capacitor increases the effective capacitance looking into the gate of M_1, resulting in less dependency on L_g and L_s for the same frequency of application

matching. Since increasing the C_{gs} directly will also cause an increase in the size of transistor M_1, PCSNIM topology neither changes the amount of the intrinsic gate induced noise nor increase any capacitance of C_{gd} and C_{db} of M_1.

The PCSNIM implementation follows the following process: the dc-bias V_{gs}, which provides the minimum frequency (F_{min}), is firstly selected. Based on the F_{min}'s power constrain equation 3-44, the transistor M_1's size is determined next. Third, the device's trans-conductance g_m and C_{gs} will be determined when MOS transistor operating in saturation mode. In the next place, the degeneration inductor L_s is calculated at resonance to cancel out the capacitance of C_t from equations (3-53), (3-55) and (3-57). Since C_t constitutes the additional capacitance C_{ex} and C_{gs}, the value of C_{ex} with associated off-chip inductor L_g can be calculated to satisfy the PCSNIM simultaneously at last. The values for L_s and C_{ex} should be chosen taking into the considerations in trade-offs between the noise and power gain. Large size of L_s would directly increase F_{min} and large C_{ex} leads to the gain reduction since the effective cut-off frequency f_T of the composite transistor will reduce and push the resonant frequency boundary.

Although the noise resistance R_n of the PCSNIM is not affected by the C_{ex} compared to the PCSIM topology, it is dependent on the value of trans-conductance g_m. Therefore, a blind pursuit for low power dissipation with gate-length reduction will result in an extremely large value of R_n. Excessive large R_n will affect LNA design in noise performance.

Considering that the cut-off frequency f_T changes with the extra capacitance C_{ex}, this will result in power gain reduction. f_T of the LNA is reduced by a ratio of C_t/C_{gs}. The maximum oscillation frequency (f_{max}) will also be affected due to the functional dependence of f_T. Therefore, the value of C_{ex} cannot be too large with reference to C_{gs}.

4.1.3 DC Biasing Circuitry

Current mirror is a common method of generating DC biasing current for the transistors, as shown in Figure 4-6. This biasing current is constructed with reference transistor(s) and reference resistor(s). Since the biasing transistor connects its gate and source together with CS amplifier, the drain current of both reference and output will have the same gate-source voltage V_{gs}. Hence the output current can be obtained as:

$$I_{out} = \frac{(W/L)_{cs}}{(W/L)_{ref}} I_{REF} \qquad (4\text{-}5)$$

A key property of this topology is that it allows precise copying of the current with no dependency on process and temperature. The ratio of I_{out} and I_{REF} is given by the ratio of device dimensions, a parameter that can be controlled with reasonable accuracy. In general, the size (width) of the reference transistor is chosen to have a small value in order to reduce the power dissipation of the reference path. A large resistor is placed between the gates of two transistors to avoid any current noise leaking from the DC reference path.

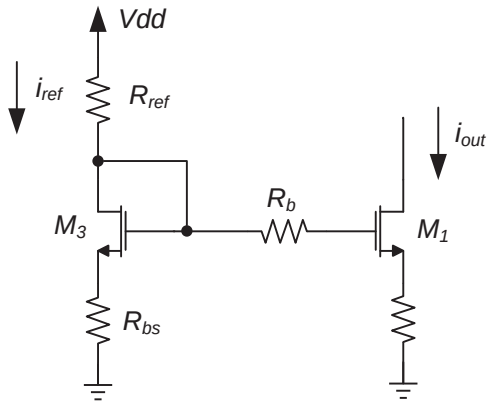


Figure 4-5: DC current biasing using current mirror topology

In practice, channel length modulation will affect in current in M1; however, similar to CS-CG amplifier, a cascode current source can be used to suppress this effect.

4.1.4 Output Circuitry

An important property of the cascode topology is its high output impedance. To calculate the total output impedance R_{out} of the circuit, the circuit can be viewed as a common-source stage with degenerated impedance $Z_{in.eq}$, which is formed by L_s, r_{01} and the input equivalent impedance.

$$Z_{in.eq} = \frac{V_{eq}}{i_{eq}} = (R_{Ls} + sL_s + r_{01}) - \frac{(R_{Ls} + sL_s)[g_{m1}r_{01} + sC_t(R_{Ls} + sL_s)]}{sC_t\left(R_S + R_{ge} + R_{Lg} + sL_g + \frac{1}{sC_t} + R_{Ls} + sL_s\right)} \quad (4\text{-}6)$$

Thus, the R_{out} is given by:

$$R_{out} = \left[[(g_{m2} + g_{mb2})r_{02} + 1]Z_{in.eq} + r_{02}\right] || Z_d \quad (4\text{-}7)$$

The load impedance Z_d is constructed by a RLC tank ($= \frac{1}{sC_d} \| sL_d \| R_d$) as in Figure 4-7, tuned at resonance frequency.

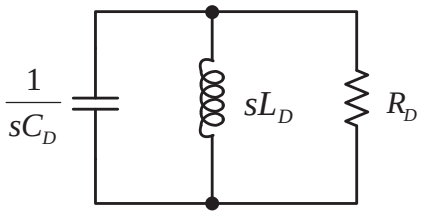


Figure 4-6: RLC tank output load

Assuming $g_{m2}r_{02} \gg 1$ and $g_{m2} \gg g_{mb2}$, the output impedance R_{out} will have an approximate value of $g_{m2}r_{02}Z_{in.eq}$. The cascode stage M_2 boosts the output impedance of M_1 by a factor of $g_{m2}r_{02}$. Therefore, more than two cascode stages are usually stacked up to achieve even higher output impedance, but the requirement of additional power budget makes multiple cascode topologies less attractive for lower power application.

A detailed derivation of gain expression is explained in the previous chapter. Since the voltage gain can also be written as the product of total input trans-conductance and total output impedance ($G_m R_{out}$) this allows an intuitive judgment of the output impedance. G_m is determined by the trans-conductance of a transistor, such as M_1, which varies with the bias current and device capacitances. An increase in the voltage gain can also be achieved by maximizing R_{out}. This method in conjunction with the derivation in chapter 3 provides the same outcomes.

The fact that if the R_{out} reaches its maximum, an extra stage is required to match the output impedance to the standard 50Ω. Therefore, an output buffer stage, which also acts as the driver to the first-stage of mixer is included in the LNA design. The output buffer stage will address impedance matching and serves as an intermediate interface between different RF front end blocks. The output buffer is a suitable lead-in to the mixer as it assures that the LNA gain will not be affected by any changes made to the input impedance of the mixer. The current mirror can also be used to drive the buffer, as shown in Figure 4-8(a).

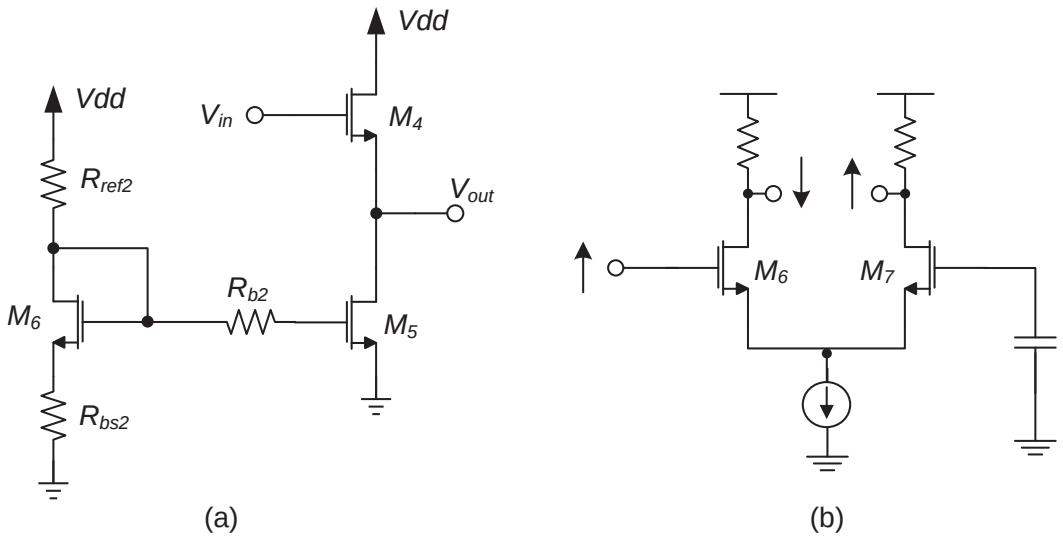


Figure 4-7: (a) Conventional output buffer stage and (b) Conventional differential balun topology

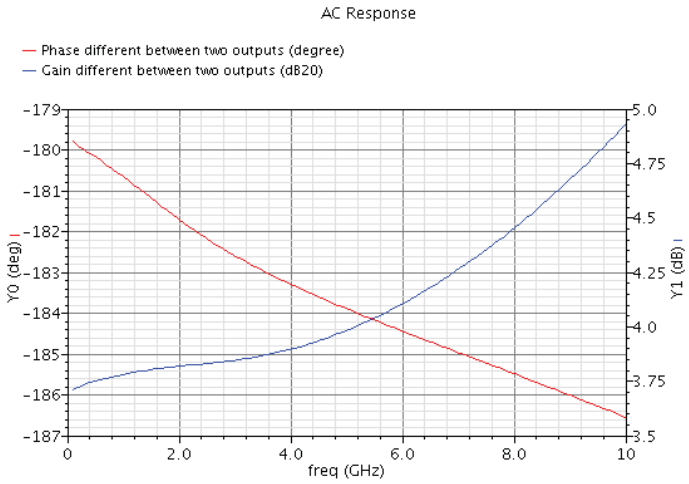


Figure 4-8: Simulated phase imbalance and amplitude imbalance for conventional differential active balun topologies of Figure 4-8(b).

In order to generate differential signals from the single-ended topology, the balun is also designed and attached to the output stage. As shown in the literature review, it is common to apply the configuration of a differential amplifier due to its many advantages in gain and isolation at high frequencies. The simulation's results (see Figure 4-9) of the conventional differential balun in Figure 4-8 (b) express that there is a 5-8 dB mismatch in the output gain, as well as a phase mismatch from 180° at low frequency to 167° at high frequency. Since the differential structure has a symmetrical configuration, the unbalanced output signal is a result of unbalanced input signals present at M_6 and M_7. To offset this output drift, the input offset voltage is introduced at gate of M_7. In order to inject signal power to M_7, a CR feedback circuit from [77, 169] is adopted here, as shown in Figure 4-10 (a). An improved version of an LCR compensation circuitry is shown in Figure 4-10(b). This topology, more flexible in narrow band frequency tuning, however results in a large area occupied by the inductor [77]. The value of the capacitor and inductor can be calculated with the LCR circuit operating at tuned resonance frequency.

A cascode topology would isolate the active balun circuit from variation in the load condition and isolate the output matching network from DC bias point variation in the circuit. This also contributes to the improvement of inter-modulation immunity at the receiver by reducing the static DC offset in a direct conversion receiver[169]. However,

the differential topology indisputably consumes more power, hence there is a trade-off between the gain and power dissipation for practical implementation.

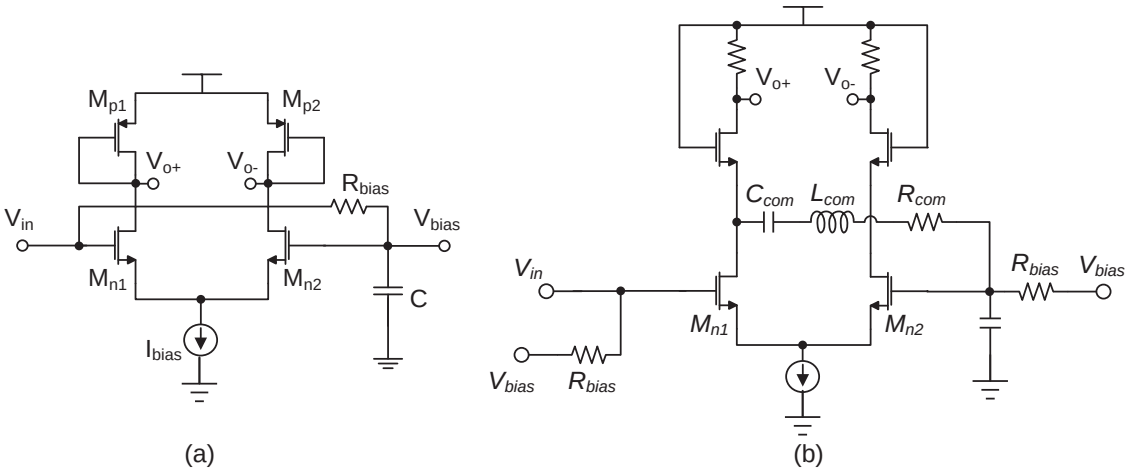


Figure 4-9: Cascode differential balun with (a) RC compensation circuit [77, 169] and (b) RLC compensation circuit [77]

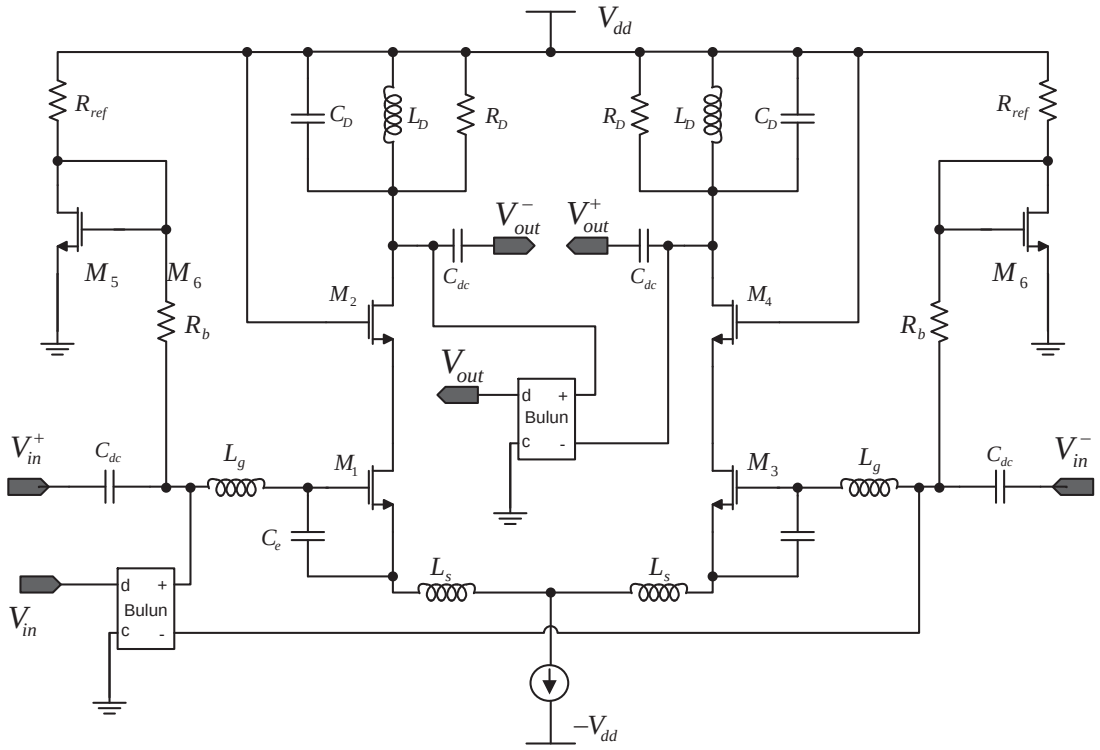


Figure 4-10: Differential LNA circuitry

4.1.5 Differential Circuitry

Figure 4-11 shows the differential circuit, which is constructed using two symmetrical single-ended LNAs.

The use of differential topology offers several important advantages. Firstly, differential LNA offers a stable reference point but selecting on-chip ground as the reference point for single-ended LNA may not be very reliable due to the presence of parasitic resistance and capacitance. Moreover, these parasitic components are unpredictable due to the IC packaging, temperature and production process. The measured result in each half of the circuit in the differential topology will always correlate to the other half. This will minimise unexpected result and instability. The degenerating inductors are connected together at the "virtual ground". At this point, a current source is usually placed to provide a current that is twice the current flowing down from each side of the LNA section. Any parasitic reactance in series with the bias current source would be irrelevant. Two "ideal" baluns are used in the design for a transformation between differential and single-ended signals for both input and output. Two AC sources could also be applied with opposite polarity in order to achieve the same effect. Then again, both baluns will be matched to 50Ω at tuning frequency as in the singled-ended LNA design.

Another advantage of using the differential circuit is noise reduction and common-mode disturbance rejection. In mixed-signal applications, both the supply and substrate voltages may be noisy; hence, this property becomes particularly important.

Provided the amplifier's input noise source is distributed equally between two signal paths, which indicate the noise signal will not be amplified by the same factor as the input signals. The noise signal at each terminal will have the same amplitude but with inverted phases, which will cancel out each other at the differential circuit's output. This inherent immunity will improve common-mode rejection ratio (CMRR). Moreover, as the output signal amplitude in differential is twice that in the single-ended LNA, the SNR ratio will also be improved.

For equal noise figure, the power consumption of this amplifier will be twice that of its single-ended counterpart. Offsetting this disadvantage is the addition of improved linearity that is attained by dividing the input voltage between two devices.

4.2 Design Implementation of the Mixer

Down-converting mixer design starts with the analysis of a conventional differential Gilbert mixer. The PCSNIM topology and current bleeding technique employed in trans-conductor and switching/mixing stage respectively address both low power and low noise requirements. The quadrature topology will be discussed in detail for practical implementation.

4.2.1 Linearity Consideration for Mixer

Mixer linearity, which is dependent on the transistors' drain current and gate overdrive voltage. It is a critical design parameter and serves as a starting point for mixer design. In short-channel MOSFETs, the drain current and gate overdrive voltage have following equation [170]:

$$I_{D,sat} = W_{v_{sat}} C_{ox} \frac{V_{od}^2}{V_{od} + E_{sat} \cdot L} \qquad (4\text{-}8)$$

where V_{od} is the voltage overdrive and equals to $V_{gs} - V_{\text{th}}$ and E_{sat} is the velocity saturation field strength corresponding to the critical electrical field at which the carrier velocity becomes saturated. E_{sat} must satisfy the equation of $2v_{sat}/\mu_{eff}$ to provide a continuous velocity model. The v_{sat} is the saturation velocity and μ_{eff} is the unified formulation of mobility.

From the linearity definition, the coefficients c_1 and c_3 from Taylor series expansion for general two-port system can be determined and substituted in P_{1dB} and P_{IIP3} definition[170], yielding:

$$P_{1dB} \approx 0.29\frac{v_{sat}\cdot L}{\mu_1 \cdot R_S}V_{od}\left(1+\frac{\mu_1 \cdot V_{od}}{4v_{sat}\cdot L}\right)\left(1+\frac{\mu_1 \cdot V_{od}}{2v_{sat}\cdot L}\right)^2 \quad (4\text{-}9)$$

$$P_{IIP3} = \frac{8}{3}\frac{v_{sat}\cdot L}{\mu_1 \cdot R_S}V_{od}\left(1+\frac{\mu_1 \cdot V_{od}}{4v_{sat}\cdot L}\right)\left(1+\frac{\mu_1 \cdot V_{od}}{2v_{sat}\cdot L}\right)^2 \quad (4\text{-}10)$$

where

$$\mu_1 \cong \mu_0 + 2\theta V_{sat.L} \quad (4\text{-}11)$$

An accurate ratio of P_{IIP3} to P_{1dB} is

$$9.17\left[1+0.145\frac{\mu_1 \cdot V_{od}}{v_{sat}\cdot L}\left(1+\frac{\mu_1 \cdot V_{od}}{4v_{sat}\cdot L}\right)\right] \quad (4\text{-}12)$$

which also depends on the overdrive voltage.

According to equation (4-9) and (4-10), linearity can be improved by increasing the gate overdrive voltage LO. However, an increase in the gate overdrive voltage will also result in the increase of power consumption, which is unacceptable in most applications. V_{od} is usually adjusted to 0.2-0.5V. The simulated results of P_{1dB} and P_{IIP3} versus V_{od} are listed in Table 4-1 using the SPICE model data for the IBM CMRF8SF (130nm) process. Figure 4-12 illustrates the corresponding P_{1dB} and P_{IIP3} as a function of V_{od}.

Table 4-1: Estimation of 1dB Compression point and IIP3 vs V_{od}

$L=0.12\times 10^{-6}$ $V_{sat}=1.01\times 10^{7}$ $\mu_0=4.40\times 10^{-2}$ $\theta=0.5$ $R_s=10$ $\mu_1=\mu_0+2\times\theta\times V_{sat}\times L$			
V_{od}	P_{1dB} approximate (dBm)	P_{IIP3} accurate (dBm)	P_{IIP3} (dBm)
0.01	-5.4748	-5.4644	4.1609
0.1	5.0190	5.0143	14.6547
0.2	8.5553	8.5331	18.1910
0.3	10.8204	10.7800	20.4561
0.4	12.5540	12.4946	22.1897
0.5	13.9889	13.9097	23.6246
0.6	15.2294	15.1298	24.8652
0.7	16.3319	16.2111	25.9676

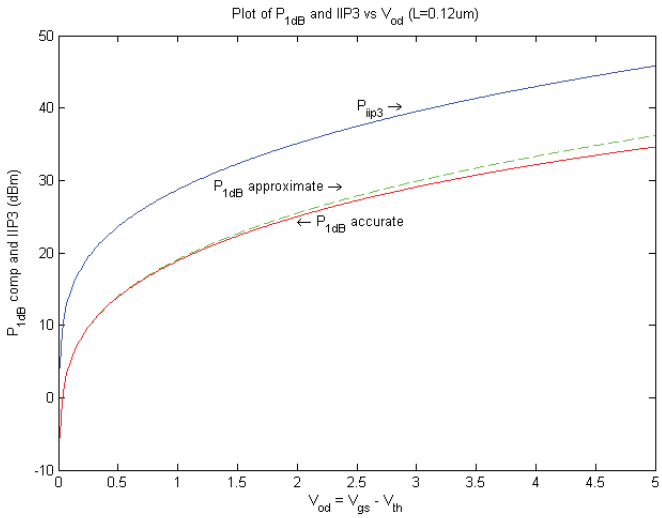


Figure 4-11: Plot of 1dB compression point and input referred 3rd order intercept point (IIM3) with voltage overdrive V_{od}

Another observation is that W and C_{OX} do not appear in the in P_{1dB} and P_{IIP3} equations. This suggests that IIP3 and device trans-conductance g_m can be decoupled through W and C_{OX} factors. Note that the above derivation is based on the assumption of quasi-static nonlinearity, which is valid when the operating frequency is well below the transition frequency w_T of the device.

4.2.2 Trans-conductance stage

The previous chapter, "Design Methodology", explained that noise power in the Gilbert cell is mostly injected during the trans-conductor stage. The noise performance can be improved by increasing the LO amplitude and decreasing the DC current. Since large g_m will minimise the noise injection, the transistor with inductive degeneration is also employed for the trans-conductor stage with the parallel capacitor C_{ex} applied for PCSNIM technique for low power consumption. The same principles and implementation steps for LNA design applies for trans-conductance stage, as shown in Figure 4-3. The trans-conductance circuitry with PCSNIM topology inherits the advantages of low noise and low power dissipation. The degenerated inductor at the sources of trans-conductance will increase the linearity of the mixer.

The approximate voltage gain of the mixer with source degeneration is given by:

$$G_C = \frac{V_{RF}}{V_{IF}} \approx \frac{2}{\pi}\left(\frac{R_L}{R_g + \frac{1}{g_m}}\right) \quad (4\text{-}13)$$

where g_m is given by

$$g_m = \sqrt{\frac{2K_P W I_D}{L}} \quad (4\text{-}14)$$

Therefore, for a certain conversion gain, g_m can be obtained through the expression above.

Alternatively g_m can also be computed with reference to its definition and the known magnitude of voltage overdrive V_{od}. Assuming a desired drive current, g_m yields to

$$g_m = \frac{2I_D}{V_{gs} - V_{\text{th}}} \quad (4\text{-}15)$$

and the gate width (W) of the transistors for the mixer can be calculated by:

$$W = \frac{g_m^2 \cdot L}{2K_P I_D} \quad (4\text{-}16)$$

where $K_P = \mu_0 C_{OX}$.

The optimum size for trans-conductance transistor can also be computed with reference to F_{min} as discussed in Chapter 3, this yields:

$$W_{opt} \approx \frac{1}{3\omega L C_{OX} R_S} \quad (4\text{-}17)$$

The transistor gate length can be determined by simulation. The following sub-section will discuss the switching pairs with current bleeding technique to produce stable oscillation and low power dissipation.

4.2.3 Switching Pairs with Current Bleeding Technique

Figure 4-13 shows a typical current bleeding circuit, which is constructed with two PMOS transistors providing the main DC current into the trans-conductor stage in the double balanced Gilbert mixer. PMOS transistors are chosen here because the common-source configuration provides higher output impedance at the drain. Since the output impedance is greater than the input impedance for the switching pair at the source which has an approximate value of $1/g_{m\ sw}$, most of the RF signal will flow into the switching pairs. Using a single-balanced mixer with current bleed as an example, the output current of the LO can therefore yield to [155]:

$$i_{LO} = \frac{Z_{bld}\,[g_{m\ sw1}(t) - g_{m\ sw2}(t)]}{1 + Z_{bld}\,[g_{m\ sw1}(t) + g_{m\ sw2}(t)]} \times i_{RF} \qquad (4\text{-}18)$$

where Z_{bld} is the output impedance of the current bleeding circuit..

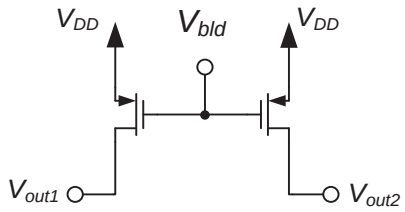


Figure 4-12: Current bleeding circuit

The current bleed circuit provides most of the turn on current for the switching stage to reduce the power in the switching stage. However, excessive current bleeding should be avoided due to the presence of large parasitic tail capacitance. The tail capacitance comprises the switching capacitance C_{gs}, output Miller capacitance from the trans-conductor and the output capacitance of the bleeding circuit and it will significantly reduce the overall gain. An extra parallel inductor will be required to compensate the tail capacitance. This, however, will increase the die size [155]. Therefore, the gate length of the bleeding transistors should be scaled reasonably.

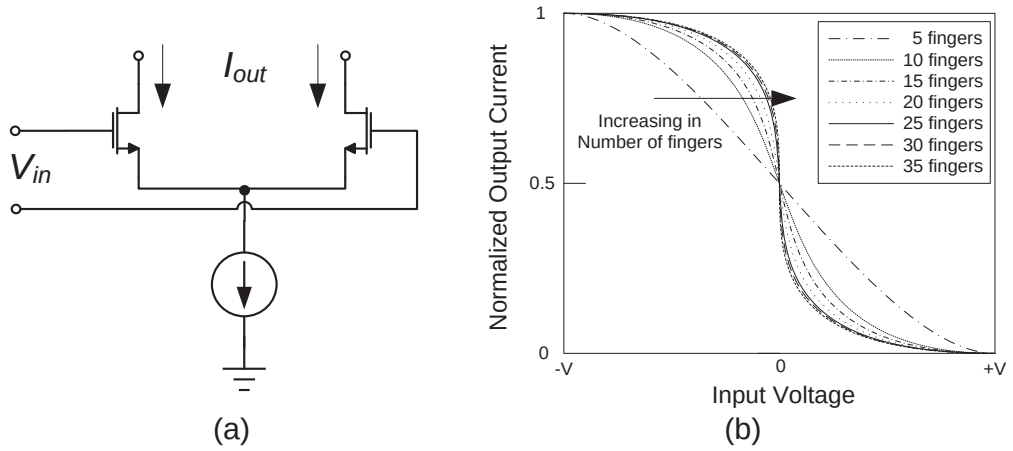


Figure 4-13: (a) Switching circuit and (b) its normalized output current vs. input voltage

The transistors are operated in saturation mode by adjusting the switch voltage. The voltage overdrive is a crucial consideration in the design of a mixer. Figure 4-14 (b) demonstrates the normalized plot of the output current of one branch of a differential amplifier versus the differential input voltage with different number of transistor finger for the switching circuit in Figure 4-14 (a). Figure 4-14 (b) indicates that switching voltage is inversely proportional to the transistor size for the same amount of DC current. The LO power cannot be too high as it would drive the trans-conductors into the triode region and consequently affect the gain. Moderate LO signal with voltage overdrive between 0.2 to 0.4V is suitable to provide an acceptable compromise between gain and noise figure.

Since the g_m and initial transistor size of the trans-conductance stage can be calculated from the certain required conversion gain and minimum F_{min}, the transistor size of the trans-conductance can be further determined after several simulations for the initial prediction.

4.2.4 Quadrature circuitry

A quadrature mixer consists of a pair of Gilbert mixers in order to provide quadrature down conversion. In order to increase the trans-conductor matching, the trans-

conductors of two Gilbert mixers were combined in parallel to form a quadrature double-balanced mixer. In this manner, process variations in the trans-conductor transistors are shared between I and Q signals, consequently improving amplitude and phase mismatch.

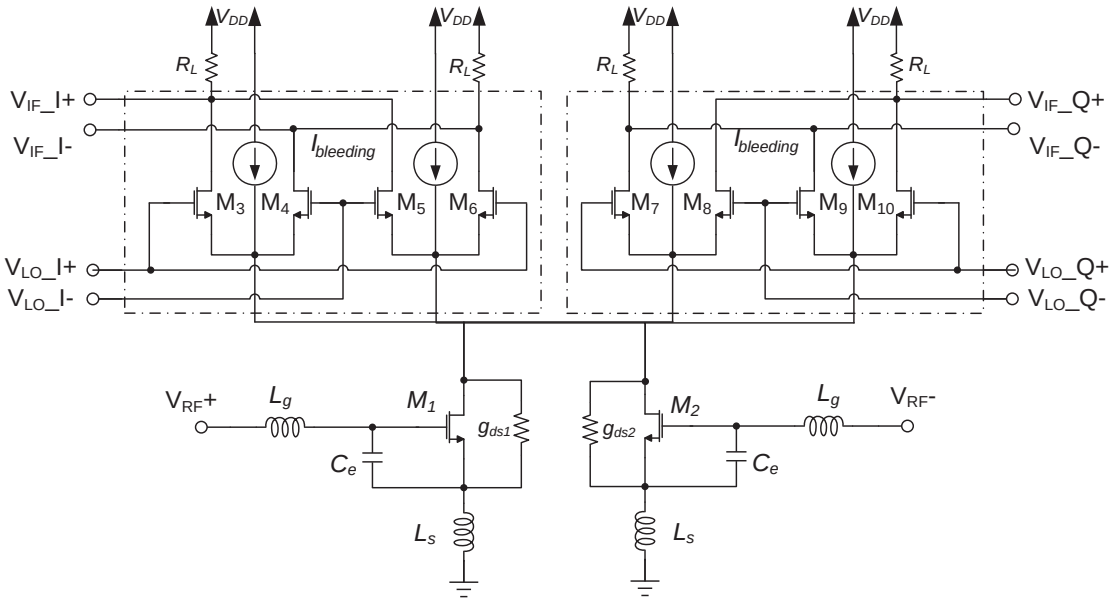


Figure 4-14: Proposed complete quadrature mixer

Since the symmetrical topology enjoys equal power dissipation in each pair, twice of the current will flow though each trans-conductor. Hence the width of the quadrature mixer trans-conductor transistors will have twice of the value compared to the conventional Gilbert mixer trans-conductors. The quadrature mixer therefore has the same total trans-conductance and same conversion gain as the conventional mixers.

The linearity of the quadrature mixer should also have the same scales as the conventional Gilbert mixers since the dominant source of nonlinearity is generally at the trans-conductor stage. Since the quadrature Gilbert mixer trans-conductor transistors have the same length and approximately similar overdrive voltage as the conventional Gilbert mixer trans-conductor transistor, it therefore should exhibit similar linearity[160].

4.3 Design Implementation of Voltage Control Oscillator

4.3.1 LC cross-couple stage

The implementation of VCO begins with the analysis of conventional LC cross-coupled VCO, as shown in Figure 3-25. The transistors M_1 and M_2 are cross-coupled to produce a negative resistance of $1/g_m$. Similar to other differential topologies, M_1 provides a constant current for the cross-couple stage. The inductor and capacitance act as a LC tank for oscillation. The varactors provide variable capacitance according to the gate voltage. Figure 3-27 shows the parasitic resistance and capacitance for this VCO topology. The spiral inductor has wire capacitance and resistance.

4.3.2 Switched Tuning Technique

In practical design, typical LC-tank VCO is tuned by varying the tank capacitance with a varactor. MOS transistors with drain, source and bulk (D, S and B) connected together act as an MOS capacitor. Depending on different amplitude in the oscillator (voltage between B and G), the MOS capacitor performs different small-signal C-V characteristic, as shown in Figure 4-16 [171]. In the case for a PMOS capacitor, the accumulation region distributes the resistance in the substrate to ground; the depletion (moderate inversion) region distributes the resistance in series with a small capacitor; and in the inversion region, the resistance of the MOSFET channel is much lower than the spreading resistance.

The critical parameter for varactor design is the tuning range ability. One solution to achieve a large tuning range is by removing the connection between D, S and b and connecting B to the power supply to avoid the transistor (usually NMOS) entering the accumulation region[117]. A more attractive alternative is the use of the PMOS device in the depletion and accumulation regions only[171]. These two approaches are expressed as I-MOS and A-MOS by their dominated region, as shown in Figure 4.-17.

The advantage of A-MOS device is that with the large tuning range ability, it also provides lower parasitic resistance and less sensitivity to substrate-induced noise.

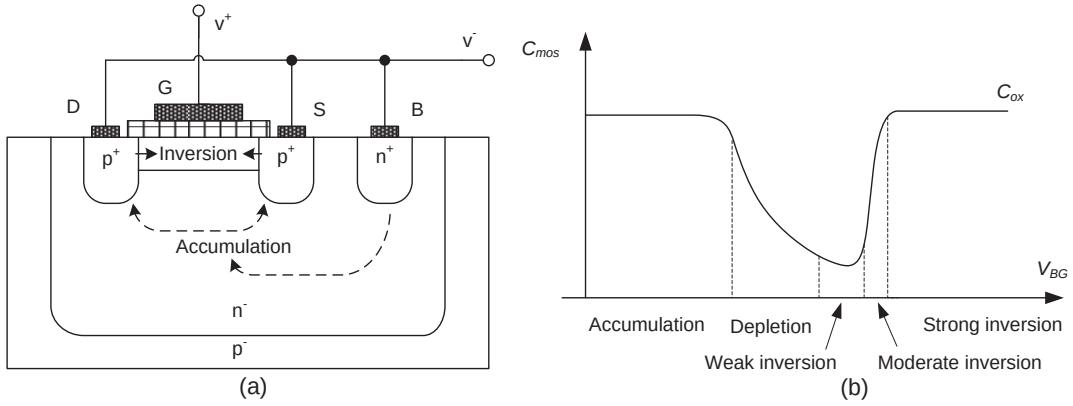


Figure 4-15: (a) cross-section and (b) Tuning characteristics describing MOS capacitor in inversion, depletion and accumulation regions when D, S, B are connected together

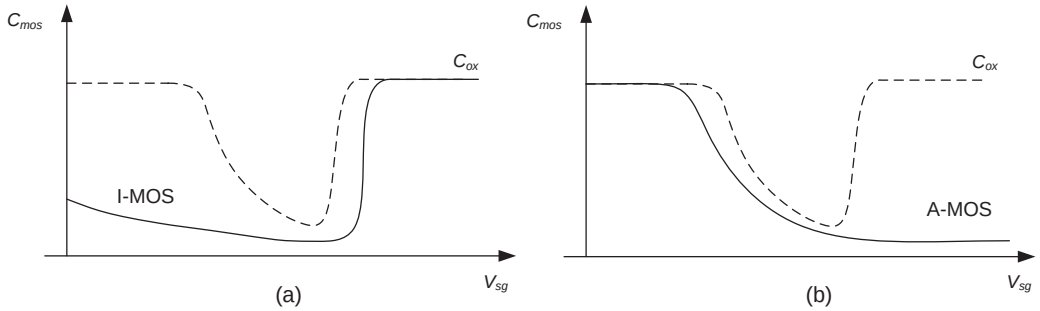


Figure 4-16: Tuning characteristics for (a) the inversion-mode MOS capacitor (I-MOS) and (b) the accumulation-mode MOS capacitor (A-MOS) [171]

In a LC resonator, the nominal tank resonance frequency is given by

$$f_{tank} = \frac{1}{2\pi\sqrt{L(C_p + C_v)}} = \frac{1}{2\pi\sqrt{LC_{tank}}} \qquad (4\text{-}19)$$

The varactor capacitance tuning ratio for maximum and minimum tank capacitance C_{max}/C_{min} can be determined by

$$\frac{f_{tank\_max}}{f_{tank\_min}} = \frac{2\pi\sqrt{L \cdot C_{tank\_max}}}{2\pi\sqrt{L \cdot C_{tank\_min}}} \qquad (4\text{-}20)$$

$$(4\text{-}21)$$

$$\frac{C_{tank\_max}}{C_{tank\_min}} = \left(\frac{f_{tank\_max}}{f_{tank\_min}}\right)^2 = \eta_{tank}$$

Realised capacitance ratio must be larger than required ratio η_{tank}. Therefore we can calculate varactor capacitance tuning ratio as

$$\frac{C_{v\_max}}{C_{v\_min}} \geq \frac{C_p}{C_{v\_min}}(\eta_{tank} - 1) + \eta_{tank} \qquad (4\text{-}22)$$

Since CMOS junction capacitors have relatively poor Q value, it is advisable to use only as much junction capacitance as necessary to achieve the desired tuning range[31]. In a practical design, in order to avoid any excessive degradation of phase noise, tuning ranges are often limited to below 5-10%. A continuous varactor array can improve the linearity of the capacitance tuning-control[172]. The softly switched tuning method provides robust tuning characteristic because the global control linearity of a discrete system has low sensitivity to process, voltage, temperature and RF-input signal.

4.3.3 Folded-Cascode Topology

Aside from RFID's need for low power consumption, another significant design criterions is low supply voltage. A folded-cascode topology can be adopted under ultra low supply voltage condition.

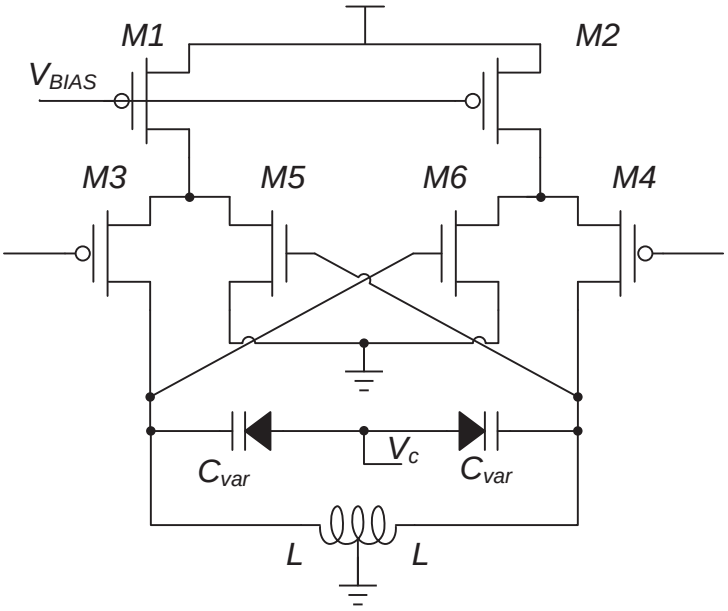


Figure 4-17: The folded-cascode VCO topology

The basic circuit schematic of folded-cascode topology consists of one core positive feedback NMOS transistors (M_5 or M_6) and one coupling PMOS transistor (M_3 or M_4),, as shown in Figure 4-18. This topology enables the current flow though the LC tank only at the drain of the coupling PMOS device. Since only one transistor consumes power over the supply voltage, the operation voltage supply and power consumption can be significantly reduced compared to the conventional cross-coupling differential circuit. The NMOS latches cross-coupled the signal and feeds through the folded-cascode PMOS pass-gates to produce the negative resistance. Furthermore, this topology also compensates the resistive energy loss in the tanks and maintains the sustained oscillation for the VCO. The bias voltage V_{bias} in the circuit diagram is set up carefully to enable PMOS triode region loads M_1 and M_2 providing low resistance path to the supply rail in the circuit [131]. The VDD voltage level will almost remain at the VCO output node since the cascode PMOS coupling transistors are shielded from its source[136]. Therefore, in this way, the supply voltage can be maintained at a low level to keep all transistors in working condition.

4.3.4 QVCO

Two "tail-free" LC tank VCOs provide a direct and a cross connection here that force the two VCOs to oscillate in quadrature. In the Figure 4-19, $M5_I$ and $M6_I$ are NMOS latch transistors for the I-VCO, while $M5_Q$ and $M6_Q$ for the corresponding Q-VCO. In the other hand, $M3_I$ and $M4_I$ play the role of PMOS coupling transistor for the I-VCO and $M3_Q$ and $M4_Q$ for the Q-VCO. The positive feedback NMOS latch transistors and PMOS coupling transistors are connected in a folded cascode structure as described above. In addition, the PMOS cascode pass-gate directly and cross coupled to force the appropriate quadrature interactions between I and Q LC-tank outputs. The ports labelled I+, I- and Q+, Q- are the quadrature outputs of the I- and Q-VCO respectively and these steady-state outputs have the polarities in accordance with I and Q. The phase currents into the LC tanks of the I-VCO and the Q-VCO can be approximately represented as $g_m\vec{Q}$ and $g_m\vec{I}$ respectively, where the g_m denotes the large signal trans-conductance of the coupling PMOSs in the triode region. Since the $\vec{Q}$ equals to $\pm j\vec{I}$ in a quadrature system [173], the LC resonator impedance and the negative resistance latch can be rearranged to $\frac{1}{\pm \mathrm{j} g_m}$. Hence, with an on-chip inductor, the frequency of the oscillator is given by [131]:

$$\omega \approx \frac{\mathrm{R}}{\mathrm{L}}\sqrt{\left(\frac{1}{|\mathrm{G_m}|\cdot \mathrm{R}}\right)-1} \qquad (4\text{-}23)$$

where the average parallel negative resistance $-\frac{1}{\mathrm{G_m}}$ is generated by the cross-coupled latch devices across the cascode devices in a transformation from series to parallel of the resonant tank. Furthermore, since the sustained oscillations only take place at a frequency when the average magnitude of the negative resistance equals to the parallel resistance of the tank $R(Q^2+1)$, no bimodal oscillation will occur in this circuit.

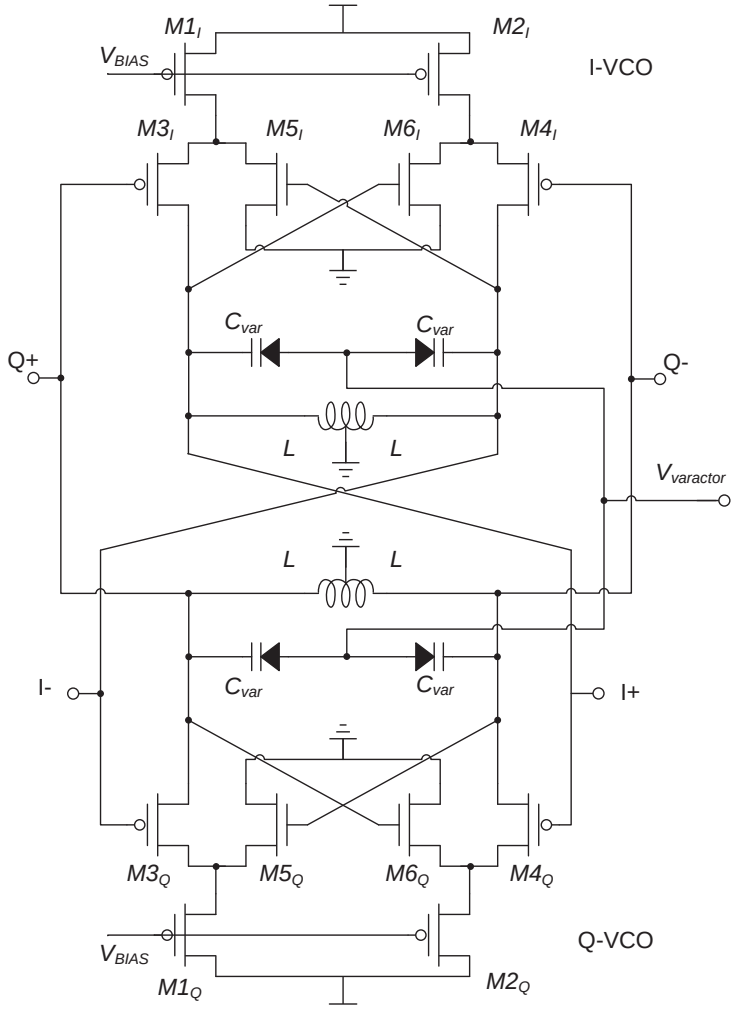


Figure 4-18: proposed fold-cascode CMOS QVCO circuit diagram

4.4 Layout Implementation

The final design task is to implement the circuitry developed in previous chapters with the IBM 0.13μm CMOS8RF (CMRF8SF) process technology. This technology features high density logic integration suitable for RF analogue and mixed signal applications, and offers 5 -8 levels of global metal with common wiring level M1, M2 and MQ. This research used 6 metal levels and aluminium (MA) as the last metal at a larger pitch for design. As the cross section in Figure 4-20 shows, it includes one (or two) thick copper levels MQ with aluminium (LY) and thick copper (E1) and thick aluminium (MA) levels.

Perhaps the most important consideration, when laying out a precision analogy design is how to avoid large Torrance. Several papers discussed the strategy of performance layout design, especially for RF design [174-176].

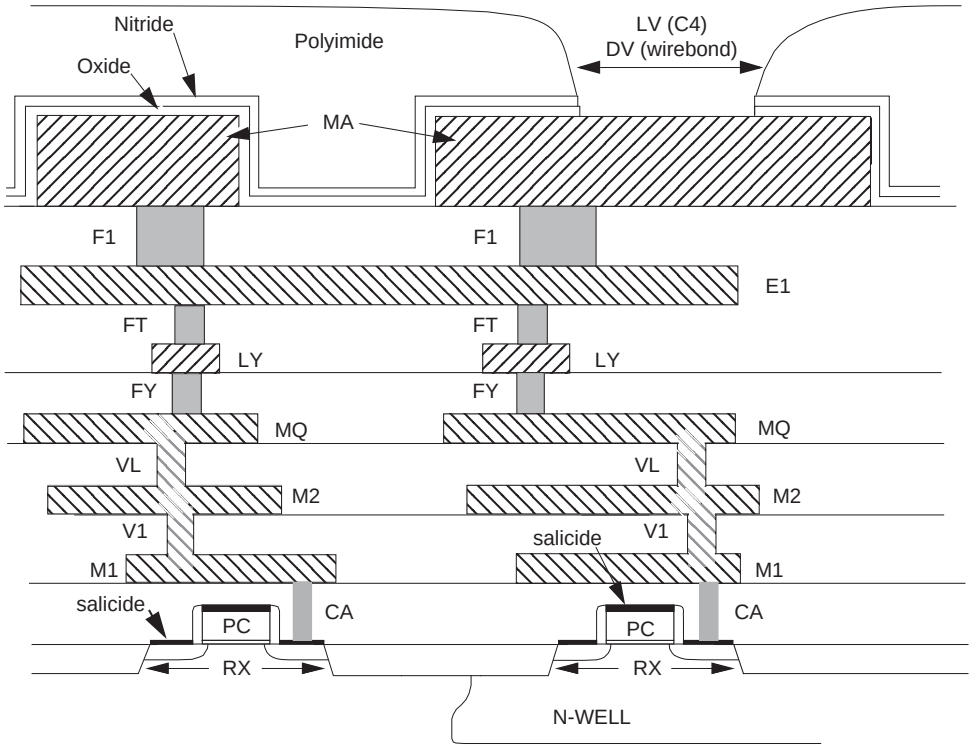


Figure 4-19: Cross Section of the 6 Level of Metal "MA" Last Metal Option (2 Thin Mx: x=1,2 and 1 Thick = MQ and RF Metal = LY, E1, MA) with either DV or LV as final Passivation[103].

4.4.1 Layout Consideration for Passive Components

Spiral Inductors

The top metal is most commonly used for passive RF elements: e.g. inductors. As the distance between the top metal layer and silicon substrate increases, the parasitic capacitance is reduced.

The spiral inductors provided from IBM CMOS8RF use primarily the last three levels from Figure 4-20. The inductors are fabricated using 5μm wide traces of top thick aluminium layer (MA), interconnected through via contact (F1) with thick copper layer (E1), which is used as an underpass contact to the spiral centre. The ground plane of the spiral inductor contacts the BFMOAT (or Metal) ground plane, as shown in Figure 4-21

(b). This composite structure is designed to maximise self resonant frequency and optimize the quality factor since it reduces the substrate parasitic of the spiral inductor [177]. A test result shows that by using of poly-shields for instance, both the quality factor and the tolerance level are improved [176].

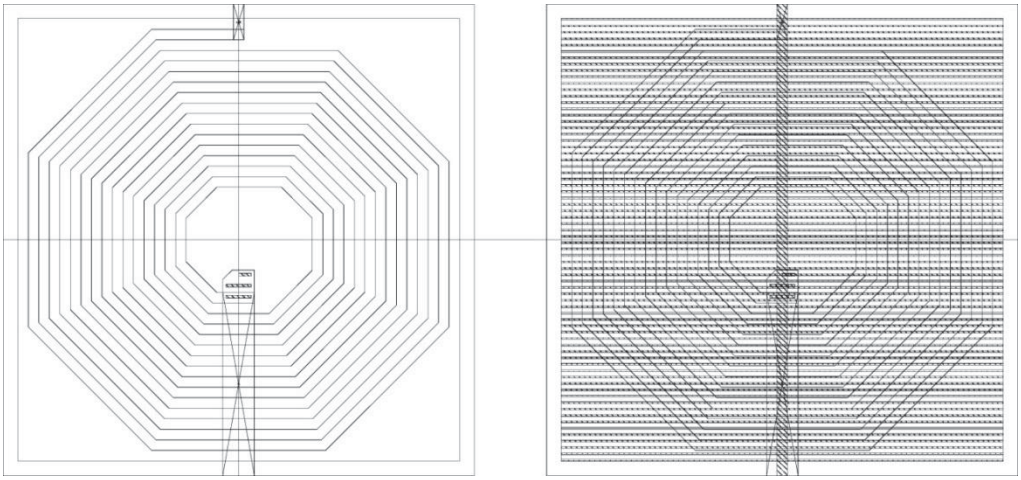


Figure 4-20: (left) a standard inductor and (b) with metal M1 ground-plane shield structure

MIM Capacitors

The most area efficient capacitor type in CMOS technology is the double-poly capacitor. Lot of effort has put into the design of metal-metal sandwich structures to reduce the overall cost and its analogy feature.

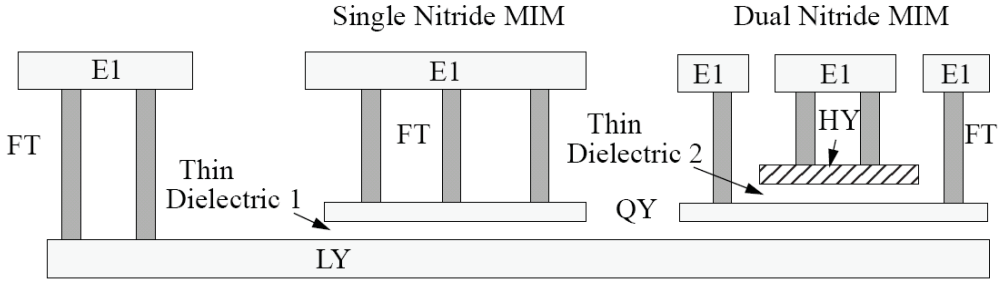


Figure 4-21: Cross Section of the MIM capacitors

The dual aluminium nitride metal-to-metal (MIM) capacitor from the CMRF8SF process is formed by adding a thin insulator and a thin metal layer (HY) and another thin layer of metal (QY), between E1 metal and the underlying layer of metal LY. Another thin metal layer QY is connected to E1 with the via level FT to construct a sandwich form for the double-poly capacitor, as shown in Figure 4-21.

Poly Resistor

The CMOS8RF technology provides several types of resistors and resistor geometries. As shown in Table 4-2, the p+ ploy layer resistor (OPppcres) is selected due to its reasonably high sheet resistance (340 Ω/□), low tolerance, lower parasitic capacitance and smallest minimum ground-rule layout dimension. In order to achieve higher resistance, multiple numbers of series bars are used in the layout design.

Table 4-2: Comparison for different resistor technology [19]

Specification	N+ S/D Resistor	N-Well Resistor	P+ Poly Resistor	RP Poly Resistor	RR Poly Resistor	Kx BEOL Resistor	L1 BEOL Resistor
Sheet Resistance (Ω/□)	73	540	340	228	1700	58.5	60
Tolerance (%)	13	19	14	8	20	9	9
Parasitic Capacitance ($fF/\mu m^2$)	1.05	0.93	0.0838	0.08	0.08	0.03	0.01
Mis-match Sensitivity (%)	0.4	0.3	0.4	0.7	0.6	0.1	0.1

4.4.2 Layout Consideration for MOSFET

Large device widths and minimum gate lengths are required for MOS transistor to achieve high g_m and maximum operating frequency. Similar to all modern CMOS processes, the IBM 130nm process also uses a P-type substrate. All PMOS devices must therefore reside in an N-well. Whenever a PMOS devices' source terminal does not connect directly to *Vdd*, a design decision must be made for an appropriate connection for the N-well body thermals. Connecting the N-well to *Vdd* simplifies layout and reduces parasitic capacitances at the source terminal. The only drawback is the larger PMOS threshold voltage when N-well (Bulk terminal) was connected to PMOS's source terminal. However this makes no difference to the circuit design in this thesis and the difference does not significantly affect the circuit.

In terms of layout design for transistors, multi-fingered layouts are commonly applied for RF design. The cut-off and maximum oscillation frequencies can be increased by use of multiple fingers [31]. Another significant advantage of using multiple fingers is that it offers a large reduction in the gate's resistance; thereby, giving better noise performance. Furthermore, multi-fingered layout tends to reduce the overall spread on chip area. In the designs, all the transistors have single finger width of approximate 5μm.

4.4.3 Layout Consideration for I/O Terminals / Pads

The actual receiver requires little in the way of external interfacing. It is a fully integrated receiver designed to interface directly with the antenna input signal (usually single-ended). The LNA and mixer only require DC operating suppliers, while the VCO operates individually with an initial start-up DC power supply and a bias controlled voltage for varactor. However, more external connections are necessary to check the analogue signal performance for each front-end block. Table 4-3 lists the analogue and digital I/O implemented on the test device.

Table 4-3: Complete list of input and output ports on the implemented design.

Name	Description
Vsig_sin	Original single-ended RF input signal
Vsig+	Differential (+) RF input signal
Vsig-	Differential (-) RF input signal
VLNA_sin	Single-ended output RF signal after LNA
VLNA+	Differential (+) RF signal after LNA
VLNA-	Differential (-) RF signal after LNA
VBalun+	Differential (+) RF signal after active balun
VBalun-	Differential (-) RF signal after active balun
I-VLO+	In-Phase (+) LO signal from I-QVCO
I-VLO-	In-Phase (-) LO signal from I-QVCO
Q-VLO+	Quadrature (+) LO signal from Q-QVCO
Q-VLO-	Quadrature (-) LO signal from Q-QVCO

VIF+	Differential (+) IF signal after Mixer
VIF-	Differential (-) IF signal after Mixer
VLNAdd	DC Supply Voltage for LNA
VMIXdd	DC Supply Voltage for Mixer
VVCOdd	DC Supply Voltage for VCO
VLOb1	Bias voltage for LO
VLOb2	Bias voltage for varactor in LO

In the actual design, either C4 plated terminals or wire bond terminals may be used for I/O pads. The active C4 terminal with MA last metal structure is a solder ball over a transition metallurgy pad. The size of the wire bond pads used for CMOS8RF technology is for standard gold ball bonds (90μm). The width of the I/O pad in this design is 110μm that is also compatible with probe skating. To be noticed, although the size of integrated circuits in deep-submicron CMOS technology is dramatically shrunk, the bond pad has a relatively large size for wire bonding. In other words, the large parasite capacitance of bond pad often limits the performance of the circuits in RFIC [178]. As most fixture display relative tolerances, these parasitic capacitances should be kept as small as possible so as to reduce the absolute uncertainty of the measurement.

Two kinds of probe pad patterns (ground-signal-ground, GSG) are shown in Figure 4-22. For two port microwave wafer probing[179], the conventional probe pad structure has a higher loss due to low CMOS substrate resistivity. Its cross-sectional view and its equivalent circuits show the existence of parasitic fringe capacitance (C_1) and a lossy $C_2 - R_S - C_3$ path, which introduces substrate parasitic effects, as shown in Figure 4-22(c).

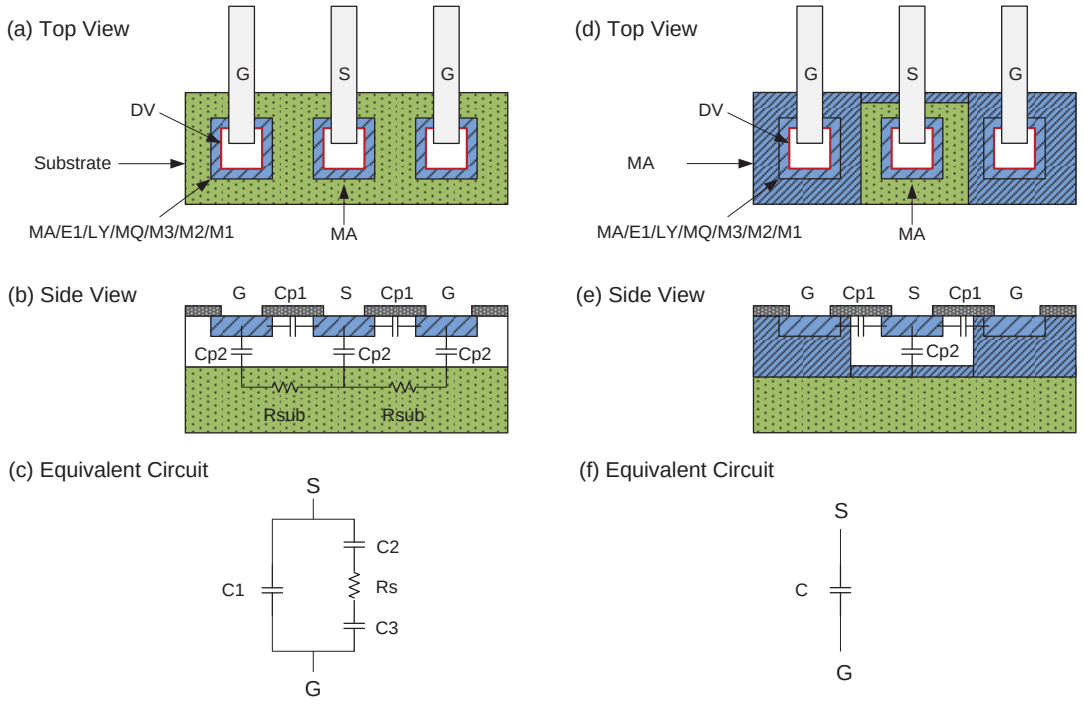


Figure 4-22: One-port GSG top view, side view and the simple equivalent circuit for (left) the conventional probe pad layout and (right) ground shield underneath pad layout

The second probe pad pattern uses a ground shield underneath the signal pad, as shown in Figure 4-22(d) and (e). Using ground shield under the signal pad has several advantages in CMOS RF probing. One benefit is that coupling between the probes ports will be minimised compared to the unshielded pad structure since the signal pad is isolated from the substrate and hence signal leakage is prevented from signal pad to substrate. This coupling becomes important especially in a CMOS technology with a low substrate resistivity. Ground shield is achieved by connecting using the top metal layer *MA* straight to the ground pad. The *MA* layer should be extended in every direction around and under the signal pad to prevent peripheral fringe capacitance to the substrate. Another benefit of the process of de-embedding the pad is that the equivalent circuit of the pad parasitic is only capacitive with a high quality factor (Q), as shown in Figure 4-22 (f) [180]. However by using extensive substrate grounding near the signal pad (pseudo ground shield), the tolerance levels are increased as the low-accuracy oxide layer now dominates the impedance[176].

Figure 4-23 in next page shows the completed layout diagram for the RF front-end that includes singled-end LNA, differential LNA, QVCO, Mixer and Baluns.

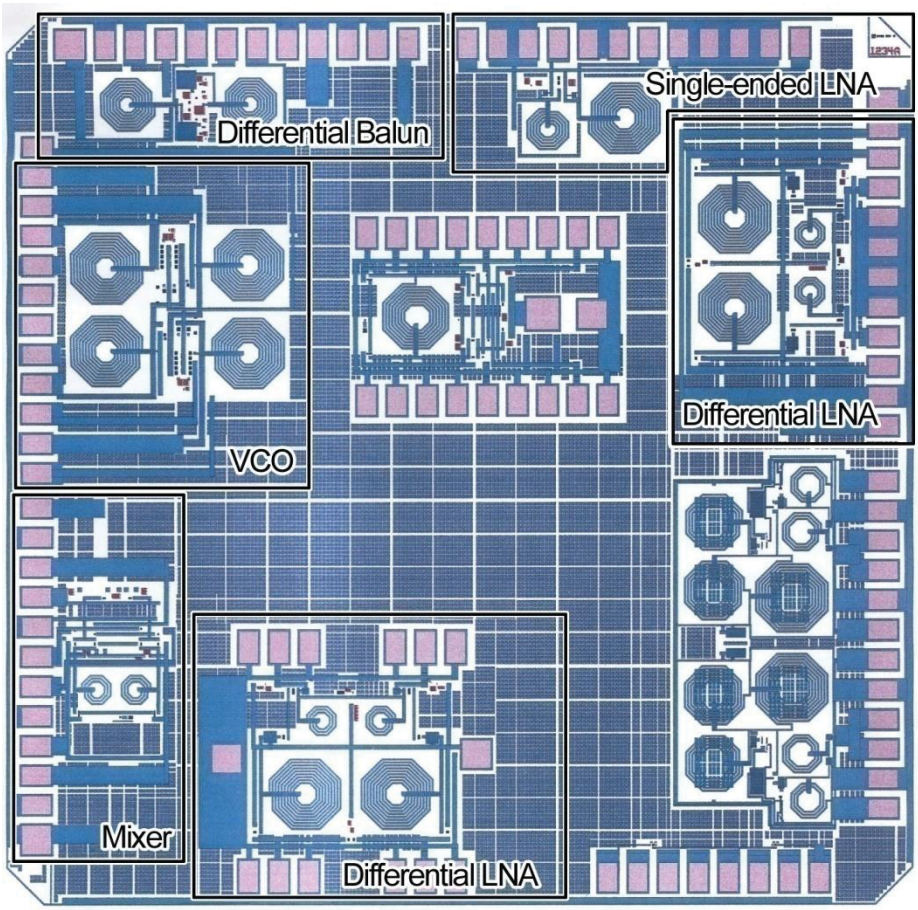


Figure 4-23: Completed layout diagram for the RFID front-end

4.5 Summary

This chapter presents the implementation procedures and the design trade-off considerations for each RF front-end block. The aim of this chapter is to carry out the designs with the consideration in cost, power consumption, noise performance, linearity and high integration. This design implementation was also evaluated in terms of its sensitivity, selectivity, spurious response, dynamic range and stability. Different topologies, techniques, and components are discussed to overcome those problems mentioned in previous chapters.

The considerations in Layout implementation were also discussed for passive and active components, as well as pads. These considerations are critical and will also affect the performance of simulation and measurement results as we will see in Chapter 5.

CHAPTER 5: SIMULATION, SETUP AND RESULTS

In this chapter, work undertaken to experimentally verify the previous chapter's RFID receiver front-end's design is presented; where the chapter's contents are ordered as follows: in the first place, the methodology employed verifying the front-end's blocks' operations is discussed; Second, several critical figures of merit are simulated by software, including the S-parameters, power consumption, linearity, noise figure, phase noise level, stability and so on; third, the simulation method is explained and discussed to evaluate the system performance; since the design is intended to investigate the effect of variations in all of the above parameters, many individual tested results were characterised to obtain information on the correlation between the simulated parameters next; proper testing methodology and testbench is investigated for robust test results during the test experiments at the same time; in the end, the practical measurement result is achieved.

5.1 Simulation and Measurement Setup

5.1.1 Simulation Technique

Cadence Design System's circuit simulator Spectre RF includes several useful RF circuit analysis tools, including Periodic Steady-State (or PSS) and Periodic small-signal analysis methods. The PSS analysis directly computes the periodic steady-state response of a circuit. The Periodic small-signal analysis uses the PSS solution as a periodically time-varying operating point that is used for linear calculation, which then achieves the response of the circuit to small perturbation sources. The periodically time-

varying linear model of the circuit can be developed to represent frequency conversion. Spectre RF provides a variety of periodic small-signal analysis, including periodic AC (pac), periodic noise (pnoise), periodic transfer function (Pxf), periodic s-parameter (psp) and periodic stability (pstb). Due to the effectiveness of these analyses, Spectre RF is the dominant simulator for RF integrated circuits and is thus used in this thesis.

In general, RF analysis is performed by measuring the DC operation status, power dissipation spectrum, AC signal response, noise performance, scattering parameters (s-parameters). In following chapter, each simulation analysis is carried out with its definition, results analysis and discussion. These simulation results are compared with theoretical results for performance evaluation. In the end, some critical measured results are obtained for the practical chip.

5.1.2 S-parameter Measurement

In a RF device, isolation defines how much signal leakage will occur between ports. The signal reflection from output to input can degrade system performance and further disturb other parts of the system. S-parameter analysis is used to measure the input impedance of the two-port system. A vector network analyser (VNA) is used to measure the two ports s-parameter of the device under test (DUT). The test frequency is generated by a variable frequency source and fed to the input ports.

Prior to performing the S-parameter measurement with a VNA, an accurate calibration is necessary. Nowadays, sufficiently advanced calibration with systematic errors correction is available on the VNA. A full 2 port calibration can improve uncertainty and dynamic range of the DUT measurement. Furthermore, calibration will effectively eliminate all sources of systematic errors inherent in the VNA measurement system.

Measurement for more than two ports DUT, such as typical mixer, can be obtained using a standard 2-port calibrated VNA with extra measurements taken by the correct interpretation of the results obtained. The S-parameter matrix can be accomplished from successive two port measurements at a time, with the unused ports being terminated in high quality loads that are equivalent to the system impedance. The potential risk of this approach is the return loss or VSWR of the loads themselves, which must be suitably specified to be as close as possible to perfect system impedance, typically 50Ω. Some VNC associated analysis software is available to determine the worst acceptable VSWR of the loads.

An Agilent DCA-J18000C is used in this work for time domain reflectometry (TDR) calibration and S-parameter measurement for the chips. It is also used to model the accurate transmission media characterization for the DUT. The completed test equipment is shown in Figure 5-1.

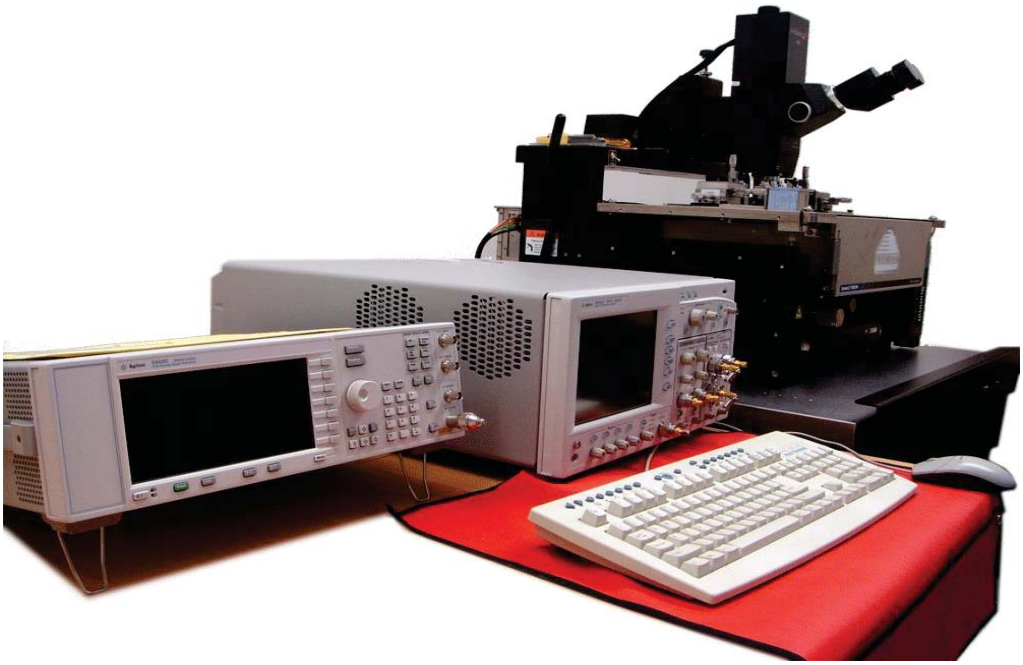


Figure 5-1: Facilities for S-parameter Measurement

5.1.3 Linearity Measurement

Linearity, defined in Chapter 3, can be represented by intermediation (IM3) and measured by applying two closely spaced input tones at frequencies f_1 and f_2. In the case of a mixer, the third order products from the mixing of these tones with the LO (at frequency f_{LO}) occur at frequencies given by $(2f_1 \pm f_2) \pm f_{\mathrm{LO}}$ and $(2f_2 \pm f_1) \pm f_{\mathrm{LO}}$. Only $(2f_1 - f_2) - f_{\mathrm{LO}}$ and $(2f_2 - f_1) - f_{\mathrm{LO}}$ are of interest as they fall in, or close to the IF band. The IM3 performance is often summarized by giving the 3rd order intercept point (IMP3 intercept) intersected between fundamental RF input signal and IM3 (or/and IM5) with the extrapolated gain plot. As a rule of thumb, the IM3 intercept point is approximately 10dB above the 1dB compression point.

5.1.4 Noise Measurement

LNA and mixer noise measurement was performed outside the campus. The DUT was mounted on Rogers PCB laminate with properly biased tees settings. External tuner matching was required since the device was degenerated due to the package and pads. A grounded fence was located both above and below the DUT to reduce induced parasitic parameters. The procedures for DUT noise measurement used a low noise floor oscilloscope as shown in Figure 5-2, which is similar to that in paper [181].

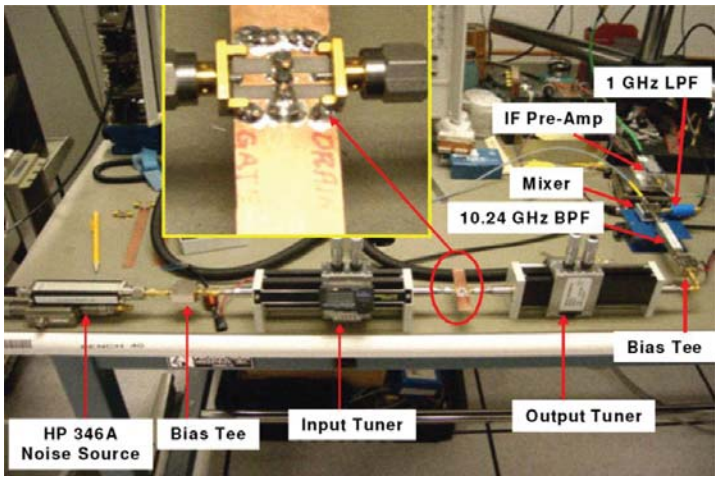


Figure 5-2: Test Setup for Noise Figure Measurement from [181]

5.1.5 Phase Noise Measurement

Since the phase noise is the critical property for VCO design, the measuring techniques need to be treated carefully with diversification. The techniques for measuring the phase noise include direct spectrum measurement technique, demodulation technique and so on. Firstly, the deviations from the pure sine wave signal need to be quantified to determine their output effect. The basic phase noise measurement concept is given by:

$$V(t) = V_0\left[1 + \frac{\alpha(t)}{V_0}\right] sin[2\pi v_0 t + \emptyset(t)] \qquad (5\text{-}1)$$

Where $\alpha(t)$ represents amplitude variations or amplitude modulation of the signal and $\emptyset(t)$ represents the phase fluctuations modulating the ideal linear phase change of the signal.

With a spectrum analyser, all signals appear as sidebands on either side of the carrier and provide spectral density of $S_v(v_0 \pm f)$ from a given offset. The single sideband phase noise of a signal is measured in quantity perspective as $L(f)$. It is in power format since the phase fluctuations of the carrier signal are normalized to the total signal power. $L(f)$ can be achieved directly from the spectrum analyser if the AM noise is much less than the PM noise. In other words, the phase noise sidebands to be measured must be greater than the spectrum analyser's own noise by at least 10dB [182]. Necessary corrections for the normalization are required for a 1Hz bandwidth and to account for the logarithmic scaling of the spectrum analyser. The spectrum analysers used to perform direct spectrum measurement of phase noise should include a synthesised local oscillator to prevent their own drift from affecting the result.

Alternatively, performance demodulation of the amplitudes, phase or frequency, fluctuations can produce a time-domain voltage $v(t)$ as:

$$v(t) = v_0 + \frac{1}{2\pi}\frac{d\emptyset(t)}{dt} \qquad (5\text{-}2)$$

The analysis of this baseband signal can further generate the spectral density of the amplitude fluctuation $S_A(f)$, the phase fluctuations $S_\emptyset(f)$, or the frequency fluctuation $S_v(f)$. The single sideband phase noise $L(f)$ can be calculated from the $S_\emptyset(f)$ or $S_v(f)$ only if the mean square phase fluctuations $\emptyset^2(t)$ are small relative to one radian. The spectra densities of phase and frequency fluctuations are directly related to the square of the offset frequency in a same oscillator, as shown in Figure 5-3.

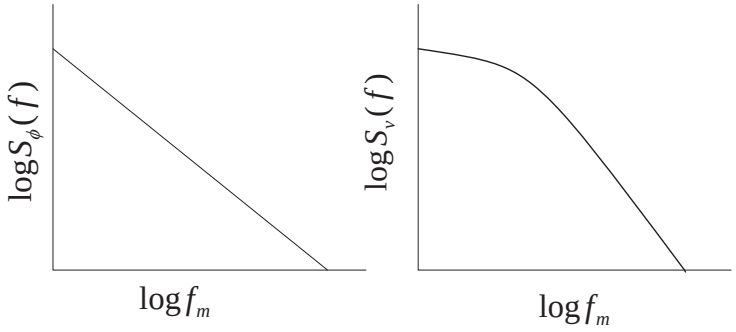


Figure 5-3: The representations for spectra densities of phase (left) and frequency (right) fluctuations

5.1.6 Frequency Pushing Effect Measurement

One conventional way to measure frequency pushing is to compute the VCO frequency for different tune voltage at its normal supply voltage. Verifying and recording the VCO frequency behaviour on different tune voltages is carried out either by increasing or decreasing the supply voltage with a specific amount in voltage change (Δv).

5.2 Low Noise Amplifier

5.2.1 Simulation and Measurement Setup

Both single-ended and differential LNA are designed and simulated with the testbench in Figure 5-4 (a) and (b) respectively. The singled-end LNA topology was based on Figure 3-11. The CS inductance degenerate transistor M_1 has corresponding size of 250/0.12µm. The cascode stage CG transistor M_2 was chosen to have the same size as M_1. Source impedance R_s is a standard 50Ω. The degenerate spiral on-chip inductor L_s with ground-plane shield was given a small value of 1.2nH. The capacitor C_{ex} is added parallel to C_{gs1} of M_1. In addition to power reduction, C_{ex} also reduces the input network Q value, which is significant to enhance the linearity. Typical value for C_{ex} is between 1.5 to 2.5 times of C_{gs1} value and therefore it is approximately 580fF. The gate inductor L_g is used to eliminate the rest of imaginary part of input impedance and match the input to the signal source impedance of 50Ω. The calculated value of L_g was 46nH, which is implemented externally by either discrete components or the microstrip transmission line matching that will be further explained in the following chapter.

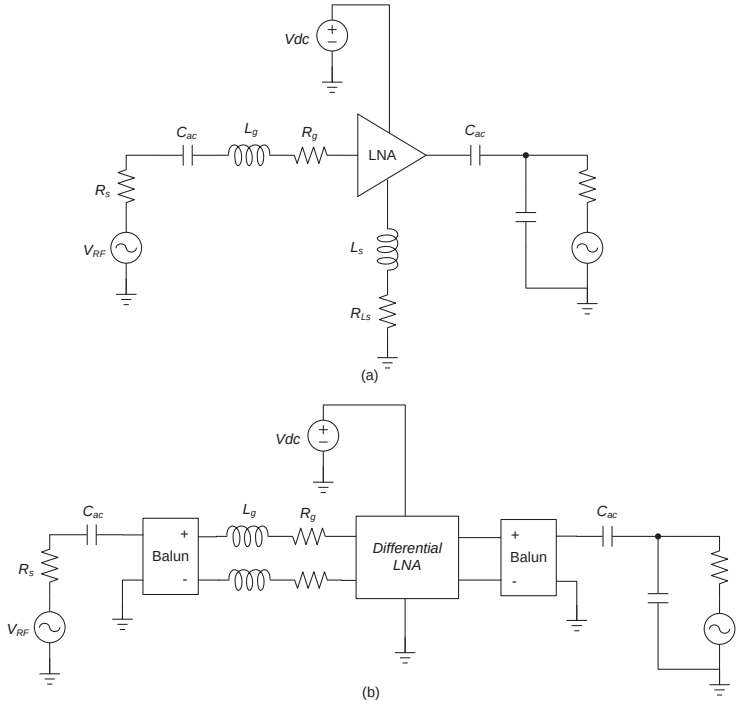


Figure 5-4: Testbench for (a) single-ended LNA and (b) differential LNA simulation

The capacitor C_{ac} is used to block the reverse bias of DC voltage from M1. Similarly, another capacitor C_{ac} is located at output port for DC voltage block and both are implemented off-chip.

The size of current mirror transistor M_3 is 18/0.12μm. The current of M_1 is dependent on the current reference resistor R_{ref}, which is in series with M_3. A resistor R_B, with large value, sits between the current mirror and CS stage to filter out the inducted noise current from M_3

Output tank inductor L_d and capacitor C_d was selected to force the load of LNA beyond 250Ω, which is necessary to achieve high gain. Their values are 11nH and 3.1pF, respectively. Obviously, either buffer or external impedance matching is required to perform the impedance transformation.

Both singled-ended and differential LNAs (as part T8BTAU) were fabricated using the 130nm IBM CMOS fabrication process available through MOSIS. Figure 5-5 shows the layout diagram and the micro-photograph of the die for singled-end LNA. It occupies a total area of 0.57mm^2 (with pads and border). The outer diameters of the inductors were respectively 240μm for L_d and 140μm for L_s with 5μm wide trace of top thick aluminium layer MA and underpass contact copper layer E1. The capacitors C_{ex} and C_d were fabricated as MIM capacitors and the resistors were fabricated using poly layer with high sheet resistance (340Ω/□). In the meantime, the differential LNA layout was also designed and sent to the foundry for fabrication and testing. The layout of the differential LNA is shown in Figure 5-6.

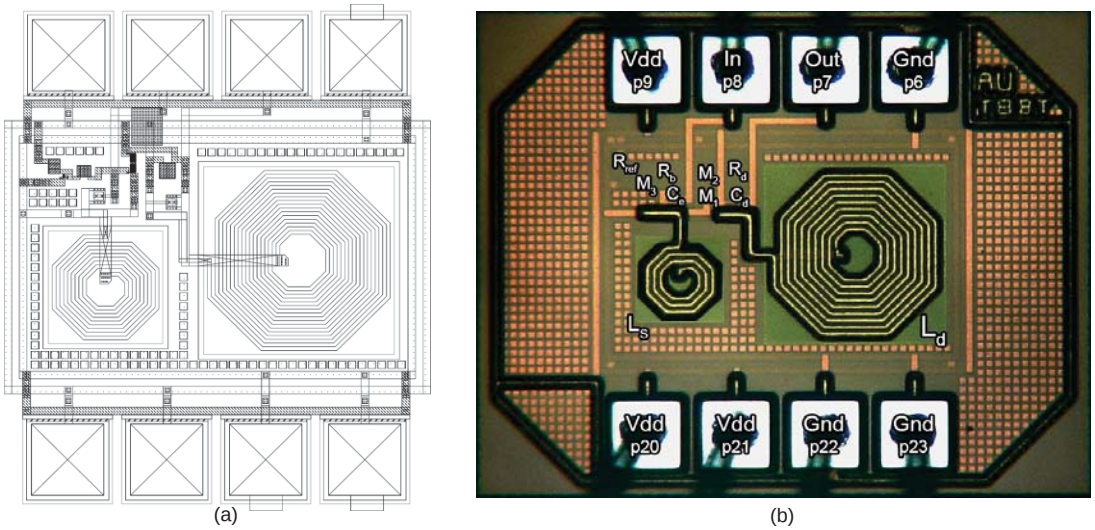


Figure 5-5: (a) Singled-ended LNA layout diagram and (b) its die microphotograph

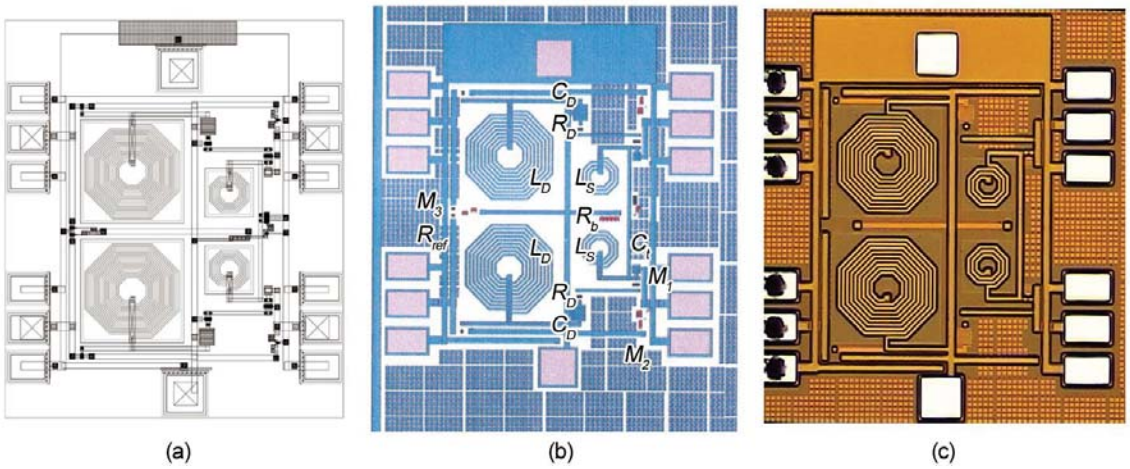


Figure 5-6: Differential LNA (a) layout diagram, (b) fabricated die diagram, and (c) die microphotograph from Figure 4-11

5.2.2 Packaging Modelling and Impedance Matching

After the wafers are fabricated by the foundry, the qualified wafers are sent to a packager for dicing, assembly and packaging in order to physically connect to the "outside world". The die chip is packaged by bond-wire according to a bonding diagram provided.

A ceramic package was selected initially due to its cost effectiveness; however, ceramic packages possess high parasitic components, which require de-embedding. In addition to the package material, die size and package technology were considered as well. A die chip is placed in the cavity of the packages and connected each other through the wire bonding. A typical die also contains the overhead and residual scribe lanes from the foundry that may require some extra space between the die edge and the package cavity edge. Various package technologies have been developed according to the die size and I/O pin numbers. Dual in-line package (DIP), sometimes also called a DIL package, is one of the common package technology in microelectronics for small number of pins allocated in two rows. Figure 5-7 shows a single-ended LNA packaged in 28-pin ceramic DIP packages with its external connections for one of the design in this thesis.

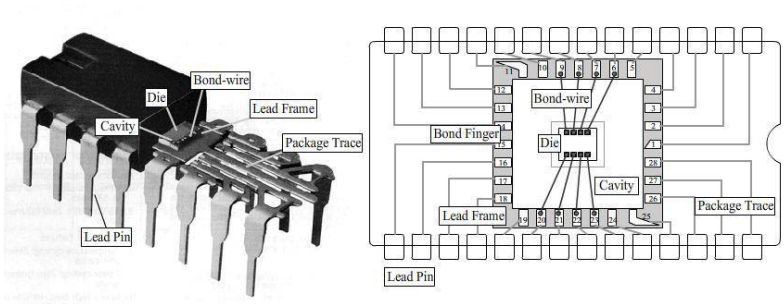


Figure 5-7: a singled-ended LNA die packaged in a plastic DIP28.

In RFIC design, the electrical parameters of the package must be taken into account at the design stage. For this reason, an accurate and scalable package model representing the package lead and bond wire is highly desirable and was the driving force for this work. In this packaging structure, the parasitic electrical parameter will not just count for the bond wires but also the package trace for defined package. Therefore, a complete electrical parameter model for the package is represented in Figure 5-8. With a properly setup testbench, the open circuit de-embedding technology can be used for achieving the electrical parameter just for the bond wires [183, 184]. Thus, each electrical parameter from the bond wire can be extracted.

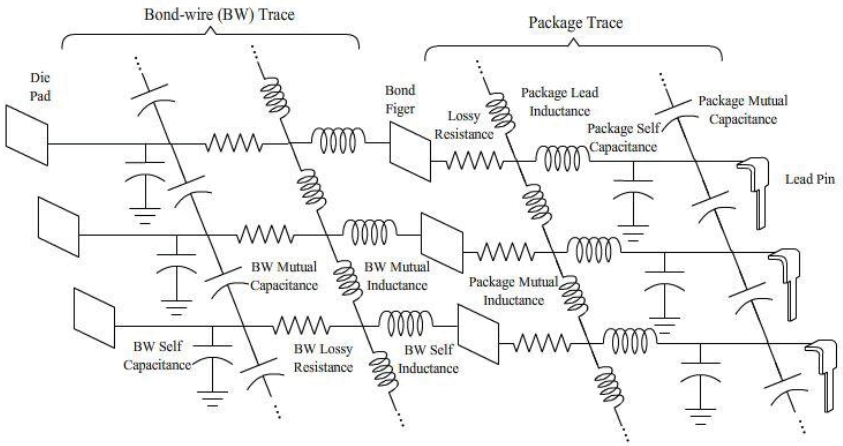


Figure 5-8: Parasitic components model between die pad and package lead pin.

Since bond wires and package introduce extra passive components, an impedance re-matching network is necessary. Moreover, the influence of interconnect parasitic on crosstalk noise in the wafer levels becomes more and more severe because of the high-frequency dispersion and higher losses on the silicon substrate. In millimetre-wave frequency design, microstrip line and coplanar waveguide line have been widely used for impedance matching network[185]. Figure 5-9 demonstrates a traditional parallel-plate microstrip line. The conducting strips are etched on one side of the PCB, while the other side of the PCB is usually treated as ground plane to help prevent excessive field leakage. This structure reduces radiation loss [186]. The current and voltage flow is confined to two plates separated by a dielectric medium.

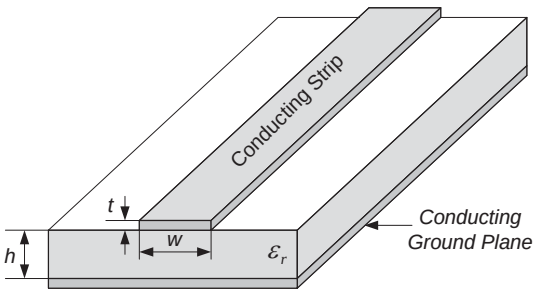


Figure 5-9: Microstrip transmission line geometry

The shortcomings of this kind of single layered PCB are: high radiation loss and interference between neighbouring conductor traces. Hence, substrates with high dielectric constants ε_r are preferred for achieving high board density of the components' layout as they minimise field leakage and cross coupling. Multilayer techniques are also widely used to achieve balanced circuit board design. However, they also increase the cost and complexity in fabrication process. Instead of using wafer levels, the PCB circuit board levels are implemented with same principle but with more flexibility and less unexpected interference.

The matching methodology is carried out by using the Smith Chart. Matching circuit design for an amplifier can be easily and quickly achieved by using the normalized impedance and admittance Smith Chart by some computer-aided softwares [187, 188]. In addition, the Smith Chart is also used to present the frequency dependence of scattering parameters and other characteristics [189].

5.2.3 Case Study of Microstrip Line Impedance Matching

As an example, a generic matching network configuration is carried out for the single-ended LNA, as shown in Figure 5-10. The measured input power reflection S_{11} and output power reflection S_{22} are known from simulation. A matching network that consists of a series microstrip transmission line connected to a parallel open-circuit or short circuit stub is used for standard port impedance matching (50Ω) [190]. Four adjustable parameters are considered and calculated in this case: length l_S, characteristic impedance of the stub (either open- or short-), length l_T and characteristic impedance of the series transmission line segment.

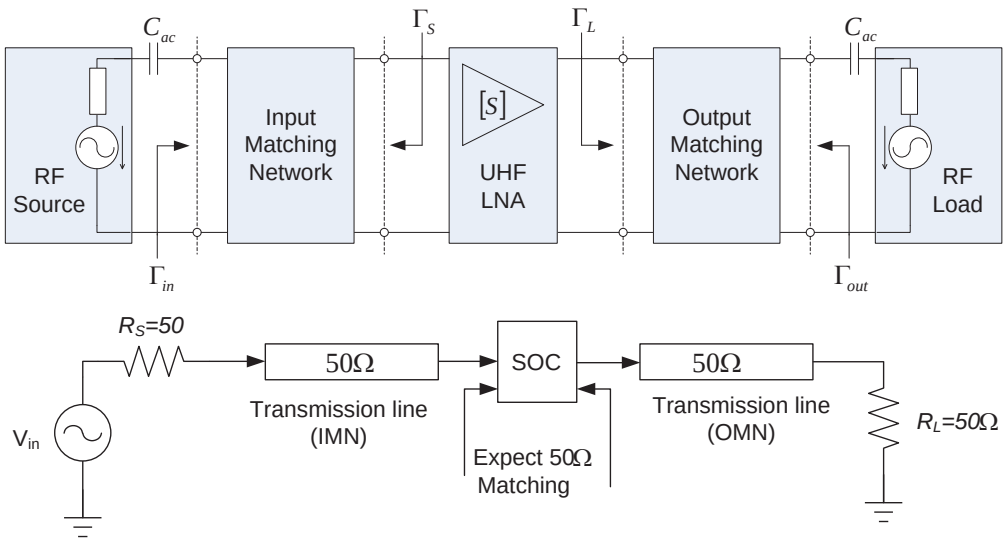


Figure 5-10: Generic LNA with Matching Network

In order to achieve maximum unilateral transducer gain, where signal flows only in one direction, we make the assumption of reverse isolation S_{12} approaching 0. From the equation for S-parameters [191], the source and load reflection coefficient towards the LNA needs to become the complex conjugate of S_{11} and S_{22}. The matching procedure can be quite confusing without deep understanding and proper considerations. The general method used in the matching circuit is to choose either "toward the load" or "toward the generator" on Smith Chart depending on the output or input matching network respectively. The source reflection coefficient needs to take the conjugate of S_{11}, while the load reflection coefficient does not [192]. The method used in this thesis follows a unified procedure that can be adopted in both input and output matching networks but by taking both source and load reflection coefficients from the backside of an amplifier toward the input or output line, which is the complex conjugate of S_{11} and S_{22}. From the reflection coefficient points on the Smith Chart, only one direction "toward the load" needs to be focused on. Therefore, the source and load reflection coefficients can be converted to impedance format or angular format in either z-chart or y-chart in Smith Chart.

The basic concept for input impedance matching is to select the length l_S of the stub such that it produces a susceptance B_S sufficient to move the normalized input admittance $y_{in} = 1$ (or $z_{in} = 1$) to SWR circle that passes through the normalized source impedance point, as shown in Figure 5-11. It is notable in this figure that the source SWR circle associated with source impedance intersects the constant conductance circle g=1 at two points suggesting two possible solutions: short-circuit stub and open-circuit stub.

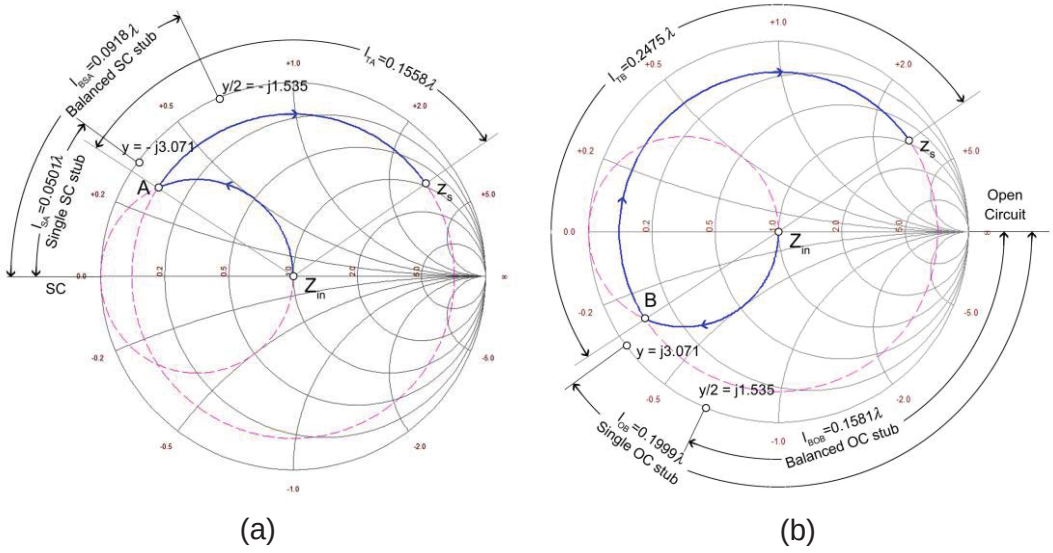


Figure 5-11: Analysis of two possible (a) short-circuit single-stub and (b) open-circuit single-stub matching networks for an input matching system example.

The length of a short-circuit stub can be found in the Smith Chart by measuring the corresponding length l_{SA}, starting from the $\Gamma_0 = -1$ point on the real axis (short circuit) and moving along the outer perimeter of the Smith Chart g=0 toward the generator (clockwise) to the intercept point A. The short-circuit stub can be replaced by an open-circuit stub if its length is increased by a quarter wavelength. Similarly, the open-circuit stub and short-circuit stub can also be calculated for point B.

This substitution may become necessary in printed circuit design. Open-circuit subs are sometimes preferred because they eliminate the deployment of a via, which is otherwise necessary to obtain the ground connection for a short-circuit stub. This through-hole connection in printed circuit boards will result in additional parasitic inductances. However, at high frequencies, it is very difficult to maintain perfect open-circuit (as well as short-circuit) conditions because of changing temperatures, humidity and other parameters of the medium surrounding the open transmission line. Moreover, in order to minimise the circuit layout area, the first priority is to select the shortest line segments.

The length of the series transmission line segment can be calculated by the phase rotation along the SWR circle from Smith Chart. Selecting either point A or B on the circle rotates on the direction of "toward generator" to the Z_S. Sometimes it is preferable to say from Z_S "toward load" to either point A or B on the SWR circle.

The output matching network follows the same procedure as input matching process. To minimise the transmission interaction between the shunt stub and transmission line segment, the shunt stub must be balanced along the transmission line. For this, admittance of each side of balanced shunt stub must be equal to half of the total admittance. It is notable that the length for balanced open-circuit stub can be either increased or decreased from the single stub situation. The complete LNA matching procedure is performed in detail in Appendix 8-7 with the complete input/output impedance matching network diagram for single and balanced stub, as shown in Figure 5-12. Figure 5-13 illustrates one example of impedance matching network by using single open-circuit stub from Figure 5-11 (b).

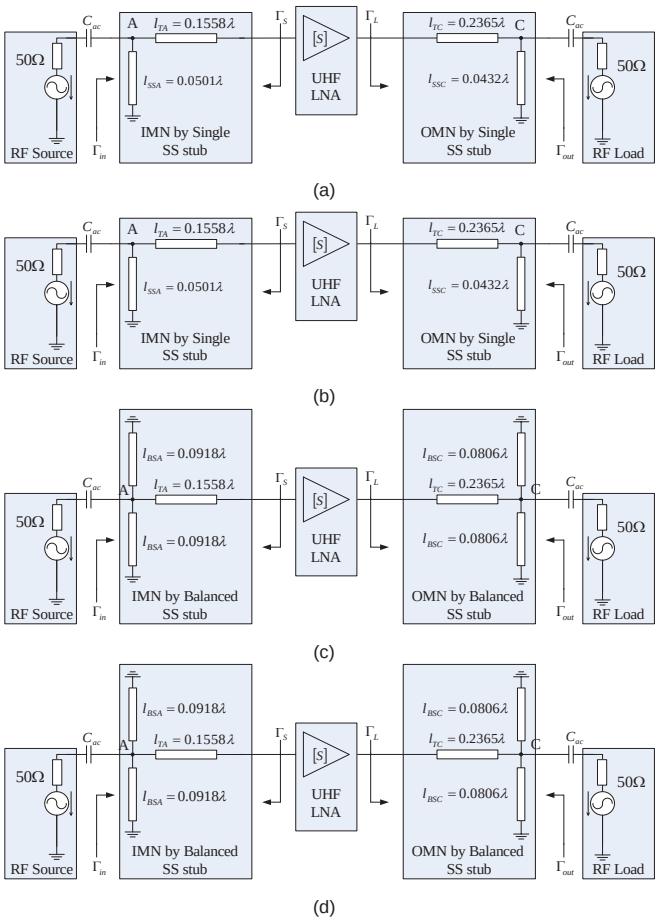


Figure 5-12: Complete LNA matching schematics using (a) single short-circuit, (b) open-circuit stub, (c) balanced short-circuit and (d) balanced open-circuit stub

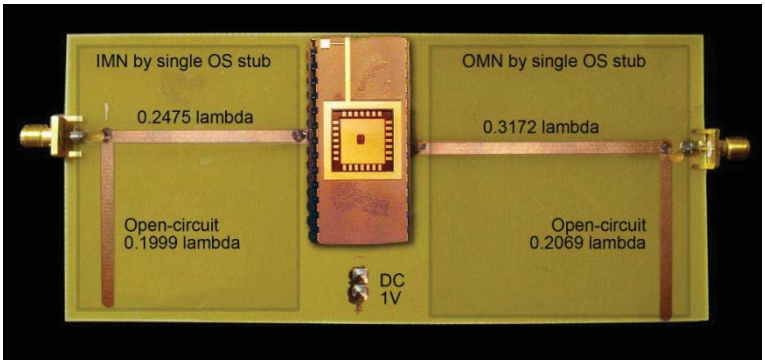


Figure 5-13: Impedance matching network by both using single open-circuit microstrip transmission line stubs

5.2.4 Results

Power dissipation

By performing the DC analysis of the circuit, we can calculate the total amount of current consumed by the LNA. With a supply voltage ranging from 0.5 to 1.5V, the tail current of the single-ended LNA ranges from 0.75 to 4.8mA, as shown in Figure 5-14. This single-ended LNA provides impressive power dissipation, such as 0.4mW at 0.5V and 0.83mW at 0.7V power supply voltage. However, the supply voltage directly impacts the gain of the amplifier.

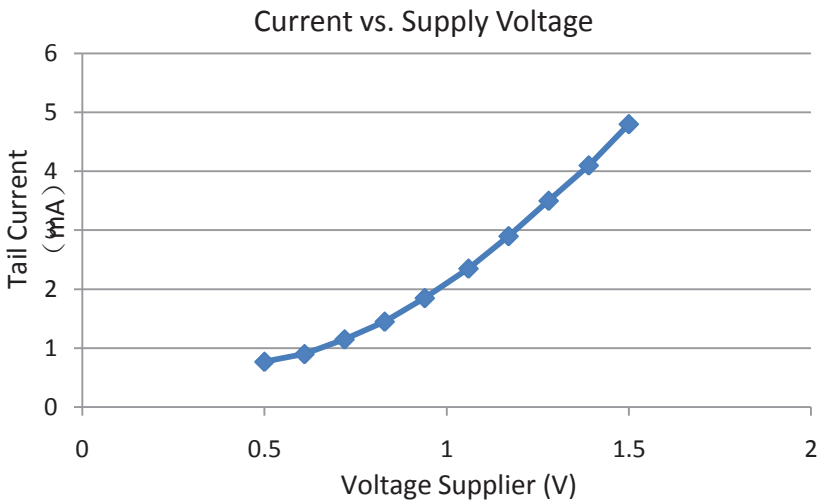


Figure 5-14: The current and power dissipation due to changing in voltage supplier.

S-parameters

Voltage gain (dB) can be measured from a signal's AC analysis or, alternatively, by using an s-parameter. S_{21} represents the forward gain of the 2-port LNA and the plot of the simulated voltage gain for singled-ended for 0.7V power supply voltage is shown in Figure 5-15. The voltage gain of the LNA reaches its peak at required frequency. The peak gain is above 16dB with only 1.2mA bias current. As the voltage varies from 0.7 to 1V, S_{21} curves changes by approximately 3dB. The supply voltage can go down further to reduce power dissipation, but results in a smaller gain. Conversely, a higher

gain also results in more power consumption. This proves the trade-off between sensitivity and power consumption in dynamic operations.

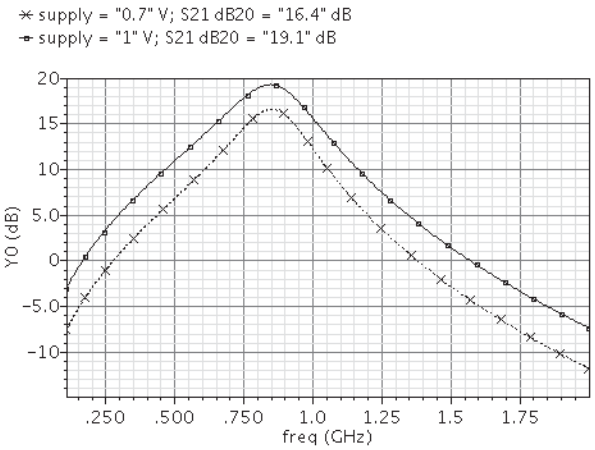


Figure 5-15: Simulated S_{21} results of the single-ended LNA with different supply voltage

In chapter 3, the newly derived equation 3-73 for gain is also simulated in MATLAB and shows a corresponding behaviour to the simulation plot, as shown in Figure 5-16. The consideration of the g_{ds} does have effect on the gain result as compared to ideal simulation result with a reduction of 2dB at tuning frequency.

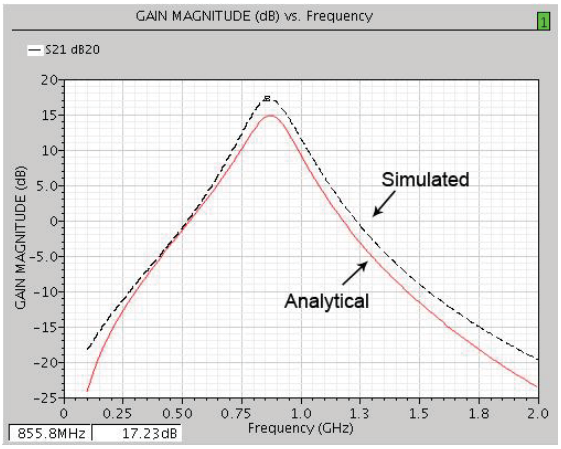


Figure 5-16: gain-magnitude (in dB) comparison between simulated and analytical (equation 3-73) results

The input impedance (Z_{in}) is measured from the plot of S_{11}, which represents the input reflection coefficient. The input impedance of the LNA can be read either from the S-parameter impedance or corresponding Smith Chart shown in Figure 5-17(a) and (b), respectively. The input impedance in the Smith Chart moves along a constant-resistance circle with z value of 0.61. Therefore, as the frequency increases, the capacitive reactance decreases and, as the reactance becomes inductive, the impedance plot moves clockwise along the constant-resistance circuit. Using the formula between Z_{in} and constant line (reference), impedance Z_0, Z_{in} of the LNA can be calculated as z/Z_0. This result shows that the LNA is very closely matched to the source impedance. S_{11} in Figure 5-17 (a) also shows the changing results when different voltage was applied.

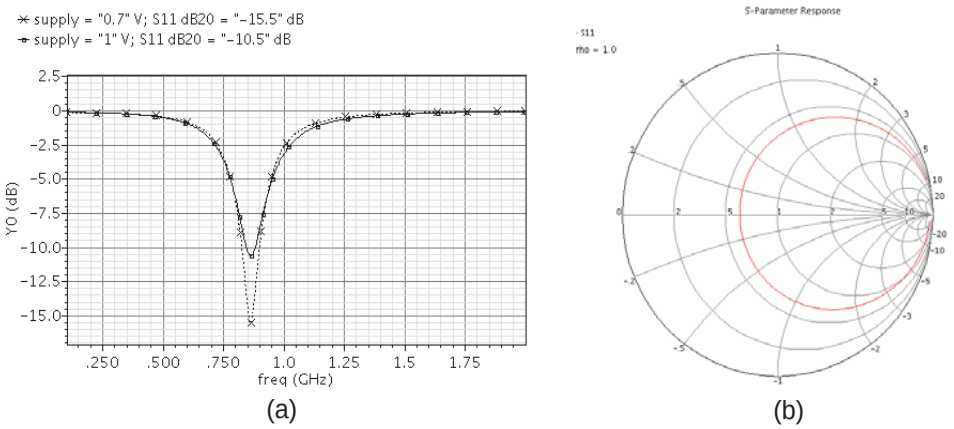


Figure 5-17: (a) simulated S_{11} results of the single-ended LNA with different supply voltage and (b) representing S_{11} in Smith Chart format

In addition, S_{12} and S_{22} have also been simulated, as shown in Figure 5-18(a) and (b), respectively. S_{12} has a simulated value of -36dB at tuning frequency. The measured S_{22} has a value of -27dB with 250Ω output source impedance. If a buffer stage is applied for impedance matching of 50Ω, an approximate 4-6dB loss will occur. Therefore, the balun with certain gain is added with the buffer to remain the unity gain.

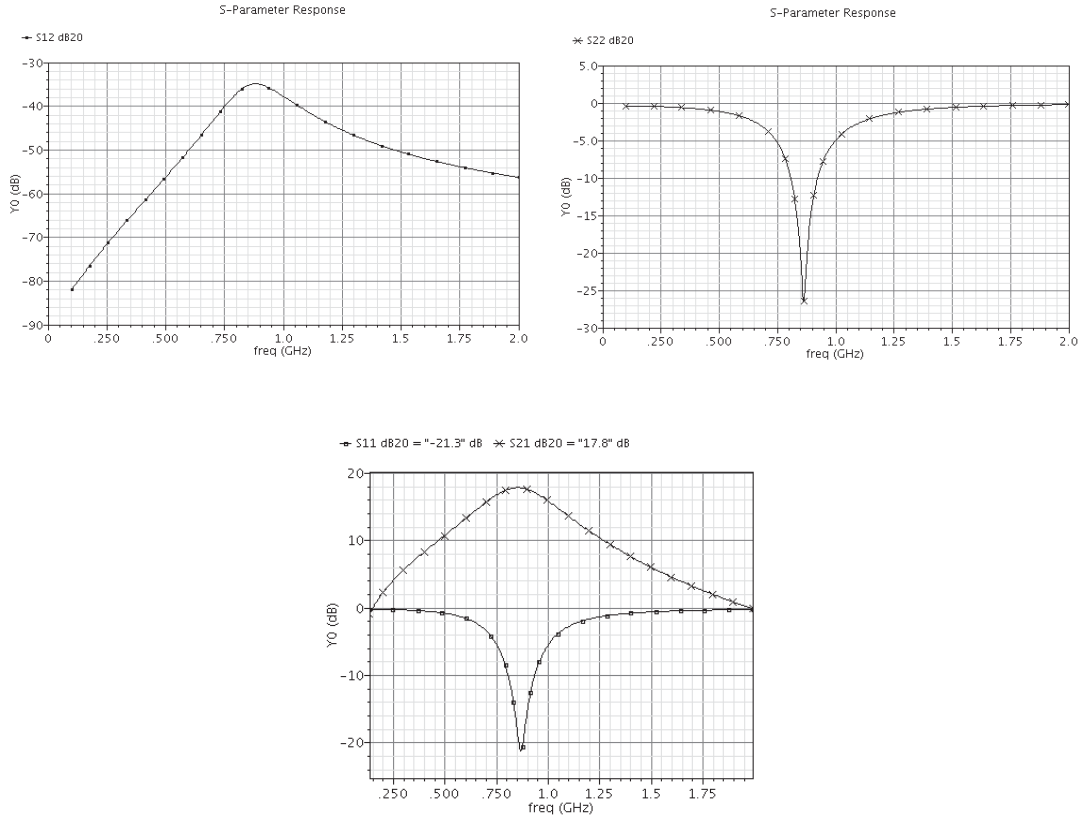


Figure 5-18: simulated S_{21} and S_{22} results of (top) the single-ended LNA and (bottom) differential LNA

Using the previous chapter's appropriate impedance matching technique and TDR calibration of S-parameters, Figure 5-19 demonstrates the measured s-parameter results from Figure 5-13's impedance matching network. With a power supply of 1V and 50Ω port resistor, the measured input reflection coefficient (S_{11}) gives a value around -30dB and the forward power gain (S_{21}) is approximated to be 16dB at tuning frequency. The power dissipation is approximately 1.6mW with 1.6mA drain current through the LNA transistor. Measured S-parameter values lying in line with our expected results prove that the impedance matching method used here is appropriate. With the same power dissipation, the measured S_{21} is off by about 1 dB from simulations at the peak but generally matches well. The measured S_{11} was better due to the improved impedance matching circuit. However, it is slightly off-tuned due to the passive elements at the

inputs. The discrepancies are most likely coming from parasitic components associated with the inaccuracy of the layout modelling and simulations.

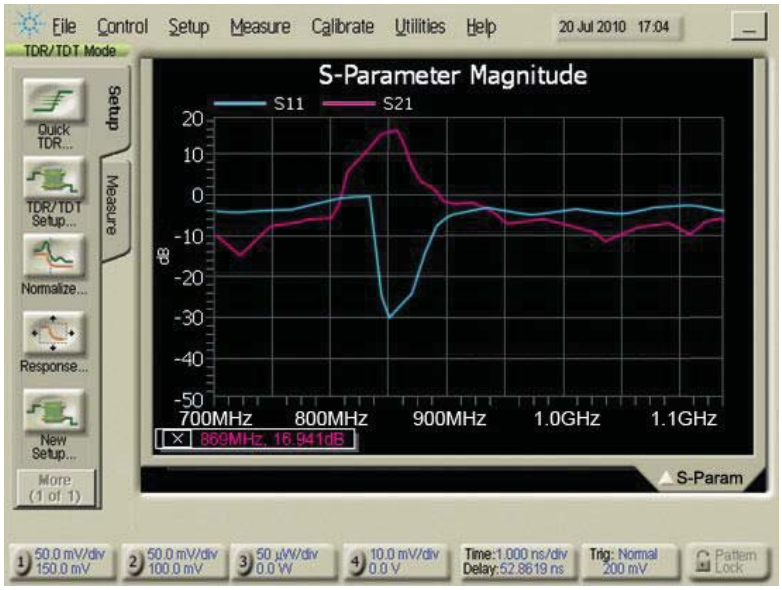


Figure 5-19: Measured S-parameter for Single-ended LNA

Noise Figure

The standard noise figure of the LNA can also be achieved from S-parameter analysis. The noise figure plot in decibel for singled-end LNA is shown in Figure 5-20. Due to the PCSNIM technique, noise figure is minimised at resonant frequency at around 1.1dB. This example demonstrates how to optimise the trade-off between all those specifications in LNA designs. It is also notable that with reduction in power dissipation, the NF of LNAs increases due to the larger value of R_n,.

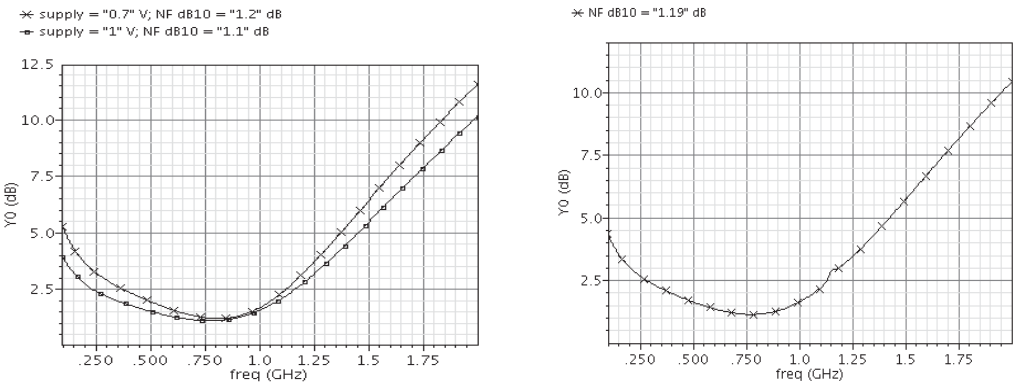


Figure 5-20: Simulated NF results of the singled-ended LNA with different supply voltage (left) and differential LNA with supply voltage of 1V

Furthermore, since the g_{ds} is involved in analytical noise expression and contributes its own thermal noise, the analytical NF plot from MATLAB is approximately 0.3dB above the simulated NF, as shown in Figure 5-21. The noise figure falls down to approximate 1.4dB at the tuning frequency of 866MHz. This simulation result is very close to the redefined noise figure curve plotted by MATLAB. The de-embedded noise measurement result is also shown in Figure 5-21. The minimum measured noise figure is approximately 2dB at around 866 MHz with 1.6mA bias current. The measured noise figure is around 1dB higher than in the simulations due to the external impedance matching and pad parasitic components. Since the induced gate noise is not included in the device model in simulation, it would also cause the discrepancies.

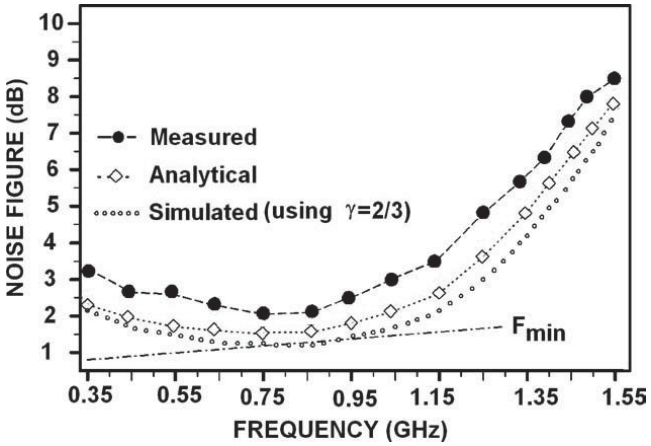


Figure 5-21: Simulated, Analytical and measured result of NF for singled-ended LNA

Linearity

The linearity of the LNA is performed with PSS analysis. The input third-order intercept point (IIP3) and the 1-dB compression point were determined using a two-tone test at 866 MHz with 1 MHz tone separation. The IIP3 can be simulated in this way at the point where the amplitude of the Intermodulation tones at $2\omega_1 - \omega_2$ and $2\omega_2 - \omega_1$ are equal to the amplitude of the fundamental tones at ω_1 and ω_2. The plots in Figure 5-22(a) shows the IIP3 point of the LNA at the tuning frequency. The results indicate an IIP3 of -11.5dBm and a 1-dB compression point of -16.1dBm.

As discussed in the previous chapter, although differential topology consumes double the power, the trade-off is the advantage of improved linearity. Figure 5-22(b) identifies the improvement of 1-dB compression and IIP3 values of -9.1dBm and -9.4dBm compared with a single-ended case. Measured 1-dB compression and IIP3 values are very close to the simulated results.

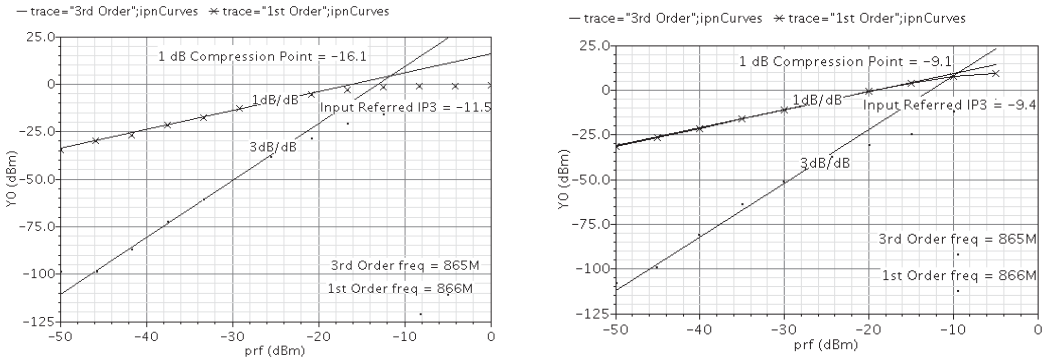


Figure 5-22: Simulated IIP3 and 1dB compression point for (a) single-ended LNA and (b) differential LNA

Result summary and performance comparison

More results and diagrams are also available in the Appendix 8-3 and 8-4. Table 5-1 below shows a summary of performance comparison of the proposed UHF LNA with some other UHF LNA designs indicating low NF achieved at low power dissipation.

The NF can be further reduced by increasing the power dissipation. Since the main target of this thesis is to approach low power mobile solution, power dissipation will be considered as the priority. In general, the proposed LNA has demonstrated several advantages due to the consideration of the g_{ds} during analysis that will bring more realistic results from design.

Table 5-1: Summary of the 866 MHz UHF RFID LNA performance and comparison with previous UHF LNA designs

	Proposed Work		[76]	[74]	[75]	[73]	[57]	[40]
	Sing.	Diff.						
Technology (nm)	130		250	350	180	350	250	180
S_{11} (dB)	-30	-21.3	-11.8	-10	-29	-14	-18	N/A
S_{21} (dB)	17	17.8	7.2	17.5	12.5	17	12	15
S_{12} (dB)	-34	-32	-27.4	N/A	-60	-22	N/A	N/A
S_{22} (dB)	-25	-20	-20	N/A	-33	N/A	N/A	N/A
NF (dB)	2	1.19	4.7	2	0.7	3.4	1.35	2.9
P1dB (dBm)	-11.5	-9.1	-1.8	-6	-4	-5.1	-4	N/A
IIP3 (dBM)	-16.1	-9.4	-9.3	N/A	-9	-23	-15	-15
P_{diss} (mW)	1.6	3	19.5	21.6	3.9	13	2	4.32
Supply Voltage (V)	1		2.5	2.7	1.8	2.3	1.25	1.8
f_0 (MHz)	866		900	900	915	900	900	900

Since there is no paper available with the same operating frequency at 866 MHz, the proposed LNA designs were compared with GSM LNAs operated at 900 MHz in this table. The proposed designs demonstrate the advantages in both gain and power dissipation. With the power consumption of only 1.6 mW, the singled-end LNA shows a noise figure of 2dB and good S-parameters. Although the differential LNA drives more power than singled-ended topology, it provides better noise figure and improved linearity. The performances of these designs once again prove that considering finite g_{ds} effects improves the overall performance of LNA design optimization methodologies.

5.3 Balun

5.3.1 Simulation and Measurement Setup

The differential Balun and its testbench are phase and gain compensated for the simulation shown in Figure 5-23 (a) and (b). The CS differential pair transistors have the same size of 80/0.12μm. The cascode pair transistors, with a slightly smaller size of 50/0.12μm, were chosen for larger r_0 value. The buffer stages convert the impedance to 50 Ω with size of 100/0.12μm.

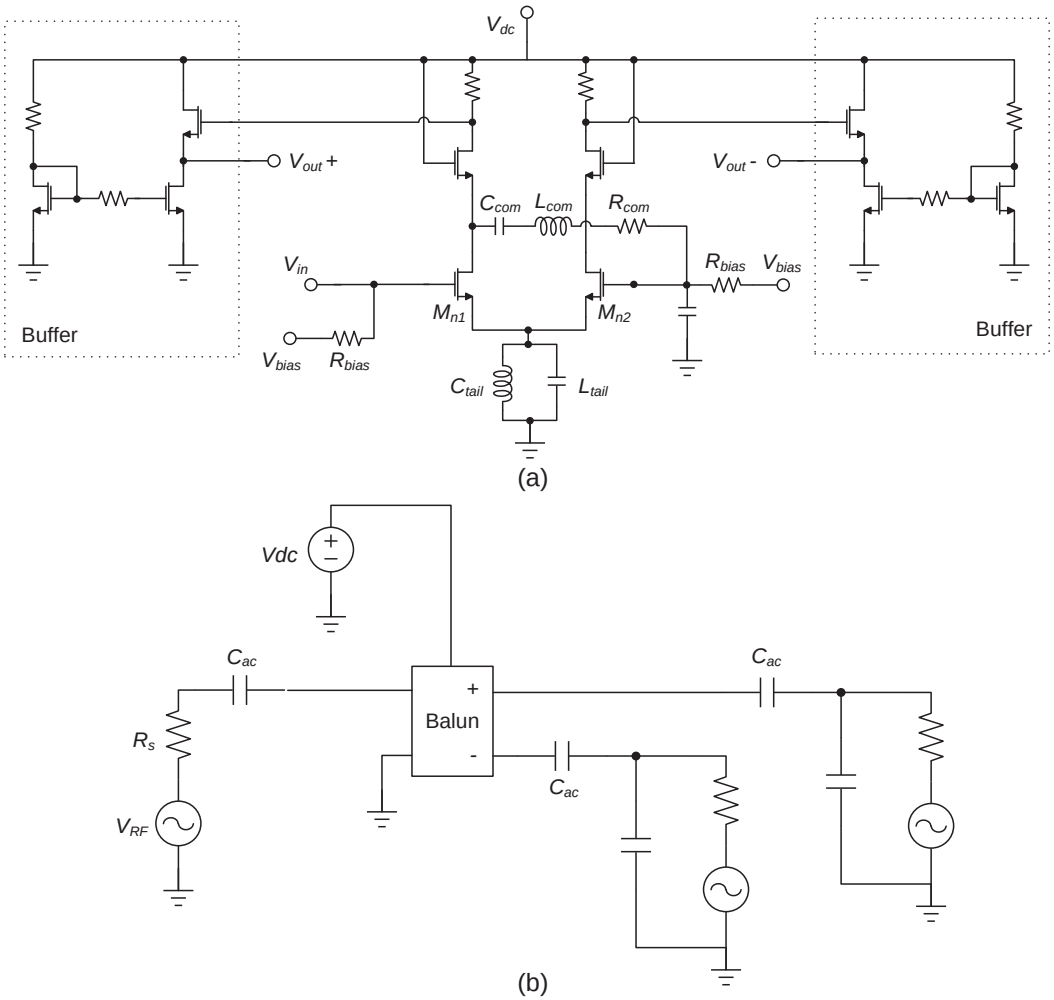


Figure 5-23: (a) Circuit of differential balun with phase and gain compensation, (b) the testbench for the balun.

In order to minimise the power supply voltage and maximum swing, the LC tank is also applied at the tail of the differential pair. The value of the capacitors C_{com}, C_{tail} and inductors L_{com}, L_{tail} for the LC tank at compensation and tail can be calculated as 6.7pF and 4.8nH, respectively.

The layout diagram of this differential balun using the same fabrication process technology is shown in Figure 5-24. It occupies a total area of 0.36mm^2 with pads.

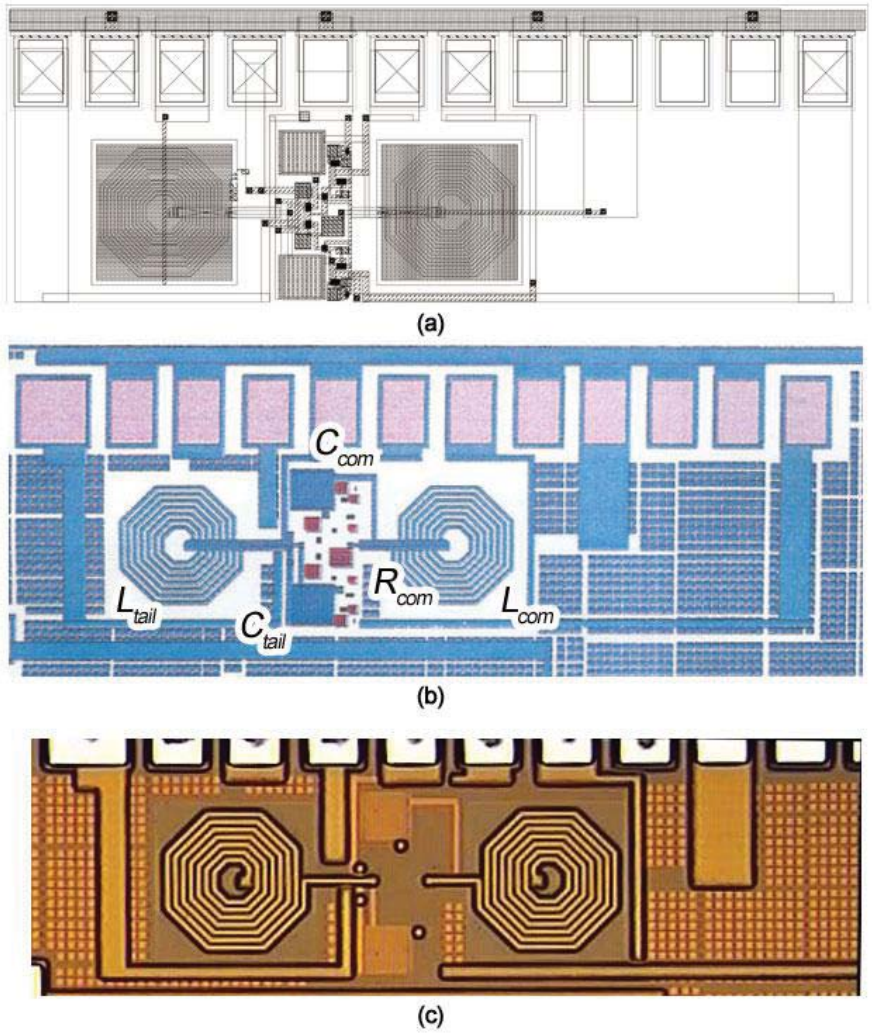


Figure 5-24: Differential balun (a) layout diagram, (b) fabricated die diagram, and (c) its die microphotograph from Figure 5-23

5.3.2 Results

The balun was initially designed to work with single-ended LNA to provide differential outputs. However, since the differential LNA was also designed and performed in this work, the balun was only tested in simulation not measurement. Following results are the simulation result only.

Driving under DC power supply V_{dc} of 1V, the differential balun will consume 1.4mA of current. The output voltage gives 1.7dB gain on each differential port. This means the overall gain is 6.5dB, which is 2.11 times greater than the original single ended input signal. Their input and output transient responses are plotted in Figure 5-25.

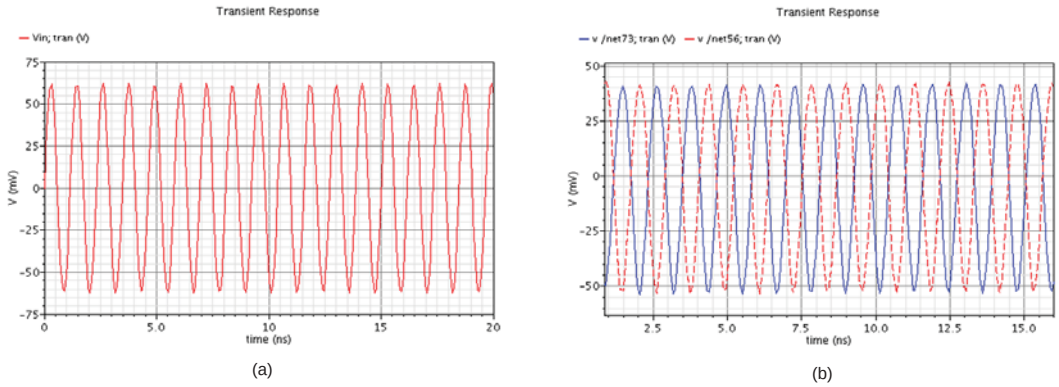


Figure 5-25: Transient Response at (a) input and (b) output of the balun

The simulation result for a balun was more likely to focus on its gain and phase imbalance. Figure 5-26(a) shows the gain and phase imbalance response for a conventional differential balun without the compensation circuit. The gain imbalance between two outputs is around 4-5dB and 1-2 degree in phase imbalance. With the compensation circuitry, the result has less than 0.8 dB in gain imbalance and 0.5 degree in phase imbalance, as shown in Figure 5-26(b)

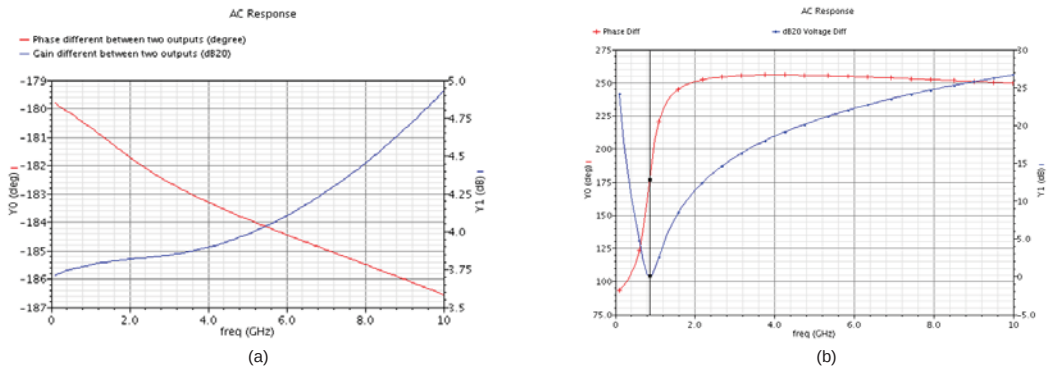


Figure 5-26: Gain and phase imbalance response for (a) conventional differential balun and (b) differential balun with compensation technique.

By varying the capacitance value C_{com} for the compensation tank and tail tank, the frequency can be tuned for a certain range, as shown in Figure 5-27.

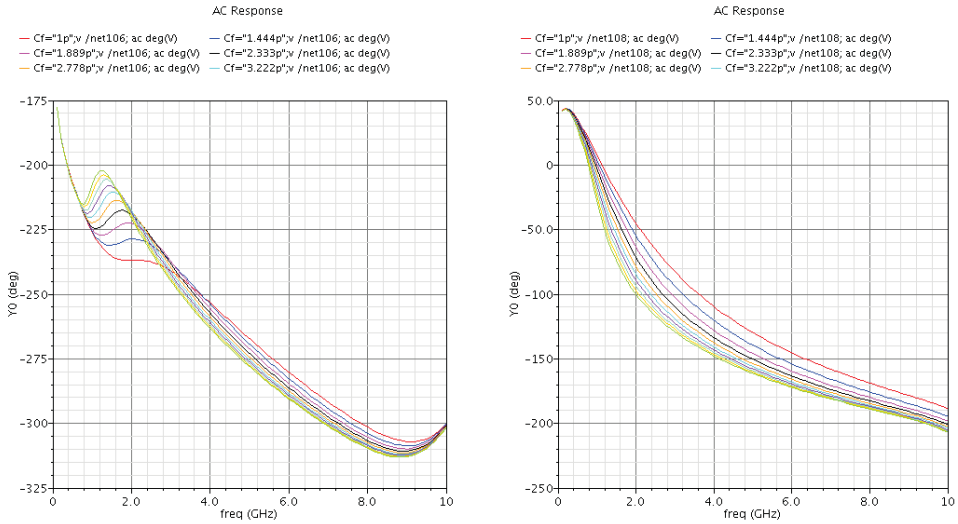


Figure 5-27: Gain and Phase shift in different frequency due to the changing of capacitance of C_{com} for the compensation tank and tail tank

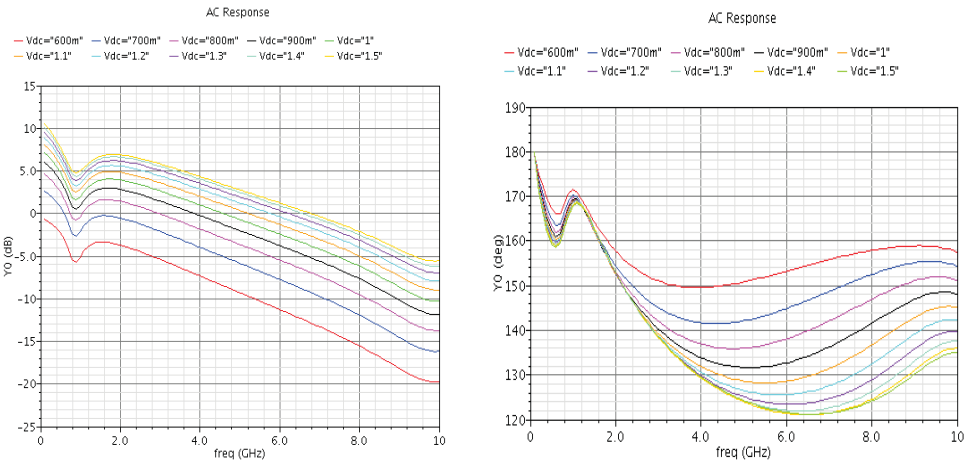


Figure 5-28: Gain and Phase shift in different voltage supplier

Furthermore, with difference of dc power suppliers, the gain and phase imbalance also vary as demonstrated in Figure 5-28. The gain imbalance increases with the increase in supply voltage, while the phase imbalance remains almost the same at tuning frequency.

5.4 Mixer

5.4.1 Simulation and Measurement Setup

For mixer simulation, the testbench in Figure 5-29 is used for the proposed differential Gilbert mixer. The PORT0 provides an RF input signal to the mixer that is matched with the differential mixer input impedance through an off-chip ideal balun. PORT1 provides an ideal LO signal and the LO signal adds up with LO DC overdrive voltage (V_{DC_LO}) of 1.37V and half gain with inverted phase for each branch.

The transistors of the trans-conductor stage have a corresponding size of 220/0.12µm. The NMOS switching pair transistors are smaller at 100/0.12µm. The current bleeding drives more than 70% of the current through the trans-conductor stage with a size of 60/0.35µm.

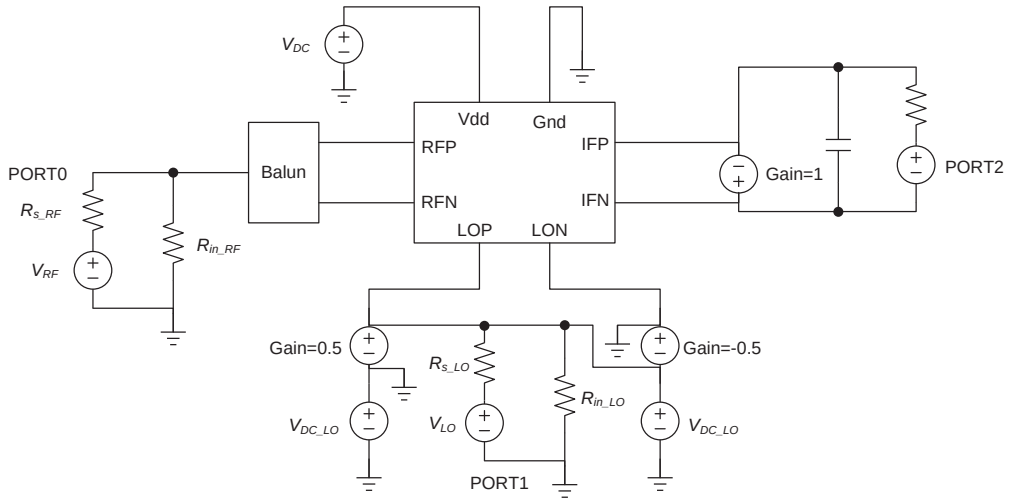


Figure 5-29: Testbench for mixer simulation

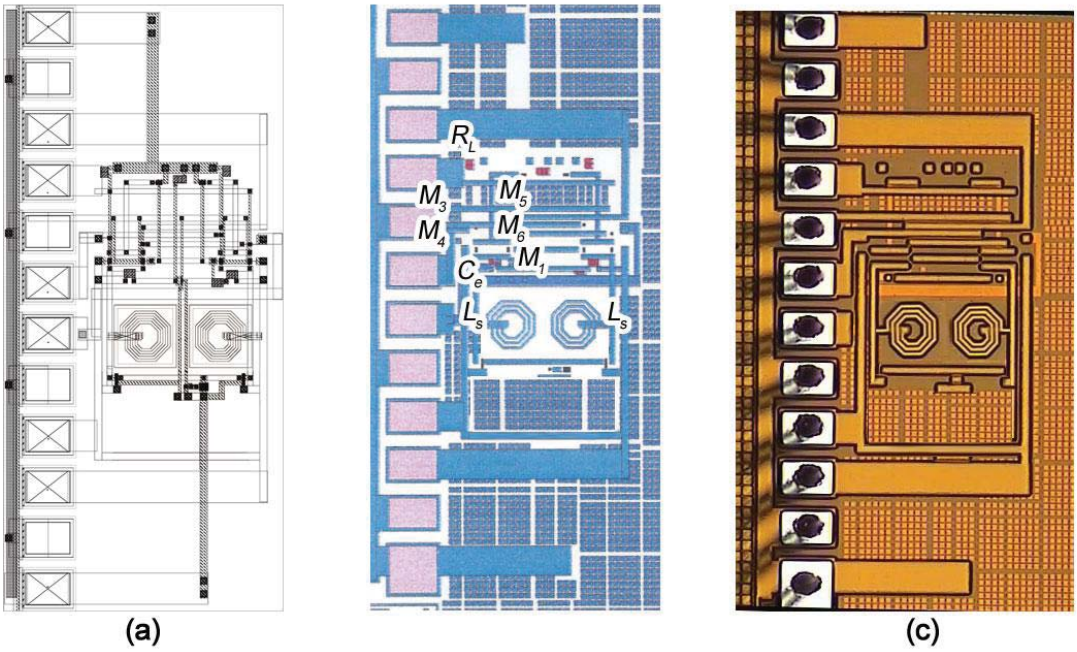


Figure 5-30: Mixer (a) layout diagram, (b) fabricated die diagram, and (c) its die microphotograph from Figure 4-15

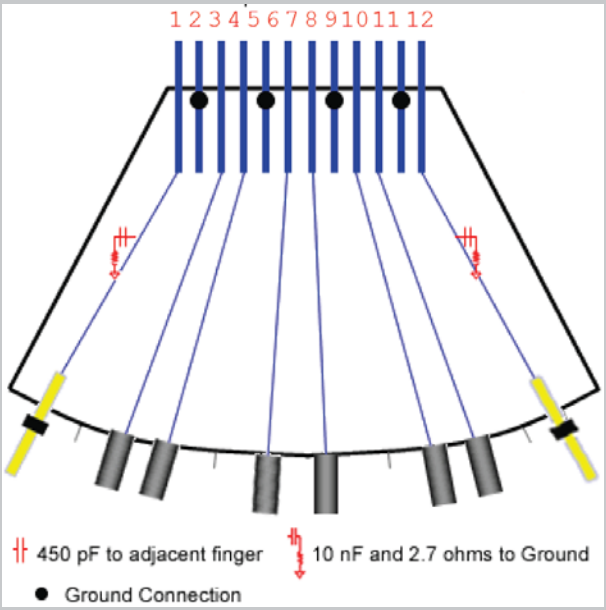
Top View of the UNITY 12-06-100W Probe	Pin	Code	Type
	1	P	DC Power
	2	G	Ground
	3	S	RF signal + (GS)
	4	S	RF signal - (SG)
	5	G	Ground
	6	S	LO signal + (GS)
	7	S	LO signal - (SG)
	8	G	Ground
	9	S	IF signal + (GS)
	10	S	IF signal - (SG)
	11	G	Ground
	12	P	DC power

Figure 5-31: Top view of the unity probe with pin description for mixer measurement

The prototype chip of the proposed differential mixer is also designed and fabricated with the same technology and occupies a total area of 0.54mm^2 ($1050 \times 520\mu\text{m}$). The layout and die microphotograph of the mixer is shown in Figure 5-30. Two off-chip baluns were used to perform the single-ended to differential conversion at the mixer RF input and LO inputs. The LO input power was set to 0dBm for all the measurements. Measurements were carried out by a custom designed 12-pin unity probe, as shown in Figure 5-31. Each differential signal pin is isolated with ground adjacent in the GSSG format. An external buffer is used to provide singled-end IF output from differential signal. Biasing voltage is properly adjusted for best noise performance. The RF input signal was swept and the output IF signal was measured by spectrum analyser.

5.4.2 Results

Conversion Gain

The mixer's frequency conversion performance is represented by conversion gain or loss. The voltage conversion gain is the ratio of the RMS voltage of the IF and RF signals. Sometimes, power conversion gain is used to measure the power delivered to the load and the available RF input power level. Two simulation methods can be employed for calculating the voltage conversion gain by applying a small-signal analysis, such as PSS with PAC or PXF, or two-tone large signal QPSS analysis in Cadence SpectreRF. Figure 5-32 shows the simulated conversion gain plot for the mixer relative to the LO signal power using PSS with PAC. It shows that the maximum voltage conversion gain is reached around 16.8dB with approximately 2dB LO signal power. Using this LO signal power level, Figure 5-33 shows the variation of simulated voltage conversion gain versus RF input frequency. The simulated conversion voltage gain is 15dB with only 2.8mA tail current and 1V supply voltage. The voltage conversion gain also varies with frequency of the RF signal. Figure 5-33 shows the

corresponding measured result to be nearly 14.5dB, which is close to the simulated plot.

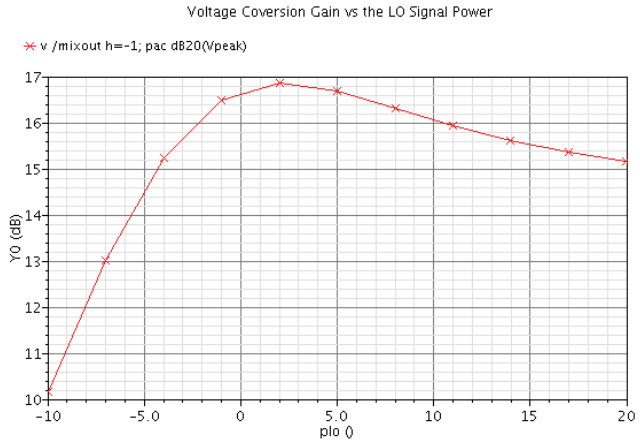


Figure 5-32: voltage conversion gain versus LO signal power (swept PSS with PAC)

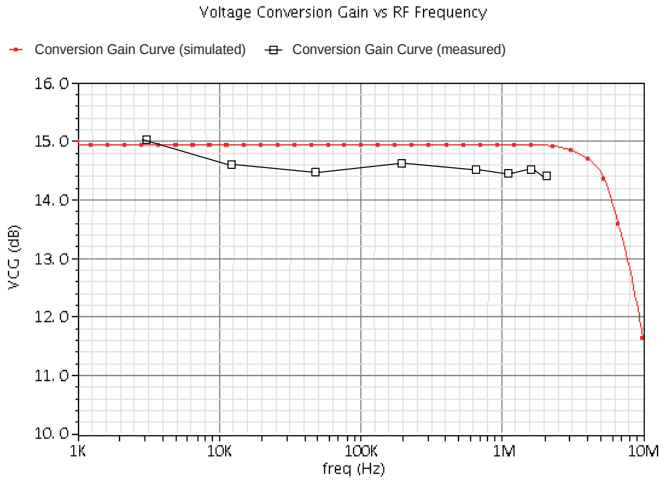


Figure 5-33: Simulated and measured voltage conversion gain versus RF input frequency

In the meantime, power dissipation can be simulated by the large signal QPSS analysis. Figure 5-34 shows the spectrum data of the total power by using QPSS analysis. In additional to that, the power of the main output harmonics is also plotted. Measuring with 1.2V supply voltage, the mixer itself consumes 5mA current with extra 2.2mA for the buffer stages. The internal voltage gain of the mixer is approximately 3dB below the measured gain due to the balun and buffer.

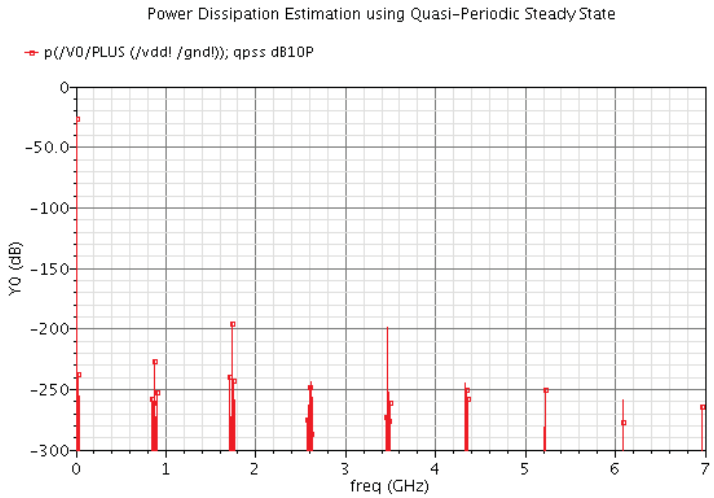


Figure 5-34: Power spectrum at the power source using QPSS analysis

S-parameters

For input impedance matching, the mixer's characteristics behave like the LNA proposed previously with a S_{11} value of -27dB at 866MHz in Figure 5-35. The 2-port S-parameter measurement was processed for the differential RF input ports from the network analyser. Measured S_{11} value in Figure 5-35 shows a result of -19.5dB at a tuning frequency of 920MHz. The tuning frequency is slightly mismatched from 866 MHz due to the mismatching at the input impedance.

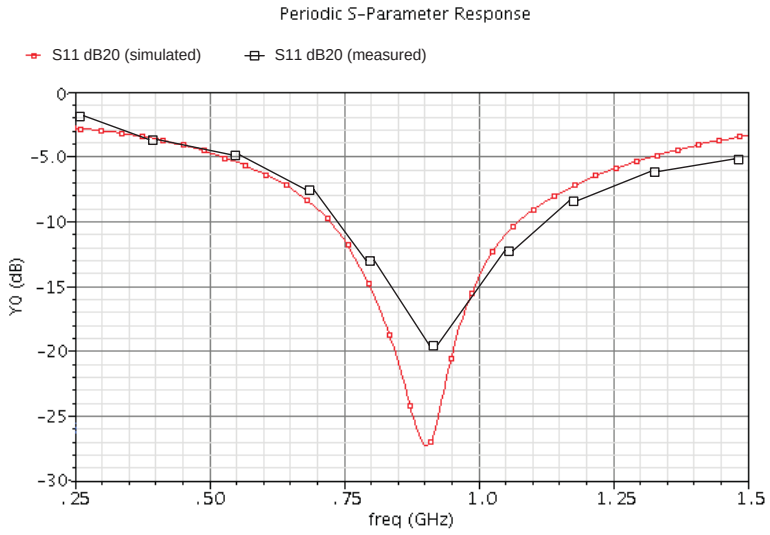


Figure 5-35: Simulated and measured input reflection coefficient S_{11}

Noise

Noise performance of the mixer also affects the sensitivity of the receiver. Figure 5-36 shows the improved simulated results with single-sideband (SSB NF) and double-sideband (DSB NF) noise figure at 866MHz. With the proposed topology, SSB NF has an approximate value of 10.5dB and 7.5dB for DSB NF at the operating frequency.

The NF measurement is only carried out for DSB as SSB NF measurements require an extra filter at the input stage to filter out the noise from the image sideband.

The SSB NF can be approximated predicted by applying an extra 3 dB compensation gain for the measured DSB NF result from the spectrum analyser. Figure 5-36 also shows the DSB NF at 1 MHz baseband frequency and 1/f noise corner at different LO frequencies. The measured NF was approximately 8.7dB and the 1/f noise corner is lower than 45 kHz across the LO frequency range. The noise figure is about 1.2dB higher than the simulated result. Since the internal coupling effect between L_s and L_g was not taken into account during the simulation, it would eventually affect the efficiency of C_{ex}. Furthermore the input matching would also affect the NF. As long as external parasitic resistances are concerned, they cannot be extracted and included in the simulation. The large value of inductance of L_g would also be expressed in large equivalent resistance, which will induce noise. The matching network is therefore not optimised in this case, which explains the shifting of S_{11} measurement. The 1/f noise corner is slightly higher due to the parasitic capacitances at the trans-conductance output.

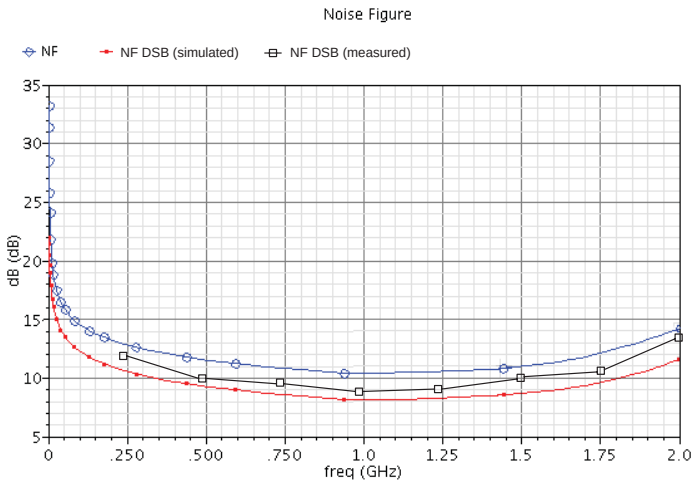


Figure 5-36: Simulated SSB, DSB NF and measured DSB noise performance

Linearity

Figure 5-37 (a) shows the simulated output power versus input power of the mixer. The value of P_{1dB} is given by -13 dBm. The measured P_{1dB} in Figure 5-37 (b) shows a result of -15dBm. The drop in measured P_{1dB} can also be accepted for the same reason as explained previously.

Qpac analysis is applied to plot the third order input referred intercept point. Since the mixer is down-converting to the baseband, the first order harmonic is set at 1.1MHz and the third order harmonic at 0.9MHz. This is defined by the in-band frequency produced by the Intermodulation (IM). The input power levels were swept and the IF and IM3 output power levels were simulated and measured. The simulated results for IIP3 in Figure 5-38 (a) presents a reasonably good result of 0.7dBm. Same two-tone test was also employed for measurement, but only achieved -5.1dBm for IIP3, as shown in Figure 5-38 (b). The disparities between simulated and measured P_{1dB} and IIP3 values are due to the limitation of the output swing and variation with the frequency offset of the blocking signals at later stages. As the buffer is designed initially to have a minimum noise with no gain and low linearity, the degradations of P1dB and IIP3 are

expected. Also the P_{1dB} can be increased by decreasing the trans-conductance of the input stage but with negative impact on the noise figure. Moreover, since the buffer is DC coupled with the mixer, adjusting the biases voltage in the mixer would also affect the buffer performance simultaneously. Even if all the above parameters are taken into account; the measured results indicates the system performs very well at the operating frequency 866 MHz.

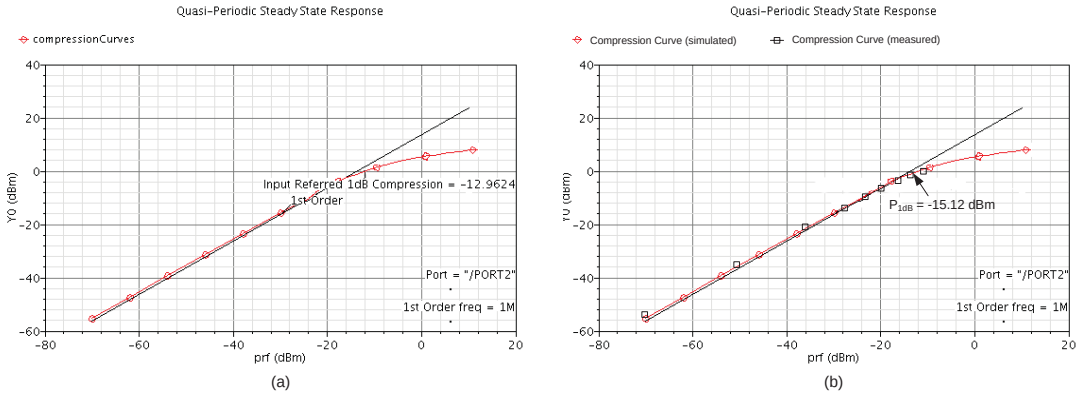


Figure 5-37: (a) Simulated and (b) measured IF output power versus input power and P_{1dB} curves

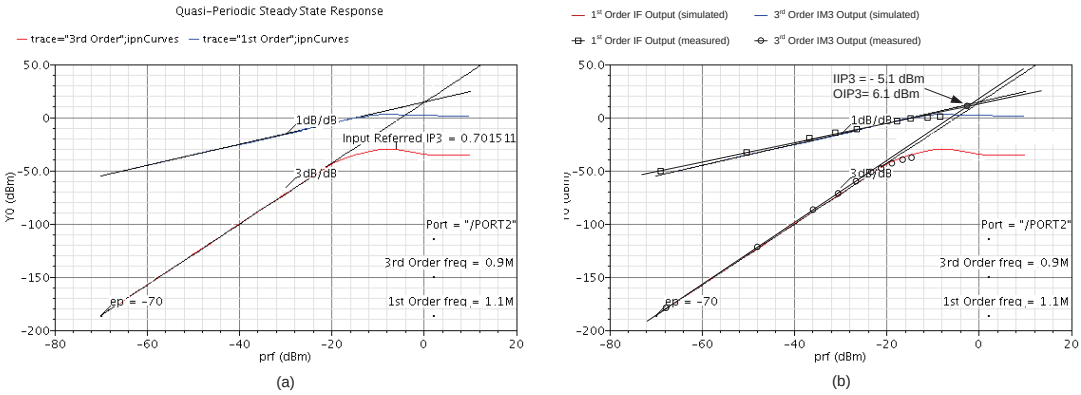


Figure 5-38: (a) simulated and (b) measured IIP3 point

Port-to-port Isolation

The isolation required between a mixer's ports relies heavily on the circuitry, which is critical for the mixer to function properly. RF-to-LO feedthrough affects the local oscillator by letting strong interferers at the input pass to the LO. RF-to-IF feedthrough

might create an even-order distortion problem for homodyne receivers. In order to avoid the impact from the following stages of the mixer, a good LO-to-IF feedthrough is also necessary. Figure 5-39 (a), (b) and (c) shows the simulated RF-to-LO, RF-to-IF and LO-to-IF feedthrough using PAC and PXF analysis, respectively. All simulated port-to-port feedthrough is under -50dB indicating good isolation between two ports. The measured RF-to-IF and LO-to-IF feedthrough in Figure 5-40 can also be achieved by the network analyser as a function of RF input power. The measured RF-to-IF and LO-to-IF feedthrough gave values of -45dB and -43dB that are in accordance with the simulated result. Good port-to-port isolations are achieved on the basis of symmetrical layout structure.

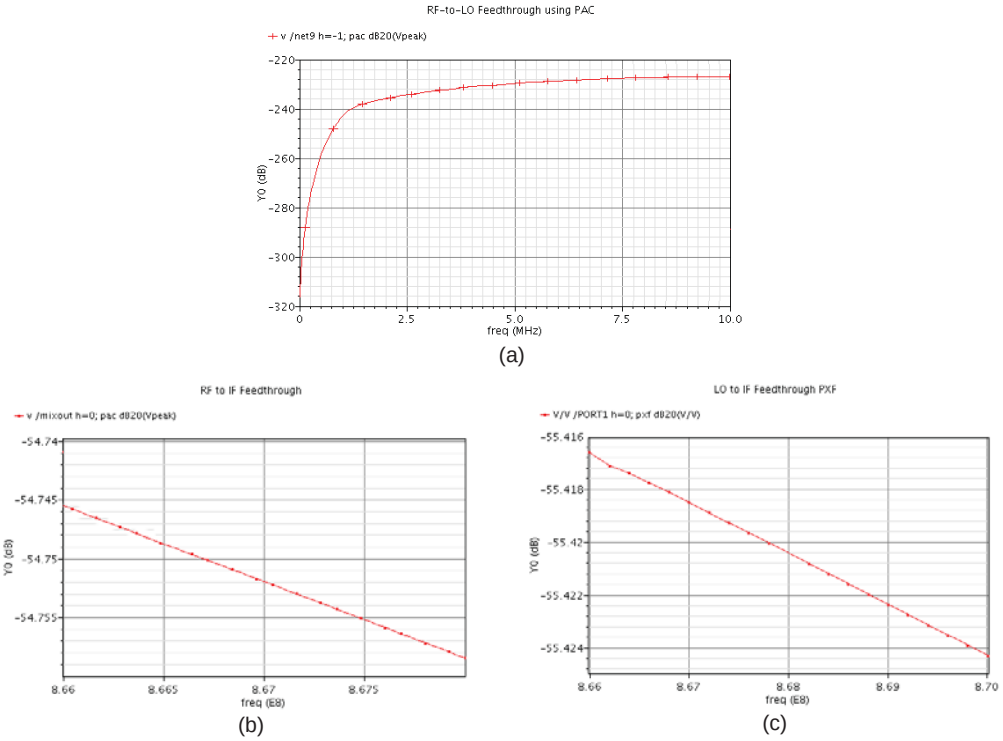


Figure 5-39: Simulated (a) RF-to-LO (b) RF-to-IF and (c) LO-to-IF feedthrough for the mixer

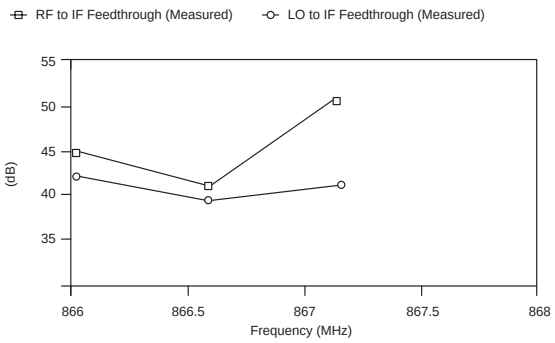


Figure 5-40: Measured RF-to-IF and LO-to-IF feedthrough for the mixer

Result summary and performance comparison

Table 5-2 summarises the proposed mixer's performance, comparing it with recently published mixers. Since some of these publications were only based on simulation[193], the proposed mixer still shows a number of attractive advantages related to both noise performance and power consumption.

Table 5-2: Summary of the proposed mixer performance and comparison with previous mixer designs

	Proposed Work	**[158]**	**[194]**	**[51]**	**[195]**	**[155]**	**[196]**	**[197]**
Technology (nm)	130	130	350	130	90	180	130	0.18
S_{11} (dB)	-19.5	-8.8	N/A	-22	-10	N/A	<-10	N/A
Conversion Gain (dB)	14.5	17.5	23	15	12.1	16	42.5	7
NF (dB)	8.7	3.9	3.2	15	8.4-11.5	9.8	6.5	8.5
P1dB (dBm)	-15	-10.5	N/A	N/A	-13	N/A	-40	N/A
IIP3 (dBM)	-5.1	0.84	-1.5	-3	N/A	-5	-30	2
P_{diss} (mW)	6	34.5	21	12	9.8	7	2	2.1
Supply Voltage (V)	1.2	1.5	N/A	1.5	N/A	N/A	1	2.7
f_0 (GHz)	0.866	1-5.5	2.1	2	0.1-3.85	5.2	1.57	1.96

The table 5-2 indicates most of mixer designs consume large amount of power dissipation in order to bring down the noise figure [158][194], or vice versa [51]. Even paper [196] and [197] consume less power compared to this work, it suffers with either worse linearity or worse conversion gain. A scaled down technology has the advantage of less power consumption, but exchanges with less conversion gain and higher noise figure as demonstrated in paper [195]. In conclusion, the proposed mixer design balances each design performance criteria and design parameters.

5.5 Voltage Control Oscillator

5.5.1 Simulation and Measurement Setup

The same IBM 130 nm technology is also applied to the proposed low-voltage folded-cascode quadrature VCO. As the unity gain frequency of the transistor is beyond 10GHz, oscillation below 1GHz is therefore easy to achieve.

In order to accomplish image rejection for the receiver, the image reject quadrature mixer is required to work with the QVCO. Passive quadrature image reject mixer bridge circuit has the simplest structure and enjoys power free advantage as described in some papers [129, 131]. However, as mentioned in the previous chapter, active mixers are preferred in this work. A quadrature active mixer can be constructed with two symmetric mixers as proposed above[197].

The layout design of this proposed QVCO is critical for its performance. Furthermore, the performance of the QVCO could be degraded due to the parasitic effects inherent from the layout. The QVCO occupies approximately 1mm^2 ($950 \times 1120\mu\text{m}$) chip area, as shown in Figure 5-41. The core positive feedback NMOS latch transistors and the PMOS coupling transistors have corresponding size of 125/0.12μm and 165/0.12μm.

The pull-up PMOS transistors have a size of 95/0.75µm. The on-chip centre-tapped inductor is designed to have a value of 11nH along with the on-chip depletion-mode varactors at operating frequency. Each varactor can be constructed using 10 200× 0.12µm PMOS with an estimated operating range of 0.5-1.4pF by varying the voltage in the range of 0.1-2V. The substrate leakage, bonding pad capacitance and bonding wire inductance will all degrade the performance of the VCO by around 10-15% in terms of the centre frequency and the phase noise behaviour[131]. Furthermore, for the measurement considerations, the VCO buffer is also attached after the VCO core.

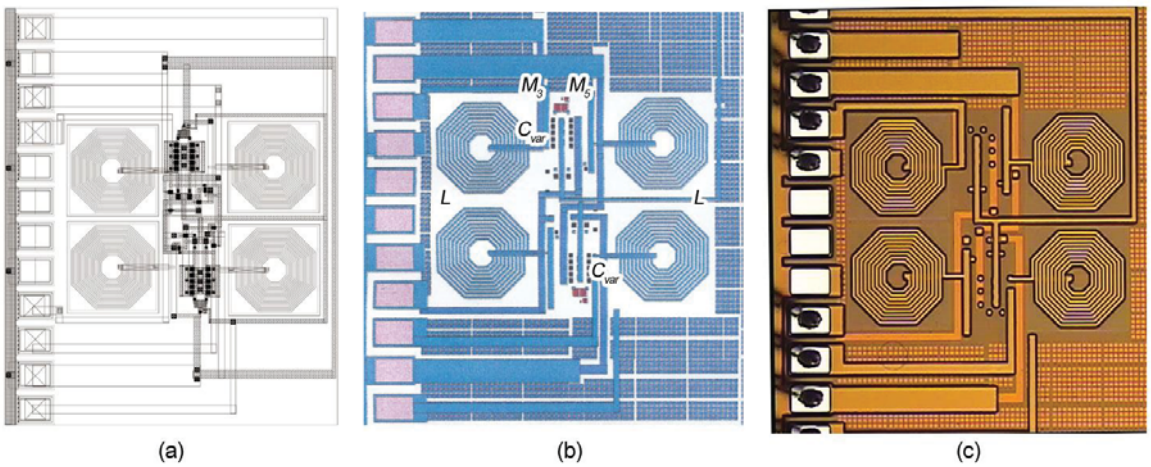


Figure 5-41: The proposed QVCO(a) layout diagram, (b) fabricated die diagram, and (c) its die microphotograph from Figure 4-19

5.5.2 Results

Transient Signal

Figure 5-42 shows the simulated transient start-up of the proposed quadrature VCO output. The signal rises up monotonically from zero to a maximum, after which it stabilises with the power supplies' level. This oscillation model and its frequency ambiguity verify the working of this topology and its accordance with other quadrature VCO designs [173, 198].

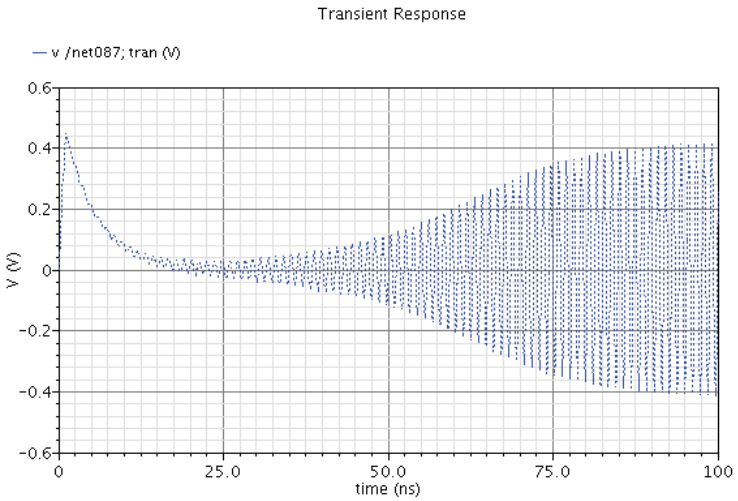


Figure 5-42: Start-up transience signal of the proposed VCO

The output signal amplitude of the VCO is not only limited by supply voltage, bias current and operating frequency, but also by the Q value from the inductor and the equivalent tank resistance. The increase in bias current of the VCO will also raise the amplitude in direct proportion until the voltage reaches the limit of supply voltage. Figure 5-43 shows four sinusoidal transient quadrature responses with different supply voltages. From the simulation, change in the supply voltage provides variable peak-to-peak output signals and corresponding frequencies. With 0.6V, 0.7V, 0.9V and 1.0V supply voltages, the outputs are 0.55V at 877MHz, 0.685V at 862MHz, 0.870V at 855MHz and 0.98V at 847MHz respectively. The grounded tank alternately charges and discharges energy to provide the swing output signal. The swing magnitude is highly dependent on the Q of the inductor. Therefore, due to the poor performance of Q of the on-chip inductor, the output swing is slightly less than the supply voltage. At the same time, because of its symmetric structure and the symmetric inductor, the output waveform is reasonably symmetric. However, as the supply voltage increases, a slight distortion occurs due to the increase in phase noise. Figure 5-44 shows the frequency spectrum of the QVCO output for VDD=0.75V. The oscillation centre frequency is around 866MHz.

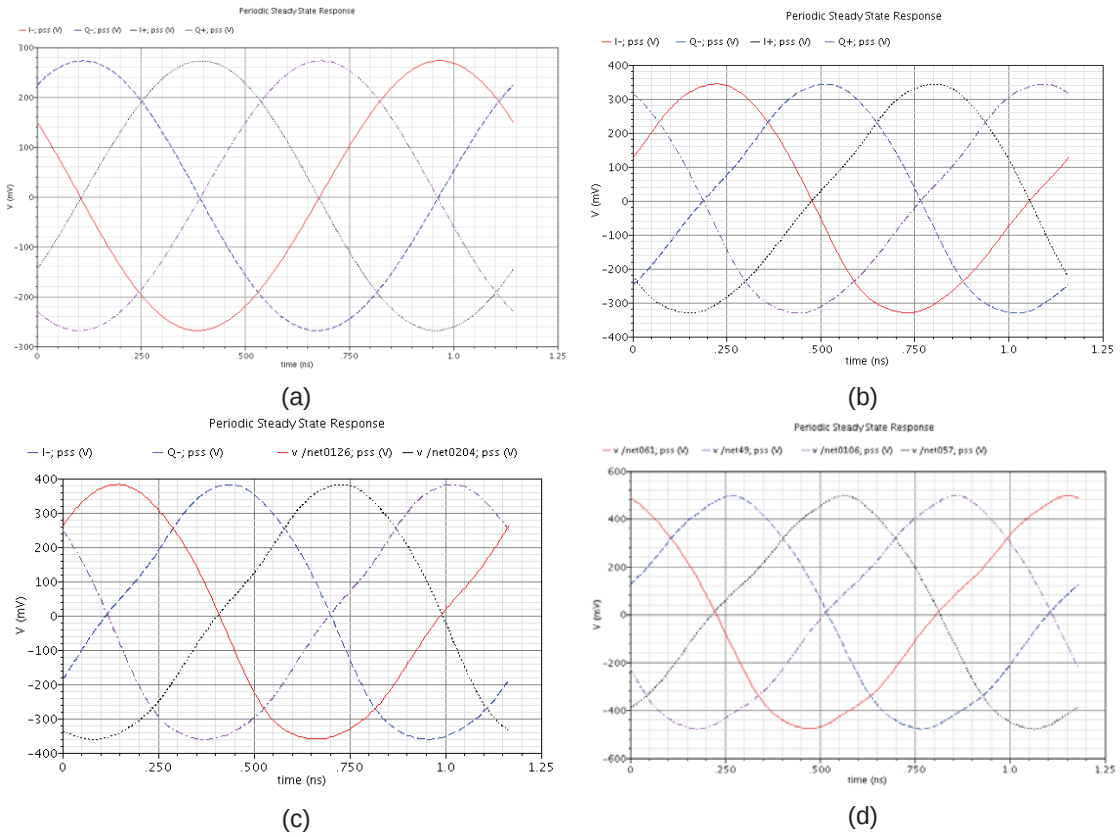


Figure 5-43: Quadrature transient response of the proposed scalable VCO with (a) V_{dd} =0.6V, (b) V_{dd} =0.7V, (c) V_{dd} =0.9V and (d) V_{dd} =1V

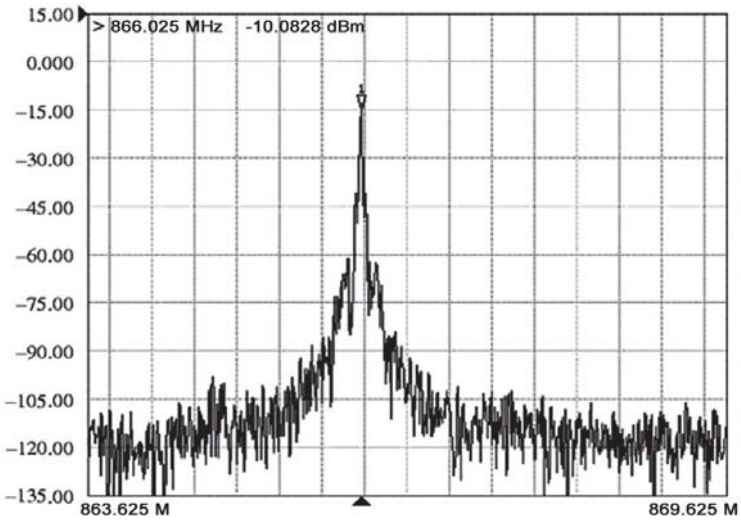


Figure 5-44: Output frequency spectrum of the proposed QVCO at VDD=0.75V.

Bands Tuning Range

The tuning sensitivity (expressed in Hz/V) is the differential derivation of the output frequency versus tuning voltage curve in the VCO. The slope of tuning sensitivity changes as a function of frequency. The above diagram shows the frequency of the VCO changing continuously with the controlled input voltage. By varying the LC tank inductor's value, the VCO can tune a certain range of frequency as demonstrated in Figure 5-45. In practice, changing the inductance of the inductor for measurement is not feasible; therefore, PMOS depletion-mode varactors provide capacitance characteristic for VCO frequency tuning as illustrated in Figure 5.-46. The capacitance behaviour of the series PMOS varactors versus tuning voltage is demonstrated in Figure 5-47. As shown in this diagram, with properly biasing voltage, the capacitance of the varactors can vary from 0.4pf up to 1.45pf with 2V biasing voltage. The measured results as illustrated in the Figure 5-46 match well with the simulation. Since the capacitance of the serial varactors can only go up to 1.45pF, it struggled to approach 866 MHz precisely in frequency. Apart from this issue, an approximate 11.5% of tuning range was achieved, which compares favourably with other QVCO structures published recently [125, 198].

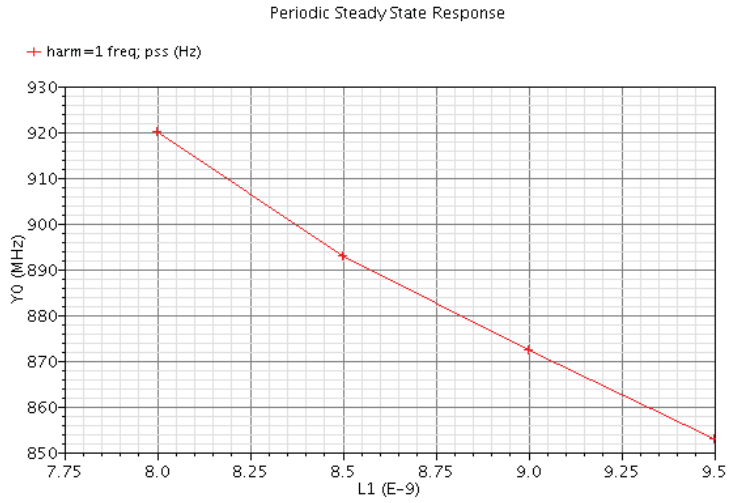


Figure 5-45: Frequency tuning behaviour due to the change of LC tank inductor value

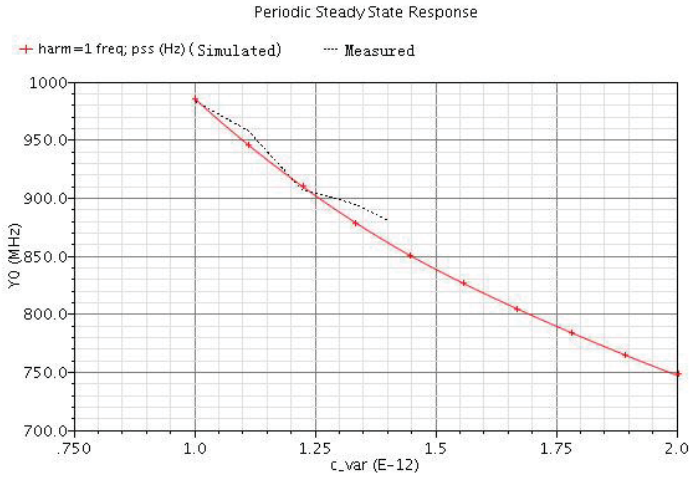


Figure 5-46: Simulated and measured frequency tuning behaviour due to the change of the PMOS varactors

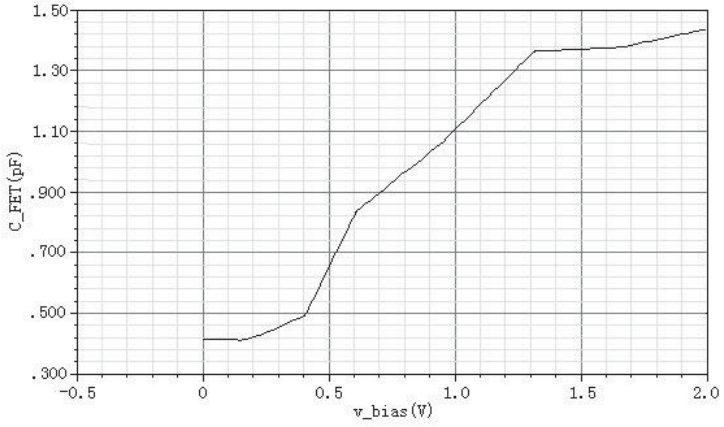


Figure 5-47: The capacitance plot of designed series PMOS depletion-mode varactors

Phase Noise

In the simulation, the on-chip inductor is assumed to have an approximate value of 5-6nH. The output noise voltage spectral density and phase noise are shown in Figure 5-48. With supply voltage of 1V, the diagram indicates a phase noise of about -140dBC/Hz at 3-MHz offset from the carrier. Since this value is only simulated in an ideal environment without considering the effects of other noise sources, the measured phase noise would be much worse. Compared to the recently published low voltage

QVCO designs, the proposed QVCO gave considerably favourable results, especially in the manner of power dissipation.

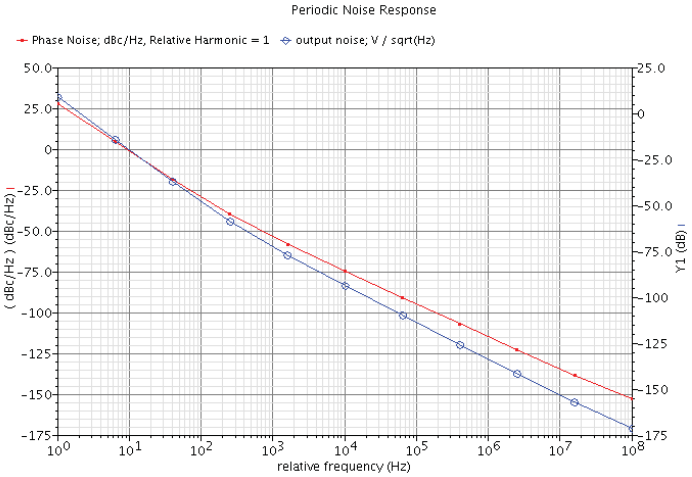


Figure 5-48: Simulated output noise voltage spectral density and phase noise performance.

Power dissipation

The power dissipation in the QVCO includes the following two sources: (a) dynamic power dissipation due to switching current from charging and discharging the tank and (b) short-circuit current when both n-channel and p-channel transistors are momentarily turned on the same time. In addition, there is some static power dissipation due to leakage current and sub threshold current. However, since the most RF designs using CMOS technologies ignore the static power dissipation, only the dynamic power dissipation is calculated through simulation. With 3.4mA tail current for each I- and Q-VCO, the proposed QVCO with folded-cascode topology exhibited very low power dissipation of only 5mW within the supply voltage scaling range. This is a very attractive advantage of low-power RFID applications.

Overall FOM

In the end, the overall figure of merit (FoM) for QVCO performance is used to characterise the trade-off performance relative to other QVCOs of the same type. The

following formulation represents this relationship with power dissipation (P_{diss}), phase noise ($L(\Delta\omega)$), oscillating frequency (ω_0) and offset from carrier ($\Delta\omega$).

$$FoM| = L(\Delta\omega) - 20\,log\left(\frac{\omega_0}{\Delta\omega}\right) + 10log\left(\frac{P_{diss}}{1mW}\right) \quad (5\text{-}3)$$

Therefore, with only 5mW power consumption and -140dBc/Hz at 3-MHz offset from the carrier, this QVCO design has a resulting FoM of around -181dBc/Hz. This result is still acceptable when compared to the recently published designs, especially in UHF range.

Result summary and performance comparison

Table 5-3 below shows a summary of performance comparison of the proposed QVCO with some other QVCO designs.

Table 5-3: Summary of the QVCO performance and comparison with recent designs

	Proposed Work	**[105]**	**[199]**	**[131]**	**[164]**	**[200]**	**[201]**
Technology (nm)	130	1000	180	180	180	130	130
Centre frequency (GHz)	0.866	0.915	7.128	3.5	5.15	5.1	4.5
Tuning range (MHz)	100 (11.5%)	18	4.6%	11.7%	N/A	N/A	N/A
Phase noise (dBc/Hz)	< -140 @ 3 < -130 @ 1 MHz	-118 @ 500 kHz	-111 @ 1 MHz	-150 @ 600 kHz	-124 @ 1 MHz	-118 @ 1MHz	-112@ 1MHz
Power (mW)	5	30	2.2	10	8.7	3.7	4.8
FOM	-181	-169	-183	N/A	-189	-186	-181
Supply Voltage (V)	0.6-1	3	1	1.8-0.75	1.45	1.2	N/A

With only 2.5 mW power consumption and -130 dBc/Hz at 1-MHz offset from the carrier, this QVCO design has a resulting FOM of around -185 dBc/Hz. This

performance is quite acceptable when compared to the recently published designs, especially in the UHF range. The uses of folded cascode topology provide advantages of low phase noise and low quadrature error simultaneously. Also, low phase noise is achieved at very low power dissipation compared to other QVCO designs shown in this table.

CHAPTER 6: CONCLUSIONS

This chapter describes the research outcomes of this thesis and summarizes the work performance so far. Conclusions are drawn from the findings and the key contributions to knowledge are identified from previous chapters. The limitations of the presented design are also discussed, followed by recommendations for future improvements. Moreover, several directions for future research have been highlighted to improve the current system.

6.1 Summary and Contributions of Research

This thesis presents and discusses a design for a fully integrated low power RF receiver front-end for RFID applications. A comprehensive literature review of the present state-of-art for RFID systems is presented in Chapter 2, along with limitations of the RF receiver front-end. An ideal RFID receiver front-end design should possess the following characteristics: simple architecture, low cost and most importantly, low power dissipation. Various front-end blocks incorporating the low-noise amplifier, mixer, voltage-control oscillator and baluns were proposed. Front-end blocks are the first components in a RFID receiver and have a significant impact on the overall system performance.

Conventional active mixers create a great deal of noise, for that reason, the demand for low-noise is mostly fulfilled by the LNAs. Hence, the LNA was initially designed by applying PCSNIM topology with 130nm IBM CMOS technology. The disadvantages of input matching, noise behaviour and power dissipation in conventional SNIM designs

are mitigated by the use of PCSNIM. This impedance matching topology is widely adopted due to its improved noise behaviour performance. However, through the investigation of the noise sources in the MOSFETs, some simulated noise sources have not been in agreement with the analysis. The finite drain-source conductance of the transistor is used for the PCSNIM topology in this thesis, thus achieving more precise analytical models and providing an additional degree of freedom in circuit design. A thorough design analysis was therefore performed and design guidelines were developed at the same time. Numerical simulation revealed the noise behaviour of the developed topology was satisfactory. Comparisons between the improved simulated and measured results demonstrated that this design is more suitable for practical applications. The proposed model generated measured values of 17dB gain and a 2dB noise figure (1.4dB analytical result) for a single-ended LNA operating at 866 MHz with only 1.6mW power consumption.

An integrated on-chip low-noise mixer is also demonstrated utilising PCSNIM topology and current bleeding techniques on the same 130nm CMOS technology. The design is proposed to replace the conventional Gilbert cell mixer that typically exhibits a high noise figure. Since the dominant source of noise is generated from the trans-conductor stage, merging the PCSNIM LNA into this stage overcomes the noise issue. This noise reduction technique combines the LNA and mixer into a single component to reduce the noise figure and chip size, while maintaining satisfactory conversion gain and linearity. The front-end system design can be also simplified through this combination. Additionally, the PCSNIM topology also exhibits favourable power consumption characteristics. Together with the current bleeding technique, the DC current required by the trans-conductors becomes independent of the switching pairs and the load resistors. This allows the mixer to have a higher linearity even with low voltage headroom and low power dissipation. Referring to results of previous design work result performed on the LNA, the proposed mixer also demonstrates the ability to scale with

technology and design requirements. The mixer works at the targeted 866MHz RF/LO signal with a zero IF output and has a power conversion gain of 14.5dB, a low 8.7dB DSB noise figure (11.7dB SSB noise figure) and an IIP3 of -5.1dBM. The mixer core itself consumes only 6mA from a 1.2V supply and the complete test circuit consumes 10mA with baluns for each port. The measured S11 has an upward drift in frequency caused by the coupling between the inductors and parasitic components and also result in a measured noise figure higher than the simulated result.

A low phase noise VCO design is explored next. The quadrature VCO structure is selected to overcome the image rejection issue. As the main target for this work is to design a low power receiver front-end, a folded-cascode topology is employed for the QVCO. The supply voltage is reduced to 1V to minimise power consumption. The proposed QVCO provides satisfactory oscillation with good phase noise performance. The simulated result shows a phase noise of -140dBc/Hz at 3MHz offset from the carrier with only 5mW of power dissipation. This gives a FoM value of -181dBc/Hz, which compares favourably with recently published designs.

To conclude, the research carried out in this thesis has achieved the following outcomes and contributions to knowledge:

- Development and implementation of a completed RF receiver front-end for RFID systems.
- Addition of finite transistor drain-source conductance into the system design, which provides a more precise analytical model and an extra degree of freedom for design considerations.
- Achievement of low power consumption for all active RF components, providing a new approach for ultra-low power RFID receivers' design.
- Evaluation of the implemented methodology and tools.

The methodology employed in this thesis achieved the expected outcome. The conclusions presented offer guidelines both in terms of improvements in system design and performance.

6.2 Opportunities for Further Research

Although the major design goals for a low power RFID receiver front-end were achieved, several challenges were encountered, e.g. system complicity, overall performance, system integration, and precise model analysis. As such opportunities for improvement exist in each of the RFID front-end blocks to enhance overall performance.

Noise characterisation is an important issue for front-end RF designs. From the measured performance of the LNA and mixer, the noise performance still leaves room for improvement. The simulated and measured noise results still face several challenges, such as accurate characterisation of noise sources, modelling of parasitic components and substrate induced channel noise. Tunnelling current induced from MOSFET gate oxide should also be considered for future simulations [168].

Regarding the targeted process technology, modern scaled technologies, such as the 130-nm technology adopted in this thesis exhibit lower power consumption. However, by shrinking device sizes, lower transistor trans-conductance became a challenging design issue when performing NF optimisation. Drain-source conductance analysis was only performed for single-ended LNAs in this work. In future research, drain-source conductance analysis should also be applied to mixer and VCO designs for more precise simulation results.

A further challenge in RF design is the pre-designed inductors provided by the fabrication process foundry. These inductors have several performance limitations. Patterned-ground-shielding is required to compromise system performance (Q increased by 20%). Low Q is a primary factor affecting QVCO performance in a monolithic design. Custom inductor layouts with a particular block design may be necessary to obtain optimal performance. The design of such an inductor could not be developed for this thesis due to time constraint and excessive work load. However, research has been performed in the field of RF Micro-Electro Mechanical Systems (MEMS) to improve inductor performance and particularly towards increasing quality factor Q. A higher value of Q could also improve the receiver's NF performance. MEMS capacitors can also achieve high Q and they are a good option to replace existing CMOS passive components [202-208].

The on-chip inductor in LNA design can be replaced with transistors to create active inductor-less LNA, but with additional power consumption [209, 210]. This trade-off always exists, so we chose to reduce power by using a passive inductor and in any-case, the chip size is small enough with the 130nm technology.

As further device scaling leads to a reduction in supply voltage, a new challenge for the proposed circuit topologies is overcoming the limitation of low voltage headroom. Although the folded-cascode topology enjoys the advantage of low voltage operation, its voltage output headroom and phase performance are both affected.

At the same time, a thorough investigation should be performed into VCO designs to define theoretical and practical limitations. Monte Carlo analysis should be also carried out to characterise QVCO performance over process and component tolerance variations [131]. Furthermore, PLL should also be designed in future work to create a complete VCO block.

The balun implemented in this work is only suitable for narrow band applications. A broadband balun, or broadband transformer, would be more widely applicable. However, broadband design requires more modelling constraints and consideration of skin effect and materials.

In general, the optimisation of trade-offs between power consumption, system architecture simplification, sensitivity, linearity and parasitic component behaviour is a significant design challenge and is worthy of ongoing research. From a system point of view, a top-down design combining the RF front-end and digital back-end circuits will enable the creation of complete RF SoC designs in the future.

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APPENDICES

8.1 SPICE BSIM3 Parameters

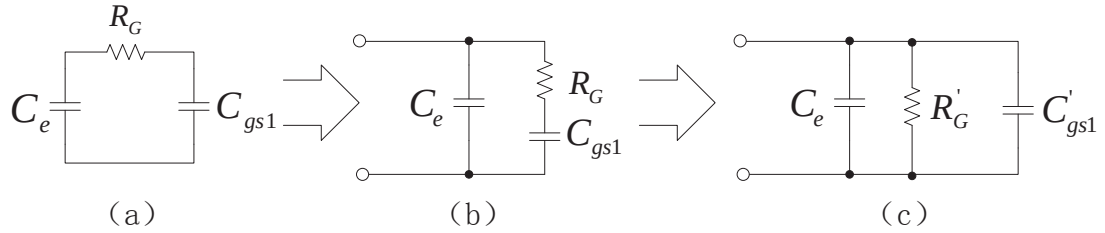
SPICE 3f5 Level 8, Star-HSPICE Level 49, UTMOST Level 8

```
* DATE: Sep 24/07
* LOT: T75T                WAF: 3001
* Temperature_parameters=Default
.MODEL CMOSN NMOS (                       LEVEL   = 49
+VERSION = 3.1          TNOM    = 27          TOX     = 3.1E-9
+XJ      = 1E-7         NCH     = 2.3549E17   VTH0    = 0.0541243
+K1      = 0.3515227    K2      = -0.0280822  K3      = 1E-3
+K3B     = 4.070674     W0      = 1E-7        NLX     = 1E-6
+DVT0W   = 0            DVT1W   = 0           DVT2W   = 0
+DVT0    = 1.318384     DVT1    = 0.1414428   DVT2    = 0.2322006
+U0      = 439.5521957  UA      = -4.54345E-10  UB    = 3.634408E-18
+UC      = 4.691069E-10  VSAT   = 1.90977E5   A0      = 1.7414863
+AGS     = 0.7665367    B0      = 2.757907E-6  B1     = 5E-6
+KETA    = 9.870802E-3  A1      = 8.081318E-4  A2     = 0.3
+RDSW    = 150          PRWG    = 0.3536078   PRWB    = 0.1084003
+WR      = 1            WINT    = 7.739778E-9  LINT    = 1.035925E-8
+DWG     = 3.829886E-9  DWB     = 1.21414E-8   VOFF    = -0.0375898
+NFACTOR = 2.5          CIT     = 0           CDSC    = 2.4E-4
+CDSCD   = 0            CDSCB   = 0           ETA0    = 2.767166E-6
+ETAB    = 0.4629603    DSUB    = 4.084204E-6  PCLM    = 0.9746787
+PDIBLC1 = 0.994348     PDIBLC2 = 0.01        PDIBLCB = 0.1
+DROUT   = 0.9980277    PSCBE1  = 7.955079E10  PSCBE2  = 5.002622E-10
+PVAG    = 0.5010963    DELTA   = 0.01        RSH     = 7
+MOBMOD  = 1            PRT     = 0           UTE     = -1.5
+KT1     = -0.11        KT1L    = 0           KT2     = 0.022
+UA1     = 4.31E-9      UB1     = -7.61E-18   UC1     = -5.6E-11
+AT      = 3.3E4        WL      = 0           WLN     = 1
+WW      = 0            WWN     = 1           WWL     = 0
+LL      = 0            LLN     = 1           LW      = 0
+LWN     = 1            LWL     = 0           CAPMOD  = 2
+XPART   = 0.5          CGDO    = 3E-10       CGSO    = 3E-10
+CGBO    = 1E-12        CJ      = 8.383543E-4  PB     = 0.8911869
+MJ      = 0.5522633    CJSW    = 2.463297E-10  PBSW   = 0.8
+MJSW    = 0.3086109    CJSWG   = 3.3E-10     PBSWG   = 0.8
```

```
+MJSWG   = 0.3086109     CF      = 0           PVTH0   = 2.009264E-4
+PRDSW   = 0           PK2     = 1.30501E-3    WKETA   = -2.594684E-3
+LKETA   = 0.0144671     PU0     = 4.4729531     PUA     = 1.66833E-11
+PUB     = 0           PVSAT   = 653.2294237   PETA0   = 1E-4
+PKETA   = -0.0237138     )
*
.MODEL CMOSP PMOS (                          LEVEL   = 49
+VERSION = 3.1          TNOM    = 27          TOX     = 3.1E-9
+XJ      = 1E-7         NCH     = 4.1589E17     VTH0    = -0.2256378
+K1      = 0.2479965     K2      = 0.0100335     K3      = 0.0990496
+K3B     = 6.4928146     W0      = 1E-6          NLX     = 2.817855E-7
+DVT0W   = 0           DVT1W   = 0           DVT2W   = 0
+DVT0    = 0           DVT1    = 0           DVT2    = 0.1
+U0      = 113.5081851   UA      = 1.448104E-9   UB      = 2.832586E-21
+UC      = 7.196711E-12  VSAT    = 2E5           A0      = 1.4059833
+AGS     = 0.8501722     B0      = 1E-5          B1      = 2.303043E-6
+KETA    = 0.0398539     A1      = 2.277496E-4   A2      = 0.658498
+RDSW    = 108.0955922   PRWG    = -0.4769563    PRWB    = 0.5
+WR      = 1           WINT    = 0           LINT    = 7.575551E-9
+DWG     = 7.697623E-10  DWB     = -2.171108E-8  VOFF    = -0.1022829
+NFACTOR = 1.5332272     CIT     = 0           CDSC    = 2.4E-4
+CDSCD   = 0           CDSCB   = 0           ETA0    = 1.329187E-3
+ETAB    = -6.663089E-3  DSUB    = 1.922357E-3   PCLM    = 2.0326797
+PDIBLC1 = 0           PDIBLC2 = -9.22392E-10  PDIBLCB = 0.1
+DROUT   = 1           PSCBE1  = 3.786151E9    PSCBE2  = 1.156909E-9
+PVAG    = 0.5845723     DELTA   = 0.01          RSH     = 7
+MOBMOD  = 1           PRT     = 0           UTE     = -1.5
+KT1     = -0.11         KT1L    = 0           KT2     = 0.022
+UA1     = 4.31E-9       UB1     = -7.61E-18     UC1     = -5.6E-11
+AT      = 3.3E4         WL      = 0           WLN     = 1
+WW      = 0           WWN     = 1           WWL     = 0
+LL      = 0           LLN     = 1           LW      = 0
+LWN     = 1           LWL     = 0           CAPMOD  = 2
+XPART   = 0.5         CGDO    = 3E-10         CGSO    = 3E-10
+CGBO    = 1E-12         CJ      = 1.174314E-3   PB      = 0.8213848
+MJ      = 0.4093691     CJSW    = 1.315954E-10  PBSW    = 0.893802
+MJSW    = 0.1         CJSWG   = 4.22E-10      PBSWG   = 0.893802
+MJSWG   = 0.1         CF      = 0           PVTH0   = 5.912762E-4
+PRDSW   = 40.5641941    PK2     = 2.503394E-3   WKETA   = 0.0351557
+LKETA   = 0.0167725     PU0     = -1.4369524    PUA     = -5.08742E-11
+PUB     = 0           PVSAT   = 50          PETA0   = 1E-4
+PKETA   = -0.0107023     )
*
```

8.2 Capacitive transformation steps of finding R_G due to the addition of C_e across M1:

(1) RC Series to Parallel transformation



$$R_G^{'} = \frac{R_G^{\,2} + X_{gs1}^{\,2}}{R_G} = \frac{R_G^{\,2}}{R_G}\left(1 + \frac{X_{gs1}^{\,2}}{R_G^{\,2}}\right) = R_G\left[1 + \left(\frac{1}{\omega_o C_{gs1} R_G}\right)^2\right] = R_G\left[1 + Q^2\right]$$

$$C_{gs1}^{'} = \frac{C_{gs1}}{R_G^{\,2}\omega_o^{\,2} C_{gs1}^{\,2}} \cdot \frac{1}{1 + \left(\frac{1}{\omega_o C_{gs1} R_G}\right)^2} = C_{gs1} \cdot \frac{Q^2}{1+Q^2}$$

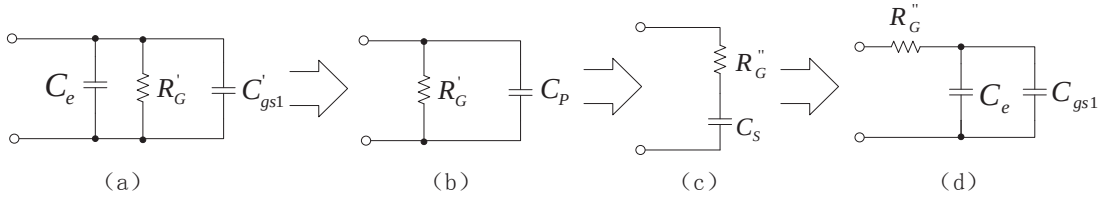
Due to the small value of C_{gs1} and R_G, which leads $Q = \frac{1}{\omega_o C_{gs1} R_G} >> 1$, $R_G^{'}$ and $C_{gs1}^{'}$ can be represented now as:

$$R_G^{'} \approx R_G Q^2$$

and

$$C_{gs1}^{'} \approx C_{gs1}$$

(2) RC Parallel to Series transformation



$$R_G^{''} = \frac{\frac{1}{R_G^{'}}}{\frac{1}{R_G^{'\,2}} + \frac{1}{X_P^2}} = R_G^{'} \frac{1}{1 + \frac{R_G^{'\,2}}{X_P^2}} = R_G^{'} \frac{1}{1 + \omega_o^2 C_P^2 R_G^{'\,2}} = R_G^{'} \frac{1}{1 + Q^{'2}}$$

$$C_S = C_P \cdot \frac{1 + Q^{'2}}{Q^{'2}} = \left(C_{gs1} + C_e\right) \cdot \frac{1 + Q^{'2}}{Q^{'2}}$$

The new $Q^{'}$ can be re-calculated again as following:

$$Q^{'} = \omega_0 C_P R_G^{'} = \omega_0 \left(C_{gs1} + C_e\right) R_G Q^2 = \omega_0 \left(C_{gs1} + C_e\right) R_G \left(\frac{1}{\omega_o C_{gs1} R_G}\right)^2 = \frac{1}{\omega_o R_G} \cdot \frac{C_{gs1} + C_e}{C_{gs1}^2}$$

and we can see the new $Q^{'} >> 1$, therefore, the $R_G^{''}$ and C_S can be represented now as:

$$R_G^{''} \approx \frac{R_G^{'}}{Q^{'2}} = \frac{R_G \left(\frac{1}{\omega_o C_{gs1} R_G}\right)^2}{\left(\frac{1}{\omega_o R_G} \cdot \frac{C_{gs1} + C_e}{C_{gs1}^2}\right)^2} = R_G \frac{C_{gs1}^2}{\left(C_{gs1} + C_e\right)^2}$$

and

$$C_S \approx \left(C_{gs1} + C_e\right)$$

From the expression of C_S, the capacitor C_{gs1} parallel with C_e can be formed again, as shown in Figure 2 (d). The fundamental RC Series / Parallel transformation steps can be reviewed from following two transformations.

8.3 Published Journal Paper I: A 12 dB 0.7V 850 μW CMOS LNA for 866MHz UHF RFID Reader[211]

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Research Article

A 12 dB 0.7 V 850 μW CMOS LNA for 866 MHz UHF RFID Reader

Jie Li and S. M. Rezaul Hasan

Center for Research in Analog & VLSI Microsystem Design (CRAVE), School of Engineering and Advanced Technology (SEAT), Massey University, Albany, Auckland 0632, New Zealand

Correspondence should be addressed to S. M. Rezaul Hasan, hasanmic@massey.ac.nz

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The design of a narrow-band cascode CMOS inductive source-degenerated low noise amplifier (LNA) for 866 MHz UHF RFID reader is presented. Compared to other previously reported narrow-band LNA designs, in this paper the finite g_{ds} $(= 1/r_0)$ effect has been considered to improve the nanometric design, achieving simultaneous impedance and minimum F_{min} noise matching at a very low power drain of 850 μW from a 0.7 V supply voltage. The LNA was fabricated using the IBM 130 nm CMOS process delivering a forward power gain (S_{21}) of $\approx$ 12 dB, a reverse isolation (S_{12}) of ≈ -34 dB, an output power reflection (S_{22} @866 MHz) of ≈ -25 dB, and an input power reflection (S_{11} @866 MHz) of ≈ -12 dB. It had a minimum pass-band NF of around 2.2 dB and a third-order input referred intercept point (IIP3) of ≈ -11.5 dBm.

1. Introduction

RFID (radio-frequency identification) is one of the fastest growing wireless communication technologies for commercial product tracking. As the low noise amplifier (LNA) is the first block in the front-end of the RFID reader which is tuned at a certain transreceiver frequency, it needs to be designed optimally to minimize the noise for the following stages and avoid the distortion of the source signal (requires good linearity). To overcome design trade-off difficulties between gain, power, noise figure (NF) and matching in the optimization of the LNA, the design of the matching circuits at the input and the output are based, respectively, on minimal NF and maximal power transfer. In recent years, considerable research on CMOS LNA design in submicron technologies at 900 MHz have been reported by many authors in [1–4]. A lower frequency standard for UHF RFID at 866 MHz is also implemented in Europe, Africa, and New Zealand. Low power dissipation at low supply voltage is a significant design criterion for RFID applications synthesized by design trade-off between gain, NF, input and output impedance matching and high linearity. In this paper we discuss the design and the experimental results for a 0.7 V low-power 130 nm CMOS 866 MHz single-ended common-source telescopic cascode LNA using an *enhanced* power constrained simultaneous noise and impedance matching (PCSNIM [5, 6]) technique.

2. Principles and Circuit Design

An inductively source degenerated telescopic cascode topology has been chosen for the 866 MHz RFID LNA design due to its current reuse structure and hence it consumes less bias current than the folded cascode. Figure 1 shows the circuit diagram of the proposed RFID LNA. M_1 and M_2 forms the cascode configuration and their bias currents are driven by M_3 and R_{ref}. L_d, R_d, and C_d form the output tank circuit tuned at 866 MHz with an angular frequency bandwidth of $1/(R_d * C_d)$. C_{ac} denotes ac-coupling capacitor (one at the source input and the other at the output load) while C_b is an ac grounding capacitor at the gate of the cascoding device M_2. L_s provides the inductive source degeneration. An *improved* PCSNIM technique is adopted here for the telescopic cascode LNA structure optimization. C_e is in parallel with C_{gs1} of M_1 in order to achieve minimum noise figure F_{min} with power constraint and higher unity gain frequency ω_T. Optimal impedance Z_{opt}

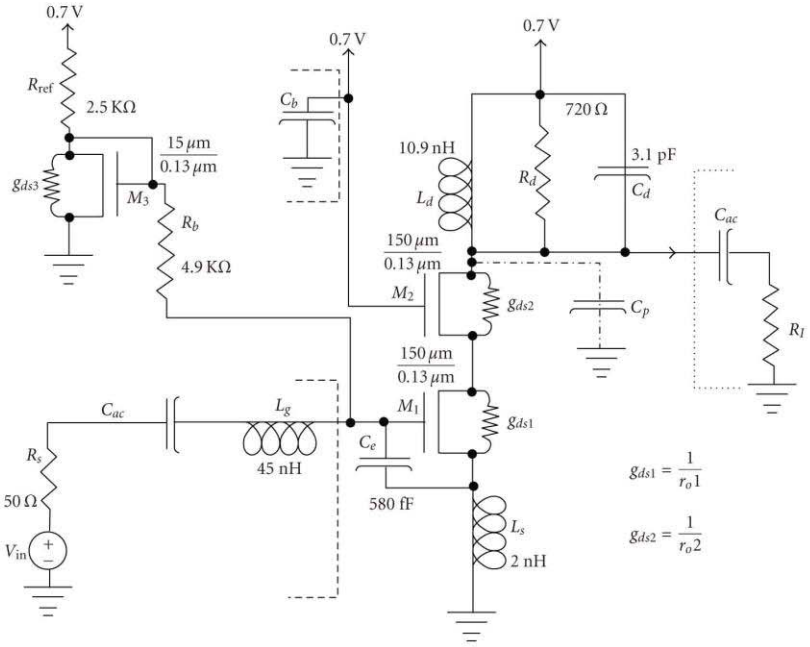

FIGURE 1: Proposed narrow-band circuit topology for 866 MHz RFID LNA.

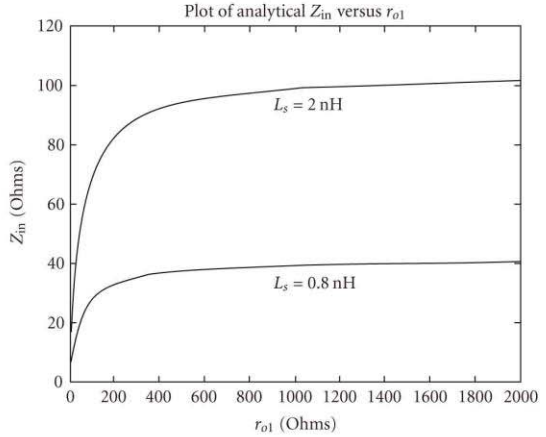

FIGURE 2: Variation of the analytical Z_{in} with finite output impedance (r_{o1}) of M1 fornanometric CMOS.

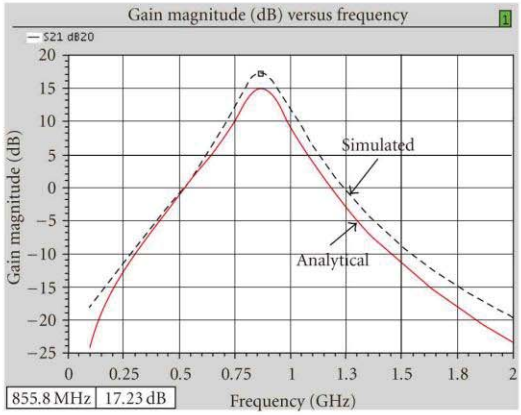

FIGURE 3: Analytical and simulated gain-magnitude (A_V in dB) of the RFID LNA.

for noise match can be derived to achieve the theoretical F_{min} [5, 6]. The effect of the finite device conductance g_{ds} (= $1/r_0$) due to the deeply scaled short channel length is included in this design optimization. With regard to the input impedance matching at resonance, we can easily derive

$$Z_{in} \cong \frac{g_{m1}}{C_t} \frac{L_s g_{m2}}{(g_{ds1} + g_{m2})}, \quad (1)$$

where C_t equals $C_{gs1} + C_e$, g_{ds1}(= $1/r_{o1}$) is the output conductance of M_1, while g_{m1} and g_{m2} are the transconductances of the cascode transistors M_1 and M_2, respectively. Typically Z_{in} at resonance changed by 6%–12% due to the inclusion of g_{ds1} in (1) as indicated by the plot in Figure 2 of the analytical Z_{in} with variation in the r_{o1} of M_1 (being around 450 ohms in this design) from the long channel assumption ($r_{o1} \rightarrow \infty$). In addition, as shown in Figure 2, the extent of Z_{in} inaccuracy with long channel assumption also varies

with the chosen value of L_s, the source inductor. Equation (1) also indicates that for deep nanometric design the finite output conductance of M_1 adds an additional trade-off factor in determining the value of the capacitor C_e (in C_t) required for achieving power-constrained input matching. Changing the overdrive and/or the geometry of M_2 (and hence g_{m2}) in relation to g_{ds1} provides an additional degree of freedom to reach this value of C_e for input matching. Essentially this trade-off enables a lower value of C_e and hence a higher ω_T in achieving input impedance matching for a given g_{m1}. In addition, inclusion of the finite g_{ds} effect provides a more accurate power constrained simultaneous optimization of noise and impedance matching for nanometric CMOS (hence it is termed *enhanced* PCSNIM). The s-domain gain transfer function of the RFID LNA can be determined by first finding the short circuit transconductance (G_{M1}) and then the open circuit output impedance (Z_{OUTM1}) at the drain of M_1. Hence, we can deduce the voltage gain as

$$A_v(s) = \frac{\left[g_{m1} + \left((sC_t + g_{m1})(R_{Ls} + sL_s)\right)/(r_{01} + R_{Ls} + sL_s)\right] * (1/(sC_d + 1/R_d + 1/sL_d))}{\left[1 + sC_t\left(R_s + R_{\mathrm{Lg}} + R_{Ls} + R_{\mathrm{ge}} + sL_g + sL_s\right) + \left(g_{m1} + sC_t\right)\left((r_{01}(R_{Ls} + sL_s))/(r_{01} + R_{Ls} + sL_s)\right)\right]}, \tag{2}$$

where R_s is the source resistance, R_{Lg} is the series resistance of the gate inductor, R_{Ls} is the series resistance of the source inductor, and R_{ge} is an equivalent gate resistance due to the addition of C_e, which is smaller than the original gate resistance R_g of the transistor M_1. The dB magnitude comparison of the theoretical (analytical) gain with the simulated gain is shown in Figure 3 indicating close agreement between the two. A technique based on determining the short circuit output noise current power at the drain of M_1 was used for the noise analysis. In this method the output load is shorted compared to the method in [5] where the output noise current is determined with the output load. Since the noise factor is defined as the ratio of the total mean-squared output noise current due to all the noise sources to the input source only, and as the noise factor mostly depends on the front-end noise sources farthest from the output load, almost the same value of noise factor is obtained using this technique without the extra calculation, compared to if the output noise current with load is used in the computation. Hence, the noise factors of the front-end noise sources using this short circuit output noise current method, are added to obtain the overall frequency behavior of the noise factor ($N(f)$) given by

$$\begin{aligned} N(f) = 1 &+ \frac{\delta_1\alpha_1}{5}\frac{\omega^2 C_{gs1}^2}{R_s g_{m1}}\frac{\left\{g_{m1}r_{01}^2R_s - \omega^2L_s\left[L_s + g_{m1}r_{01}\left(L_s + L_g\right)\right]\right\}^2 + \omega^2 r_{01}^2\left[L_s(1 + g_{m1}R_s) + g_{m1}r_{01}\left(L_g + L_s\right)\right]^2}{\omega^2C_t^2\left(r_{01}^2 + \omega^2L_s^2\right)\left(\omega L_s + g_{m1}r_{01}/\omega C_t\right)^2} \\ &+ \frac{\gamma_1 g_{m1}}{\alpha_1 R_s}\frac{r_{01}^2\left\{\left[1 - \omega^2C_t\left(L_g + L_s\right)\right]^2 + \omega^2C_t^2R_s^2\right\}}{\omega^2C_t^2\left(\omega L_s + g_{m1}r_{01}/\omega C_t\right)^2} \\ &+ 2j|c_1|\frac{\omega C_{gs1}r_{01}}{R_s\omega^2C_t^2\left(\omega L_s + g_{m1}r_{01}/\omega C_t\right)^2} \\ &\times\sqrt{\frac{\delta_1\gamma_1}{5}\frac{\mathfrak{A}\omega^2r_{01}^2\left[L_s(1 + g_{m1}R_s) + g_{m1}r_{01}\left(L_g + L_s\right)\right]^2\left\{\left[1 - \omega^2C_t\left(L_g + L_s\right)\right]^2 + \omega^2C_t^2R_s^2\right\}}{\left(r_{01}^2 + \omega^2L_s^2\right)}}, \end{aligned} \tag{3}$$

where $\mathfrak{A}$ denotes $\{g_{m1}r_{01}^2R_s - \omega^2L_s[L_s + g_{m1}r_{01}(L_s + L_g)]\}^2$. It is evident from (3) that inclusion of g_{ds1} $(= 1/r_{o1})$ provides a more detailed expression and hence a more accurate estimate of the noise factor.

3. Simulation and Experimental Results

The LNA (as part T8BTAU) was fabricated using the 130 nm IBM CMOS process available through MOSIS. Figure 4 shows the microphotograph of the 0.571 sq.mm die. The outer diameters of the inductors were, respectively, 240 μm for L_d and 140 μm for L_s with 5 μm wide trace of top thick aluminum layer MA and underpass contact copper layer E1. The capacitors C_e and C_d were fabricated as MIM (metal-insulator-metal) capacitors, and the resistors were fabricated using p+ poly layer with high-sheet resistance (340 $\Omega/\square$). Figure 5 shows the simulated and measured forward power gain, S_{21} under matched condition [8], indicating reasonably high-Q tuning at 866 MHz with measurement being 4 dB below simulation due to loss along external matching circuit. The measured input reflection coefficient S_{11} is approximately ≈ -12 dB at 866 MHz as shown in Figure 6, while the

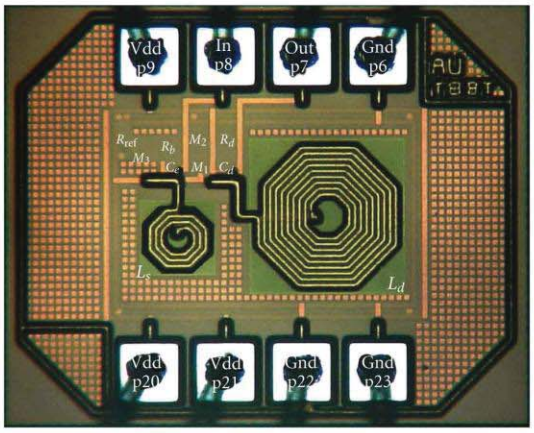

FIGURE 4: Microphotograph of the fabricated RFID LNA.

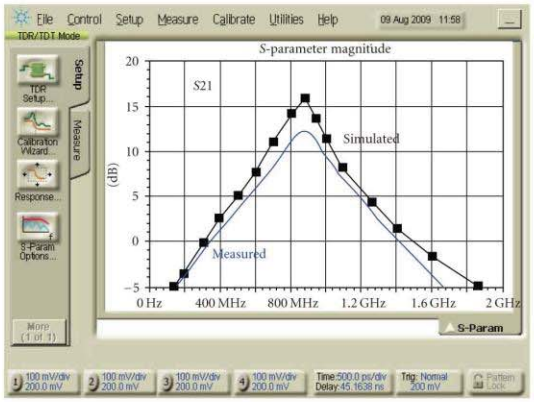

FIGURE 5: Forward gain, S_{21} (in dB) of the RFID LNA.

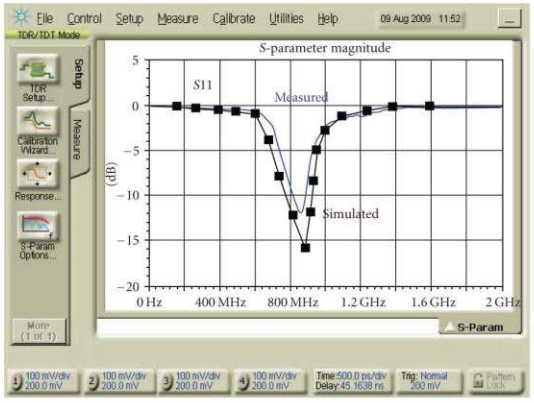

FIGURE 6: Input reflection coefficient, S_{21} (in dB) of the RFID LNA.

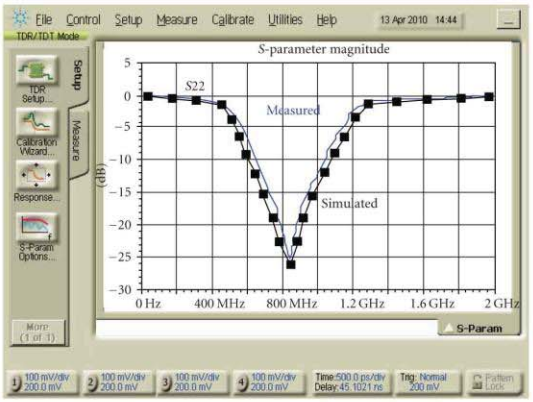

FIGURE 7: Output reflection coefficient, S_{22} (in dB) of the RFID LNA.

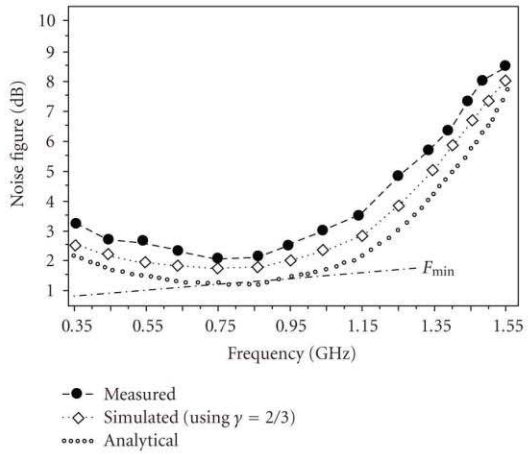

FIGURE 8: Noise figure (NF in dB) of the RFID LNA.

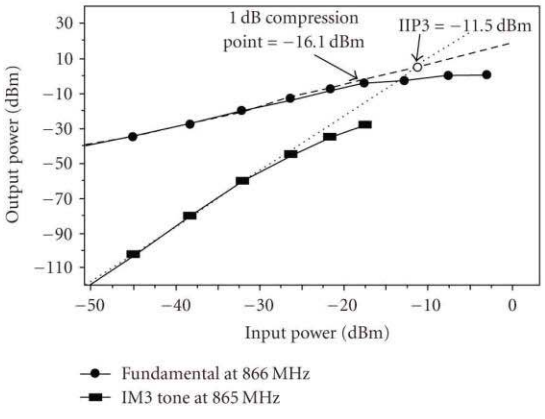

FIGURE 9: The IIP3 and 1 dB compression points for the UHF RFID LNA.

Table 1: Summary of the 866 MHz UHF RFID LNA performance and comparison with previous UHF LNA designs.

	This work	[1]	[2]	[3]	[4]	[5]	[7]
Technology (nm)	130	250	350	180	350	0.25	180
S_{11} (dB)	−12	−11.8	−10	−29	−14	−18	N/A
S_{21} (dB)	12	7.2	17.5	12.5	17	12	15
S_{12} (dB)	−34	−27.4	N/A	−60	−22	N/A	N/A
S_{22} (dB)	−25	−20	N/A	−33	N/A	N/A	N/A
NF (dB)	2.2	4.7	2	0.7	3.4	1.35	2.9
IIP3 (dBm)	−11.5	−1.8	−6	−4	−5.1	−4	N/A
P1dB (dBm)	−16.1	−9.3	N/A	−9	−23	−15	−15
P_{diss} (mW)	0.85	19.5	21.6	3.9	13	2	4.32
Supply Voltage (V)	0.7	2.5	2.7	1.8	2.3	1.25	1.8
f_0 (MHz)	866	900	900	915	900	900	900

output reflection coefficient S_{22} is measured to be ≈ -25 dB at 866 MHz as shown in Figure 7. These measurements were carried out using external matching elements and indicates close agreement with the simulation. All measurements include trace and connector losses. Figure 8 shows the comparison of the analytical, simulated and measured NF spectrum which verifies the close approximation provided by (3) due to the inclusion of the finite g_{ds} effect. The measured NF was around 2.2 dB. The IIP3 and the 1-dB compression points were determined to be −11.5 dBm and −16.1 dBm, respectively, as shown in Figure 9. Finally, Table 1 shows a summary of performance comparison of the proposed UHF LNA with other UHF LNA designs indicating the low NF achieved at sub-mW power.

4. Conclusion

The improved power constrained optimization of an UHF RFID LNA design at 866 MHz considering finite g_{ds} effects is presented and measurement results are demonstrated. The design achieves very low NF using only a 0.7 V supply voltage and consuming only 850 μW

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8.4 Published Journal Paper II: A 0.7 V 850 μW CMOS LNA for UHF RFID reader[212]

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A 0.7 V 850 μW CMOS LNA FOR UHF RFID READER

Jie Li and S. M. Rezaul Hasan
CRAVE—Centre for Research in Analogue and VLSI microsystem dEsign, School of Engineering and Advanced Technology, Massey University, Albany, Auckland, New Zealand; Corresponding author: hasanmic@massey.ac.nz

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ABSTRACT: *The design of a narrow-band cascoded CMOS inductive source-degenerated low noise amplifier (LNA) for 866 MHz UHF RFID reader is presented. Compared to other previously reported narrow-band LNA designs, in this work the finite g_{ds} ($= 1/r_0$) effect has been considered to improve the nanometric design, achieving simultaneous impedance and minimum F_{min} noise matching at a very low power drain of 850 μW from a 0.7-V supply voltage. The LNA was fabricated using the IBM 130 nm CMOS process delivering a power gain (S_{21}) of ≈12 dB, a reverse isolation (S_{12}) of ≈−34 dB, and an input power reflection (S_{11}@866 MHz) of ≈−12 dB. It had a minimum pass-band NF of around 2.2 dB and a 3rd order input referred intercept point (IIP3) of ≈−9.5 dBm.* © 2010 Wiley Periodicals, Inc. Microwave Opt Technol Lett 52:2780–2782, 2010; View this article online at wileyonlinelibrary.com. DOI 10.1002/mop.25600

Key words: *radio frequency identification; radio frequency integrated circuits*

1. INTRODUCTION

RFID (radio-frequency identification) is one of the fastest growing wireless communication technologies for commercial product tracking. As the low noise amplifier (LNA) is the first block in the front-end of the RFID reader which is tuned at a certain trans-receiver frequency, it needs to be designed optimally to minimize the noise for the following stages and avoid the distortion of the source signal (requires good linearity). To overcome design trade-off difficulties between gain, power, noise figure (NF) and matching in the optimization of the LNA, the design of the matching circuits at the input and the output are based, respectively on minimal NF and maximal power transfer. In recent years, considerable research on CMOS LNA design in submicron technologies at 900 MHz has been reported by authors in [1–4]. A lower frequency standard at 866 MHz for UHF RFID is also implemented in Europe, Africa, and New Zealand. Low power dissipation at low supply voltage is a significant design criterion for RFID applications synthesized by design trade-off between gain, NF, input and output impedance matching and high linearity. In this article we discuss the complete design and the experimental results for a 0.7-V low-power 130 nm CMOS 866 MHz single-ended common-source telescopic cascode LNA using an enhanced power constrained simultaneous noise and impedance matching (PCSNIM [5, 6]) technique.

2. PRINCIPLES AND CIRCUIT DESIGN

An inductively source degenerated telescopic cascode topology has been chosen for the 866 MHz RFID LNA design because of its current reuse structure and hence it consumes less bias current than the folded cascode. Figure 1 shows the circuit diagram of the

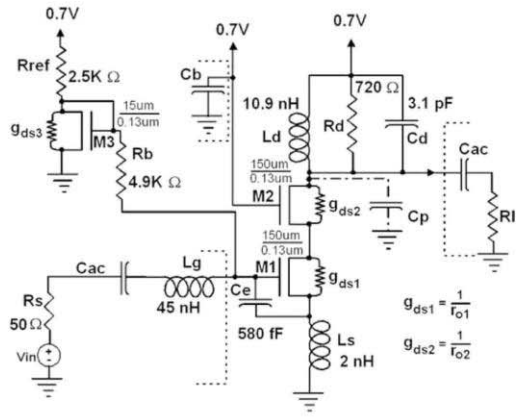

Figure 1 Proposed narrow-band circuit topology for 866-MHz RFID LNA

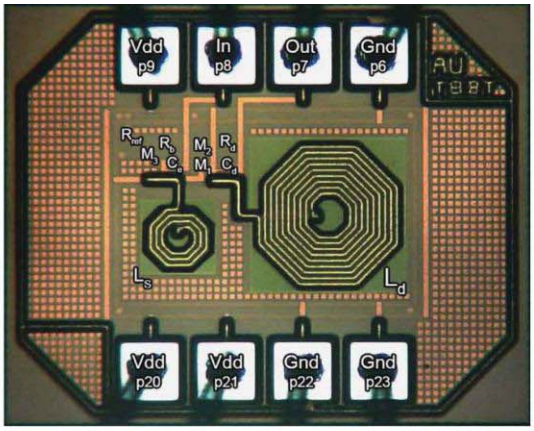

Figure 2 Micro-photograph of the fabricated RFID LNA. [Color figure can be viewed in the online issue, which is available at wileyonlinelibrary.com]

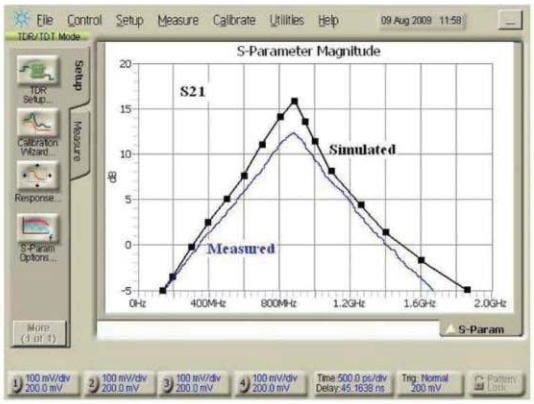

Figure 3 Forward power gain, S_{21} (in dB) of the RFID LNA. [Color figure can be viewed in the online issue, which is available at wileyonlinelibrary.com]

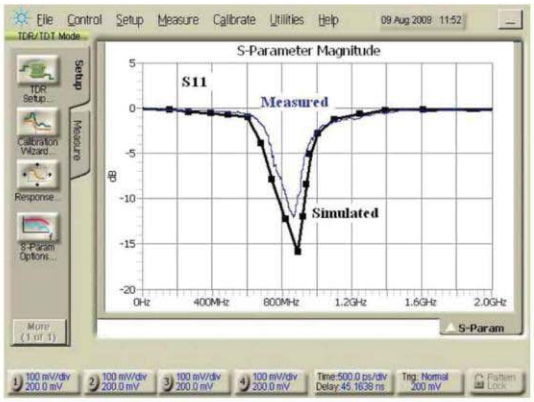

Figure 4 Input reflection coefficient, S_{11} (in dB) of the RFID LNA. [Color figure can be viewed in the online issue, which is available at wileyonlinelibrary.com]

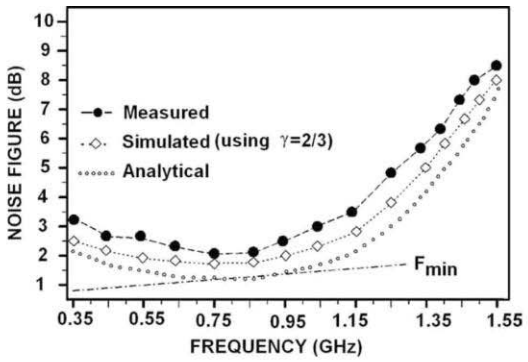

Figure 5 Noise Figure (NF in dB) of the RFID LNA

proposed RFID LNA. M_1 and M_2 forms the cascode configuration and their bias current are driven by M_3 and R_{ref}. L_d, R_d, and C_d forms the output tank circuit tuned at 866 MHz with an angular frequency bandwidth of $\frac{1}{R_d * C_d}$. C_{ac} are AC-coupling capacitors while C_b is an AC grounding capacitor at the gate of the cascading device M_2. An improved PCSNIM technique is adopted here for the cascode structure optimization. C_e is in parallel with C_{gs1} of M_1 to achieve minimum noise figure F_{min} with power constraint and higher ω_T. Optimal impedance Z_{opt} for noise match can be derived to achieve theoretical F_{min} [5]. With regard to the input impedance matching at resonance, we can easily derive:

$$Z_{in} \cong \frac{g_{m1}}{C_t} \frac{L_s g_{m2}}{(g_{ds1} + g_{m2})} \tag{1}$$

where, C_t equals $C_{gs1} + C_e$, g_{m1} and g_{m2} are the trans-conductances of the cascode transistors. The effect of the finite device conductance $g_{ds} = (1/r_0)$ at deeply scaled channel length is thus included in this design which provides an additional degree of design flexibility. The s-domain gain transfer function of the RFID LNA can be determined by first finding the short circuit transconductance (G_{M1}) and the open circuit output impedance (Z_{OUTM1}) at the drain of M_1. Hence, we can deduce the voltage gain as:

$$A_v(s) = \frac{\left[g_{m1} \frac{(sC_t + g_{m1})(R_{Ls} + sL_s)}{(r_{01} + R_{Ls} + sL_s)}\right] * \left(\frac{1}{sC_d + 1/R_d + 1/sL_d}\right)}{\left[1 + sC_t(R_s + R_{Ls} + R_{ge} + sL_g) + (g_{m1} + sC_t)\frac{r_{01}(R_{Ls} + sL_s)}{r_{01} + R_{Ls} + sL_s}\right]} \tag{2}$$

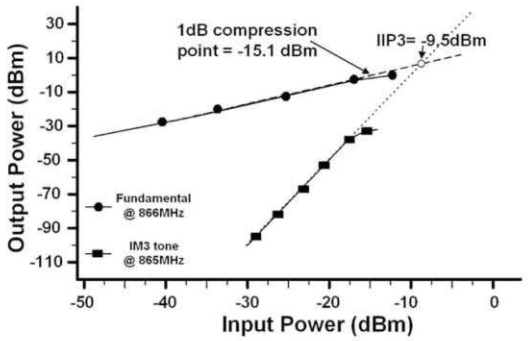

Figure 6 The IIP3 and 1dB compression points for the UHF RFID LNA

TABLE 1 Summary of the 866-MHz UHF RFID LNA Performance and Comparison with Previous UHF LNA Designs

	This work	[1]	[2]	[3]	[4]	[5]	[7]
Technology (nm)	130	250	350	180	350	0.25	180
S_{11} (dB)	−12	−11.8	−10	−29	−14	−18	N/A
S_{21} (dB)	12	7.2	17.5	12.5	17	12	15
S_{12} (dB)	−34	−27.4	N/A	−60	−22	N/A	N/A
NF (dB)	2.2	4.7	2	0.7	3.4	1.35	2.9
IIP3 (dBm)	−9.5	−1.8	−6	−4	−5.1	−4	N/A
P1dB (dBm)	−15.1	−9.3	N/A	−9	−23	−15	−15
P_{diss} (mW)	0.85	19.5	21.6	3.9	13	2	4.32
Supply voltage (V)	0.7	2.5	2.7	1.8	2.3	1.25	1.8
f_0 (MHz)	866	900	900	915	900	900	900

where, R_s is the source resistance, and, R_{ge} is smaller than the original gate resistance R_g of the transistor M_1 due to the addition of C_e. A novel technique based on determining the short circuit output noise current power at the drain of M_1 was used for the noise analysis. Noise factors of the front-end noise sources are added to obtain the overall frequency behavior of the noise factor ($N(f)$) given by.

$$N(f) = 1 + \frac{\delta_1\alpha_1}{5}\frac{\omega^2 C_{gs1}^2}{R_s g_{m1}}\frac{\left\{g_{m1}r_{01}^1 R_s - \omega^2 L_s\left[L_s + g_{m1}r_{01}\left(L_s + L_g\right)\right]\right\}^2 + \omega^2 r_{01}^1\left[L_s(1 + g_{m1}R_s) + g_{m1}r_{01}\left(L_g + L_s\right)\right]^2}{\omega^2 C_t^2\left(r_{01}^2 + \omega^2 L_s^2\left(\omega L_s + \frac{g_{m1}r_{01}}{\omega C_t}\right)^2\right.} + \frac{\gamma_1 g_{m1}}{\alpha_1 R_s}\frac{r_{01}^2\left\{\left[1 - \omega^2 C_t(L_g + L_s)\right]^2 + \omega^2 C_t^2 R_s^2\right\}}{\omega^2 C_t^2\left(\omega L_s + \frac{g_{m1}r_{01}}{\omega C_t}\right)^2} + 2j|c_1|\frac{\omega C_{gs1}r_{01}}{R_s\omega^2 C_t^2\left(\omega L_s + \frac{g_{m1}r_{01}}{\omega C_t}\right)^2}$$
$$\times\sqrt{\frac{\frac{\delta_1\gamma_1}{5}\left\{g_{m1}r_{01}^2 R_s - \omega^2 L_s[L_s + g_{m1}r_{01}(L_s + L_g)]\right\}^2 + \omega^2 r_{01}^2[L_s(1 + g_{m1}R_s) + g_{m1}r_{01}(L_g + L_s)]^2\left\{\left[1 - \omega^2 C_t(L_g + L_s)\right]^2 + \omega^2 C_t^2 R_s^2\right\}}{(r_{01}^2 + \omega^2 L_s^2)}} \quad (3)$$

3. SIMULATION AND EXPERIMENTAL RESULTS

The LNA (as part T8BTAU) was fabricated using the 130 nm IBM CMOS process available through MOSIS. Figure 2 shows the micro-photograph of the 0.571 mm^2 die. The outer diameters of the inductors were respectively 240 μm for L_d and 140 μm for L_s with 5 μm wide trace of top thick aluminum layer MA and underpass contact copper layer E1. The capacitors C_e and C_d were fabricated as MIM capacitors and the resistors were fabricated using p^+ poly layer with high sheet resistance (340 Ω/□). Figure 3 shows the simulated and measured forward power gain S_{21}, indicating reasonably high-Q tuning at 866 MHz with measurement being 4-dB below simulation due to loss along external matching circuit. The measured input reflection coefficient S_{11} is approximately ≈−12 dB at 866 MHz as shown in Figure 4. Figure 5 shows the comparison of the analytical, simulated, and measured NF spectrum which verifies the close approximation provided by (3) due to the inclusion of the finite g_{ds} effect. The measured NF was around 2.2 dB. The IIP3 and the 1-dB compression points were determined to be −9.5 and −15.1 dBm, respectively as shown in Figure 6. Table 1 shows a summary of performance comparison of the proposed UHF LNA with other UHF LNA designs indicating low NF achieved at sub-mW power.

4. CONCLUSION

The improved power constrained optimization of an UHF RFID LNA design at 866 MHz considering finite g_{ds} effects is presented and measurement results are demonstrated. The design achieves very low NF using only a 0.7-V supply and 850-μW power dissipation.

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BAND-NOTCHED DESIGN OF THE PLANAR MONOPOLE ANTENNA FOR WLAN/WiMAX APPLICATIONS

Kang-Kang Chen and Ji-Xiang Zhao
Department of Signal and Information Processing, China Jiliang University, Hangzhou 310018, China; Corresponding author: chenkk0124@gmail.com

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ABSTRACT: *A simple printed monopole antenna with tunable slots is proposed for wireless local area network (WLAN) and worldwide*

8.5 Published Conference Paper I: A Bias-Controlled Noise-Canceling CMOS Tuned Low Noise Amplifier for UWB Transceivers [213]

A Bias-Controlled Noise-Canceling CMOS Tuned Low Noise Amplifier for UWB Transceivers

S. M. Rezaul Hasan
Center for Research in Analog & VLSI microsystem dEsign(CRAVE),
Institute of Technology and Engineering,
Massey University, Auckland, New Zealand
hasanmic@massey.ac.nz

Jie Li
Center for Research in Analog & VLSI microsystem dEsign(CRAVE),
Institute of Technology and Engineering,
Massey University, Auckland, New Zealand

***Abstract*—This paper describes a noise canceling tuned CMOS LNA using the TSMC 0.18μm 3M2P CMOS process technology for 3.1GHz-10.6GHz Ultra Wide Band (UWB) RF Receiver system. Bias-controlled noise canceling technique is used to improve the Noise Figure of a common-gate RF amplifier, which is Ultra-Wide-Band tuned by a matched 3rd order Band-pass Butterworth LC filter section. The amplifier had a –3db bandwidth(between the corner frequencies) of around 6.3 GHz with a power gain(S21) of ≈ 11dB consuming around 55mW. Also, the amplifier had a noise figure(NF) under 5dB within the UWB pass-band utilizing the bias-controlled noise canceling technique. It had an IIP3 of -2.4dBm and a 1dB compression point of -13dBm at 5GHz. In addition S-parameter simulations indicated a reverse isolation of -100dB (from the S12 plot).**

I. INTRODUCTION

Wireless systems using Ultrawideband(UWB)[1] technology is a newly emerging low-power and high data rate broad-band communication technique with RF signal in the 3.1GHz to 10.6GHz RF spectrum. Two techniques to exploit the UWB spectrum are presently being pursued. One uses multi-band OFDM modulation with 14 528-MHz sub-bands and a fast frequency hopping scheme[2]. The other employs narrow binary base-band signal pulses (impulses!) to switch the RF carrier's amplitude between "Full" and "Null" states[5], or its polarity which results in signal spreading over several gigahertz of bandwidth[3]. The consequence is a broad-band RF trans-reception with the benefit of reduced power dissipation. Similar to a narrow-band system, a UWB receiver will require a preamplification stage consisting of a Low Noise Amplifier (LNA), but, the LNA input impedance must in this case be matched to a 50ohm antenna over the entire extent of the UWB spectrum. In addition, the LNA must exhibit near-flat power-gain over the entire UWB bandwidth, have a low noise figure(NF) and a low DC power consumption. This paper describes the improved design of a low power tuned CMOS UWB LNA[6] which employs a bias-controlled noise cancellation technique to improve the Noise Figure of the tuned UWB LNA.

II. BIAS-CONTROLLED NOISE CANCELING COMMON-GATE UWB LNA TOPOLOGY

Fig. 1 shows the circuit architecture of the bias-controlled noise canceling UWB LNA. A three-segment 6th order band-pass butterworth passive LC π-section is used to interface the antenna with the input of a common-gate(CG) pre-amplification stage[9]. The passive LC π-section is matched at the input to the antenna characteristic impedance of 50Ω and at the output to the input impedance of the CG pre-amplifier looking into the source. The CG stage is chosen at the input for exploiting its low noise figure[6], and its low input impedance ($\cong \frac{1}{g_m}$) which has a broadband behavior. The impedance matched band-pass LC Butterworth section was obtained using an automatic filter generation software [7]. Consideration was given to monolithic realizibility of passive component values, pass-band ripple, phase behavior and stop-band roll-off in choosing the appropriate filter-section among several types available (Bessel, Butterworth, Chebyshev, Elliptic, Hourglass etc.). A π-section was chosen instead of a T-section in order to facilitate absorption of the MOSFET capacitances into the grounded capacitor at the output-end of the LC-filter section. Although the band-pass π-section uses low-Q inductors available in low-cost CMOS process, a sharp enough pass-band to stop-band roll-off is obtained in conjunction with shunt peaking within the amplifying section of the UWB LNA (out-of-band signals are de-emphasized twice, once by the filter and once by the shunt peaking amplifier). Compared to the recently reported UWB LNA[4] (& well-know narrow-band LNA topologies[6]) based on an inductive source degenerated telescopic cascode, the proposed CG architecture provides easy pre-inclusion of MOSFET parasitic capacitances (C_{gs} & C_{sb}) at the output-end of the LC filter section into the filter capacitance value. In addition, the π-section also enables DC-biasing of the source terminal through the output-end inductor. The component level description of the topology is as follows: L1,C1,L2,C2,L3 & C3 are the components of the passive LC π-section. The absolute component values are obtained by frequency-scaling (scale-factor $=10^9$) a normalized band-pass

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filter (matched to 50Ω at the input-port and $\frac{1}{g_{m1}}$ of M1 at the output-port) with approximately 3.1Hz-10.6Hz Bandwidth. The curved plate of the capacitor indicates the bottom-plate in a monolithic implementation. The parasitic capacitance at the bottom-plate of the floating capacitor C2 is absorbed in the value of the grounded capacitor C3. M1 is the input CG NMOS device loaded with the drain DC-feed choke L4. R4 constitutes the DC-bias drain-load which is partially harnessed from the series resistance of the choke L4 (assuming a fairly low inductor quality, Q < 4). L4 is set to resonate with the total capacitance at the drain node of M1 (C_{D1tot}) near an upper middle frequency of the UWB. The outputs from the drain and source of M1 are fed into two common source amplifiers Ma & Mb respectively with Ma being current source biased. Varying the current source with Vbc causes the channel length modulation of Ma to vary C_{GS} and the overall capacitance & hence the impedance Za at node 4. The noise voltages at node 4 and node 3 due to the drain current noise of M1 are out of phase and tend to mutually cancel at the node 5[8]. The low-Q inductor L6 provides shunt peaking of the output at node 5. The resultant noise cancelled signal at node 5 is then fed into the telescopic cascode stage M4,M5 through the source-followers M2, M3. The cascode is loaded with the drain DC-feed choke L5. R5 constitutes the DC-bias drain-load of the cascode which is partially harnessed from the series resistance of the choke L5 (assuming a fairly low inductor quality, Q < 6). L5 is set to resonate with the total capacitance at the drain node of M5 (C_{D5tot}) near a lower middle frequency of the UWB. The combination of parallel resonant tanks near the two ends of the UWB ensures reasonably flat gain at the final output. The final pre-amplifier output is provided through the source-follower M6 which can then be cascaded to a correlator[4] for carrier (or pseudo-carrier) removal.

The noise-factor (F) of the pre-amplifier is given by $F = \frac{SNR_{in}}{SNR_{out}}$, where, SNR_{in} and SNR_{out} are the Signal-to-Noise-Ratio's at the input source and at the output respectively. The noise contributing elements in the amplifier are the thermal noise due to resistors and finite inductor Q and the drain current noise of the MOSFET devices (mainly M1). If v_n is the input referred noise voltage, i_n is the input referred noise current, and, R_S is the source resistance, then $F = 1 + \frac{\overline{(v_n + i_n R_s)^2}}{4kTR_s}$ [6]. The noise figure (NF) is given by $NF = 20\log_{10} F$ which is a Figure-Of-Merit for the UWB low-noise pre-amplifier.

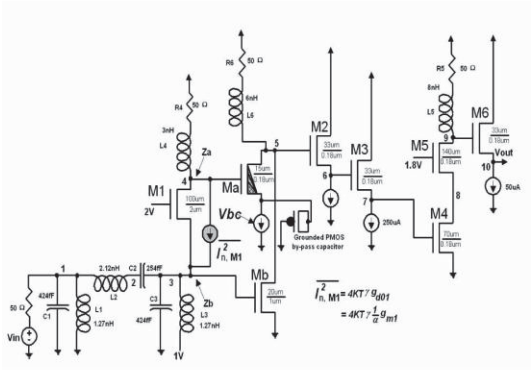

Figure 1. A bias-controlled noise-canceling tuned common-gate ultrawideband low-noise RF pre-amplifier.

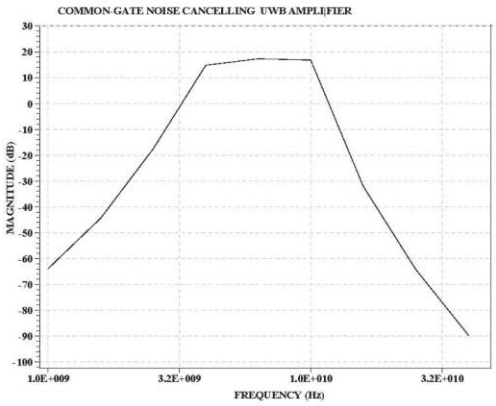

Figure 2. The T-SPICE RF gain-magnitude (in dB) and bandwidth of the tuned noise-canceling UWB low-noise pre-amplifier.

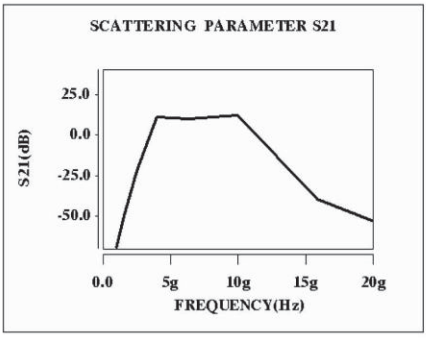

Figure 3. HSPICE simulated scattering-parameter forward power-gain, S_{21} (in dB) of the tuned noise-canceling UWB pre-amplifier.

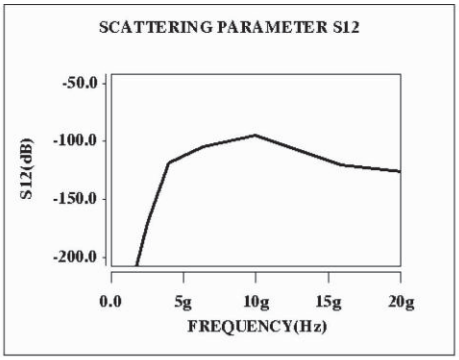

Figure 4. HSPICE simulated scattering-parameter *reverse* power-gain, S_{12} (in dB) of the tuned noise canceling UWB pre-amplifier.

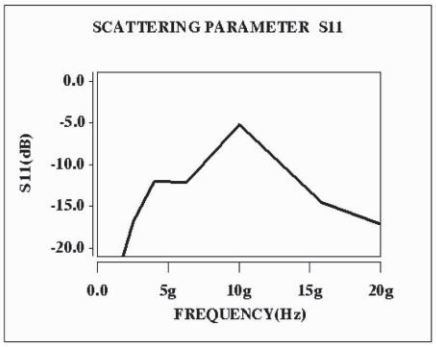

Figure 5. HSPICE simulated scattering-parameter input reflection co-efficient, $\Gamma_{in}(S_{11})$ (Return Loss in dB) of the tuned noise-canceling UWB pre-amplifier.

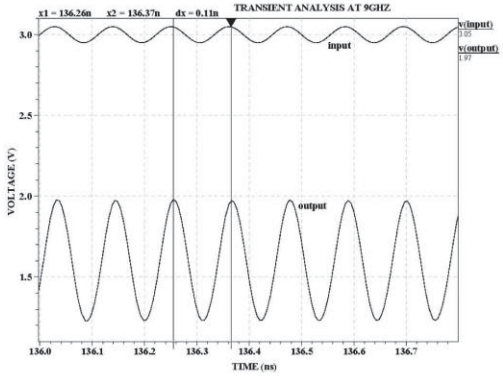

Figure 6. The T-SPICE transient analysis output of the noise-canceling UWB LNA at 9GHz RF input.

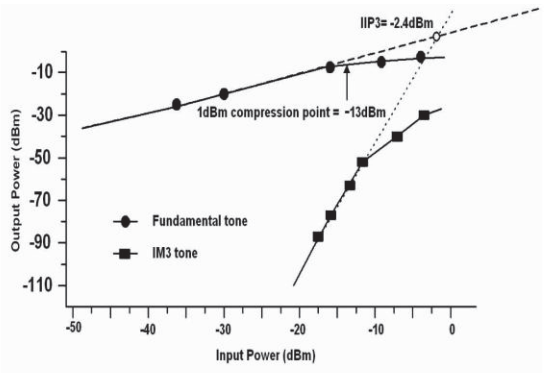

Figure 7. The HSPICE simulated IIP3 and 1dB compression point for the noise-canceling UWB LNA at 7GHz.

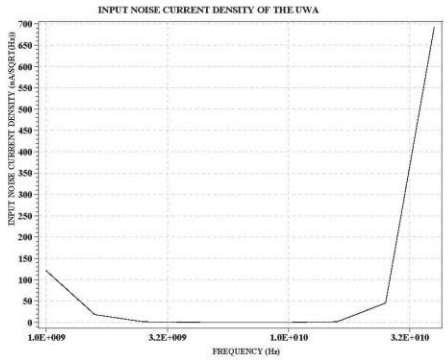

Figure 8. The T-SPICE simulated input noise current spectral density function for the tuned noise-canceling UWB LNA.

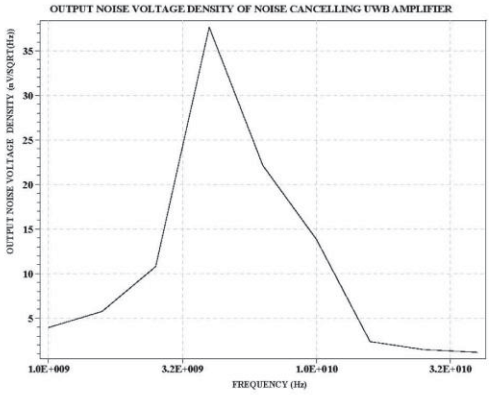

Figure 9. The T-SPICE simulated output noise voltage spectral density function for the tuned noise-canceling UWB LNA.

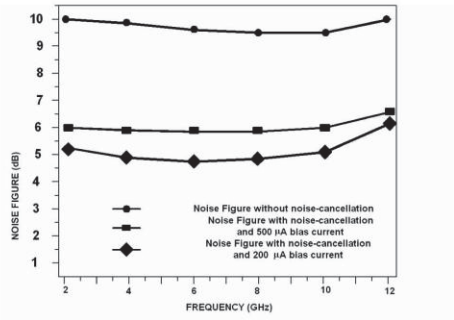

Figure 10. The simulated Noise Figure of the tuned noise-canceling UWB LNA.

III. Simulation Results

Extensive circuit simulations (using Tanner T-SPICE and Meta-software HSPICE) were conducted on the Ultra-Wide-Band amplifier using the TSMC 0.18μm 3M2P CMOS process technology. Fig. 2 shows the gain-magnitude and bandwidth behavior of the proposed UWB pre-amplifier. A near-constant gain of over 11dB is obtained over a 6.3GHz wide pass-band frequency range. In order to obtain practical network-level characterization of the proposed UWB pre-amplifier, power-wave description of the amplifier's characteristics in terms of a two-port scattering parameter model[6] was also undertaken using HSPICE (*not available with T-SPICE*). Fig. 3 shows the simulated forward power-gain S_{21} which appears to be in reasonably close agreement with the T-SPICE dB-magnitude simulation in Fig. 2. Next, Fig. 4 depicts the simulated reverse power-gain parameter S_{12} indicating the reverse isolation of the UWB amplifier. The maximum reverse gain is around -100dB which is a significant improvement over the results reported for the topology in [8][10], mainly because the proposed architecture is also a multi-stage topology with inter-stage source-follower isolation as well as a tuned front-end π-section isolating the input from the amplifier section. The input reflection coefficient $\Gamma_{in}(S_{11})$ is shown in Fig. 5 in terms of dB Return Loss, RL (which is expressed as RL= $-20\log|S_{11}|$). As the figure indicates, the input reflection coefficient corresponds to an average return loss of around -10dB within the UWB pass-band which is close to the results achieved in [4][8]. Result of a T-SPICE transient analysis is shown in Fig. 6 indicating linear output for a sinusoidal RF input at 9GHz. The Total-Harmonic-Distortion (THD) for this case was found to be around -57dB. The amplifier had a power consumption of around 55mW, mostly due to the large bias current through M1 in order to reduce $\frac{1}{g_{m1}}$ and hence the input referred noise current of the CG device M1. In order to evaluate intermodulation distortion (IM3) and dynamic range IIP3 and 1-dB compression point[6] simulations were carried out using a two-tone input of 8Ghz and 9Ghz. The resulting IM3 product at 7Ghz which falls in the middle of the UWB pass-band was varied by changing the amplitude of the two-tone inputs. The results of these simulations indicate a IIP3 of -2.4dBm and a 1dB compression point of -13dBm (referred to the input) as shown in Fig. 7. Figs. 8 and 9 indicates respectively the input noise current spectral density function and the output noise voltage spectral density function. The average output noise voltage spectral density was ≈15nV/sqrt(Hz) (with a peak of ≈38nV/sqrt(Hz)) while the input noise current spectral density was below 0.06nA/sqrt(Hz) within the amplifier's output pass-band. Finally, Fig. 10 shows the simulated Noise Figures(NF) for different cases. With Mb turned off NF was hovering at around 10dB, while with Mb turned on with a 500μA bias current it was at around 6dB. If the bias current is reduced to 200 μA the NF improved to around 5dB (or just below 5dB). This simulation indicates the viability of the novel technique of bias-controlled noise cancellation.

IV. Conclusion

A novel bias-controlled noise-canceling UWB LNA design has been described and extensive SPICE simulation results has been reported. The amplifier is found to provide reasonable power gain within a 6.3GHz pass-band along with excellent reverse isolation and is suitable for applications in emerging UWB transceiver applications. In addition, the UWB amplifier has a low Noise Figure which can be improved by bias-controlled noise-cancellation. It has a wide dynamic range (IIP3 =-2.4dBm) as well as low power dissipation(55mW), and hence, compares favorably to other recently reported UWB low-noise pre-amplifiers.

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8.6 Published Conference Paper II: Comparison of Optimized Low-Power LNA Topologies for 866 MHz UHF RFID [214]

The 16th Electronics New Zealand Conference (ENZCon), Dunedin, New Zealand, 18-20 November, 2009

Comparison of Optimized Low-Power LNA topologies for 866 MHz UHF RFID

[1] Jie Li and [2] S. M. Rezaul Hasan

Centre for Research in Analogue and VLSI Microsystems Design (CRAVE)
School of Engineering and Advanced Technology (SEAT)
Massey University, Albany Highway, Gate 4, Building 106, Albany, Auckland

Email: [1] J.Li.2@massey.ac.nz [2] hasanmic@massey.ac.nz

Abstract: **The design topologies of optimized CMOS low noise pre-amplifier (LNA) for UHF RFID reader at 866 MHz is investigated. Simulations and analysis based on inductively degenerated common-source (CS) single-end telescopic LNA, folded-cascode LNA and differential LNA are performed in detail. The significant feature of the LNA design is the simultaneous impedance and minimum F_{min} noise matching at a low UHF radio frequency, achieved at a very low power drain of 0.95 mW from a 0.7 V supply voltage for single-ended, 1.33 mW from a 0.5 V supply voltage for folded-cascode and 2 mW from a 0.7 V supply voltage for differential topology. Design using sub-1V supply voltage is quite challenging owing to inductor size and bias drain related noise factor degradation. The LNA was simulated in IBM 130nm 6-metal 1 poly RFMOS process technology to deliver a power gain (S_{21}) of over 16 dB, a reverse isolation of -40dB and an input power reflection of -16dB for all design topologies at 866 MHz. It had a minimum pass-band NF of around 1.2 dB (for all topologies) and a 3rd order input referred intercept point (IIP3) of -11.5 dBm for single-ended telescopic topology and -9.5 dBm for differential topology.**

Keywords: CMOS LNA, RFID, impedance matching, low power consumption, noise matching, narrow-band.

1 INTRODUCTION

RFID (radio-frequency identification) is one of fastest growing wireless communication technology nowadays for commercial products tracking. A RFID system usually consists of a transponder tag and a reader as shown in Fig. 1. The low noise amplifier (LNA) is the first block in the front-end of the RFID reader that is tuned at a certain trans-receiver frequency. A longer distance can be achieved under UHF band at low power dissipation. However, the LNA need to be designed optimally to minimize the noise for following stages and avoid the distortion of the source signal (requires good linearity).

Considerable research on CMOS LNA design in submicron technologies has been approached in recent years: from topology investigation[1, 2] and guideline[3] to various novel ideas on the design improvement of multiple band[4], low-noise figure[5-7], high power gain[8], low power consumption[7, 9-11], and high linearity. The LNA designs at 900 MHz also have been reported by authors in [2, 4, 5, 7, 12]. A lower frequency standard operated at 866 MHz for UHF RFID is also implemented in Europe, Africa and New Zealand. Narrow-band CMOS LNA design at such sub-GHz frequencies has not been widely reported so far. Low power dissipation is a significant design criterion for RFID applications which will be synthesized by finding the trade-off between gain, low noise figure, input and output impedance matching and high linearity.

In this paper we discuss the complete design and comparison results for three integrated 130 nm CMOS 866 MHz LNAs. One is a single-ended common-source telescopic cascode LNA using an enhanced PCSNIM technique from [2], a folded-cascode LNA operated at 0.5V supply voltage and a differential LNA.

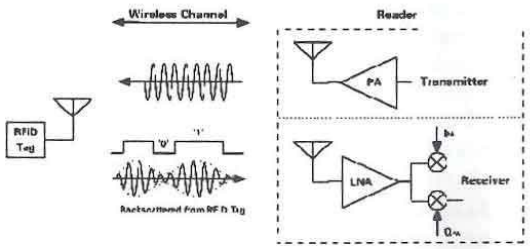

Fig.1 The Simulation Environment of Return Link for RFID system (Receiver, Wireless channel, and Tag)

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2 OPTIMIZED LOW-POWER UHF RFID LNA TOPOLOGIES

2.1 Single-Ended telescopic cascode LNA

A single-ended 866 MHz LNA is shown in Fig. 2. This amplifier has the commonly used cascoded architecture form, which provides a good isolation between the input and output stages. The input inductive degeneration topology formed by M_1 and L_s is employed here to get better noise performance for the narrow band applications. L_g is an external inductor for input reactance matching with L_s and C_e. The output impedance matching can be obtained by tuning the L_d, C_d, and R_d at 866 MHz with an angular frequency bandwidth of $(R_d * C_d)^{-1}$. Typically, both the input and the output impedances are required to match to R_s (50 Ω). M_3 in conjunction with R_{ref} controls the DC bias current through telescopic cascode while a large R_b ensures that noise and any ac signal pick-up at the gate of the current mirror is blocked and decoupled. C_{dc} is the DC blocking capacitance at both terminals.

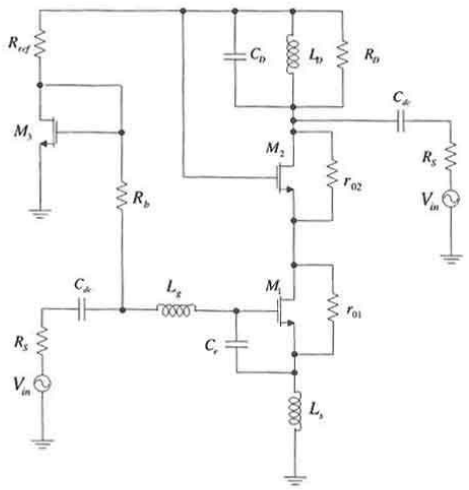


Fig.2 The Completed telescopic cascode LNA topology with DC bias voltage

Power constrained simultaneous noise and impedance matching technique (PCSNIM) is used as the basic design methodology. A smaller device size of M_1 is chosen for minimizing power dissipation. The extra capacitor C_e is in parallel with C_{gs1} of M_1 in order to achieve minimum noise figure $F_{\min}$ with power constrain and higher ω_T [2]. Optimal impedance Z_{opt} for noise match can be derived to achieve theoretical $F_{\min}$ $\left(\cong 1+\frac{2}{\sqrt{5}}\frac{\omega C_{gs1}}{g_{m1}}\sqrt{\delta\gamma\left(1-|c|^2\right)}\right)$ [2]. With regard to the input impedance matching, we can easily derive:

$$Z_{in} \cong R_l + R_g + s(L_s + L_g) + \frac{1}{sC_t} + \frac{g_{m1}}{C_t}\frac{L_s g_{m2}}{(g_{ds1} + g_{m2})}$$

$$\cong \frac{g_{m1}}{C_t}\frac{L_s g_{m2}}{(g_{ds1} + g_{m2})} \qquad \text{(at resonance)}$$

where R_l is the series resistance of the gate inductor, and R_g is the gate resistance of the transistor M_1. R_l can be neglected for high Q inductors and R_g can be reduced to insignificant levels by inter-digitating the device[1]. C_t here equals to $C_{gs1} + C_e$ and the effect of finite device conductance $g_{ds} = (1/r_0)$ is included at deeply scaled channel length.

At the central frequency of 866 MHz, the imaginary term of Z_{in} will be zero to match Z_s, which gives

$$s(L_s + L_g) + \frac{1}{sC_t} = 0$$

Optimum values can be calculated from above equations to satisfy PCSNIM technology. The noise figure NF is defined as

$$F = F_{\min} + \left[\frac{\gamma}{\alpha g_{m1} R_s}\right]\left[1 - \frac{Q_{opt}}{Q_s}\right]^2$$

The typical value of α is about 0.85, the optimum source quality factor (conductance) Q_{opt} and the actual source quality factor Q_s are defined as

$$Q_{opt} = \alpha\sqrt{\frac{\delta}{5\gamma}\left(1-|c|^2\right)}$$

and

$$Q_s = \frac{1}{\omega C_t R_s}$$

The expression for the width of the optimum device under power-constrained minimum noise figure is given by

$$W_{opt} = \frac{3}{2}\frac{1}{\omega L C_{ox} R_s Q_{sp}} \approx \frac{1}{3\omega L C_{ox} R_s}$$

The calculated width might give an extraordinary large value for short-channel CMOS technology (130nm) under low UHF frequency range. Hence, smaller value is adopted in order to satisfy the power-constrained technology practically. Furthermore, the impact of this input matching technique on linearity can also deteriorate under short-channel CMOS. A larger MOSEFT or a larger capacitor C_e can enhance the linearity by reducing L_g and L_s at the same time, but the NF may deteriorate.

2.2 *Folded-Cascode LNA*

The significant criteria for RFID application is not just low power consumption but low supply voltage as well. A folded-cascode topology can be adopted under ultra low supply voltage condition.

The basic circuit schematic of folded-cascode LNA consists of one NMOS transistor and one PMOS transistor as shown in Fig. 3. The voltage supply can be significantly reduced compared to the above telescopic cascode circuit. Similar to telescopic cascode topology, M_1 is the input transistor to provide the transconductance (g_m) of the LNA and M_2 is used as the current buffer to minimize the Miller effect and improve the response at high frequencies. However, one inherent feature of the folded cascode is that it allows simple gain control. This can be used to improve the overall linearity of the receiver. This is achieved by varying the gate voltage of M_2 to affect the impedance looking from the source (Z_p), hence adjusting the overall gain of the LNA. The overall voltage gain (A_{total}) of the tuneable LNA can be represented to be

$$A_{total} = A_v G_{tune} \cong g_{m1} R_o G_{tune}$$

where A_v is the fixed voltage gain of a conventional cascode LNA, R_o is the impedance of the output RLC resonant tank, and G_{tune} is the gain tuning factor that represents the portion of the AC signal current generated by input transistor M_1, which flows into the source of M_2. It is given by,

$$G_{tune} = \frac{Z_{blk}}{Z_{blk} + Z_p} = \frac{Z_{blk}(1 + g_{m2} r_{o2})}{Z_{blk}(1 + g_{m2} r_{o2}) + r_{o2}}$$

where $Z_{blk} = j\omega L_{blk}$ is given a large value to represent "blocking impedance" and Z_p is

$$Z_p = \frac{1}{g_{m2}} \| r_{02} \cong \frac{1}{g_{m2}}$$

where g_{m2} and r_{02} are the transconductance and the output resistance of M_2 respectively. It is evident that the A_{total} can be adjusted by varying g_{m2}, which is controlled by V_{bias}. Another advantage is that this gain control technology does not affect input matching.

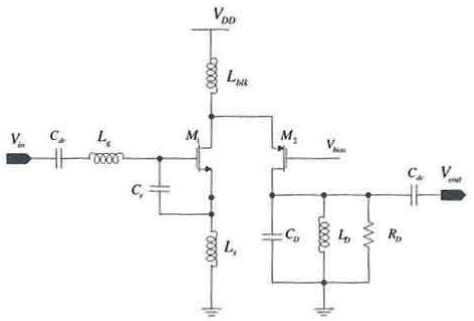


Fig.3 The folded-cascode LNA topology

2.3 *Differential LNA*

The single-ended and folded cascode architectures have the shortcoming of being sensitive to parasitic ground inductance. Differential architectures, on the other hand, will be somewhat immune to the common-mode interference from substrate or supply perturbations[1]. Therefore the differential LNA is also presented here in Fig. 4. The degenerating inductors (L_s) are connected together at the "virtual ground". At this point, a current source is usually placed to provide a current that is twice the current flowing down from each side of the LNA section. Any parasitic reactance in series with the bias current source is largely irrelevant. Two "ideal" balun (balanced to unbalanced) transformers are used here to supply a transformation between differential and single-end signals for both input and output. Two AC sources can also be applied with opposite polarity here to achieve the same effect. Again, they will both be matched to 50 Ω at 866 MHz as in the singled-ended LNA design.

Another advantage of applying differential topology is its ability to reject common-mode disturbance. In mixed-

signal applications, both the supply and substrate voltages may be noisy. Hence, this attribute becomes particularly important.

However, for equal noise figure, the power consumption of this amplifier is twice that of its single-ended counterpart. Offsetting this disadvantage is the improved linearity that is attained by dividing the input voltage between two devices.

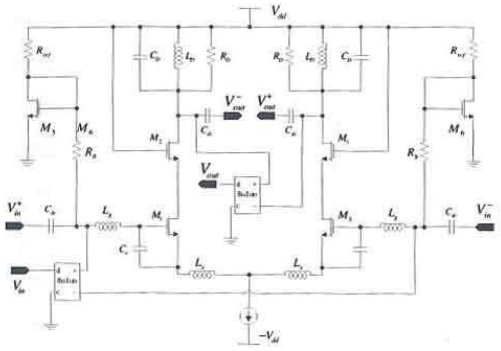


Fig. 4 The differential LNA topology

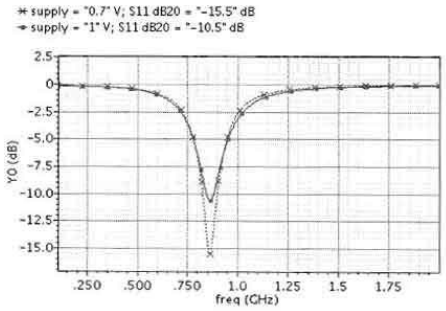
3 SIMULATION RESULTS

The results for the proposed 866 MHz UHF RFID LNA simulated using Cadence Spectre, Virtuoso and Assura are now discussed. The results of the singled-end telescopic LNA are shown in Fig. 5. With a supply of 0.7 V, at 866 MHz, the input reflection coefficient S_{11}=-15 dB, forward power gains S_{21} is around 16 dB, and noise figure is 1.2 dB. The power dissipation is only around 0.95 mW. The supply voltage can go down further to reduce power dissipation, but with a smaller gain, on the other and, a higher gain also results in more power consumption. Fig. 5 (a), (b) and (c) also demonstrate the S_{11}, S_{21} and noise figure behaviour under both 0.7 V and 1 V voltage supplies. Due to the PCSNIM technique, noise figure is minimized at resonance frequency at around 1.1 dB. This example proves how to optimize the trade-off between all those specifications in LNA designs. The IIP3 and the 1-dB compression point were determined using a two-tone test at 866 MHz with 1 MHz tone separation. The results indicate an IIP3 of -11.5 dBm and a 1dB compression point of -16.1dBm as shown in fig. 6.

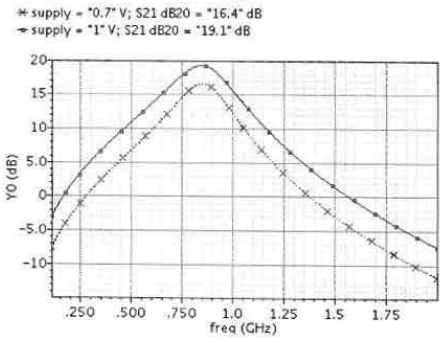
Fig. 7 shows the S_{11}, S_{21} and noise figure simulated results for folded cascode architecture as well as their different behaviours under different PMOS bias voltage from 0V to 0.1V. With this voltage control technique, most s-parameters maintain the similar results compared with single-end cascode topology. However, with 0.5 V supply voltage, the folded cascode LNA consumes 1.33 mV, which is slightly higher than singled-end architecture.

In order to maintain low noise figure as in single-ended telescopic cascode topology, the differential topology is duplicated symmetrically by two single-ended telescopic cascode LNA to give the same noise figure of 1.2 dB as shown in Fig.8 (b). The power consumption is also doubled but we can identify the improvement of 1 dB compression and IIP3 values of -9.1 dBm and -9.4 dBm compared with single-ended case with values of -16.1 dBm and -11.5 dBm respectively.

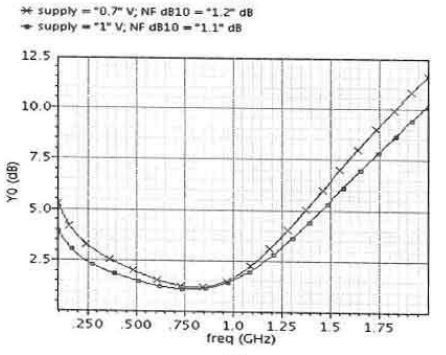
Completed specifications of all the proposed LNA designs are summarized in Table I. Table I compares the performance of the proposed UHF LNAs with other UHF LNA designs indicating very low NF achieved at sub-mW power dissipation.



(a)



(b)



(c)

Fig.5 Simulated S- parameter results of the singled-end LNA in Fig.2 with two different supply voltages: 0.7V and 1V (a) S_{11} (b) S_{21} and (c) NF

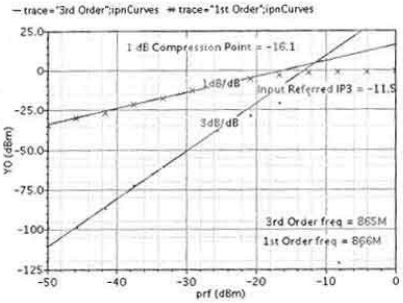
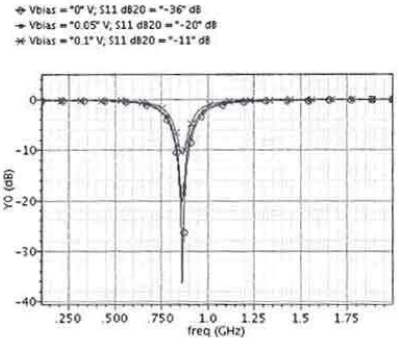
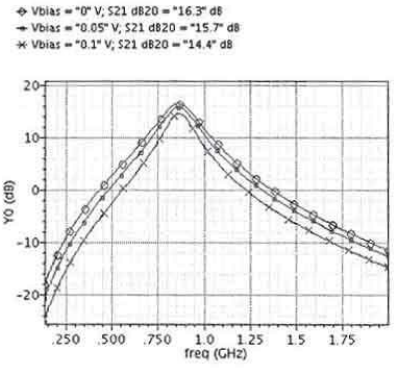


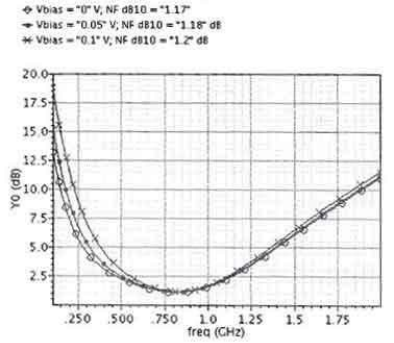
Fig.6 Simulated IIP3 and 1dB compression point results of the singled-end LNA in Fig.2



(a)

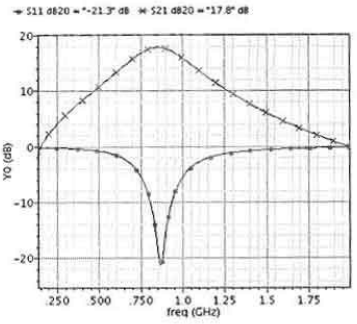


(b)

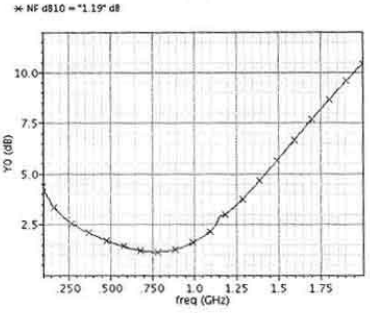


(c)

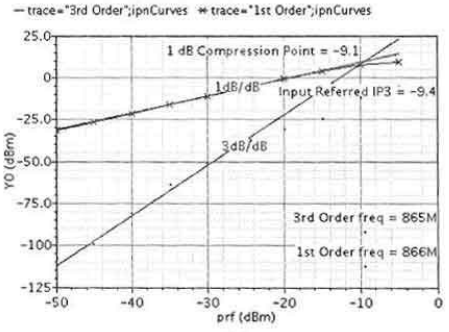
Fig.7 Simulated S-parameter results of the folded cascode LNA in Fig.3 with different PMOS bias voltage: 0V, 0.005V and 0.1V (a) S_{11} (b) S_{21} and (c) NF



(a)



(b)



(c)

Fig.8 Simulated S-parameter, noise figure, IIP3 and 1dB compression point results of the differential LNA in Fig.4 (a) S_{11} and S_{21} (b) NF and (c) IIP3 and 1dB compression point

4 CONCLUSIONS

The optimized UHF RFID LNA at 866 MHz has been designed and simulated results demonstrated. The design achieves very low NF of 1.2 dB with only power dissipation of 0.95 mW for singled-end, 1.33 mW for folded cascode and 2 mW for differential topologies respectively.

TABLE I

SUMMARY OF THE PERFORMANCE OF PRESENTED UHF RFID LNAS AND COMPARISON WITH PREVIOUS UHF LNA DESIGNS

	This Work			[2]	[4]	[5]	[6]	[7]	[9]	[10]	[12]	[13]
Process Technology (μm)	0.13			0.25	0.18	0.35	0.24	0.35	0.18	0.18	0.35	0.18
Topology	┤	╥	╫	╥	┤	┤	┤	┤	┤	┤	‖	╫
S11 (dB)	-16	-36	-21	-18	-12	-10	-38	-10	N/A	-29	-11	N/A
S21 (dB)	16.4	16.3	17.8	12	14	17.5	8.8	14	15.85	12.5	13.4	15
S12 (dB)	-39	-41	-42	N/A	N/A	N/A	N/A	-34	-51.3	-60	N/A	N/A
NF (dB)	1.20	1.18	1.19	1.35	2.3	2	1	1.05	0.9	0.7	3.2	2.9
IIP3 (dBm)	-11.5		-9.4	-4	-14	-6	7.1	0	-5.01	-4	10.8	N/A
P1dB (dBm)	-16.1		-9.1	-15	N/A	N/A	N/A	-12	-19.5	-9	1.4	-15
Power Dissipation (mW)	0.95	1.33	2.0	2	7.5	21.6	7.5	9	0.5	3.9	33	4.32
Supply Voltage (V)	0.7	0.5	0.7	1.25	1.8	2.7	2	1.8		1.8	3.0	1.8
Centre Frequency (MHz)	866			900	900	900	800	920	404	915	900	900

N/A: not available ┤: single-ended cascode topology ╥: folded-cascode topology ‖: common-gate topology ╫: differential topology

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8.7 Published Conference Paper III: Performance Analysis of Microstrip Line Matching Network for 866 MHz UHF LNA [215]

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Performance Analysis of Microstrip Line Matching Network for 866 MHz UHF LNA

Jie Li[1] and Rezaul Hasan[2]

Center for Research in Analog and VLSI Microsystems Design (CRAVE),
School of Engineering and Advanced Technology (SEAT)
Massey University, Albany, Auckland

Email: [1]J.Li.2@massey.ac.nz [2]S.M.Hasan@massey.ac.nz

Abstract: **This paper presents a method to design the matching networks by using single stub microstrip line for an UHF LNA that operates on 866 MHz. The superior performance characteristics of the Microstrip line make it one of the most important medium of transmission in microwave transistor amplifiers in both microwave integrated-circuit and PCB-circuit technology. The parallel-plate microstrip line configuration is primarily used for low impedance, high-power applications. MATLAB programming is used to obtain the Smith chart results for input and output Microstrip line matching networks. The LNA simulation result exhibits a voltage gain of 17 dB, drawing 1.8 mW power consumption from a 1V power supply.** .

Keywords: Microstrip Line, Impedance Matching, UHF, LNA, MATLAB

I. INTRODUCTION

Matching circuits analyse can be troublesome at microwave frequencies. Ideally, an optimum matching network is lossless, which in another word, the impedance seen into the matching network Z_0 is equivalent to the load Z_L to eliminate reflections, especially at tuning frequency. This arrows maximum power delivery and minimize the signal noise of the system. Conventional matching networks contain a number of lump elements. However, the influence of parasitic in those discrete elements becomes more noticeable when the frequency increases. Especially, inductors usually are avoided in such design since they tend to have higher resistive losses than capacitors. Alternatively, distributed components are widely been used when wavelength becomes significantly small comparing with the characteristic circuit component length. Among all transmission line technologies, microstrip line is widely applied. Fig. 1 demonstrates a traditional parallel-plate microstrip line. The conducting strips are etched on one side of the PCB, while the other side of the PCB is usually treated as ground plane to help preventing excessive field leakage. This structure reduces radiation loss [1]. The current and voltage flow is confined to two plates separated by a dielectric medium.

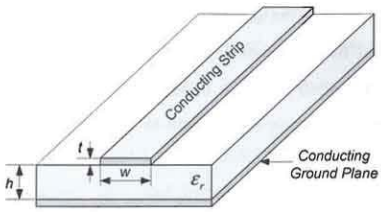

Fig. 1: Microstrip transmission line geometry

The shortcomings of this kind of single layered PCB are high radiation loss and interference between neighbouring conductors traces. Hence substrates with high dielectric constants ε_r is prefer for achieving high board density of the components layout since they minimize field leakage and cross coupling. Multilayer techniques are also widely used to achieve balanced circuit board design, with the increasing on cost and the higher complex of the fabrication process instead.

The Smith Chart, even was developed in early 20th century, has retained its popularity due to its easy and intui-

tive display of the reflection coefficient as well as the line impedance. The reading accuracy from the Smith Chart is sufficient for most practical microwave transistor amplifier design issue. Matching circuit design for amplifier can be easily and quickly approached by using the normalized impedance and admittance Smith Chart from computer-aided software [2, 3]. Furthermore, the Smith Chart is also used to present the frequency dependence of scattering parameters and other characteristics [4]. In this paper, a complete procedure of constructing an impedance matching network for an UHF LNA by using transmission microstrip line associate with the Smith Chart is approached.

II. SOME USEFUL EQUATIONS

[4-6] defines all the formulas and equations used in this paper. For the purposes of obtaining fast and generally reliable estimations of the line parameters, the thickness t of the conductor forming the line is assumed negligible compared to the substrate height h. In this case, the empirical formulas that depend only on the line dimensions (w and h) and the dielectric constant ε_r can be adopted. Depending on the ratio w and h, two separate regions applies.

For narrow strip lines, $w/h < 1$, the line impedance can be represented in [4-6]

$$Z_0 = \frac{Z_f}{2\pi\sqrt{\varepsilon_{eff}}} \ln\left(8\frac{h}{w} + \frac{w}{4h}\right)$$

where $Z_f = \sqrt{\mu_0/\varepsilon_0} = 376.8\Omega$ is the wave impedance in free space, and ε_{eff} is the effective dielectric constant that was given by

$$\varepsilon_{eff} = \frac{\varepsilon_r + 1}{2} + \frac{\varepsilon_r - 1}{2}\left[\left(1+12\frac{h}{w}\right)^{-1/2} + 0.04\left(1-\frac{w}{h}\right)^2\right]$$

while for a wide line when $w/h > 1$, Z_0 has:

$$Z_0 = \frac{Z_f}{\sqrt{\varepsilon_{eff}}\left[1.393 + \frac{w}{h} + \frac{2}{3}\ln\left(\frac{w}{h} + 1.444\right)\right]} \quad (1)$$

with $$\varepsilon_{eff} = \frac{\varepsilon_r + 1}{2} + \frac{\varepsilon_r - 1}{2}\left(1+12\frac{h}{w}\right)^{-1/2} \quad (2)$$

There is only a small discontinuity when w/h =1. For practical design purposes, w/h ratios that based on a given characteristic impedance Z_0 and dielectric constant ε_r of the substrate is approached as well. Assuming in an infinitely thin line conductor, this ratio can be written in a form of

$$\frac{w}{h} = \frac{8e^A}{e^{2A} - 2} \qquad \text{for } \frac{w}{h} \le 2 \quad (3)$$

$$\frac{w}{h} = \frac{2}{\pi}\left\{B - 1 - \ln(2B-1) + \frac{\varepsilon_r - 1}{2\varepsilon_r}\left[\ln(B-1) + 0.39 - \frac{0.61}{\varepsilon_r}\right]\right\}$$

$$\text{for } \frac{w}{h} \ge 2$$

where $$A = 2\pi\frac{Z_0}{Z_f}\sqrt{\frac{\varepsilon_r + 1}{2}} + \frac{\varepsilon_r - 1}{\varepsilon_r + 1}\left(0.23 + \frac{0.11}{\varepsilon_r}\right) \quad (4)$$

$$B = \frac{Z_f \pi}{2Z_0\sqrt{\varepsilon_r}}$$

The achieved effective dielectric can further evaluate the phase velocity, wavelength and the related wave number to the phase velocity of the microstrip line in following expressions:

$$v_p = \frac{1}{\sqrt{\mu\varepsilon}} = \frac{1}{\sqrt{\mu_0\varepsilon_0\varepsilon_{eff}}} = \frac{c}{\sqrt{\varepsilon_{eff}}} \quad (5)$$

$$\lambda = \frac{v_p}{f} = \frac{c}{f\sqrt{\varepsilon_{eff}}} = \frac{\lambda_0}{\sqrt{\varepsilon_{eff}}} \quad (6)$$

$$\beta = \frac{2\pi}{\lambda} = \frac{2\pi f}{v_p} \quad (7)$$

where c is the speed of light.

III. MATCHING NETWORK IMPLEMENTATION

A generic LNA matching network configuration is shown in Fig. 2. Input and output matching networks are needed to reduce undesired reflections to improve the power capabilities. In this work, matching networks are designed for a prefabricated CMOS cascode LNA [7] with known VSWR, measured input power reflection S_{11} and output power reflection S_{22} as shown in Table I. A matching network that consists of a series microstrip transmission line connected to a parallel open-circuit or short circuit stub is used for standard port impedance matching (50Ω) [5]. Four adjustable parameters are counts to consider or calculate in this case: length l_S and characteristic impedance Z_{0S} of the stub (either open- or short-), and length l_T and characteristic impedance Z_{0T} of the series transmission line segment.

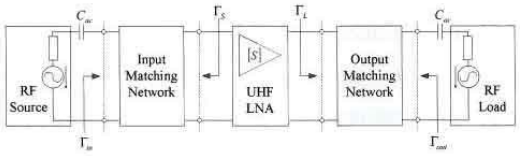

Fig. 2: Generic LNA with matching network.

TABLE I: Typical parameters of a pre-fabricated LNA and its expected result at 866 MHz, V_{dc} =1V, $Z_0 = 50\Omega$

Operating Frequency (MHz)	866
Noise Figure (dB)	2
VSWR	1.5
Measured input power reflection S_{11}	0.6886 - j0.4774
Measured output power reflection S_{22}	0.82526 + j0.289
Assumed reverse isolation S_{12}	≈0
Expected Power gain S_{12}	>15dB

In order to achieve maximum unilateral transducer gain, where signal flows only in one direction, we make the assumption of reverse isolation S_{12} approaching 0. From the defining equation for S-parameters [8], the source and load reflection coefficient towards the LNA needs to become the complex conjugate of S_{11} and S_{22}. The matching procedure can be quite confusing without a very clear train of thought. The general method used in matching circuit is to choose either "toward the load" or "toward the generator" on Smith chart depending on the output or input matching network respectively. The source reflection coefficient needs to take the conjugate of S_{11} while the load reflection coefficient doesn't [9]. Transformation under conditions brings up the error. The method used in this paper follows a unified procedure that can be adopted in both input and output matching network. Take both source and load reflection coefficient looking from the amplifier back toward the input or output line, which is the complex conjugate of S_{11} and S_{22}. Only one direction "toward to the load" from the reflection coefficient points on the Smith chart need to focus.

Therefore, the source reflection coefficient can be represented as $\Gamma_S = S_{11}^* = 0.6886 + j0.4774$ for an input matching, or $S_{11}^* \approx 0.8379\angle +34.73°$ in angular format. Similarly, the load reflection coefficient is $\Gamma_L = S_{22}^* = 0.82526 - j0.289$ for output matching, or represented in angular form as $0.87445\angle -19.308°$. Converting into impedance format can be easily approached. Hence source impedance format now can be calculated as $Z_S \approx 45.9 + j147$, or $z_S = 0.918 + j2.94$ in normalized format, and load impedance $Z_L \approx 103 - j253$, or $z_L = 2.06 - j5.06$ in normalized format. In order to better understand and utilize the use of Smith Chart, one more transformed representation step is approached to find the normalized admittances, that can be expressed as $y_S = 0.0968 - j0.3099$ and $y_L = 0.0690 + j0.1695$.

Input Matching Network

The basic concept for input impedance matching is to select the length l_S of the stub such that it produces a susceptance B_S sufficient to move the normalized input admittance $y_{in} = 1$ (or $z_{in} = 1$) to SWR circle that passes through the normalized source impedance point $z_S = 0.918 + j2.94$, as shown in Fig. 3.

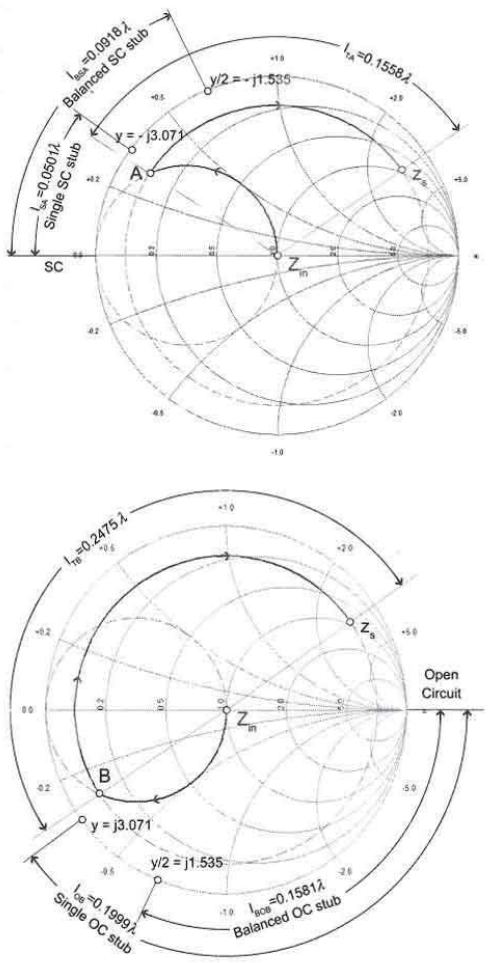

Fig. 3: Analysis of two possible (a) short-circuit single-stub and (b) open-circuit single-stub matching networks for input matching system.

To start with input impedance matching in Fig. 2, the source impedance point $z_S = 0.918 + j2.94$ is located in Smith Chart first. It can be identified in the Smith Chart as the intersection of the circle has radius 0.8379 with angular -34.73° shown as point z_S in Fig. 3. It is noticeable that the source SWR circle associated with $z_S = 0.918 - j2.94$ intersects the constant conductance circle g=1 in two points (at $y_A = 1 - j3.071$ and at $y_B = 1 + j3.071$) suggesting two possible solutions. The corresponding susceptance values for the stub are $jb_A = y_A - y_{in} = -j3.071$ and $jb_B = y_B - y_{in} = j3.071$, respectively. In the first case, the length of an short-circuit stub can be found in the Smith Chart by measuring the length l_{SA}, starting from the $\Gamma_0 = -1$ point on the real axis (short circuit), and moving along the outer perimeter of the Smith Chart g=0 toward the generator (clockwise) to the point where $y = -j3.071$. The length in this case is $l_{SA} = 0.0501\lambda$. The short-circuit stub can be replaced by an open-circuit stub if its length is increased by a quarter wavelength $l_{OA} = 0.3001\lambda$. The can be also proved from the formula $\frac{\lambda}{2\pi}[tan^{-1}(-3.071) + \pi] = 0.3001\lambda$.

This substitution may become necessary in printed circuit design, open-circuit subs are sometimes preferred because they eliminate the deployment of a via, which is otherwise necessary to obtain the ground connection for a short-circuit stub. This through-hole connection in printed circuit boards will result additional parasitic inductances. However, at high frequencies, it is very difficult to maintain perfect open-circuit (as well as short-circuit) conditions because of changing temperatures, humidity, and other parameters of the medium surrounding the open transmission line. Moreover, in order to minimize the circuit layout area, the first priority is to select the shortest line segments.

Studying from the open-circuit as shown in Fig. 3(b), very similar to the first solution, $jb_B = j3.071$ yields the length $l_{OB} = 0.1999\lambda$ for the open-circuit stub, and $l_{SB} = 0.4499\lambda$ for the short-circuit stub. In this case, creating an open-circuit stub requires a shorter length than a short-circuit stub.

The length of the series transmission line segment can be approached by the phase rotation along the SWR circle from either point A or B on the Smith Chart "toward generator" to the Z_S (or sometime it's preferable to say from Z_S "toward load" to either point A or B on the Smith Chart). It is easy to get both transmission line segment length $l_{TA} = (0.2018 - 0.0460) = 0.1558\lambda$ and $l_{TB} = (0.2018 + 0.0460) = 0.2478\lambda$ respectively.

Output Matching Network

To approach the output impedance matching network shown in Fig. 2, similarly locating $z_L = 2.06 - j5.06$ in the Smith Chart as shown in Fig. 4. Two intersect point C and D are also detect from the corresponded load SWR circle and the constant conductance circle g=1. The corresponding susceptance values for the stub are $y_C \approx 1 - j3.58$ and $y_C \approx 1 + j3.58$. The corresponding length of the short-circuit stub and open-circuit stub are found in the same way as $l_{SC} = 0.0432\lambda$, $l_{SD} = 0.4569\lambda$ and $l_{OC} = 0.2931\lambda$, $l_{SC} = 0.2069\lambda$ respectively. The shortest length of the series microstrip transmission line segment plus stub is obtained by using a short-circuit shunt stub. The length of two series transmission line segments are found by moving from point C and C on the Smith Chart "toward generator" to the z_L as $l_{TA} = 0.2365\lambda$ and $l_{TC} = 0.31718\lambda$.

Single stub to Balanced stub Network

To minimize the transmission interaction between shunt stub and transmission line segment, the shunt stub must be balanced along the transmission line. For this, admittance of each side of balanced shunt stub must be equal to half of the total admittance.

For input matching network, admittance of each side of balance stub will be equal to $\pm j3.071/2 = \pm j1.5355$. Using the Smith Chart in Fig. 3, the length of each side of stub $l_{BSA} = 0.0918\lambda$ for balanced short-circuit stub from point A and $l_{BOB} = 0.1581\lambda$ for balanced open-circuit stub from point B. It is noticeable that the length for balanced open-circuit stub is reduced from the single open-circuit stub instead of increasing in short-circuit stub situation. Similar approaching is processed for output matching network in Fig. 4., admittance value $\pm j3.58/2 = \pm j1.79$ of each side of balance stub lead to the length of each side of stub $l_{BSC} = 0.0806\lambda$ for balanced short-circuit stub from point C and $l_{BOD} = 0.1693\lambda$ for balanced open-circuit stub from point D.

The complete LNA matching schematic diagram is shown in Fig. 5 and Fig. 6 for single and balanced stub.

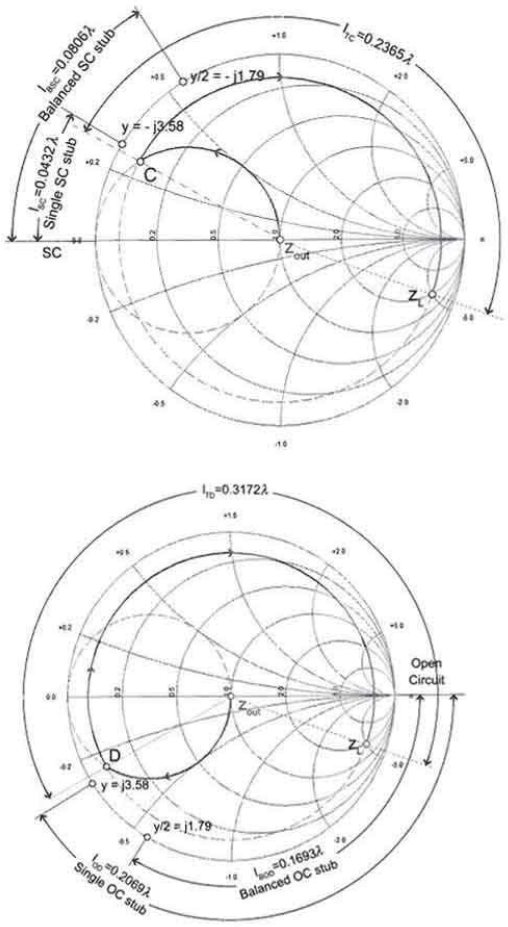

Fig. 4: Analysis of two possible (a) short-circuit single-stub and (b) open-circuit single-stub matching networks for output matching system.

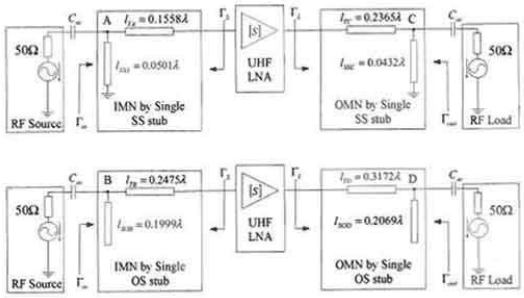

Fig. 5: Complete LNA matching schematic using single short-circuit and open-circuit stub

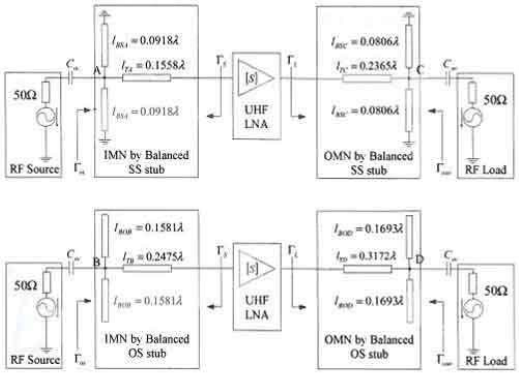

Fig. 6: Complete LNA matching schematic using balanced short-circuit and open-circuit stub

IV. RESULT

MATLAB is used to confirm the matching network. The code in section VI demonstrates one example for both input and output matching by using single open-circuit microstrip transmission line stubs. The MATLAB simulated Z_{in} and Z_{out} values after the matching networks are very close to the desired Z_S and Z_L values as shown at the bottom of the code. Fig. 3 and Fig. 4 are the output figures after running the MATLAB codes.

Here a 50 Ω characteristic Microstrip line is desired to construct for this research. The relative dielectric constant ε_r and the board height w are provided by FR4 PCB foundry in an approximated value of 4.6 and 1.45mm, respectively [6]. For a wide line, $w/h > 1$, a value of 3.4575 is obtained for the effective dielectric constant from (2). The more precise computed value of the characteristic impedance is 50.2243 Ω from (1). Therefore, by choosing the case where w/h ≤2 from (3) and (4), a value of 1.5583 and 1.8477 is calculated for A and w/h ration. Using the obtained ratio of w/h , the trace width equals to 2.698mm. From equations (5-7), the corresponding phase velocity, wave length and related wave number can be found as 1.61×10^8m/s, 0.1859m and 33.7965 m^{-1}, respectively. The value of λ /10 is less than 20 cm, which is comparable with typical circuit component dimensions. Fig. 7 shows one example of input / output impedance matching network by using single open-circuit stub from figure 8 (b).

Fig. 8 shows the s-parameter results of this impedance matching network from Fig. 7 by using TDR calibration of S-parameters. With a power supply of 1V and 50 Ω port resistor, at turning frequency, the input reflection coefficient S_{11} gives a value around -30 dB; the forward power gain S_{21} is around 17 dB. The power dissipation is approximate 1.8 mW with 1.8 mA drain current through the LNA transistor. Measured S-parameter values in line with our expected results, proves that the impedance matching method used here is appropriate.

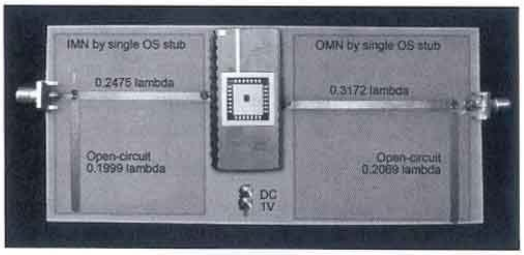

Fig. 7: Impedance matching network by both using single open-circuit microstrip transmission line stubs

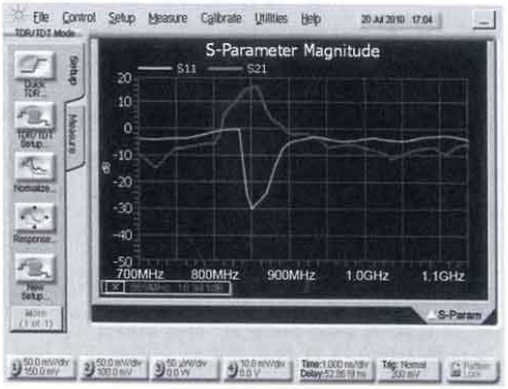

Fig. 8: S-Parameters for microstrip transmission line impedance matching network in Fig. 7

V. CONCLUSION

Input and output matching networks are designed for an UHF RFID LNA that operates on 866 MHz using the Smith Chart through MATLAB programming. In this design, the unilateral transducer gain reaches around 17 dB with -30 dB input reflection coefficient at the turning frequency. Presentation of the results show the Smith Chart impedance matching theory and practice implementation is correct and feasible for UHF LNA.

VI. SAMPLE CODE

```
global Z0;
set_Z0(50);
f=866e6;
%define desired input and output impedances
Zin=Zout=50;
%define source and load impedances
ZL=103+j*253
ZS=45.9-j*147
%create smith chart, SWR circle and G=1 circle
sm=smith_chart;
const_SWR_circle(ZL,'m--');
const_SWR_circle(ZS,'m--');
const_G_circle(real(1/Zout),'m--');
const_G_circle(real(1/Zin)
global rf_Network;
init_network;
%achieved length values for transmission line l_B & l_D
l_TB=0.2478;
l_TD=0.31718;
%achieved length value for open-circuit stub l_B & l_D
l_OB=0.1999;
l_OD=0.20690;
% locates desired input and output impedances values
Add_shunt_impedance(Zout);
Add_shunt_impedance(Zin);
%add open-circuit stub for input and output networks
Add_shunt_oc_stub(360*l_OB,f,Z0)
Add_shunt_oc_stub(360*l_OD,f,Z0);
%add transmission line stub for input and output net-
works
Add_trans_line(360*l_TB,f,Z0);
Add_trans_line(360*l_TD,f,Z0);
%input and output impedances value after matching
network
Zin_A=rf_imp_transform(f,sm)
Zout_A=rf_imp_transform(f,sm)
```

Calculated input and output impedances value after running above matching networks in MATLAB:

```
ZS = 4.5900E+001 -1.4700E+002I
ZIN_A = 4.6011E+001 +1.4725E+002I
ZL = 1.0300E+002 +2.5300E+002I
ZOUT_A =  1.0303E+002 -2.5303E+002I
```

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