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On the g_m-Boosted Miller-Effect Minimized Inverter-Cascode Transimpedance Amplifier for Sensor Applications

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ABSTRACT This paper presents the small-signal operation of a g_m-boosted inverter-cascode transimpedance amplifier which has not been reported previously and whose comprehensive analysis is not available in any reported article or text-book. A simplified sequential equivalent-circuit method is employed which eliminates the need for complicated circuit analysis techniques. The analysis shows that the gain and the gain-bandwidth of the g_m-boosted inverter-cascode transimpedance-amplifier is enhanced by the gain of the g_m-boosting amplifier. This is due to the increased output impedance of the TIA, and, the reduced input-referred miller-effect capacitance through miller-effect trade-off employing the g_m-boosting loop. To verify the actual performance improvement achieved, circuit simulation results as well as measured experimental results are also provided.

INDEX TERMS Analog CMOS circuits, g_m-boosting, inverter-cascode transimpedance amplifier, small-signal analysis, simplified inspection-based analysis technique.

I. INTRODUCTION

Transimpedance amplifiers (TIAs) are today one of the most crucial front-end analog conditioning circuits particularly for meeting the challenging current-sensing specifications in electronic systems, sensor and biomedical applications with nano- and pico-ampere sensed currents. This is in addition to the well-established traditional broad-band fibre-optic storage and optical transceiver applications which employ inductive bandwidth enhancements. Many TIA designs in sensor and biomedical application require very high gain along-with low-bandwidth due to the slowly varying signals in such applications. Comparative reviews of many possible TIA topologies have been discussed by authors in [1], [2]. Nano-pore DNA analysis [3], [4] using solid-state nanopore (diameter $\leq$ 30nm) requires TIAs with very high gain and low bandwidth. When a single DNA molecule passes through the nanopore, the individual nucleotide bases are identified by the variation of the current through the nanopore due to the particular base (an A, a C, a G or a T) passing through the nanopore, which is sensed by the TIA. The change in the current through the nanopore thus constitutes the DNA sequence.

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In addition, the front-ends of many other slowly-varying transducer applications such as radiation sensor [5] and pressure sensor [6] mostly require high gain TIAs. One well-known technique to enhance the gain of amplifiers is by employing g_m-boosted cascoding devices. The g_m-boosting technique has been employed in many analog building blocks such as transconductance-amplifiers [7], RF-frontend LNA [8], RF mixers [9] and so forth. The 2nd author recently reported numerous g_m-boosted cascode structures [10] as well as a g_m-boosted source follower structure [11]. However, the employment of g_m-boosting in TIA designs have still not been fully explored as evident from the comparative studies in [1], [2]. TIAs being a sub-topic in feed-back amplifier design it has also not been discussed in detail in the available popular analog CMOS text-books [12]–[16] and other avenues. Improvement of the intrinsic-gain, output-impedance and band-width through g_m-boosting can further enhance the performance of TIAs. The inverter-cascode TIA is an well-known TIA topology for high-gain biomedical applications. In this context, the implementation and comprehensive small-signal mid-band characteristics of a g_m-boosted inverter-cascode TIA is investigated in this work. The complete circuit analysis of a g_m-boosted inverter-cascode TIA has not been reported before. Like several recent

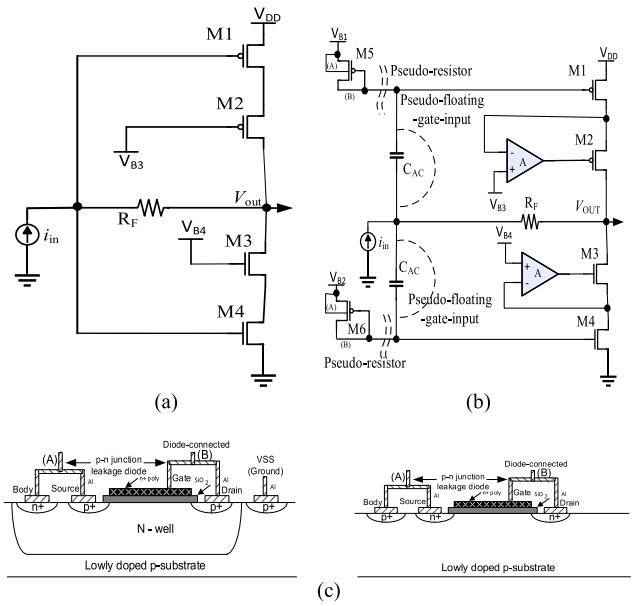

FIGURE 1. (a) An inverter-cascode TIA with resistor feed-back biasing, (b) a g_m-boosted inverter-cascode TIA with resistor feed-back and pseudo-floating-gate biasing options, and (c) cross-sections of diode-connected devices as p-n junction leakage-diodes (high resistance pseudo-resistors), PMOS leakage-diode (on the left) and NMOS leakage-diode (on the right).

articles by the 2nd author, complete mid-band derivations of the g_m-boosted inverter-cascode TIA is developed using a simplified inspection technique [10] which was not reported before. Elementary circuit transformations [17] along with suitable use of Norton amplifier model [18] is employed for a ''pictorial'' transformation based mid-band gain expression derivation. In order to provide a verification of the design improvements achieved by the g_m-boosting, comparison with the ordinary inverter-cascode TIA is also provided through circuit simulations and experimental results. Standard integrated circuit symbols [12], [13], [15], [16] have been utilized for all the MOSFET device parameters in the small-signal analysis following the general convention for microelectronic circuit analysis. As a note on using clearly-defined composite current/voltage notations in the derivations, it is to be mentioned that, all the voltages and currents in lower-case alphabets along-with upper-case subscripts are quantities that have both a large-signal DC-bias along-with a small-signal (AC) variation superimposed on it. Also, all the upper-case voltage/current notations along-with upper-case subscripts are large-signal DC quantities. And, finally, all the lower-case voltage/current symbols along-with lower-case subscripts are AC values.

II. TRANS-CONDUCTANCE-BOOSTED INVERTER-CASCODE TRANSIMPEDANCE AMPLIFIER AND ITS ANALYSIS

The topology of the standard inverter-cascode TIA with resistor-feedback biasing is shown in the Fig. 1(a) where cascoding is employed to reduce the input referred miller capacitance for the TIA. Next, the Fig. 1(b) shows the circuit topology of the proposed g_m-boosted inverter-cascode TIA with both resistor feed-back and Quasi-floating-gate (QFG) [19], [20] biasing options. Here AC coupling can be employed at the input in the form of Quasi-floating-gate inputs for separating the DC-bias circuits for the PMOS and the NMOS inverter sections. This is done in order to maintain higher overdrive dynamic range for these inverter devices to operate in saturation and achieve linear small-signal current-to-voltage transimpedance gain. The bias voltages for the PMOS and NMOS input devices are provided by diode-connected PMOS pseudo-resistors. Here PMOS and NMOS cascoding devices are connected in a negative-feedback loop employing differential amplifiers with gain ''A''. The g_m-boosting differential-amplifier is assumed to have high input-impedance (similar to that of an ideal operational amplifier [17]) so that there is negligible current flowing into its terminals at mid-band frequencies. The gates of the cascoding devices M2 and M3 are biased by the DC level at the output of the g_m-boosting differential amplifiers. Fig. 1(c) shows the cross-sections of diode-connected CMOS devices as p-n junction leakage-diodes (pseudo-resistors) with PMOS leakage-diode (on the left) and NMOS leakage-diode (on the right), where, a p-n junction leakage-diode provides a high resistance path. Alternatively, resistor-feedback biasing can also be provided by shorting the AC coupling capacitors and opening the pseudo-resistors. Fig. 2(a) shows the AC equivalent circuit of the open-loop TIA for determining the open-loop gain (with loading effect), the loop-gain and the closed-loop transimpedance gain. This AC-equivalent circuit is co-incident for both the biasing options as the resistance at the input is dominated by the feed-back resistor R_F with the pseudo-resistor having a very high resistance value in the range of several Mega-ohms. This circuit is obtained by using a 2-port Y-model for the feed-back return-path [13] so that the admittance parameters are $Y_{11} = 1/R_F$ and $Y_{22} = 1/R_F$ for the open-loop feed-forward TIA. Also, the feed-back factor, β is given by the admittance parameter, $Y_{21} = 1/R_F$. A simplified form of this open-loop AC equivalent circuit is shown in the Fig. 2(b) which is essentially a shunt combination of the NMOS and the PMOS inverter sections of the g_m-boosted inverter-cascode TIA. The values of the resistances $1/g_{m5}$ and $1/g_{m6}$ are very high due to the very small leakage-current flowing through the diode-connected pseudo-resistors, and, as a consequence the overall resistance across the current-source input is dominated by R_F. Fig. 2(c) depicts the small-signal equivalent circuit of the g_m-boosted NMOS half (section) of the TIA, while, Fig. 2(d) shows its output shorted equivalent circuit for finding the G_m of the Norton Amplifier model [18] of this half. It is easily observed now that $-g_{m3}(A+1)v_y$ and $g_{mb3}v_{b1s1}$ are two current-sources due the same voltage $(0\text{-}v_y)$ across them (with voltages at b3 and s3 being zero and v_y, respectively). Hence, they are reduced to two conductors of values $g_{m3}(A+1)$ and g_{mb3}, respectively. In the next diagram in Fig. 2(e) the 3 resistors are combined in parallel and the Norton source

is converted into a Thevenin's equivalent source. From the simplified equivalent circuit of the Fig. 2(e) simple ohm's law shows that,

$$i_{out} = -\frac{g_{m4} v_{in} r_{o4}}{r_{o4} + \frac{1}{(A+1)g_{m3}} \parallel \frac{1}{g_{mb3}} \parallel r_{o3}} \tag{1}$$

Simplifying

$$i_{out} = -\frac{g_{m4} v_{in} r_{o4}}{r_{o4} + \frac{1}{(A+1)g_{m3} + g_{mb3} + \frac{1}{r_{o3}}}} \tag{2}$$

$$= -\frac{g_{m4} v_{in} r_{o4} \left[(A+1)g_{m3} + g_{mb3} + \frac{1}{r_{o3}}\right]}{r_{o4}\left[(A+1)g_{m3} + g_{mb3} + \frac{1}{r_{o3}}\right] + 1} \tag{3}$$

$$= -\frac{g_{m4} v_{in} r_{o4} [\{(A+1)g_{m3} + g_{mb3}\} r_{o3} + 1]}{r_{o4} + r_{o4}[(A+1)g_{m3} + g_{mb3}] r_{o3} + r_{o3}} \tag{4}$$

Changing sides and rationalizing,

$$G_{m1} = \frac{i_{out}}{v_{in}} = -\frac{g_{m4} r_{o4} [\{(A+1)g_{m3} + g_{mb3}\} r_{o3} + 1]}{r_{o4} + r_{o4}[(A+1)g_{m3} + g_{mb3}] r_{o3} + r_{o3}} \tag{5}$$

Next Fig. 2(f) shows the input shorted equivalent circuit of the NMOS section for finding the R_{out1} of the Norton amplifier model. Following-on Fig. 2(g) shows the successive simplification of the equivalent circuit in Fig. 2(f) by first merging the two current sources and then converting the Norton's source into the Thevenin's equivalent voltage source. Using KVL in the final equivalent circuit in the right-hand-side circuit of Fig. 2(g),

$$v_{out} = v_y + v_y [(A+1)g_{m3} + g_{mb3}] r_{o3} + \frac{v_y}{r_{o4}} r_{o3} \tag{6}$$

So that,

$$R_{out1} = \frac{v_y + v_y [(A+1)g_{m3} + g_{mb3}] r_{o3} + \frac{v_y}{r_{o4}} r_{o3}}{\frac{v_y}{r_{o4}}} \tag{7}$$

And in the final form,

$$R_{out1} = r_{o4} + r_{o4}[(A+1)g_{m3} + g_{mb3}] r_{o3} + r_{o3} \tag{8}$$

Similarly, applying the same small-signal analysis procedures to the PMOS cascode section (M1 and M2), the composite trans-conductance is given by,

$$G_{m2} = -\frac{g_{m1} r_{o1} [\{(A+1)g_{m2} + g_{mb2}\} r_{o2} + 1]}{r_{o1} + r_{o1}[(A+1)g_{m2} + g_{mb2}] r_{o2} + r_{o2}} \tag{9}$$

Also, the output impedance of the PMOS cascode section is given by,

$$R_{out2} = r_{o1} + r_{o1}[(A+1)g_{m2} + g_{mb2}] r_{o2} + r_{o2} \tag{10}$$

Next, Fig. 3 shows the final open-loop small-signal AC equivalent circuit of the g_m-boosted inverter-cascode TIA. From the input side of this equivalent circuit, the input voltage v_{in} imposing at the gates of M1 and M4 is equal to the product of the composite resistance and the current i_{in} at the input so that,

$$v_{in} = i_{in} \frac{1}{g_{m5} + g_{m6} + \frac{1}{R_F}} \tag{11}$$

Since g_{m5} and g_{m6} is very small compared to $1/R_F$,

$$v_{in} = i_{in} R_F \tag{12}$$

From the output side of the equivalent circuit, the trans-conductance current sources $G_{m1} v_{in}$ and $G_{m2} v_{in}$ can be merged into one, so that the output voltage v_{out} is given by,

$$v_{out} = v_{in}(G_{m1} + G_{m2})(R_{out1} \parallel R_{out2} \parallel R_F) \tag{13}$$

Applying (12) into (13), the open-loop transimpedance gain is given by,

$$Z_{TIA}^{open-loop} = \frac{v_{out}}{i_{in}} = R_F(G_{m1} + G_{m2})(R_{out1} \parallel R_{out2} \parallel R_F) \tag{14}$$

And, finally the closed loop trans-impedance gain is given by,

$$Z_{TIA}^{closed-loop} = \frac{Z_{TIA}^{open-loop}}{1 + \beta Z_{TIA}^{open-loop}} \tag{15}$$

$$Z_{TIA}^{closed-loop} = \frac{R_F(G_{m1} + G_{m2})(R_{out1} \parallel R_{out2} \parallel R_F)}{1 + (G_{m1} + G_{m2})(R_{out1} \parallel R_{out2} \parallel R_F)} \tag{16}$$

With variation in the g_m-boosting gain "A" G_{m1} and G_{m2} essentially remains equal to respectively, g_{m4} and g_{m1}. However, with increasing g_m-boosting gain "A" the output impedances R_{out1} and R_{out2} increases so that the overall output impedance ($R_{out1} \parallel R_{out2} \parallel R_F$) increases and approaches R_F gradually with R_F being much smaller than the g_m-boosted output impedances R_{out1} and R_{out2}. The overall transimpedance gain of the g_m-boosted inverter-cascode TIA thus increases with the g_m-boosting gain "A".

A. MILLER-CAPACITANCE SUPPRESSION WITH g_m-BOOSTING

The input impedance looking towards the source of M3 ($R_{in\_S\_M3}$) can be determined using the Fig. 2(i) where,

$$v_x = -v_x [(A+1)g_{m3} + g_{mb3}] r_{o3} + i_x . r_{o3} + i_x [\frac{R_F . R_{out2}}{(R_F + R_{out2})}] \tag{17}$$

Since R_F is much smaller than the g_m-boosted R_{out2}, we can write from (17),

$$R_{in\_S\_M3} = \frac{v_x}{i_x} = \frac{r_{o3} + R_F}{1 + [(A+1)g_{m3} + g_{mb3}] r_{o3}} \tag{18}$$

Similarly, the input impedance looking towards the source of M2 ($R_{in\_S\_M2}$) is given by,

$$R_{in\_S\_M2} = \frac{r_{o2} + R_F}{1 + [(A+1)g_{m2} + g_{mb2}] r_{o2}} \tag{19}$$

Hence, the total miller capacitance at the input is given by,

$$C_{miller\_input} = C_{gd\_M1}\left[1 + g_{m1}\frac{(r_{o2} + R_F)}{1 + [(A+1)g_{m2} + g_{mb2}] r_{o2}}\right] + C_{gd\_M4}\left[1 + g_{m4}\frac{(r_{o3} + R_F)}{1 + [(A+1)g_{m3} + g_{mb3}] r_{o3}}\right] \tag{20}$$

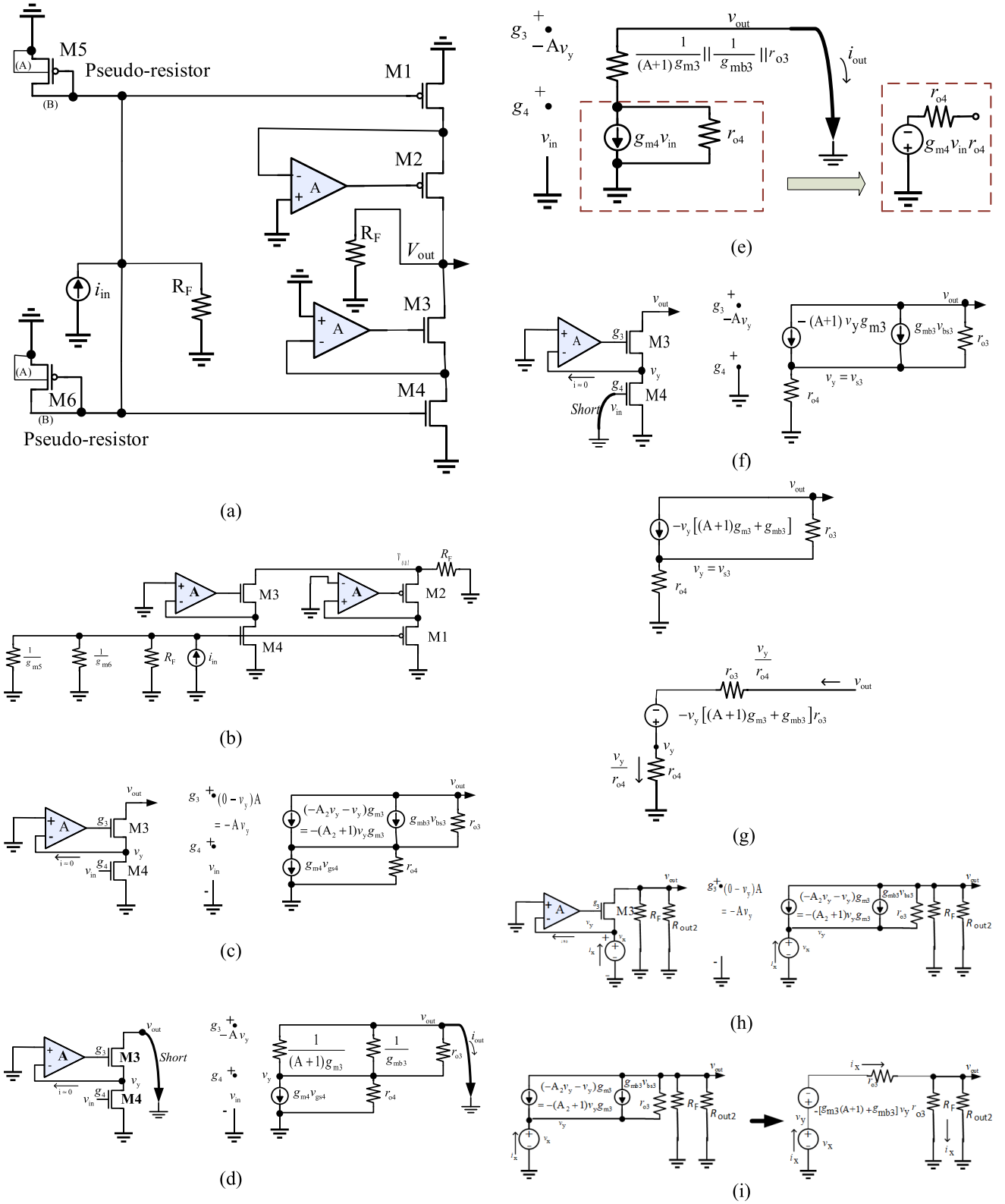

FIGURE 2. (a) The open-loop AC equivalent circuit of the g_m-boosted inverter-cascode TIA for determining the open-loop transimpedance gain, the loop-gain and the closed-loop transimpedance gain, (b) a simplified form of the open-loop AC equivalent circuit, (c) small-signal equivalent circuit of the NMOS half (section), (d) output shorted equivalent circuit for finding G_m employing conversion of current sources to resistors, (e) simplified equivalent circuit of the circuit in (d) combining the three resistors and converting the Norton's source to Thevenin's source, (f) input-shorted equivalent circuit of the NMOS section for finding the R_{out} of the Norton amplifier model, (g) successive simplification of the equivalent circuit in (f) by first merging the two current sources and then converting the Norton's source into the Thevenin's equivalent voltage source, (h) AC-equivalent circuit and small-signal model for determining the impedance looking into the source of M3, and (i) Norton's to Thevenin's transformation to obtain the final equivalent circuit for determining the impedance looking into the source of M3.

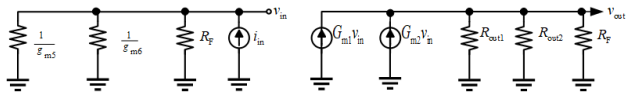

FIGURE 3. The final open-loop small-signal AC equivalent circuit of the g_m-boosted inverter-cascode TIA.

The miller capacitance at the drain of M1 is given by,

$$C_{\text{miller\_drain\_M1}} = C_{\text{gd\_M1}}\left[1+\frac{1+[(\text{A}+1)g_{\text{m2}}+g_{\text{mb2}}]\,r_{\text{o2}}}{g_{\text{m1}}.(r_{\text{o2}}+R_{\text{F}})}\right] \tag{21}$$

And, similarly the miller capacitance at the drain of M4 is given by,

$$C_{\text{miller\_drain\_M4}} = C_{\text{gd\_M4}}\left[1+\frac{1+[(\text{A}+1)g_{\text{m3}}+g_{\text{mb3}}]\,r_{\text{o3}}}{g_{\text{m4}}.(r_{\text{o3}}+R_{F})}\right] \tag{22}$$

The total capacitance at the input of the TIA is then given by,

$$\begin{aligned} C_{\text{tot\_input}} &= C_{\text{PD(sensor)}} + C_{\text{gs\_M1}} + C_{\text{gs\_M4}} + C_{\text{gs\_M5}} \\ &\quad + C_{\text{gs\_M6}} + C_{\text{db\_M5}} + C_{\text{db\_M6}} \\ &\quad + C_{\text{gd\_M1}}\left[1 + g_{\text{m1}}\frac{(r_{\text{o2}}+R_{\text{F}})}{1+[(\text{A}+1)g_{\text{m2}}+g_{\text{mb2}}]\,r_{\text{o2}}}\right] \\ &\quad + C_{\text{gd\_M4}}\left[1 + g_{\text{m4}}\frac{(r_{\text{o3}}+R_{\text{F}})}{1+[(\text{A}+1)g_{\text{m3}}+g_{\text{mb3}}]\,r_{\text{o3}}}\right] \end{aligned} \tag{23}$$

Then the time-constant at the input, τ_{input} is given by,

$$\tau_{\text{input}} = R_{\text{F}}C_{\text{tot\_input}} \tag{24}$$

Inspecting (23) it is clearly evident that the time-constant at the input reduces with increasing g_m-boosting gain "A" thus enhancing the bandwidth.

Next, the total capacitance at the drain of M1,

$$\begin{aligned} C_{\text{tot\_drain\_M1}} &= C_{\text{db\_M1}} + C_{\text{sb\_M2}} + C_{\text{gs\_M2}}(A+1) \\ &\quad + C_{\text{gd\_M1}}\left[1+\frac{1+[(\text{A}+1)g_{\text{m2}}+g_{\text{mb2}}]\,r_{\text{o2}}}{g_{\text{m1}}.(r_{\text{o2}}+R_{\text{F}})}\right] \end{aligned} \tag{25}$$

Then the time-constant at the drain of M1, $\tau_{\text{drain\_M1}}$ is given by,

$$\begin{aligned} \tau_{\text{drain\_M1}} &= \frac{r_{\text{o2}}+R_{\text{F}}}{1+[(\text{A}+1)g_{\text{m2}}+g_{\text{mb2}}]\,r_{\text{o2}}} \\ &\quad \times\left[\begin{array}{l} C_{\text{db\_M1}} + C_{\text{sb\_M2}} + C_{\text{gs\_M2}}(A+1) \\ +C_{\text{gd\_M1}}\left[1+\frac{1+[(\text{A}+1)g_{\text{m2}}+g_{\text{mb2}}]r_{\text{o2}}}{g_{\text{m1}}.(r_{\text{o2}}+R_{\text{F}})}\right] \end{array}\right] \end{aligned} \tag{26}$$

Simplifying (26)

$$\begin{aligned} \tau_{\text{drain\_M1}} &= \frac{C_{\text{db\_M1}}+C_{\text{sb\_M2}}}{[(\text{A}+1)g_{\text{m2}}]} + \frac{C_{\text{gs\_M2}}}{g_{\text{m2}}} \\ &\quad + \frac{C_{\text{gd\_M1}}}{[(\text{A}+1)g_{\text{m2}}]} + \frac{C_{\text{gd\_M1}}}{g_{\text{m1}}} \end{aligned} \tag{27}$$

Again, inspecting (27) it is clearly evident that the time-constant at the drain of M1 also reduces with increasing g_m-boosting gain "A" thus improving frequency response. Following-on, the total capacitance at the drain of M4 is given by,

$$\begin{aligned} C_{\text{tot\_drain\_M4}} &= C_{\text{db\_M4}} + C_{\text{sb\_M3}} + C_{\text{gs\_M3}}(A+1) \\ &\quad + C_{\text{gd\_M4}}\left[1+\frac{1+[(\text{A}+1)g_{\text{m3}}+g_{\text{mb3}}]\,r_{\text{o3}}}{g_{\text{m4}}.(r_{\text{o3}}+R_{\text{F}})}\right] \end{aligned} \tag{28}$$

Then the time-constant at the drain of M4, $\tau_{\text{drain\_M4}}$ is given by,

$$\begin{aligned} \tau_{\text{drain\_M4}} &= \frac{r_{\text{o3}}+R_{\text{F}}}{1+[(\text{A}+1)g_{\text{m3}}+g_{\text{mb3}}]\,r_{\text{o3}}} \\ &\quad \times\left[\begin{array}{l} C_{\text{db\_M4}} + C_{\text{sb\_M3}} + C_{\text{gs\_M3}}(A+1) \\ +C_{\text{gd\_M4}}\left[1+\frac{1+[(\text{A}+1)g_{\text{m3}}+g_{\text{mb3}}]r_{\text{o3}}}{g_{\text{m4}}.(r_{\text{o3}}+R_{\text{F}})}\right] \end{array}\right] \end{aligned} \tag{29}$$

Or, simplifying,

$$\begin{aligned} \tau_{\text{drain\_M4}} &= \frac{C_{\text{db\_M4}}+C_{\text{sb\_M3}}}{[(\text{A}+1)g_{\text{m3}}]} + \frac{C_{\text{gs\_M3}}}{g_{\text{m3}}} \\ &\quad + \frac{C_{\text{gd\_M4}}}{[(\text{A}+1)g_{\text{m3}}]} + \frac{C_{\text{gd\_M4}}}{g_{\text{m4}}} \end{aligned} \tag{30}$$

Again, inspecting (30) it is clearly evident that the time constant at the drain of M4 reduces with increasing g_m-boosting gain "A" thus enhancing bandwidth. Inspecting (20), (21), (22), (23), (25), (28) it is clear that the g_m-boosted inverter-cascode trades miller-capacitance with the g_m-boosting gain "A" between the input and the internal node. Since the pole due to the photo-diode (or sensor) capacitance constitutes the dominant-pole for the transimpedance amplifier, this trading enables the reduction of the input time-constant and enhancement of the bandwidth for the transimpedance-amplifier. Thus, while cascoding reduces the miller capacitance appearing at the TIA input, the g_m-boosting supresses the miller capacitance at the TIA input further by the g_m-boosting gain "A". Also, inspecting (24), (27) and (30) it is clear that g_m-boosting reduces all the time constants resulting in an overall bandwidth improvement.

B. TRANSFER-FUNCTION OF THE g_m-BOOSTED INVERTER-CASCODE TIA

Since the time-constants at all the nodes with miller-effect capacitances have been determined, the only remaining time-constant is at the output of the TIA, which is given by,

$$\tau_{\text{output}} = R_{\text{F}}(C_{\text{dg\_M2}} + C_{\text{dg\_M3}} + C_{\text{db\_M2}} + C_{\text{db\_M3}}) \tag{31}$$

Hence the four poles of the TIA are,

$$\begin{aligned} \omega_{\text{input}} &= \frac{1}{\tau_{\text{input}}}, \quad \omega_{\text{drain\_M1}} = \frac{1}{\tau_{\text{drain\_M1}}}, \\ \omega_{\text{drain\_M4}} &= \frac{1}{\tau_{\text{drain\_M4}}}, \quad \omega_{\text{output}} = \frac{1}{\tau_{\text{output}}}. \end{aligned} \tag{32}$$

C. A ZERO CAN BE DETERMINED AS FOLLOWS

For a zero at the output of the open-loop TIA, $v_{out}(s_z) = 0$ and there is no small-signal current flowing into R_F. Then performing a KCL at the output node using Laplace domain susceptances of the capacitors,

$$v_{gd2}s_zC_{gd2} + v_{gd3}s_zC_{gd3} = (g_{m2}v_{gs2} + g_{m3}v_{gs3}) \quad (33)$$

$$(v_{gs2} + g_{m2}v_{gs2}r_{o1})s_zC_{gd2} + (v_{gs3} + g_{m3}v_{gs3}r_{o4})s_zC_{gd3} = (g_{m2}v_{gs2} + g_{m3}v_{gs3}) \quad (34)$$

$$(v_{gs2} + g_{m2}v_{gs2}r_{o1})s_zC_{gd2} + (v_{gs3} + g_{m3}v_{gs3}r_{o4})s_zC_{gd3} - (g_{m2}v_{gs2} + g_{m3}v_{gs3}) = 0 \quad (35)$$

$$v_{gs2}(s_zC_{gd2} + s_zC_{gd2}g_{m2}r_{o1} - g_{m2}) + v_{gs3}(s_zC_{gd3} + s_zC_{gd3}g_{m3}r_{o4} - g_{m3}) = 0 \quad (36)$$

Because of the symmetry of the upper and lower halves of the TIA, $v_{gs2} = -v_{gs3}$. This can be ascertained from the push-pull operation at the output of the TIA. When the small-signal input-voltage of the open-loop TIA goes up the drain current of M1 goes down while the drain current of M4 goes up. As a result the v_{gs} of M2 goes down and the v_{gs} of M3 goes up. Consequently, the output voltage goes down aided by both the top and the bottom halves of the TIA. Exactly the opposite happens when the input voltage goes down with the output going up aided by both the halves of the TIA. Hence $v_{gs3} = -v_{gs2}$.

Then from (36),

$$[s_z(C_{gd2} - C_{gd3} + C_{gd2}g_{m2}r_{o1} - C_{gd3}g_{m3}r_{o4}) - g_{m2} + g_{m3})]v_{gs} = 0 \quad (37)$$

And,

$$s_Z = \frac{(g_{m2} - g_{m3})}{(C_{gd2} - C_{gd3} + C_{gd2}g_{m2}r_{o1} - C_{gd3}g_{m3}r_{o4})} \quad (38)$$

The zero is possibly complex, and, although the devices in the upper and lower PMOS and NMOS halves are symmetrically located, they are unmatched. Consequently there is a finite value of this zero of the overall transfer function.

D. NOISE EQUATIONS FOR THE G_m-BOOSTED INVERTER-CASCODE TIA

Considering only thermal-noise of resistors and the drain-current noise of the MOSFET devices, the noise-inserted [21], [22] g_m-boosted inverter-cascode TIA with noise-current-spectral-densities associated with all the devices is shown in the Fig. 5, where the drain-current-noise can be expressed by a current-source connected across the drain and the source of the MOSFET devices operating in the saturation region [13]. Thus, the noise-current-power-spectral-densities of MOSFETs and the resistor R_F in the Fig. 5 are given by [23],

$$\overline{i^2_{n,mj}} = 4KT\frac{\gamma_j}{\alpha_j}g_{mj} \quad (39)$$

where γ and α are noise dependent MOSFET parameters. Also, j = 1 . . . . . 6 for the devices M1 through M6, and j = 9 . . . . .18 for the devices M9 to M18.

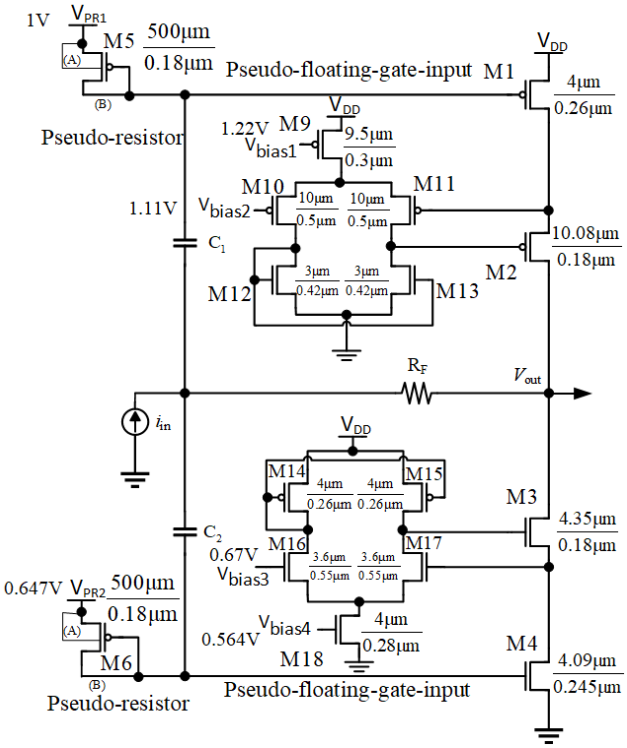

FIGURE 4. Complete transistor-level diagram of the g_m-boosted inverter-cascode TIA.

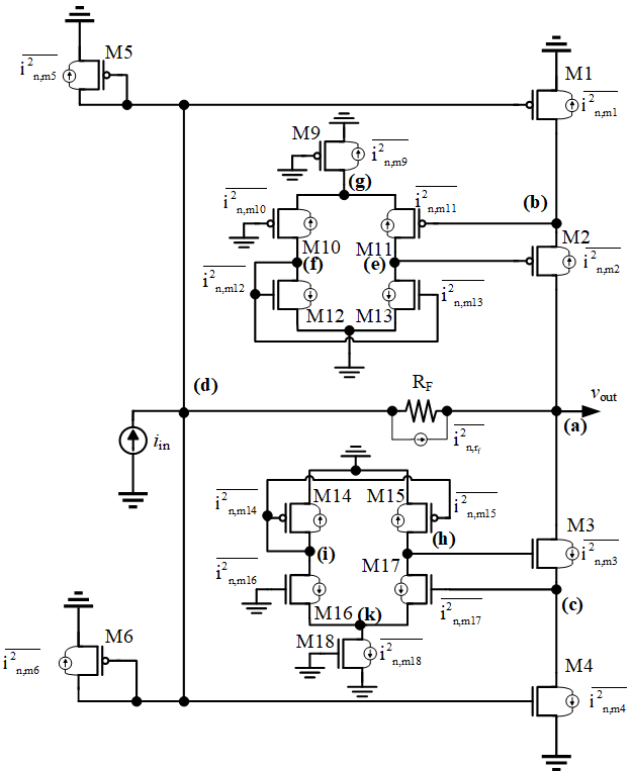

FIGURE 5. Noise inserted (noise perturbed) AC equivalent circuit of the CMOS g_m-boosted inverter-cascode TIA.

And in addition,

$$\overline{i^2_{n,R_F}} = 4KT\frac{1}{R_F} \quad (40)$$

where, K is the Boltzman constant and T is the temperature in Kelvin. Next, the noise-current-power-spectral-density of R_F arriving at the node (a) splits into two equal components, so that the component at the drain of M2 is given by, $\frac{\overline{i^2_{n,R_F}}}{2}$. The noise-current-power-spectral-density at the drain can be referred to the source directly, but the drain-current-noise-power cannot be referred to the source directly; it is referred as noise-voltage-power-spectral-density to the gate-node [21]. Thus the noise-current-power arriving at the drain of M2 can be referred to the source of M2 at node (b). Next, the noise-voltage-power-spectral-density referred to the gate of M2 at node (e) is given by,

$$\overline{v^2_{n,in\text{-}e}} = \overline{i^2_{n,m2}}\left(\frac{1}{g_{m2}}\right)^2 \tag{41}$$

Thus, the input referred noise-current-power-spectral-density at the drain of M11 (@ node (e)) can be written as,

$$\overline{i^2_{n,in\text{-}e}} = \overline{v^2_{n,in\text{-}e}}(2\pi f)^2(C_{gd11} + C_{db11} + C_{gd13} + C_{db13} + C_{gs2} + C_{gd2})^2 \tag{42}$$

Since in the saturation region, C_{gs} ($\approx 2/3C_{ox}$) $\gg C_{gd}$, we can simplify the above as,

$$\overline{i^2_{n,in\text{-}e}} = \overline{v^2_{n,in\text{-}e}}(2\pi f)^2(C_{db11} + C_{db13} + C_{gs2})^2 \tag{43}$$

Similarly, the noise-voltage-power-spectral-density referred to node (f) due to M12 and M13 is given by,

$$\overline{v^2_{n,in\text{-}f}} = \overline{i^2_{n,m12}}\left(\frac{1}{g_{m12}}\right)^2 + \overline{i^2_{n,m13}}\left(\frac{1}{g_{m13}}\right)^2 \tag{44}$$

And, the noise-current-power-spectral-density referred to the source of M10 (@ node (g)) can be found by,

$$\overline{i^2_{n,in\text{-}f}} = \overline{v^2_{n,in\text{-}f}}(2\pi f)^2(C_{gd10} + C_{db10} + C_{gs12} + C_{db12} + C_{gs13} + C_{gd13})^2 \tag{45}$$

which can be simplified to,

$$\overline{i^2_{n,in\text{-}f}} = \overline{v^2_{n,in\text{-}f}}(2\pi f)^2(C_{db10} + C_{gs12} + C_{db12} + C_{gs13})^2 \tag{46}$$

Hence, the total input referred noise-current-power-spectral-density at node (g) is the sum of the noise-current-powers at nodes (e), (f) and the drain-current-noise-power of M9, given by,

$$\overline{i^2_{n,in\text{-}g}} = \overline{i^2_{n,in\text{-}e}} + \overline{i^2_{n,in\text{-}f}} + \overline{i^2_{n,in\text{-}9}} \tag{47}$$

Accordingly, the total noise-voltage-power-spectral-density referred to the gate of M11 at node (b) is given by,

$$\overline{v^2_{n,in\text{-}b}} = \overline{i^2_{n,in\text{-}g}}\left(\frac{1}{g_{m10} + g_{m11}}\right)^2 \left(\frac{1}{A_V^2}\right) + \overline{i^2_{n,m11}}\left(\frac{1}{g_{m11}}\right)^2 \tag{48}$$

where, A_V is the expression for the voltage-divider-gain due to the source-follower operation of M11, which is given by,

$$A_V = \left(\frac{\frac{1}{g_{m10}}}{\frac{1}{g_{m10}} + \frac{1}{g_{m11}}}\right) \tag{49}$$

Following-on,

$$\overline{i^2_{n,in\text{-}b}} = \frac{\overline{i^2_{n,R_f}}}{2} + \overline{v^2_{n,in\text{-}b}}(2\pi f)^2(C_{db1} + C_{gs2} + C_{bs2} + C_{gs11})^2 \tag{50}$$

The input referred noise of the bottom half-circuit can be found in the same way as mentioned above, as follows:

The noise-voltage-power-spectral-density referred to the gate of M3 at the node (h) is given by,

$$\overline{v^2_{n,in\text{-}h}} = \overline{i^2_{n,m3}}\left(\frac{1}{g_{m3}}\right)^2 \tag{51}$$

Thus, the input referred noise-current-power-spectral-density at the drain of M17 (@ node (h)) can be written as,

$$\overline{i^2_{n,in\text{-}h}} = \overline{v^2_{n,in\text{-}h}}(2\pi f)^2(C_{db17} + C_{db15} + C_{gs3})^2 \tag{52}$$

Similarly, the noise-voltage-power-spectral-density referred to node (i) due to M14 and M15 is given by,

$$\overline{v^2_{n,in\text{-}i}} = \overline{i^2_{n,m14}}\left(\frac{1}{g_{m14}}\right)^2 + \overline{i^2_{n,m15}}\left(\frac{1}{g_{m15}}\right)^2 \tag{53}$$

And the noise-current-power-spectral-density referred to the source of M16 (@ node (k)) can be found by,

$$\overline{i^2_{n,in\text{-}i}} = \overline{v^2_{n,in\text{-}i}}(2\pi f)^2(C_{db16} + C_{db14} + C_{gs14} + C_{gs15})^2 \tag{54}$$

Hence, the total input referred noise-current-power-spectral density at node (k) is the sum of the noise-current-powers at nodes (h), (i) and the drain-current-noise-power of M18,

$$\overline{i^2_{n,in\text{-}k}} = \overline{i^2_{n,in\text{-}h}} + \overline{i^2_{n,in\text{-}i}} + \overline{i^2_{n,in\text{-}18}} \tag{55}$$

Accordingly, the total noise-voltage-power-spectral-density referred to the gate of M17 at node (c) is given by,

$$\overline{v^2_{n,in\text{-}c}} = \overline{i^2_{n,in\text{-}k}}\left(\frac{1}{g_{m16} + g_{m17}}\right)^2 \left(\frac{1}{A_{V1}^2}\right) + \overline{i^2_{n,m17}}\left(\frac{1}{g_{m17}}\right)^2 \tag{56}$$

where, A_{V1} is the expression for the voltage-divider-gain due to the source-follower operation of M17, given by,

$$A_{V1} = \left(\frac{\frac{1}{g_{m16}}}{\frac{1}{g_{m16}} + \frac{1}{g_{m17}}}\right) \tag{57}$$

The total noise-current-power-spectral-density referred to the node (c) is given by,

$$\overline{i^2_{n,in\text{-}c}} = \frac{\overline{i^2_{n,R_f}}}{2} + \overline{v^2_{n,in\text{-}c}}(2\pi f)^2(C_{db4} + C_{gs3} + C_{bs3} + C_{gs17})^2 \tag{58}$$

Thus, the total input referred noise-voltage-power and noise-current-power spectral-densities at input node (d) are given by,

$$\begin{aligned}\overline{v^2_{\text{n,in-d}}} &= \overline{i^2_{\text{n,m5}}}\left(\frac{1}{g_{\text{m5}}}\right)^2 + \overline{i^2_{\text{n,in-b}}}\left(\frac{1}{g_{\text{m1}}}\right)^2 + \overline{i^2_{\text{n,m1}}}\left(\frac{1}{g_{\text{m1}}}\right)^2 \\ &\times \overline{i^2_{\text{n,m6}}}\left(\frac{1}{g_{\text{m6}}}\right)^2 + \overline{i^2_{\text{n,in-c}}}\left(\frac{1}{g_{\text{m4}}}\right)^2 + \overline{i^2_{\text{n,m4}}}\left(\frac{1}{g_{\text{m4}}}\right)^2 \\ &+ \overline{i^2_{\text{n,R}_\text{f}}}(R_\text{F})^2 \end{aligned} \tag{59}$$

$$\begin{aligned}\overline{v^2_{\text{n,in-d}}} &= \overline{i^2_{\text{n,m5}}}\left(\frac{1}{g_{\text{m5}}}\right)^2 + \overline{i^2_{\text{n,m6}}}\left(\frac{1}{g_{\text{m6}}}\right)^2 + \overline{i^2_{\text{n,m1}}}\left(\frac{1}{g_{\text{m1}}}\right)^2 \\ &+ \overline{i^2_{\text{n,m4}}}\left(\frac{1}{g_{\text{m4}}}\right)^2 \\ &+ \left[\frac{\overline{i^2_{\text{n,R}_\text{f}}}}{2} + \overline{v^2_{\text{n,in-b}}}(2\pi f)^2(C_{\text{db1}}+C_{\text{gs2}}+C_{\text{bs2}}+C_{\text{gs11}})^2\right] \\ &\times \left(\frac{1}{g_{\text{m1}}}\right)^2 \\ &+ \left[\frac{\overline{i^2_{\text{n,R}_\text{f}}}}{2} + \overline{v^2_{\text{n,in-c}}}(2\pi f)^2(C_{\text{db4}}+C_{\text{gs3}}+C_{\text{bs3}}+C_{\text{gs17}})^2\right] \\ &\times \left(\frac{1}{g_{\text{m4}}}\right)^2 + \overline{i^2_{\text{n,R}_\text{f}}}(R_\text{F})^2 \end{aligned} \tag{60}$$

Eliminating terms with denominators of the form Rg_m^2,

$$\begin{aligned}\overline{v^2_{\text{n,in-d}}} &= \overline{i^2_{\text{n,m5}}}\left(\frac{1}{g_{\text{m5}}}\right)^2 + \overline{i^2_{\text{n,m6}}}\left(\frac{1}{g_{\text{m6}}}\right)^2 + \overline{i^2_{\text{n,m1}}}\left(\frac{1}{g_{\text{m1}}}\right)^2 \\ &+ \overline{i^2_{\text{n,m4}}}\left(\frac{1}{g_{\text{m4}}}\right)^2 \\ &+ \left[\overline{v^2_{\text{n,in-b}}}(2\pi f)^2(C_{\text{db1}}+C_{\text{gs2}}+C_{\text{bs2}}+C_{\text{gs11}})^2\right]\left(\frac{1}{g_{\text{m1}}}\right)^2 \\ &+ \left[\overline{v^2_{\text{n,in-c}}}(2\pi f)^2(C_{\text{db4}}+C_{\text{gs3}}+C_{\text{bs3}}+C_{\text{gs17}})^2\right]\left(\frac{1}{g_{\text{m4}}}\right)^2 \\ &+ \overline{i^2_{\text{n,R}_\text{f}}}(R_\text{F})^2 \end{aligned} \tag{61}$$

Next, neglecting 4$^{\text{th}}$ order capacitance product terms,

$$\begin{aligned}\overline{v^2_{\text{n,in-d}}} &= \left[\overline{i^2_{\text{n,m5}}}\left(\frac{1}{g_{\text{m5}}}\right)^2 + \overline{i^2_{\text{n,m6}}}\left(\frac{1}{g_{\text{m6}}}\right)^2 \right. \\ &\left. + \overline{i^2_{\text{n,m1}}}\left(\frac{1}{g_{\text{m1}}}\right)^2 + \overline{i^2_{\text{n,m4}}}\left(\frac{1}{g_{\text{m4}}}\right)^2\right] \\ &+ \left[[\overline{i^2_{\text{n,in-9}}}\left(\frac{1}{g_{\text{m10}}+g_{\text{m11}}}\right)^2(\frac{1}{A_\text{V}^2}) + \overline{i^2_{\text{n,m11}}}\left(\frac{1}{g_{\text{m11}}}\right)^2\right. \\ &\left.\times (2\pi f)^2(C_{\text{db1}}+C_{\text{gs2}}+C_{\text{bs2}}+C_{\text{gs11}})^2\right]\left(\frac{1}{g_{\text{m1}}}\right)^2 \\ &+ \left[[\overline{i^2_{\text{n,in-18}}}\left(\frac{1}{g_{\text{m16}}+g_{\text{m17}}}\right)^2(\frac{1}{A_\text{IV}^2}) + \overline{i^2_{\text{n,m17}}}\left(\frac{1}{g_{\text{m17}}}\right)^2\right. \\ &\left.\times (2\pi f)^2(C_{\text{db4}}+C_{\text{gs3}}+C_{\text{bs3}}+C_{\text{gs17}})^2\right]\left(\frac{1}{g_{\text{m4}}}\right)^2 \\ &+ \left[\overline{i^2_{\text{n,R}_\text{f}}}(R_\text{F})^2\right] \end{aligned} \tag{62}$$

$$\begin{aligned}\overline{i^2_{\text{n,in-d}}} &= \overline{v^2_{\text{n,in-d}}}[\frac{1}{R_\text{F}^2} + (2\pi f)^2(C_{\text{PD}}+C_{\text{gs5}}+C_{\text{db5}}+C_{\text{gs6}}+C_{\text{db6}} \\ &+ C_{\text{gs1}}+C_{\text{gd1}}+C_{\text{gs4}}+C_{\text{gd4}})^2] \end{aligned} \tag{63}$$

which can be simplified as,

$$\begin{aligned}\overline{i^2_{\text{n,in-d}}} &= \left[\overline{i^2_{\text{n,m5}}}\left(\frac{1}{g_{\text{m5}}}\right)^2 + \overline{i^2_{\text{n,m6}}}\left(\frac{1}{g_{\text{m6}}}\right)^2 \right. \\ &\left. + \overline{i^2_{\text{n,m1}}}\left(\frac{1}{g_{\text{m1}}}\right)^2 + \overline{i^2_{\text{n,m4}}}\left(\frac{1}{g_{\text{m4}}}\right)^2\right] \\ &\times [\frac{1}{R_\text{F}^2} + (2\pi f)^2(C_{\text{PD}}+C_{\text{gs5}}+C_{\text{db5}} \\ &+ C_{\text{gs6}}+C_{\text{db6}}+C_{\text{gs1}}+C_{\text{gs4}})^2] \\ &+ \left[[\overline{i^2_{\text{n,in-9}}}\left(\frac{1}{g_{\text{m10}}+g_{\text{m11}}}\right)^2(\frac{1}{A_\text{V}^2}) + \overline{i^2_{\text{n,m11}}}\left(\frac{1}{g_{\text{m11}}}\right)^2\right. \\ &\left.\times (2\pi f)^2(C_{\text{db1}}+C_{\text{gs2}}+C_{\text{bs2}}+C_{\text{gs11}})^2\right]\left(\frac{1}{g_{\text{m1}}}\right)^2 \\ &\times [\frac{1}{R_\text{F}^2} + (2\pi f)^2(C_{\text{PD}}+C_{\text{gs5}}+C_{\text{db5}} \\ &+ C_{\text{gs6}}+C_{\text{db6}}+C_{\text{gs1}}+C_{\text{gs4}})^2] \\ &+ \left[[\overline{i^2_{\text{n,in-18}}}\left(\frac{1}{g_{\text{m16}}+g_{\text{m17}}}\right)^2(\frac{1}{A_{\text{V1}}^2}) + \overline{i^2_{\text{n,m17}}}\left(\frac{1}{g_{\text{m17}}}\right)^2\right. \\ &\left.\times (2\pi f)^2(C_{\text{db4}}+C_{\text{gs3}}+C_{\text{bs3}}+C_{\text{gs17}})^2\right]\left(\frac{1}{g_{\text{m4}}}\right)^2 \\ &\times [\frac{1}{R_\text{F}^2} + (2\pi f)^2(C_{\text{PD}}+C_{\text{gs5}}+C_{\text{db5}} \\ &+ C_{\text{gs6}}+C_{\text{db6}}+C_{\text{gs1}}+C_{\text{gs4}})^2] \\ &+ \left[\overline{i^2_{\text{n,R}_\text{f}}}(R_\text{F})^2\right] \times [\frac{1}{R_\text{F}^2} + (2\pi f)^2(C_{\text{PD}}+C_{\text{gs5}}+C_{\text{db5}} \\ &+ C_{\text{gs6}}+C_{\text{db6}}+C_{\text{gs1}}+C_{\text{gs4}})^2] \end{aligned} \tag{64}$$

Or, eliminating terms with denominators of the forms $R^2g_\text{m}^2$, $R^2g_\text{m}^3$, as well as terms with 4$^{\text{th}}$ order capacitance

product terms,

$$\overline{i^2_{n,in\text{-}d}} = \left[\overline{i^2_{n,m5}}\left(\frac{1}{g_{m5}}\right)^2 + \overline{i^2_{n,m6}}\left(\frac{1}{g_{m6}}\right)^2 + \overline{i^2_{n,m1}}\left(\frac{1}{g_{m1}}\right)^2 + \overline{i^2_{n,m4}}\left(\frac{1}{g_{m4}}\right)^2\right] \times [(2\pi f)^2 (C_{PD} + C_{gs5} + C_{db5} + C_{gs6} + C_{db6} + C_{gs1} + C_{gs4})^2] + \left[\overline{i^2_{n,R_f}}(R_F)^2\right] \times [\frac{1}{R_F^2} + (2\pi f)^2 (C_{PD} + C_{gs5} + C_{db5} + C_{gs6} + C_{db6} + C_{gs1} + C_{gs4})^2] \quad (65)$$

Or,

$$\overline{i^2_{n,in\text{-}d}} = \left[\overline{i^2_{n,m5}}\left(\frac{1}{g_{m5}}\right)^2 + \overline{i^2_{n,m6}}\left(\frac{1}{g_{m6}}\right)^2 + \overline{i^2_{n,m1}}\left(\frac{1}{g_{m1}}\right)^2 + \overline{i^2_{n,m4}}\left(\frac{1}{g_{m4}}\right)^2\right] \times [(2\pi f)^2 (C_{PD} + C_{gs5} + C_{db5} + C_{gs6} + C_{db6} + C_{gs1} + C_{gs4})^2] + [\frac{4KT}{R_F} + 4KTR_F (2\pi f)^2 (C_{PD} + C_{gs5} + C_{db5} + C_{gs6} + C_{db6} + C_{gs1} + C_{gs4})^2] \quad (66)$$

Or,

$$\overline{i^2_{n,in\text{-}d}} = \left[4KT\frac{\gamma_5}{\alpha_5}\frac{1}{g_{m5}} + 4KT\frac{\gamma_6}{\alpha_6}\frac{1}{g_{m6}} + 4KT\frac{\gamma_1}{\alpha_1}\frac{1}{g_{m1}} + 4KT\frac{\gamma_4}{\alpha_4}\frac{1}{g_{m4}}\right] \times [(2\pi f)^2 (C_{PD} + C_{gs5} + C_{db5} + C_{gs6} + C_{db6} + C_{gs1} + C_{gs4})^2] + [\frac{4KT}{R_F} + 4KTR_F (2\pi f)^2 (C_{PD} + C_{gs5} + C_{db5} + C_{gs6} + C_{db6} + C_{gs1} + C_{gs4})^2] \quad (67)$$

Or in the final form,

$$\overline{i^2_{n,in\text{-}d}} = \frac{4KT}{R_F} + \left[4KTR_F + 4KT\frac{\gamma_5}{\alpha_5}\frac{1}{g_{m5}} + 4KT\frac{\gamma_6}{\alpha_6}\frac{1}{g_{m6}} + 4KT\frac{\gamma_1}{\alpha_1}\frac{1}{g_{m1}} + 4KT\frac{\gamma_4}{\alpha_4}\frac{1}{g_{m4}}\right] \times [(2\pi f)^2 (C_{PD} + C_{gs5} + C_{db5} + C_{gs6} + C_{db6} + C_{gs1} + C_{gs4})^2] \quad (68)$$

Since the transconductances of the diode-connected pseudo-resistors are very small due to the flow of the leakage-current as their bias-current, it is essential to choose appropriate sizes of these devices in order to reduce the input referred noise with increasing frequency.

III. SIMULATION AND EXPERIMENTAL RESULTS

The g_m-boosted inverter-cascode TIA was simulated and fabricated using the 180-nm TSMC CMOS process technology, and, a 1.8V power-supply was employed for the simulations and the measurements. Relatively similar component and device sizes for the corresponding transistors were employed for the g_m-boosted inverter-cascode TIA and the non-g_m-boosted (basic) inverter-cascode TIA for their performance comparison. Both numerical solution using MATLAB to determine the effect of varying the g_m-boosting gain "A" based on the derived equations, as well as, Cadence spectre circuit simulation of the overall gain-bandwidth was carried out. All the bias voltages and device sizes are shown in the Fig. 4. The transconductances, body-transconductances and output resistances of the MOFET devices in the Fig. 4 were as follows: For M1, $g_{m1} = 372.269$ μ-siemens and $r_{o1} = 100.35$ k-ohms. For M2, $g_{m2} = 630.58$ μ-siemens, $g_{mb2} = 176.9$ μ- siemens and $r_{o2} = 26.40$ k-ohms. For M3, $g_{m3} = 692.45$ μ- siemens, $g_{mb3} = 150.53$ μ-siemens and $r_{o3} = 10.37$ k-ohms. For M4, $g_{m4} = 647.25$ μ-siemens and $r_{o4} = 80.73$ k-ohms. For pseudo-resistors M5 and M6, $g_{m5} = g_{m6} \approx 0.01$ μ- siemens and $r_{o5} = r_{o6} \approx 26.7273$ M-ohms. For M9, $g_{m9} = 201.88$ μ-siemens, and $r_{o9} = 50.80$ k-ohms. For M10, $g_{m10} = 113.53$ μ-siemens, $g_{mb10} = 36.42$ μ-siemens and $r_{o10} = 1.49$ M-ohms. For M11, $g_{m11} = 109.63$ μ-siemens, $g_{mb11} = 35.12$ μ-siemens and $r_{o11} = 1.70$ M-ohms. For M12, $g_{m12} = 119.80$ μ-siemens and $r_{o12} = 858.66$ k-ohms. For M13, $g_{m13} = 112.92$ μ-siemens and $r_{o13} = 448.90$ k-ohms. For M14, $g_{m14} = 107.43$ μ-siemens and $r_{o14} = 653.70$ k-ohms. For M15, $g_{m15} = 102.32$ μ-siemens and $r_{o15} = 501.41$ k-ohms. For M16, $g_{m16} = 113.39$ μ-siemens, $g_{mb16} = 30.83$ μ- siemens and $r_{o16} = 1.87$ M-ohms. For M17, $g_{m17} = 109.37$ μ-siemens, $g_{mb17} = 29.73$ μ-siemens and $r_{o17} = 2.18$ M-ohms. For M18, $g_{m18} = 213.79$ μ-siemens and $r_{o18} = 33.49$ k-ohms. The feedback resistor $R_F = 4,532$ ohm. A photo-diode (sensor) capacitance of 2.7pF was used in the simulations. The various device capacitances are as follows: $C_{db_M1} = 2.84$fF, $C_{db_M4} = 0.002$fF, $C_{gd_M1} = 1.62$fF, $C_{gd_M4} = 1.39$fF, $C_{gs_M1} = 6.53$fF, $C_{gs_M2} = 9.66$fF, $C_{gs_M3} = 4.41$fF, $C_{gs_M4} = 5.78$fF, $C_{gs_M5} = 16.6$fF, $C_{gs_M6} = 16.54$fF, $C_{sb_M2} = 1.12$fF, $C_{sb_M3} = 0.49$fF. The Fig. 6 shows increasing closed-loop gain of the g_m-boosted inverter-cascode TIA with increasing g_m-boosting gain "A" in accordance with (14) – (16) and the theoretical discussions. Next, Fig. 7 shows the considerable reduction of the miller capacitance at the input with the g_m-boosting gain "A" while Fig. 8 shows the variation of the total capacitance at the TIA input. Fig. 9 shows that the dominant pole position at the input moves to higher frequency with the g_m-boosting gain "A", and, in addition, Figs. 10 and 11 indicate that the non-dominant pole positions at the sources of M2 and M3 also moves to higher frequencies with the g_m-boosting gain "A". Fig. 12 shows the variation of the input referred noise current spectral density with frequency indicating a noise current density of around

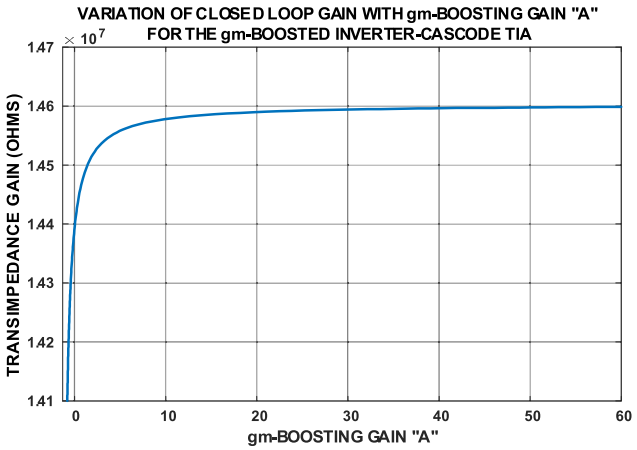

FIGURE 6. Variation of closed-loop gain of the g_m-boosted inverter-cascode TIA with g_m-boosting gain "A."

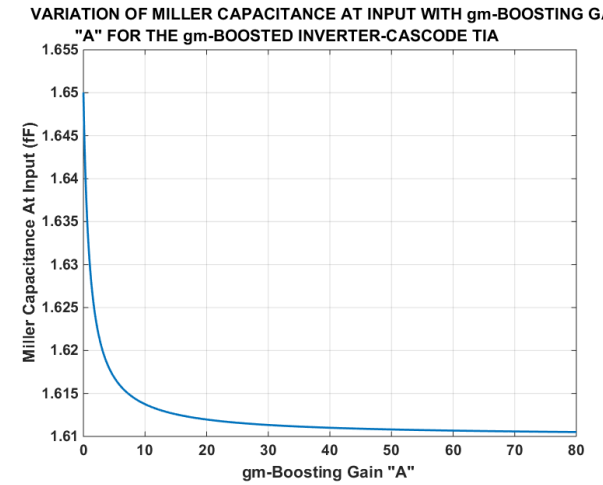

FIGURE 7. Reduction of the Miller capacitance at the TIA input with g_m-boosting gain "A."

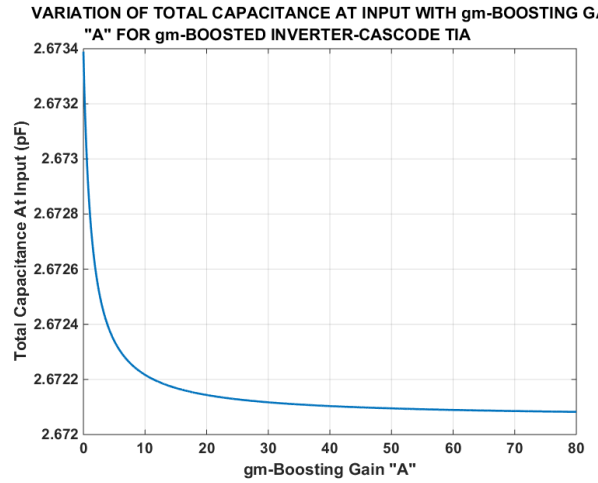

FIGURE 8. Variation of the total capacitance including $C_{PD(sensor)}$ at the TIA input with the g_m-boosting gain "A."

13 pA/sqrt(Hz) within the bandwidth of the TIA. The theoretical input referred noise current spectral density is also shown which is close to the simulated curve. Following-on, Fig. 13 shows a transient simulation of the g_m-boosted

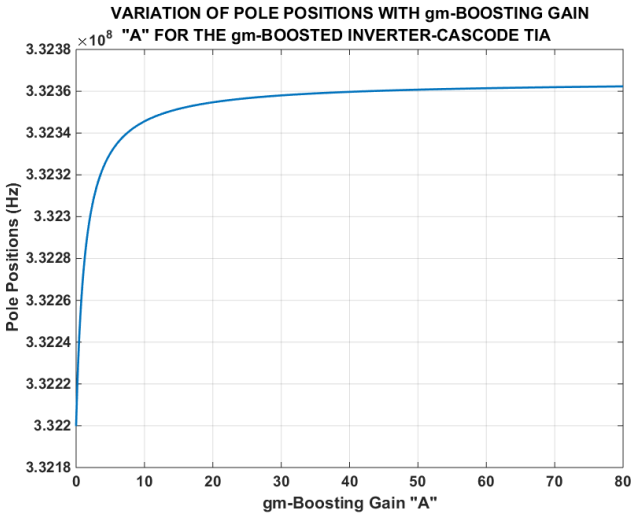

FIGURE 9. Variation of the pole position at the input of the TIA with the g_m-boosting gain "A."

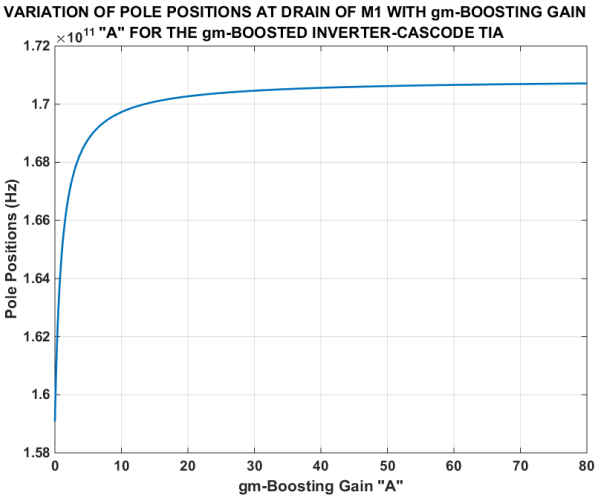

FIGURE 10. Variation of the pole position at the source of M2 with g_m-boosting gain "A."

inverter-cascode TIA indicating a nominal transimpedance gain of around 94dBΩ.

Next, Fig. 14 depicts an AC-analysis simulation of the closed loop g_m-boosted inverter-cascode TIA indicating a gain of around 133 dBΩ along with a bandwidth of around 3.1 MHz which is suitable for many slowly varying sensing and biomedical applications requiring high gain without the need for very high bandwidth. Simulation of an inverter-cascode TIA with similar device sizes and feed-back resistor but without g_m-boosting yielded a gain of only around 85 dBΩ. Compared to a gain-bandwidth of only around 37,344 Ω-MHz without g_m-boosting, a gain-bandwidth of around 13,847,191 Ω-MHz was indicated by the AC-simulation employing the g_m-boosting around the inverter-cascode TIA. Fig. 15 depicts respectively, (a) the open-loop gain (bode-plot), and, (b) the phase variation,

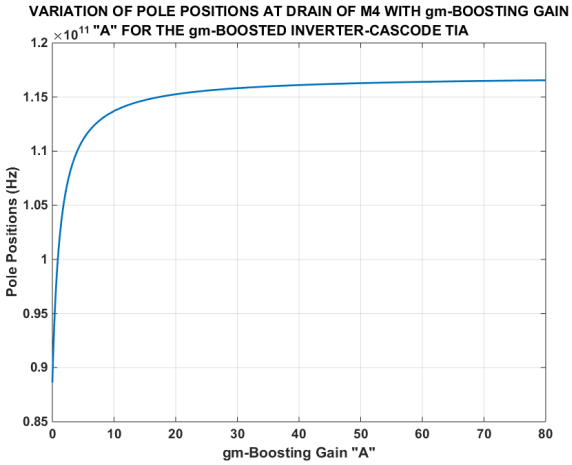

FIGURE 11. Variation of the pole position at the source of M3 with g_m-boosting gain "A."

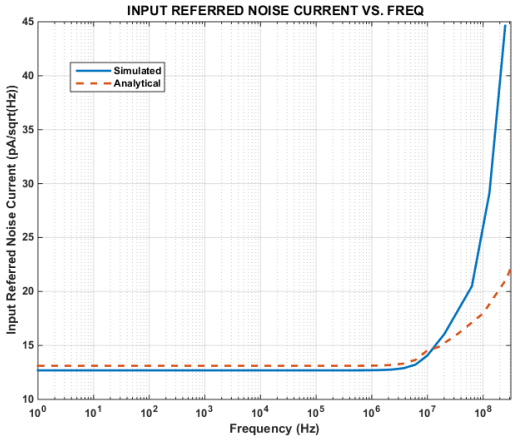

FIGURE 12. Circuit simulated and numerically calculated Input referred noise current spectral density for the g_m-boosted inverter-cascode TIA.

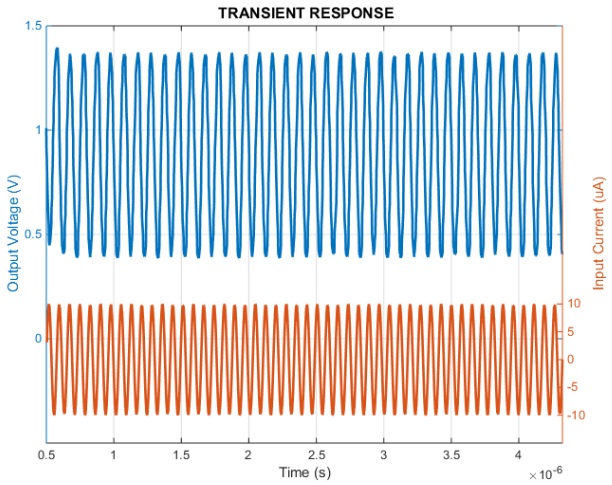

FIGURE 13. A transient simulation of the g_m-boosted inverter-cascode TIA indicating a transimpedance gain of around 94 dBΩ. It shows the transient sinusoidal response of the TIA for a nominal 12 MHz input-signal. As shown in this figure, the peak-to-peak output-voltage swing is around 1V for a test peak-to-peak input-current swing of 20 μA.

obtained from the simulation of an open-loop configuration of the g_m-boosted inverter-cascode TIA which also represents the loop-gain (T) of the TIA for unity feed-back ($\beta = 1$).

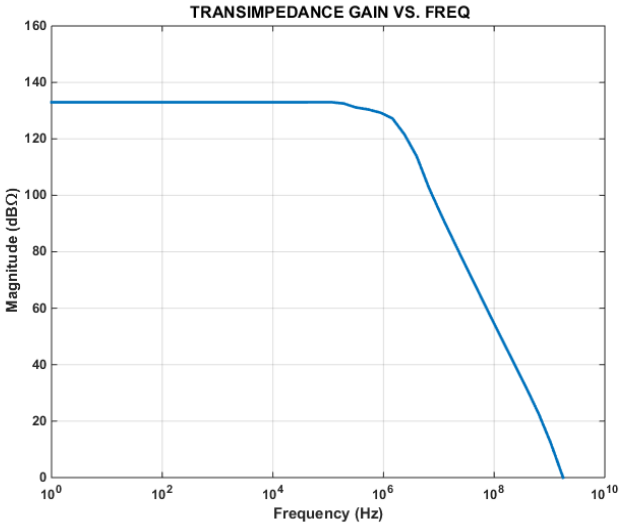

FIGURE 14. The AC-analysis simulation of the g_m-boosted inverter-cascode TIA.

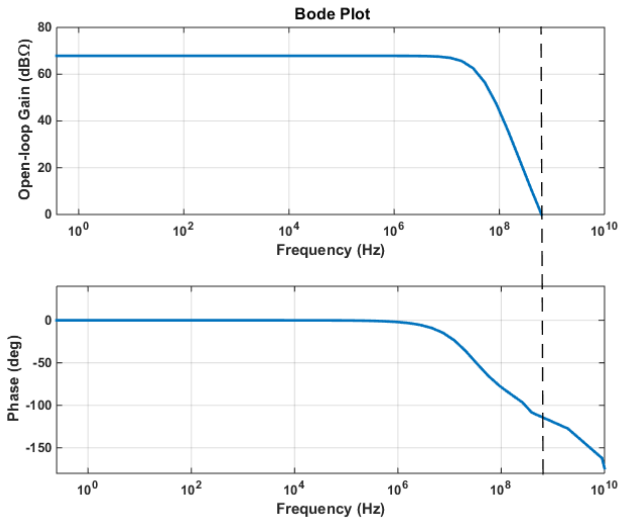

FIGURE 15. (a) The open-loop gain, and (b) the phase response, obtained from the simulation of an open-loop configuration of the g_m-boosted inverter-cascode TIA.

The plots thus indicate stable operation with a phase-margin of 66° for the unity feed-back loop-gain. Since the feed-back factor of $1/R_F$ will reduce (scale-down) the loop-gain while having the same poles and zeros, the TIA is expected to have a higher phase margin than 66°.

Following-on, Fig. 16 shows the photomicrograph of the fabricated g_m-boosted inverter-cascode TIA with a large area consumed by the feedback resistor. Next, Fig. 17(a) shows the experimental setup for testing the fabricated g_m-boosted inverter-cascode TIA, while, Fig. 17(b) shows the top and bottom photos of the fabricated PCB used for mounting and testing the TIA chip in a DIP package. A voltage signal wave-form from a Tektronix AFG3021C single-channel arbitrary function generator is the primary input to the PCB.

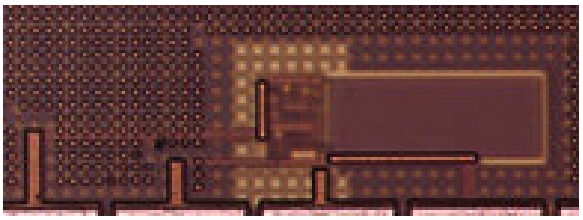

FIGURE 16. The photomicrograph of the fabricated g_m-boosted inverter-cascode TIA.

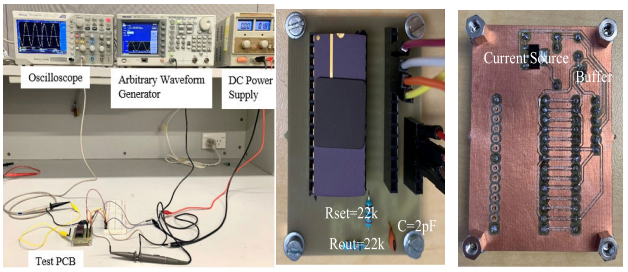

FIGURE 17. (a) Experimental setup for testing the fabricated g_m-boosted inverter-cascode TIA, and (b) the top and bottom photos of the fabricated PCB used for mounting and testing the TIA chip in a DIP package.

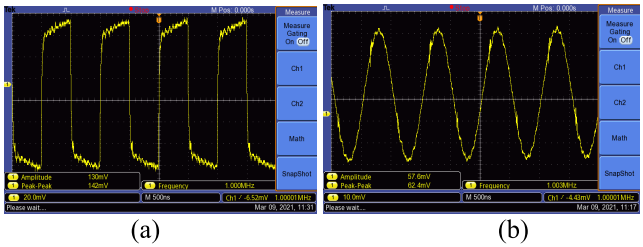

FIGURE 18. Transient voltage outputs of the fabricated g_m-boosted inverter-cascode TIA for current-source inputs, (a) square-wave input, (b) sinusoidal-wave input.

A current source IC LT3092EST#PBF on the PCB employs this voltage wave-form to produce an equivalent current wave-form of the same shape, as an input to the fabricated g_m-boosted inverter-cascode TIA for measuring the transimpedance gain. The PCB used a 1.8V power-supply, and, 2 resistors, Rout=Rset=22k were connected to the current-source IC (underneath the PCB) to generate a current source output of 10 μA based on the data-sheet of the current source IC. A 2pF capacitor was used at the input as an equivalent photodiode (sensor) capacitance at the TIA input. The amplified voltage signal output from the TIA is fed to a non-inverting buffer-gate SN74LVC1G17DBVR and then displayed and measured out using a Tektronix TBS 1102b-EDU digital oscilloscope. A measured maximum gain of around 100 dBΩ was achieved by the fabricated g_m-boosted inverter cascode TIA compared to the AC-simulated mid-band gain of around 133 dBΩ. Fig. 18 shows the measured transient voltage outputs of the fabricated g_m-boosted inverter-cascode TIA for current source inputs, (a) square-wave input, (b) sinusoidal-wave input. A gain-bandwidth of around 325,000 Ω-MHz was displayed by the fabricated TIA.

IV. CONCLUSION

A g_m-boosted inverter-cascode TIA is proposed and its operation is discussed thoroughly using mathematical derivations. Simulations and experimental fabrication results are also provided. It is evident that the g_m-boosting enhances the transimpedance gain and drives the transfer function poles further down in frequency on the bode plot. Considerable gain-bandwidth improvement is thus achieved by the TIA compared to the topology without g_m-boosting. Also, a simplified inspection-based small-signal analysis method is demonstrated for the g_m-boosted inverter-cascode TIA which has not been provided before in literature.

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