A Two-Dimensional Extensible Bus Technology and Protocol for VLSI Processor Core

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Abstract

Intellectual property (IP) core design modularity and reuse in Very-Large-Scale-Integration (VLSI) silicon have been the key focus areas in design productivity improvement in order to shorten product development lead time as well as minimize design error on new product [11]. The System-On-Chip (SoC) design approach has been adopted in microprocessor design flow with many functional blocks reuse in silicon. SoC has the advantage of cost efficiency and higher fabrication yield. The fundamental building block of SoC is the interconnection of intellectual property (IP) core through a shared bus to establish an on-chip communication. As IP core integration is severely constraint by silicon wafer sizes (cost per die), the right level of integration is never an easy decision. System-in-Package (SiP) addresses this drawback with package level IP core integration. However, SiP has the drawback of lower fabrication yield which results in higher manufacturing cost [6]. In order to address these issues, a new level of integration has been suggested in order to reduce the drawbacks of SiP and SoC approaches. This new integration methodology is also known as System-in-System (SiS) which emulates SoC and SiP at the system level.

The thesis contains a detailed treatment on the processor architecture and SoC used. The design methodologies have been discussed too.

The thesis also contains treatment on the verification methodologies and technologies that are used in design validation.

Research includes the design of two dimensional XBUS system for external IP core integration on SoC. The thesis proposed a system level bus for IP integration through the XBUS. As there are multiple ways of integrating IP core at the system level, the XBUS is limited to two channels (hence two dimensional) in order to simplify implementation complexities.

Based on experimental results, the proposed method can be introduced as a very promising method for the design of SoC and various other high-performance computer systems.

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