Hindawi Publishing Corporation
Active and Passive Electronic Components
Volume 2013, Article ID 148518, 6 pages
http://dx.doi.org/10.1155/2013/148518

Research Article

A 0.8 V 0.23 nW 1.5 ns Full-Swing Pass-Transistor XOR Gate in 130 nm CMOS

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Received 18 December 2012; Accepted 5 March 2013

Academic Editor: Ching Liang Dai

A power efficient circuit topology is proposed to implement a low-voltage CMOS 2-input pass-transistor XOR gate. This design aims to minimize power dissipation and reduce transistor count while at the same time reducing the propagation delay. The XOR gate utilizes six transistors to achieve a compact circuit design and was fabricated using the 130 nm IBM CMOS process. The performance of the XOR circuit was validated against other XOR gate designs through simulations using the same 130 nm CMOS process. The area of the core circuit is only about 56 sq $\cdot \mu$m with 1.5659 ns propagation delay and 0.2312 nW power dissipation at 0.8 V supply voltage. The proposed six-transistor implementation thus compares favorably with other existing XOR gate designs.

1. Introduction

Low-power circuits have become a major design forethought with the overwhelming growth of portable applications, particularly, for battery operated hand-held devices. In addition, higher power consumption raises the temperature of the chip which in turn affects the reliability of the devices and circuits [1]. Various low-power techniques have been explored to enhance the basic logic gates such as the XOR gate which influence the overall power consumption in many system-on-chip (SOC) implementations. One of the effective ways to reduce the overall power consumption is by reducing the supply voltage. XOR gate optimization in terms of power, speed, and transistor count has significantly improved the performance of larger and complex circuits. Over the years, various 2-input XOR gate designs have been widely reported to enhance the performance of various applications such as full adder, parity generator, encryption processor, and comparator. Traditional eight-transistor static CMOS XOR gate can operate with full output swing but with the drawback of power dissipation and transistor count [2]. On the other hand, XOR circuit based on the transmission gate [3] is used to overcome the signal degradation caused by the PMOS and NMOS devices in pass-transistor logic. However, it has the drawback of the loss of driving capability and requires complementary signals to switch the PMOS and NMOS devices and hence needs more transistors and area. A cross-coupled (CC) XOR gate based on the pass-transistor logic has been reported in [4], which claims to have improved speed and power consumption than the six device pass-transistor XOR gate and works well under a low-voltage regime. A six-transistor XOR gate realized from a modified four-transistor XOR gate by cascading a standard inverter as an output driver can be found in [5], which improves the poor output signal level for certain inputs. Powerless XOR gate (P-XOR) is proposed in [6] using a four-transistor circuit with no power supply connection which consumes less power than other designs but at the expense of a large delay. Another four-transistor XOR gate design was reported in [7], based on the Gate-Diffusion-Input (GDI) cell [8]. A three-transistor XOR gate can be found in [9] using a CMOS inverter and a PMOS pass transistor. It provides low-power-delay product (PDP) but has a voltage degradation with the input combination $A = 1$ and $B = 0$. Elgamel et al. [10] also proposed a similar three-transistor XOR gate, but it consumes high power when $A = 1$ and $B = 0$ and, in addition, produces a poor logic "1" for this input combination. However, it may reach an acceptable logic high voltage level with appropriate transistor sizing. Thus,

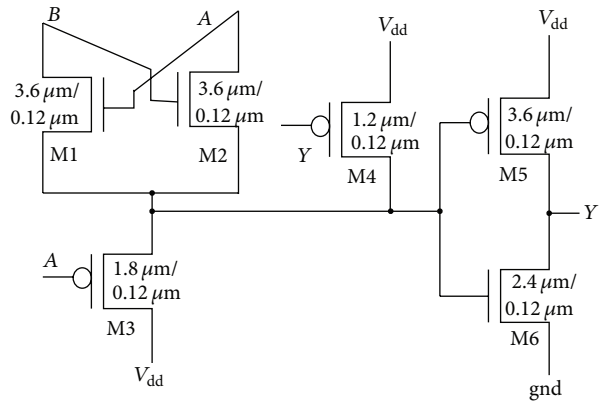

Figure 1: Circuit diagram of the proposed six-transistor pass-transistor-based full-swing CMOS XOR gate.

both the circuits [9, 10] may not operate reliably at low-supply voltage. In this brief paper, we present a novel low-power, low-voltage, and full-swing 2-input XOR circuit using 6 devices, implemented in 130 nm IBM CMOS technology.

2. Novel XOR Gate Topology for Low-Power CMOS Design

A low-power constrained 2-input XOR gate using six transistors is proposed which provides full output voltage swing for all input combinations and enables low-voltage operation with a small propagation delay. The proposed XOR circuit is based on pass-transistor logic with an inverter as the output driver to achieve perfect output swing. Pass-transistor design enables small transistor count along with smaller input loads (with signal input to source/drain instead of gate) offering very low-power operation with high performance. Since an NMOS device passes a strong "0" but a weak "1," while a PMOS device passes a strong "1" but a weak "0;" the complementary pass transistors are organized to pass a strong output logic level for all input combinations of "1" and "0".

Figure 1 shows the schematic of the proposed XOR circuit along with the device sizes using the 130 nm CMOS process. It performs a perfect full-swing operation for every input pattern. V_{dd} connections to the source terminals of M3 and M4 are used to drive a full-rail output of "1". For $A = B = 0$ condition, transistor M3 is ON, passing a strong "1" from V_{dd} to the inverter input which generates a "0" at the output Y to turn ON M4, when $A = 0$, $B = 1$, and transistors M2 and M3 are ON, which passes signals "0" and "1," respectively. To solve this problem, W/L ratio of M2 is increased making it larger than the W/L ratio of M3 so as to pass only a signal "0" to the inverter input and generate the strong output $Y = 1$. For $A = 1$ and $B = 0$, only the device M1 is ON, and a strong "0" is passed to the inverter generating a full-rail "1" to output Y. With $A = B = 1$, transistors M1 and M2 are ON, and a weak signal "1" is passed to the inverter input and, as a result, the output Y will also be degraded. However, the feedback path causes transistor M4 to turn ON when $Y = 0$ thus passing the perfect signal "1" from V_{dd} to the inverter input resulting in the generation of the perfect signal "0" at Y. This pass-transistor XOR thus does not suffer from signal level deteriorations like other pass-transistor XOR gates. The transistor sizes are carefully chosen for optimal power-delay performance under various operating conditions.

3. XOR Gate Performance Analysis and Simulation Results

Extensive simulations of the proposed XOR gate along with five other existing XOR gates found in the literature have been carried out using the 130 nm IBM CMOS technology in order to analyze the performance comparison. The simulations were carried out on the Cadence Spectre platform and the Synopsys HSPICE platform using the same test environment to measure the propagation delay and the power dissipation in each case. All the simulations were carried out with a 0.6 V to 1.2 V supply voltage range, a load capacitance of 10 fF and a throughput (clocking) rate of 200 MHz. The simulations consist of functional verification, power, timing analysis, design rule checking (DRC), and layout versus schematic (LVS) of the layout verified using Cadence Assura. The performance of all the XOR test circuits has been evaluated in terms of the worst-case propagation delay. Propagation delay is evaluated from the time interval between the 50% input and the 50% output voltage transition points. The figure-of-merit power-delay product (PDP) is calculated from the product of the worst case propagation delay and the average power consumption. Several input patterns that covered all possible cases of input values were applied, and the simulation results verified the correct functionality for every input combination up to the lower end of the supply voltage range. Figure 2 shows the HSPICE transient circuit simulation of the full-swing operation of this pass-transistor XOR gate indicating rise and fall times in the range of few hundred pico seconds (@ supply voltage, $V_{dd} = 0.8$ V). Table 1 summarizes the results of these simulations providing a comparison of the propagation delay, the power dissipation, and the PDP between the proposed circuit and the other recently reported designs. The proposed XOR gate offers lower-propagation delay than the other six-transistor XOR gates as shown in Table 1 and depicted in the line graph in Figure 3. The worst circuit in term of speed is the three-transistor XOR gate. It has the highest propagation delay against voltage scaling. The six-transistor designs by the authors in [4, 5] are close to the proposed XOR gate in term of power dissipation and propagation delay, but the proposed XOR gate provides better overall improvement compared to these other previous designs. The proposed XOR circuit performed satisfactorily for low-supply voltages, with the 0.2312 nW power dissipation compared to the 0.2319 nW dissipation by the design in [5] (@ supply voltage, $V_{dd} = 0.8$ V). The 4T XOR gates in [6, 7] and the 3T XOR gates in [1, 9, 10] have almost identical average power dissipation for all the supply voltages. The line graph in Figure 4 demonstrates the effect of voltage scaling on the average power dissipation. All other circuits have higher PDP than the proposed XOR circuit as evidenced in

Table 1: Comparison of the simulation results for different CMOS XOR gates with the proposed XOR gate.

	V_{dd} (v)	Proposed (6T)	6T [5]	6T [4]	4T [6]	4T[7]	3T [1, 9, 10]
Delay (ns)	0.6	2.1107	2.3113	7.0638	2.5818	4.1910	15.48
	0.8	1.5659	1.7672	3.6837	4.5128	3.9308	8.7314
	1	1.4691	1.6475	1.6469	4.2216	8.9244	13.038
	1.2	1.4200	1.6018	1.5500	4.1087	7.2075	12.901
Average power (nW)	0.6	0.1351	0.1352	0.1385	0.2672	0.2672	0.2672
	0.8	0.2312	0.2319	0.2401	0.4586	0.4586	0.4586
	1	0.3674	0.3689	0.3842	0.7269	0.7269	0.7268
	1.2	0.5523	0.5574	0.5835	1.0931	1.0931	1.0928
PDP (aJ)	0.6	0.2852	0.3125	0.7526	0.6899	1.1198	4.1363
	0.8	0.3620	0.4098	0.8845	2.0696	1.8027	4.0042
	1	0.5397	0.6078	0.6327	3.0687	6.4871	9.4760
	1.2	0.7843	0.8928	0.9044	4.4912	7.8785	14.098

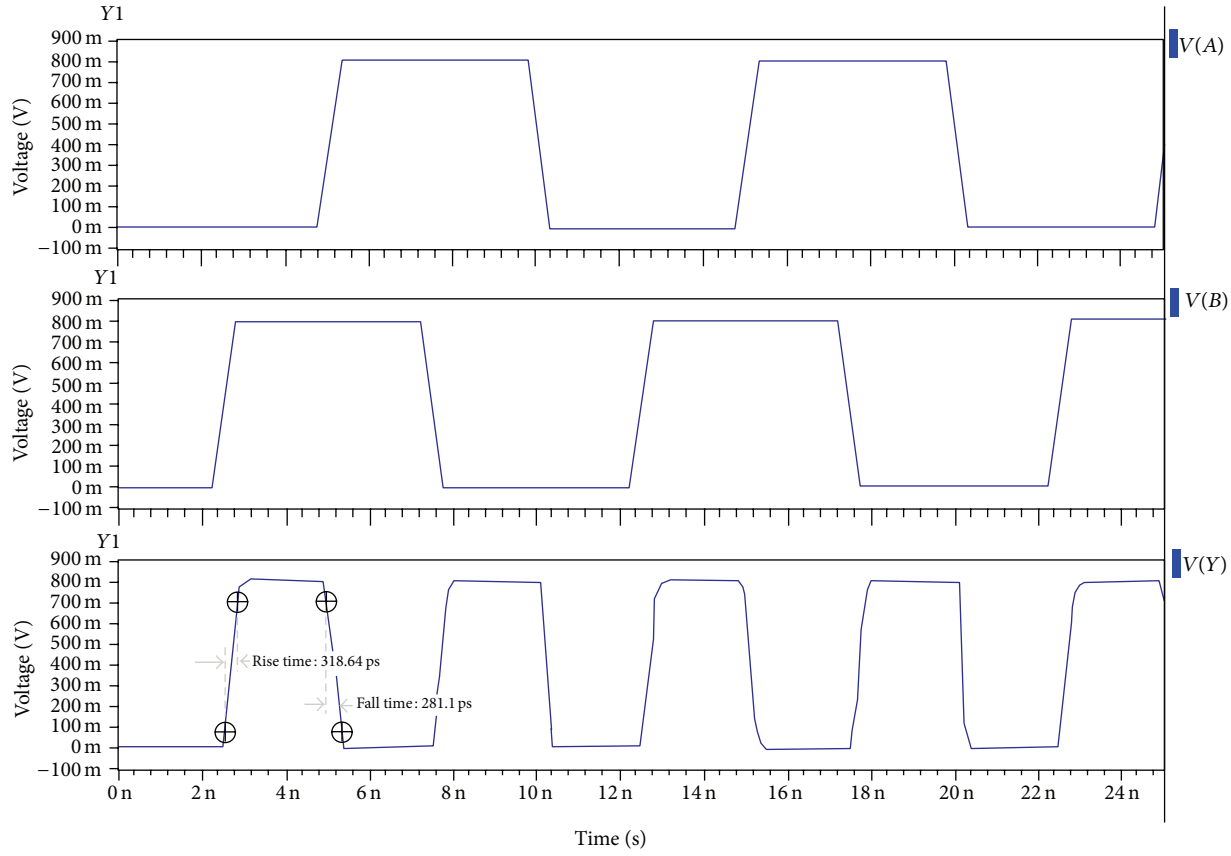

Figure 2: HSPICE transient simulation of full-swing output voltage of the novel pass-transistor XOR gate.

Table 1 and illustrated in Figure 5. At 0.8 V supply voltage, the proposed XOR circuit has at least 13.2% improvement in PDP over the design by the authors in [5] and 143.6% over the circuit by the authors in [4]. As output load is one of the parameters that affect the performance of the circuits, we have varied the output load from 10 fF to 50 fF at 0.8 V supply voltage for all circuits to study its effect on the propagation delay. The proposed XOR gate is found to be the best circuit in terms of the propagation delay for all values of output loads as shown in the line graph in Figure 6. Thus, from the simulation results, it is clear that the proposed new XOR gate has the lowest propagation delay as well as the lowest power consumption along with high output driving capability. The improvements attained by the proposed circuit are thus clearly evident when compared to these other XOR gate circuits.

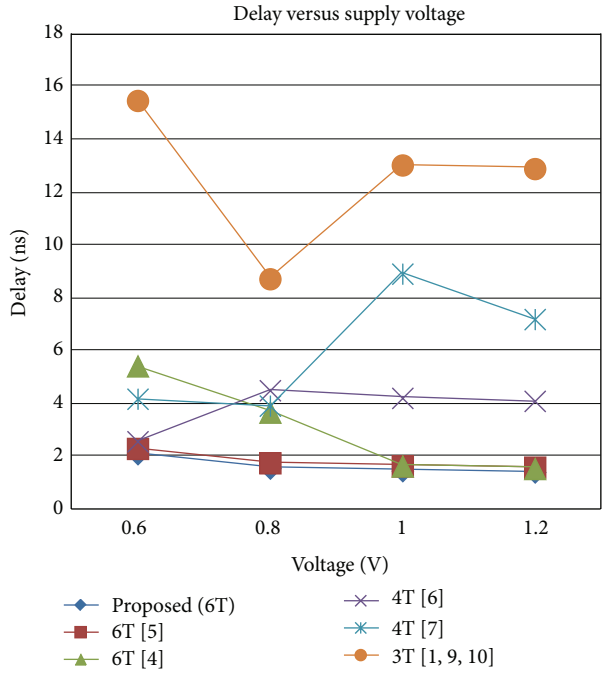

Figure 3: Line graph showing the comparison of the propagation delay versus supply voltage scaling for different CMOS XOR gates with the proposed novel CMOS pass-transistor-based full-swing XOR gate.

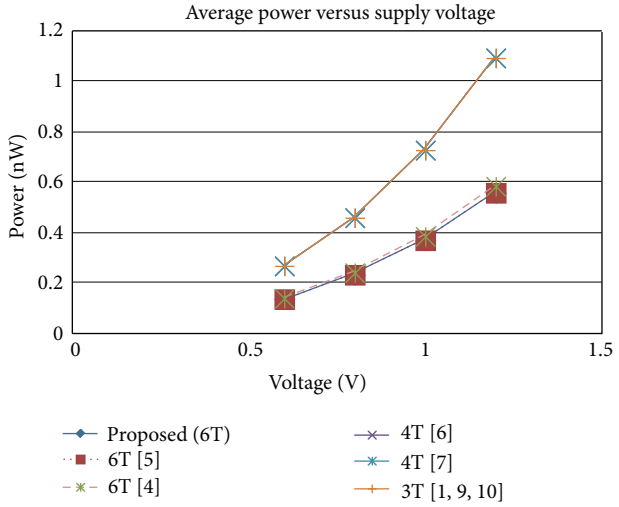

Figure 4: Line graph showing the comparison of the power dissipation versus supply voltage scaling for different CMOS XOR gates with the proposed novel CMOS pass-transistor-based full-swing XOR gate.

In order to verify the noise immunity of the proposed XOR gate, the noise margins (NM_H and NM_L) of the proposed XOR gate and the other gates were determined based on DC input-output voltage transfer analysis. The noise margins for a 0.8 V supply voltage are shown in Table 2. The proposed XOR gate indicates acceptable values of noise margin when compared with the other XOR gates.

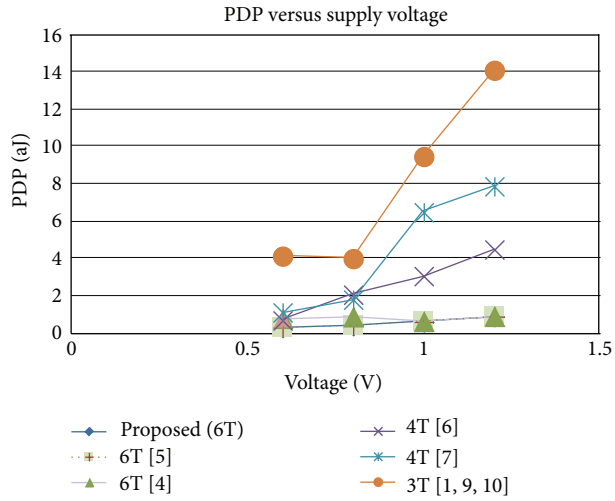

Figure 5: Line graph showing the comparison of the power-delay product (PDP) versus the supply voltage scaling for various XOR gates with the proposed novel CMOS pass-transistor-based full-swing XOR gate.

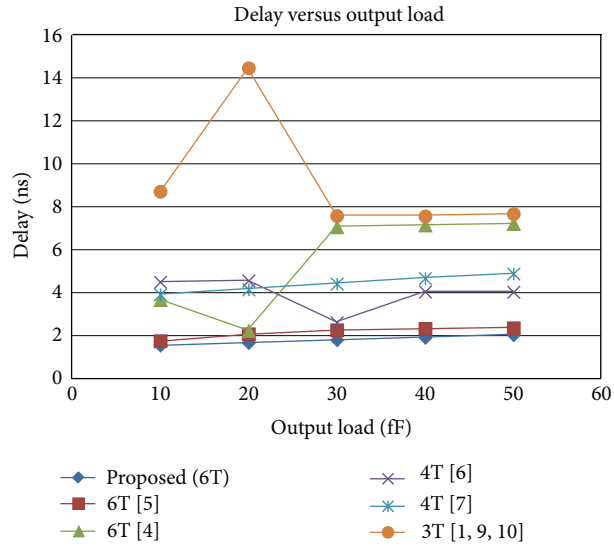

Figure 6: Line graph showing the comparison of the propagation delay versus output load for various CMOS XOR gates with the proposed novel CMOS pass-transistor-based full-swing XOR gate.

4. XOR Gate Fabrication and Experimental Results

The mask layout of the XOR gate illustrated in Figure 7 was fabricated in the 130 nm IBM CMOS process. Minimum channel length is used for all the devices, and optimum channel width is carefully chosen for each device in order to achieve verified functionality with low-power dissipation and smallest possible propagation delay. The photomicrograph of the fabricated XOR gate along with bonding pads is shown in Figure 8. The silicon area of the XOR gate was 8.02 μm × 7.03 μm (≈56 sq·μm) excluding the bonding pads. Figure 9

Table 2: Comparison of noise margins of different CMOS XOR gates with the proposed XOR gate.

Type of XOR	V_{dd} (V)	V_{oh} (V)	V_{ih} (V)	V_{il} (V)	V_{ol} (V)	NM_H (V)	NM_L (V)
Proposed (6T)	0.800	0.7186	0.3889	0.2867	0.0796	0.3297	0.2071
6T [5]	0.800	0.7204	0.3967	0.3022	0.0687	0.3237	0.2335
6T[4]	0.800	0.7205	0.3967	0.3022	0.0687	0.3238	0.2335
4T [6]	0.800	0.9460	0.6000	0.4489	0.1172	0.346	0.3317
4T [7]	0.800	1.0809	0.6444	0.4233	0.1423	0.4365	0.2810
3T [1, 9, 10]	0.800	1.0797	0.5978	0.4100	0.1332	0.4819	0.2768

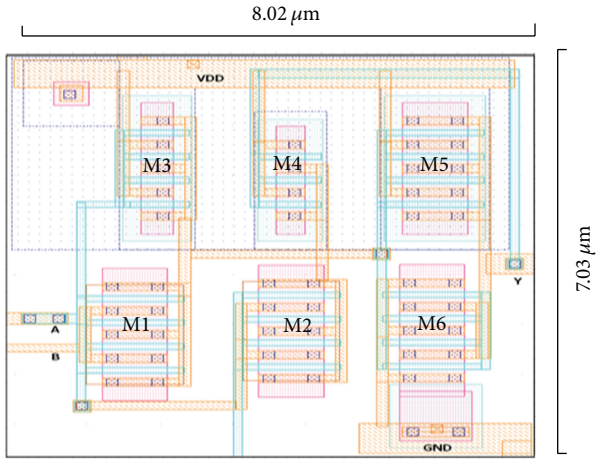

Figure 7: Layout of the proposed novel CMOS pass-transistor-based full-swing 2-input XOR gate.

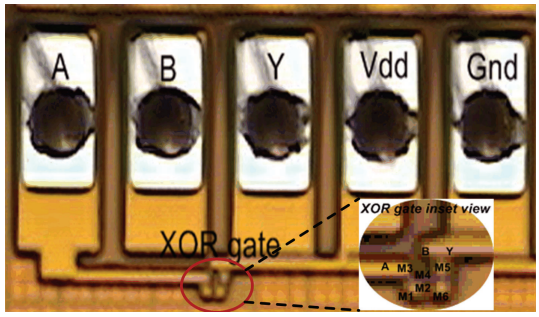

Figure 8: Microphotograph of the fabricated novel CMOS pass-transistor-based full-swing XOR gate along with bonding pads.

displays the functional verification of the XOR gate with a snapshot of the XOR input and output waveforms for several input combinations using the Tektronix TLA5202 Logic Analyzer. Level shifter was used to generate low voltage (0.8 V) from high voltage (5 V) of the pattern generator to the XOR gate input. Finally, Figure 10 provides the Agilent DCA-J (86100C Infiniium) oscilloscope electrical waveforms for the fabricated XOR gate (yellow = input A, blue = input B, and green = output Y) indicating a correct operation for a supply voltage of 0.8 V.

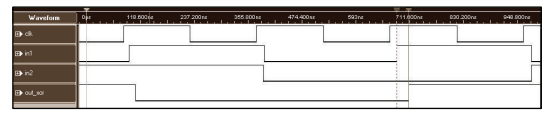

Figure 9: Logic analyzer waveform of the input and the output for the fabricated novel CMOS pass-transistor-based full-swing XOR gate.

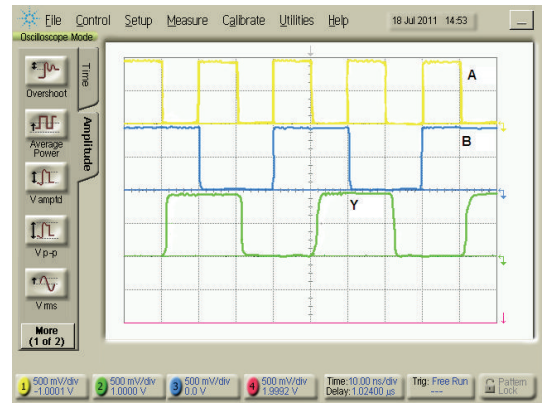

Figure 10: Oscilloscope waveforms for the fabricated novel CMOS pass-transistor-based full-swing XOR gate (yellow = input A, blue = input B, and green = output Y).

5. Conclusion

This paper demonstrates a new pass-transistor-based full-swing 2-input XOR gate topology implemented in 130 nm CMOS process suitable for reducing the power and propagation delay of an overall system on chip. The proposed XOR gate was compared to other peer XOR designs, and the results indicate satisfactory performance and improvements in term of power consumption, propagation delay, and power-delay product compared to the other designs. The proposed XOR gate has a lower-gate delay and a lower-power-delay product in comparison to its peer designs. It is thus suitable for small area and low-power applications such as RFID tags.

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