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A 6 GHz Integrated High-Efficiency Class-F⁻¹ Power Amplifier in 65 nm CMOS Achieving 47.8% Peak PAE

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Abstract: This paper reports a “single-transistor” Class-F⁻¹ power amplifier (PA) in 65 nm CMOS, which operates at the microwave center frequency of 6 GHz. The PA is loaded with a Class-F⁻¹ harmonic control network, employing a new “parasitic-aware” topology deduced using a novel iterative algorithm. A dual-purpose output matching network is designed, which not only serves the purpose of output impedance matching, but also reinforces the harmonic control of the Class-F⁻¹ harmonic network. This proposed PA yields a peak power-added efficiency (PAE) of 47.8%, which is one of the highest when compared to previously reported integrated microwave/millimeter-wave PAs in CMOS and SiGe technologies. The amplifier shows a saturated output power of 14.4 dBm along with an overall gain of 13.8 dB.

Keywords: Class-F; inverse Class-F; CMOS; power amplifier; high efficiency; 5G; mobile communications; 6 GHz



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1. Introduction

The exponential rise in the demand for a high data rate in cellular and WLAN communications requires the current systems to demonstrate their capability to handle the upcoming throughput requirements. In order to deal with this challenge, shifting the systems to higher frequency bands in the spectrum is the only viable solution. A significant module in wireless systems is the power amplifier (PA). Integrated power amplifiers operable at microwave/millimeter-wave frequencies focusing 5G-communications are expected to demonstrate high efficiency and wideband operation within a small form factor. In a transceiver system, the power amplifier is the most dissipative module, which consumes power from the system's battery. Hence, in order to extend the battery life in portable devices, it is imperative to design a power amplifier that demonstrates a high power efficiency [1–5]. Moreover, recently, the Federal Communications Commission (FCC) has also emphasized maximizing the battery life of the client device operating at the new unlicensed 6 GHz band (5.925 GHz to 7.125 GHz) [5]. Therefore, there is a crucial need for a 6 GHz power amplifier that exhibits high efficiency and thereby improves the battery life of the client device.

“Single-Transistor” PAs are desirable for 5G-mobile communications as they offer low-voltage operation, a small form factor, and a high power-added efficiency (PAE) if the PA is harmonically tuned. Moreover, the “single-transistor” approach incurs lower power consumption and, hence, naturally exhibits superior power efficiency over the multi-transistor approach (e.g., cascode or stacked, etc.). The term “single-transistor” means transistors are merged (shunted) in a parallel combination but are represented as one device in the circuit. “Single-transistor” integrated Class-F/F⁻¹ power amplifiers operable at “5G-millimeter-wave frequencies” have been investigated in recent years. However, an integrated “single-transistor” Class-F/F⁻¹ power amplifier operable at a “5G-microwave frequency” of 6 GHz has not been reported so far in the literature. A single-transistor millimeter-wave Class-F/F⁻¹ power amplifier in SiGe-BiCMOS was reported in [6]. This

power amplifier employed a wave-shaping network connected at the collector node of the active device, which allows it to transform from Class-F⁻¹ to Class-F when the frequency shifts from 24 GHz to 31 GHz. The amplifier was operating at 2.2 V and delivered 40.7% PAE along with a gain of 10.3 dB and an output power of 17.1 dBm. Very recently, a 65 nm CMOS single-transistor Class-F power amplifier operable at 5G-millimeter-wave frequencies was reported in [7]. The 1.1 V driven power amplifier rendered 46.4% peak PAE, a power gain of 10 dB along with an output power of around 14.75 dBm. To the best of the author’s knowledge, this paper reports the first “single-transistor” integrated Class-F⁻¹ power amplifier operable at a “5G-microwave frequency” of 6 GHz. The amplifier is designed in 65 nm CMOS technology. The proposed design employs a “parasitic-aware” Class-F⁻¹ harmonic control network connected at the drain terminal of the NMOS device. There are several Class-F⁻¹ circuit topologies based on the LC network [6–10]; however, the proposed Class-F⁻¹ LC-network is a new topology deduced using a novel iterative algorithm. A dual-purpose output matching network is incorporated in the design, which reinforces the waveform-shaping capability of the Class-F⁻¹ harmonic network along with performing the typical task of output impedance matching. The proposed amplifier offers one of the highest PAEs (47.8%) compared to many other monolithic microwave/millimeter-wave CMOS and SiGe power amplifiers reported so far.

This paper is organized as follows. Section 2 describes the details of the Class-F⁻¹ amplifier’s circuit topology, which includes a harmonic control network and dual-purpose output matching circuit. Moreover, the section also explains in detail the iterative algorithm employed to extract the component values of the harmonic network. Measurement results and a comparison table are reported in Section 3. Finally, Section 4 concludes the work presented in this paper.

2. Single-Transistor Class-F⁻¹ Power Amplifier

Figure 1 shows the proposed Class-F⁻¹ PA using a “single-transistor” approach, implemented in 65 nm TSMC CMOS technology. The active device in the design employs an NMOS transistor M₁. The total width of the device (W_T) is 384 μm, which is divided into six power-cell units. Each power-cell unit contains 32 fingers (N_f), and each finger is 2 μm wide (W_f). The amplifier is biased, with a drain supply V_{DD} of 1.1 V and gate supply V_{GG} of 480 mV. A 5 Ω resistor (R_g) and a small inductor (L_s) are incorporated, respectively, at the gate and at the source of the transistor for the purpose of establishing unconditional stability for the power amplifier.

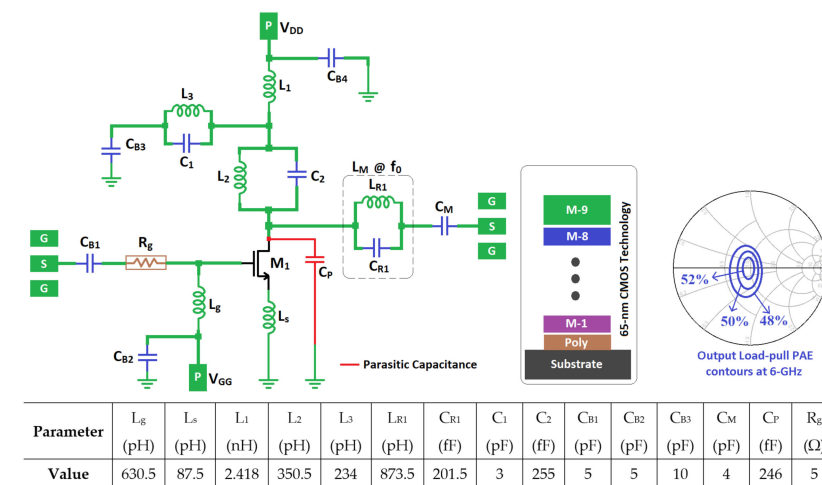


Figure 1. Circuit diagram of the proposed “single-transistor” Class-F⁻¹ PA in TSMC 65 nm CMOS and its load-pull PAE contours at 6 GHz. The figure also shows the BEOL stacked metal layers of the technology with color-coded scheme (reflecting the corresponding components in the schematic), as well as the values of the component parameters.

The drain terminal is loaded with a novel “parasitic-aware” Class-F⁻¹ harmonic control network, which harvests the parasitic capacitance C_P (246 fF) in its implementation. The parallel resonant tank (L_2, C_2) behaves as an inductor at the fundamental frequency f_0 , and combines its inductance with L_1 to tune out the parasitic capacitance C_P . However, the tank circuit (L_3, C_1) resonates at f_0 to create an open circuit, and, hence, does not interrupt the fundamental frequency’s path to resonate out the C_P . At the second harmonic frequency $2f_0$, the resonant tank (L_2, C_2) acts again as an inductor, which resonates out the parasitic capacitance C_P . However, the tank circuit (L_3, C_1) becomes overall capacitive at $2f_0$ and constitutes a low impedance path to the ground, thereby discarding the presence of the inductor L_1 and leaving the second harmonic to resonate with the remaining circuit, whereas at $3f_0$, the tank (L_2, C_2) becomes capacitive and constitutes a series LC resonant circuit with the inductor L_1 resulting in the formation of a short circuit path to the AC ground. A second short circuit path for the third harmonic is also established by the tank circuit (L_3, C_1), which behaves as an overall capacitor, thus dumping $3f_0$ into ground. Hence, with the help of this passive frequency-steering the employed harmonic network accomplishes the requirements for Class-F⁻¹ loading.

In order to determine the values of the inductors (L_1, L_2) and the capacitor C_2 , a novel “educated” and deterministic iterative technique is employed. It begins by inserting an incremental capacitance value, ΔC in (1) in each k^{th} iteration step of contiguous steps and then executing and validating a sequence of equations in a loop to finally extract the required reactive component values. The following equations are loaded in MATLAB in a routine and then the values of the components C_2, L_1 , and L_2 are extracted instantly at the end of the iterative search.

$$C_2 = [\Delta C]_k + C_P \quad (1)$$

where $[\Delta C]_k$ is an incremental value in fF (such as 1fF, 3fF, 7fF, etc.) at the k th step, with $k = 1, 2, 3 \dots n$. Additionally, in the equations below, f_{1o}, f_{2o} , and f_{3o} are the fundamental, 2nd and 3rd harmonics of the 6 GHz microwave center frequency, while f_{0R}, f_{2R} , and f_{3R} are the calculated resonance frequencies in each iteration. In addition, $L_{eq@2f_0}$ and $X_{Leq@2f_0}$ are, respectively, the required equivalent inductance and the corresponding inductive reactance of the parallel resonant tank (L_2, C_2) to tune out C_P at the 2nd harmonic. Further, $X_{Ceq@3f_0}$ and $C_{eq@3f_0}$ are, respectively, the equivalent capacitive reactance and the corresponding equivalent capacitance of the tank (L_2, C_2) at the 3rd harmonic. Finally, $X_{Leq@f_0}$ and $L_{eq@f_0}$ are, respectively, the equivalent inductive reactance and the corresponding equivalent inductance of the tank (L_2, C_2) at the fundamental frequency. The parasitic “ C_P ” thus provides the starting “educated” search reference for C_2 , while L_1 and L_2 are found deterministically using C_2 . It is thus different from any “brute force” algorithm, which may employ roughly estimated trial values. Now, for this proposed iterative technique:

$$L_{eq@2f_0} = \frac{1}{(2\pi f_{2o})^2 C_P} \quad (2)$$

$$X_{Leq@2f_0} = 2\pi f_{2o} L_{eq@2f_0} \quad (3)$$

$$X_{C2@2f_0} = \frac{1}{2\pi f_{2o} C_2} \quad (4)$$

$$X_{L2@2f_0} = \frac{(X_{Leq@2f_0} X_{C2@2f_0})}{(X_{C2@2f_0} + X_{Leq@2f_0})} \quad (5)$$

$$L_2 = \frac{X_{L2@2f_0}}{2\pi f_{2o}} \quad (6)$$

$$f_{2R} = \frac{1}{2\pi \sqrt{L_{eq@2f_0} C_P}} \quad (7)$$

$$X_{L2@3fo} = 2\pi f_{3o} L_2 \quad (8)$$

$$X_{C2@3fo} = \frac{1}{2\pi f_{3o} C_2} \quad (9)$$

$$X_{Ceq@3fo} = \frac{(X_{L2@3fo} X_{C2@3fo})}{(X_{L2@3fo} - X_{C2@3fo})} \quad (10)$$

$$C_{eq@3fo} = \frac{1}{(2\pi f_{3o} X_{Ceq@3fo})} \quad (11)$$

$$L_1 = \frac{1}{(2\pi f_{3o})^2 C_{eq@3fo}} \quad (12)$$

$$f_{3R} = \frac{1}{2\pi \sqrt{L_1 C_{eq@3fo}}} \quad (13)$$

$$X_{L2@fo} = 2\pi f_o L_2 \quad (14)$$

$$X_{C2@fo} = \frac{1}{2\pi f_o C_2} \quad (15)$$

$$X_{Leq@fo} = \frac{(X_{L2@fo} X_{C2@fo})}{(X_{C2@fo} - X_{L2@fo})} \quad (16)$$

$$L_{eq@fo} = \frac{X_{Leq@fo}}{2\pi f_o} \quad (17)$$

$$L_T = L_1 + L_{eq@fo} \quad (18)$$

$$f_{0R} = \frac{1}{2\pi \sqrt{L_T C_P}} \quad (19)$$

Since the parameters $C_P = 246$ fF (captured through parasitic extraction incorporating the transistor's parasitic capacitance (C_{ds}) plus parasitics associated with the layout interconnects), $f_{1o} = 6$ GHz, $f_{2o} = 12$ GHz, and $f_{3o} = 18$ GHz are known, they are used to extract the required component values by employing the above iterative technique.

It can be seen from the above equations and Table 1 that the required resonance conditions at the 2nd and 3rd harmonics (f_{2R} and f_{3R}) are automatically in agreement, and satisfaction of the resonance condition at the fundamental, f_{0R} , is the validating parameter in this iterative component extraction method. For the first three iteration values of ΔC , the deduced reactive components resonate close to f_{0R} , but for the last iteration value of $\Delta C (=9$ fF), f_{0R} comes exactly to 6 GHz thereby completing the component search. It can be noted that the proposed algorithm starts from a specific reference value and quickly converges to the solution, as shown in the table. It is judiciously designed around a single parameter, i.e., a parasitic capacitance, and, hence, is different from other optimization algorithms, which perform a search based on arbitrary values of the various parameters.

Table 1. Comparison of results extracted by the iterative technique.

ΔC (fF)	C_2 (fF)	L_1 (nH)	L_2 (pH)	f_{3R} (GHz)	f_{2R} (GHz)	f_{0R} (GHz)
1	247	2.80	357	18	12	5.66
2	248	2.75	356	18	12	5.7
5	251	2.59	354	18	12	5.8
9	255	2.42	351	18	12	6.0

Determining the component values of the tank circuit (L_3, C_1) constitutes a separate sub-problem and have been evaluated for resonance at f_0 and for equivalent capacitive

AC-bypass to ground at $2f_0$ and $3f_0$. Hence, setting C_1 to a suitable value of 3 pF, L_3 can be easily deduced as follows:

$$L_3 = \frac{1}{(2\pi f_0)^2 C_1} = 234 \text{ pH} \quad (20)$$

For the purpose of satisfying the Class-F⁻¹ condition, the output-matching network also has to present an open-circuit to the second harmonic so that this harmonic would reflect back towards the drain of the active device. A simple output-impedance matching can be established by just using the two components, inductor L_M and capacitor C_M ; however, in order to stop the second harmonic from propagating towards the load, a simple technique is employed. In this technique, the inductor L_M (1.165 nH) is judiciously decomposed into a $2f_0$ -tank circuit by employing the design equations below:

$$L_{R1} = \frac{3}{4} L_M = 873.75 \text{ pH} \quad (21)$$

$$C_{R1} = \frac{1}{4\omega_0^2 L_{R1}} = 201.5 \text{ fF} \quad (22)$$

The above-mentioned design equations can be used to convert any inductor into a $2f_0$ -tank-circuit. The tank-circuit (L_{R1} , C_{R1}) offers an open-circuit to the second-harmonic and behaves as the inductor L_M at the fundamental. Hence, the proposed output-matching network adds the second harmonic content at the NMOS drain terminal. This causes further refinement in the voltage waveform, resulting in a reduction in the current–voltage overlap and, hence, improving the power-added efficiency.

The proposed Class-F⁻¹ harmonic control network, along with the dual-purpose output-matching network connected at the drain of the NMOS transistor, performs the desired wave-shaping operation as shown in Figure 2. The voltage waveform approximates itself as a half-sinusoidal wave as the second harmonic content is dominant, whereas the current waveform is approximating itself as a square wave due to the higher third harmonic content (Figure 3). Load impedance observed from the drain terminal of the NMOS device (Figure 4) maintains a constant impedance close to the optimum value of 50 Ω at the fundamental frequency (f_0). The impedance trace depicts a high impedance at the second harmonic frequency ($2f_0$) and low impedance at the third harmonic frequency ($3f_0$). The input impedance matching is realized with the help of a DC-blocking capacitor, C_{B1} , as shown in Figure 1. The output load-pull simulations of the power amplifier offer around 52% peak PAE at 6 GHz, as indicated by the contours on the Smith chart in Figure 1.

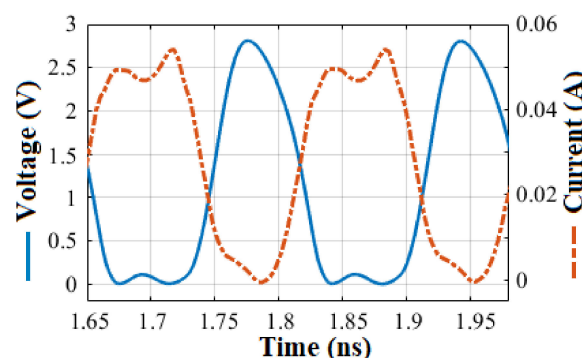


Figure 2. Voltage and current waveforms at the drain of the NMOS device.

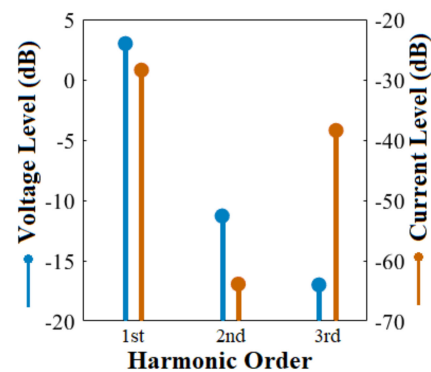


Figure 3. Voltage and current spectrum up to the 3rd harmonic frequency.

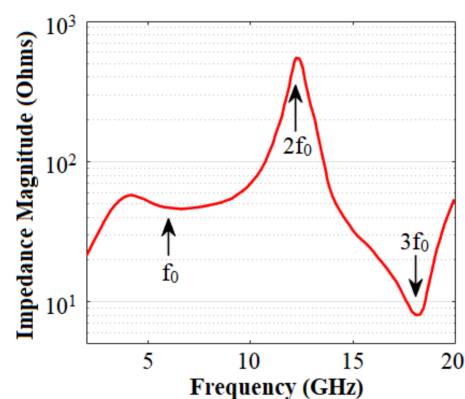


Figure 4. Impedance trace as a function of frequency.

3. Measurement Results

Figure 5 shows the photomicrograph of the implemented power amplifier employing the 65 nm TSMC CMOS process with a PA size of $753 \mu\text{m} \times 927 \mu\text{m}$. A Cascade Micro-Tech Summit 11K probe-station along with infinity-quad-probe (50 GHz RF and 100- μm pitch) and a Rohde & Schwarz ZVA50 Vector Network Analyzer employed for on-wafer testing, as shown in Figure 5. Standard SOLT calibration was performed for the purpose of on-wafer small-signal S-parameter measurements with the results shown in Figure 6. The measured S_{11} and S_{22} values are under -10 dB for a considerable range of frequencies of interest. The measured maximum S_{21} was 14.1 dB along with a -3 dB range of 3.67–7.4 GHz, thus offering a 3.7 GHz wide small-signal bandwidth ($\text{BW}_{3\text{dB}} = 67.4\%$). Stability analysis reveals that the amplifier's stability factor (k) is greater than 1, as shown in Figure 7, ensuring unconditional stability of the proposed power amplifier.

Large signal measurements were conducted with the help of a power meter and power sensors. The measured results captured at the operating frequency of 6 GHz are shown in Figure 8. The amplifier exhibits a peak power-added efficiency (PAE) of 47.8%, saturated output power, P_{SAT} , of 14.4 dBm and, a power gain of 13.8 dB. The output power at the 1 dB compression point, $\text{OP}_{-1\text{dB}}$, is 12.9 dBm. Figure 9 shows the measured PAE traces from 5 GHz to 7 GHz with respect to the input power. P_{OUT} stays above 12 dBm from 3.5 GHz to 7.5 GHz, whereas PAE remains higher than 30% from 4 GHz to 7.5 GHz, as shown in Figure 10. Normalized AM–AM and AM–PM distortion curves are depicted in Figure 11. The measured AM–PM distortion at $P_{\text{in}, -1\text{dB}}$ (6 dBm) is less than 2° , indicating good linearity performance.

Table 2 compares the proposed PA with several previously reported PAs in CMOS and SiGe. It can be easily inferred from Table 2 that the proposed amplifier yields the highest peak PAE (47.8%) as compared to the referenced papers. According to the author's knowledge, there are no "single-transistor" integrated microwave Class-F/ F^{-1} PAs that have been reported so far; however, two millimeter-wave Class-F/ F^{-1} PAs with similar

“single-transistor architecture” have been reported, and these have been included in the table, although they are in a totally different RF spectrum compared to the other PAs in the table. The proposed PA offers a very high efficiency and operationwise reasonable output power. The saturated output power of 14.4 dBm resides within the designated power limits outlined by the FCC [5] for establishing 5G communications at 6 GHz. Moreover, this power level helps to extend the client device battery life as well. Table 2 also shows that when compared to other 6 GHz power amplifiers, the proposed PA offers low-voltage operation (1.1 V) and small form factor.

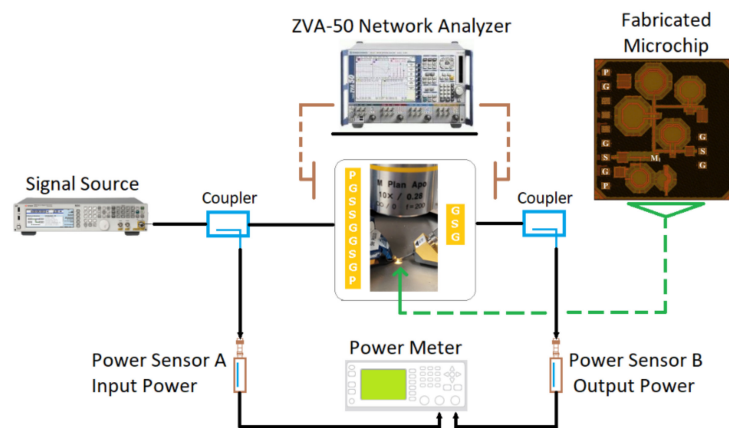


Figure 5. Chip photomicrograph of the fabricated 65 nm CMOS Class-F⁻¹ PA and Cascade Microtech Summit 11K Probe-Station test set-up.

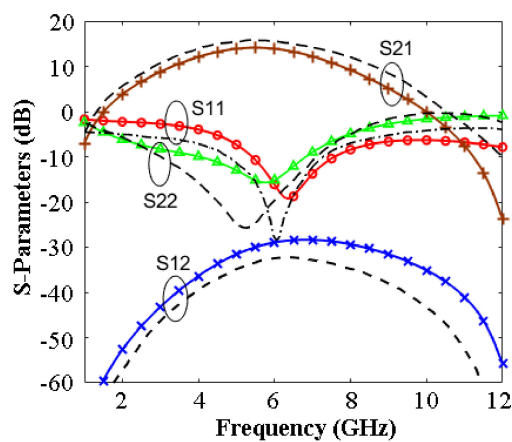


Figure 6. Simulated (black dotted) and measured (colored solid) traces of S-parameters for the fabricated PA.

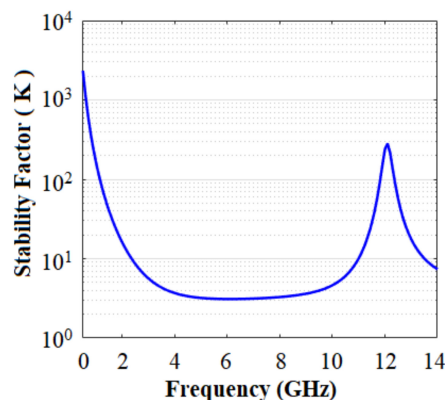


Figure 7. Stability curve.

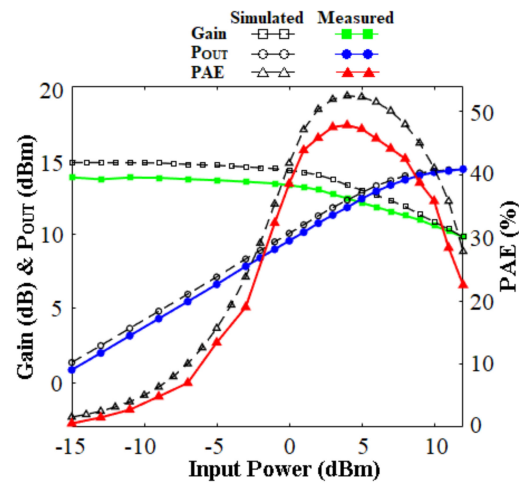


Figure 8. Simulated and measured performance parameter traces for the proposed PA: output power, gain, and PAE versus input power.

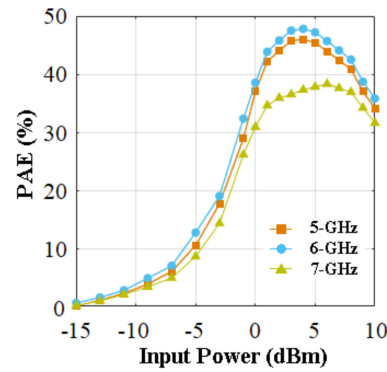


Figure 9. Measured PAE traces at different frequencies.

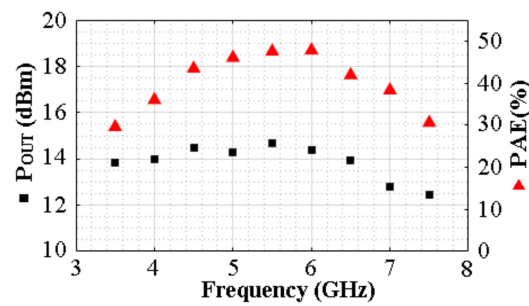


Figure 10. Measured PAE and output power traces versus frequency for the fabricated Class-F⁻¹ PA.

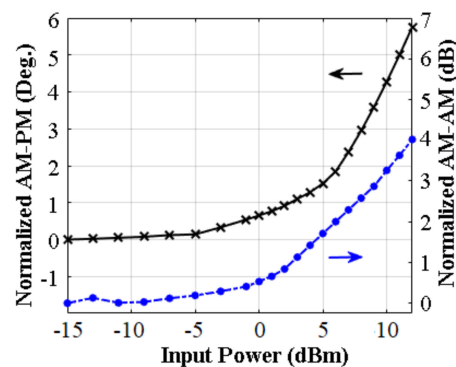


Figure 11. Measured AM-AM and AM-PM distortion across input power.

Table 2. Comparison of recently reported CMOS and SiGe-BiCMOS PAs.

Referenced Work	Process Technology	Architecture	Amplifier's Class	Freq. (GHz)	Gain [dB]	P _{SAT} [dBm]	Peak PAE (%)	Supply Voltage (V)	Area on-Chip (mm ²)
This Work	65 nm CMOS	Single Transistor	Class-F ⁻¹	6	13.8	14.4	47.8	1.1	0.69
[6]	130 nm SiGe	Single Transistor	Class-F ⁻¹ /F	31	10.3	17.1	40.7	2.2	0.27
[7]	65 nm CMOS	Single Transistor	Class-F	29	10	14.75	46.4	1.1	0.12 * ¹
[11]	180 nm CMOS	Cascode Stages	Class-F ⁻¹	4.6	11.6	27.8	32	3.6	2.32
[12]	65 nm CMOS	Differential	Class E/F	6	N/A	25.6	34 * ²	1.8	9.03
[13]	250 nm SiGe	Push-pull Stages	Class AB	6	12	24	24.7	1.8	2.08
[14]	65 nm CMOS	Differential	Class AB	6	23.6	22.4	28.4	3.3	0.89
[15]	65 nm CMOS	Differential Cascode	Class AB	6	19.4	18.9	27.9	3	0.73 * ³

*¹ Area without pads (active area); *² drain efficiency; *³ circuit is not fully integrated (output matching network is off-chip); green shading: mmW PAs; blue shading: Single-Transistor.

4. Conclusions

A highly power-efficient Class-F⁻¹ PA for 5G communications at 6 GHz, employing a “single-transistor” design implemented in 65nm CMOS, is proposed. The amplifier employs an iterative algorithm based parasitic-aware harmonic control network along with a dual-purpose output-matching network. The amplifier offers a low-cost, low-voltage driven, area-constrained, wideband, and a highly power-efficient PA for establishing 5G communications at 6 GHz.

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References

- Grebennikov, A.; Raab, F.H. History of Class-F and Inverse Class-F Techniques: Developments in High-Efficiency Power Amplification from the 1910s to the 1980s. *IEEE Microw. Mag.* **2018**, *19*, 99–115. [CrossRef]
- Vasjanov, A.; Barzdenas, V. A Review of Advanced CMOS RF Power Amplifier Architecture Trends for Low Power 5G Wireless Networks. *Electronics* **2018**, *7*, 271. [CrossRef]
- Kouhalvandi, L.; Ceylan, O.; Ozoguz, S. A Review on Optimization Methods for Designing RF Power Amplifiers. In Proceedings of the 2019 11th International Conference on Electrical and Electronics Engineering (ELECO), Bursa, Turkey, 28–30 November 2019; pp. 375–378. [CrossRef]
- Gao, S. High-efficiency class-F RF/microwave power amplifiers. *IEEE Microw. Mag.* **2006**, *7*, 40–48. [CrossRef]
- Federal Communications Commission. (2020, Apr. 2), FCC Fact Sheet: Unlicensed Use of the 6-GHz Band. Available online: <https://docs.fcc.gov/public/attachments/DOC-363490A1.pdf> (accessed on 6 April 2020).
- Mortazavi, S.Y.; Koh, K.-J. 14.4 A Class F⁻¹/F 24-to-31 GHz power amplifier with 40.7% peak PAE, 15 dBm OP_{1dB}, and 50 mW Psat in 0.13μm SiGe BiCMOS. In Proceedings of the 2014 IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC), San Francisco, CA, USA, 9–13 February 2014; pp. 254–255.
- Ali, S.N.; Agarwal, P.; Gopal, S.; Mirabbasi, S.; Heo, D. A 25–35 GHz Neutralized Continuous Class-F CMOS Power Amplifier for 5G Mobile Communications Achieving 26% Modulation PAE at 1.5 Gb/s and 46.4% Peak PAE. *IEEE Trans. Circuits Syst. I: Regul. Pap.* **2019**, *66*, 834–847. [CrossRef]
- Mortazavi, S.Y.; Koh, K.-J. Integrated Inverse Class-F Silicon Power Amplifiers for High Power Efficiency at Microwave and mm-Wave. *IEEE J. Solid-State Circuits* **2016**, *51*, 2420–2434. [CrossRef]

9. Mortazavi, S.Y.; Koh, K.-J. A 28-GHz inverse class-F power amplifier with coupled-inductor based harmonic impedance modulator. In Proceedings of the 2015 IEEE Custom Integrated Circuits Conference (CICC), San Jose, CA, USA, 28–30 September 2015; pp. 1–4.
10. Ali, S.M.A.; Hasan, S.M.R. A 38-GHz Millimeter-Wave Double-Stacked HBT Class-F⁻¹ High-Gain Power Amplifier in 130-nm SiGe-BiCMOS. *IEEE Trans. Microw. Theory Tech.* **2020**, *68*, 3039–3044. [[CrossRef](#)]
11. Chen, F.; Wang, Y.; Hsiao, Y.-H.; Lin, J.-L.; Chen, Y.-C.; Wang, H. A 4.6-GHz Class-F–1 high power CMOS power amplifier. In Proceedings of the 2017 IEEE International Symposium on Radio-Frequency Integration Technology (RFIT), Seoul, Korea, 30 August–1 September 2017; pp. 183–185. [[CrossRef](#)]
12. Wang, H.; Hashemi, H. A 0.5–6 GHz 25.6 dBm fully integrated digital power amplifier in 65-nm CMOS. In Proceedings of the 2014 IEEE Radio Frequency Integrated Circuits Symposium, Tampa, FL, USA, 1–3 June 2014; pp. 409–412.
13. Gruner, D.; Boeck, G. Fully integrated 5.6–6.4 GHz power amplifier using transformer combining. In Proceedings of the 2009 Ph.D. Research in Microelectronics and Electronics, Cork, Ireland, 12–17 July 2009; pp. 160–163.
14. Ye, W.; Ma, K.; Yeo, K.S. 2.5 A 2-to-6 GHz Class-AB power amplifier with 28.4% PAE in 65nm CMOS supporting 256QAM. In Proceedings of the 2015 IEEE International Solid-State Circuits Conference—(ISSCC) Digest of Technical Papers, San Francisco, CA, USA, 22–26 February 2015; pp. 1–3.
15. Lindstrand, J.; Tormanen, M.; Sjoland, H. A Decade Frequency Range CMOS Power Amplifier for Sub-6-GHz Cellular Terminals. *IEEE Microw. Wirel. Compon. Lett.* **2020**, *30*, 54–57. [[CrossRef](#)]