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**Biomedical Integrated Circuit Design**  
**for**  
**An Electro-Therapy Device**

*A Thesis Presented in Partial Fulfilment  
of The Requirements for The Degree of*

**Doctor of Philosophy**

*in*

*Electronics and Computer Engineering  
(Bioelectronics)*

*at*

*School of Engineering and Advanced Technology  
Massey University, Albany Campus, New Zealand*

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**In the name of God**  
**Most Gracious, Most Merciful**

Dedication

To my parents, whose boundless love and belief in me, from the core of my being, empowered me to be the woman that I am.

To my lovely children and to my talented kids, Zain, Taim and Yoseph, whom are the light in my life.

**“Our Actions Today are The Future of The Human Being.”**

## **Abstract**

A biomedical integrated circuit design (IC) is utilized for the development of a novel non-invasive electro-therapy device, for low frequency multi-channel biomedical stimulation to transform immune activity and induce anti-viral state. Biomedical integrated circuit design is an important branch of modern electronic engineering that uses the application of electronic engineering principles for biomedical disciplines, to develop bioelectronics devices that are implanted within the body and for non-invasive devices to improve patient's lives. These devices use the application of an electric field to stimulate reactions to restore normal cell functions and activate the cells to treat a variety of disorders or disease conditions. Bioelectronics devices can be designed for use as alternative treatments to overcome the deficiencies of several conventional medical treatments. It could potentially assist as drug-free relief when therapeutic drugs become ineffective, costly, with serious side effects and cannot be replaced, loss of future treatment options, and hence, life threatening, as for drug resistant Human immunodeficiency virus (HIV-1) patients.

Since the underlying mechanisms of the biological system and disease state is dominated by electrostatic interactions, specifically, the interaction between HIV-1 and the host cell that is predominantly by electrostatic interactions (protein charge-charge interaction) has an important role in its life cycle replication. At given pulses, the charge distribution and polarization of the electro-active protein molecules takes place, inducing conformation change which can enhance immune activity and inhibit the interaction of HIV-1 and host cells, disturbing its life cycle, leading to the mechanisms of the inactivation signal-induced virus death. These electrically induced protein transformations is used in this research as blood-cell treatment and as anti-HIV-1 electrotherapy.

Advances in bioelectronics technology, which involve new CMOS IC design, and in bio-electrochemistry science, which include cellular function, electro-active biomolecules and their responses, have contributed to this project to develop the concept of a novel electro-therapy device, for biomedical treatment applications. This involves understanding of the underlying mechanisms of the biological system and disease condition from an electronic engineer's point of view as well as the interface



between the electronic signal and the biological cells, and how electronic devices and circuitry directly communicate with the electro-active body tissue and blood cells.

This research project addresses the design and development of a novel energy-efficient miniature biomedical device using a new CMOS technology. It can generate, deliver and control an appropriate periodical low frequency electrical pulses, through the low-resistance skin surface to a patient's blood. The notable feature of such a smart device is its cellular specificity: the parameters of the generated electrical pulse which are designed and selected in order to stimulate only one particular type of tissue (blood) leaving the others unaffected. The device comprises a mixed-signal low power dual-band waveform generator (WFG) chip along with a novel two band tuning system. It was fabricated using Global Foundries (GF) 8RF-DM 130-nm CMOS process with a supply voltage of  $\pm 1\text{V}$  for the analog circuit and  $+1\text{V}$  for logic circuits. The WFG core (band I) can be tuned in the range 6.44 kHz - 1003 kHz through bias current adjustment, while a lower frequency (band II) in the range 0.1 Hz to 502 kHz can be provided digitally. Two WFG approaches, that comprise relaxation oscillators with different relaxation timing networks, have been developed for comparison.

Since the aim of this work is to transfer electrical signal in a specifically controlled fashion through the tissue, a novel low power active electrode-pair signal delivery system, compatible with human skin with high signal integrity, is developed. The circuit was fabricated in a 130-nm CMOS process using a low supply-voltage of  $+1.2\text{V}$  to deliver bi-phase square waveform signals from 16 selectable low-frequency channels. The individual active electrode can also be used to deliver mono-phase square/triangular waveform output signals. Accuracy, safety, low power, light-weight, miniature and low-cost characteristics are the main concerns. Being a miniature bioelectronics component with low power consumption, the proposed device is suitable both as a non-invasive and as an implantable biomedical device, in which WFG and electrodes circuitry can communicate with the electro-active biomolecule, strongly stimulating certain events in a complex biological system.

A theoretical analysis, experiment design and performance are carried out in in-vitro environments to examine the effect of the designed signal on human blood cellular proteins. Proteins that display a heterogeneous structure have various conductivities and permittivity (determining the interaction with the electrical field) and possess dielectric properties with a large conformation change, undergoing structural rearrangements in

response to cellular signals. The frequency-dependent dielectric present in proteins involves the redistribution and alignment of the proteins charged molecule and its polar molecule in response to an applied external electrical field can also induce conformation change. Interference polarization within proteins could interrupt the interaction between both sides of predominantly host cell proteins and of the HIV-1 infective envelope and its protein particles. This could disturb the signalling proteins for cell activation, and, hence, the virus cannot conjugate with the target cells and control the host cell protein activity. Since the virus is unable to reproduce out of a host cell, hence the virus cannot mutate and develop resistance easily, and use alternative binding and entry mechanisms as in the pharmacological approaches. After carefully studying the interaction of the HIV-1 virus and the host cell, with respect to signal transfer, CD4 receptor, co-receptors CCR5 and nuclear transport factor nucleoporins FG Nup153 proteins of the lymphatic system, which are essential targets for HIV-1 infection and its life cycle replication represent an attractive target to investigate in this research project. The activities of the underlying mechanism of the target cell are then examined utilizing immunofluorescence microscopy technique with specific fluorescent labelled antibodies, and accurate results are obtained with relatively low cost. The results demonstrated that the low frequency electrical pulse could inhibit virus attachment and fusion. It is also could provide a permeability barrier, that prevents the import and export of large macromolecule virus particles through the nuclear pore complex. These effects could induce an antiviral state for a period of time, and stop HIV-1 virus replication, with no potential risks and harm to the host cells, compared to the common drugs. This is promising for the conception of HIV-1 treatment in vivo. Although further investigations are required in order to fully use the application of electrical stimulation in vivo for treatment, the result is provides the necessary impetus for the applications of low frequency electrical stimulation on human immune response. This might offer important antiviral therapy against the most devastating pathogens in human history.

This doctoral research is not only of academic interest but also highly relevant to medical applications. It is considered potentially beneficial in the development of knowledge in advanced technology for electro-medical treatment devices, their design, structure and applications to extend life, and for future growth in the biotechnology industry, therefore beneficial for the patients, physicians and for humanity.

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## **List of Abbreviations**

AA	Amino Acid
Ab	Antibody
D	Aspartic Acid
BJT	Bipolar Technology
BSA	Bovine Serum Albumin
CCII	Current Conveyor
CFOA	Current Feedback Operational Amplifier
Clk	Clock
Clk_bar	Clock_bar
CM	Current-Mode
CSE	Clocked Storage Element
D-FF	D-Flip Flop
DRC	Design Rule Checking
ELF	Extra Low Frequency
FBS	Fetal Bovine Serum
FD	Frequency Divider
FF	Flip Flop
FG	Phenylalanine-Glycine
h	Hour
HCl	Hydrochloric acid
HIV-1	Human immunodeficiency virus
IC	Integrated Circuit
Kap	Karyopherin
LVS	Layout Versus Schematic
mAbs	Monoclonal Antibodies
min	Minute
MLF	Moderate Low Frequency
MUX	Multiplexer
NES	Nuclear Export Signal
NLS	Nuclear Localization Signal
nm	Nano-metric

NPC	Nuclear pore complex
Op-Amp	Operational Amplifier
OTA	Operational Trans-conductance Amplifiers
PFA	Paraformaldehyde
PG	Pass Gate
PIC	Pre-Integration Complex
PS	Path Selector
PVT	Process And Temperature Variation
Q	Glutamine
SC	Stratum Corneum
SDL	Schematic-Driven Layout
ST	Schmitt Trigger
STG	Stage
TG	Transmission-Gate
TGFF	Transmission-Gate Flip Flop
VTC	Voltage Transfer Characteristic
WFG	Waveform Generator
WFG <sub>INTG</sub>	Waveform Generator Based on Integrator Timing Network
Y	Tyrosine

## List of Symbols

$A$	Area	Meter Square
$C$	Capacitor	Farad
$C_{ox}$	Gate oxide capacitance	Farad
$g_m$	Trans-conductance	Microampere/microvolt
$W$	Channel width of the MOSFET	Micro-meter
$L$	Channel length of the MOSFET	Micro-meter
$r_o$	Output resistance of MOSFET	Ohms
$\mu_n$	Electron mobility	Meter square/Volts seconds
$I_B$	Bias Current of MOSFET	Microamperes
$I_D$	DC Drain current of MOSFET	Microamperes
$V_C$	Capacitor Voltage Output	Volts
$V_{DD}$	Positive Supply Voltage	Volts
$V_{INT}$	Integrator Voltage Output	Volts
$V_o$	Output Voltage	Volts
$V_{SS}$	Negative Supply Voltage	Volts
$V_{GS}$	Gate-source voltage of MOSFET	Volts
$V_{LTH-}$	Lower Threshold Voltage	Volts
$V_{ST}$	Schmitt Trigger Voltage Output	Volts
$V_{TH}$	Threshold voltage	Volts
$V_{UTH+}$	Upper Threshold Voltage	Volts
$V_{in}$	Input Voltage	Volts
$V_{sat-}$	Low Negative Saturation Level	Volts
$V_{sat+}$	High Positive Saturation Level	Volts
$R$	Resistor	Ohms
$P$	Power	Watts
$f$	Frequency	Hertz
$\tau$	Time constant	Seconds
$T$	Time Period	Seconds
$\omega$	Angular frequency	Radians per second

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# **Chapter 1**

## **Introduction**

### **1.1 Biomedical Integrated Circuit Design**

There is a growing demand for technological improvement in healthcare. There have been promising developments in Biomedical Integrated Circuit (IC) design for a variety of low-cost, and light-weight bioelectronics circuit solutions, for battery-operated biomedical devices. Biomedical integrated circuit design is emerging as a new field of study that is using the application of electronic engineering principles to develop concepts for biomedical disciplines. It is a very wide research subject that links engineering and biological sciences with medical science and which has practical importance in the design and development of effective energy-efficient bioelectronics circuit solutions to restore health, extend life as well as to provide solutions in the challenging biomedical device industry. These devices use the application of an electric field to stimulate reactions that restore normal cell functions and activate the biological cells to recover from a disorder or disease. This concept involves the interface between the electronic signal and the biological cells, and how electronic devices and circuitry directly communicate with the electro-active biomolecule system. Albert Szent-Gjorgyi was the first who coined the word “bioelectronics”. He showed in his two volumes: introduction to a Sub-Molecular Biology (1960), and Bioelectronics (1968) that all biological cells are electrically charged and have electronic properties comparable to electronic materials [1]. The biological system behaves like a biological microelectronics circuit that acts as a storage medium as in Deoxyribonucleic (DNA) molecules that store and process information by individual molecules. The biological system behaves like biological micro-sensors that possess a range of transducing sensitive systems to detect information about the state of their environment, like the human eye and ear. Furthermore, the biological system behaves like a biological microelectronics circuit that can deliver and control the direction of the electron and the ionic currents along pathways at molecular level by individual electro-active macromolecules. These biological system features can be considered as electronic systems due to their electronic characteristics and act as biological hardware and software that organize and process information [1, 2]. This is inspiring new electronic

engineering design for investigating the electro-active biological cell and developing smart electro-medical devices [3]. Since designing a suitable device for electro-medical treatment depends on the condition of the disorder or disease, understanding the biological system features and the disease conditions, from an electronic engineer's point of view, is therefore, essential and potentially beneficial to assist the designer in developing the required electro-medical treatment devices, using the application of an electric field for medical treatment. The application of an electric field for electrotherapy is considered one of the oldest medical treatments since Ancient Greece and the most important documented medical therapies recognized by scientists [4, 5]. It is potentially useful as drug-free relief and overcomes the deficiencies of several conventional medical treatments. It has potential for treating a variety of chronic diseases that have significant social and economic effects. It may assist when therapeutic drugs become useless and cannot be replaced, as in untreatable diseases like cancers and Human immunodeficiency virus that develop drug resistance.

Currently, many biomedical engineering, and medical researchers around the world are using electronic characteristics of biological materials to develop devices that employ electrical stimulation as an effective medical therapy. In modern clinical treatments there are several electro-medical devices that utilize the electrically conductive body medium with the application of electrical fields to improve patients' lives, using either old or new technology for devices that are implanted within the body, and also for non-invasive devices. To our knowledge, both types of devices are important in design considerations for electro-medical treatment. Various electronic devices that are implantable inside the body are developed and have sufficiently enhanced the methods of applying electrical stimulation with no risk. An example is Deep Brain Stimulation (DBS), which delivers electrical current signal to stimulate certain region in the brain, [6]. A microelectronic circuit or a brain implant that is fixed inside the skull under the skin, to make direct contact with the brain surface, transmitting electrical signals that reactivate a paralyzed member in patients with Parkinson' disease, can improve their quality of life [7]. The sub-retinal implantable prosthesis and implantable electrical stimulator for a cochlear prosthesis, which are based on human eye and ear function respectively, use the application of electrical fields, as in the artificial retina implant inside the eye, which produces and sends electrical impulses to the brain to enhance the vision ability [8], and in an optical device

fixed inside the eye as a retina implant to electrically stimulate the cells of the eye which is successfully bringing vision to blind people who have genetic retinal degeneration [9]. Programmable multichannel stimulators based on electrical stimulation of the auditory nerve in the cochlear region are used for cochlear implant prosthesis in deaf patients to recover hearing sensation [10]. Today, more than 130,000 deaf people in the world are using a cochlear implant which allows them to hear normally [3]. Design techniques to provide electrical signals are also used in the cardiac pacemaker system for cardiac activity to improve a patient's heart's rhythms. It has become a remarkably important treatment technique for a slow heart rate [11, 12]. The design of implantable biomedical devices that use the application of electrical stimulation is not limited to the brain, eye, ear, and heart areas. Implantable electrical stimulation devices have been also used for intravesical electrical stimulation (IVES) in diagnosis and treatment of lower urinary tract dysfunction, to enhance bladder sensation and to improve bladder contractility in patients with impaired bladder emptying [13]. Today, implantable electrical stimulation devices are used for vestibular implants to treat balance disorders, brain implants to treat speech disorders, and implants for treating urinary incontinence [3]. Moreover, in a new area of implants, electrical stimulation devices are being developed for the treatment of immune inflammatory disorders of the vagus nerve [14].

The concept of various non-invasive biomedical devices, that only contact the body's cells by using an external electrode, can also be developed for electrical stimulation treatment. These devices use an electrode and the conductivity of the patient's skin cells to communicate, such as sensors for monitoring body's activities, and as in a device that delivers a direct electrical signal onto a patient to stimulate reactions that can heal various pains or disorders and for disease treatment. This can be achieved by treating local inflammation and stimulating muscles, increasing blood flow, and activating natural hormones in the body. An example is a non-invasive transcranial current stimulation, a brain stimulation modality that uses the application of electric fields with a weak electric current, using a pair of electrodes. It is a promising application in modulating brain activity for treatment of brain disorders [15]. Non-invasive transcutaneous electrical nerve stimulation (TENS) utilizes surface electrodes over the posterior tibial nerve which was used for treatment of an overactive bladder (OAB) symptoms [16]. Recently, electrical stimulation to induce the electroporation

effect, has been used for breast cancer therapies when conventional treatments become useless or costly, with serious side effects, and for chemo-resistive patients. This technique specifically controls electric fields of short duration and high intensities, to open up transient pores (aqueous pathways) through semi-permeable membranes and tissues, allowing targeted delivery of therapeutic materials including drugs, antibodies, and genes [17]. Nanosecond pulsed electric field (nsPEF) technology is also used to treat skin cancer in humans. The effects of nsPEF therapy are highly localized to only the cells located between suction electrodes, while tissues outside the edge of the suction electrode show no effects from the therapy [18]. These types of biomedical devices based on electrical stimulation therapy, were approved by America's Food and Drug Administration (FDA) as a standard method for medical treatments, which exist in the market.

The requirement for both types of device is to develop an appropriate biomedical electrical circuit solution for each particular electro-medical treatment device. In both types of smart devices however, it is necessary to generate and deliver an appropriate electrical signal with specific waveform and frequency, to be applied internally or externally to a particular area of the body. Waveform generators (WFG) and electrodes circuitry can communicate with the electro-active biomolecule, highly stimulating certain events arising in a complex biological system. The design of WFG, as well as electrodes, therefore, has become important in a wide range of biomedical signal processing systems. These devices must be portable, miniaturized, adaptable, safe, secure, reliable, operate with low power battery and low cost. Examples of the development of implantable and non-invasive biomedical devices that utilize waveform generators as discussed in this section are summarized in Figure 1.1. Such devices should be accurate, and take into account the interference between biological materials and the device elements. This can be assured by monitoring the biological activities and the responses, with application of an electrical field. These devices must operate at low voltage and be safe to use without exceeding the health safety standards of the International Commission on Non Ionizing Radiation Protection (ICNIRP) and the U.S. Federal Communication Commission (FCC) standards state that human exposure must be restricted to lower levels of electric field [19].



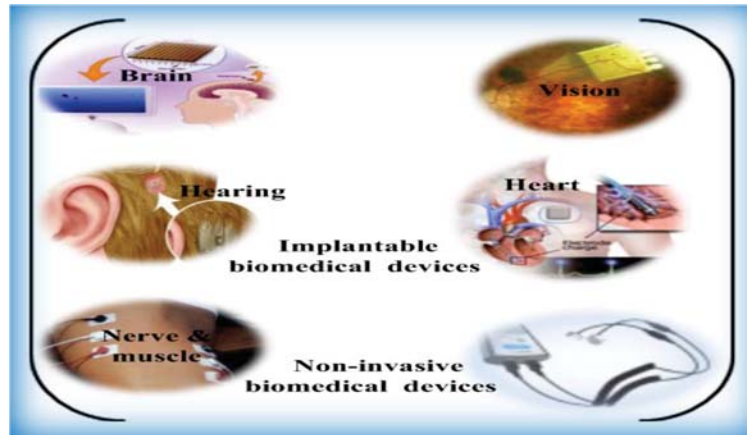


Figure 1.1. Schematic diagram representing the development of a variety of implantable and non-invasive biomedical devices in the real world. These devices use the application of an electric field with an appropriate electrical signal and specific frequency to be applied internally or externally to a particular area of the body, to treat a variety of disorders or disease conditions, and to improve patients' lives [3][7][9].

The applications of biomedical integrated circuits (IC) design are promoted and increase every day. CMOS (Complementary Metal-Oxide Semiconductor) technology is used widely today to design small-size and low-power consumption biomedical devices. This research project addresses the design and development of a smart non-invasive battery operating biomedical device, using a new 130 nanometer (nm)-CMOS technology for bio-electrical treatment which can generate, control and deliver a periodical low frequency bipolar square waveform signal and low voltage electrical field through the low-resistance skin surface to a patient's blood, to stimulate a reaction in order to hopefully treat body fluid related pathogens, particularly HIV-1. Given the massive burden of the illnesses on patients, it is necessary to develop novel alternative treatments that exceed the current pharmaceutical therapeutic approaches in terms of efficiency and safety. It can be used when conventional treatments become useless and costly, with serious side effects, and for drug resistive patients. Essentially, advances in bio-electro-chemistry science in understanding cellular function and response, as well as the heterogeneous structure of the proteins (which comprise various conductivities and permittivity, that determining the interaction with the electrical field), inspires the conceptual design of treatments based on a systematic consideration of the fundamentals of disease development. In particular, an interaction of the HIV-1 and

host cell proteins, that is dominated by electrostatic interactions, considered the main driving forces for the progress of the disease state, represents a desirable objective for such an approach. Therefore, this research project will introduce the underlying mechanism of the disease and outline a path that will combine bio-electrochemistry science at the molecular level, engineering principles and medical science to advance functional design in vitro as a promising foundation and value for the establishment of HIV-1 treatment in vivo.

## **1.2 Relevance**

Today, health care issues demand concern all around the world. It is an area that involves private and public sectors with significant social and economic impacts. Good health is essential for carrying out the basic daily life tasks through to the development of nations. The development of societies is evaluated according to the health of their people, because health is a balance between people and their environment. People with illness or chronic pain may struggle to participate and communicate with others in everyday life. This may occur in both chronic illness and unexpected disease which can be an enormous psychological burden and can cause serious handicaps, especially if the disease causes feebleness or death in human and in economically important animals. The impact of such disease is measured by financial cost, mortality and morbidity. Pathogenic disease is considered the greatest cause of death, and kills millions of people worldwide every year, more than all other diseases [20-23]. Most pathogenic diseases are infectious and caused by a micro-organism such as fungi, bacteria, and viruses, which affects the normal physiological functions by causing dysfunction or tissue damage. However, there are different types of pathogenic disease around the world which need significant consideration.

The major three pathogenic diseases that cause about half of all deaths in the world are tuberculosis (TB), malaria and AIDS. These diseases pose a continuous threat globally, because of increased immigration and travel. HIV-1 and TB are also multidrug resistant and because of co-infection of HIV-1 with TB and it is one of the risk factors for development of cancer in humans that increases death rates annually for the next 10 years [20]. In 2010, it was estimated that 34 million people were living with HIV-1, 3 million people were diagnosed with HIV-1 infection and 2 million people had died from

AIDS [21]. Thus it can be concluded that HIV-1 disease can be a significant economic burden including healthcare-associated infections (HAI) and costs involving hospital, nursing, laboratory and diagnostics, investigations, medical treatment, outbreaks of disease and infection prevention, time and loss of production. In United States, the cost burden for HAI is between about 25.0 and 31.5 billion dollars per year. In English hospitals, it was estimated at 1.6 billion dollars which is 1% of the total national hospital budget. The global goal is to prevent and treat disease, to reduce the disease burden. Many health organizations such as the World Health Organization (WHO) and Centre for Disease Control and Prevention (CDC) are organizing and monitoring many treatment programs and have developed a strategy for the 21st Century that improves the people's health, to reduce the chronic disease death rates annually for the next 10 years, by 2%. The four major goals of the CDC are: a) surveillance and response, b) applied research, c) infrastructure and training, and d) prevention and control. Achieving these goals will assist in treating pathogenic disease, particularly HIV-1 now, and preventing it tomorrow [22, 23].

### **1.2.1 Virus Replication**

HIV-1 is a retrovirus which develops slowly in the human cells (T lymphocytes) over years. The structure of the HIV-1 has a capsid (core) made up of subunit icosahedral protein segments to form virus shapes. Its core contains two copies of RNA genome coated with nucleocapsid proteins and the important enzymes for HIV-1 replications. The life cycle of the HIV-1 virus however, is complex and involves many phases, so, its life cycle will not be reviewed in detail here; more details can be found in [21]. Only the part that is important for the concept of this research project will be covered in this research project (more details will presented in chapter 6). In general, the primary entry of the HIV-1 begins with attachment and binding of the virus's spike protein glycoproteins gp120 to the host cell CD4 surface receptor. CD4 expression on target cells is not sufficient for viral entry. HIV-1 requires a chemokine co-receptor, CCR5, in the early stages of infections, a protein that acts with CD4 to bind the virus's spike protein to the host cell membrane, enabling the HIV-1 envelope to fuse with the host cell plasma membrane, facilitating entry and releasing- its core in the cytoplasm. [24]. Conformation change of this co-receptor protein is the major mechanism that prevents the virus from binding onto the target host cell. In addition, CCR5 may be

involved in different stages of HIV-1 entry, and for replicative capacity. Thus co-receptor CCR5 plays a key role in the development of HIV-1 infections, and the lifecycle of the virus could be easily disturbed without CCR5 binding affinity [25]. After the fusion has occurred, the core of the virus, which includes the two RNA genomes and the important enzymes, is then released into the cytoplasm of the host cell.

The HIV-1 life cycle is accomplished by import and export and passage of their large molecules infecting viral particles' pre-integration complex (PIC) and the viral RNA respectively, through nuclear envelopes, utilizing host nuclear transport protein, nucleoporin Nups153, one of the nuclear pore complex (NPC) components [26, 27]. Thus HIV-1 cannot reproduce without the host cell proteins. It controls the activities of the host cells allowing its envelope domain protein to assemble with host cell domain proteins with a large conformation change, undergoing structural rearrangements to facilitate fusion and making new copies of itself inside the cells; this harms the immune system causing weakening and damage to the natural body defenses. HIV-1 host cells interaction is predominantly by charge-charge interactions (more details in Chapter 6) to control all their metabolic capacities [24, 28, 29], which play an important role in the HIV-1 life cycle replication. This creates many difficulties for producing the exact drugs to fight against the viral cycle without harming the human hosts, therefore, HIV-1 disease have no cure until now. It has the capability to develop drug resistance to therapeutic agents through multiple mechanisms. It is a mutation associated with responses to the therapeutic drug [30]. In one patient, the virus can change into a quasi-species to escape the host immune system which increases the pathogenicity of the virus and presents a challenge for vaccine development. The complex regulation of the replication and reformation to penetrate host cell defense mechanisms can also escape antiviral treatment [21].

However, antiviral drugs are used which target and disturb different parts of the life-cycle of the virus at any stage inside the host cell. These include inhibitors to deactivate the vital co-receptor, as in an antiviral blocker of CCR5 [31] to impair the HIV-1-CCR5 interactions [25]. Reverse transcriptase and APOBEC3G protein inhibitors used to block HIV-1 reverse transcriptase from error inducing APOBEC3G protein, is also used in anti-HIV-1 drugs [32, 33]. Antibodies are also used to inhibit the virus diffusion into the host cell but cannot prevent the HIV-1 interaction with the primary receptor CD4. The most effective HIV-1 treatment in Pharmaceutical

approaches, however, is by using a cocktail of anti-HIV-1 drugs at high dosage to prevent the development of drug resistance. This type of treatment deactivates their genomes to prevent replication, but does not destroy the provirus HIV-1 DNA in the nucleus of the host cell [34].

For prevention and treatment of diseases caused by retroviruses using a traditional approach, frequent recombination and high mutation rate in the virus creates multiple problems. Thus, such diseases require series routines for monitoring therapeutic agent efficiency and response to resistance. These need high quality techniques that are used for diagnostics and testing of resistance genotyping of such diseases. This is costly and might not be available in all medical laboratories [20]. It is high risk due to the side effects of therapeutic drugs and sensitivity to the new modification of the therapeutic agents. An example of the side effects such as anemia, depression, difficulty sleeping, headache, dizziness, rash, fever, nausea, stomach pain, diarrhea, vomiting, loss of appetite, constipation, darkening of palms, hair loss, tingling, numbness, or burning sensation, muscle aches, hypersensitivity reaction, liver and kidney problems, high blood sugar and cholesterol, and fatigue [35]. The new approach is to select specific therapeutic drugs based on genetic testing, now considered in modern clinical practice because of a significant number of deaths, (about 100,000 annually and about 2 million annual hospitalizations in the United States), related to inappropriate drug reactions, which is a serious problem in industrialized countries [20]. It is a big challenge, involving complex pharmaceutical process and experimental laboratory cost. These problems still remain in the recent fight against the most devastating pathogen in human history.

However, if all the above approaches and drug modifications to optimize the therapeutic drugs become useless and cannot be replaced, the drug resistance cannot be stopped and the disease becomes untreatable, risking increasing HIV-1 drug resistance, and loss of future treatment options, and hence, life threatening. Outbreaks of the disease may not be controlled, killing millions of people. Additionally, the economic burden of related healthcare-associated infections is significant, thus developing an alternative treatment to therapeutic drugs such as electro-medical treatment, using the applications of electrical field obviously becomes very important. A reduction in burden could be achieved with these new medical treatments from advanced effective low cost new technology device design.

### 1.3 Develop Concept

Proteins are built up from amino acids (AA) that are composed of a central carbon atom bonded to a hydrogen atom, an amino group (N-terminal), a carboxyl group (C-terminal) and a side chain (R) with covalent bond as shown in Figure 1.2. The presence of ionized amino and the carboxyl ( $\text{COO}^-$ ) group produces a predominant dipolar which can be then rotated. Although, typically there are 20 amino acids in nature, their distinctive structures are due to the presence of various non-polar and polar amino as well as charged acid side chains. The specific protein sequence formed by its amino acids are connected together to form polypeptide polymer chains and build up the primary structure of a protein. Accordingly, each polypeptide also has various non-polar and polar amino acid side chains and produces dipolar. Although the peptide bond is polar, it cannot rotate freely, thus, its motion is restricted [21]. However, these polypeptides are folded into a three-dimensional (3D) structure by a variety of intramolecular interactions, such as electrostatic force within the side chain sequence which characterizes the active proteins that affect the final protein conformation [1]. Commonly, in the 3D complex structure of the protein, however, the non-polar side chains (hydrophobic residues) are stifled inside the protein core, while the polar and charged groups are distributed on the protein surface and considered as the predominant group to be in contact with other predominantly protein groups, and with the aqueous medium interact in a complex process to perform various cell functions. The structural rearrangement of the protein changes its molecular shape, due to the bond rotation, without breaking the covalent bonds defines the protein conformation [34].

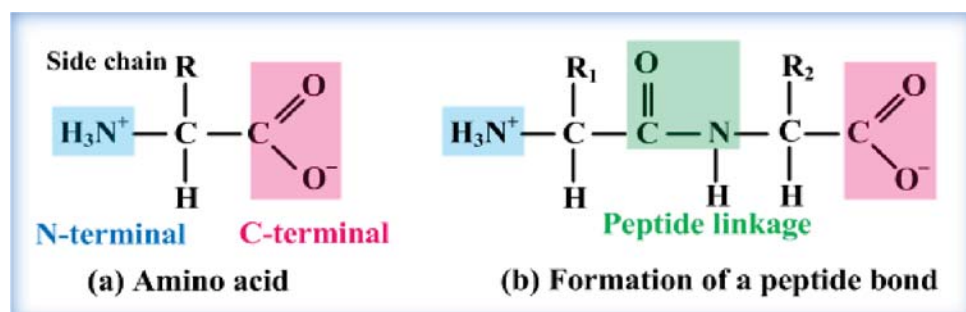


Figure 1.2. The primary protein structure, (a) amino acid structure, and (b) amino acids are connected together by a covalent linkage called a peptide bond to form polypeptide polymer chains and to build up the primary structure of a protein.

Proteins involve their amino acid and are therefore, a dynamic molecular structure, and the distribution of high and low charges on a side chain with degrees of polarity in their sequence domain, along with hydrophobic residues, displays a heterogeneous structure. Thus the proteins comprise various conductivities and permittivity (determining the interaction with the electrical field) allows proteins to assemble with other proteins along-with a large conformational change involving structural rearrangement in response to intercellular and/or extracellular signalling to perform required cell functions [1, 36]. Living organisms themselves produce electric currents that stimulate intercellular signalling and extracellular signals to regulate all biological processes. These signals enable the cell to sense and amplify small changes in the ion concentration [37, 38] of specific molecules, to produce and metabolize energy contained in molecules in its environment, to communicate with other cells in its neighbourhood, to move, to maintain its structure, to regulate its growth in response to signals in its surroundings, to speed up chemical reactions, to sense if it has been infected by a virus, to replicate itself when it is appropriate to do so and to detoxify and/or transport poisonous molecules out of it [3, 21]. The organism's cells that respond to internal signals, can also respond to external signals such as various forms of radiation and electric forces that could similarly induce conformation changes to enhance or inhibit cell functions. One of the specific factors that could attenuate and destroy the pathogens in the body using the application of electrical field is due to complex biological effects in which change of the charge distribution of the proteins active molecules takes place. Therefore, when an electrical pulse with a given frequency is applied, the redistribution and alignment of the proteins charged molecule and its polar molecule in response to an applied external electrical field can be a useful mechanism that interrupts the communication between HIV-1 virus and the host cell.

The frequency-dependent dielectric present in proteins involves the orientation and polarization of its randomly orientated polar molecules and of its charged molecules, making them rotate, move, align and polarize in response to the low frequency electrical force. This could induce an antiviral state for a period of time. Interference polarization within proteins could disturb the interaction between both sides of predominantly charged and/or polar host cell proteins and of the HIV-1 infective envelope and its protein particles.



The HIV-1 and host cell interaction process is characteristically dominated by charge–charge interactions to induce conformational changes, in order to control host cell protein functions, and to stimulate different signals that are vital for virus cellular processes and replication. Since HIV-1 viral attachment and fusion requires stable and sustained interactions with the target cell, the interaction of the HIV-1 envelope proteins domain region with the coreceptor domain region, is considerably diminished, and hence, the dynamic forces of a virological synapse (cell-to-cell interaction to allow cell-to-cell transmission) [39] are possibly inadequate to maintain the attachment of the HIV-1 virus for a sufficient period of time. Such stable interactions can be only provided by the immunological synapse (signaling proteins for cell activation) [40]. Similarly, the applications of the electrical stimulation could disturb the binding process of its effective factors that mediate the passage of its large macromolecular infected particles and its RNA through NPC. Thus the HIV-1 virus cannot conjugate with the target cells, disturbing its life cycle, and suggests that the mechanisms of the inactivation signal induces virus death. This may disturb the life cycle of the HIV-1 virus and hence, its replication, with no potential risks and harm to the host cells compared to the pharmacological approach.

The type, intensity and duration of the electrical stimulation force must be selected carefully to stimulate an appropriate action and must not be so strong that it would produce undesirable responses. It is well known that high frequency waveforms have enough energy to break any cell's chemical bonds (ionization), while in lower frequency waveforms, the energy has a non-ionizing effect that breaks down the chemical bonds [41, 42]. Considering proteins as dielectric materials [43] when applying a low frequency electrical pulse, proteins present a large low frequency permittivity, while at high frequencies dielectric loss takes place. Furthermore, applying a low intensity electrical field enhances ion transport across the cell membrane, due to the fact that nano scale pores form in the cell membrane temporarily, while at a high intensity, the electrical field causes dielectric break down; the cell is unable to recover from the pore formation process, causing in cell death. Thus, high intensity electrical fields can be used in electroporation therapies for treating a variety of cancerous pathologies [1, 44]. However, naturally, the variability of the dielectric properties of proteins is important for the biological function of a protein [43, 45].

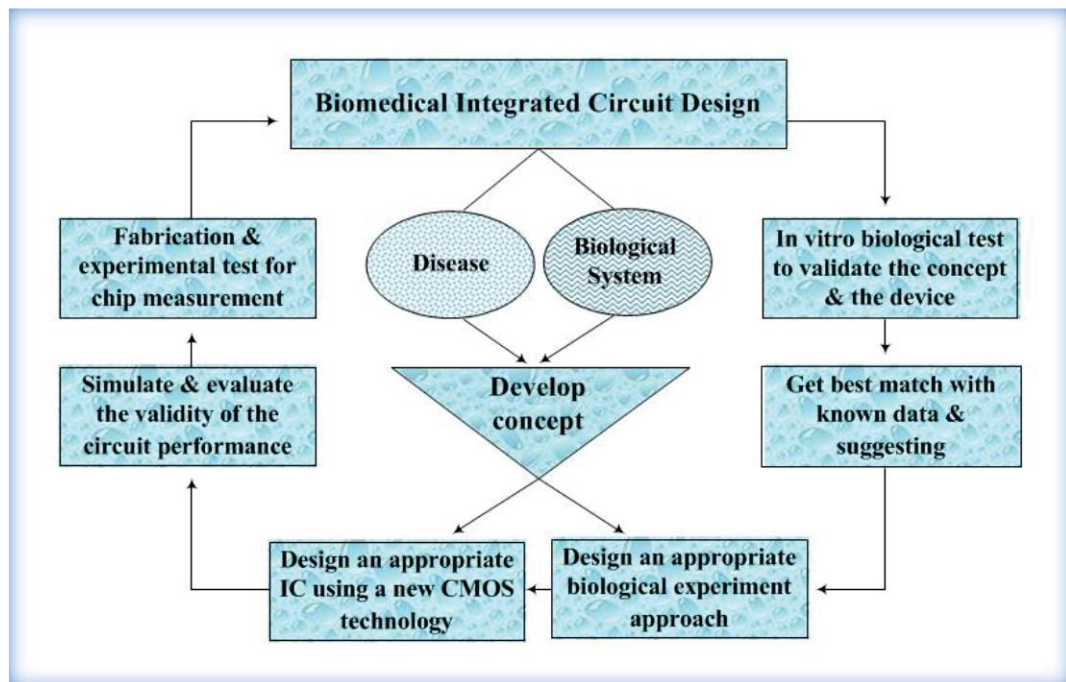


The movement of the charged molecule and the free ions, in response to an applied external electrical field can also be a useful mechanism to induce an action comparable to the normal cell endogenous electrical field. An endogenous field, which induces variation in membrane potential, due to the movement of the charged residues in the intrinsic plasma membrane proteins, as well as free ions, has importance in biological processes, such as wound healing and tissue regeneration. Since the surface charge can change with the pathophysiological state of the cell [36], thus inducing a small electric current can also enhance the normal cell functions by inducing a variation in membrane potential, and affect subcellular mechanisms, particularly the intracellular  $\text{Ca}^{2+}$  concentration or other voltage-dependent ionic activities [46]. An additional notable feature of this electrical stimulation is its cellular specificity. Therefore, the parameters of the generated electrical pulse can be designed and selected in order to stimulate only one particular type of tissue, such as blood, nerve, muscles, urine, leaving the others unaffected [47]. Moreover, in the electrical stimulation approach, the type of waveform must be carefully considered. Using a periodical waveform with certain stimulation frequencies can interact with the periodical intrinsic oscillators of the biological cell networks, which enhances their intrinsic oscillatory activity [48], a phenomenon that describes the natural frequency of the human body, which is an essential process in the living organism that enhances cell communication [49]. Since disease can disrupt the biochemical systems in biological cells, this inhibits the normal protein synthesis in lymphocytes, therefore, applying certain stimulation frequencies can enhance the biochemical parameters of the blood and normalize protein synthesis in lymphocytes [50].

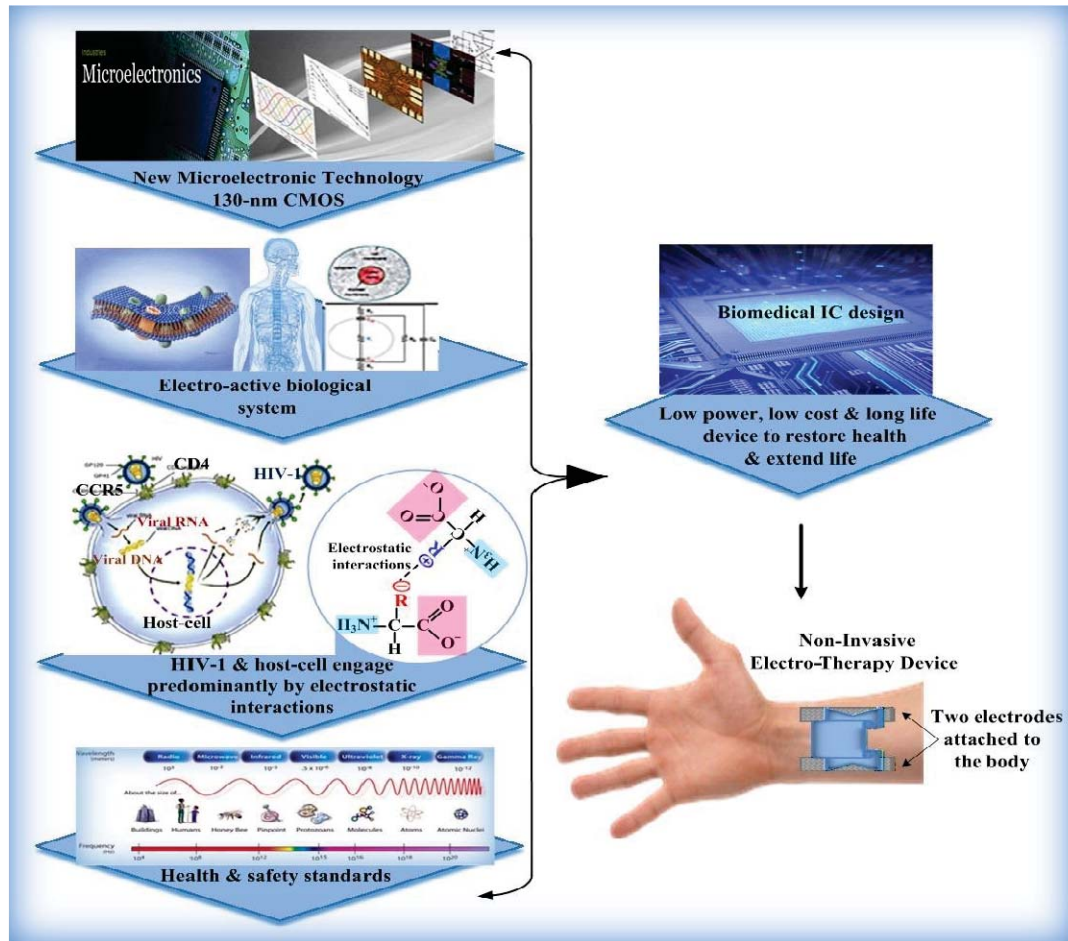
Studies on frequency dependent dielectric properties of human blood, covering a frequency range from 1 Hz to 40 GHz, using broadband dielectric spectroscopy, have also shown no evidence of harmful effects at low frequencies [51]. The modes and the duration of the electrical stimulation pulse should be taken into consideration. Clinically, using the long duration Monopolar mode leads to charge accumulation at the electrode-skin site, causing muscle contractions which may damage the tissue, while using the long duration bipolar mode of operation, each pulse is followed by a pulse of reversed polarity which ensures charge balancing and hence, prevents damage that may occur at the electrode-skin interface [3, 44].

Theoretically, and in my opinion, the periodical low frequency square waveform with wide pulses can block the interaction between the virus and the domain regions of the host cells for a sufficient period of time, therefore, the HIV-1 virus cannot mutate and develop resistance in the absence of the host cell proteins as in traditional pharmaceutical approaches, so that the HIV-1 virus will then vanish. Interestingly, using an application of periodical low frequency bipolar square waveform signal and low voltage electrical field can, therefore, induce enhancement and/or inhibition effect, prompting an antiviral state for a period of time, but is not expected to seriously disturb the host cell protein structure and its conformation state. Indeed, the protein molecules have non-polar hydrophobic amino acid residues building up the core, and the polar and charged amino acid residues are mostly located on the surface of the molecule, and there is no rotation around the peptide bond, thus the back bone of the protein does not rotate freely and only the polar or charged site chains rotate [1, 21]. These electrically induced protein transformations can be studied invivo/in-vitro as blood-cell treatment and as anti-HIV-1 electro-therapy. This may offer an antiviral therapy to target the most devastating pathogen in human history (more details in chapter 6).

Figure 1.3 (a) and (b) summarizes and shows the development and design steps of the biomedical integrated circuit for electro- therapy device of this research project.



(a) Block diagram shows the design steps of the proposed biomedical IC.



(b) Schematic diagram shows that advances in 1) microelectronics technology involving new CMOS biomedical IC design, 2) bio-electro-chemistry science including cellular function, electro-active biological cells and their responses, and 3) knowledge of the disease condition, concerning the underlying mechanisms of the biological cells and disease state (HIV-1 and host cell engage predominantly by protein charge-charge interaction), are combined in this research project, in order to develop the concept and design a biomedical device capable of communicating with electro-active biological cells and how this could be utilized for biomedical treatment applications.

Figure 1.3: The development and design steps of electro-therapy concept and device of this research project, (a) block diagram, and (b) Schematic diagrams.

## **1.4 Research Goals**

The goal of this research project is to combine advances in engineering (involving new CMOS technology) and biology (including the electro-active body medium) as well as the underlying mechanisms of the biological cells and disease state (HIV-1 and host cell engage predominantly by electrostatic interactions) to develop the concept and introduce a biomedical device capable of communicating with body tissue and cells, for biomedical treatment benefits. A corresponding goal is the characterization of this concept in-vitro, and, if possible, the device in-vivo, to investigate the effect of low frequency and low voltage electrical pulse on human blood cellular proteins, to stimulate a potential reaction that can induce a short-term, or long-term anti-HIV-1 viral state. Besides, this research project can develop knowledge for advanced technological electro-medical treatment devices, their design, structure and applications. The research project therefore, has the following aspects:

1. Concept development for anti-HIV-1 electro-therapy.
2. Biomedical IC Design. A novel low power and low frequency non-invasive biomedical device comprising a dual-band WFG with ultra-wide low-frequency tuning range and an active-electrode-pair will be developed, based on a new 130nm IBM CMOS technology.
3. Bio-electrochemistry experimental work. A theoretical analysis, experiment design and performance will be carried out in in-vitro environments to examine the influences of the periodical low frequency bipolar square waveform signal and low voltage electrical field on human blood cells.

## **1.5 Scope of This Study**

The electrical characteristics of biological materials have inspired the researcher to utilize applications of low frequency and low electrical field on the human immune response, specifically, the underlying mechanisms of HIV-1 and host-cell interactions. These are predominantly by electrostatic force, involving charge-charge interactions of the dynamic molecular proteins that control cell function, which are of particular interest in this research project which might offer important antiviral therapy targets against HIV-1 by eliminate the virus completely. The required electric signal is

generated from an electrical WFG. In this work, non-invasive techniques which do not require implantation into the body, will be the focus; a device which can generate, control and deliver an appropriate low frequency low voltage pulse via electrode, through the low-resistance skin surface to a patient's blood. This method has practical advantages, as it is convenient for the patient, with no harm. The biomedical device of this research project comprises a mixed-signal low power dual-band WFG chip with a wide low frequency tuning range. The circuit provides periodical square/triangular waveforms along with a square waveform complementary signal for low frequency electrical stimulation applications. Two WFG approaches will be developed in this research project, for comparison. Since the aim of this work is to transfer electrical signals, in a specifically controlled fashion, through the electro-active tissue, an active electrode will be developed to provide biphasic square waveform output signals to overcome the deficiencies of using passive electrodes. Thus, a good quality signal can be transmitted by reducing the sensitivity to cable and environmental noise. The WFG with surface electrodes is battery operated with low power consumption, and hence, low cost. In the light of this an in vitro bio-electrochemistry experiment will be carried out to examine the concept of this research project. The following objectives clarify the works carried out in this research project:

1. Develop a new theoretical model and derivative of a novel mathematical model to determine the controllable variable parameters as well as component sizing for high gain, low frequency, low power, and small chip area WFG circuit design and also to study the trade-off between these important parameters.
2. Develop IC for the extra low frequency (ELF) WFG design comprising a novel hysteresis Schmitt Trigger and utilizing a RC relaxation timing network.
3. Develop a novel concept employing a combination of the different types available of on-chip p+ polysilicon resistors in the 130-nm IBM CMOS process, in order to fully implement the large integrated resistors.
4. Develop small-size on-chip capacitors with low capacitance.
5. Develop IC for a novel low-power dual-band WFG<sub>INT</sub> design with ultra-wide low-frequency tuning-range comprising a hysteresis Schmitt Trigger and realizing an integrator relaxation timing network along with a novel two band tuning system.
6. Develop IC and derive a novel mathematical model integrator building block comprising a first order electronically adjustable gm-C integrator to perform three

tasks; (1) the timing network, (2) for low frequency design, and (3) for the electronically tuneable WFG<sub>INT</sub> circuit (band I), linearly controlled by the bias current (IB) of the gm-C integrator through a smart and simple tuning technique.

7. Develop a novel low power hybrid frequency tuning technique composed of two models; (1) the analog (band I, electronically adjusting the bias current of the gm-C integrator), and (2) the digital model (band II, frequency divider), comprised of a 16 stage divide-by-2 frequency divider (FD) in series with dual 8-1 multiplexers (MUXs) and a path-selector (PS). The PS output can drive complementary active electrode circuits to realize a biphasic square waveform for electro-medical stimulation using the chosen frequency.
8. Develop and optimize a low power miniaturized IC for a novel active electrode-pair design to deliver an appropriate biphasic and monophasic waveforms for low frequency simultaneous multichannel biomedical applications.
9. Implement and simulate the electronic model in VLSI.
10. Set-up experimental measurement to validate the fabricated chip performance.
11. Evaluate the design using a comparison of the proposed circuit design and the signal characteristics with recent and relevant publications and literature.
12. Develop the theoretical model of the complete free energy non-invasive biomedical device of this research project involving signal-processing circuitry, by mounting all IC signal source and the active electrode on the electrodes (transducers) with solar panel charged regulated power-supply.
13. Develop applications. Complete the theoretical analysis of the underlying mechanism of the HIV-1 virus and host cell interaction, in order to design and set up the bio-electrochemistry experiment in-vitro, to study the effect of the generated periodical low frequency bi-phase square waveform signal on the cell surface receptor CD4 protein, co-receptors CCR5 protein and on the binding activities of CCR5 N-terminal domain, as well as on the distribution of nucleoporins Nup153 utilizing the Immunofluorescence microscopy technique. Compare the results with recent and relevant publications.

In biomedical integrated circuit design, however, high accuracy is required and needs careful consideration of how the circuit and system work. The movement towards low-power applications requires novel device architectures, and a good design methodology, including system level simulation is necessary. The biomedical integrated



circuit design of this research project is state-of-the-art in terms of safety, low power, miniaturization, light-weight, and portability; an IC solution that can be suitable for use with electrical stimulation applications. In particular, the proposed WFG design is important for battery-operated implantable and non-invasive biomedical devices, enabling the reduction of the overall system cost.

The bio-electrochemistry experiment is developed to examine the concept of this research project, and to study the effect of the designed electrical signal on the molecular mechanics of HIV-1 and host-cell interactions. Since this type of experiment is considered as including high level physical contaminants (PC3) which is not appropriate in Massey University labs or any other normal labs, the electrical stimulation test is performed on healthy human blood cells only. Therefore, the in vitro biological experiments required for this project work were conducted primarily in Human Nutrition lab building 27, and the biology lab building 10, School of Food and Nutrition (SoFN) laboratories, which are permanently located at Albany campus, College of Health, Massey University. Health and safety induction for laboratory users and for the campus environment as well as the biological compliance for physical containment (PC1 and PC2) was completed, before beginning any work.

All bio-electrochemistry experiments were done with human Ethics (SOA 16/12) considered and approved by the Massey University Human Ethics Committee. A copy of the Ethic approval has been provided in Appendix A. This was followed by my self-training, studying and understanding of the basic principles in biological laboratory research techniques including advanced computable fluorescence microscopy techniques, used for imaging biological specimens. My study resources include, microbiology books, online academic lecture, and web tools, including those about cell biology and functional proteins, immunobiology reagents and Immunoassays and technical protocols. Although it was time consuming, during this time, I gained extensive workshop experience in the biological laboratory research environment in addition to my extensive workshop experience in the chemical laboratory research for my Master's degree, to meet the lab research requirements, which enabled me to conduct the biological experiments for this research project with success. Based on this, valuable findings were achieved. This finding may offer important antiviral therapy targets against the most devastating pathogen in human history.

## 1.6 Thesis Overview

**Chapter 1** provides a brief introduction to the need for design of biomedical integrated circuit solutions for bio-electrical stimulation to restore health, specifically, WFG and active electrode design for biomedical devices. This chapter briefly describes the relevant disease and a novel an appropriate electro-medical concept for this research including the importance of the protein structure involved in HIV-1-host cells interactions, predominantly by charge-charge interactions, which play an important role in its life cycle replication. Based on this, a novel biomedical IC solution for a non-invasive biomedical device is proposed to investigate the applications of a periodical low frequency bi-phase square waveform pulse on the human immune response, specifically, the molecular mechanism of HIV-1 and host-cell interactions.

**Chapter 2** provides an overview of this project's system model, theory, design, and approaches. The chapter starts, with a brief summary of the important properties of the WFG followed by a basic theory of oscillators and oscillator approaches. Relaxation oscillator architecture and the hysteresis Schmitt Trigger concept are explored along with the principles of operation of a WFG circuit. Two specific WFG circuit theories related to this research project are introduced. WFG approaches that have been developed by various researchers are presented. This includes a comprehensive review of a recent CMOS WFGs design approach based on hysteresis Schmitt Trigger, termed "current mode operational trans-conductance amplifier (OTA)" which has shown massive potential for low power circuit design. The importance of the relaxation timing network, including passive RC and active integrator gm-C approaches, are also discussed. Tuning system approaches including analog and digital models are provided in this chapter. A comparative study of a number of different flip-flops (FF) architectures was reviewed, to classify those that are the best power and area efficient designs to re-design and use for a FD designed circuit. Sources of power dissipation in a digital model are discussed. Finally, a brief summary of the active electrode feature and approaches is provided. This knowledge is essential to complete the system design on a single chip, using both the analog and digital circuit solutions.

**Chapter 3** presents design criteria, implementation and fabrication of a WFG circuit for ELF CMOS micro-power applications. Since the fundamental building block of a WFG and the overall performance of the WFG circuit in this project, is determined



by the characteristics of the OTA design, their design parameters are discussed at the start of this chapter, which is fairly important. The importance of the key factors for low power, low frequency and small chip area WFG circuit design is presented next, followed by circuit design and topology. Circuit operation and the mathematical derivations related to gain, frequency, duty cycle and its controllable variable parameters, with simulation and performance analyses, are described and presented in this chapter. Advanced physical design that defines the physical size of the circuit is introduced. Accordingly, a novel concept of employing a combination of the different types available of on-chip p<sup>+</sup> polysilicon resistors in the 130-nm IBM CMOS process, used to fully implement the large integrated resistors, is also presented. Using the same topology, two sets of device dimensions and circuit components, designed and fabricated for comparing relative performance, silicon area and power dissipation, are also introduced. Experimental results and a comparison of the two fabricated ELF WFG designs with the circuits' simulation outputs are presented in this chapter.

**Chapter 4** presents design criteria, implementation and fabrication of dual-band CMOS WFG with wide low-frequency tuning range. Appropriate design requirements for a novel WFG<sub>INT</sub> circuit to increase the performance of the device are presented, followed by circuit design and topology including gm-C integrator realization. Circuit operation and the new mathematical derivations related to gain, frequency, and its controllable variable parameters, as well as component sizing for low power and low frequency WFG design, are discussed. A novel hybrid frequency tuning technique composed of two models, the analog (electronically adjusting the bias current of the gm-C integrator) and the digital (frequency divider) model, including a new mathematical approach, is also presented. The robustness of the designed WFG<sub>INT</sub> circuit, including temperature variation and signal integrity, is also presented. In order to optimize the layout for size, the technique to implement the device in analog and digital models is also described. The measurement results and comparisons of the fabricated WFG<sub>INT</sub> circuit design with 1) the circuit's simulation output, 2) with the ELF WFG of this work, and 3) with reported designs, are also presented. The optimization flowchart of the designed dual-band WFG<sub>INT</sub> including the circuit design process performed in this work, is introduced at the end of this chapter.

**Chapter 5** presents the design criteria, implementation and fabrication of a low power CMOS active-electrode-pair for low-frequency multi-channel biomedical

stimulation. A brief introduction to the skin layer and skin electrical model study by different researchers is introduced, followed by the active electrode circuit realization of this work and the parameters that control the circuit performance. The circuit design, with theoretical analysis to optimize the performance of the active electrode circuit, is presented. Using the same topology, two identical active electrode circuits, developed and fabricated to drive the load in a differential fashion, utilizing a complementary active electrode circuit, are introduced. The measurement results and a comparison of the performances of the fabricated electrode chip with reported designs, are also presented. The new theoretical model, including a schematic diagram of the completed, proposed, non-invasive biomedical device, comprising a dual-band WFG, two identical active electrodes, power supply circuitry with free energy solar rechargeable battery, and biological interfacing device are also illustrated in this chapter.

**Chapter 6** presents the in vitro Biological experiment design and performance to investigate the effect of low frequency electrical pulses on the human blood cells. A brief introduction to HIV-1 and host cell interaction and immune-based therapies in the pharmacological approach, followed by a brief analysis of the CCR5 protein structure as well as the NPC features and its important component, Nup153, is given at the beginning of this chapter. Details on protein-protein interactions that involve charge-charge interactions determining the interaction between the predominant HIV-1 regions and the predominant regions of host cell CCR5 and Nup153 reported by different researchers are described in this chapter which is important to support the concept of this research project. The concept of frequency-dependent polarization is also presented. A theoretical analysis with design and setup of the bio-electrochemistry experiment in-vitro, to examine the cell surface receptor CD4, co-receptors CCR5 and the CCR5 N-terminal domain as well as the distribution of Nup153 in response to electrical stimulation utilizing the immunofluorescence microscopy technique, is described and discussed in this chapter. Experimental results and valuable findings are illustrated and discussed in this chapter.

**Chapter 7** presents the thesis conclusions with a summary of contributions made by the researcher, limitations and future research suggestions in this interesting area.

## **Chapter 2**

# **Overview of The System Model, Theory, Design and Approaches**

### **2.1 Introduction**

An integral part of many modern electronic systems, including medical treatment devices, is a waveform generator (WFG). The demand for low-power and miniaturized WFG has become considerably more important in a wide range of applications such as communication, wireless sensor networks instrumentation systems as well as signal processing and battery-operated medical treatment devices. They are used either as stand-alone signal sources or as part of a system. Multipurpose signal source WFG, which generates monophasic or biphasic square, triangle, and sine wave outputs, provides and delivers, as stimulus, electrical pulse signals with a wide range of frequencies which are required widely for signal processing systems for simulation and control in electro-medical treatment. This is required for the long-life battery-operated biomedical devices that are implanted in the body and for non-invasive devices (section 1.1). Such smart devices require a waveform signals generator as well as electrode circuitry that directly or indirectly communicates with the electroactive biomolecule. Thus the low power miniaturized design of both these circuits becomes important in a wide range of biomedical signal processing systems.

Generally, WFG can be designed according to the medical device requirements. It is also low-power, low cost, miniaturized and fully integrated on-chip circuitry with high functionality which is desired for long-life battery-operated medical treatment devices. This requires high-performance analog and/or digital integrated circuit design. The completed design system on a single chip, using both the analog and digital circuits implemented on the same die, can only be achieved in a new sub-micron CMOS process technology, which has advantages over other technology. Scaled CMOS facilitates a high integration level for multiple functions on a single die. CMOS devices that have ultra-low power characteristics, are miniaturized and can be fabricated in large numbers with high circuit performance enable a rapid transition in the microprocessor industry to this new technology; these unique characteristics are the basis for using

CMOS technology in the development of such systems. One of the rapidly developing areas of CMOS is in analog circuits, covering a variety of applications from biomedical circuits operating at a low hertz range, audio circuits operating at a moderate kilohertz range to current wireless applications operating at a high gigahertz (GHz) range of frequencies [52]. The digital circuit is normally high cost, due to the larger area and high amounts of energy that will be consumed. The nanometre (nm) CMOS technology is becoming mainstream in the integration of low power, low cost and small area digital circuitry for signal processing.

The fundamental principles for low-power analog and digital signal design, which combine and integrate typical approaches, will be presented throughout this chapter. These include the basic principles of the analog WFGs and the active electrode circuit, as well as the digital frequency divider system with a theoretical approach, and the recommendations for accomplishing a few simple functions with standard building blocks to form a respectable enhancement to the proposed design. The outline of this chapter is as follows: in section 2.2, the chapter starts with descriptions of the important properties of the WFG. The basic theory of oscillators and power efficient low frequency relaxation oscillators is introduced in section 2.3. The concept of hysteresis Schmitt Trigger and the use of a different relaxation timing network to develop the typical WFG circuit are all introduced in section 2.4 and 2.5 respectively. Various circuit architectures suitable for WFG and a previously published current mode WFG approaches are also discussed in section 2.6. Tuning circuit approaches are presented in section 2.7. A discussion of digital design for a frequency divider circuit is included in section 2.8 to provide in-depth aspects of the design of low power and small chip area digital circuitry. A short review of an active electrode is presented in section 2.9, and chapter 2 concludes in section 2.10. A comprehensive review of literature related to this research project is also included.

## **2.2 Waveform Generator Overview**

Depending on the application, there is a requirement to generate signals having various waveforms, such as square, triangle, exponential, sinusoidal, and saw-tooth. The several circuits used for generating these signals are normally called signal generators or waveform generators. The WFG produces a time dependent signal of prescribed

characteristics, such as waveform shape, amplitude and frequency. Its amplitude and frequency can be decided and adjusted, by changing appropriate component values. These WFGs can be designed according to the output waveform, the parameter used and the range of frequency. Although there are many properties to be considered in any WFG design, the important properties of the WFG can be summarized as follows [52, 53]:

1. **Periodicity** that describes the type of the waveform, including i) Single shot delivery by a pulse generator that generates a single pulse in response to a stimulus, ii) Stationary waveforms that have fixed properties: output signal shape, amplitude and frequency are constant over a long period of time, iii) Modulated waveforms which have some properties that vary from interval to interval in response to a signal.
2. **Shaping** which can be generated using i) Simple functions designed in concept with simple basic active and passive elements. These involve sine-waves as generated by resonant elements, square waves generated by utilizing a timing element network; exponential and triangular waves are mostly the product of square waves. ii) Complex functions obtained by applied operations on simpler functions such as modulation, and filtering. For example, it can generate sinusoidal waves in complex fashion by applying a low-pass filter to simple square/triangular WFG.
3. **Speed** required for operating frequency of the designed WFG circuit. It can be designed to operate at low speed (sub-frequency of 1Hz), audio frequency (20Hz to 20kHz), or high speed as in a wireless communication circuit (MHz to a high GHz) range of frequencies. The frequency of the circuit is the critical property of the circuit as this affects the choice of approaches, the type of components, the design limitations and the accuracy. The architecture of traditional low-frequency circuit design requires appropriate large size active and passive devices, operating with low power consumption, and reasonable bandwidth with low or no noise, while most high frequency circuit design is critical rather than complex, requiring appropriate small size, active and passive devices. Thermal and high noise effects, as well as the high power consumption, are the most important factors considered in high frequency circuit design, especially for wide bandwidth design. However, the shrinking size feature of CMOS has enabled the design of complex analog circuits in the 1Hz to high GHz range [54].

4. **Frequency-determining components** which include the basic building block of the WFGs. For example, WFGs that utilize internal crystal oscillators are resonant and expensive, while WFGs that are based on a regenerative comparator and a reference supply, switch to a change state when a certain threshold level has been crossed, and are level controlled, as in one-shots and multivibrators. Their frequency typically depends on RC time constant and they are low in cost.
5. **Controlling parameters**, including amplitude, frequency, and shape, which are affected by the design parameters of the WFG. This is absolutely controlled by parametric accuracy; the desired characteristics are usually specified with a small magnitude of error that indicates the deviation from perfection. For a given application, the design WFG circuit may have frequency variations of about of 0.01 %, but amplitude variations and shape distortion of about 10%. The reliability of the desired function depends on the specifications and performance of the WFG.

It is possible to consider an enormously wide range of WFGs, classified and designed in many different ways, but mostly designed and constructed based on a simple oscillator circuit. Oscillators are essential in a wide-range of applications including telecommunications, control systems, measurement systems, sensor interface and signal processing, depending on their frequency [55-57]. An oscillator circuit is one which is capable of generating independently repetitive oscillations between two different states of one of the variables that defines it [53]. Circuits that oscillate autonomously and generate time functions, in some influential way involving nonlinearity systems which utilize the positive feedback concept, are the most desired in the square WFG architecture.

## 2.3 Basic Theory of Oscillator

A simple oscillator circuit is based on the positive feedback concept. Positive feedback is the desired nonlinear behaviour in the system, which can be used to design various useful oscillator circuits [58]. Positive feedback occurs when the output signal is returned to the input terminal of the same circuit through the feedback network that is in phase with the input signal. Consider the positive feedback circuit in Figure 2.1, in which the external input signal  $V_s$  is applied to a simple non-inverting operational amplifier (Op-Amp) circuit, which has a voltage open loop gain of  $A(s)$ . The output  $V_o$

of the circuit is in phase with input signal  $V_s$ , and is feedback to the input through a feedback network  $\beta(s)$  to produce the input signal  $V_{in} = V_s + V_f$  of the circuit. The feedback voltage  $V_f = \beta(s) V_o$  depends on the feedback network  $\beta(s)$  gain, considering the closed loop gain  $A_{closed} = A/(1 - A\beta)$ , for constant open loop gain  $A = V_o / V_{in}$ , so that the  $A_{closed}$  gain of the Op-Amp circuit increases as the feedback network  $\beta(s)$  increases. Under some conditions, the gain can tend to infinity, the Op-Amp circuit then stops amplifying and starts oscillating, producing infinity output with no external input ( $V_s = 0$ ). A simple oscillator circuit can be then realized, utilizing positive feedback with no external input, and it generates a signal with specific frequency that maintains infinity output as shown in Figure 2.2.

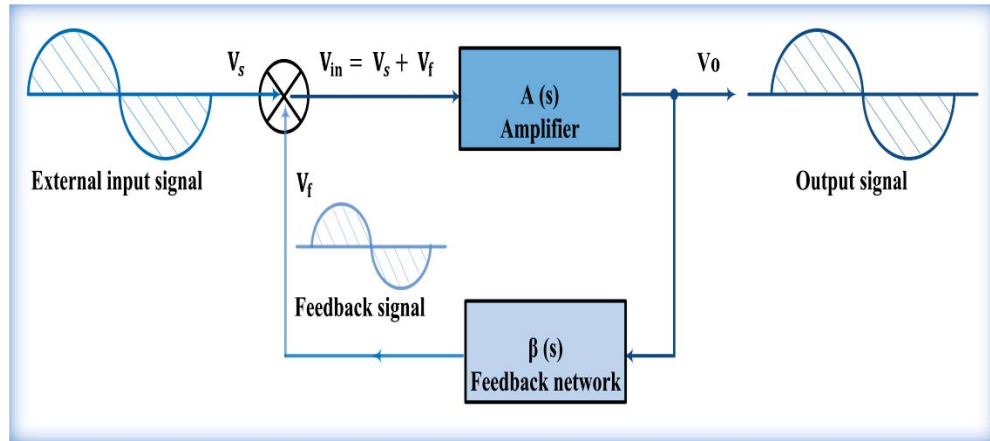


Figure 2.1. Block diagram of a simple positive feedback system.

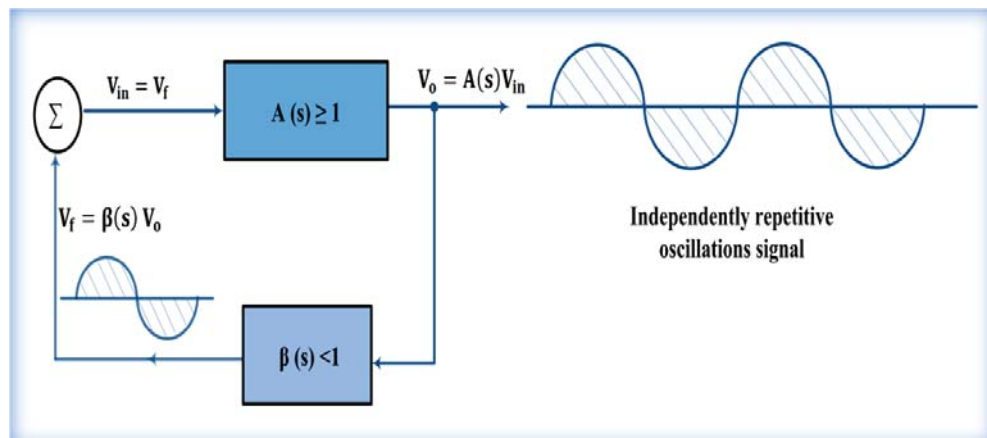


Figure 2.2 Schematic diagram of a simple oscillatory system.



Generally, the circuit will sustain oscillations only at frequencies that satisfy the Barkhausen criteria, for which the loop gain must be equal or larger than unity [ $\beta(s) A(s) \geq 1$ ] and its phase ( $\angle$ ) zero or  $360^\circ$  ( $\angle_A + \angle_f = 0$ ). The input  $V_{in}$  of the oscillator circuit is then driven from its output  $V_o$  by feedback network  $V_f = \beta(s) V_o$ . Since  $V_o = A(s)V_{in}$ ,  $V_f = \beta(s) A(s) V_{in}$ . Since the feedback network attenuation factor is a fraction and less than unity ( $\beta(s) < 1$ ), to start with the oscillations, the loop gain must be unity [ $\beta(s) A(s) = 1$ ]. The open loop gain  $A(s)$  ( $s = j\omega$ ) which is frequency dependent should then be sufficient so that the feedback signal ( $V_f$ ) is equal to the input signal ( $V_{in} = V_f$ ) and its phase zero, which satisfies the Barkhausen criteria [59]. For optimum oscillator design, and in order for the oscillation to start [60], the open loop gain  $A(s)$  of the Op-amp circuit must be 2 to 3 times greater than the required value to guarantee oscillation in the presence of temperature and process variations (PVT) [58].

### 2.3.1 Oscillators Approaches

Indeed, the above basic oscillator circuit can be used to design several types of oscillators, based on the output waveform requirement, the components used, the range of frequency, the feasibility of a low-power consumption and a small chip area. Specifically, the periodical oscillator is one type of oscillator that can generate a perfectly periodical signal with specific frequency and maintain infinity output.

The periodical oscillator is characterized by its frequency  $f_o = 1/T$ . Its response spectrum is composed of a fundamental frequency  $f_o$  and an infinite number of multiples of this frequency [52]. In this type of oscillator, a stable cycle will be achieved, independently of the initial conditions (starting point) of the system.

However, since power efficiency is today the most important design requirement of reliable long life battery operation, several research works have reported on the realization of oscillators in low power sub-micron CMOS technology [61-63]. One of the critical design limitations of an oscillator using an integrated circuit is the generation of consistent oscillator circuits. A ring oscillator is a type of oscillator commonly used in a radio frequency identification system, and in biomedical sensor devices, composed of an odd number of inverter cells (gain stages) in a loop, which generates square waveform output signals. In order to sustain an oscillation, three to five stages are required for optimum performance, requiring a large transistor account and high power consumption [58]. Although a ring oscillator can be operated in the



subthreshold region, the stability of its frequency deteriorates significantly due to PVT variations [64]. A crystal oscillator uses the resonance of a piezoelectric properties of quartz crystals that oscillate in response to electrical stimulus as the frequency-determining element [59]. It has high frequency stability in the presence of PVT variations and can be implemented in nano-scale technology with low power consumption [65]. The limitation in this oscillator is that it is relatively expensive and consumes a large chip area which is not desirable in many miniaturized implantable devices [66]. Currently the feasibility of a monolithic inductor in sub-micron CMOS technology indicates that LC oscillator design can be used. It is commonly used in high-quality communication systems, because of its low phase noise characteristics and available solution for high frequency operation voltage control oscillator (VCO) circuits. To realize a relatively low resonant frequency ( $f_o = 1/2\pi\sqrt{LC}$ ), large inductor and capacitor values are then required to implement the large time constant, which would consume a large chip area, which is not optimal in IC implementation and also cannot be realized economically. In addition, passive LC components cannot be electronically tuned [3]. It also has a large chip inductor and capacitor suffering from resistive components which tend to lower quality [66].

Relaxation oscillators, that are characterized as a simple circuitry configuration with less sensitivity, can generate a periodic non-sinusoidal repetitive output signal, such as square-waveform, exponential waveform and a triangle waveform. Fully integrated relaxation oscillators, operating with low power consumption and consuming a small silicon area, have found wide applications in many VLSI systems, which includes biomedical portable devices and wireless sensor devices [67-71]. Since low power consumption and a low cost are the driving forces in today's biomedical battery-operated device, this determines the relaxation oscillator's configurations for the future WFG design in this research project. Moreover, further comparison reveals that relaxation oscillators typically have frequency stability in the presence of PVT variations, often used in high accuracy low-frequency applications, and can be integrated fully on-chip, since capacitors and resistors are readily available in most technologies [72]. Although large capacitor and resistor values are required to implement the large time constant which consumes a large chip area, in terms of accuracy and efficiency, and chip area, state-of-the-art design will be applied in this research to overcome these challenges.

### **2.3.2 Relaxation Oscillator Architecture**

Relaxation oscillators are classified as an important class of oscillators, mainly used in applications of low power signal processing systems including WFGs. The architecture of one of the most common relaxation oscillators is implemented using a comparator circuit and RC relaxation timing network [52]. This type of conventional relaxation oscillator circuit based comparator suffered from noise in the output signal, and chattering in signal shaping may take place. Although this configuration of relaxation oscillator circuits is sometimes modified to eliminate the noise, comparators remain the main noise sources in the circuit. However, the use of such oscillators is associated with trade-offs because they require large power and large size MOSFET devices to reduce the noise in comparators, which is not desirable in low power, and miniaturized biomedical devices. Large size gates of MOSFET devices also increase the ratio of gate parasitic capacitors which are sensitive to voltage and temperature, [67]. Therefore, in a hysteretic input-output relationship as in hysteresis Schmitt Trigger, operation depends on the regenerative feedback circuit [52, 73] which is used to eliminate comparator chatter in signal shaping [74]. One of the earliest forms of hysteresis circuit in the literature was first proposed in 1938 by Otto Schmitt, and hence ‘Schmitt Trigger’ is its name. It is a thermionic circuit based on positive feedback around the differential pair [75]. It was used in cathode ray oscillography, thermostating and lighting control applications. Nowadays, with modern design demands, Schmitt Trigger is used to ease the noise effect in triggering devices and analog-to-digital conversion. Besides, it is a fundamental block in multivibrators, monostables, and pulse width modulators [52, 76, 77]. They are widely used in both analog and digital in instrumentation and communication systems to produce different signal waveforms, including square waveform, and triangular waveform and to improve the immunity of the circuit to noise and disturbances [74, 78].

## **2.4 Hysteresis Schmitt Trigger Concept**

A system that exhibits hysteresis has an output that is a two-valued fraction of the input, over a portion of the input range, in which the response is not absolutely dependent on the value of the input, but also depends on the threshold of the circuit [53]. A common form of hysteresis is seen in two-states Schmitt Trigger, based on

regenerative feedback circuit with fractional positive feedback. Once the output has switched to a change state, it remains there until the input crosses a certain threshold level beyond the switching point to cause the circuit to change state and switch back to the original state [52, 79]. Figure 2.3 (a) and (b) shows the basic Schmitt Trigger circuit and its voltage transfer characteristic (VTC) that represents the output  $V_o$  against the trigger input signal  $V_{in}$ . It employs Op-Amp with positive feedback at the non-inverting terminal, to provide the upper  $V_{UTH+}$  and lower threshold  $V_{LTH-}$  of the circuit from a voltage divider across the output, while the trigger input signal  $V_{in}$  is applied to the inverting-input terminal. The output of the hysteresis Schmitt trigger  $V_o$  circuit has a two quasi-stable states (high positive saturation level ( $V_{sat+}$ ) and low saturation negative level ( $V_{sat-}$ ) with respect to the input signal  $V_{in}$ . Therefore, the output of the circuit is a function of the input and remains at its state until the input voltage exceeds a certain threshold voltage, so:

$$V_o(V_{in}) = \begin{cases} V_{sat+} & \text{if } V_{in} \leq V_{LTH-} \\ V_{sat-} & \text{if } V_{in} \geq V_{UTH+} \end{cases} \quad (2.1)$$

And for  $V_{LTH-} < V_{in} < V_{UTH+}$ ,  $V_o$  = the previous state achieved. For high level output voltages,  $V_{UTH+} = +\beta V_{sat+}$ , while for low level output voltages,  $V_{LTH-} = -\beta V_{sat-}$ , where the feedback network  $\beta = R_1/(R_1 + R_2)$ . Intend the input voltage  $V_{in}$  increasing from below  $V_{LTH-}$  as in Figure 2.3 (b) the output  $V_o$  remains at its high positive level ( $V_{sat+}$ ), until the input voltage crosses a high threshold  $V_{UTH+} = +\beta V_{sat+}$ . The output switches to its low level  $V_{sat-}$ , remaining there until  $V_{in}$  crosses a certain low threshold.

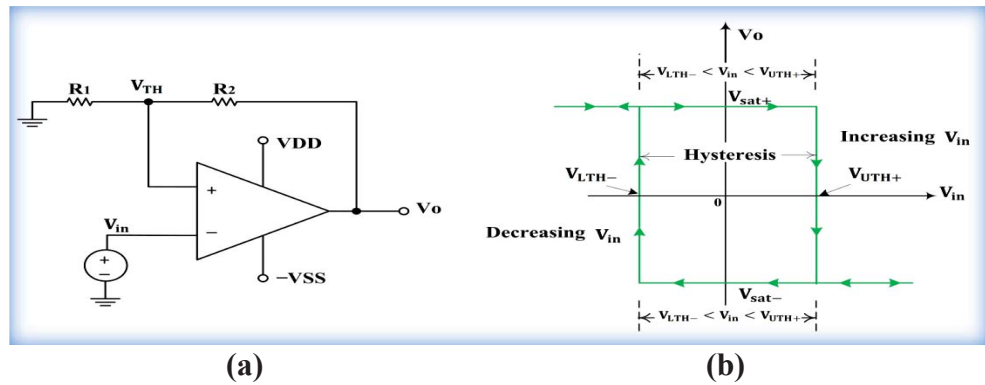


Figure 2.3. Schmitt Trigger, (a) basic Schmitt trigger circuit and (b) voltage transfer characteristic of the Schmitt trigger.

Because of the positive feedback, the threshold voltage simultaneously drops, emphasizing the input voltage. As the input decreases from a high level and crosses a low threshold ( $V_{LTH} = -\beta V_{sat-}$ ), the output switches high again, to  $V_{sat+}$ , and the threshold voltage simultaneously increases, again emphasizing the input voltage, then the system returns to the original state. Therefore, the Schmitt Trigger configuration exhibits hysteresis in its VTC. If the input signal is sinusoid, the circuit output signal is a pure square waveform. The hysteresis Schmitt Trigger's configuration does not respond to the input noise  $V_{noise}$ , as in a comparator configuration.  $V_{noise}$ , in hysteresis Schmitt Trigger's circuit, is smaller in value than the difference between the two threshold voltages, and can be given as in [52] by,

$$V_{noise} < \beta[V_{sat+} - (-V_{sat-})] = \beta[V_{sat+} + V_{sat-}] \quad (2.2)$$

Therefore, hysteresis Schmitt Trigger's output signal has no chatter (multiple output transitions) as in a comparator circuit, due to the presence of AC noise when the triggering input signal crosses the reference signal. Since in a basic comparator configuration, using Op-Amp circuit without using positive feedback, it compares the triggering input signal to a reference voltage to change its state. When the input signal exceeds the reference level ( $V_{Ref}$ ), the output becomes high and when the input signal is less than the reference level, the output becomes low [52]. Figure 2.4 shows the comparison between the output VTC of the comparator and of the hysteresis Schmitt Trigger circuit.

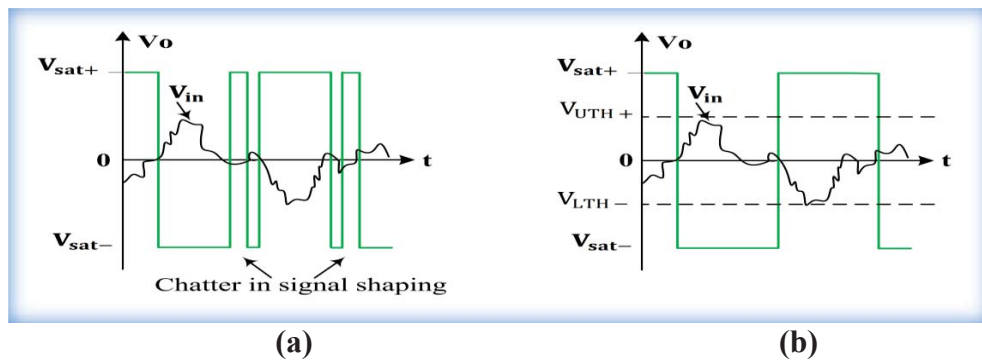


Figure 2.4. Comparison between the output voltage transfer characteristic of the comparator and the hysteresis Schmitt Trigger circuit, (a) comparator response to noisy signal, and (b) hysteresis Schmitt Trigger response to noisy signal [52].

The operation of a simple hysteresis Schmitt Trigger circuit with two stable states considered as a bistable circuit. Oscillator design conditions that utilize the hysteresis Schmitt Trigger concept with a relaxation timing network can be used for the applications of relaxation oscillators to perform useful functions, as in many astable multivibrator circuits that generate periodical square waveform signals [52, 80]. Hence there is rising interest in designing WFG circuits based on relaxation oscillators that employ a hysteresis Schmitt Trigger concept and a relaxation timing network, which will be utilized for the development of the biomedical device of this research.

## **2.5 Principles of Operation of Typically WFG Circuit**

Typically, a WFG circuit utilizes a combination of hysteresis Schmitt Trigger based positive feedback and a relaxation timing network circuit. The WFG circuit has time dependent elements which determine the frequency of oscillation. Its time constant is set by an appropriate network, normally comprising a capacitor. The circuit oscillates with no input and generates a periodical signal with a specific frequency that maintains infinity output. Generally, WFG can be classified based on a relaxation timing network circuit, which can be summarized as follows:

1. Resistor and capacitor (RC) relaxation timing network.
2. An integrator relaxation timing network.

The WFG circuit oscillates between two quasi-stable states with no external trigger input signal, remaining in its quasi-stable state for a fixed interval of time, and then returns to its original stable state [80]. Indeed, an internal trigger signal is produced which drives the circuit to return to its original stable state. Basically, the charging and discharging of a capacitor produces the required internal trigger signal. The component values of the timing network are used to set the time constant for which the circuit remains in each state.

### **2.5.1 Theory of WFG Based on RC Network**

Figure 2.5 shows a basic block diagram of a typical WFG circuit. The WFG utilizes a hysteretic Schmitt-Trigger circuit and passive RC relaxation timing network as negative feedback.

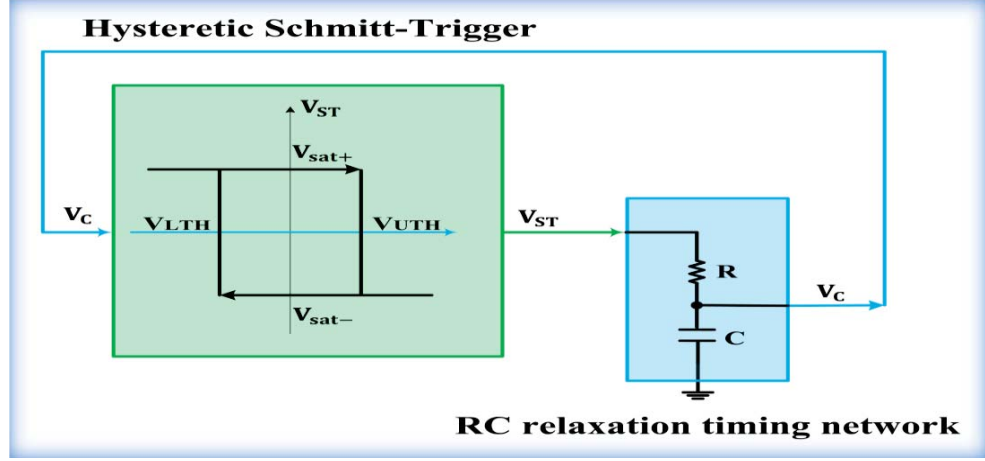


Figure 2.5. A basic block diagram of a typical WFG circuit, based on a RC relaxation timing network.

Infinity oscillation is achieved by switching the voltage source to charge and discharge the capacitor through a resistor  $R$ , which forms the internal trigger signal of the circuit. The output of the hysteresis Schmitt Trigger  $V_{ST}$  circuit oscillates between two quasi-stable states  $V_{sat+}$  and  $V_{sat-}$ , and is a function of the capacitor voltage ( $V_C$ ) internal trigger (input signal). The output of the circuit is saturated at its high positive level  $V_{sat+}$  for  $V_C \leq V_{LTH-}$  and is saturated at its low negative level  $V_{sat-}$ , for  $V_C \geq V_{UTH+}$ , where  $V_{UTH+}$  and  $V_{LTH-}$  are the upper and lower thresholds of the circuit respectively. The operation of the circuit as described in [52] can be given by,

$$V_{ST}(V_C) = \begin{cases} V_{sat+} & \text{if } V_C \leq V_{LTH-} \\ V_{sat-} & \text{if } V_C \geq V_{UTH+} \end{cases} \quad (2.3)$$

Initially, the state of the hysteresis circuit's output ( $V_{ST}$ ) is such that at its high positive level  $V_{sat+}$  for  $V_C \leq V_{LTH-}$ . The capacitor is charging, the voltage across the capacitor rises exponentially toward upper threshold level  $V_{UTH+}$  of the circuit. The state of the hysteresis circuit output remains at its high positive quasi-stable state for a fixed interval time  $TI$  until  $V_C$  reaches  $V_{UTH+}$ . As  $V_C$  exceeds  $V_{UTH+}$ , the inverting input (-) becomes positive with respect to the (+) input. This switches the output, so that it flips from  $V_{sat+}$  to  $V_{sat-}$ . As  $V_{ST}$  switches to  $V_{sat-}$ , the capacitor is discharging through  $R$  exponentially toward lower threshold level  $V_{LTH-}$  of the circuit. The state of the hysteresis circuit output remains at its low negative quasi-stable state for a fixed interval

time,  $T_2$ , until  $V_C$  reaches the  $V_{LTH-}$ . As  $V_C$  exceeds  $V_{LTH-}$ , switching at the output takes place so that it flips from  $V_{sat-}$  to  $V_{sat+}$ . The system then returns to its original stable state. This process repeats and the waveform becomes periodical. The time period,  $T$ , of the square waveform is determined by the charging and discharging time of the capacitor. However, the high output level of the WFG depends on the supply voltage, while the frequency ( $f_o = 1/T$ ) of the generator circuit is set by the RC time constant; the higher the RC, the lower the frequency which can be then achieved. Based on the periodical charging and discharging operation of the capacitor,  $C$ , the WFG circuit provides a periodical square waveform output signal at  $V_{ST}$  and exponential waveform at  $V_C$  with no input.

### 2.5.2 Theory of WFG Based on Integrator

The basic block diagram of a typical WFG circuit that utilizes a combination of hysteresis Schmitt Trigger and an integrator as a timing network is shown in Figure 2.6.

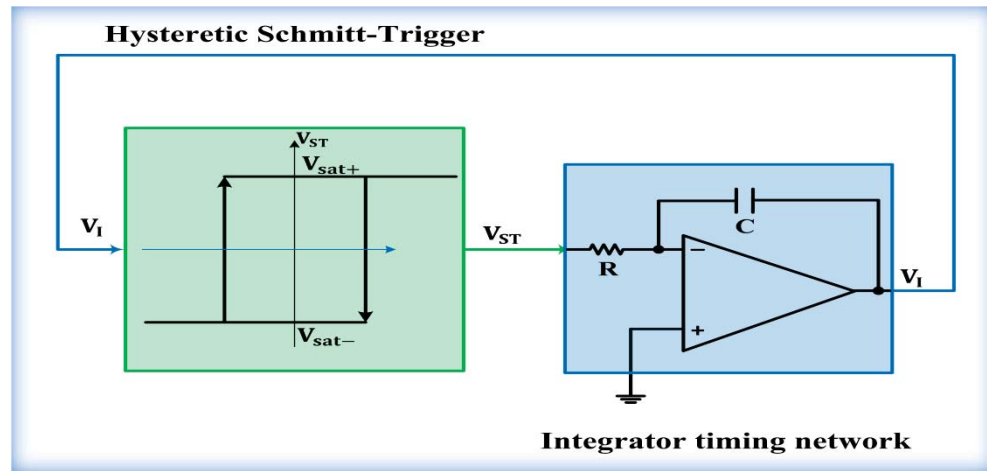


Figure 2.6. A basic block diagram of a typical WFG circuit based on a hysteretic Schmitt trigger and an integrator relaxation timing network.

The integrator is a useful building block circuit formed from an active Op-Amp and frequency-dependent feedback RC circuit. The integrator circuit provides a ramp output voltage  $V_I$  that is the integration of the input voltage  $V_{ST}$  in the time domain. The operation of the circuit as described in [52, 53, 81] can be given by,

$$V_{ST} (V_I) = \left\{ \begin{array}{ll} V_{sat+} & \text{if } V_I \geq V_{I+} \\ -V_{sat-} & \text{if } V_I \leq -V_{I-} \end{array} \right\} \quad (2.4)$$

The output of the circuit consists of two integration intervals,  $T1$  and  $T2$ . When the state of the hysteresis circuit output,  $V_{ST}$ , is such that at its high positive,  $V_{sat+}$ , then it is applied to the integrator input  $V_{ST}$  is integrated for a fixed interval time,  $T1$ . The integrator output  $V_{I+}$  will decrease linearly to its  $V_{I-}$  with time, at the rate  $+V_{sat+}/RC$ . The progression of the hysteresis circuit will be towards  $V_{sat-}$ . When  $V_{I+}$  reaches its low negative level  $V_{I-}$ , the output  $V_{ST}$  switches, so that it flips from  $V_{sat+}$  to  $V_{sat-}$ , and it is applied to the integrator input. The state of the hysteresis circuit output remains at its low negative quasi-stable state,  $V_{sat-}$ , for a fixed interval time,  $T2$ . The integrator output,  $V_{I-}$ , increases linearly to its  $V_{I+}$  with time at rate  $-V_{sat-}/RC$ . The progression of the hysteresis circuit now will be towards  $V_{sat+}$ . As  $V_{I-}$  reaches  $V_{I+}$ , another switching at the output takes place so that the output,  $V_{ST}$ , of the circuit again becomes  $V_{sat+}$ . The system returns back to its original stable state, starting a new cycle and generating a predictable waveform. The time period,  $T$ , of the square waveform is a function of the integrator output  $V_{I+}$  and is determined by the charging and discharging time of the capacitor. The resultant hysteretic Schmitt Trigger output is a square waveform signal,  $V_{ST}$ , while the integrator output,  $V_I$ , is a triangle waveform signal.

## 2.6 Waveform Generator Approaches

The previous sections introduced the oscillator circuit, model and theory that can be applied to develop a WFG circuit. This section provides a review of the most commonly used WFG architectures based on hysteresis Schmitt Trigger and the relaxation timing network. Taking a top-down approach, a series of WFG architecture circuits are discussed stage by stage and individual circuits are analysed.

Today, the advances of CMOS technology enable the integration of complete largely mixed analog-digital signal process systems on a single chip. Recently, research in the field of analog CMOS circuits has gained attention and these have become an important design aspect of any low-power signal generation system. Linear and non-linear circuits, like amplifiers, integrators, and WFG are necessary analog building



blocks, since their components often critically define system performance. In order to accomplish a high performance, these circuits are typical architecture in the way that their function is principally determined by a few carefully selected passive components, including resistors and capacitors, which are primarily used in these circuits, while active components are mainly used to provide appropriate gain. However, analog signal generation can be more valuable in terms of chip area and power dissipation, particularly for low speed and accuracy circuits [66] since WFG architectures based on oscillators are considered complex digital circuits, and supply voltage  $V_{DD}$  in digital WFG model has to be adequately high to ensure robust operation of the circuit. Also, switching activity of the logic gate in a digital oscillator increases dynamic power dissipation, resulting in high power consumption in the device, and power dissipation is a strong determinant of cost [3]. Furthermore, in applications that require a variable output signal, to electronically control amplitude and frequency, analog design is preferable in terms of accuracy and power dissipation of the circuits. Therefore, an analog model is the most appropriate in designing an ultra-low power WFG circuit. Particularly in biomedical applications, the analog WFG model is ideal and a dominant solution, since speed requirements are typically modest, while power efficiency is of primary importance. Thus, this section will focus only on presenting analog WFG approaches.

A typical voltage mode WFG circuit utilizes a comparator or Op-Amp with a combination of positive feedback and an RC time constant element. It operates by switching a voltage source to charge and discharging a capacitor. [52, 79, 82]. Voltage mode WFG has poor frequency stability and low slew rate, since the performance of this circuit is restricted by the signal bandwidth and slew rate of the Op-Amp [83] and its dynamic range is controlled by the frequency-dependent gain of the operational amplifier. Besides, the circuit employs passive elements, to set its time constant, and hence, its frequency and amplitude cannot be electronically controlled [84]. In [85] it is demonstrated that such circuits have non-ideal and highly nonlinear behaviour. However, using Op-Amps circuits and some commercial ICs to construct such WFGs, the internal circuits are relatively questionable and complicated. A common drawback of voltage mode WFG circuits is that they require high supply voltage, and extra passive components are often necessary which vary with process conditions, and would incur loss of accuracy [86]. In addition, the adjustable time constant of these circuits requires

complex tuning circuits such as digitally controlled switched-capacitor or switched-resistor matrices. Because of such limitations, the voltage mode circuits are therefore considered relatively complex and as a high-power solution which is not desirable in low power applications [87].

Analogue WFG implementation using current-mode (CM) techniques offers advantages over the voltage mode counterpart due to the simplicity in implementation, and compact structures, requiring less active and passive components. Furthermore, current scaling and replication is realized simply by using current mirrors [58, 88, 89]. Therefore, there is a growing interest in developing the CM circuit because of its potential to operate with low supply voltage and achieve relatively large dynamic range with good linearity [73, 90-94]. It also provides an attractive low power circuit design, which is becoming rapidly dominant in conventional approaches based on voltage-mode designs [92]. Consequently, a wide variety of developments of CM analog circuits have been the beginning of new building blocks, ranging from the current conveyors (CCII) through to operational trans-conductance amplifiers (OTAs).

Current conveyors are one of the CM building blocks which, from its introduction in 1968, and earlier formulation in 1970, has proved to be functional and versatile. Besides, it has been revealed that the main advantages of current conveyors over conventional Op-Amps is that they are capable of providing wider bandwidth and accuracy [95]. The structure of the CCII approaches has the ability of the circuit to act as a voltage buffer between its inputs and to convey current between two ports at extremely different impedance levels [73, 96]. Since the first CCII active oscillators were developed in 1975 by Soliman [97] many researches have been extended to develop hysteresis Schmitt Trigger based on the CCII building blocks as relaxation oscillators. One of the earliest CCII based nonlinear Schmitt Trigger circuit was built the first time in 1995 [95]. The circuit was built using one CCII and three passive resistors. This Schmitt Trigger circuit has been commonly used in the realization of relaxation oscillators and square/triangular WFG [83, 95, 98-100]. However, this Schmitt Trigger circuit is not electronically tuneable, and uses a floating resistor which is not preferred in IC implementation [76].

A number of CM based Schmitt Trigger configurations as relaxation oscillators were using the first and second-generation CCII proposed in the literature [73, 76, 83, 97, 99-104] which were configured using a single or many CCII and/or a current

feedback operational amplifier (CFOA) [105] with passive and floating resistors and capacitors. A current conveyor based Schmitt Trigger was configured for a low frequency (0.24kHz) square-wave generator for interfacing for sensors in [100]. The circuit consists of two AD844 CCII+ along with five external passive elements (three resistors and two capacitors). The first CCII+ acts as an astable multivibrator which oscillates and generates a square-wave output. The second CCII+ integrates the square wave to generate a triangular wave output. The frequency of the oscillator and its amplitude can be adjusted only through the passive grounded capacitor and grounded resistor which may vary with PVT variations. In addition, this CCII+ based WFG employed  $\pm 15\text{V}$  supply voltage. A current conveyor based Schmitt Trigger as a relaxation oscillator was employed also for a low frequency (80Hz) square/triangular waveform generator in [73]. The circuit was built using three commercially available discrete second generation (CCII+) ICs (AD844AN), along with seven external passive elements (six resistors and one capacitor). In addition, this CCII+ based WFG used  $\pm 6\text{V}$  supply voltage. Moreover, the CCII+ components used are essentially monolithic current feed-back operational amplifiers, comprising many internal circuits. Another current conveyor based square/triangular wave oscillator for low frequency (24.1kHz) capacitive analog sensor interfaces was proposed in [104]. It is based on two CCII+ elements, a floating capacitor and six resistors. The oscillator was simulated using the AMS  $0.35\mu\text{m}$  CMOS technology with each CCII+ consisting of 18 transistors and two resistors. The measured results were based on AD844 discrete CCII+ components (using  $\pm 15\text{V}$  rail voltage).

Recently, a low frequency (99Hz) square/triangular WFG with wide oscillation frequency range utilized two CCII+ as active elements and three grounded resistors and one grounded capacitor was proposed in [106]. It is used in a wide range capacitive/resistive sensor front end. The experimental measurements have been performed employing AD844 and passive components using a high supply voltage of  $\pm 9\text{V}$ . The main drawback of the CCII+ WFG design of [100], [73], [104] and [106] was using a high supply voltage resulting in high power consumption. There is also a large device count in each CCII+ component as well as large input differential pair device size for the AMS  $0.35\mu\text{m}$  CMOS monolithic design in [104]. In addition, the circuit employs passive elements to set its time constant, hence its frequency and amplitude cannot be electronically controlled, and the temperature sensitivity of the required extra

discrete passive component in these CCII+ implementations would also incur loss of accuracy.

However, WFG based on CCII has better frequency stability compared to voltage mode. Its frequency is determined and controlled by the passive device (grounded capacitors and resistors). Since the passive components values alter in integrated circuit, resulting from PVT variations [76], and their values are not adjustable, the time constant of this integrator must be tuned with suitable tuning circuits. However, tuning the passive devices to obtain accurate frequency response characteristics is difficult [107]. It is well known that CCII are limited for practical design requiring component matching conditions with extra components for implantation as well as complex tuning circuitry; they will be more complicated to design, and consume more power with a large chip area.

Currently, an alternative approach utilizing an operational trans-conductance amplifier (OTA) has attracted consideration for analog circuit design, due to its high performance and flexibility [54]. It classifies a very simple and robust topology that can be designed to be electronically tuneable, providing optimum oscillation frequency values for a particular specification, and for most of its parameters including DC gain, output swing, linearity and other parameters in the performance of the system [108]. State-of-the-art analog CMOS technology driven design is bringing about remarkable growth from the development and application of OTA designs. It provides an attractive low power, low cost circuit design solution. The IC pioneers who developed OTA utilizing CMOS for the first time in 1984, were H. Khorramabadi and P.R. Gray [109]. By adopting a novel CMOS active device based OTA, a number of implementations have emerged, such as oscillators, active filters, and WFGs [110-114]. Of particular interest here is a current-controllable WFG based on OTA which can be designed utilizing a relaxation oscillator circuit. Simple WFGs can be realized by employing an OTA as a switching current source for charging and discharging a grounded capacitor followed by a Schmitt trigger. These WFG features are simple in implementation and compact configuration with a wide swing capability compared to other existing designs [86, 107, 115-117] They have good frequency stability and can be designed for electronically controlling its frequency and amplitude [84, 107].

The first current mode WFG circuit was developed by Filanovsky [117] shown in Figure 2.7(a). It employs a single differential N-MOSFET OTA with four resistors

and an RC relaxation timing network. It represents an alternative to the free running multivibrators with a conventional Op-Amp. It oscillates and generates a square waveform output signal with oscillation frequency of 5.78kHz which was used for sensor signal applications. Filanovsky [117] also developed a generator based on two differential N-MOSFET OTAs and four external elements, as shown in Figure. 2.7(b), to facilitate wide range frequency control in the range of 5kHz-700kHz, as bias current is varied from 3 $\mu$ m-1mA. This circuit delivers a linear dependence of the oscillation frequency on the sensor control current. These designs used a  $\pm 8$ V supply voltage resulting in high power consumption, with the main drawback being the temperature sensitivity of the extra passive resistors used, and the large silicon area due to the use of large capacitor values.

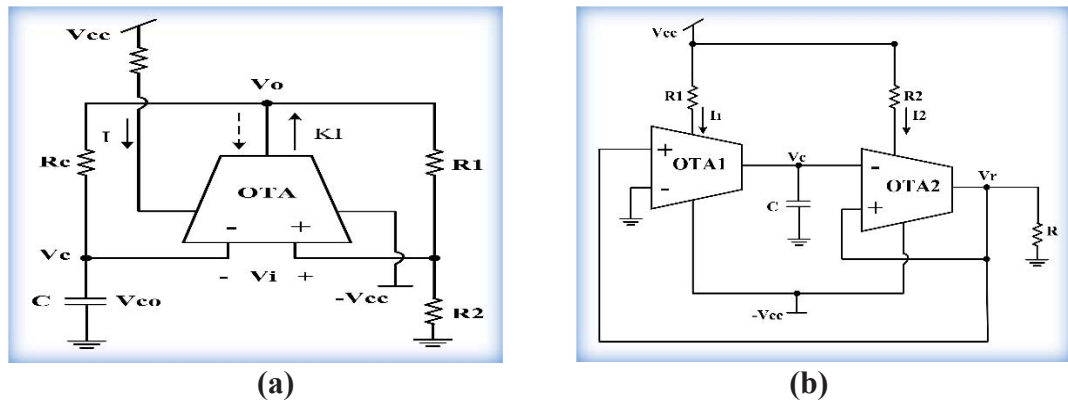


Figure 2.7. Waveform generator architectures based on, (a) single differential N-MOSFET OTA, (b) two differential N-MOSFET OTAs [117].

Another of the earliest available square/triangle wave voltage control oscillators (VCO) with a wide swing capability was realized using discrete LM3080 ICs OTA in [110]. The VOC circuit was based on the first order OTA-C integrator, along with a Schmitt Trigger circuit as shown in Figure 2.8. Its Schmitt Trigger was configured based on two active elements, the MC14575 CMOS comparator and OTA with one passive resistor. An extra two resistors for the voltage divider circuit was used in the input of OTAs. The oscillation frequency/bias current characteristic was measured in the range of 5 $\mu$ A-200 $\mu$ A, which demonstrated good linearity. The temperature stability of the output frequency is maintained to within  $\pm 60$ ppm/ $^{\circ}$ C over a

wide frequency range (10kHz-40kHz). The circuit was operated using a high supply voltage of  $\pm 5V$ .

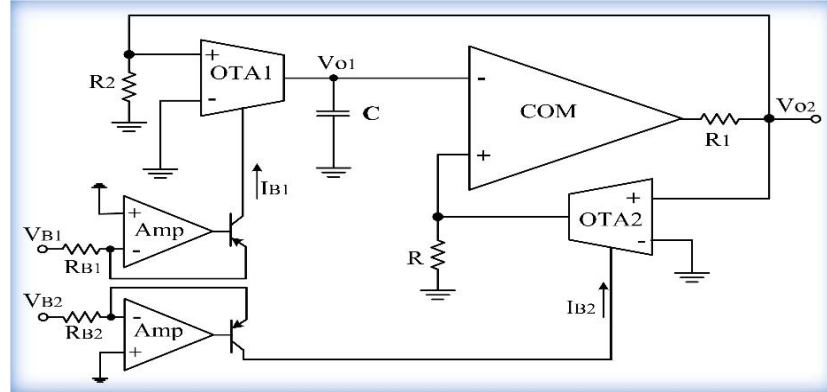


Figure 2.8. WFG architectures based on discrete LM3080 ICs OTAs and one comparator [110].

The Pseudo-differential CMOS OTA was also used for the design of fully differential relaxation oscillators to generate a square waveform in [111]. The OTA circuits were fabricated in a  $1.2\text{-}\mu\text{m}$  CMOS process to produce sub-oscillation frequency of  $0.7\text{Hz}$  for biomedical applications. The oscillator circuit is basically an integrator in series with a Schmitt Trigger, in a positive feedback loop, as shown in Figure 2.9. The integrator circuit was based on the second order OTA-C filter building block.

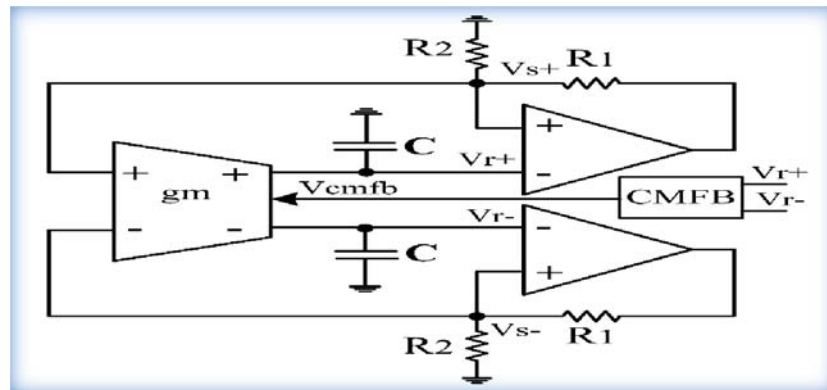


Figure 2.9. WFG architectures based on one OTA and a two-stage comparator [111].

Its Schmitt Trigger circuit was based on a two-stage comparator and six passive elements (four resistors and two capacitors). It provides good tuning range and a large input voltage swing. The main drawback for the both the Schmitt Trigger circuit in [111] and [110] designs was using a comparator which is the main noise source in the circuit. As previously mentioned in section 2.4, the comparator can amplify the noise in the input signal, causing chattering, which distorts the output signal. However, these two circuits are further complicated requiring a large components account (extra active and passive elements) and high supply voltage.

Figure 2.10 shows a WFG circuit based on a single dual-current output OTA (DO-OTA) and two external passive components to generate a clock signal, as proposed in [86]. The DO-OTA was built using two discrete single-ended commercial CA3080 OTA ICs to provide oscillation frequency of about 1Hz, 10kHz and 100kHz, with different capacitor values for clock signal applications. Based on the first approaches, in [86] they developed a second WFG by adding N-MOS as a switching element to generate a pulse waveform output. These two WFGs can also be electronically tuneable, by varying the DC bias current. Although these WFG designs are compact configurations, the supply voltages used were high in the range of  $\pm 5V$  to  $\pm 10V$ .

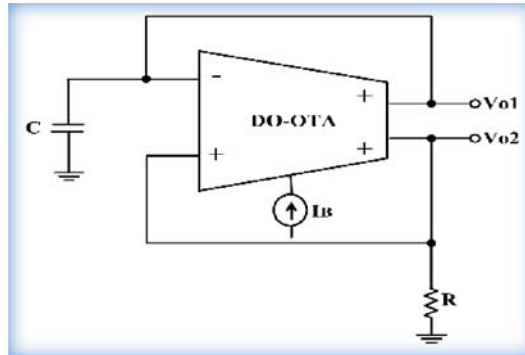


Figure 2.10. WFG architectures based on a dual output DO-OTA, using two single-ended commercial CA3080 OTA ICs [86].

CM generator circuits employing three OTAs and three passive elements were proposed in [77] (integrated) and in [116] (using discrete LM13600 ICs), as shown respectively in Figure 2.11 (a) and Figure 2.11 (b). In addition, in [107] they



implemented a square wave generator circuit, similar to that in Figure. 2.11 (b), but with the addition of an extra OTA and buffers for final signal shaping and inversion. These later circuits have been modified from the astable multivibrator WFG circuit in [52, 80] to one with frequency and amplitude control. To achieve electronic tunability, the Op-Amp circuit was replaced with OTAs.

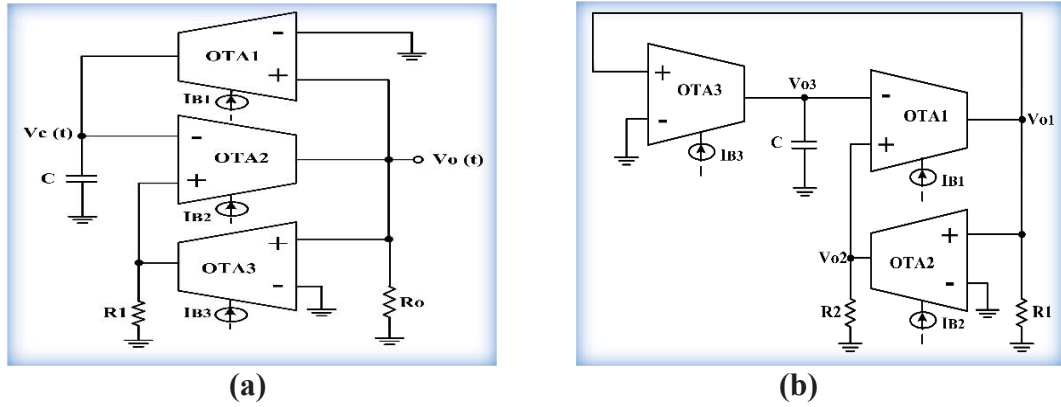


Figure 2.11. WFG architectures based on (a) three CMOS OTAs [77], (b) using three commercial available LM13600 ICs [116].

They have the advantage of good frequency and amplitude stability, as they can be linearly controlled through the DC bias current. They are implemented using three OTAs and three passive elements. They were constructed to use for low frequencies and a wide tuning range of amplitude and frequency applications, such as a clock (carrier) signal employed in a multipurpose modulator circuit by feeding the input signal at different nodes in the circuit, as in [77]. It is also used for integrated sensor signal processors with good temperature stability as in [116] and [107]. However, the use of three or more OTAs can result in increased chip area and power consumption [76].

Recently, in some WFG design approaches, a hybrid approach using the CM analog building blocks that utilize CCII and an OTA was demonstrated, and the related applications have been reported. One example in [118] employed two circuits to generate square/triangular waveforms. It is based on a CCII, a capacitor, a BJT based OTA and a voltage divider network. The frequency can be tuned by changing the voltage division ratio or the time-constant (RC values). The performance was measured using a commercial CFA AD844 and OTA LM13700, with a high supply voltage



( $\pm 12\text{V}$ ) and consuming high power (192mW). Moreover, the saturation voltage of the circuit is less than expected, due to the use of a voltage divider. The experimental results showed that a part of the current which flows into this BJT based OTA, through the voltage divider network, further limited the output swing. They reported that a CMOS OTA would perform better, due to higher input impedance than the BJT counterpart.

The design and implementation of the two CM evolution approaches (CCIIs and OTAs) of WFG were discussed. It can be concluded that both architectures can be utilized for WFG design using active and passive components. The CCIIs solution is further complicated due to the fact that extra active CCIIs and passive components are required. In addition, in CCII architectures one or more floating resistors and capacitors are essential, which not desirable in IC implementation. Moreover, CCIIs have poor frequency stability and suffer from lack of independent electronic control over the oscillation frequency and the output level, compared with OTA architecture. CCII frequency is controlled using passive devices (grounded capacitors and resistors), and their values alter in an integrated circuit, resulting from PVT variations. Since their values are not adjustable a complex tuning system is then required to obtain accurate frequency response characteristics. This makes them inappropriate for low power applications. Using a few active and passive components can also reduce the PVT variations.

However, OTAs circuit configuration has been recognised for a remarkably long time, as the same principle is still used in today's CMOS based WFG. It can be designed and implemented with relatively few CMOS devices and passive components. Additionally, its amplitude and frequency can be electronically controlled, allowing more flexibility. Since the  $gm$  of the OTA circuit can be controlled directly by the DC biasing current, tuning of the amplitude and frequency, with simple tuning circuitry, can be also designed and realized easily. It has a simple and compact structure, compared with a number of other architectures. One advantage of using CMOS technology is that the aspect ratio ( $W/L$ ) of every transistor can be chosen differently to suit the design requirements, in contrast with bipolar technology, where the transistors have the same dimensions and may not satisfy the design requirements. Therefore, WFGs based on CMOS OTAs can be designed and integrated for a power efficient and small chip area solution for a low cost longer battery-life biomedical device for this research project.

Since the overall performance of WFG circuits can be determined by the transconductance characteristics, an appropriate design can be then achieved by determining its controllable variable parameters and analysing the important trade-off between these variables for high gain, low frequency design and low power consumption and optimizing silicon area. (This will be discussed in the following chapters).

### **2.6.1 Relaxation Timing Network Approaches**

There is a powerful motivation for developing integrated solutions for WFG circuits that are competent to operate at very low frequency. Low frequencies design is conventionally achieved by using large off-chip capacitors. This is in contrast with the typical trend of implementing complete systems on-chip which has the advantage of increased reliability and packaging simplicity by eliminating the external components [119]. There are two on-chip operative aspects in low speed design. One involves the most common technique including passive-RC with very large capacitors (typically in the order of several hundred pico-farads) on-chip, while others are realized using active integrator building blocks [111]. The choice is dependent on the design specification and applications. However, many applications require that WFG is electronically tuneable; their oscillation frequency is a function of a control input, typically a voltage. The required tuning range is directed by two factors: (1) the variation of the frequency with PVT and (2) the frequency range necessary for the applications [58].

#### **2.6.1.1 Passive RC Approaches**

The passive-RC circuits are the most used to realize relatively very low frequencies in the range of sub-Hz to kHz. Large capacitor values are then required for a large time constant. Typically, the capacitor is mostly implemented off-chip, to reduce the chip area. However, on-chip, a large capacitor such as double-poly or metal-metal capacitors is used, with the passive-RC technique [72]. For full integration of the passive-RC circuit, without the need for a large capacitor, many approaches can be used, involving increasing the resistance needed to produce a large time constant [66]. The important thing in implementing fully integrated analog single large resistors is to find a proper form for resistors that are available in a standard CMOS technology. The conductive layers in CMOS technologies can be used to design an appropriate resistor. The actual resistance value is set by changing the length and width of diffused regions

[120]. The main drawback of using fully integrated large resistors is the self-heating of the resistor due to non-uniformity of the composition inside the component which causes change in the current distribution, leading to non-uniform power dissipation [121].

The RC circuit noise sources analysis model was studied by [3, 58] to obtain the total power spectral densities (PSD) in the RC output circuit. By modelling the noise of  $R$  by a series input noise voltage, the total power spectral densities (PSD) in the circuit are then given by,

$$P_{n,out} = \frac{kT}{C} \quad (2.5)$$

Where  $k$  is the Boltzmann constant,  $T$  is the absolute temperature and  $C$  is the load capacitor. The interestingly simple  $kT/C$  result reveals that the total noise at the output of the RC circuit is independent of the value of the  $R$  and is limited by the size of the capacitor. Indeed the noise source  $kT/C$  in a RC circuit affects the performance in high-accuracy applications. In order to minimize the noise in the circuit, a large capacitor value is then required. Table 1 in [54] provides a comparison between capacitor values and corresponding  $kT/C$  noise (the total rms noise voltage at the output  $\sqrt{kT/C}$ ) at 300 °K.

Table 2.1. A comparison between capacitor values and corresponding  $kT/C$  noise.

Capacitor values, pF	$\sqrt{kT/C}$ , μV
0.01	640
0.1	200
1	64
10	20
100	6.4

### **2.6.1.2 Active Integrator Building Block Approaches**

Another approach for a low frequencies timing network can be realized by designing active integrator building blocks. Active components that replace the passive components can significantly reduce power and chip area consumption. It is considered the most effective technique and widely used today, in IC signal processing and signal generating system design. Furthermore, electronically tuneable circuits attracted interest in the implementation of analog WFG, since in practice, tolerances of the electronics components in IC are unacceptable and hence, after manufacturing, fine-tuning is necessary. These can also be designed for low frequency applications to eliminate the need for using a large and invariable passive resistor and capacitor [122]. An active integrator building blocks configuration can be varied from single-stage form to lossy integrator form. The later design involves a number of active components in parallel with the single integrator, their outputs connected together to build a summing integrator that enhances the integrator gain [123]. The most accurate active integrator design is to minimize the integrator stages. Coupling between integrators in multiple stages or N order is limited for practicable design. They require accurate matching of the characteristic frequencies and tuning circuit's technique with additional components (extra active and passive elements for implantation). In addition, linearity is also essential in multiple stages integrators, since it specifies large input voltage and hence a linearizing system is required [59]. They will be more complicated to design, being noisy circuits, consuming a large chip area and high power. For a low power, low noise application, the most appropriate approach is by using less order integrator form [66, 124].

Since 1960, considerable research has realized the integrators design, using discrete circuit implementations with single-ended circuitry. Although several theoretically pleasing designs were invented and used commercially, for discrete design, only a few of the circuit approaches are well designed to VLSI implementations. Integrator realizations are extensively discussed in [3, 66, 125]. Currently, there is a wide range of integrator building block techniques well designed for VLSI implementations. The two most common techniques include the Op-Amp-RC and gm-C integrator building blocks [66]. However, the choice and the design of an integrator building block depends on the system specification and performance.

**1. The Op-Amp-RC Technique** is realized using a single Op-Amp and RC circuit as shown in the typical integrator relaxation timing network Figure 2.6. This technique uses a closed-loop circuit to design a single active integrator circuit. A lossy Op-Amp-RC integrator can be simply built by connecting an additional resistor in parallel with the feedback capacitor without the need for an extra active element [123, 126]. The time constant of an Op-Amp-RC integrator is determined by the RC circuit [123] which has the same limitations as in the passive-RC technique already discussed in section 2.6.1.1. In addition, to gain a wide tuning range, the time constant of this integrator must be tuned with suitable tuning circuits such as digitally controlled switched-capacitor matrices as shown in Figure 2.12. Furthermore, Op-Amp with sufficient gain requires a multi-stage topology, which imposes more components and will consume a large amount of power.

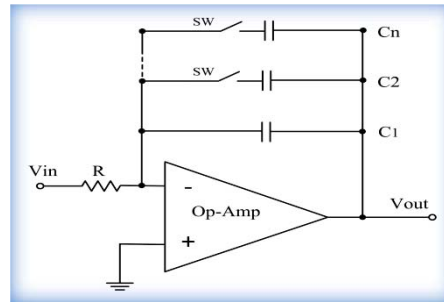


Figure 2.12. Op-Amp-RC integrator (a) first order Op-Amp-RC Integrator, (b) digitally controlled switched-capacitor matrices for tuning the time constant of the Op-Amp-RC integrator circuit [59].

Because of such limitations, the Op-Amp-RC technique is generally considered as a high-power solution which is not desirable in low power applications [87]. It is obvious that the Op-Amp-RC technique is generally considered as a high-power solution; such limitations preclude the use of these integrators in low power design, and an appropriate voltage or current control scheme for externally adjusting the integrator characteristics does not exist.

**2. A gm-C Technique** basically implements an operational transconductance amplifier loaded by a capacitor, as shown in Figure 2.13. It converts the input voltage ( $V_{in}$ ) to an output current and is considered as a voltage-controlled current source, characterized by

its  $gm$ . The output current signal is then integrated at the tran-sconductor output by the capacitor  $C$ , to provide the output voltage signal ( $V_{out}$ ). The time constant of a gm-C integrator is determined by the capacitor  $C$  value and its tran-sconductor ( $gm$ ) [123]. For a large time constant, a large capacitor is also required. An active gm-C integrator, however, can be implemented in CMOS process technology to operate with appropriately low frequencies, by controlling the parameters of its  $gm$  without the need for large capacitor values [111, 119]. Its frequency can easily be tuned, using either a digitally controlled switch capacitor system or by adjusting the  $gm$  [124]. Since the  $gm$  gain is a function of a bias current, which can be controlled directly by the DC biasing current, the oscillation frequency can be easily electronically tuned by varying the  $gm$  of the integrator circuit [52, 54, 59, 66, 84, 122, 127].

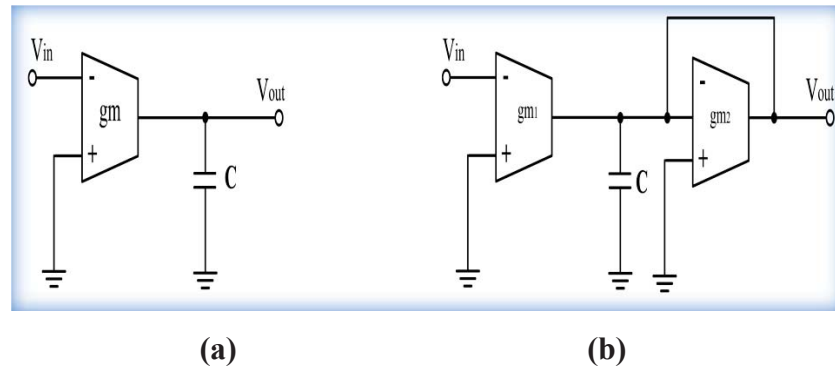


Figure 2.13. Gm-C integrator (a) first order integrator, (b) a lossy integrator [123].

In a gm-C integrator, grounded or floating capacitors can be used at the tran-sconductor output. The latter can be realized with metal-metal capacitors, while, the grounded capacitors can be implemented with either metal-metal capacitors or with MOS capacitors based on MOSFET gate capacitors. Practically, in the gm-C integrator technique, only grounded capacitors are typically preferred, as the use of floating capacitors results in the top-plate and bottom-plate parasitic [123, 128]. The parasitic capacitance of the tran-sconductor must also be taken into account. These parasitic capacitances have significantly affected the value of the integrating capacitor, and hence the time constants of the integrator [59]. A gm-C integrator serves as the basic building block in many integrator structures. A lossy gm-C integrator, Figure 2.13 (b), can also be formed by adding another-stage tran-sconductor that is coupled in parallel, with the

first stage to construct a summing integrator, which requires extra MOSFET transistors and consumes more chip area and power. Many applications are designed with a few order gm-C integrator and hence, they are attractive for low power integration. The component count of these structures is often very low [129]. A prevailing advantage of the gm-C technique is that its  $gm$  can be designed for low frequency applications, and can be controlled directly by the biasing current. In addition, the open loop gm-C technique does not have speed limitations as in the closed-loop Op-Amp-RC technique [123]. Accordingly, the gm-C integrator approach is the most preferred for the implementation of an electronically tuneable circuit [3, 59].

From the above statement, it can be concluded that a gm-C integrator is typically considered as practical relaxation timing network solution, and has great potential for working at a low frequency with low supply voltage which can suit the design of this project. The  $gm$  will be a design parameter, much as are resistors and capacitors, and the main emphasis will be placed upon those designs in which the key parameters of interest are proportional to the  $gm$  of the OTA. The performance of a gm-C integrator, involving its gain, transfer function, frequency and linearity, is then dependent directly on the  $gm$  characteristics, and hence, an accurately designed value of the  $gm$  is desirable for the integrator transfer function.

Generally, in a linear system the dynamic range of the integrator, the ratio of the power in the maximal undistorted input to the minimum detectable signal is calculated at the corner frequency  $f_c$ , its maximum signal-to-noise ratio (SNR) which can be given as in [3],  $[SNR = (V_L^2/2)/(V_{noise}^2)]$ , where  $V_L^2/2$  is the maximum signal power achievable at the output with no distortions, and  $V_{noise}^2$  is the noise signal. In a nonlinear system with gain control, the dynamic range can significantly exceed the SNR. This is due to the fact that the system adapts its gain to handle a wide range of input levels. Therefore, at any given gain setting, the SNR and straightforward dynamic range are identical, but over its whole range of gain settings, the dynamic range significantly exceeds the SNR. For a nonlinear system, as in an oscillator circuit, there may be a maximal SNR, equivalent to 4 orders of magnitude at any given gain setting. It can also handle eight orders of magnitude in the dynamic range (1mV to 10V inputs) over its entire range of gain settings [3]. However, the cost of achieving a wider linear range  $V_L$  in the integrator, for a given bandwidth, is not free. If the bias current of

the  $gm$  is  $I_B$ ,  $V_L$  is the input linear range,  $C$  is the capacitor load, then the bandwidth of the integrator  $f_c$  can be given as in [3] by,

$$f_c = \frac{I_B}{2\pi C V_L} \quad (2.6)$$

The power needed to achieve a large  $V_L$  for a given bandwidth can be given by,

$$P = 2VDDI_B = 2VDD(2\pi C f_c V_L) \quad (2.7)$$

Equation (2.7), shows that for a given bandwidth a large power consumption is required to attain a large  $V_L$ . However, gm-C integrator based OTA design that converts the input voltage to an output current with very small transconductance and high linearity, should have high input impedance to accurately sense the input voltage signal. High output impedance is required so the output signal appears as a current source, as well as high DC gain with wide bandwidth, so as not to create phase and magnitude errors in the integrator response. Also large signal handling capability is needed at the input and output for good dynamic range, as well as a practical tuneable mechanism to be used for electronically frequency tuning [59, 66].

In today's technology, an accurately IC implemented gm-C integrator with corner frequencies from below 1Hz to over 1GHz can be achieved, if sub-threshold or above-threshold operation, with capacitance scaling and a simple tuning technique applied [3]. System level performance and power dissipation can be predicted by modelling the behaviour of individual MOSFET transistors. The short channel devices, such as 130-nm CMOS optimized for operation at a low supply voltage, can achieve excellent performance, provided that the supply voltage is lowered along with threshold voltage, since the threshold voltage has a considerable amount of the available headroom. However, architecture plays a key role in determining power; a high order integrator gm-C measures the complexity of the circuit, including the number of devices required to implement it. In addition, the bandwidth, precision and technology have significant effects on determining the power of the circuit. All these characteristics will be analysed and considered carefully in the gm-C integrator design (chapter 4) of this research project.



## 2.7 Tuning Circuit Approaches

A WFG with variable tuning range is required due to: (1) the variation of the oscillation frequency with PVT variation and (2) the wide oscillation frequency range necessary for the applications. The oscillation frequency of some oscillator circuits varies by a factor of two, due to the PVT, thus requiring a sufficient tuning range to adjust the oscillation frequency to the desired value. This is also required, as some applications, including signal processes, and integrated clock frequencies, that vary by one to two orders of magnitude, depending on the mode of operation, require a wide tuning range [58]. Frequency tuning of the WFG can be achieved by many different complex approaches to tuning systems. The conventional tuning techniques are realized by using off-chip switched capacitor matrix “varactors” [123] (Figure 2.12 *and/or* a variable resistance. As mentioned above, since RC timing is mostly used to realize relatively low frequencies, large resistor and capacitor values are then required for a large time constant [80]. The tunability can also be enhanced by a fully implemented switched capacitor matrix, using the large capacitor values available in a standard CMOS technology, [72] which can be switched in and out for uneven tuning, while a variable resistance can be accomplished by using a bank of MOSFETs, as shown in Figure 2.14, [59]. Realizing this technique for a large time constant could provide a limited tuning range, and consume high power with a large chip area, which may be useful in some applications [130].

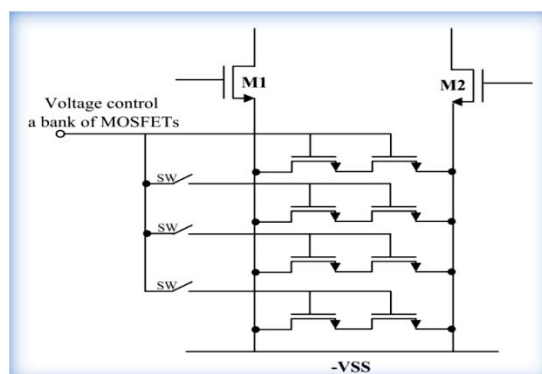


Figure 2.14. Resistive tuning techniques, voltage controls a bank of MOSFETs [59].

The model for the design of the gm-C integrator circuits for this work is to combine the low frequencies timing network with suitable tuning circuits. Since the advantage of using the gm-C technique is that its  $gm$  can be controlled directly by the biasing current, which can be used to vary the oscillation frequency of the WFG core, miniaturization with good performance is required for such circuits. Therefore, it is challenging to achieve a wide tuning range with good performance in a compact silicon area with low power consumption. It would be necessary to employ multiple stages or use  $N^{\text{th}}$  order gm-C circuits. Several approaches of CMOS circuits for the integrated gm-C circuit based on open-loop-integrator building blocks have been developed [123, 131-134], and the design involves a number of active and passive components. A lossy integrator can be formed by connecting an additional tran-sconductor to the integrator output, as shown in Figure 2.13b, while a linear system with  $N$  state variable would be built of  $N$  integrators with single coupling between any and all integrators. Also a summing integrator that enhances the integrator gain can be built by connecting an additional tran-sconductor to the integrator output, in parallel with the single integrator. The frequency scaling of the gm-C integrator circuits can be also achieved with a digitally controlled switched-capacitor matrices technique or by varying the  $gm$  of the integrators, by switching on and off parallel connected unit tran-sconductor. However, coupling between integrators in multiple stages or  $N$  order is limited for practical design. They are very complicated, as they require a large and component-intense circuit with high supply voltage resulting in high power consumption and large chip area. It also adds more complexity and noise to the circuit and may cause signal distortion [66]. The most serious disadvantages of design using such approaches is that the complexity and noise cause the shape of the integrator frequency response to deteriorate. Furthermore, the frequency response of the circuit becomes inaccurate and unperiodical when extremely wide bandwidths are being targeted [123]. Practically, using such approaches with complicated tuning systems in this research project is not preferred; the most accurate active integrator design is to minimize the integrator stages.

A first order gm-C integrator that is constructed with relatively few devices, will be used in this work. Since the  $gm$  gain of the OTA is proportional to an external DC bias current, external control of the integrator parameters over several decades, by controlling the bias current, can then be obtained. It is considered power efficient for a longer battery life, compared with a number of other topologies. The tunability of the

gm-C integrator is restricted by the limited bandwidth of  $gm$  that depends on the bias current. It is a challenge to implement a gm-C integrator that has both an appropriately wide bandwidth and high DC gain at once. This trade-off is more difficult to achieve with the very low supply voltages (1.2 V) of modern 130-nm CMOS technologies, particularly since, in this work, the focus is on a low power, small silicon area, WFG with wideband, in which the wide bandwidth and DC gain of the designed WFG become more necessary, compared to their narrower band counterparts.

The application configuration for bipolar electro stimulation employing two identical active electrodes requires output of WFG and its complementary signal, fed to the dual active electrode inputs, in order to drive the differential output signal to load resistor  $R_L$  in a differential fashion. In this research project, a novel tuning technique will be used, by designing a hybrid tuning system composed of an analog model and a digital model that is compatible with the applications requirement. Since the analog gm-C integrator design parameters ( $W$ ,  $L$ ,  $I_B$ ,  $gm$  and  $C$ ) are the key factors for an appropriate application, a wide tuning range of the WFG core, using a single MOSFET device as a current source, can be achieved, by setting up and control of these parameters by the designer, without requiring an extra complex and complicated circuit, while a digital model utilizing a frequency divider system will be also designed to provide a bipolar biphasic source that is fed into two identical active electrode circuits. A sufficiently wide band will be obtained to compensate for PVT variations, as required for low frequency biomedical applications.

## 2.8 Digital Model for Frequency Divider

Digital integrated circuit design is the basis of modern signal processing that is used in communications systems. The most important consideration when designing a digital integrated circuit is how to optimize the functions of the systems. The next main concerns are power and chip area. For proper digital systems design, it is important that the critical factors limiting the performance of the circuit can be identified and hence, appropriate power and area consumption can be approximated, and then minimized. Although the development of modern IC digital systems is typically complex, the fundamental concepts and the principles are not new. It is important, for quick and precise logical analysis of a complex digital circuit, to consider MOSFETs, as simple

logic-controlled switches. At this point, it can utilize most of the MOSFET characteristics to design a complete digital model that functions properly for low frequencies, and a low power frequency divider system in this research project. For robust digital circuit operation, symmetrical logic design is essential for proper functionality, while low threshold voltage with quantifiable MOSFET sizing, reduces power and chip area consumption [3]. However, in order to design high density digital circuits with high functionality, design trade-offs between size, power, and chip area are then important.

### 2.8.1 Frequency Divider Theory

In order to synthesize a wide range of low frequency signals, a frequency divider system can be utilized which can be realized using a “divide-by-two ( $f/2$ )” frequency division circuit as illustrated in Figure 2.15, with its waveform output.

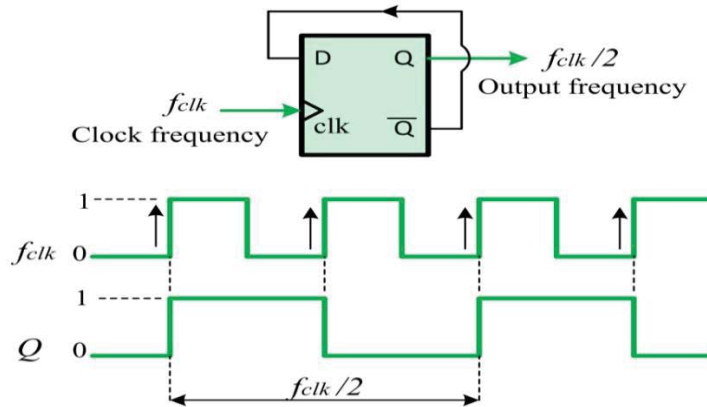


Figure 2.15. Schematic diagram of the frequency divider for “divide-by-2” ( $/2$ ) frequency division circuit with its waveform output.

The frequency dividers (FD) are basic building blocks that are mostly used in logic design, particularly for generating timing signals or clock dividers. They are mostly configured based on clocked flip-flops (FF), which are the storage circuit used to realize a synchronous logic circuit. Most of the clocked FFs have data input signals (D) and clock signals (clk), that save the state of the data input signal from one clock cycle to the next, therefore, they are principally synchronous in their operation, since the data

input signals change states in synchronism with the clock transitions [135]. A clocked FF, known more precisely as an edge-triggered FF, which can be positive edge-triggered or negative edge-triggered, responding to their input only at the transition of the clock. Typical clocked FFs have a differential output,  $Q$ , and the inverted output  $\bar{Q}$ . Their output values change only just after a clock edge. To configure divide-by-2 ( $f/2$ ) frequency division, the inverted output  $\bar{Q}$  of a FF is connected directly back to the D input providing the FF circuit “feedback”. Assuming the FF change on the positive-going transitions, then every positive edge of the output of the FF circuit will change its state, producing a square waveform output at one half the frequency of the input clock. The FF circuit divides the input frequency to produce frequency divisions by a factor of two. A range of low frequencies can then be obtained by using an appropriate N-stage of  $/2$  FFs circuit. The output signal at the last FF circuit will have a frequency that is equal to  $1/2^N$  of the input clock frequency [136]. For optimum performance, the design of the FF must be considered carefully, for low frequency circuits, and to satisfy the minimum requirements, including low power consumption and small chip area [136, 137].

### 2.8.2 Flip Flop Approaches

The FD has an important role in the signal generator and in signal processing systems, including clock generation. It dominates the operation frequency, power consumption and chip area of the system. In the early days, the IC designers were more intent on the performance and silicon area of the digital circuits. Reliability and cost also had core importance where power dissipation was a peripheral concern for them [138]. In recent years, power consumption is being given the same importance in comparison to silicon area and has become one of the important aspects in digital systems. This is because of the necessity to dissipate this energy in high-density circuits and to extend the battery life in portable systems such as biomedical devices [3]. Continually increasing demands for portable devices and the remarkable growth of this class of systems in biomedical applications, which require complex functionality and low supply voltage, has increased the demand for power efficient FD circuits. FD circuits are one of the most energy and area consuming components of digital circuits. Therefore, minimizing the power and chip area of the FD is essential in low-power and small-size long-life battery operated biomedical systems. However, FFs are considered

the basic building block of FD digital circuits in synchronous CMOS design. The appropriate FF architecture is then of fundamental importance in the design of FD circuits and, in particular, of both low-power and small chip area. There are numerous different types of FFs; an extensive discussion of the various possibilities is not attempted here. Typically, there are three basic types of edge-triggered FFs, S-R, J-K, and D-FF [135] [52].

Early clocked FFs are SR flip-flops and J-K flip-flops, and they were first developed in 1958[139]. Clocking makes the FF change its output signal depending upon the values of the input signals at the transition. Therefore, FFs can be designed to change their output, either on the rising edge of the clock, or on the falling edge. Clocked SR FFs that are triggered by the rising edge of the clock signals can be simply built from a pair of cross-coupled NOR gates. SR FFs are not desirable in ICs because they have an indeterminate state when both inputs are high ( $S=R=1$ ). They respond to the clock signal transition at the clock input only for certain combinations of  $S$  and  $R$  [135]. In a clocked J-K flip-flop, its inputs,  $J$  and  $K$ , control the state of the FF in the same ways as the  $S$  and  $R$  inputs do for the clocked SR FF, except that when both  $J$  and  $K$  inputs are high, the ( $J=K=1$ ) condition does not produce an indeterminate output. In this case, if both  $J$  and  $K$  are high, the FF will change states and toggle to its opposite state for the positive going transition of the clock. Hence, by setting  $J$  and  $K$  inputs of each FF to 1, and taking the output of one FF to the clock input of the next, so that it will change states, and toggle at each cycle of the clock input, the first FF toggles on each input clock pulse, producing a toggle in the second FF, so its output will be a square waveform at one half the frequency of the input clock. This configuration acts as a ripple counter; the clock pulse is applied only to the first FF, whose output  $Q$  triggers the clock of the second FF, which in turn triggers the third FF and so on through the chain producing a ripple effect in the timing signal as it passes through the chain. However, the time required from when the first J-K FF changes, to when the last J-K FF has settled, is quite large. This is due to the changes rippling through from FF to FF. So this configuration is a poor choice for a synchronous logic circuit and is not preferred in FD IC applications [135]. In addition, clocked SR and J-K FFs that require a large device count in each circuit, result in increased chip area and power consumption.

Since the importance of designing power-efficient high-performance synchronous systems has been recognized, several research studies have been conducted

to develop new architectures and design techniques to overcome the previous FFs design deficiency. Consequently a number of published works have proposed new architectures of FFs that improve functionality and speed [140-143] or improvements in other timing element characteristics such as immunity, noise and testability [144, 145]. Other works on reducing energy and design of low-power FFs were demonstrated and published in [145-151] while other research focusing on aspects related to FF comparisons adopted figures of merit and evaluated parameters [137, 152]. Other published works have compared the energy-performance scheme of various FF architectures [137, 144, 153-157].

Study to investigate the effects that arise in nm CMOS technologies on low-power and high performance FFs is continuing to identify the optimal or near-optimal choice in design trade-offs between the power, speed and chip area. One example, in [145] demonstrated, in their comparative analysis, utilizing the most common FFs topology using 0.25nm CMOS technology with scaled supply voltages ( $V_{DD}$  is scaled from 2.5V to 1V). These FF are as follows: 1) Conventional master-slave latch-pairs (MS) which involve the transmission-gate FF (TGFF) with input gate isolation which is derived from the PowerPC603 latch-pair and the pseudo-static  $C^2$ MOSFF; 2) Pulse-triggered latch, which is also a two-stage FF where the first stage is a pulse generator (PG), and the second stage is a latch; this type includes the semi-dynamic FF (SDFF), the hybrid latch-FF (HLFF) and a fully differential pulsed-latch which is the modified sense amplifier based FF (MSAFF); 3) FFs with internal clock gating; internal clock gating offers disabling of the internal clock when the input data are equal to the output data. This type includes the clock-on-demand FF (COD-FF) and a TGFF with internal clock gating (GTGFF). Their results show that the optimal FFs topology and size is dependent upon the particular operating conditions. The comparative analysis also shows that MS latch-pairs typically consume less energy than pulse triggered latches. The TGFF is the most energy efficient topology and the best overall choice for low power digital design among the FFs presented. The TGFF possesses relatively good energy-delay trade-off, large race margin, sufficient noise robustness, and the low energy required to drive data and clock inputs. The study shows that the TGFF maintains relatively large internal race immunity (by mean of a data race through both latches on the active clock edge that causes multiple transitions on the output), which makes it suitable for large-scale designs.



The comparisons in [137] were to identify an optimal design choice of clocked storage elements (CSE) in 130nm CMOS technology at supply voltage of 1.2V, such as the semi-dynamic flip-flop (SDFF), the implicitly pulsed flip-flop with push-pull latch (IPP), the single-ended skew-tolerant flip-flop (STFFSE), the transmission-gate pulsed latch (TGPL), and the transmission-gate master-slave latch (TGMS). Their analysis studied the energy-efficient characteristic over all storage element configurations and interface loads that allow them to define the natural target application for all CSEs. The effects of the transistor size, delay target, output load, and input load restriction to the CSE performance are also investigated quantitatively. From the system viewpoint, the simulation results that extract an accurate set of energy-efficient configurations for each CSE, demonstrated that the low-power CSEs, such as TGMS or IPP, have to be the optimal or near-optimal choice. Practically, their results show that master-slave latch flip-flops offer the most energy-efficient solution, due to their simpler structure and low internal switching activity.

However, earlier comparisons involve a limited number of the existing FF architectures and do not cover the entire range of applications and limitations that are observed in real designs. The researchers, in [158, 159] carried out their study, Part I and Part II respectively, which is a thorough comparison among 19 FFs topologies belonging to four different classes in a 65nm CMOS technology, which is the widest comparison presented in the literature. They are, as follows, together with the following respective classes: 1) Master-Slave (MS): a) Transmission-Gate FF (TGFF); b) Write-Port Master Slave FF (WPMS); c) Gated Master Slave FF (GMSL); d) Data-transition look ahead FF (DTLA). 2) Pulsed, both implicit (IP) and explicit (EP): e) Hybrid Latch-FF (HLFF); f) Semi-Dynamic FF (SDFF); g) UltraSPARC Semi-Dynamic FF (USDFF); h) Implicitly Push-Pull FF (IPPPF); i) Conditional Precharge FF (CPFF); j) Static Explicit Pulsed FF (SEPPF); k) Transmission-Gate Pulsed Latch (TGPL). 3) Differential: l) Modified Sense-Amplifier FF (MSAFF); m) Skew-Tolerant FF (STFF); n) Conditional Capture FF (CCFF); o) Variable Sampling Window FF (VSWFF). 4) Dual-edge-triggered (DET): p) Transmission-gate Latch-Mux (DET-TGLM); q) Symmetric Pulse Generator FF (DET-SPGFF); r) Static Pulsed Latch (DET-SPL) [18]; s) Conditional Discharge FF (DET-CDFF).

In part I of their study, they investigated the effects that arise in 65nm technologies and affect the energy-delay area trade-offs that are important in the



application, such as speed, low power, and low standby energy. An extensive analysis for 65nm CMOS FFs with a 1V supply voltage was adopted in Part II of their study. Their comparison includes the energy-efficient curve EEC extracts, selecting the most energy-efficient FFs normalized to the reference technology values, and the influence of layout parasitic (routing paths) in the transistor-level design phase; the impact of leakage was also considered in both standby and active mode. Wide loading and switching activity conditions were also investigated, and other properties (e.g., the clock load and the related dissipation of the clock distribution network) were analyzed in detail. Furthermore, the FFs input capacitance and the effect of local wire parasitic in the transistor-level design are considered as a further independent variable to be optimized. Their results demonstrated, in part I and part II of their study, that the best low-energy FFs are the Dual-Edge-Triggered Transmission-gate Latch-Mux (DET-TGLM) and the TGMS. Hence, MS FFs based on transmission gates (TGFF, DET-TGLM) are the best when energy is the main concern. On the other hand, DET-TGLM is significantly worse in term of leakage than TGMS and WPMS. The layout efficiency of the selected FFs has been also analysed. The results show that the MSAFF, HLFF and TGMSFF, have the smallest areas and exhibit a very efficient area-delay trade-off. Actually, the MSAFF requires a very low area due to its regularity, while the TGMSFF and HLFF which have the simplest architectures among the MS considered, and Pulsed FFs require a very small silicon area. Besides, analysis of the relationship between area and leakage for the various FFs, shows that area is mostly proportional to leakage regardless of the FF architectures and the transistor sizing. A smaller size of the layout is required when the leakage impact increases, and hence, a small transistor size. Since the circuits with the highest leakage are those with a high number of transistors and layout complexity. Therefore, it has been shown that leakage has a significant influence on the optimum transistor sizing, especially for MS FFs. Interestingly, TGFF and HLFF have the minimum leakage normalized to the reference technology in [160], because MS FFs have very simple architectures and typically small transistor sizes, while HLFF is the simplest among IP FFs and comprehensively utilizes stacking. In addition, the ranking of their analyzed MSFFs does not change for different switching activity and capacitor load ( $CL$ ) values. These results showed that the TGMSFF largely remains the most layout-efficient and energy-efficient, and hence, additional figures relative to this FF class are not required. Based on above design review, all the above TGMSFF

profiles are seeing an increase in the performance and reduction in silicon area, leakage and power consumption, which indicates that TGMSFF is offering similar and good performance in all the above nano-meter CMOS technology process comparison studies.

It can be concluded that, from all the above approaches, TGMS FFs are clearly the optimum choice and the most power-efficient FFs, among the most efficient and best-known ones, in the efficient energy region. They also have the best layout efficiency. Thus, D-FFs based on transmission gates are the best when power consumption and chip area are the main concern. The appropriate FF architecture is of fundamental importance in the design of FD circuits of this project. Considering that the suitability of FFs for a given application is challenging, and so is their selection, since it involves a large number of existing architectures, most the above approaches involved comparisons of a number of existing FF architectures based on energy-delay products and also power-delay products which were directed toward high frequency applications. This is a more performance oriented metric for circuits and design styles, considering whether the high speed is of a higher importance and main concern than power consumption. This will not be applied in this research project, as appropriate D-FF based TGMSFFs using 130-nm CMOS technology are the focus of this work and are optimized for low frequency performance, low power consumption and a small silicon area, the major concerns in this project. In practical designs and for dependable results, an appropriate sizing methodology will be applied since the target of this project is a portable device for biomedical applications.

However, a Transmission-Gate (TG) composed of N-MOS and P-MOS source and drain terminals connected in parallel with complementary signals controlling their gates voltages is preferred instead of a pass transistor to improve the noise performance of the D-FF circuit, at the cost of an extra clock signal, that is, the complement of clock [54, 135]. Although a simple, realized using only single NMOS or PMOS devices, as shown in the schematic diagram in Figure 2.16 (a) reduces the number of active devices, pass transistor is not often used except where the chip area is highly important. The greatest disadvantage of using NMOS pass transistor configuration is that it is not good at passing a logic “1”, but ends up with a  $V_{THN}$  drop below it (“1-  $V_{THN}$ ”). This is due to the voltage dropping by at least a  $V_{GS}$  of  $V_{THN}$  to keep NMOST on, which significantly increases power dissipation and becomes impractical, when used in low power supply

voltage circuits such as 3.3V or lower. But NMOS pass transistor is good at passing “0”, since it completely turns off and pulls to ground, while using PMOS pass transistor in gate design is complementary to the NMOS’s operation, and hence, is good at passing “1”, but not good at passing a “0”, since the PMOS device does not completely turn off, thus, the output is pulled down to a  $V_{THP}$ .

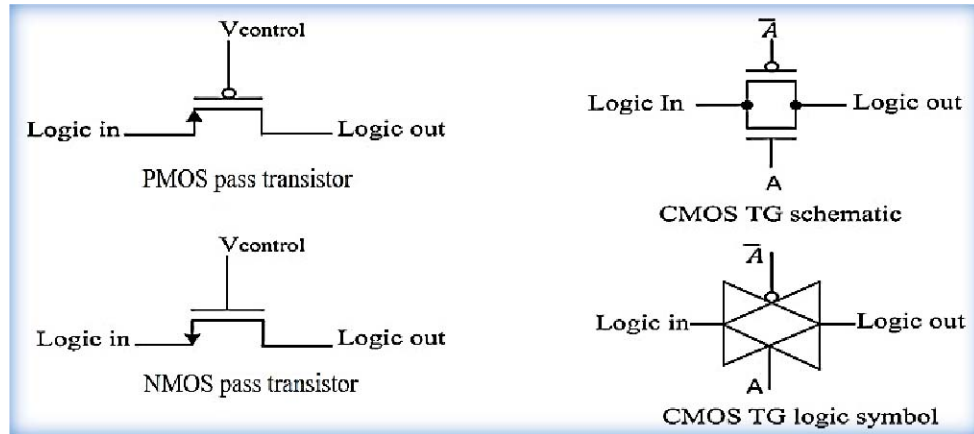


Figure 2.16. Schematic diagram of the logic gate (a) a simple PMOS and NMOS pass transistor and (b) a CMOS transmission gate and its logic symbol.

As shown in Figure 2.16 (b), using CMOS TG realized NMOS and PMOS transistors with complementary signals controlling their gates voltages ( $A$  and  $\bar{A}$ ), they can pass both logic levels well, and hence, this has advantages for its rail-to-rail output swing. A CMOS TG is a circuit that can be used in both analog and digital circuit design. Typically, it is used as a stand-alone building block for logic circuitry, such as D-Flip-Flop and multiplexer/demultiplexer (MUX/DEMUX). They can carefully block or transmit data without needing a completed hardware-controlled system, with a negligible degradation in the characteristics quality of the data. It operates like a voltage controlled switch to pass logic levels between nodes of a circuit. However, the symmetrical behaviour of the whole TGMS block can be achieved by proper sizing, while low threshold voltage, with quantified MOSFETs sizing, reduces power and chip area consumption. This depends on the application’s requirements; sizing TGMS for high frequency design however, is different from low frequency design.

### 2.8.3 Sources of Power Dissipation In A Digital Model

The main sources of power dissipation in a digital CMOS circuit can be summarized and given as in [3, 52, 161] by,

$$P_{Total} = P_{dynamic} + P_{short-circuit} + P_{static} + P_{leakage} \quad (2.8)$$

The first term is the dynamic power dissipation that is caused by charging capacitances in the circuit. Consider the inverter in Figure 2.17 that has input pulse with a period  $T$  and frequency,  $f_{clk}$  with load capacitance of  $C_L$ .

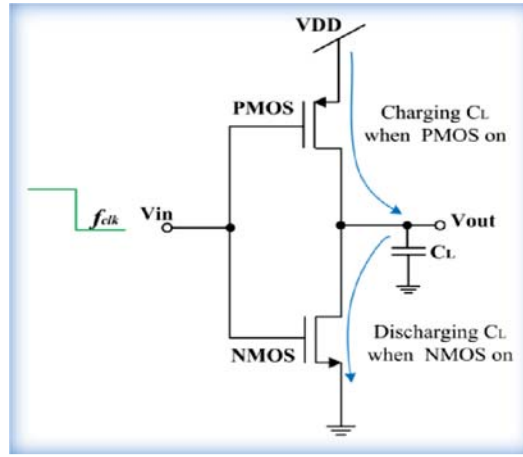


Figure 2.17. Schematic diagram of dynamic switching power dissipation in CMOS inverter.

When the inverter changes states, it will supply a charge to  $C_L$  or sink the charge stored on  $C_L$  to ground. When the output switches from a “0” to a “1”, the PMOS device is on, the load capacitance  $C_L$  is charging from 0V to  $V_{DD}$ , through the PMOS transistor. A certain amount of energy is drawn from the power supply. By charge conservation, the charge ( $Q_{C_L}$ ) stored on the capacitor is the charge flowing from the supply. The average amount of current,  $I_{average}$ , that the inverters draw from  $V_{DD}$ , can be then given as in [54] by,

$$I_{average} = \frac{Q_{C_L}}{T} = \frac{V_{DD} \cdot C_L}{T} \quad (2.9)$$

Knowing a gate switching frequency,  $f_{clk}$ , the average dynamic power dissipated by the inverter can be given by,

$$p_{average} = V_{DD}I_{average} = \frac{C_L V_{DD}^2}{T} = C_L V_{DD}^2 f_{clk} \quad (2.10)$$

When the output switches from a “1” to a “0”, the load capacitance  $C_L$  is discharged and the stored energy is dissipated through the NMOS transistor. Therefore, energy of  $C_L V_{DD}^2$  is consumed from the supply voltage on a “0” to a “1”, output transition, and only stored capacitive energy is dissipated in a “1” to a “0”. Thus only the “0” to a “1” transition consumes energy from the supply. Equation (2.10) shows that the dynamic power consumption is proportional to the clock frequency, therefore, with a high clock frequency, large power is proportionally consumed. Also, the dynamic power consumed is very sensitive to the supply voltage, hence, decrease in the supply voltage can considerable, decreasing the power consumption. Using a CMOS gate that is continuously switching at maximum speed, such as in a CMOS TG transmission gate, consumes an amount of power equivalent to that in a single NMOS gate that is continuously switching at the same maximum speed. This would be the specified superiority of CMOS logic with respect to power consumption [135].

The second term occurs during the transition on the input signal, when both the NMOS and PMOS transistors are simultaneously active or on, conducting current, so that there is short circuit current ( $I_{sc}$ ) from the supply  $V_{DD}$  to ground. It is possible that the DC path between the supply  $V_{DD}$  and ground exists briefly while the output is changing. This short circuit current normally takes place for very small intervals. The short circuit power dissipated by the inverter can be given by,

$$P_{short-circuit} = I_{sc} V_{DD} \quad (2.11)$$

Practically, this power due to the direct-path current is considerable only in large inverters, such as in buffers. Usually, this power consumption, due to the charging and discharging parasitic capacitances, is not taken into account. However, using low supply voltage can lower considerably the short circuit power dissipated. Also this

power represents less than 20% of the dynamic switching power consumption if the NMOS and PMOS transistors are sized carefully [162].

The two sources of power dissipation in digital CMOS circuits discussed above are due to transitions at gate terminals and referred to as dynamic power dissipation, while the other types of power dissipation are due to the current that flows when the gate terminals are not in switching activity mode, and are then usually referred to as static power dissipation. This third term is the static power consumption that is caused by current in devices when the circuit is static and not switching (the output is in the low or high state). It is equal to the product of the supply voltage  $V_{DD}$  and current  $I_{DD}$  drawn from the supply by it, so,

$$P_{static} = V_{DD}I_{DD} \quad (2.12)$$

Equation (2.12) shows that the static power consumption is also proportional to the supply voltage. Ideally, CMOS logic in steady state is considered to have zero static power dissipation [52]. This is one of the most attractive features of CMOS technology. However, as the CMOS technology scales down to achieve higher density, a leakage current  $I_{leakage}$  that arises from substrate injection, gate leakage and sub-threshold effects that is the main source of power dissipation in deep sub-micron CMOS technology circuits. This power dissipation is equal to the product of the supply voltage and the leakage current which can be simply given by,

$$P_{leakage} = V_{DD}I_{leakage} \quad (2.13)$$

$I_{leakage}$  is mainly determined by the CMOS fabrication process technology characterization [161]. In general, leakage current can be controlled by an appropriate topology, reducing total transistor width, lowering supply voltage and removing power (sleep transistor) [3]. However, the  $P_{leakage}$  dissipation has importance only in deep sub-micron technology, otherwise the magnitude of leakage current is usually neglected.

Indeed, the above analysis of power dissipation, specifies that by reducing  $f_{clk}$ , the dynamic power can certainly be reduced. The importance of using lower  $V_{DD}$  is obvious in equation (2.10), in which the dynamic power is reduced in proportion to the

square of any reduction in  $VDD$ . The importance of reduction of loading capacitance is also obvious in equation (2.10); the lower the load capacitance, the smaller the dynamic power. It also uses lower  $VDD$ ; a good supplement to short-circuit power and static power dissipation. However, power consumption as well as the silicon area of the FFs depends on appropriate FFs architectures and the  $W/L$  ratios of the MOSFET transistors.

The low power consumption in digital systems design comprises optimization at different design levels. This optimization includes the technology, the logic style, and the circuit architecture, that are used to implement digital circuits [3]. Optimization in technology level is related to materials used in the fabrication process technology [163], its dimension and concentration, like oxide thickness and substrate profile, and device structure [164]. The design level involves optimization in physical design, placement, routing and sizing strategy, while logic design optimization techniques include logic minimization [165]. The architectural level usually is the design solution for reducing supply voltage; it can achieve high performance utilizing parallel or pipelined structures [166].

## 2.9 Active Electrode

The next part of the system is the electrode. This electrode is required for the communication network between the electro-medicine device and the body, by using the conductivity of the body. Typically, these electrodes, the common transducers, are simple surface electrodes and use a passive metallic disc with wire connected to the bio-signal amplifier. The transducers may be made of stainless steel, gold or Ag/AgCl; the latter is the most used for DC derivations with low frequency signals [167]. In fact, conventional passive electrodes have a significant effect on the purity of the signal transmission. This is because the electrode wire is the main source of noise, including power line interference and the movement of the wire. Another drawback of using a passive electrode is that short circuits may happen between adjacent electrodes [168] increasing the noise generated at the metal-skin interface, which degrades the source signal quality. Passive electrodes also require unusually extensive skin preparation to improve the skin contact and connectivity, which is not practical for daily use [169].

A good quality signal can be transmitted by using an active electrode utilized buffer amplifier, as close to the transducers as possible, for shielding, and it eases mains



interference [167, 168, 170]. The active electrode has system connectors to supply the electronic components with power. Figure 2.18 shows different types of electrodes. In the 1960's and 1970's, the concept of active electrode was developed for the first time in [171, 172] respectively.

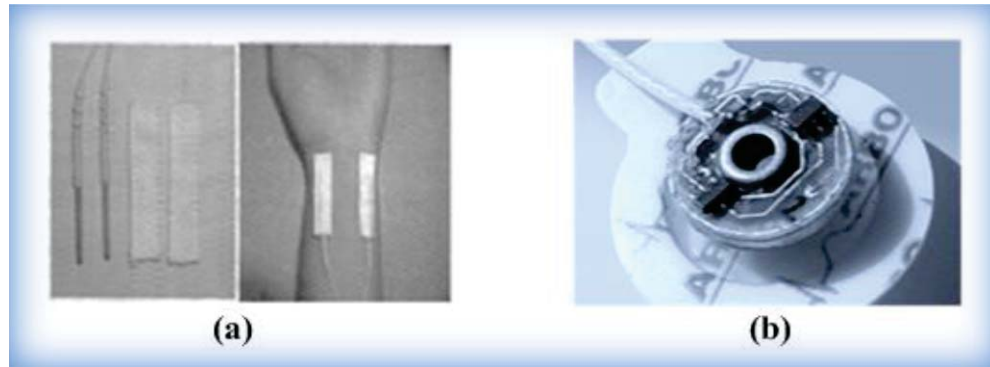


Figure 2.18: Types of electrodes: (a) passive electrodes, and (b), active electrode using commercial Op-Amps with Ag/AgCl transducer for biomedical applications [173].

In the 1960's such an electrode had not been used, due to the large size of the IC transistor which could not be mounted on the electrode, and also due to their high cost [168]. An early active electrode was demonstrated in 1971 when [175, 176] developed an active electrode for electrocardiogram (ECG) recording, realized from buffer amplifiers, constructed of discrete components within a metal case, connected to ground to provide shielding of the circuitry. Multielectrode probes that consisted of gold electrodes incorporated onto a silicon chip for the membrane potential recording were developed in [177-179]. In 2004 [180] employed the active electrode in a medical acupuncture system to study the skin response to laser stimulation effect. Presently, several types of active electrode circuit have been developed for bio-signal sensing, measurement and stimulation. Examples are electro-oculography (EOG), electroencephalography (EEG), electro-cardiogram (ECG) [167, 181, 182] electrical impedance tomography (EIT), for monitoring patient heart activities and respiration system [169, 183] and for bio-impedance measurement [184]. The main feature realized in active electrodes is signal buffering. By utilizing a buffer amplifier circuit, one can develop active electrodes for bioelectrical stimulation. A simple buffer can be employed



by utilizing an Op-Amp in a voltage follower configuration. A variety of active electrodes has been reported in the literature, usually, using commercial Op-Amps, for example, NJMO62M Op-Amp [168], LMC7111 Op-Amp [181], TLC272 Op-Amps [182] and LMP7701 Op-Amp [185]. Some authors [186] employed buffer circuits with class-AB output stage in a neuronal stimulation and recording application. The buffer circuit was fabricated using  $0.6\mu\text{m}$  CMOS technology which can generate output current of about 10mA, using 5V supply voltage with power consumption of  $150\mu\text{W}$  when no input signal is applied. Some other authors [187] developed a compact ( $= 0.02\text{mm}^2$ ) buffer for both voltage and current mode electro-bio-stimulation. This is a high-current class-AB voltage follower, with the OTA component based on a local common mode feedback (LCMFB) amplifier. It was fabricated with a  $0.6\mu\text{m}$  CMOS process using 5V supply voltage and power consumption of  $245\mu\text{W}$  for the voltage mode, while in current mode the circuit provided output current of  $300\mu\text{A}$  or  $30\mu\text{A}$  with input resistance of  $10\text{k}\Omega$  or  $100\text{k}\Omega$  respectively. The design in [174] used two-stage OTAs employing PMOS input stages with large gate areas, to improve noise performance, and configured a unity-gain-buffer for simultaneous acquisition of EEG and EIT signals. It was fabricated using AMS  $0.35\mu\text{m}$  technology, and power consumption in the readout mode was about 1mW. In [188, 189] a super buffer realizing a class-AB amplifier with large transistor count (22 and 20 respectively) was designed to provide large output current. It is implemented using 45nm CMOS technology with +3V supply voltage. The work reported in [190] used two-stage OTAs (transistor count 19) to design a wideband current driver circuit for cancer tissue impedance analysis. It was fabricated using a  $0.35\mu\text{m}$  CMOS technology with  $\pm 2.5\text{V}$  supply voltage.

The aim of the above approaches was to design compact high performance circuit for the signal buffering task at low power drain, and to transmit a superior quality signal by shielding mains interference. In addition to the buffering task, a simple buffer architecture with the desired attributes that has a small transistor count while achieving large driving capability at low power consumption is attractive for a biomedical device. The proposed active electrode is based on the [186] architecture that utilized a class-AB amplifier to deliver a large output current of 10mA, which is too high for the applications of this research project. In addition, the circuit is based on  $0.6\mu\text{m}$  CMOS technology using high supply voltage of 5V. Therefore, the buffer circuit of this work is developed using new 130-nm CMOS technology with low supply voltage of only 1.2V

and occupies a small number of MOSFETs. Since the output current of the typical OTA circuit is limited by the bias current, using a large bias current increases the power requirement. Thus, a trade-off between power consumption and slew rate exists [66]. To overcome this deficiency, an adaptive basic current scheme realizes three MOSFETs employed to release boosting of the bias current, by providing a scaled copy of the input stage differential current back to the bias current, instead of using a class-AB amplifier with four MOSFETs. Therefore, the buffer circuit can achieve an appropriate driving capacity with low power consumption, which is compatible with the requirements of the biomedical applications of this work.

## **2.10 Conclusion**

The overview of the system model, theory, design and approaches including basic concept for a WFG circuit are presented above. Relaxation oscillators architecture that are characterized as a simple circuitry configuration with less sensitivity, will be implemented based on hysteretic input output relationship as in hysteresis Schmitt Trigger to generate a periodical repetitive output signal. The principles of operation of a typical WFG generator circuit, utilizing a combination of hysteresis Schmitt Trigger based positive feedback, and a relaxation timing network circuit, based on RC and an integrator building block, was introduced for comparison. Different CM circuit configurations, which realize distinct characteristics as building blocks in WFG designs, were presented. This included a comprehensive review of a recent low power CMOS WFGs design approach based on hysteresis Schmitt Trigger, termed “current mode OTA” which has shown massive potential for low power circuit design. Design of a WFG based on CMOS OTAs is therefore considered as a simple circuit, with a power efficient and small chip area solution for the miniaturized, low-cost, longer battery life biomedical device for this research project. The importance of the relaxation timing network, including passive RC and active integrator gm-C approaches, was also discussed. The active integrator gm-C approach could be an attractive, electronically tuneable, low frequency and small chip area solution. Since the overall performance of WFG circuits can be determined by the transconductance characteristics, an appropriate design can be then achieved by determining its controllable variable parameters and

analysing the important trade-offs between these variables for high gain, low frequency design and to reduce power consumption and optimize the silicon area.

In addition, a comparative study of a number of different FF architectures was reviewed, to classify those that are the best power and area efficient designs to re-design and use for a FD designed circuit. This digital circuit is a part of a hybrid tuning system composed of analog and digital models that is compatible with the applications requirements of this research project. Among a large number of FFs that have been discussed above, the most common and simplest FF architectures used for a FD circuit, is the master-slave D-FF based TGMS. It utilizes the most distinctive MOSFETs characteristics in simple logic-controlled switches to design a complete and optimum digital model that functions properly for low frequencies, in a low power and small silicon area frequency division system for this work. The ability to design high density digital circuits with high functionality, design trade-offs between size, power, and chip area, will be considered. Finally, the CMOS technology can be used, as it is small in size so that it can be integrated to develop an active electrode utilized buffer amplifier to overcome the deficiencies of using passive electrodes, and a good quality signal can be transmitted by reducing the sensitivity to cable and environmental interference.

130nm CMOS technology, with various low-voltage techniques, and state-of-the-art simplified design, can be applied to meet the design requirements of a novel biomedical device of this research project.

# **Chapter 3**

## **Design Criteria, Implementation and Fabrication of Waveform Generator Circuit for Extra Low-Frequency CMOS Micro-Power Applications**

### **3.1 Introduction**

To achieve the required specifications, creative circuit design is necessary. Creative design also demands the necessary skills to identify and master the exact trade-offs between the different limitations. The low power characteristics of circuit design are important for the topical problem of power dissipation. Therefore, it requires knowledge and understanding of devices, circuits, technologies and systems. The low power design [3] imposes the five considerations that determine the power consumption of the systems. These involve: 1) the task that it performs; 2) the technology that it is implemented in; 3) the topology or architecture used to satisfy the task need; 4) the bandwidth of the task; and, 5) the output precision of the task. By increasing the task, bandwidth, and output precision of a system, the complexity and the power consumption of the devices implementing that system increases. Achieving high performance and low-power analog circuits, using today's nm-CMOS technologies, requires state-of-the-art architecture, for an appropriate low supply voltage circuit design. This involves a good choice of topology, such as using cascades of multiple-stage topology, with adequate DC gain per stage to increase the open-circuit voltage gain and the output swing requirement, without consuming extra overdrive. Hence, the design of precision power efficient circuits with low supply voltage for low frequency and miniature WFGs constitutes an important aspect of analog CMOS design. As previously mentioned in section (2.6), analog WFG implementation CM techniques utilizing an OTA has attracted consideration for analog circuit design, due to its high performance and flexibility. However, the WFG designs in published literature, usually, using commercial OTAs, or were built using complex circuitry with extra active and passive elements and high supply voltage, which is not desirable in low power applications. The need for a minimal circuit solution for WFG, in terms of the number of active and passive components, is indeed a matter for implementation of IC. This

would obtain accurate frequency response characteristics that can be achieved by reducing the effects of PVT variations of using complex circuitry, with extra active and passive elements. It would also consume less power and less silicon area. These aspects are desirable for modern IC implementation design.

However, the low frequency WFG, based on relaxation oscillators utilizing a RC relaxation network with a wide tuning range and low-power consumption, is the most challenging circuit design. An optimum low frequency WFG circuit, designed with good performance, is not an easy design, for it demands that the best trade-off among many different variables which all interact, is identified. In this chapter, the design of a new hysteresis Schmitt trigger with its applications for a novel CMOS ultra-low-power and ELF WFG, along with a novel RC relaxation timing network circuit, is presented. The outline of this chapter is as follows: first of all, trade-off of low power CMOS WFG design analysis will be discussed in section (3.2). The design criteria of novel CMOS ELF WFG will be presented in section (3.3). The circuit design and topology will be presented in section (3.4). The ELF WFG circuit operation will be discussed and described in detail in section (3.5). Simulation and performance analyses are presented in (3.6). Section (3.7) provides layout design and fabrication details for the most important active and passive elements of the circuits. Experimental results are presented in section 3.8 and chapter 3 concludes in section 3.9.

## **3.2 Trade-off of Low Power CMOS WFG Design Analysis**

The previous chapter has introduced power efficient WFG approaches; now a basic and simple analysis of the low power operational transconductance amplifier OTA design will be thoroughly explored in depth. Furthermore, the brief discussion of overall principles and parameter controlled design for high gain, low frequency, and low voltage trans-conductance design, is presented. The trans-conductance characteristics are very important in the WFG circuit because they determine the overall performance of the circuits, such as gain, frequency response, linearity, and power consumption. When designing a trans-conductance amplifier, the trade-off concerns that arise are many; for an appropriate design, the basic theoretical analysis of the trans-conductance is necessary in order to determine its controllable variable parameters, which are the key factors for low power, low frequency and small chip area WFG circuit design.

An ideal trans-conductance amplifier is a voltage-controlled current source which has an infinite input and output impedance [130]. The simplest single-common source (CS) MOSFET transistor operating in the saturation (sat) region shown in Figure 3.1 is considered as a trans-conductance amplifier, generating an output current in response to an input voltage. As the drain source voltage ( $V_{DS}$ ) exceeds  $(V_{GS} - V_{THN}) = V_{DS,sat}$  the drain current ( $I_D$ ) becomes a constant current source, following the square-law relationship.

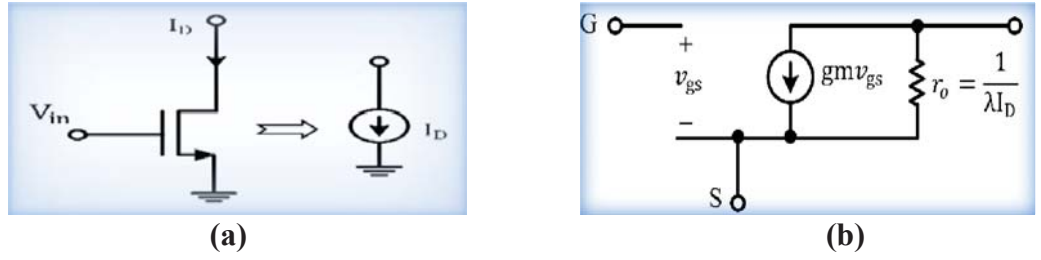


Figure 3.1 Trans-conductance amplifier (a) a single common source MOSFET transistor operating in the saturation region as a current source, (b) the small-signal model.

So,

$$I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{THN})^2 \quad (3.1)$$

Where,  $\mu_n$  is the mobility of electrons of NMOS,  $C_{ox}$  is the gate oxide capacitance per unit area ( $C_{ox} = \epsilon_{ox}/t_{ox}$ ), the dielectric constant of the gate oxide divided by the gate oxide thickness),  $W$  and  $L$  are the width and the length of the MOSFET,  $V_{GS}$  is the gate-source voltage, and  $V_{THN}$  is the threshold voltage. CS MOSFET in the saturation region Figure 3.1 (b), operates as a voltage-dependent current source, behaving as current source in parallel with its output resistor,  $r_o$ , so,

$$r_o = \frac{1}{\lambda I_D} \propto \left( \frac{L^2}{V_{DS,sat}^2} \right) \quad (3.2)$$

Where,  $\lambda \propto (1/L)$  is the channel-length modulation parameter. The output resistance is then dependent on the channel length as well as on  $V_{DS,sat}$ . Output resistance is an important parameter in the circuit design. High  $r_o$  may cause the open-circuit voltage

gain,  $A_v = gm r_0$ , to increase and the intrinsic speed of the MOSFETs to decrease as will be explained next; this can then be suitable for use in low frequency applications design. However, cascode devices can be used to increase the output impedance of the trans-conductance amplifier, but at the cost of output swing. A long-length device is preferred for large output resistance and for low power consumption. Another important characteristic of the MOSFET trans-conductance amplifier devices that must be taken into account, is the trans-conductance,  $gm$ , which relates the change in drain current to a change in gate-source voltage, which can be given by,

$$gm = \frac{\partial I_D}{\partial V_{GS}} = \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{THN}) = \sqrt{\mu_n C_{ox} \frac{W}{L} 2I_D} \quad (3.3)$$

In analog design,  $gm$  has a significant effect on the circuit operation, including the intrinsic speed of the MOSFETs, and hence, the frequency response of the circuit. It can also affect the open-circuit voltage gain,  $A_v$ , of a CS NMOS device, since the voltage gain for a CS NMOS device operating in strong inversion is the product of the trans-conductance ( $gm$ ) and the output resistor  $r_0$  which can be given by the two following equations,

$$\begin{aligned} A_v = gm r_0 &= \frac{\sqrt{\mu_n C_{ox} \frac{W}{L} I_D}}{\lambda I_D} = \frac{\sqrt{\mu_n C_{ox} \frac{W}{L}}}{\sqrt{I_D}} \cdot L \propto \frac{\sqrt{L}}{\sqrt{I_D}} \\ &= \frac{\mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{THN})}{\lambda \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{THN})^2} = \frac{2}{\lambda (V_{GS} - V_{THN})} \propto \frac{L}{(V_{GS} - V_{THN})} \end{aligned} \quad (3.4)$$

The  $A_v$  gain is not only dependent on a CMOS technological parameter; the width, length,  $V_{GS} - V_{THN}$  and biasing current of the MOSFET device for the designed circuit can be chosen by the designer. As per (3.4), it is obvious that for high gain,  $L$  must be chosen as large as possible, and  $V_{GS} - V_{THN}$  as small as possible, and hence, the DC drain biasing current is also reduced. However, by making the value of  $V_{GS} - V_{THN}$  too small, less than the typical CMOS technological value, the MOSFET is then entering a weak inversion, resulting in a small absolute value of the current, accordingly, small  $gm$  and, hence, small gain, which can produce a large noise and smaller signal-to-noise ratios (SNR). This result shows that the largest possible voltage gain with less power



consumption can be achieved by choosing long channel length  $L$ , or/and small  $V_{GS} - V_{THN}$ . This may assist the decrease in the MOSFETs intrinsic speed, which can then be suitable for use in low frequency biomedical applications design, since the intrinsic speed, ( $f_{int}$ ), increases as the CMOS technology scales down [58] so,

$$f_{int} \approx \frac{g_m}{2\pi C_{gs}} = \frac{3 \mu_n C_{ox} (V_{GS} - V_{THN})}{4\pi C_{ox} L^2} = \frac{3\mu_n}{4\pi} \cdot \frac{(V_{GS} - V_{THN})}{L^2} \quad (3.5)$$

Where,  $g_m = (\mu_n C_{ox} W/L)(V_{GS} - V_{TH})$ , and  $C_{gs} \left( = \frac{2}{3} WLC_{ox} \right)$ . For short-channel MOSFET,  $f_{int}$  is not dependent on the mobility,  $\mu_n$ , since the latter starts to decrease because of velocity saturation with decreasing length, due to an increasing electrical field between the drain and the channel. Thus the term  $\mu_n/L$  will be considered as a constant value, and hence  $f_{int}$  in short-channel MOSFET devices can be given by,

$$f_{int} = \frac{g_m}{2\pi C_{gs}} \propto \frac{(V_{GS} - V_{THN})}{L} \quad (3.6)$$

The intrinsic frequency  $f_{int}$  is directly proportional to  $(V_{GS} - V_{THN})$ , and inversely proportional to  $L$ , opposite to the open-loop voltage gain in equation (3.4), which has an inverse relationship. Equation (3.6) shows that a low speed MOSFET can be designed using small  $(V_{GS} - V_{THN})$  and hence, a small DC drain biasing current. For a given bias current, the minimum allowable  $V_{GS} - V_{THN}$  for operation in saturation can be reduced only by increasing the width and hence, the capacitance of the MOSFET device.

Interestingly, based on above analysis, sufficient gain with the desired low speed, can be achieved by using a long channel length,  $L$ , resulting in larger output resistance and hence, large gain. The  $C_{gs} = (2/3)WLC_{ox}$  of the MOSFET devices has also increased considerably, enhancing the reduction of its intrinsic frequency. While using a small  $(V_{GS} - V_{THN})$ , and hence, a small DC drain biasing current, this also enhances the low frequency gain, reducing the intrinsic frequencies of the MOSFET devices, and significantly reduces power consumption.

However, operational trans-conductance amplifier, (OTA) is also a form of trans-conductance topology, and is considered as a voltage-driven current source. A wide variety of OTA structures have been presented in the literature. Most of them use high supply voltage and were used for high speed signal generation circuits. Due to the



low supply voltage of the nm COMS technologies adopted in this research project with the low speed signal WFG circuits, the number of practicable OTAs become limited. CMOS differential pairs in conjunction with a current mirror configuration is a form of trans-conductance topology that will be developed in the proposed WFG circuits of this project. It can be designed to have a high-output impedance, which enhances the overall gain of the circuit. And it also has a high-output impedance, usually with a low-frequency pole associated, which can limit the speed of the OTA circuit.

This configuration shown in Figure 3.2, consists of an identical NMOS differential input pair M1-M2 with an identical PMOS current mirror load, M3-M4 that converts a differential input to a single ended output. The advantage of such a configuration is the flexible circuit and can be designed for the low frequency signal with small chip area and low power biomedical WFG circuit of this project.

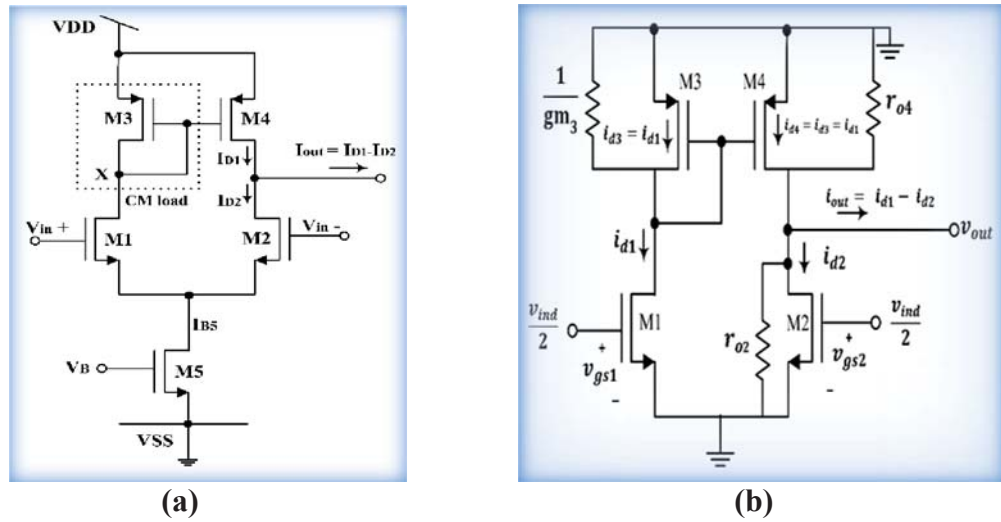


Figure 3.2. CMOS Operational trans-conductance amplifier, (a) schematic diagram (b) the small signal model of the differential amplifier with a current mirror load.

By considering the simplified small-signal model shown in Figure 3.2 (b), the low frequency gain of the OTA can be found by replacing the diode-connection M3, with  $(1/gm_3)$  resistor, the resistance looking into the drain of M4 with  $(r_{o4})$ , and the resistance looking into the drain of M2 with  $(r_{o2})$ . The drain current  $i_{d1} = i_{d3}$  is mirrored to the output via M4, and hence,  $i_{d4} = i_{d1}$ . Knowing that  $i_{d1} = -i_{d2}$ ,  $i_{d1} =$

$gm_1 v_{gs1}$ ,  $i_{d2} = gm_2 v_{gs2}$ , and  $v_{ind} = v_{gs1} + v_{gs2}$ , since  $v_{gs1} = v_{gs2}$ , the output current ( $i_{out}$ ), the output voltage ( $v_{out}$ ) and the voltage gain ( $A_v$ ) can be given respectively by,

$$i_{out} = i_{d1} - i_{d2} = \frac{gm_1 v_{ind}}{2} - \left(-\frac{gm_2 v_{ind}}{2}\right) = gm v_{ind} \quad (3.7)$$

$$v_{out} = (i_{d1} - i_{d2}) \cdot (r_{o2} // r_{o4}) = gm_{1,2} v_{ind} \cdot (r_{o2} // r_{o4}) \quad (3.8)$$

$$A_v = \frac{v_{out}}{v_{ind}} = gm_{1,2} \cdot (r_{o2} // r_{o4}) \quad (3.9)$$

Now examining equation (3.9) carefully, by substituting the expressions for  $r_o$  and  $gm$ , equation (3.2) and (3.3) respectively, and  $\lambda \propto (1/L)$ , then the proportion can be determined between  $(W/L)_{1,2}$ , the drain current and the small signal voltage gain  $A_v$  which can then be given by,

$$A_v = \sqrt{2 \mu_n C_{ox} \frac{W_{1,2}}{L_{1,2}} I_{D1,2}} \cdot \frac{1}{2\lambda I_{D1,2}} = K \cdot \sqrt{\frac{W_{1,2}}{L_{1,2} I_{D1,2}}} \cdot \frac{1}{\lambda}$$

$$A_v \propto \sqrt{W_{1,2}} \sqrt{\frac{L_{1,2}}{I_{D1,2}}} \quad (3.10)$$

The effects of the controllable variable ( $W_{1,2}$ ,  $L_{1,2}$  and  $I_{D1,2}$ ) on the small signal voltage gain,  $A_v$ , of the OTA circuit can be chosen by the designer. Equation (3.10), shows that the gain increases as the  $W_{1,2}$  or  $L_{1,2}$  increases and as the DC drain biasing current is reducing. Since in sub-micro CMOS devices that have short-channel length, the open-circuit voltage gain is considerably lower than the open circuit gains in long-channel devices [58], long-channel length can be used for large open-circuit voltage gain. Using long-channel length can also reduce the intrinsic frequencies of the MOSFET devices (3.6), and significantly reduces power consumption. However, to increase the output impedance, cascode devices can also be used, or a gain-boosting technique, that employs an amplifier to drive the gate of the differential input, but at the cost of output swing and consuming extra headroom voltage, resulting in large supply voltages [58]. An alternative option, cascades of multiple-stage topology, will be used

in this research project, to increase the gain and the output swing requirement without consuming extra overdrive, since the overall gain of the multiple-stage operational amplifier is equal to the product of all the stages. From the above analysis, utilizing a differential input pair, with current mirror load configuration, can save almost half of the die area and power dissipation.

In conclusion, a current mode based OTA circuit can be designed to achieve the largest possible voltage gain, with low speed and lower power consumption. However, what is most interesting in this type of circuit, is that  $g_m$  in CMOS OTA can be controlled by the biasing current, and hence, can achieve a tuneable range of frequencies of the circuit, by varying bias current. This simple result is considered greatly important in the design of a low power device, using submicron CMOS for high gain and for a tuneable low frequency WFG circuit, for this research project.

### **3.3 Design Criteria of ELF CMOS WFG Circuit**

The most remarkable contribution of this proposed ELF WFG circuit topology is that a novel current controllable ELF WFG, utilizing CM OTAs, is presented. Its operation mode can be characterized using a high-level model, comprising a hysteretic Schmitt trigger, based on positive feedback and time dependent elements, in a negative feed-back loop, formed by an RC circuit which determines the frequency of oscillation. The circuit oscillates with no input and generates a periodical signal (square waveform and exponential waveform) with sub-low frequency, and maintains infinity output. It is well defined in an integrated circuit, controllable, stable, and obtainable at low cost with small chip area, which could be used for signal shaping that will suit the required application. The ELF WFG has been designed and fabricated using devices available in 130-nm IBM CMOS technology with a  $\pm 1.2V$  voltage supply. Using the same topology, two sets of device dimensions and circuit components are designed and fabricated for comparison of relative performance, silicon area and power dissipation. Primarily of interest is the accuracy, small size, and low power consumption. It is also less sensitive to process variation and environment. Using 130-nm CMOS technology with the potential advantages of CM based OTA design allows for circuit simplification which meets the demand for low power biomedical applications in a battery operated system, with superior performance. However, to realize minimum active building block circuit

solutions, it is more important to focus on minimum dimensions and low account transistor circuit solutions for on chip integration, which would require a small chip area and consume less power. The novel contribution of the ELF WFG design in this chapter is to:

1. Scale down the device feature size of the circuit by using an appropriate 130-nm CMOS technology, with appropriate increase in the performance of the device.
2. Decrease the number of active devices to reduce the supply voltage and chip area. The Schmitt Trigger is further compacted using six MOSFET transistors including the output stage that provides maximum swing output voltage.
3. Reduce the passive element, to eliminate temperature sensitivity issues and to reduce the chip area.
4. Use cascaded gain topology with adequate DC gain per stage to reduce supply voltage. Multiple-stage topology can be used to increase the gain and the output swing requirement without consuming extra overdrive, since the overall gain of the multiple-stage operational amplifier is equal to the product of all the stages.
5. Employ the novel concept of a combination of the different types available of on-chip p+ polysilicon resistors in the 130-nm IBM CMOS process, such as the OPRRP resistor (with sheet resistance of  $1700\Omega/\square$ ), OPRPP resistor (with sheet resistance of  $228\Omega/\square$ ) which is used to fully implement the large integrated resistors (as hetero-resistors).
6. Use a simple current mirror configuration for the two approaches to provide multiple bias current, so as to reduce power consumption. This is based on copying currents to one or several current sources from one stable reference current. It is less sensitive to circuit parameters and manufacturing variations as well as producing no noise in the circuit, because it uses one passive resistor and a few single NMOS devices. A current mirror configuration that provides accurate current copying is controlled by the device ratios ( $W/L$ ) only and is independent of process and temperature. It requires minimum headroom and consumes low power, which is mostly preferred in low power biomedical devices. The power efficient CMOS cascode current mirror to supply independent biasing for low voltage applications, already designed and published in [191] is a type of copying current design that provides multiple current sources, and may suit other important low power biomedical applications.

### 3.4 Circuit Design and Topology of The ELF WFG

The circuit comprises a hysteresis Schmitt Trigger based on positive feedback and a relaxation timing network in a negative feed-back loop, formed by an RC circuit. The schematic diagram of the proposed CMOS ELF WFG based on RC relaxation timing network topology, is shown in Figure 3.3. The circuit utilizes a single, three stage, cascaded OTA along with two resistors and one capacitor.

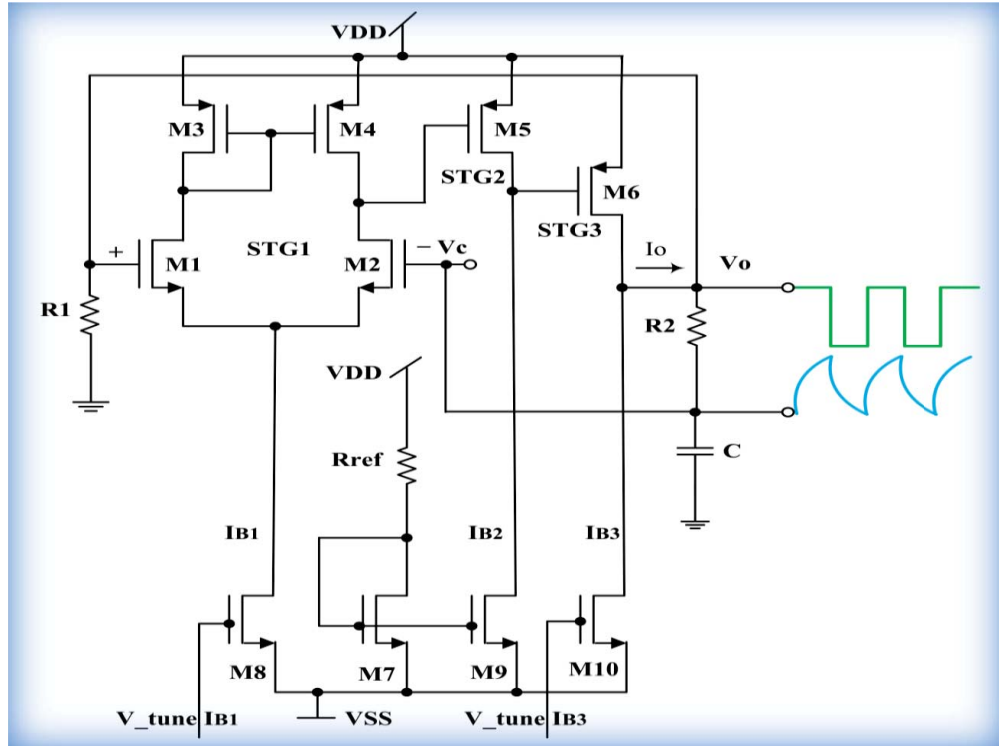


Figure 3.3. Proposed, ELF WFG. Based on the periodical charging and discharging operation of the capacitor  $C$ , ELF WFG circuit, provides a periodical square waveform output signal at  $V_o$  and an exponential waveform at  $V_c$  with no input.

It is thus more compact than the designs proposed in [117], as well as other standard designs [80], due to the use of simple gain stages and a minimum number of passive components. The first stage (STG1) employs an NMOS differential input pair along with a PMOS active current mirror load. It is followed by two simple PMOS common source (inverter amplifier) gain stages (STG2) and (STG3), respectively.

STG3, STG2, STG1 and  $R1$  are connected in a positive feedback loop from the output to the non-inverting terminal, to form a simple hysteretic Schmitt Trigger. The three stage amplifier provides large loop-gain around the positive feed-back path for the tripping action of the hysteretic Schmitt Trigger. The circuit also employs an RC relaxation timing network in a negative feed-back loop, from the output to the inverting terminal of the differential input, which determines the tripping period and hence the frequency of the ELF WFG at the output. It is the combination of this positive feed-back gain loop and the negative feed-back relaxation loop that contributes to the sustained waveform oscillations. The input/driver transistors in the gain stages act as current switching components and, hence affect the amplitude and frequency of the waveform through the DC bias currents. Thus the circuit can also be viewed as a current-steering oscillator. A simple current mirror configuration, M7, M8, M9 and M10, is used for the two approaches to provide multiple bias current from one reference current ( $I_{Ref}$ ). Based on the periodical charging and discharging operation of the capacitor  $C$ , ELF WFG circuit, provides a periodical square waveform output signal at  $V_o$  and an exponential waveform at  $V_c$  with no input.

### 3.5 Circuit Operation of The ELF WFG

The operation of the ELF WFG (oscillator) can be understood through the waveforms shown in Figure 3.4 attained by the periodical charging and discharging of the capacitor  $C$ . The nodes in the circuit have an upper and a lower quasi-stable voltage level, as well as an unstable voltage level between these extremes, during state transition where the devices operate in the linear amplification region. These extreme voltage levels correspond to the lower discharged voltage  $-V_{clp}$  and the upper charged voltage  $+V_{cup}$  of the capacitor voltage,  $V_C$ . Also, the maximum and minimum output voltage ( $V_o$ ) levels of the ELF WFG are indicated by  $V_{sat+}$  and  $V_{sat-}$ , respectively. When the capacitor passes through the uncharged state (zero crossing in the voltage scale), the devices in the differential amplifier are in a transition, to switch the path of the bias current. During the positive half-cycle of the output (Period  $T1$ ), the capacitor is charging from  $-V_{clp}$  to  $+V_{cup}$  and M1 is carrying most of the bias current  $IB1$ . During this period M2 is almost cut-off, while M4 is in deep triode [58] (with very small drain current).

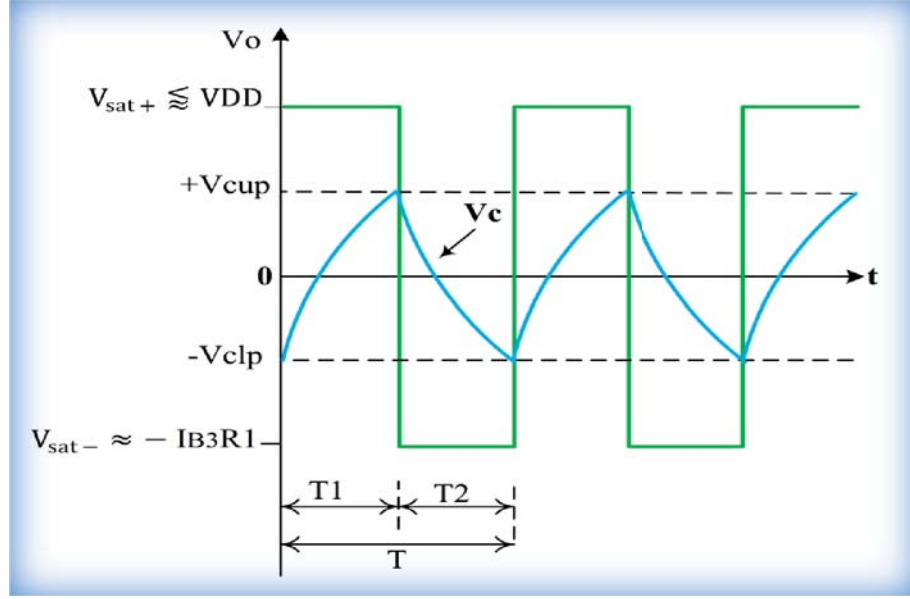


Figure 3.4. Waveforms in the proposed ELF WFG.

The diode-connected M3 also carries the bias current  $IB1$ , but the mirror is inactive, as M4 is not in saturation. With M4 in deep triode, M5 is almost turned off [58] resulting in the bias current  $IB2$  becoming a constant charging current, contributing electrons to the gate of M6 and bringing its potential down near the negative supply voltage. M6 is thus acting as a switch operating in the deep triode region, resulting in the maximum output voltage ( $V_{sat+}$ ) being near the positive supply voltage. The drain current of the switch M6 is the sum of the bias current  $IB3$ , the capacitor charging current and the current through resistor  $R1$ . When the capacitor voltage reaches  $+V_{cup}$ , the negative half-cycle of the output (Period  $T2$ ) begins with M2 going into triode mode and carrying most of the bias current  $IB1$ . During this period M1, M3 and M4 are operating in saturation [58] with very low overdrives. Although the M3 and M4 current mirror is active, the mirror current is very small, and, most of  $IB1$  becomes a charging current bringing the gate of M5 lower towards the negative supply voltage, by supplying electrons to the gate. As a consequence, M5 is behaving almost as a closed switch, resulting in the gate of M6 being near the positive supply. Now, with M6 almost off, the continuity of the bias current  $IB3$  requires that a large (significant) part of it will now flow through the resistor  $R1$ , as the capacitor discharging current through  $R2$  (with  $R2 \gg R1$ ) is very small and diminishing with a large time constant  $R2 \times C$ . Consequently, the minimum output voltage ( $V_{sat-}$ ) achieved by the circuit can be given

by  $-IB3 \times R1$  as a rough approximation. As the discharge period begins and continues, current through M6 gradually increases (M6 moving from near-OFF in saturation to near-ON in triode), at the expense of the diminishing discharging current, so that the total of the capacitor discharge current through  $R2$ , the M6 drain current and the current through  $R1$  (total current arriving at the output node) remains equal to the sinking current  $IB3$  (*the total current leaving the output node*). Based on the above, approximate design equations relating circuit variables such as bias currents, device sizes ( $W$ ,  $L$ ), threshold voltages ( $V_{THN}$ ,  $V_{THP}$ ) and passive component values, with oscillator parameters such as amplitude, frequency and duty cycle, can now be derived. In general, the loop gain ( $A_V^+$ ) around the positive feedback path must be large to sustain oscillation which can be approximately given by,

$$A_V^+ = \frac{1}{2} (g_{m1} \cdot k + g_{m2}) \cdot g_{m5} \cdot g_{m6} \frac{r_{o4} \cdot r_{o2}}{r_{o4} + r_{o2}} \cdot r_{o5} \cdot \frac{r_{o6} \cdot R1}{r_{o6} + R1} \quad (3.11)$$

Where,  $gm1$ ,  $gm2$ ,  $gm5$  and  $gm6$  are the trans-conductance of M1, M2, M5 and M6 in the linear amplification range. The factor  $k$  is the device width ratio  $W_{M4}/W_{M3}$  for the mirror pair M4 and M3, assuming an appropriate channel length for both the devices. The bias current sources are assumed to have very high output impedances. The value of resistor  $R1$  thus affects both the positive feedback loop gain and the minimum output voltage  $V_{sat-}$ . For the positive half cycle ( $T1$ ) the capacitor charging voltage from low-to-high,  $V_{CL-to-H}(t)$  from time  $t = 0+$  (beginning of the charging period), can be given by,

$$V_{CL-to-H}(t) = -V_{clp} \cdot e^{-\frac{t}{R_2 C}} + VDD (1 - e^{-\frac{t}{R_2 C}}) \quad (3.12)$$

And thus, the low-to-high charging current is given by,

$$i_{CL-to-H}(t) = \frac{(V_{clp} + VDD) \cdot e^{-\frac{t}{R_2 C}}}{R_2} \quad (3.13)$$

Since  $V_{CL-to-H}(T1) = V_{cup}$ , the time period  $T1$  from (3.12) is given by,



$$T1 = R_2 C \ln \frac{VDD + V_{clp}}{VDD - V_{cup}} \quad (3.14)$$

M6 being ON in triode (as a switch) at the beginning of this capacitor charging period,  $t = 0+$ ,

$$i_{M6_{L-to-H}}(0+) = IB3 + i_{C_{L-to-H}}(0+) + \frac{VDD}{R_1} \quad (3.15)$$

As the charging current reduces from a maximum of  $(V_{clp} + VDD)/R_2$  at  $t = 0+$ ,  $i_{M6}(t)$  also reduces while still operating as a switch with very small drain-to-source drop. M6 thus requires a very small  $R_{DS}$  (ON), using a reasonably wide PMOS device. Also, M2 has a very low overdrive and is in saturation with only a small component of  $IB1$  flowing through it. Assuming approximately 10% of  $IB1$  flowing through M2,

$$V_{GS2_{L-to-H}}(0+) = \sqrt{\frac{0.2 IB1}{\mu_n C_{ox} \frac{W_2}{L_2}}} + V_{THN} \quad (3.16)$$

Then,

$$-V_{clp} = -|VSS| + V_{DS8} + V_{GS2_{L-to-H}}(0+) \quad (3.17)$$

Also, assuming the current source device, M8, is biased just near the edge of saturation, and the constant bias current is switching between M1 and M2 (driven by symmetrical differential input), the drain of M8 is approximately at AC (virtual) ground [58], so that,

the overdrive  $V_{OD8} \approx V_{DS8}$ , i.e.  $V_{DS8} \approx V_{OD8} = \sqrt{\frac{2 IB1}{\mu_n C_{ox} \frac{W_8}{L_8}}}$  and,

$$-V_{clp} \cong -|VSS| + V_{OD8} + \sqrt{\frac{0.2 IB1}{\mu_n C_{ox} \frac{W_2}{L_2}}} + V_{THN} \quad (3.18)$$

The above equation relates the device aspect ratios of M2 and M8 as well as the bias current  $IB1$  with the lower discharged voltage level of the capacitor for the low-to-high state transition of the Schmitt Trigger. Larger aspect ratios ( $W/L$ ) require smaller overdrives to allow the same bias current and hence bring  $-V_{clp}$  closer to the negative

supply. On the other hand, larger bias current  $IB1$  reduces the magnitude of  $V_{clp}$  and hence reduces  $T1$  as can be seen from (3.14). Also, M5 is in saturation at  $t = 0+$ , so that,

$$V_{GS5_{L-to-H}}(0+) = \sqrt{\frac{2IB1}{\mu_P C_{ox} \frac{W5}{L5}}} + |V_{THp}| \quad (3.19)$$

Hence, the voltage at the drain of M2 is given by,

$$V_{D2_{L-to-H}}(0+) = VDD - \sqrt{\frac{2IB2}{\mu_P C_{ox} \frac{W5}{L5}}} - |V_{THp}| \quad (3.20)$$

Next, for the negative half cycle ( $T2$ ), the capacitor discharging voltage from high-to-low  $V_{CH-to-L}(t)$  from time  $t = 0+$  (beginning of the discharging period), can be given by,

$$V_{CH-to-L}(t) = V_{cup} \cdot e^{-\frac{t}{R_2 C}} - |V_{sat-}| (1 - e^{-\frac{t}{R_2 C}}) \quad (3.21)$$

And hence, the high-to-low charging current is given by,

$$i_{CH-to-L}(t) = \frac{(V_{cup} + |V_{sat-}|) \cdot e^{-\frac{t}{R_2 C}}}{R_2} \quad (3.22)$$

Since  $V_{CH-to-L}(T2) = -V_{clp}$ , the time period  $T2$  from (3.21) is given by,

$$T2 = R_2 C \ln \frac{|V_{sat-}| + V_{cup}}{|V_{sat-}| - V_{clp}} \quad (3.23)$$

Hence, combining (3.14) and (3.23), the overall period is given by,

$$T = R_2 C \ln \left( \frac{VDD + V_{clp}}{VDD - V_{cup}} \right) \cdot \left( \frac{|V_{sat-}| + V_{cup}}{|V_{sat-}| - V_{clp}} \right) \quad (3.24)$$

So that, the overall frequency of the waveform is given by,

$$f_{waveform} = \frac{1}{R_2 C \ln \left( \frac{VDD+V_{clp}}{VDD-V_{cup}} \right) \cdot \left( \frac{|V_{sat-}|+V_{cup}}{|V_{sat-}|-V_{clp}} \right)} \quad (3.25)$$

With M6 being in saturation at the beginning of this capacitor discharging period,  $t = 0+$ , the drain current through M6 is given by,

$$i_{M6H-to-L}(0+) = IB3 - i_{CH-o-L}(0+) - \frac{|V_{sat-}|}{R1} \quad (3.26)$$

With significant part of  $IB3$  sinking the current through  $R1$  coming towards the output node ( $R2 \gg R1$ ), and M6 initially having very small overdrive operating in saturation, as the low discharging current diminishes, the current through M6 increases (with increasing overdrive), so that,

$$|V_{GS6H-to-L}(0+)| = \sqrt{\frac{2 \left[ IB3 - \frac{|V_{sat-}|}{R1} - \frac{(V_{cup} + |V_{sat-}|)}{R2} \right]}{\mu_P C_{ox} \frac{W6}{L6}}} + |V_{THp}| \quad (3.27)$$

M5 is in triode at  $t = 0+$  of the high-to-low discharge period; hence, using  $V_{DS5}(0+) = V_{GS6}(0+)$  for this period,

$$|V_{GS5H-to-L}(0+)| \cong \frac{IB2}{\mu_P C_{ox} \frac{W5}{L5} \left( \sqrt{\frac{2 \left[ IB3 - \frac{|V_{sat-}|}{R1} - \frac{(V_{cup} + |V_{sat-}|)}{R2} \right]}{\mu_P C_{ox} \frac{W6}{L6}}} + |V_{THp}| \right)} + |V_{THp}| \quad (3.28)$$

Hence,

$$V_{D2H-to-L}(0+) \cong VDD - \frac{IB2}{\mu_P C_{ox} \frac{W5}{L5} \left( \sqrt{\frac{2 \left[ IB3 - \frac{|V_{sat-}|}{R1} - \frac{(V_{cup} + |V_{sat-}|)}{R2} \right]}{\mu_P C_{ox} \frac{W6}{L6}}} + |V_{THp}| \right)} - |V_{THp}| \quad (3.29)$$

So for the Schmitt Trigger to operate properly,

$$V_{D2H-to-L}(0+) \ll V_{D2L-to-H}(0+) \quad (3.30)$$

M2 is now operating in the triode region and carries most of the tail bias current  $IB1$ . Hence, assuming approximately 90% of  $IB1$  flowing through M2,

$$V_{GS2H-to-L}(0+) \cong \frac{0.9 IB1}{\mu_n C_{ox} \frac{W2}{L2} \cdot V_{DS2H-to-L}(0+)} + V_{THN} \quad (3.31)$$

Using (3.29),

$$V_{GS2H-to-L}(0+) \cong \frac{0.9 IB1}{\mu_n C_{ox} \frac{W2}{L2} \cdot [V_{D2H-to-L}(0+) + |V_{SS}| - V_{OD8}]} + V_{THN} \quad (3.32)$$

Also,

$$V_{cup} \cong -|V_{SS}| + V_{GS2H-to-L}(0+) + V_{OD8} \quad (3.33)$$

Using (3.32),

$$V_{cup} \cong -|V_{SS}| + \frac{0.9 IB1}{\mu_n C_{ox} \frac{W2}{L2} \cdot [V_{D2H-to-L}(0+) + |V_{SS}| - V_{OD8}]} + V_{THN} + V_{OD8} \quad (3.34)$$

With  $V_{D2H-to-L}(0+)$  being a function of  $V_{cup}$  through (3.29), equation (3.34) now forms an implicit design equation for determining  $V_{cup}$  based on the values of the other parameters including  $IB1$ ,  $IB2$  and  $IB3$ . It is to be noted that during the positive half cycle ( $T1$ ), the  $V_{sat+}(\leq VDD)$  can diminish considerably from the supply voltage level if  $R1$  is small, due to the voltage divider action with the ON-resistance of M6 in the triode region.

### 3.6 Simulation and Performance Analyses of The ELF WFG

The proposed ELF WFG in Figure 3.3 has been designed and simulated in 130-nm CMOS process technology on Mentor Graphics Pyxis version 10 [192]. The Pyxis Schematic with IBM custom design kits is used to modularize the design and was verified to function correctly. Eldo simulator Mentor Graphics tools is used to simulate the netlist, analyse and verify the characteristics of the parameters of the circuit to

assure the accurate performance of the designed circuit. The supply voltage is set to  $\pm 1.2$  V. The design values for the active and passive elements of the different stages of the circuit are chosen depending on the specific ELF operation and power consumption constraints. Two sets of device dimensions and circuit elements are developed and simulated for comparison and are summarized in Table 3.1 and Table 3.2, respectively.

Table 3.1. Transistor dimensions for the two ELF WFG designs (1 and 2).

Transistors	(W/L) ( $\mu\text{m}/\mu\text{m}$ )	
	(1)	(2)
M1	12/0.24	18/0.24
M2	10/0.24	16/0.24
M3 = M4	14/0.24	20/0.24
M5	12/0.24	18/0.24
M6	2/0.24	10/0.24
M7	10/0.24	20/0.24
M8	6.4/0.24	14.4/0.24
M9	2.5/0.24	9.4/0.24
M10	2.5/0.24	2.6/0.24

Table 3.2. Component values for the two ELF WFG designs (1 and 2).

Stages	I bias ( $\mu\text{A}$ )		Passive components	
	(1)	(2)	(1)	(2)
Stage 1	100	150	$R1 = 15 \text{ k}\Omega$	$R1 = 1 \text{ k}\Omega$
Stage 2	30	100	$R2 = 25 \text{ M}\Omega$	$R2 = 415 \text{ k}\Omega$
Stage 2	35	20	$C1 = 1 \text{ nF}$	$C1 = 64 \text{ nF}$
Mirror reference	123	123	$R_{\text{ref}} = 19 \text{ k}\Omega$	$R_{\text{ref}} = 19 \text{ k}\Omega$

The first design uses larger values of  $R1$  and  $R2$  and a lower value of  $C$  compared to the second design, in order to function accurately and provide similar waveforms. In agreement with the theoretical analysis, the resistance and capacitance values used provide similar time-constants for the two cases, which lead to similar waveform frequencies. The purpose of implementing a second design is to investigate the variations in amplitude and frequency range with variation in the bias currents and

component sizes, as well as the power and area consumption while setting almost the same relaxation time-constant value for the desired ELF waveform. Accordingly, the product  $-R1 \times IB3$  which determines theoretically the lower output voltage level ( $V_{sat-}$ ), provides a higher peak-to-peak range for the first design compared to the second design. Small device mismatch (*'width pre-distortion'*) is introduced between M1 and M2 for waveform duty cycle adjustment (*through input referred offset voltage*). This feature also aids in the start-up of the oscillatory behaviour in association with the charge/discharge relaxation technique. Simulations indicate that the theoretical estimates of the regions of MOSFET operation during the High-to-Low and Low-to-High transitions are quite accurate. The simulated transient response of the output waveform from the first design is shown in Figure 3.5.

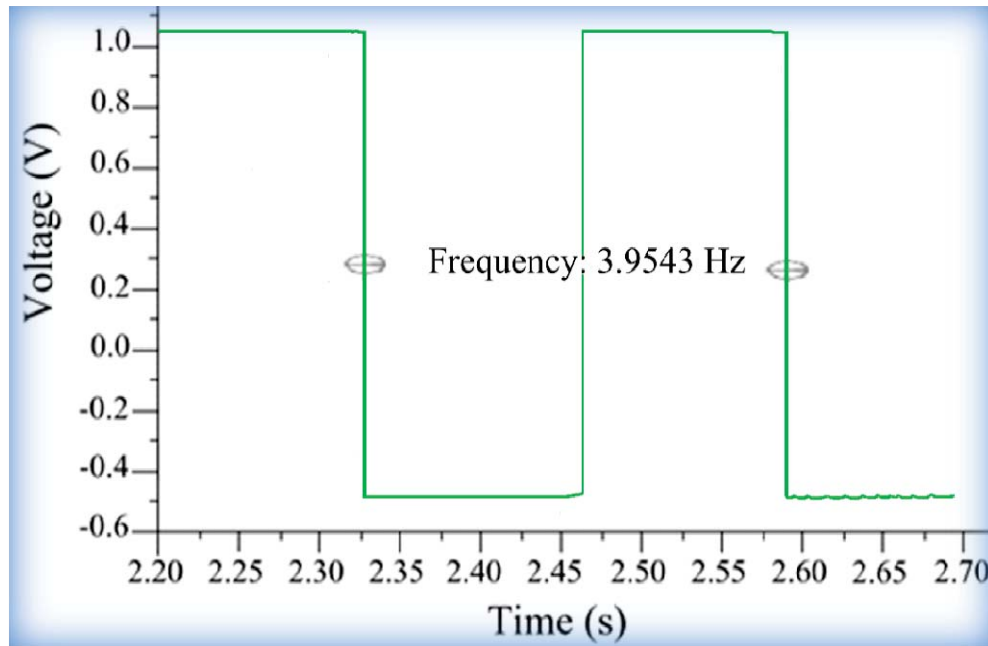


Figure 3.5. Simulated transient output waveforms for ELF WFG for the first design.

The same topology can also generate exponential waveforms, since the voltage across the capacitor rises and falls exponentially, due to charge and discharge of the capacitor  $C$ ; the ELF WFG circuit can then oscillate and generate a periodical square waveform and exponential waveform. A comparison of the simulated performance of

the first design (design 1) with the second design (design 2) is provided in Table 3.3. The analysis in section 3.5 is confirmed by the simulated values of the output high voltage ( $V_{sat+}$ ), being a bit higher in the case of  $R_I=15k\Omega$  in the first design, compared to that for  $R_I=1k\Omega$  in the second design, due to the corresponding voltage divider actions in the two cases. The first approach consumes  $691\mu W$  while the second approach consumes  $943\mu W$  when subjected to the same supply voltage range ( $V_{DD} = 1.2V$ ,  $V_{SS}=-1.2V$ ). The ELF oscillator frequencies achieved for the two designs are around  $3.95Hz$  and  $3.90Hz$ , respectively. Also, the circuit can source a considerable amount of current at the output stage, being about  $104.2\mu A$  and  $991.1\mu A$  for the first and the second design, respectively, which can be useful in current source applications. Amplitude and frequency control are discussed in the next two sub-sections.

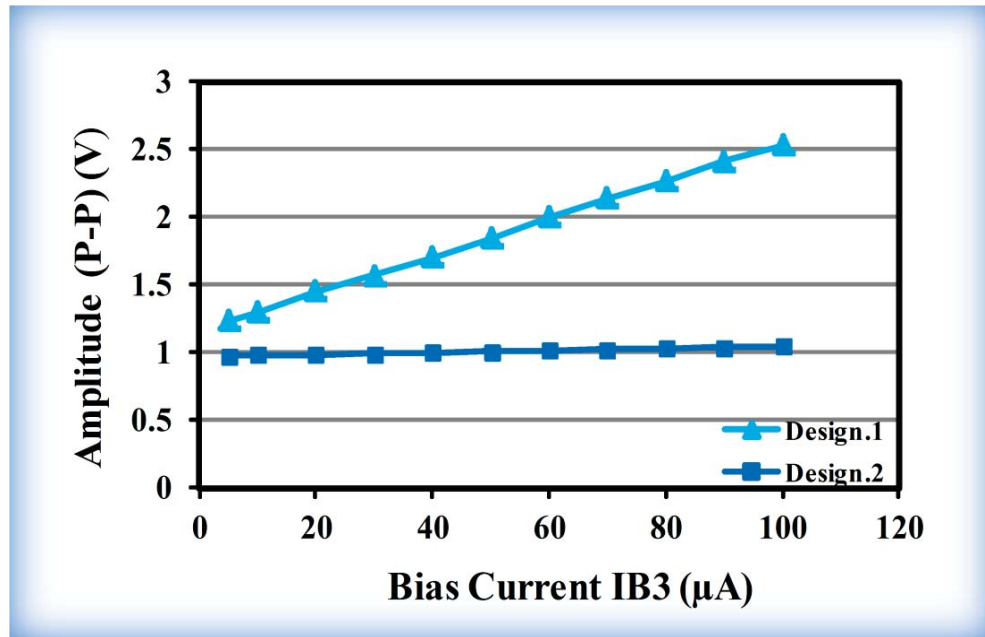
Table 3.3. Comparison of the simulation performance of the first ELF WFG design (design 1) with the second ELF WFG design (design 2).

Parameters	(1)	(2)
Technology	0.13- $\mu m$ CMOS	0.13- $\mu m$ CMOS
Amplitude	1.556 Vpp	981 mVpp
Frequency	3.95 Hz	3.90 Hz
Duty cycle	52%	54%
Output current sourcing	104 $\mu A$	991 $\mu A$
Short circuit output current	534.40 $\mu A$	2.77mA
Period	253.47ms	256.03ms
Rise time	174.78ps	199.80ps
Fall time	206.97ps	139.32ps
Slew rate	5.78GV/ns	5.33GV/ns
Supply voltage	$\pm 1.2V$	$\pm 1.2V$
Power consumption	691 $\mu W$	943 $\mu W$

### 3.6.1 Amplitude Control of The ELF WFG

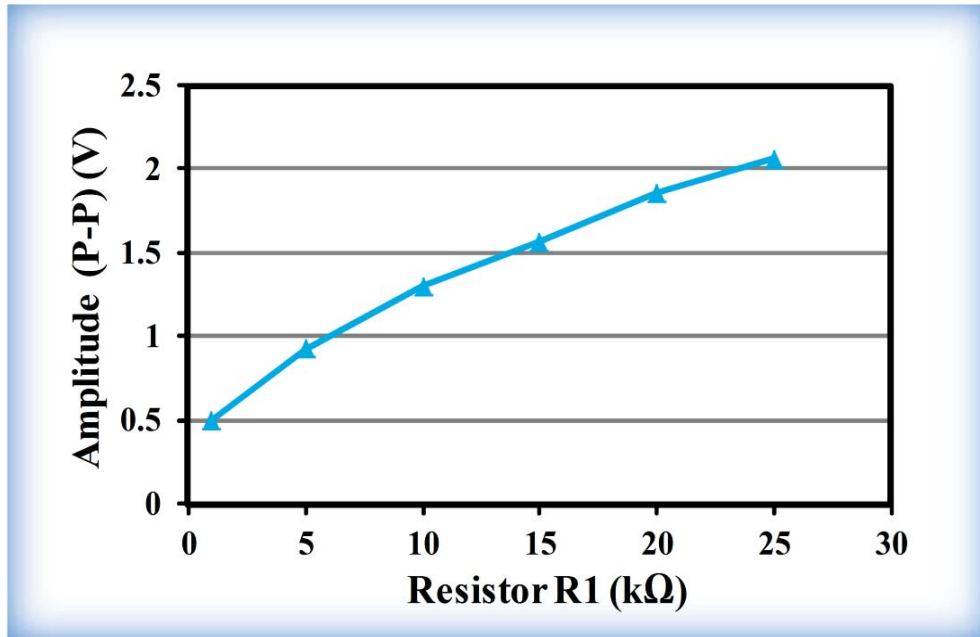
The circuit design for CMOS ELF WFG was also simulated to determine the amplitude control behaviour. The peak-to-peak output voltage of the circuit (*determined by the regenerative feedback*) can be monotonically controlled by either the bias current

$IB3$  or the resistor  $RI$ , as per the theoretical analysis in section 3.5. Plots of amplitude vs.  $IB3$  and amplitude vs.  $RI$  for the two designs are depicted in Figure 3.6 (a), (b) and (c). The first and the second design can provide amplitude (P-P) variations of 1.2V to 2.5V (using  $RI=15\Omega$ ) and 0.98V to 1.05V (using  $RI=1k\Omega$ ), respectively, with  $IB3$  variation between  $10\mu A$  and  $100\mu A$ . On the other hand, amplitude (P-P) variation of 0.5V to 2V (using  $IB3=35\mu A$ ) and 0.5V to 1V (using  $IB3=20\mu A$ ) can be achieved with  $RI$  variation between  $1k\Omega$  to  $25k\Omega$  and  $0.2k\Omega$  to  $1.2k\Omega$ , respectively, for the first and the second design. The results confirm that the output voltage of the ELF WFG is controllable by the bias current  $IB3$ , as well as by the resistor  $RI$ . For smaller values of  $RI$ , due to voltage divider action with the triode regime PMOS switch M6, the positive swing of the waveform is reduced considerably, as shown in the Figure 3.6 (b) and (c) in the lower end of the  $RI$  scale.

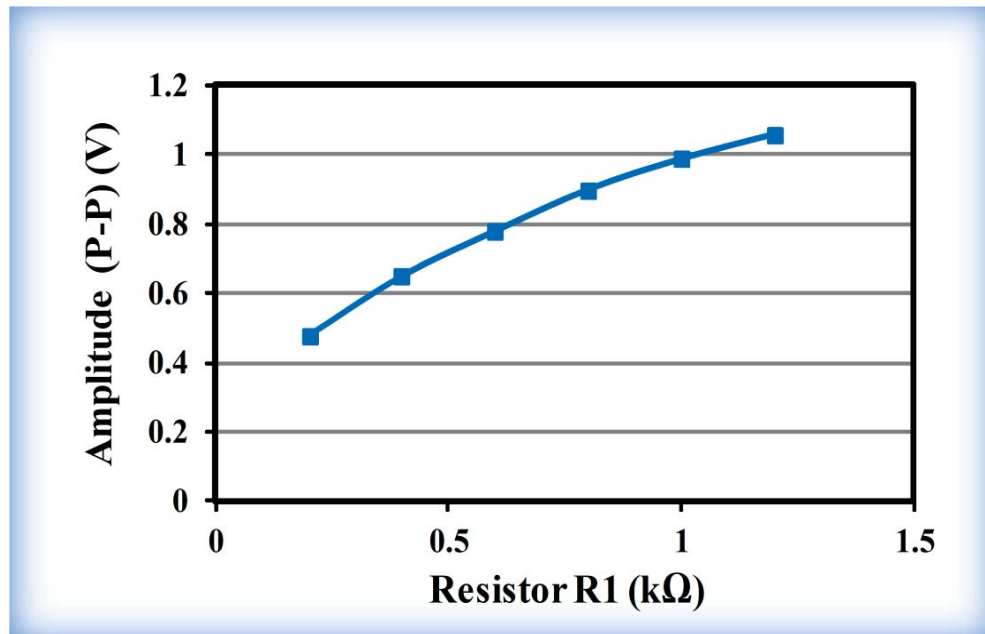


(a) Amplitude (P-P) variation with  $IB3$  for the two ELF WFG designs





(b) Amplitude (P-P) variation with  $R1$  for the first ELF WFG design



(c) Amplitude (P-P) variation with  $R1$  for the second ELF WFG design.

Figure 3.6. Amplitude (P-P) variation with the bias current  $IB3$  and resistor  $R1$ , (a) amplitude (P-P) variation with  $IB3$  for the two WFG<sub>RC</sub> designs, (b) amplitude (P-P) variation with  $R1$  for the first design and (c) amplitude (P-P) variation with  $R1$  for the second design.

### 3.6.2 Frequency Control of The ELF WFG

The circuit was also tested to determine the frequency tunability. The frequency of the output signal can be controlled by  $R2$  (while  $C$  is fixed) as well as by  $IB1$ . The resistor  $R2$  varies the frequency through the variation of the charging/discharging time constant as per equation 3.25. On the other hand,  $IB1$  varies the frequency through the variation of the lower and upper Schmitt Trigger tripping points ( $-V_{clp}$ ,  $V_{cup}$ ) as per equation 3.18 and equation 3.34. However, as evident from 3.25 variation of frequency is a weaker function of  $IB1$  compared to  $R2$ . Plots of oscillation frequency vs. bias current  $IB1$ , and, oscillation frequency vs. resistor  $R2$  for the two designs is shown in Figure 3.7, and, Figure 3.8 (a) and (b) respectively. The first and second designs can, respectively, provide a narrow frequency variation of 3.7Hz to 4.3Hz and 3.6Hz to 4.1Hz for  $IB1$  variation between  $50\mu A$  and  $250\mu A$ . On the other hand, frequency variation for the first design in the wide range of 90Hz to 1kHz can be achieved by varying  $R2$  from  $1100k\Omega$  to  $50k\Omega$ . Also, wide frequency variation for the second design of 10Hz to 350Hz can be achieved by varying  $R2$  from  $100k\Omega$  to  $5k\Omega$ .

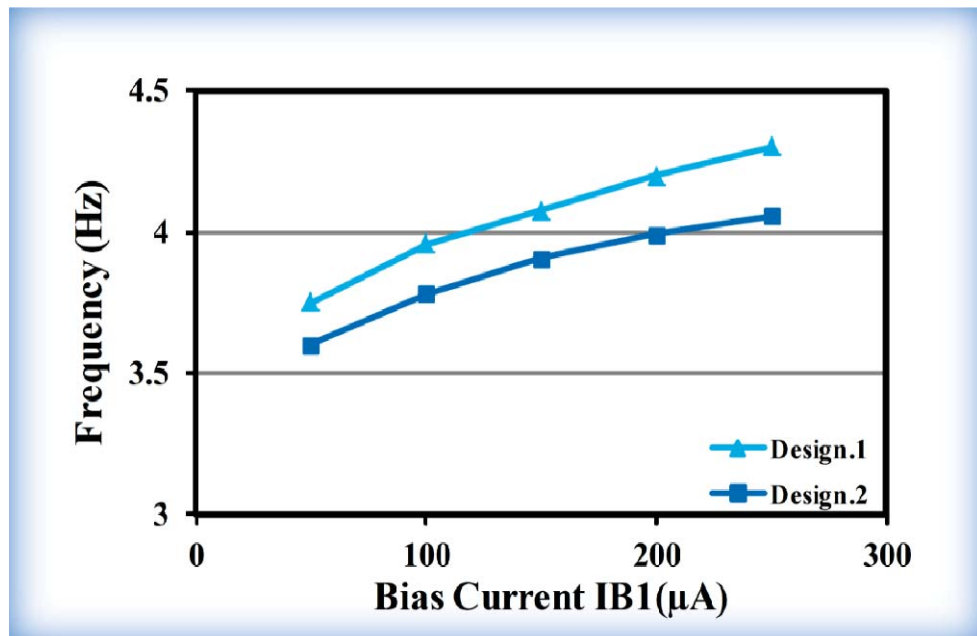
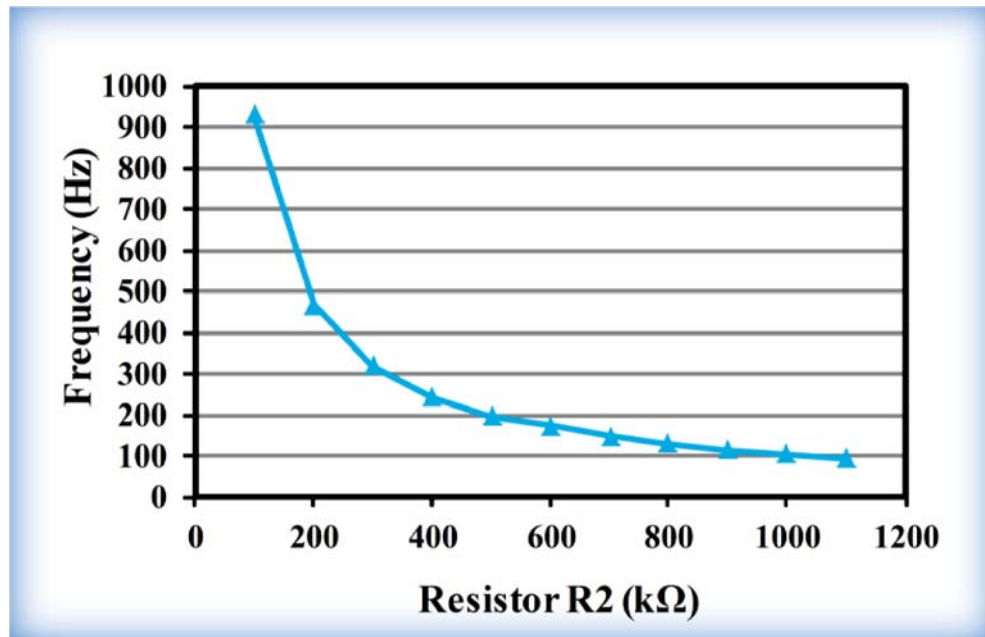
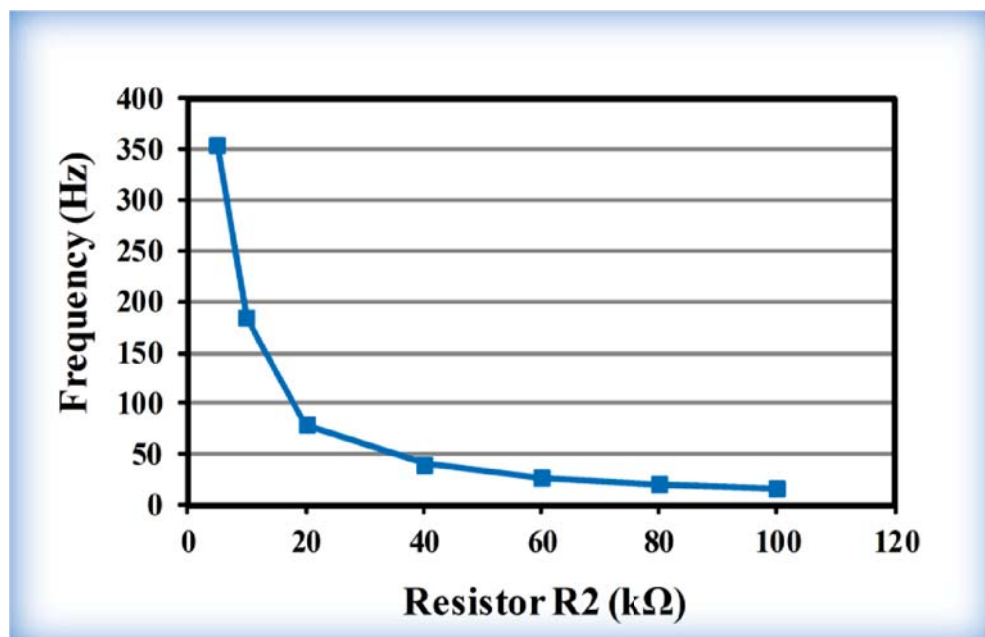


Figure 3.7. Frequency tuning with bias current  $IB1$  for the two ELF WFG designs.



(a) Frequency tuning with resistor  $R_2$  for the first ELF WFG design



(b) Frequency tuning with resistor  $R_2$  for the second ELF WFG design.

Figure 3.8. Frequency tuning with resistor  $R_2$ , (a) for the first ELF WFG design, (b) for the second ELF WFG design.

The simulations thus agree closely with the mathematical analysis. Also, the simulations indicate that for wide frequency tuning, frequency variation through the relaxation mechanism using  $R2$  is more suitable than using the bias current. The total current drain by the two waveform generators are as low as  $288\mu\text{A}$  and  $393\mu\text{A}$  to generate oscillation frequencies of  $3.95\text{Hz}$  and  $3.90\text{Hz}$ , respectively, thus enabling the circuits to be used in micro-power applications. The overall simulation results indicate that the first design (design 1) provides wider amplitude and frequency range for either bias current or resistor based multivibrator control compared to the second design (design 2), at the expense of larger resistor values. However, in order to examine the circuit ability to generate moderate low frequencies (MLF) around  $100\text{Hz}$  using small capacitor values, an extensive simulated circuit is used with a suitable set of capacitor values. The simulation results show that the two designed circuits can achieve oscillation frequency, about  $100\text{Hz}$ , with small capacitor values of  $40\text{pF}$  and  $2.3\text{nF}$  for the first and the second design, respectively, (while  $R1$ ,  $R2$  and  $IB1$  are fixed).

### **3.7 Layout and Fabrication of The ELF WFG**

Layout is the final stage of the IC circuit design. It sets up the geometry and the circuit components with interconnecting wire, by using design rules to develop the physical design. Physical design defines the physical size and performance of the circuit. The layout of the proposed ELF WFG in Figure 3.3 for the two designs has been implemented in  $130\text{-nm}$  IBM CMOS process technology on Mentor Graphics Pyxis CAD programme. The Pyxis programme provides design flow facilities and has all the functionality of the Pyxis layout to produce high quality design. It is used to create the layout and verified using design rule checking (DRC) and layout versus schematic (LVS), to ensure that the circuits function correctly [192]. Topological design rules are required, for implementing the enhancement of the layout area. A simple technique is used in this design, to minimize the chip area; all cells are connected simply in a fashion to conveniently route supply voltage and ground, as well as substrate together. The PMOS and NMOS cells are laid out end to end to minimize the area required for the layout of the MOSFETs device. This arrangement can enhance the regularity of the layout and horizontal runs of metal are then used to supply power and ground to the devices as well as for the well and substrate. Considering the design rules, all routing is

completed manually with verifying DRC. The DRC and LVS checks are performed for each completion sub-cell and they pass. Taking the size and the regularity of the implemented device and components into account, optimum size layout for all circuit is achieved to minimize the chip area, and remarkable reductions in area are achieved. The first design occupies a small chip-area of  $346.5\mu\text{m}^2$  (excluding the resistor and capacitor). The resistors for this design occupy  $31600\mu\text{m}^2$  (i.e. around  $0.0316\text{mm}^2$ ). The second design occupies  $975.62\mu\text{m}^2$  (including the resistor). This compares well with [107]; the chip area of its complete circuit is around  $70000\mu\text{m}^2$  (i.e.  $0.07\text{mm}^2$ ).

NMOS (2.5V) (Dgnfet) and PMOS (Dgpfet) devices available in this process were utilized to allow the  $\pm 1.2\text{-V}$  supply. A novel concept of employing a combination of the different types available of on-chip p+ polysilicon resistors in the 130-nm IBM CMOS process, such as an OPRRP resistor (with sheet resistance of  $1700\Omega/\square$ ), OPRPP resistor (with sheet resistance of  $228\Omega/\square$ ) which is used to fully implement the large integrated resistors (as hetero-resistors). ‘OP’, ‘RR’ and ‘RP’, respectively, denote ‘salicide block’, ‘high value resistor’ and ‘precision resistor’. The use of ‘silicide’ is to reduce the effect of high temperature on the resistivity [58]. Combining such resistances helps to improve the accuracy of the integrated precision resistors  $R1$  and  $R2$ , by achieving a lower PVT in the resistance value along with optimized area, rather than using a single homogeneous resistor of the same value and area [121] (section 2.6.1.1). The resistor with highest sheet resistivity is used, allowing for the most compact layout for a given resistance value. Considering the minimum dimensions (width and length values) and resistor matching for the recommended layout rules, [72] the resistors were built by combining identical units, OPRPP and OPRRP resistors, in series, as shown in Figure 3.9.

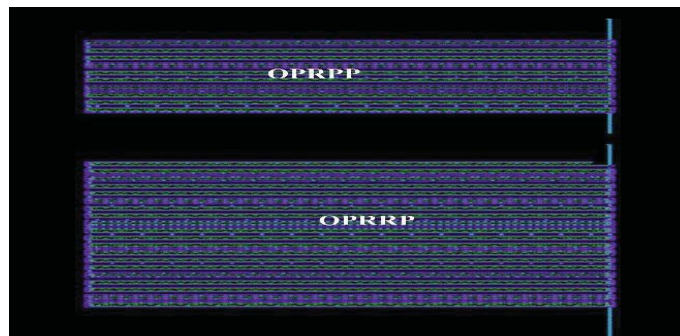


Figure 3.9. The layout of on-chip identical units OPRPP and OPRRP resistors, in series.

As explained in section 2.6.1.1, the simple  $kT/C$  result as per 2.5, reveals that the total thermal noise at the output of the  $RC$  circuit is independent of the value of the integrated  $R$  and is limited by the size of the capacitor. The on-chip current mirror resistor  $R_{ref}$  was implemented using a reasonably small-area n-well resistor. On-chip implementation of the high resistors has the advantage of reduced temperature sensitivity compared to previous discrete designs. Off-chip capacitors were used for convenience and to limit the overall passive element area. Although capacitors for the two ELF WFG designs were designed and implemented using metal-metal (MIM) to reduce the influence of parasitic parameters and temperature, this would consume a large silicon area. The single MIM capacitor (MIMCAP) is designed by adding a thin layer of metal,  $QY$ , between  $EI$  metal and the underlying layer of metal,  $LY$ .  $QY$  and  $LY$  constitute respectively the top and bottom plate layers, as shown in Figure 3.10, while  $FT$  via level is used for access to separate  $EI$  interconnect layers. The size of the capacitor was calculated using estimates in [72], for the capacitance of a MIMCAP with allowable capacitor shapes, including both square and rectangle layouts, is given by:

$$CN = (CA.L.W) + [CP.2.(L + W)] \quad (3.35)$$

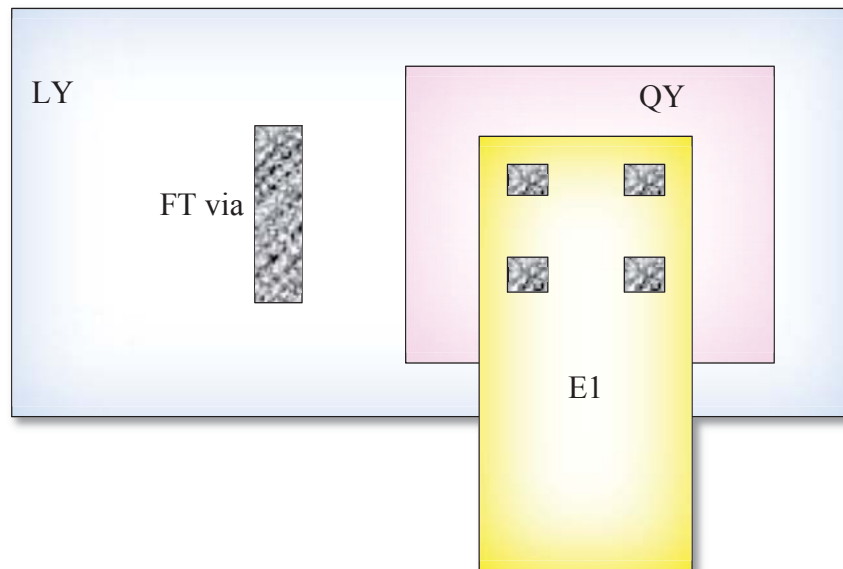


Figure 3.10. Layout for MIM capacitor.

Where,  $CA$  is the plate-area capacitance in  $\text{fF}/\text{mm}^2$  and  $C_p$  is perimeter (fringing) capacitance in  $\text{fF}/\text{mm}$ , which are provided in the CMOS8RF Design Manual.  $L$  and  $W$  are the designed length and width of the top-plate on  $QY$  layer in  $\mu\text{m}$ . A small capacitor in a small  $pF$  range would require a small silicon area, while a large capacitor value would consume a large silicon area which is a problem in miniaturized biomedical devices. As in the two ELF WFG design, considering the minimum  $QY$  plate width ( $W \geq 5.24 \mu\text{m}$ ) and the maximum area per  $QY$  plate ( $100,000 \mu\text{m}^2$ ) according to IBM design pattern density rules, the  $1\text{nF}$  capacitor for the first design is implemented using 20 MIMCAP, while the  $65\text{nF}$  capacitor for the second design requires 1300 MIMCAP with the same capacitance values of  $0.05\text{nF}$  ( $50\text{pF}$ ) connected in parallel ( $C_{Total} = \sum C_{1,2,3...N}$ ). The  $1\text{nF}$  and  $65\text{nF}$  can consume a silicon area (including  $QY$  plate,  $LY$ ,  $EI$  and wiring layers) of  $5.46 \text{ mm}^2$  and  $35440 \text{ mm}^2$  respectively, compared to the small chip-area of the two ELF WFG design. The large silicon area is not the problem. The main problem is that the maximum MIMCAP area rule is limited by all the  $QY$  pattern density rules as well as  $LY$  density rules. The  $QY$  maximum global pattern must meet the requirement of IBM design layout rules [72]. Additional on-chip implantation large MIMCAP area mostly slows the circuit response and causes a waste of power [54]. Therefore, off-chip capacitors are used to limit the overall passive element area. However, using a small MIMCAP capacitor with capacitance values of  $40\text{pF}$  which would consume a small silicon area, around  $0.2184 \text{ mm}^2$ , the first WFG design can be fully implemented on-chip with a small silicon area, to generate MLF of  $100\text{Hz}$  with optimum performance. Figure 3.11 shows the layout for the two ELF WFG circuit (design\_1 and design\_2), Figure 3.11 also shows the layout (including the on-chip designed MIMCAP) for the ELE WFG with capacitor of  $1\text{nF}$  and for MLF with capacitor of  $40\text{pF}$  for the first design for area comparison, while Figure 3.12 (a) and (b) show close views of the complete layout (excluding the capacitor) for chip fabrication for the two ELF WFG circuit. The complete layout (excluding the capacitor) for the two ELF waveform circuit designs was submitted through the American IC fabrication MOSIS academic program. Figure 3.13 and 3.14 illustrates the packaged ELF WFG microchip and the photo microchip of the fabricated die respectively. The devices/components in the layout appear hidden by the IBM CMP fill layer  $EI$  in the chip photo so that their location is indicated by rectangular enclosures.



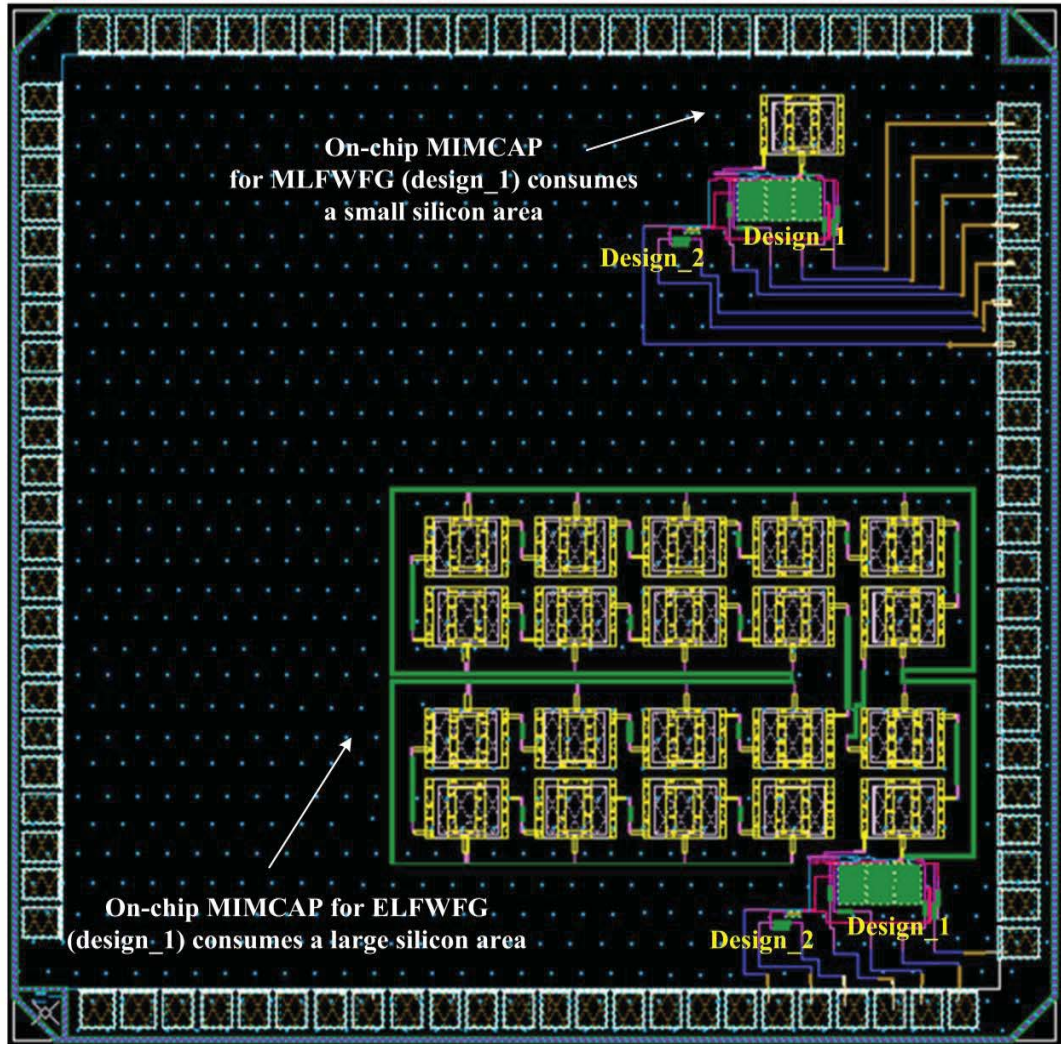
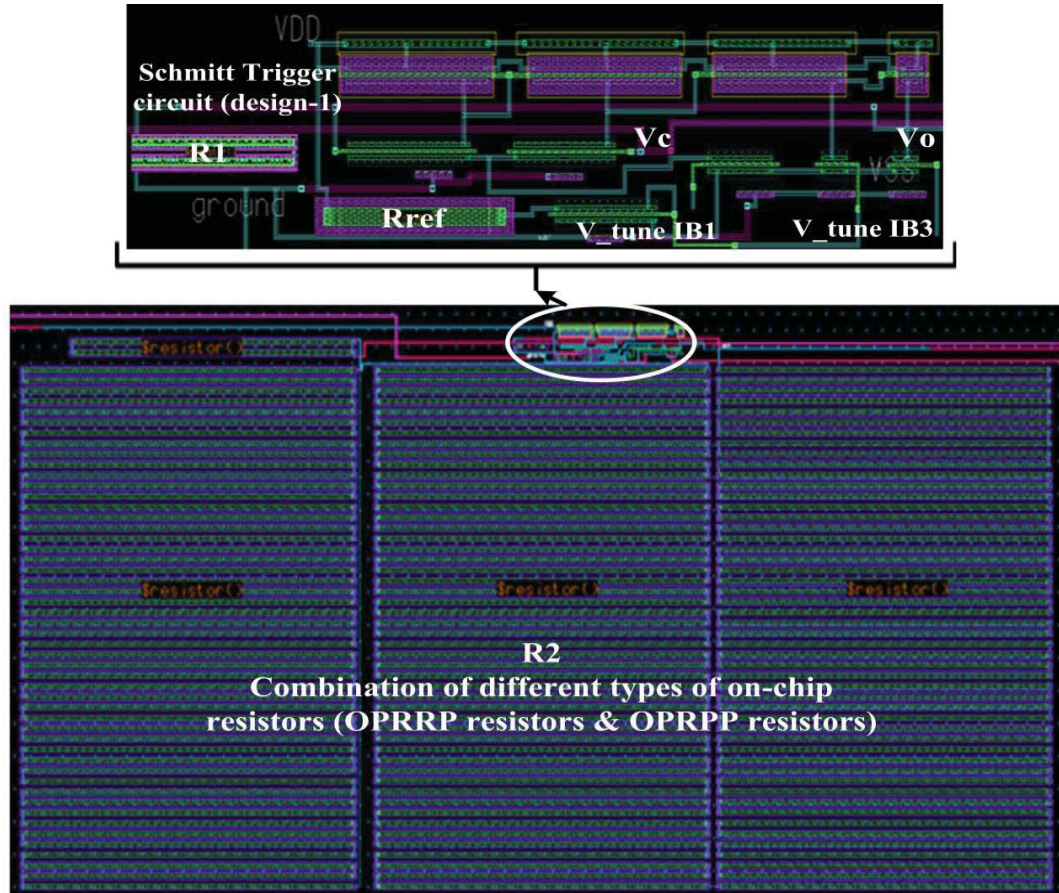
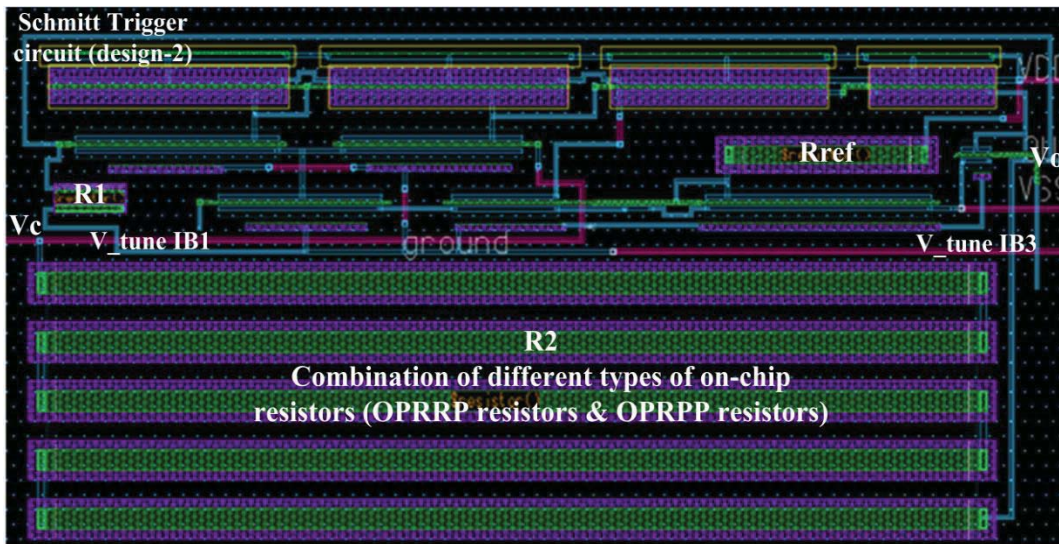


Figure 3.11. The layout for the two ELF WFG circuit (design\_1 and design\_2). The layout on top right corner and bottom right corner represent the complete layout for the two ELF WFG circuit including the on-chip designed MIMCAP for MLF WFG with 40pF, and for ELE WFG with 1nF for design\_1 for area comparison.





(a) The complete layout with the on-chip resistors for the ELF WFG circuit (design\_1).



(b) The complete layout with the on-chip resistors for the ELF WFG circuit (design\_2).

Figure 3.12. A close view of the complete layout (excluding the capacitor) for the two ELF WFG circuit, for chip fabrication (a) for the first design, (b) for the second design. The top is the Schmitt Trigger circuit, while the rectangular box is the combination of different types of on-chip resistors.

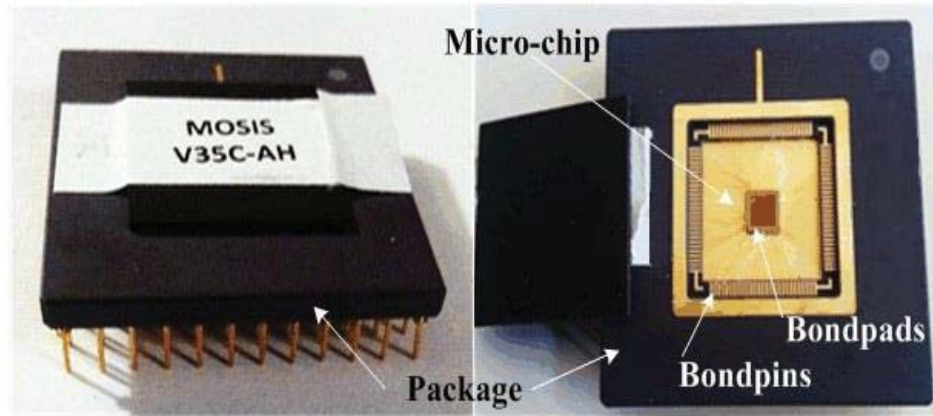


Figure 3.13. Package of the two ELF WFG circuit in PGA.

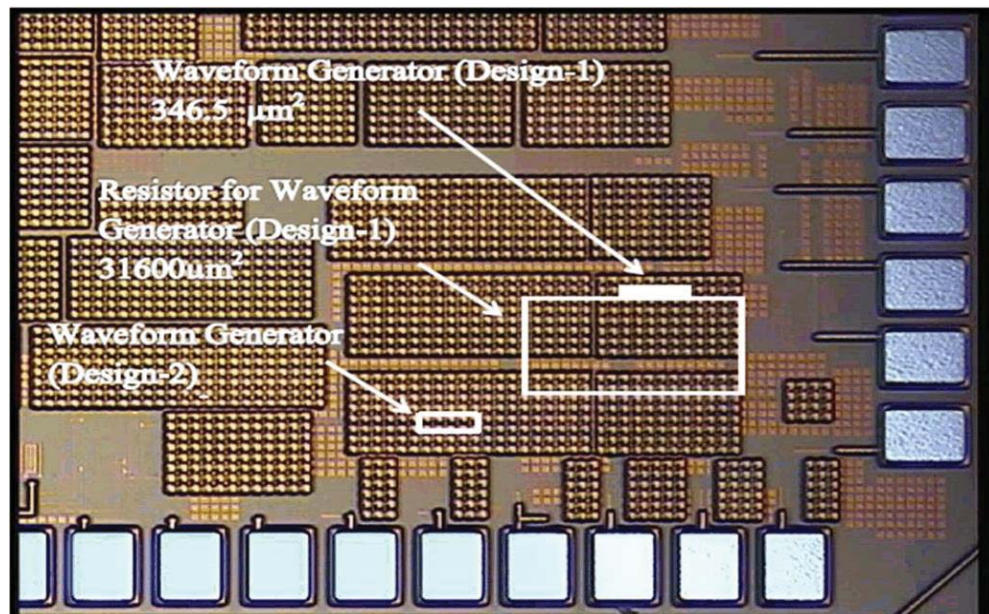


Figure 3.14. Chip photo-micrograph illustrates the location of the integrated two ELE WFG circuit.

### 3.8 Experimental Results of The ELE WFG

Transient measurements are carried out using the digital oscilloscope, Tektronix TDS1012, to evaluate signal quality of the designed circuits. Oscilloscope traces of the output ELF square waveform and the exponential waveform signal of the capacitor voltage  $V_c$ , for the first design, are presented in Figure 3.15. The measured amplitude (P-P) was about 1.22V for a  $\pm 1.2V$  supply voltage, while the measured



frequency was about 3.89Hz which is roughly close to the simulated profile value. Similar results were obtained for the second design, being about 0.96V amplitude (P-P) and 3.79Hz frequency. The variations between simulated and measured ELF frequencies are partially due to external parasitic capacitances at the external capacitor port for  $C$ . The composite value of  $C$  is possibly slightly greater than the intended value of  $C$ , due to the parallel stray capacitances at the  $C$  port. Consequently, a slightly larger time-constant results in a slightly lower measured frequency as per equation 3.25 in section 3.5. The duty cycle varied slightly compared to simulation results. This variation is mostly due to the slight deviation of passive device values after fabrication, as well as, due to the output (and/or bias) DC current imbalances of the OTAs.

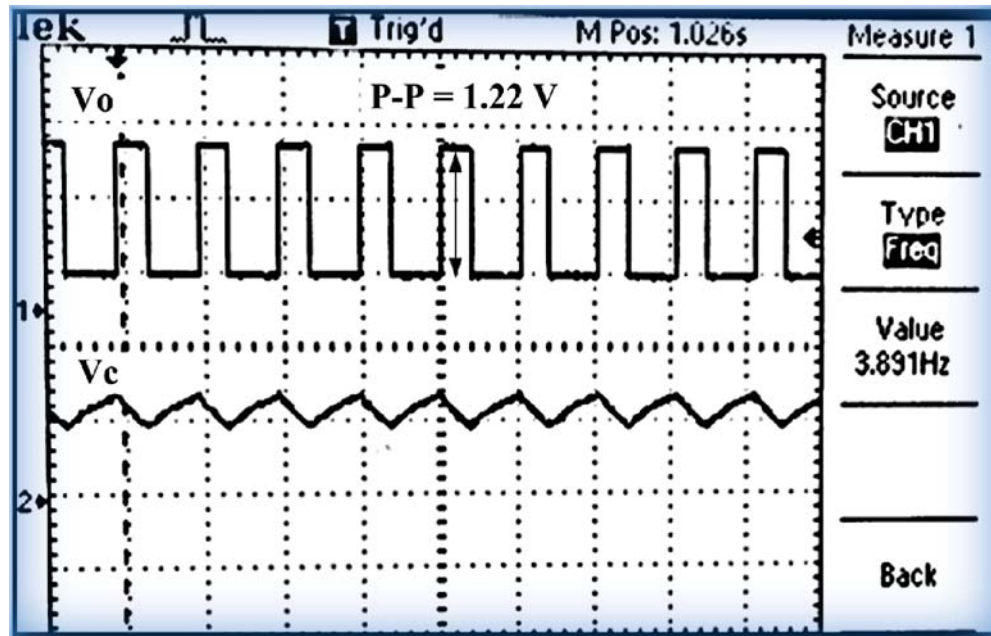


Figure 3.15. Chip outputs of the CMOS ELE WFG for the first design.

The amplitude and frequency tuning behaviour for the two waveform generator circuits was also verified through the variation of  $R1$  (for amplitude control) and  $R2$  (for frequency control) using external resistance at their accessible terminals (I/O pads) to form composite variable  $R1$  and  $R2$  elements. Although circuit techniques employed in this ELF oscillator design result in primarily square waveforms for bio-medical and other applications, other wave-shapes can be easily derived by using additional circuits for final signal shaping at the oscillator output. As mentioned in the introduction section

such additional wave shaping circuits does not affect the signal regeneration and frequency control novelty of the core ELF oscillator circuit being presented in this chapter. The voltage across the capacitor  $C$ ,  $V_C$  yields a pseudo-triangular wave-shape through the back-to-back charging and discharging of the capacitor as indicated in Figure 3.4 and demonstrated in Figure 3.15. Also, employing an OTA-based integrator building block on the square waveform at the  $V_o$  output of the Schmitt Trigger, a triangular wave shape can be created which will be designed in the following chapter. Subsequently, a low distortion sinusoidal ('pseudo-sinusoidal') wave shape can be generated, by removing the higher harmonics through low-pass filtering of this triangular wave shape [52].

A comparison of the two fabricated ELF WFG (design 1 and design 2), with some recently reported literature [76, 86, 104, 106, 107, 116, 118], and the proposed WFG<sub>ING</sub>, based on the integrator relaxation timing network, follows in chapter 4 (Table 4.4). The table provides clear statements on how the proposed two ELF WFGs differ from the previously reported WFG designs, in terms of technology, amplitude, frequency, type of circuit elements [OTA, CCII or other], number and values of the resistors and capacitors, supply voltage, power consumption, and tuning range. The presented design (Figure 3.3) is based on one CMOS differential pair with current mirror load, along with two simple single PMOS inverter amplifiers and three passive elements. As the table indicates, the proposed design utilizes fewer MOSFET devices, uses a lower supply voltage of just  $\pm 1.2V$ , provide extra low frequency with lower power consumptions of only  $691\mu W$  and  $943\mu W$  for the first design and the second design respectively, compared to previously reported WFG designs. It is more compact due to the use of simple gain stages and minimum number of passive components. This also satisfies the six criteria of novelty claimed in Section 3.3.

### 3.9 Conclusion

The design of a novel Schmitt Trigger with its applications for a novel CMOS ultra-low-power ELF WFG, based on an OTA utilizing an RC relaxation timing network, has been presented. A new compact and simple Schmitt Trigger scheme with low transistor account is implemented to reduce supply voltage, power and chip area compared to the reported WFG circuits. The ELF WFG has been designed and

fabricated using 2.5-V devices available in 130-nm IBM CMOS technology with a  $\pm 1.2\text{V}$  voltage supply. Using the same topology, two sets of device dimensions and circuit components are designed and fabricated for comparing relative performance, silicon area and power dissipation. A novel concept of a combination of the different types available of on-chip p+ polysilicon resistors in the 130-nm IBM CMOS process is used to fully implement the large integrated resistors for the first design in order to reduce the effect of PVT, function accurately and provide similar waveforms with a lower value of  $C$  compared to the second design. The core ELF oscillation is achieved for the two designs, being around 3.95Hz and 3.90Hz, with of large capacitor values of 1nF and 64nF, respectively. The two design circuits can also generate MLF, around 100Hz, with small capacitor values of 40pF and 2.3nF respectively, with negligible waveform distortion. The measured amplitude and frequencies, which are close to the simulation, are also provided. The first design is found to provide overall optimal performance compared to the second design, at the expense of higher silicon area (including resistor). The first design (design 1) provides wider amplitude and frequency range for either bias current or resistor based multivibrator control, compared to the second design (design 2), and the first design consumes 691 $\mu\text{W}$ , while the second design consumes 943 $\mu\text{W}$  using the same supply voltage. Furthermore, the first design can be fully implemented on-chip with small capacitor values of only 40pF to generate MLF of 100Hz. Therefore, the first design (design 1) presents an optimal design choice for battery-operated biomedical devices.

In fact, sub-low frequency WFG, based on oscillators with a wide tuning range, along with low-power consumption, is the most challenging circuit design. Thus the proposed ELF WFG circuit designs are state-of-the-art that provide a new implementation of ELF, low-power and low cost analog CMOS waveform circuits for battery-operated biomedical devices. This ELF WFG is published in [193]. The published manuscript is included in the ‘Appendices’ section of this thesis. The fully implemented on-chip first ELF WFG design (design 1) will not be implemented with the FD circuit. Only the proposed WFG<sub>INT</sub> based on the same Schmitt Trigger topology, utilizing an integrator relaxation timing network with the novel hybrid tuning technique will be fully implemented. The design, analysis and fabrication of the WFG<sub>INT</sub> based on integrator relaxation timing network will be presented in the chapter 4.

## Chapter 4

# Design Criteria, Implementation and Fabrication of Dual-Band CMOS Waveform Generator With Ultra-Wide Low-Frequency Tuning Range

### 4.1 Introduction

The fully integrated square WFG has an essential role in a low power and high accuracy VLSI communication and biomedical system. These systems incorporate signal processing operations that can be realized either in the digital domain, with digital signal processing (DSP) topologies, or in the analog domain, employing analog signal processing (ASP) topologies. Analog WFGs are mainly desired in signal processing systems that are apparently digital, and would require one or more analog WFGs [66]. The analog WFG is the most appropriate for configuring an ultra-low power system, both in long-channel and short-channel CMOS technology. It can be designed for an extensive range of operational frequencies (from below audio frequency to above 100 MHz), setting their oscillation frequency in a well-defined mode, operated with low power consumption and consuming a small silicon area [52]. A low power WFG, that generates stimulus output of low frequency electrical pulse signals with electronically controlled amplitude and frequency, is important in signal processing systems, particularly for battery-operated biomedical devices, enabling the reduction of the overall system cost [3]. The CMOS technology scaling greatly complicates the design of a wide tuning range WFG circuit. Actually, the use of small channel length technology results in a lower supply voltage, which limits the tuning control voltage and hence the required achievable tuning range. The main target of this work is to develop a novel, low power fully on-chip CMOS dual-band square/triangular WFG, with ultra-wide low frequency tuning-range for electro therapy devices. The circuit consists of an electronically tuneable WFG<sub>INT</sub> based on a gm-C integrator building block, along with frequency divider (FD) stages, using cascading multiple divide-by-two ( $f/2$ ) circuits in series with dual 8-1 multiplexers (MUXs) and a path selector (PS) output for driving an electrode from 16 selectable channels as shown Figure 4.1, in order to realize two mode

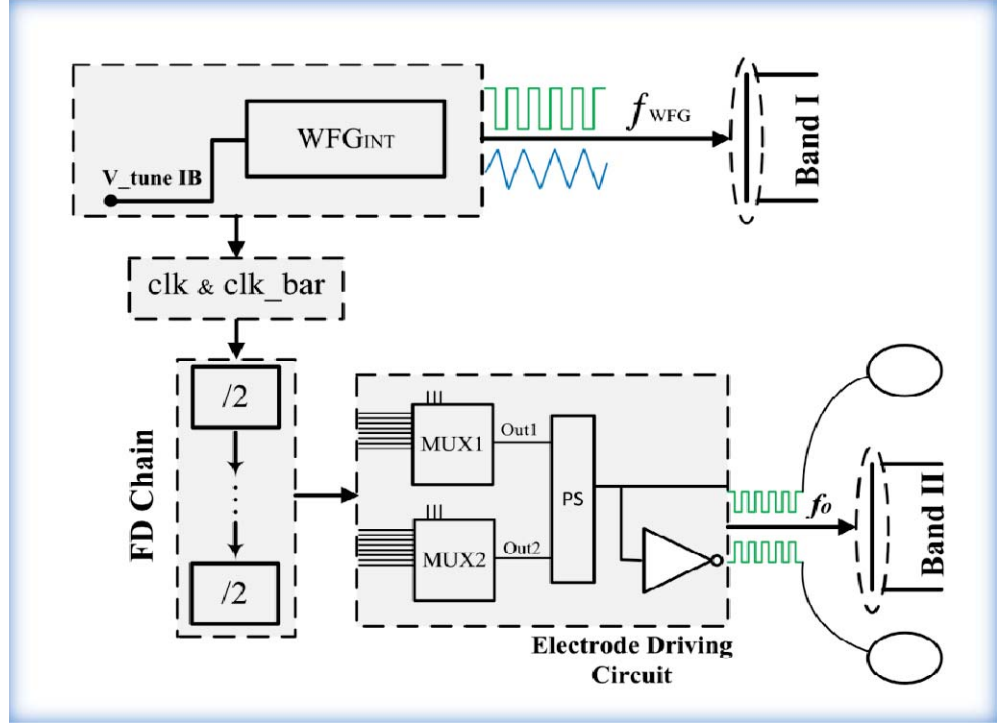


Figure 4.1. Block diagram of the proposed mixed-signal CMOS waveform generator. Oscillation frequency of WFG core circuit is  $f_{WFG}$  (band I) and the digitally channelized selectable output frequency is  $f_o$  (band II).

wideband oscillations that satisfy the minimal requirements for biomedical devices, without being over designed. The new low power 130 nm CMOS technology with low supply voltages is used in the proposed power-efficient WFG<sub>INT</sub> and FD systems. CMOS devices with high performance have continued the dominant technology for ideal analog and digital design. Scaled CMOS allows a high integration level for multiple functions on a single die. Digital circuits can be minimized so that the same function is implemented in a much smaller silicon area, when they utilize a technology with advanced feature sizes. This substantially reduces the die and cost-per-function of digital systems, and hence, in addition to the low power, area scaling is another key factor for low cost. However, utilizing the digital mode results in extra power and chip area consumption; system level performance and power dissipation can be predicted by modelling the behaviour of individual MOSFET transistors. Also using an appropriate CMOS technology advance can contribute to the total silicon area of the circuit; and using an advanced 130nm CMOS technology which has a low power characteristic, and a variety of device feature sizes for different power requirements. This technology

provides various  $V_{TH}$  voltage devices, high  $V_{TH}$  and low  $V_{TH}$ , that can be used to achieve various functions with different supply voltages. The total power consumption of the designed circuit can then be reduced by careful selection of threshold voltage ( $V_{TH}$ ), hence, supply voltage and MOSFET device sizes. The art of low frequency, low-power and small chip area design without compromising the performance of the system requires an appropriate architectural system; optimal topology with a good selection of technology devices and layout circuits are then needed to implement various functions in the architecture. If the circuit is defined, the right trade-offs, device dimensions, gain and speed, can be used to enhance the operation of the circuit.

The outline of this chapter is as follows: first of all, the design criteria of a novel CMOS dual-band WFG<sub>INT</sub> will be presented in section (4.2). The circuit design, topology and operation of the WFG<sub>INT</sub> for the desired performance will be presented in section (4.3). The design of a hybrid frequency tuning system composed of analog and digital models that is compatible with the applications requirements of this research project will be described in section (4.4). Simulation and performance analyses of the analog WFG<sub>INT</sub> and for the digital model are presented in (4.5) and (4.6) respectively. Section (4.7) provides layout design and fabrication details of the most important active and passive elements for the designed system. Experimental results for the fabricated chip are presented in section 4.8. Section (4.9) presents the optimization flowchart of the system design process. A comparison of the fabricated WFG<sub>INT</sub> with a previous ELF WFG designed in this thesis and with some recently reported literature, is presented in section 4.10. Chapter 4 concludes with section 4.11.

## 4.2 Design Criteria of CMOS Dual-Band WFG<sub>INT</sub>

A novel mixed-signal low power dual band WFG<sub>INT</sub> with wide frequency range is presented. It is based on a relaxation oscillator comprising a hysteresis Schmitt Trigger and an integrator timing network circuit along with FD using cascading multiple divide-by-two ( $f/2$ ) circuits. Using an active gm-C integrator as relaxation timing network has the advantage that its  $gm$  can be controlled directly by the biasing current. Also, it can be implemented using small  $gm$  values to provide low frequency oscillation and optimize its parameters, including DC gain, output swing, linearity and other performance parameters. This type of WFG<sub>INT</sub> circuit is preferred for tuneable, low-



power, low-cost, miniaturized single-chip design with high functionality. WFG<sub>INT</sub> circuit based OTAs can be designed to achieve a wide tuning range with practical area and power constraints. Low frequency oscillators (several kHz to < Hz) have distinctive design challenges [194], while having many interesting applications in biomedical and geophysical systems [195, 196]. Although many reported designs achieve low power consumption with a narrow frequency tuning range, many complex applications require a wide frequency tuning range, along with compensation for PVT fluctuations.

The WFG<sub>INT</sub> circuit in this research project is designed to oscillate with no input, generating a periodical low frequency square/triangular waveform signal, and maintaining infinite output. The WFG<sub>INT</sub> circuit toggles spontaneously between two quasi-stable states  $V_{sat+}$  and  $V_{sat-}$ , remaining in its quasi-stable state for a fixed interval of time, and then returns to its original stable state. No external trigger signal is required to yield the changes in the state; it is a free-running oscillator circuit. An internal trigger signal is characterized by the charging and discharging of a capacitor, producing the required internal trigger signal which drives the circuit to return to its original stable state. The component values of the gm-C integrator are designed and used to set the time constant for which the circuit remains in each state. Since  $gm$  of the integrator circuit can be controlled directly by the DC biasing current, tuning of the oscillation frequency of the WFG<sub>INT</sub> core with simple tuning circuitry can then be realized easily. It is a simple and compact structure, considered as a power-efficient and small chip area solution with low cost for the longer battery life biomedical device, compared with a number of other architectures.

As a general design requirement, and since the power dissipation of the designed digital circuit is dominated by the FD circuit which has an inherently power hungry nature, the low-power design goal of the FD circuit becomes the task of minimizing, while also remembering the precise functionality and identifying the trade-offs of such minimizations in terms of performance and area. The optimal FD architectures and size are dependent upon the particular D-FF topology and its operating condition. As previously mentioned (section 2.8.2), Master-Slave D-FF (TGMS) are more popular and simpler than other D-FF topologies; their advantages include small chip area occupation and low power dissipation, thus TGMS can be effectively implemented in power-efficient microchips. In practical designs and for dependable results, an appropriate sizing is required. Since the target design of this project is a

portable device for biomedical applications, power consumption and chip area are the major concerns in this design. Hence, the FD circuit design with small chip area and low power consumption can be based on TGMS, with the advances of CMOS technology that enables scaling down of MOSFET transistors in their size, for use in a low-cost CMOS digital circuit. When targeting a compact and extra power-efficient realization with good performance contribution, it is valuable, at least to some extent, to design a simple and suitable circuit solution based technique. An appropriate technique used to reduce the overall power consumption in this research project is through selecting 130-nm CMOS technology, using low supply voltage and low frequency operations with minimum device size and account circuit design, can enhance the low power design for life time battery operated biomedical devices. The present movement in this work is to:

1. Scale down the circuit size by using an appropriate 130-nm CMOS technology, with appropriate increase in the performance of the device.
2. Realize a low frequencies timing network by implementing a first order gm-C integrator approach, utilizing a single stage OTA as an active building block, implemented with a low transistor account; only four transistors and one grounded capacitor to reduce supply voltage, power and chip area. Design a gm-C integrator with small  $gm$  and small MIM capacitor of only 10pF, to eliminate the need for large resistors and capacitor values, hence, implement the WFG<sub>INT</sub> circuit fully on chip, with a small silicon area; since a large capacitor is needed for low frequency WFG design, the size and cost of the implant are impacted considerably by these reasonably large capacitances. A prevailing advantage of gm-C technique is that its  $gm$  can be designed for low frequency applications and can also be controlled directly by the biasing current to provide a wide frequency tuning range.
3. Design an appropriate and novel frequency tuning technique using a hybrid tuning system composed of an analog model and a digital model, so a sufficiently wide frequency output range is obtained, to compensate for PVT variations and to cover the required application bandwidth.
  - a) Analog model, comprising a first order electronically adjustable gm-C integrator using a mathematical model to design its  $gm$  parameters to perform three tasks; (1) the timing network, (2) for low frequency design, and (3) for the electronically tuneable WFG<sub>INT</sub> circuit (band I), linearly controlled by the bias current of the gm-C

integrator through a smart and simple tuning gate-voltage ( $V_{\text{tune}}$ ) that is driven by a single NMOS current source, without requiring an extra complex and complicated circuit. A large frequency tuning range with good linearity of gm-C integrator can then be achieved with small power consumption, using a small DC drain biasing current and a small  $W/L$  ratio, to the frequency scale of the gm-C integrator. This is also promising to provide a sub-frequencies output signal.

- b) Digital model, comprising a FD which provides biphasic square waveform signals with its complementary signal, for better driving the electrode from 16 selected channels for electro-medical devices.
4. Design the device sizes and biasing currents of the  $\text{WFG}_{\text{INT}}$  (including resistors and the capacitor) as well as the FD circuit to meet certain design requirements, including low speed, low power, and large output swing with small silicon area. Principally, to minimize power and silicon area consumption of the  $\text{WFG}_{\text{INT}}$ , low biasing currents and minimum size devices are used, while the digital model is designed to operate at lower power dissipation by using the “ratioed” technique, which scales down the value of  $W/L$  of each device. The silicon area of the CMOS logic gate is also scaled down by simply modifying the  $W$  of the NMOS and PMOS transistors, without degrading the performance of the logic circuit.
  5. A simple current mirror configuration is used for the  $\text{WFG}_{\text{INT}}$  to provide multiple bias current, so as to reduce power consumption and silicon area.

### 4.3 Circuit Design and Topology of The $\text{WFG}_{\text{INT}}$

The core oscillator circuit generates a bi-phase square/triangular waveform source signal. The overall implementation includes a tuneable  $\text{WFG}_{\text{INT}}$ , clock (clk) and clk\_bar translations, along with 16 stage divide-by/2 frequency divider (FD) in series with dual 8-1 MUXs and a PS. The PS output can drive electrodes for electro-medical device, using the chosen frequency.

#### 4.3.1 $\text{WFG}_{\text{INT}}$ Circuit Design

A novel current-controlled  $\text{WFG}_{\text{INT}}$  utilizing OTAs is presented. The schematic of the proposed  $\text{WFG}_{\text{INT}}$  with clk and clk\_bar circuit is shown in Figure 4.2. Its operation is characterized by a positive feedback hysteresis Schmitt Trigger along with



NMOS differential input pair M1, M2 along with a PMOS active current mirror load M3, M4. It is followed by two simple PMOS common source M5 and M6 (inverter amplifier) gain stages (STG2) and (STG3) respectively. STG1, STG2, STG3 along with resistor  $R$  are configured as voltage amplifier which are connected in positive feedback to form a hysteresis Schmitt Trigger that determines the amplitude of the generated square waveform signal (the saturation output). A simple current mirror configuration employs an NMOS M11, M12, and M13 is used to provide multiple bias current for STG1 and STG2, respectively, from one reference current ( $I_{Ref}$ ). An NMOS (M14)-based voltage controlled bias current of STG3 is also realized to control the amplitude of the circuit.

#### 4.3.3 Gm-C Integrator Realization

The tran-sconductor is an essential active building block in a timing network based on a gm-C integrator, and the complete performance of the gm-C integrator, including the integrator frequency response, linearity, and power consumption, is determined by the designed parameters of the tran-sconductor. Due to the low supply voltage in today's nm CMOS technologies adopted in this work, combined with the wide tuning range, small chip area and low power consumption target, the integrator of this WFG<sub>INT</sub> is a simple first order gm-C integrator building block (STG4). A simplified schematic view of the gm-C integrator circuit, its symbols and building block diagram is shown in Figure 4.3 (a) (b) and (c) respectively.

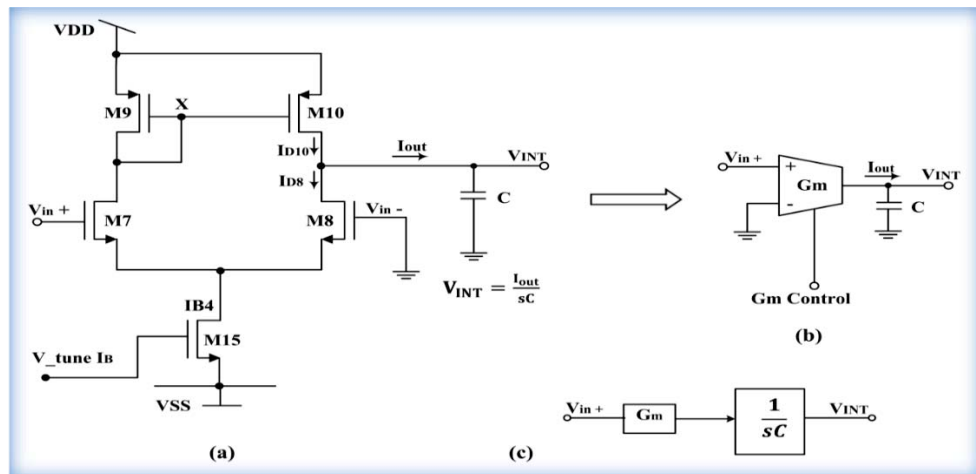


Figure 4.3. A single stage gm-C integrator based on CMOS OTA, (a) circuit implementation, (b) integrator symbol and (c) building blocks diagram.

It is implemented using a simple single-stage open loop tran-sconductor as an active building block, with only four transistors and one grounded capacitor, which has been used as the timing network as well as for the electronically tuneable WFG<sub>INT</sub> circuit. This tran-sconductor is implemented using an identical NMOS differential input pair M7, M8 along with a P-MOS active current mirror load M9, M10 that converts a differential input to a single ended output. The integrator circuit forms a relaxation timing network, in a negative feed-back loop to the inverting terminal of STG1 in Schmitt Trigger, and controls the frequency of the WFG<sub>INT</sub> at the output. One NMOS (M15)-based voltage-controlled DC bias current is designed to electronically control the oscillation frequency of the circuit using the wide range of variation of the  $gm$ . Since the parameters of the gm-C integrator can be controlled, a wide frequency tuning range can then be achieved by tuning the  $gm$  of the integrator that is driven by the M15 current source without requiring an extra complex and complicated circuit.

It is obvious that the designed gm-C circuit is more desirable for low power consumption. In gm-C integrator implementations, minimum stages are mainly beneficial in terms of complexity, noise, and power consumption; hence, it is important to consider the practicality of the integrator realization, as well as the performance requirements for the integrator building block, before deciding on the integrator archetype. A single ended CM OTA topology was implemented for this gm-C circuit which designed to offers the desired characteristics of high output impedance, wide bandwidth, high slew-rate and low power consumption. A high output impedance can enhance the gain of the circuit, and hence, reasonable gain can be achieved. In addition, high output impedance is usually associated with a low frequency pole that can enhance low frequency integrator design. Furthermore, controlling the parameters of the tran-sconductor, which can control its  $gm$  over a wide range of bias current, with a range of linearity, promotes gm-C integrator design. The most important aspect in the design of the gm-C integrator is the transconductance, which can be designed for low frequency applications.

The transfer function of the gm-C integrator in Figure 4.3 can be realized using a two-path analysis. The frequency behaviour of a differential pair with active current mirror is rather complex, as there are two different signal paths in parallel, with different transfer functions. The first path can be realized from M7 to the output through M8; contributes one pole  $\omega_{p1}$ , its transfer function  $H(s)$  can be given by,

$$H(s) = \frac{A_v}{1 + \frac{s}{\omega_{p1}}} \quad (4.1)$$

The second signal path can be realized from M7 to the output through current mirror M9 and M10, and contributes a mirror pole  $\omega_{p2}$  at node X of the circuit. Its transfer function can be given by,

$$H(s) = \frac{A_v}{\left(1 + \frac{s}{\omega_{p1}}\right)\left(1 + \frac{s}{\omega_{p2}}\right)} \quad (4.2)$$

The overall transfer function  $[Ho(s)]$  of the gm-C integrator can be then given by,

$$Ho(s) = \frac{A_v}{1 + \frac{s}{\omega_{p1}}} \left( \frac{1}{1 + \frac{s}{\omega_{p2}}} + 1 \right) \quad (4.3)$$

$$= \frac{A_v \left( 2 + \frac{s}{\omega_{p2}} \right)}{\left( 1 + \frac{s}{\omega_{p1}} \right) \left( 1 + \frac{s}{\omega_{p2}} \right)} \quad (4.4)$$

Where  $A_v = gm_{7,8} \cdot (r_{o8} // r_{o10})$  is the open loop DC-gain. The first pole  $\omega_{p1}$  at  $-3dB$  frequency is the dominant pole and is determined by the output resistance ( $r_{o8} // r_{o10}$ ) and the load capacitor  $C$ . The first pole can be then given by,

$$\omega_{p1} = \frac{1}{(r_{o8} // r_{o10}) C} \quad (4.5)$$

The second pole is a non-dominant mirror pole  $\omega_{p2}$  is determined by the  $gm_9$  and the sum of the gate-source capacitance of M9, and M10. The second pole can be given by,

$$\omega_{p2} = \frac{gm_9}{C_X} \quad (4.6)$$

So, the overall transfer function can be then given by,



$$Ho(s) = \frac{gm_{7,8} \cdot (r_{o8} // r_{o10}) \cdot \left(2 + \frac{sC_X}{gm_9}\right)}{(1 + sC(r_{o8} // r_{o10})) \cdot \left(1 + \frac{sC_X}{gm_9}\right)} \quad (4.7)$$

Where  $C_X$  is the total capacitance at X is the total capacitance at the drain node of M7 to ground, which includes  $C_{GS9}$ ,  $C_{GS10}$ ,  $C_{DB9}$ ,  $C_{DB7}$  and the Miller effect of  $C_{GD7}$  and  $C_{GD10}$ . For an identical PMOS  $C_{GS9} = C_{GS10}$ , while  $C_{DB9}$ ,  $C_{DB7}$ ,  $C_{GD7}$  and  $C_{GD10}$  are considered small and can be neglected,  $C_X = 2C_{GS9}$ . However, at low frequencies, the overall transfer function can be then given by,

$$Ho(s) = \frac{2gm_{7,8}}{sC} \quad (4.8)$$

Putting  $s=j\omega$ , the unity gain frequency,  $(\omega_c)$  can be given by,

$$\omega_c = \frac{2gm_{7,8}}{C} \quad (4.9)$$

With the corresponding time-constant of,

$$\tau = \frac{C}{2gm_{7,8}} \quad (4.10)$$

Equation (4.10) shows that the time-constant of the integrator is proportional to  $C$  and inversely proportional to  $gm_{7,8}$ . For a large time constant, a large capacitor is required. An active gm-C integrator can be implemented in CMOS process technology to operate at very low frequencies, thus implying very low  $gm_{7,8}$  values without the need for large capacitor values. The unity gain frequency  $f_c$  of the single pole gm-C integrator can be given by,

$$f_c = \frac{gm_{7,8}}{\pi C} \quad (4.11)$$

Equation (4.11) shows that the frequency of the integrator goes down as  $gm_{7,8}$  decreases

and  $C$  increases. By substituting  $gm_{7,8}$  value into (4.11) a proportionality can be then established between  $IB4$  and the integrator frequency which is given by,

$$f_c = \frac{\sqrt{\mu_n C_{ox}}}{\pi} \cdot \frac{1}{C} \sqrt{\frac{W_{7,8} I_{B4}}{L_{7,8}}} \quad (4.12)$$

$$f_c \propto \frac{\sqrt{W_{7,8}}}{C} \sqrt{\frac{I_{B4}}{L_{7,8}}} \quad (4.13)$$

Thus  $gm_{7,8}$  or specifically,  $W_{7,8}$ ,  $L_{7,8}$ ,  $IB4$  and  $C$ , will be the design parameters in the integrator relaxation timing network. A wide range of frequency tuning can thus be achieved by tuning the  $gm_{7,8}$  of the integrator using  $IB4$ . It also provides an avenue to compensate the PVT variation.

#### 4.3.4 WFG<sub>INT</sub> Circuit Operation

Figure 4.4 (a) and (b) shows the transfer characteristic of the hysteretic Schmitt-Trigger with respect to the integrator relaxation timing network and the input output waveforms.

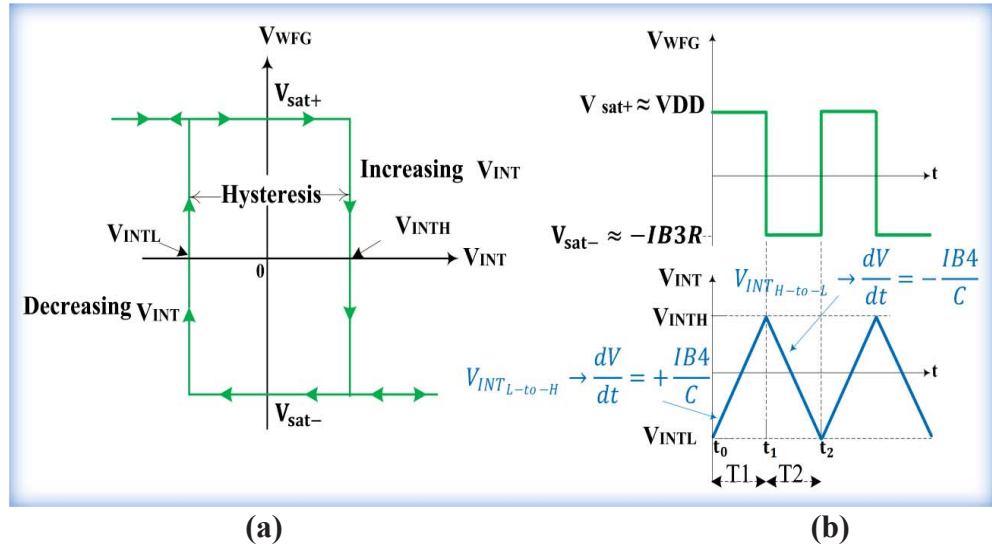


Figure 4.4. Schematic diagram of the WFG<sub>INT</sub> circuit operation, (a) transfer characteristic of the Schmitt trigger design, and (b) the square and triangular waveforms of the designed WFG<sub>INT</sub> circuit.

The circuit toggles between two quasi-stable states  $V_{sat+}$  and  $V_{sat-}$  in a free-running oscillation mode through regenerative feedback. The charging and discharging of the gm-C integrator's capacitor produces the trigger voltage  $V_{INT}$  to toggle the circuit between these two states. The component values as per (4.10) sets the state transition periods. The ramp output voltage  $V_{INT}$  is an integration (temporal-accumulation) of the output voltage  $V_{WFG}$ . The Schmitt Trigger switches to its saturated high positive level  $V_{sat+}$  when  $V_{INT}$  dips below its saturated low negative level  $V_{INTL}$  and remains in that state until  $V_{INT}$  exceeds its saturated high positive level  $V_{INTH}$ , at which point it switches to the saturated low negative level  $V_{sat-}$ . It remains in that state until  $V_{INT}$  once again exceeds  $V_{INTL}$ , so that,

$$V_{WFG}(V_{INT}) = \begin{cases} V_{sat+} & \text{if } V_{INT} \leq V_{INTL} \\ V_{sat-} & \text{if } V_{INT} \geq V_{INTH} \end{cases} \quad (4.14)$$

The Schmitt Trigger output  $V_{WFG}$  is a square waveform signal, while the integrator output  $V_{INT}$  is a triangular waveform. The characteristic of the designed first order nonlinear oscillator system based on the gm-C integrator can be given by,

$$C \frac{dV_{INT}}{dt} + V_{WFG}(V_{INT}) \cdot gm_{7,8} = 0 \quad (4.15)$$

The circuit operation is based on the differential pair switching voltages. The OTA operates as a linear amplifier with positive feedback during switching from one quasi-stable state to another. The operation of the circuit can be described by considering the two liner regions  $V_{INT} \leq V_{INTL}$  and  $V_{INT} \geq V_{INTH}$  of the triangular waveform which consists of two integration interval  $T1$  ( $t_1-t_0$ ) and  $T2$  ( $t_2-t_1$ ). Suppose initially, the output  $V_{WFG}$  at  $t=0$  is at  $V_{sat+}$  at the integrator input, and is integrated for a fixed period of time  $T1$ , then the integrator's output  $V_{INT}$  starting from its low negative level increases linearly with a constant positive slope given by  $IB4/C$  towards its high positive level. The non-inverting terminal at gate of M1 ( $V_{in1+}$ ) is also held at  $V_{sat+}$ . The capacitor  $C$  is initially discharged and the gate potential  $V_{in2-}$  of M2 in STG1 of the Schmitt Trigger is at its minimum low level  $V_{INTL}$ . It is assumed that the input is a positive rising triangular (ramp) waveform from low to high  $V_{INT \text{ L-to-H}}$ , while the gate potential  $V_{in1+}$  of M1 remains at its maximum positive level. With the difference between  $V_{in1+}$  and  $V_{in2-}$

sufficiently large, M1 conducts most of the bias current  $IB1$ , so that M2 is off, driving M4 into a deep triode region with zero current, and the output voltage of the OTA in STG1 is then equal to  $VDD$ . With M4 in deep triode, the gate of PMOS M5 is then at high potential and almost turned off, resulting in the bias current  $IB2$  becoming a constant charging current contributing electrons to the gate of M6 and bringing its potential down near the negative supply voltage. M6 is thus acting as a switch operating in the deep triode region, resulting in the maximum output voltage ( $V_{sat+}$ ) being near the positive supply voltage  $VDD$ . The drain current  $iM6_{L-to-H}$  of the switch M6 is then the sum of the bias current  $IB3$  gate pull-up current of M7 (supplying holes to gate of M7) and the current through resistor  $R$ . The  $V_{sat+}$  also causes M7 to absorb a large part of the bias current  $IB4$ . The output current of the integrator (mirrored by M9 and M10),  $I_{OINT} \approx IB4$  is then integrated by the  $C$  for rising from  $V_{INTL}$  to  $V_{INTH}$ . This causes the output of the integrator to linearly increase with a slope of  $+IB4/C$ , providing a positive linear ramp voltage  $V_{INTL-to-H}$  at the inverting input terminal  $V_{in2-}$  of M2.

The current charging  $C$  is constant and independent of the input level, thus the output level  $V_{WFG}$  remains constant. But as  $V_{INT}$  rises, the difference between  $V_{in1+}$  and  $V_{in2-}$  in STG1 reduces, and M2 turns on, drawing part of  $IB1$ . Eventually  $V_{INT}$  is saturated at its high positive level,  $V_{INTH}$  causing the square waveform voltage  $V_{WFG}$  to switch state (through positive feed-back) and saturate at its low negative level  $V_{sat-}$ . AT  $t = T1$ , the negative half-cycle of the output (period T2) begins with  $V_{WFG}$  at  $V_{sat-}$  and  $V_{INT}$  at  $V_{INTH}$ . Also,  $C$  is fully charged and the gate potential  $V_{in2-}$  of M2 has its maximum positive level, with M2 conducting most of the bias current  $IB1$ . Therefore, most of  $IB1$  becomes a charging current bringing the gate of M5 lower, towards the negative supply voltage by supplying electrons to the gate. As a consequence, M5 is behaving almost as a closed switch, resulting in the gate of M6 being near the positive supply. Now, with M6 almost off, the continuity of the bias current  $IB3$  requires that a large (significant) part of it will now flow through the resistor  $R$ . Consequently, the minimum output voltage  $V_{sat-}$  achieved by the circuit can then be given approximately by  $-IB3R$ . With the output of the Schmitt Trigger saturated at low negative level,  $V_{sat-}$ , the integrator discharges  $C$  by a current  $-IB4$ , lowering  $V_{INT}$  from  $V_{INTH}$  towards  $V_{INTL}$ . This causes the output of the integrator to linearly decrease, with a slope of  $-IB4/C$ , providing a negative linear ramp voltage  $V_{INTH-to-L}$  at  $V_{in2-}$ . As  $V_{INT}$  voltage decreases, the gate potential  $V_{in2-}$  eventually approaches the gate potential  $V_{in1+}$ , M1

turns on, drawing part of  $IB1$ . The  $V_{WFG}$  remains negative until  $V_{INT}$  reaches its low negative values  $V_{INTL}$ . Eventually, switching at the output takes place and  $V_{WFG}$  becomes  $V_{sat+}$  again. The circuit then returns to its previous pseudo-stable state, starts a new cycle and generates the periodical waveform.

Based on the above description, mathematical analysis can be applied to derive a design equation relating circuit controllable variables including oscillator parameters such as the period ( $T$ ), and the frequency ( $f$ ) of the generated output waveform. The voltage at the integrator output  $V_{INT}$  at any time ( $t$ ) is the initial capacitor voltage plus the integral of the input signal for the transition period. The time expression for the output voltage  $V_{INT}(t)$  in the charging and discharging periods can be given by,

$$V_{INT}(t) = \begin{cases} V_{INT}(t_0) + \frac{IB4}{C}(t_1 - t_0) \\ V_{INT}(t_1) - \frac{IB4}{C}(t_2 - t_1) \end{cases} \quad (4.16)$$

For the positive half cycle ( $T1$ ),  $V_{INT}$  is increased linearly from low-to-high,  $V_{INTL-to-H}(t)$  from time  $t=0+$  can be given by,

$$V_{INTL-to-H} = \frac{V_{INTH} - (-V_{INTL})}{T1} = \frac{IB4}{C} \quad (4.17)$$

Rearranging equation (4.17), the time period  $T1$  is given by,

$$T1 = \frac{C (V_{INTH} + V_{INTL})}{IB4} \quad (4.18)$$

For the negative half cycle ( $T2$ ),  $V_{INT}$  decreasing linearly from high-to-low  $V_{INTH-to-L}(t)$ , from time  $T1$ , can be given by,

$$V_{INTH-to-L} = \frac{-V_{INTL} - V_{INTH}}{T2} = -\frac{IB4}{C} \quad (4.19)$$

So,

$$T2 = \frac{C (V_{INTH} + V_{INTL})}{IB4} \quad (4.20)$$

Then the overall period ( $T$ ) is easily derived to be,

$$T = \frac{2C(V_{INTH}+V_{INTL})}{IB4} \quad (4.21)$$

Where the values of  $-V_{INTL}$  and  $+V_{INTH}$  can be given as in equations (3.18) and (3.34) since the same Schmitt Trigger circuit topology is used, as follows:

$$-V_{INTL} = -|VSS| + V_{DS12} + V_{GS2L-to-H} \quad (4.22)$$

So,

$$-V_{INTL} = -|VSS| + \sqrt{\frac{2IB1}{\mu_n C_{ox} \frac{W_{12}}{L_{12}}}} + \sqrt{\frac{0.2IB1}{\mu_n C_{ox} \frac{W_2}{L_2}}} + V_{THN} \quad (4.23)$$

And,

$$V_{INTH} = -|VSS| + V_{GS2H-to-L}(0+) + V_{OD12} \quad (4.24)$$

So,

$$V_{INTH} = -|VSS| + \frac{0.9IB1}{\mu_n C_{ox} \frac{W_2}{L_2} [V_{D2H-to-L}(0+) + |VSS| - V_{OD12}]} + V_{THN} + V_{OD12} \quad (4.25)$$

The overall frequency of the waveform can be given by,

$$f_{WFG} = \frac{IB4}{2C (V_{INTH}+V_{INTL})} \quad (4.26)$$

Equation (4.26) shows that the oscillation frequency of the designed WFG<sub>INT</sub> is proportional to the bias current  $IB4$  of the gm-C integrator and inversely proportional to the timing capacitor, as well as the integrator output swing and hence, the frequency can be electronically tuned by adjusting  $IB4$ .

#### 4.3.5 Components Sizing for Low Power & Low Frequency WFG<sub>INT</sub> Design

For an appropriate low frequency design and to reduce power consumption and optimizes silicon area, it is important to analyse the controllable parameters.

Considering the differential pair M1, M2 in STG1 having the same small signal parameters,  $gm_1 = gm_2$  and  $r_o$  being the output resistance, the loop gain of the core oscillator can be given by,

$$A_v^+ = gm_{1,2} \cdot r_{o2} // r_{o4} \cdot gm_5 \cdot r_{o5} \cdot gm_6 \cdot r_{o6} // R \quad (4.27)$$

Where,  $gm_1$ ,  $gm_2$ ,  $gm_5$  and  $gm_6$  are the trans-conductance of M1, M2, M5 and M6 in the linear amplification range. By substituting the expressions for  $gm$  and  $r_o$ , in equations (3.2) and (3.3) respectively, and  $\lambda \propto (1/L)$ , then the proportionality can be determined between loop gain  $A_v^+$ , the controllable variable ( $W/L$ ) and the drain current ( $I_D$ ) which can be then given by,

$$A_v^+ \propto \sqrt{\frac{W_{1,2} \cdot L_{1,2}}{I_{D1,2}}} \cdot \sqrt{\frac{W_5 \cdot L_5}{I_{D5}}} \cdot \sqrt{\frac{W_6 \cdot (\frac{L_6 \cdot R}{L_6 + R})}{I_{D6}}} \quad (4.28)$$

Since  $A_v^+ \propto (\sqrt{W \cdot L}) / \sqrt{I_D}$ , equation (4.28) shows that the open-loop gain goes up by increasing the square root of  $W \times L$ , and also by reducing the drain current  $I_D$ . Using small DC drain bias current also significantly improves power consumption. Hence bias current sources M12, M13 and M14 are designed to have very high output impedance  $r_{oN}$ , and in relation to this design, the values for L12, L13 and L14 should be made 2 times longer than the minimum length. The maximum output swing for the circuit, being near the positive supply voltage ( $V_{sat+} = VDD$ ), is limited by M6 going into the triode region, being ON as switch with very small drain-to-source drop. M6 thus requires a very small  $R_{DS(ON)}$  using a reasonably wide PMOS device. The minimum output value ( $V_{sat-} = -IB3R$ ) is limited by the gate voltage of M14 and the regenerative positive feedback resistor  $R$ . Basically to bring the minimum output value closer to the negative supply voltage, the drain voltage  $V_{D14}$  of M14 may not go below the gate voltage of M14 by more than  $V_{THN}$ , hence,

$$V_{D14} = VSS + V_{GS14} - V_{THN} \quad (4.29)$$

Substituting for  $V_{GS14} - V_{THN}$  gives,



$$V_{D14} = V_{SS} + \sqrt{\frac{2I_{B3}}{\mu_n C_{ox} \frac{W_{14}}{L_{14}}}} \quad (4.30)$$

Hence, to improve the swing, the value of  $V_{GS14}$  must be made small, resulting in large values of  $W_{14}/L_{14}$ . Using an appropriate resistor  $R$  can also enhance the output swing. However, more important in the circuit design are the sizes of M1 and M2 which dominate overall circuit performance. For proper operation of the three stage operational amplifier of the Schmitt Trigger, the gate potential at the inputs  $V_{in1+}$  and  $V_{in2-}$  of STG1 should be within a limited range. If the input voltage goes beyond this range, the operational amplifier gain drops and the WFG<sub>INT</sub> circuit cannot function properly. The maximum input  $V_{G1,2(MAX)}$  is limited by both M1 and M2 going into the triode region, and hence,  $V_{G1,2(MAX)} = V_{DD} - |V_{GS3}| + V_{THN}$ . Substituting for  $V_{GS3}$ , the maximum input for M1 and M2 can be given by,

$$V_{G1,2(MAX)} = V_{DD} - \left[ \sqrt{\frac{I_{B1}}{\mu_n C_{ox} \frac{W_3}{L_3}}} + V_{THP} \right] + V_{THN} \quad (4.31)$$

Where,  $|V_{GS3}|$  is written in terms of its drain current  $I_{D3}=I_{B1}$ . The minimum input voltage  $V_{G1,2(MIN)}$  is limited by M12 driven near the edge of saturation, hence,  $V_{G1,2(MIN)} = V_{SS} + |V_{DS12}| + V_{GS1,2}$ . Since the overdrive  $V_{OD12} \approx V_{DS12}$ ,

$$V_{DS12} \approx V_{OD12} = \sqrt{\frac{2I_{B1}}{\mu_n C_{ox} \frac{W_{12}}{L_{12}}}} - V_{THN} \quad (4.32)$$

So,

$$V_{G1,2(MIN)} = V_{SS} + \sqrt{\frac{2I_{B1}}{\mu_n C_{ox} \frac{W_{12}}{L_{12}}}} + \sqrt{\frac{I_{B1}}{\mu_n C_{ox} \frac{W_{1,2}}{L_{1,2}}}} \quad (4.33)$$

Equations (4.31) and (4.33) show the variables for improving  $V_{G1,2(MAX)}$  and  $V_{G1,2(MIN)}$  of the pair M1, M2 of STG1. To make  $V_{G1,2(MAX)}$  as large as possible,  $I_{B1}$  and  $L_3$  should be made as small as possible, while  $W_3$  is made as large as possible, on the other hand, to

make  $V_{G1,2(MIM)}$  as small as possible,  $L_{12}$ ,  $IB1$ , and  $L_{1,2}$  should be made as small as possible, while increasing  $W_{12}$  and  $W_{1,2}$  as much as possible.

The oscillation frequency of the designed WFG<sub>INT</sub> is set by the time constant of the gm-C integrator. Thus, the design parameter of the gm-C integrator is also important. Since  $f_c \propto (\sqrt{W_{7,8} \cdot I_{B4}}) / (C \sqrt{L_{7,8}})$ , (equation 4.13) hence, for small  $gm_{7,8}$  value design, (assuming small  $C$  value), the  $f_c$  decreases as the  $W_{7,8}$  and DC drain biasing current  $IB4$  reduce, while  $L_{7,8}$  increases. Making  $W_{7,8}$  small is in direct conflict with its open loop gain  $A_v^+ \propto \sqrt{W_{7,8} \cdot L_{7,8}} / \sqrt{I_{D7,8}}$ . Thus  $W_{7,8}$  presents tradeoffs between the gain and the frequency, such that, by increasing the width of the differential input pair M7-M8, although the gain goes up (by the square root of  $W_{7,8}$ ) the frequency is also increased by the square root of  $W_{7,8}$ . If the width  $W_{7,8}$  is narrower, then the  $gm_{7,8}$  and, hence, the frequency are reduced. Therefore, by choosing a reasonable  $W_{7,8}$ , a relatively a long channel length  $L_{7,8}$ , by about 2-5 times the minimum length, the frequency of the designed circuit decreases and the integrator open-loop gain increases. Thus, the trade-off between  $A_v^+$  and,  $f_c$  may be eliminated by controlling the  $C$  value.

The value of  $C$  can be approximately determined from the bandwidth specification in (4.13) by iteratively selecting  $W_{7,8}$ ,  $L_{7,8}$  and  $IB4$  values and solving for  $C$ . A high-impedance node usually has a low frequency pole associated that reduces the speed of the amplifier. Since the frequency response of the integrator will be dominated by the high impedance nodes ( $r_{o8}/r_{o10}$ ) (equation 4.5) and the load capacitor  $C$ , for low frequency integrator design and low capacitor load value, M8 and M10 are assumed to have high output impedance; relative to the impedance, the values for  $L_8$  and  $L_{10}$  should made at least 2 times longer than the minimum length. The  $gm_{7,8}$  value, and hence, the frequency of the circuit can also be reduced by simply reducing the biasing current  $IB4$ . The small current  $IB4$  can also enhance the gm-C DC gain. This result shows that using a small DC basic current, the lowest oscillation frequency value and largest possible voltage gain can be achieved with small capacitor value. Also, using a small DC drain biasing current, a large frequency tuning range with adequate linear range can be achieved, significantly reducing power consumption, as per (2.7). However,  $gm_{7,8}$  will be a design parameter in the WFG<sub>INT</sub> based integrator relaxation timing network much as are resistors and capacitors in a ELF WFG based RC relaxation timing network.

From the above analysis, it can be concluded that for high gain, low speed with reasonably linear output range, trade-offs must be considered, as the designer selects a circuit topology and begins the simulation process of iterating a final design with possible set of  $W$ ,  $L$ ,  $IB$  and  $C$ . Hence, the low frequency  $WFG_{INT}$  can be implemented fully on chip, with significantly reduced power consumption and silicon area.

## 4.4 Frequency Tuning Technique

In this research project a simple and novel hybrid tuning technique, composed of analog and digital models, is used, which is compatible with the application's requirements.

### 4.4.1 Analog Tuning Model

As discussed above, the frequency of the  $WFG_{ING}$  is proportional to the  $IB4$  and inversely proportional to the  $C$ , as per (4.26), which can be tuned by varying either  $IB4$  or the capacitor values. Although the digitally controlled switched-capacitor matrices “varactors” technique can be used, as previously mentioned in section in (2.6.1.2), additional components (extra active and passive elements for implantation) are required. They will be more complicated to design, will produce noise and require large power consumption. It is also necessary to achieve a wide low frequencies tuning range, thus large capacitor values are required, which could consume a large silicon area. Since  $f_{WFG}$  is a function of the differential pair DC biasing current  $IB4$ , the oscillation frequency of the  $WFG_{ING}$  integrator can be controlled independently and modified electronically by adjusting the bias current  $IB4$  of the  $gm$ - $C$  integrator, requiring no extra circuit, and would use low power consumption and occupy a small silicone area.

The tunbility can be significantly enhanced by using a single MOSFET device or even by a bank of MOSFETs, which can be switched in and out for uneven tuning. Utilizing a single MOSFET is preferred for a wide frequency tuning range, leading to minimum power consumption and chip area, which enhances the  $gm$ - $C$  integrator continuous tuning ability. Here an NMOS (M15)-based voltage controlled bias current in Figure 4.3 is used, whose value is controlled by its gate-source-voltage ( $V_{GS15}$ ). The required tuning voltage V-tune is applied using direct DC voltage source. The designed

gm-C integrator has the ability to control the frequency response of the designed WFG<sub>INT</sub> circuit within an appropriate linear tuning range.

The oscillator frequencies of the WFG<sub>INT</sub> core (band I) for fixed  $C$  can then be independently electronically tuneable, by tuning the bias current  $IB_4$  of the OTA in stage four, with low power consumption. If the applications require fixed frequencies, then, roughly, a 2:1 tuning range, with a 2:1 bias current variation, is required to accommodate PVT variation. The tuning is quite easy; this simple gm-C integrator circuit is designed to operate at low frequencies and up to high frequencies, which will be discussed in the simulation results.

#### **4.4.2 Digital Model Implementation**

The overall implementation of the digital block includes a clock (clk) and clk\_bar translations, along with a 16 stage divide-by /2 frequency divider (FD) in series with dual 8-1 MUXs and a PS. The PS output can drive electrodes for electro-medical stimulation using the chosen frequency.

##### **4.4.2.1 Clock and Clock\_Bar**

Two series connected inverters are employed, as shown in Figure 4.2, to generate the complementary rail-to-rail clock (clk) and clock\_bar (clk\_bar) signals required to clock the D-FF.

##### **4.4.2.2 The Frequency Division Circuit**

The FD circuit is implemented by cascading 16 stages of divide-by /2 Flip-Flops. Transmission-gates (TGs) are used to realize master-slave D-Flip-Flops (TGMS D-FF). TGMS are the most popular and simplest among other FF topologies, which can be effectively implemented with a small area of occupation in power-efficient systems. Edge-triggered TGMS D-FFs are implemented using static logic. Static TGMS D-FF is preferred in the design of a low FD circuit, since it can store and preserve its value even if the clock signal is stopped. Although dynamic TGMS D-FF has a lower area, its value is corrupted due to the leakage currents, and works only when the input signal changes often enough[194]; the TGMS D-FF will be always clocked which makes the FF circuit more problematic and would dissipate high power. Dynamic TGMS D-FF is used by the designer only if the small area is the higher priority requirement [135]. However, the

optimal D-FF topology and size is dependent on certain operation conditions. Each TGMS D-FF in this project is realized by a cascade connection of two D-type latches that have opposite clock phases. The two D-type latches are configured based on the cross-coupled inverters having positive feedback. This realization would require fewer transistors, and hence can be more compact than other reported configurations.

However a TG that is composed of N-MOS and P-MOS, in parallel, with complementary signals controlling their gate voltages, is used instead of a single MOSFET pass transistor at the cost of an extra clock signal (section 2.8.2), that is, the complement of the clock. This is because the TG can pass both logic levels well, and hence, has advantages in its rail-to-rail output swing, which improves the performance of the circuit. However, with the advances of 130-nm CMOS technology in scaling down MOSFET transistors in their feature size, for use in low-cost CMOS logic circuits, power consumption and area of occupation of the designed TGMS D-FF circuit can be practically optimized by optimum sizing of these circuits. Hence, the FD circuit can then be effectively implemented in small chip area and power-efficient microchips with high performance. It is more appropriate to direct the design towards the accomplishment of layout and power efficiency in the high density VLSI design.

Figure 4.5 and Figure 4.6 respectively shows the schematic diagram and the implementation of the designed TGMS D-FF for a divide-by/2 FD circuit. The circuit has  $D$  signal inputs with a clock signal, and has a differential output that is denoted  $Q$  and  $\bar{Q}$ . The  $/2$  operation was implemented by connecting the  $\bar{Q}$  output of a TGMS D-FF to its  $D$  input as data input, while  $Q$  output is used as the data output. By “feeding back” the output from  $\bar{Q}$  to the input, the output signal at  $Q$  has a frequency that is exactly one half ( $f/2$ ) that of the input frequency, and hence, the circuit divides the input frequency by a factor of two. The first D-FF is clocked by  $clk$  and  $clk\_bar$  signals, while each following D-FF is clocked by the  $Q$  output of the previous one.

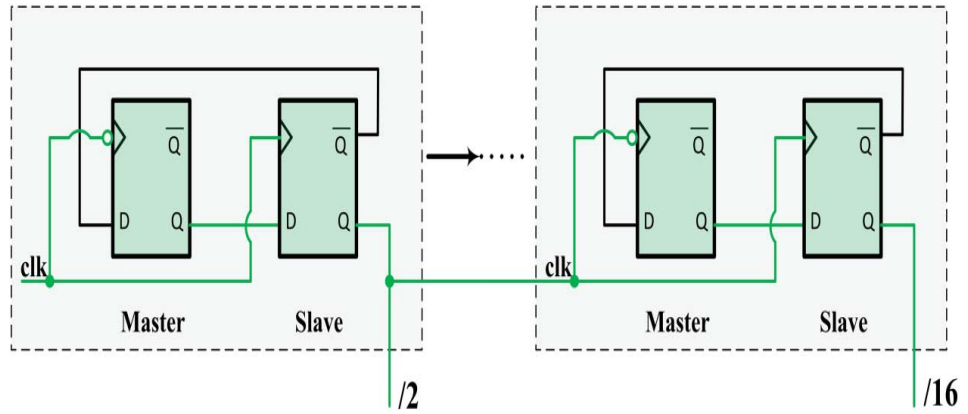


Figure 4.5. The schematic diagram of the designed TGMS D-FF for a divide-by/2 frequency division circuit.

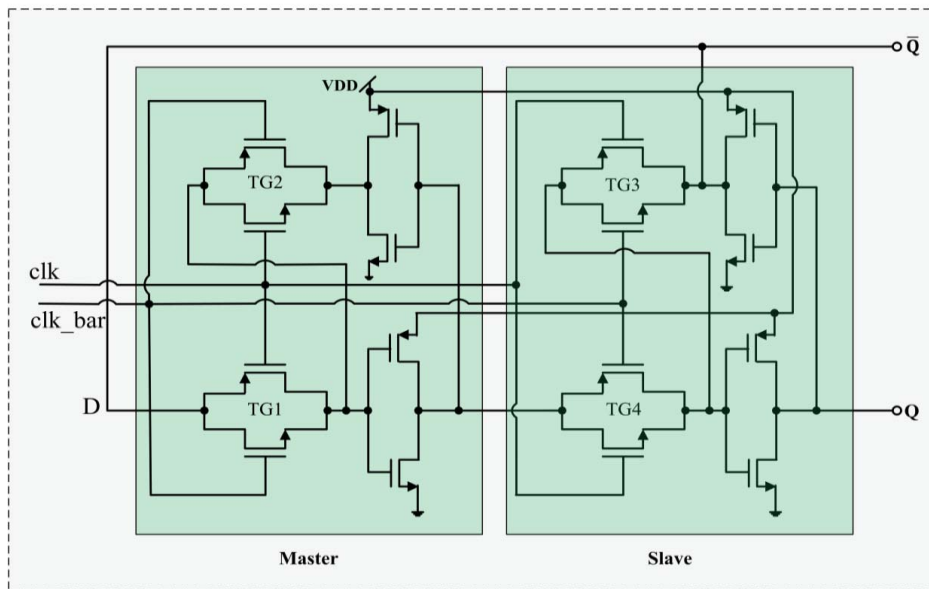


Figure 4.6. The implementation of the designed TGMS D-FF for a divide-by/2 frequency division circuit.

#### 4.4.2.3 Multiplexors And Path Selector

Two 8-to-1 Multiplexors (MUX1 and MUX2) along with a Path Selector (PS) are used to select FD outputs as shown in Figure 4.7.

## 1. Multiplexors

The MUX is implemented using CMOS TG that can pass both logic levels well to improve the performance of the circuit. Two 8-to-1 output Multiplexors (MUX1 and MUX2) are used, with a total of 16 data inputs. 8-to-1 MUX is a combinational logic circuit that has 8 data inputs, and only one output signal. Its function is to select one out of 8 input data sources and transmit selected input signal (data) to a single output line, with the help of control input signals. The routing of the required input to the output is controlled by address inputs, utilizing three simple inverters. All its address inputs (internal clk and clk\_bar) are directly driven using an efficient direct DC voltage, and hence, the desired output can be easily produced. This MUX is bi-directional and can be used as a MUX or a demultiplexer (DEMUX). Logically, the output of MUX1 and MUX2 can be given respectively by,

$$Y_{MUX1} = 1(\bar{S}_1 \cdot \bar{S}_2 \cdot \bar{S}_3) + 2(S_1 \cdot \bar{S}_2 \cdot \bar{S}_3) + 3(\bar{S}_1 \cdot S_2 \cdot \bar{S}_3) + 4(S_1 \cdot S_2 \cdot \bar{S}_3) \\ + 5(\bar{S}_1 \cdot \bar{S}_2 \cdot S_3) + 6(S_1 \cdot \bar{S}_2 \cdot S_3) + 7(\bar{S}_1 \cdot S_2 \cdot S_3) + 8(S_1 \cdot S_2 \cdot S_3) \quad (4.34)$$

$$Y_{MUX2} = 9(\bar{S}_1 \cdot \bar{S}_2 \cdot \bar{S}_3) + 10(S_1 \cdot \bar{S}_2 \cdot \bar{S}_3) + 11(\bar{S}_1 \cdot S_2 \cdot \bar{S}_3) + 12(S_1 \cdot S_2 \cdot \bar{S}_3) \\ + 13(\bar{S}_1 \cdot \bar{S}_2 \cdot S_3) + 14(S_1 \cdot \bar{S}_2 \cdot S_3) + 15(\bar{S}_1 \cdot S_2 \cdot S_3) + 16(S_1 \cdot S_2 \cdot S_3) \quad (4.35)$$

## 2. Path Selector.

A Path Selector (PS) is used to select FD outputs. The PS with two-input design utilizes two TGs. Its address inputs (internal clk and clk\_bar) are directly driven by direct DC voltage, using one inverter. Logically, its output can be given by,

$$V_{OPS} = Y_{MUX1}S + Y_{MUX2}\bar{S} \quad (4.36)$$

When the selector  $S$  is a logic “1”, MUX1 is passed to the output, while a logic “0” on  $S$  passes MUX2 to the output. A simple inverter is used at the output of the PS to realize the out of phase output waveform for driving an electrode. Figure 4.8 shows the complete architecture of the two band on-chip analog model WFG<sub>INT</sub>, based on an integrator building block and the digital model, FD circuit.



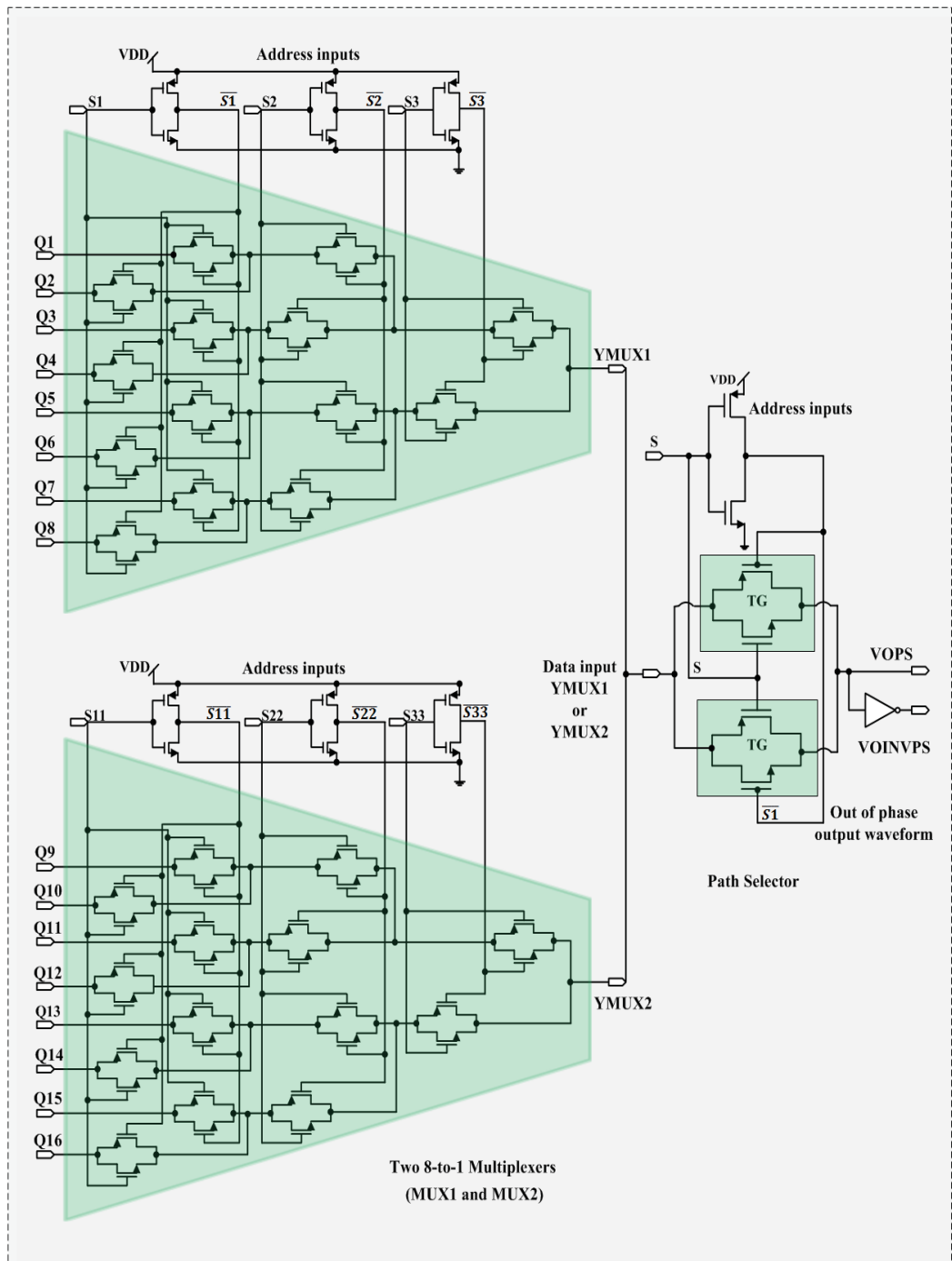


Figure 4.7. Multiplexers and path selector along with output driving circuit.

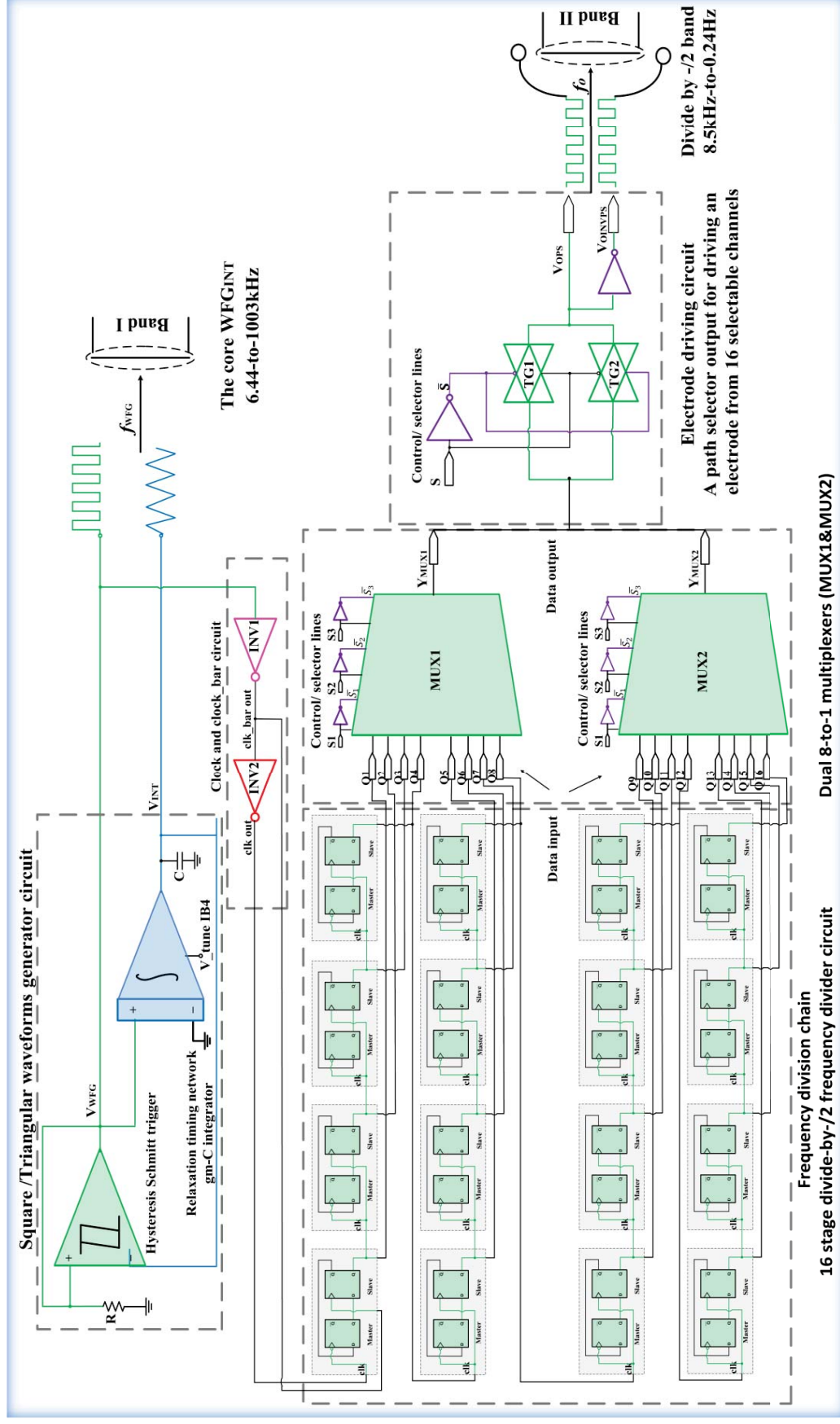


Figure 4.8. The complete architecture of the dual-band 16-channel mixed-signal WFGING with ultra-wide low frequency tuning range.

## 4.5 Simulation and Performance Analyses of The WFG<sub>INT</sub>

The proposed analog WFG<sub>INT</sub>, with amplitude and frequency tuning, in Figure 4.2 was simulated in 130-nm CMOS process technology on Mentor Graphics Pyxis version 10 [192]. The component values and device sizes of the different stages are chosen based on specific low frequency operation and power consumption constraints. To enable better headroom (and device matching), 2.5V NMOS (Dgnfet) and PMOS (Dgpfet) with minimum channel length of 0.24 $\mu$ m at dual-supply-voltage of  $\pm 1$ V were utilized for the core oscillator. The basic 130-nm node-size was used for the digital blocks (logic gates and flip-flops) at single-supply-voltage of only +1V. In order to achieve micro-power consumption, low bias currents and minimized device widths were employed. For high gain and low-frequency design, a small bias current with an appropriate channel width and length will be selected, based on the simulation, to get a good trade-off between speed, gain and power. Following the analysis presented earlier (section 4.3), optimum design values were considered for the active and passive components of the Schmitt Trigger in STG1, STG2 and STG3, and for the gm-C integrator in STG4. The key factors that control the gain of the Schmitt Trigger circuit are the bias currents and the  $W/L$  ratios of the input differential pair M1, M2 and the common-source gain stages M5 and M6. The M1, M2 input pair in STG1 which dominate overall circuit performance are matched for equal trans-conductance, each at saturation region. The desired gain of the circuit can be achieved by increasing  $W$  and  $L$  or decreasing the value of the bias current  $I_B$ . Using an iterative technique, with the possible set of  $W$ ,  $L$  and  $I_B$  optimal dimensions for MOSFET devices, minimized bias current with high gain was achieved. The width for NMOS of the differential input pair (M1 and M2) are chosen to have equal sizing as  $W1=W2=8\mu$ m, and the channel length chosen as  $L1=L2=0.24\mu$ m (with the scale factor,  $L = 0.24\mu$ m). A larger channel width  $W3=W4=12\mu$ m of the P-MOS active current mirror (M3, M4) devices that have a lower value of hole mobility is chosen to minimize the value of  $V_{GS3,4}$ , resulting in higher output swing. The channel width of the current source load, M12, is  $W12=5\mu$ m which gives operating bias current of around 66 $\mu$ A for the STG1. The gain stages transistors, M5 and M6, are chosen to have equal width of  $W5=W6=17\mu$ m, while the output resistance of the current source loads, M13 and M14, is designed to be much larger than M5 and M6 output resistances, using a channel length  $L13=L14=0.48\mu$ m of twice the

minimum length (with the scale factor,  $L = 0.24\mu\text{m}$ ), while the width of M13 is chosen as  $W13 = 4\mu\text{m}$  and M14 as  $W14 = 5\mu\text{m}$ . The operating bias currents of around  $26\mu\text{A}$  and  $33\mu\text{A}$  were drained for the STG2 and STG3 respectively, for the chosen device sizes for these two stages. However, M14, which provides bias current  $IB3$  is also utilized for the realization of an appropriate tuning technique, thereby tuning the amplitude of the  $WFG_{INT}$  (to be discussed in the next section).

The suitable design values for the active and passive elements of the gm-C integrator in STG4 are also investigated thoroughly with the size of the input pair M7, M8, being the most critical. Relatively longer channel length ( $L = 1.2\mu\text{m}$  which is 5 times the minimum length, with the scale factor,  $L = 0.24\mu\text{m}$ ) provides this OTA high output resistance and high voltage gain. The width of M7, M8 ( $W7 = W8 = 4\mu\text{m}$ ) is selected to enable enough current drive for the chosen capacitor load  $C$ . A larger channel width  $W9 = 11\mu\text{m}$  and  $W10 = 7$  of the PMOS current mirror devices, M9 and M10, is chosen to minimize the value of  $V_{SG9,10}$ , and to increase the output swing of the integrator. The purpose of the small mismatch between the PMOS devices of the gm-cell is to control the duty cycle of the integrator. The duty cycle of the  $WFG_{INT}$  can then be controlled by adjusting the width of PMOS load, M9; the wider the device, the larger the duty cycle. A long channel length of  $L15 = 12\mu\text{m}$  was chosen, and  $W15 = 0.85\mu\text{m}$  for M15. The size of M15 was designed and chosen not only to provide the bias current  $IB4$  to the integrator, but also for ultra-low-power realization of an appropriate linear tuning technique (2.7) to adjust the bias current  $IB4$ , which adds and enhances the gm-C Integrator continuous linear tuning ability, thereby tuning the frequency (time-constant) of the integrator. However, choosing an appropriate  $IB4$ , and small ( $W7,8 / L7,8$ ) ratios, to enhance the gain and to reduce the oscillation frequency of the designed gm-C circuit, will meet the requirements. After iterative simulations, bias current  $I_{ref} = 132\mu\text{A}$  for  $R_{ref} = 15\text{k}\Omega$  was achieved to optimize constant power consumption for the OTA stages. The  $WFG_{ING}$  circuit provides a peak-to-peak output voltage  $V_{p-p}$  of about 1.5V for  $R = 10\text{k}\Omega$ . The circuit can source a considerable amount of current at the output stage, being about  $164\mu\text{A}$  (peak-to-peak output current  $I_{p-p}$ ) which can be useful in current source applications. A load capacitor of only 10pF is utilized to reduce the chip area and create an oscillation frequency in kHz range. The circuit generated a typical square waveform as shown in Figure 4.9, with an oscillating frequency,  $f_{WFG} = 17\text{kHz}$  and duty cycle of 50%. Figure 4.10 represents the spectrum-analysis indicating its odd harmonics

with reducing amplitudes ( $f_1=51\text{kHz}$ ,  $f_2=85\text{kHz}$ ,  $f_3=119\text{kHz}$ , and  $f_4=153\text{kHz}$ ). A triangular waveform ( $V_{INT}$ ) is generated across C, as shown in Figure 4.11 with variable tuning range. The proposed WFG<sub>INT</sub> thus performs satisfactorily with integrated passive component values  $\leq 10\text{k}\Omega$ , and capacitance  $\leq 10\text{pF}$  and is tuneable using the gm-C integrator.

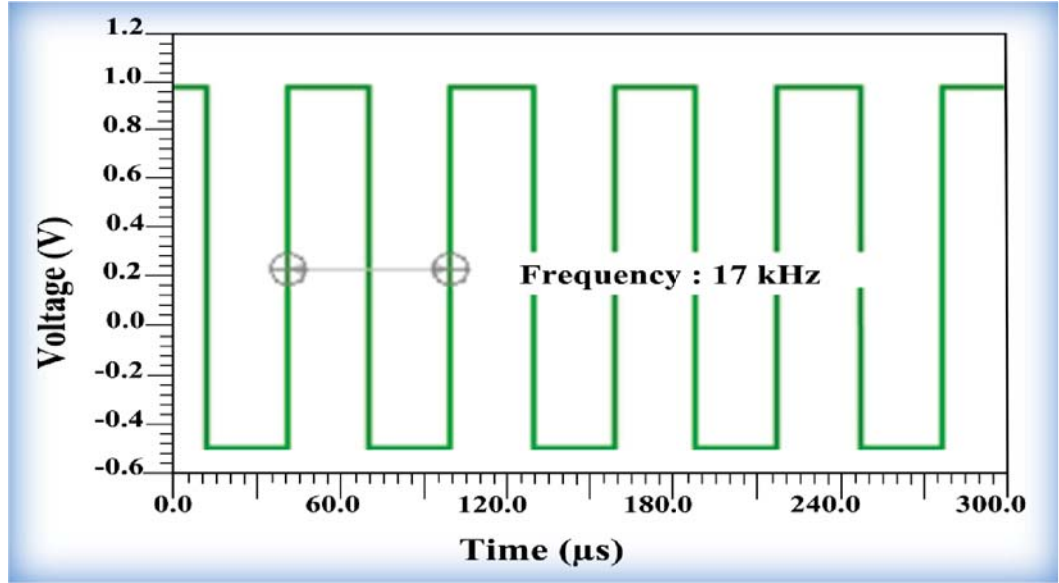


Figure 4.9. Simulated transient square waveform output of the WFG<sub>INT</sub>.

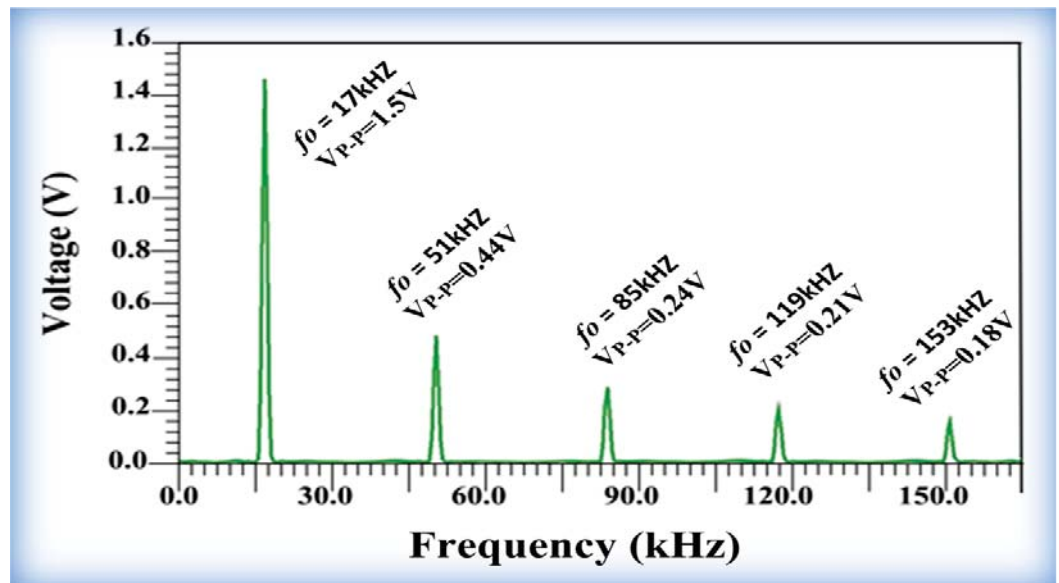


Figure 4.10. Spectrum analysis of the square waveform signal ( $f_{WFG} = 17\text{ kHz}$ ) in simulation profile.

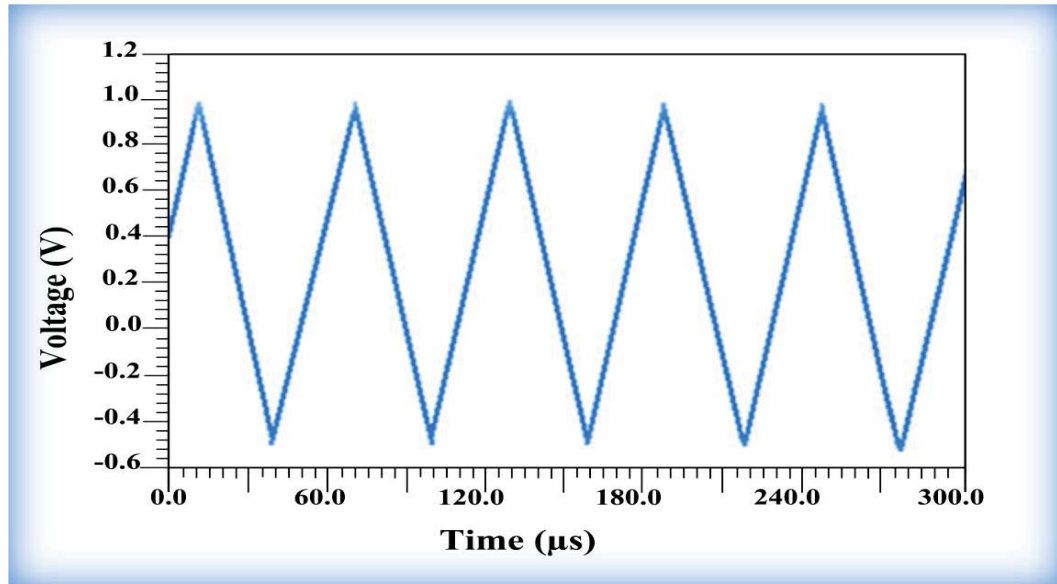


Figure 4.11. Simulated transient triangular waveform at the integrator output.

However, in addition to the square waveform and triangular waveform output signal with variable frequency, other waveform output signals, including sine waveforms, may be generated by feeding the output of the integrator (triangular waveform) into a low pass filter. A performance comparison for the amplitude and frequency control is discussed in the fabrication and experimental results section.

#### 4.5.1 Robustness of The WFG<sub>INT</sub> Circuit

##### 4.5.1.1 Temperature Variation

The temperature dependence of the circuit was investigated to test the frequency stability. For the set bias currents, and fixed values of  $R_{ref}=15\text{k}\Omega$ ,  $R=1\text{k}\Omega$  and  $C=10\text{pF}$ , varying the temperature in the range  $-50^{\circ}\text{C}$  to  $120^{\circ}\text{C}$ , the change in frequency is plotted in Figure 4.12. The results indicate that the oscillation frequency stability is maintained within  $-5^{\circ}\text{C}$  to  $+100^{\circ}\text{C}$ , with small positive and negative deviations in the  $100^{\circ}\text{C}$  to  $120^{\circ}\text{C}$  and  $-5^{\circ}\text{C}$  to  $-50^{\circ}\text{C}$  ranges respectively compared to the value at  $27^{\circ}\text{C}$ .

##### 4.5.1.2 Eye Diagram Analysis

An eye diagram provides useful graphical quality analysis of a generated (source) signal and the transfer of digital data streams. An eye diagram is a well-

established visual and useful tool for a graphical representation of the quality analysis of the generated (source) signal and transfer of digital data streams signal [197]. The graphical eye pattern is constructed by overlaying many repeated samples of a signal waveform with all possible transitions and states superimposed in one comprehensive view. Overlaying many transitions, positive- and negative-going pulses with sharp rise and fall times are superimposed on each other; the resulting graphic will be displayed at one bit intervals (unit intervals). This is referred to as the "eye period" in a single graph in the eye diagram, with a signal amplitude on the vertical axis and time on horizontal axis, [198, 199] which gives at-a-glance estimation of system performance and can provide a set of measures for the evaluation of signal imperfections. It is a valuable display for intuitive and quick assessment of the performance of the circuits that shows the parametric information of the signal. In this research project, the eye diagram is employed on a Mentor Graphics platform for the time-domain simulations to examine the variations in amplitude and timing errors (jitter) of the oscillations. Figure 4.13 shows the eye diagram of the proposed WFG<sub>INT</sub> output.

Eye height (the vertical opening) can be determined from the bit amplitude and the eye noise as,

$$\text{Eye Height} = (V_H - 3\sigma) - (V_L + 3\sigma) \quad (4.37)$$

Also, the eye width (the horizontal opening) can be determined from the bit period and the eye jitter as,

$$\text{Eye Width} = (t_{\text{crossing2}} - 3\sigma_{\text{crossing2}}) - (t_{\text{crossing1}} + 3\sigma_{\text{crossing1}}) \quad (4.38)$$

where  $\sigma$  is the standard deviation for the eye height and eye width events, "3-sigma" ( $3\sigma$ ) represents the abnormal variations, while  $V_H$  and  $V_L$  are the high and low voltage levels respectively, and  $t_{\text{crossing1}}$  and  $t_{\text{crossing2}}$  are the time-base crossing points. The results obtained yield a favorable eye diagram which demonstrates an optimum quality of the designed circuit. As seen in Figure 4.13, the simulation results in eye height and eye width, which are equal to the amplitude and bit period respectively, indicating ideal circuit performance.



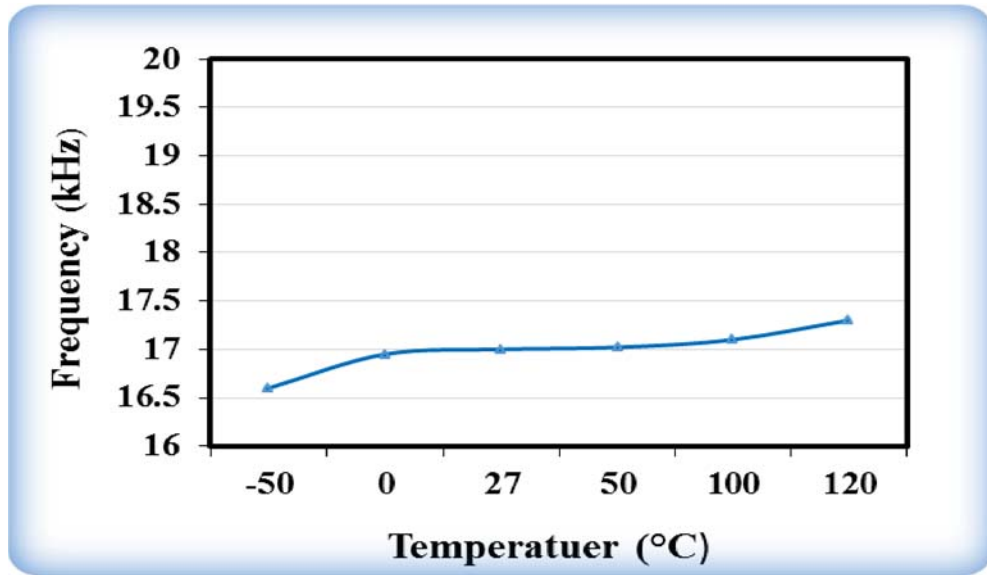


Figure 4.12. WFG<sub>INT</sub> circuit analysis for the frequency stability with temperature variations.

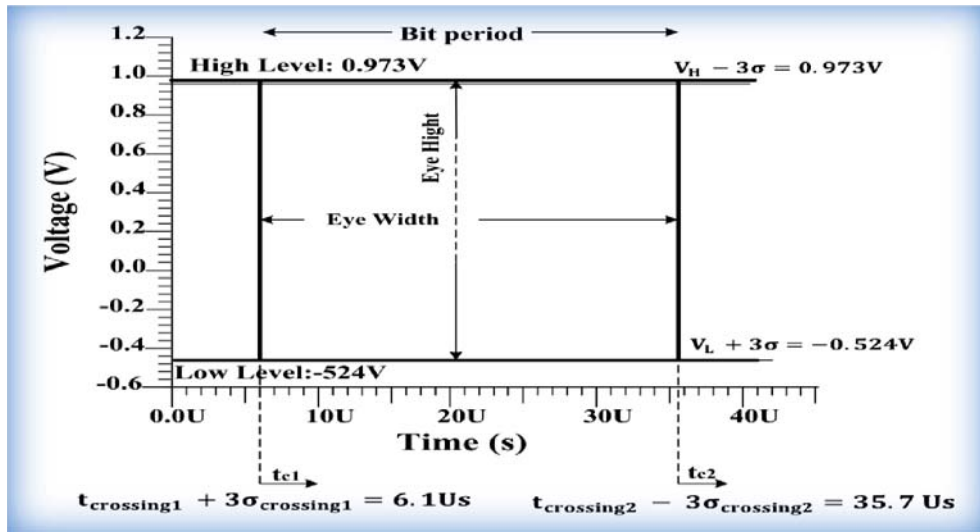


Figure 4.13. Eye diagram simulation results for the designed WFG<sub>INT</sub>.

## 4.6 Simulation Results of The Digital Model

The digital model circuit is also designed and simulated in a standard 130-nm technology. The supply voltage used for simulations is +1V, and the operating temperature is 27°C. In this work, first the performance of the clk, clk\_bar and the /2

frequency division circuit was evaluated, and then the performance of the MUXs and PS circuits. Generally, power consumption as well as silicon area of the digital circuit depends on appropriate circuit topology and the device  $W/L$  ratios. As previously mentioned in section (2.8.3), the main avenue of power dissipation in the implemented digital CMOS circuits is the dynamic power, and as per (2.10), using low  $f_{clk}$ , the dynamic power dissipation can certainly be reduced. Scaling supply voltage and lowering capacitor load can substantially reduce power dissipation. The importance of using lower  $VDD$  is also obvious in (2.10) from which the dynamic power is reduced in proportion to the square of any reduction in  $VDD$ . The importance of reduction of loading capacitance is also obvious in (2.10); the lower the load capacitance (load capacitance is proportional to the  $W$ ) [54], the smaller the dynamic power. Moreover, using lower supply voltage,  $VDD$ , supplements other power dissipation in the CMOS digital circuit including short circuit power (2.11), and leakage power (2.13).

However, the power consumption and layout area of the CMOS gate in this project research is scaled up or down by using the “ratioed” technique, with simple variation  $W/L$  ratios of the NMOS and PMOS transistors. Since each logic input variable in static CMOS requires one NMOS and one load PMOS transistor, the drain currents of the NMOS ( $I_{DN}$ ) and PMOS ( $I_{DP}$ ) transistors in any logic gate are specified by their  $W/L$  ratios that can be selected, so that  $I_{DN} = I_{DP}$  for  $V_{out} = V_{Load}$  [54]. For fixed supply voltages,  $I_{DN}$  and  $I_{DP}$  are proportional to their relevant  $W/L$  ratios. If the  $W/L$  ratio of the NMOS and PMOS transistors is doubled, the drain currents  $I_{DN}$  and  $I_{DP}$  are then doubled with no change in operation voltage levels. Or, if the  $W/L$  ratios of both NMOS and PMOS transistors are reduced by a factor of 5, then the drain currents  $I_{DN}$  and  $I_{DP}$  are both reduced by a factor of 5, with no change in operation output voltage levels. Accordingly, if the  $W/L$  ratios of NMOS and PMOS transistors are changed by the same factor, the power level ( $P_{static} = V_{DD}I_{DD}$ ) of the logic gate can easily be scaled up and down without degrading the high and low output values, where  $I_{DD} = I_{DP}$  is equal to the current through the load PMOS device, and the total power supplied by  $VDD$  is dissipated in the load and switching transistors. The power scaling is characteristic of ratioed logic circuits; with this “ratioed” technique, the digital model is designed to operate at lower power dissipation by reducing the value of  $W/L$  of each device. Moreover, reducing the value of  $W/L$  of each device achieves a significant reduction in silicon area. Initially, all digital circuits are sized for minimum size

(0.36 $\mu\text{m}$  for 130nm CMOS), and sized up iteratively for precise functionality. However, considerable power dissipation and layout area savings can be achieved by implementing all the gates with minimum transistor size.

#### 4.6.1 Clock And Clock\_Bar

The clock and clock\_bar signals are generated from the single-ended +1V supply, using a cascade of level shifting inverters and regular inverters (INTs). The level shifting inverter has a 2.5V MOSFET device, as the voltage across it can be as high as 2V, for low logic input from the  $\text{WFG}_{\text{INT}}$  of the Schmitt Trigger. It is worth noting, that series inverters are not required to sharpen the  $\text{WFG}_{\text{INT}}$  output signal, since the square output signal has no distortion [54, 194]. The symmetrical behaviour of the INVs is achieved by sizing the PMOS ( $M_{\text{INVP}}$ ) width larger than NMOS ( $M_{\text{INVN}}$ ) width; since the NMOS mobility is larger than that of PMOS, the actual sizes are extracted by means of simulations. An iterative simulation was applied to optimize the INV size, and a symmetrical output waveform is obtained by using the same channel length and by sizing the PMOS width  $W_p = 6\mu\text{m}$ , three times the NMOS width,  $W_N = 2\mu\text{m}$ , for both inverters. Figure 4.14 shows the simulated transient response of the clk and clk\_bar signals which are of rail-to-rail signal swing with frequency of 17kHz. By considering the number of MOSFET transistors as a rough metric of the layout area, given that minimizing the width of MOSFET transistors was one of the main goals, this gives the total active area for the clk and clk\_bar of  $\sum W_{\text{NINV}} L = 1.92\mu\text{m}^2$ .

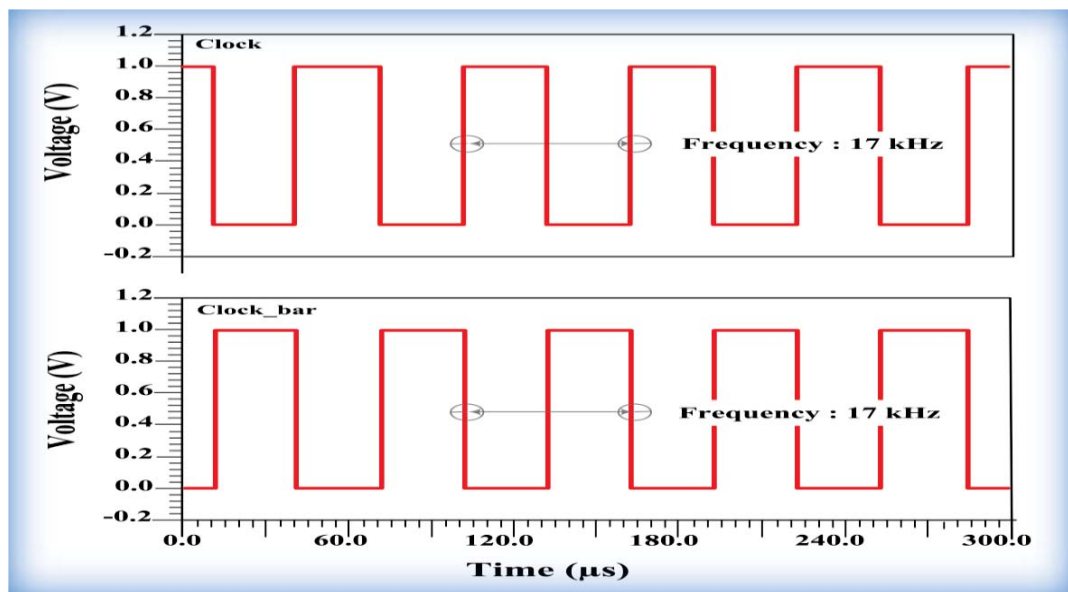


Figure 4.14. Simulated transient response of the clock and clock\_bar generator.

#### 4.6.2 FD circuit

The FD circuit also utilizes a +1V supply and its critical delay path was scaled for satisfactory performance. Power consumption as well as silicon area of the FD circuit depends on appropriate Flip-flop topology and the device  $W/L$  ratios. All of the TGMS D-FFs utilized were identical copies. To optimize the FD, the circuit was investigated for various widths of the NMOS and PMOS devices for both the INV and TG elements using the same actual channel length. Accordingly, an iterative process was employed to optimize all the FF stages for a low power budget. Initially, all transistors were sized for minimum size ( $0.36\mu\text{m}$ ) and sized up iteratively for precise functionality. By varying the  $W_{TGP,N}$  of the TG with respect to  $W_{INVP,N}$  (smaller, equal, or larger than the width in the INV). Considering minimum value  $W_{min}$ , it was found that a symmetrical and accurate functionality is obtained by sizing the  $W_{INVP}=6\mu\text{m}$  three times,  $W_{INVN}=2\mu\text{m}$ , while the  $W_{TGP}$  and  $W_{TGN}$  of the TG are sized to equally:  $W_{TGP} = W_{TGN} = 2.5W_{INVN}=5\mu\text{m}$ . The active area for each FF was  $\Sigma W_{INV} L + \Sigma W_{TG} L = 4.32\mu\text{m}^2$ , where  $\Sigma W_{INV} L$  is the sum of the areas of all the inverter devices and  $\Sigma W_{TG} L$  is the sum of the areas of all the TG devices. The overall active area of the 16 TGMS D-FFs is then equal to  $138.24 \mu\text{m}^2$ . The inverter sizing for MUX, PS and the output stage were the same as that of the clk, while NMOS and PMOS of the TG for the MUX circuit are sized, based on the standard approach, to have equal size;  $W_P$  and  $W_N$  are then varied through a wide range. The optimal  $W$  for each combination of the TG is achieved by setting the  $W_{TGP} = W_{TGN} = 5\mu\text{m}$ , which is the same as for D-FF circuit. The total active area for the two MUXs was  $\Sigma W_{TG} L + \Sigma W_{INV} L = 39.36\mu\text{m}^2$ , while the total active area for the PS and the output stage was  $\Sigma W_{TG} L + \Sigma W_{INV} L = 4.32\mu\text{m}^2$ . The total active area of the digital block (including INV) was approximately  $183.84\mu\text{m}^2$ . Figure 4.15 shows the 16 channel output square waveforms digitally selectable through MUX1, MUX2 and PS. For a general design requirement, and since the power dissipation of the designed digital circuit is dominated by the FD circuit, the low-power design goal of the FD circuit becomes the task of minimizing, while remembering the precise functionality and identifying the trade-off of such minimizations in terms of performance and area. Since the FD circuit is relatively simple and symmetrical it was easy to express all transistor widths as a function of one variable  $W_N$  ( $W_P = 3W_N$  for INV and  $W_{TG} = 2.5W_N$  for TG) for the purpose of optimization.

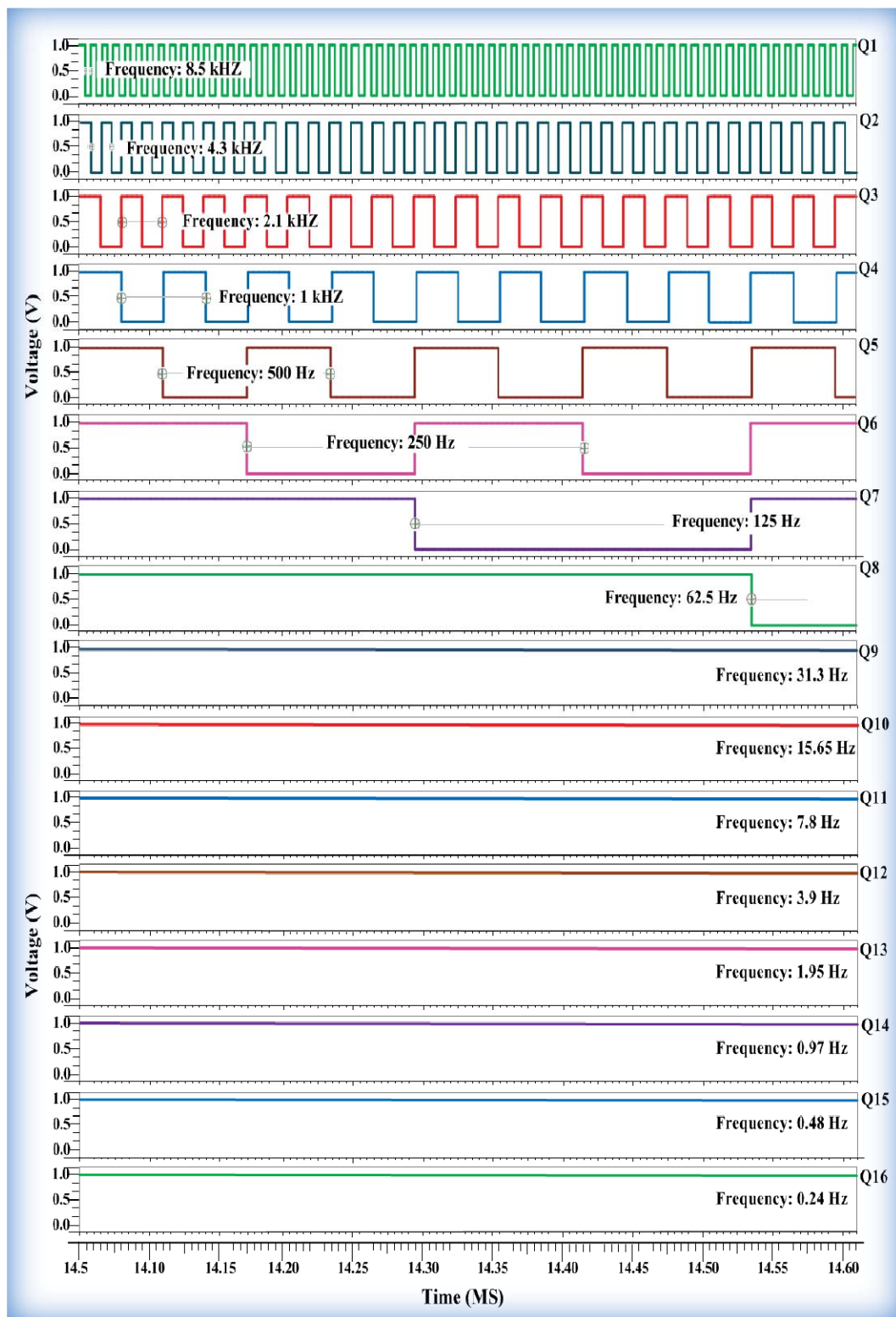


Figure 4.15. The 16 channel output square waveforms digitally selectable through MUX1, MUX2 and PS.

The optimum FD device-width  $W_N$  vs. power and area was then determined through simulations. Table 4.1 summarizes these results. Regarding sizing, the data reported in Table 4.1 considered the final iterative result of the FD transistors only, without the contribution of all iterative process. Hence  $W_N$ ,  $W_P$  and  $W_{TG}$  are the weight factors for area and power consumption. The optimal design was achieved by constraining these weight factors without impairing circuit performance. In terms of area consumption, obviously a circuit with small  $W$  consumes a small silicon area, while using small  $W$  can also reduce power consumption, but the circuit may not function properly. Figure 4.16 shows the proportionality relationship between power consumption and  $W_N$ . However, values of  $W$  that are too small lead to increase in the effective switching resistance of the logic gate and decrease the inverter gain. Consequently, for optimum operation and to improve the inverter gain, slightly oversize  $W_N$  was chosen. A high gain logic gate also enhances the resolution of any metastability in the logic signals [200]. The effect of supply-voltage scaling on the power dissipation of the FD circuit was also investigated. To evaluate low-power performance, the supply-voltage is varied from 0.6V to 1.2V yielding the power and frequency variations shown in Figure 4.17 and Figure 4.18 respectively. The FD circuit dissipates 0.45mW at input frequency of 10.3kHz with  $VDD = 0.6V$ , 1.1mW at input frequency of 13.5kHz with  $VDD = 0.8V$ , 2.1mW at input frequency of 17kHz with  $VDD = 1V$  and, 3.6mW at input frequency of 20kHz with  $VDD = 1.2V$ . The input frequency is the  $WFG_{INT}$  frequency at a particular supply-voltage. Figure 4.19 shows the simulated speed ( $WFG_{INT}$  frequency)-power trade-off of the FD circuit. The symbol “□” represents the point of the best (*optimal*) power and accurate functionality trade-off. Using  $VDD$  of +1V indicates acceptable power-frequency trade-off. The simulation results thus indicate that the designed  $WFG_{INT}$  core is able to generate up to 17kHz with a power consumption of only 0.457mW (using  $\pm 1V$ ), while the FD circuit consumes 2.1mW (using +1V), resulting in total power dissipation of only 2.557mW.

The effect of the tuning range (using  $V_{tune}$ ) of the gm-C integrator on the overall power dissipation of the proposed circuit with  $C=10pF$  was also investigated. Figure 4.20 displays the result for frequency and power vs.  $V_{tune}$  varied in the range  $\pm 0.9V$ . The proposed circuit dissipates 2.5mW at 5.8kHz (with  $V_{tune} = -0.9$ ) and 5.8mW at a high frequency of 1003kHz (with  $V_{tune} = 0.9$ ). The optimal transistor dimensions and passive component values for the proposed analog  $WFG_{ING}$  are

displayed in Figure 4.2, while, for the FD  $W_N=2\mu\text{m}$  (so that,  $W_P=6\mu\text{m}$  and  $W_{TG}=5\mu\text{m}$ ) was chosen with  $L=130\text{-nm}$ . For the TG, PMOS and NMOS devices have same device-size and hence identical layout geometry. The optimal performance of the system is presented in Table 4.2.

Table 4.1. The power and area versus generalized transistor width for the designed FD circuit.

<b>W (<math>\mu\text{m}</math>)</b>			<b>Total power consumption (mW)</b>	<b>Total active area <math>\sum WL(\mu\text{m} \times \mu\text{m})</math></b>
<b>W<sub>N</sub></b>	<b>W<sub>P</sub></b>	<b>W<sub>TG</sub></b>		
0.5	1.5	1.25	0.64	45.96
1	3	2.5	1.1	91.92
1.5	4.5	3.75	1.6	137.88
2	6	5	2.1	183.84
2.5	7.5	6.25	2.6	229.8
3	9	7.5	3.1	275.76
3.5	10.5	8.75	3.5	321.72
4	12	10	4	367.68

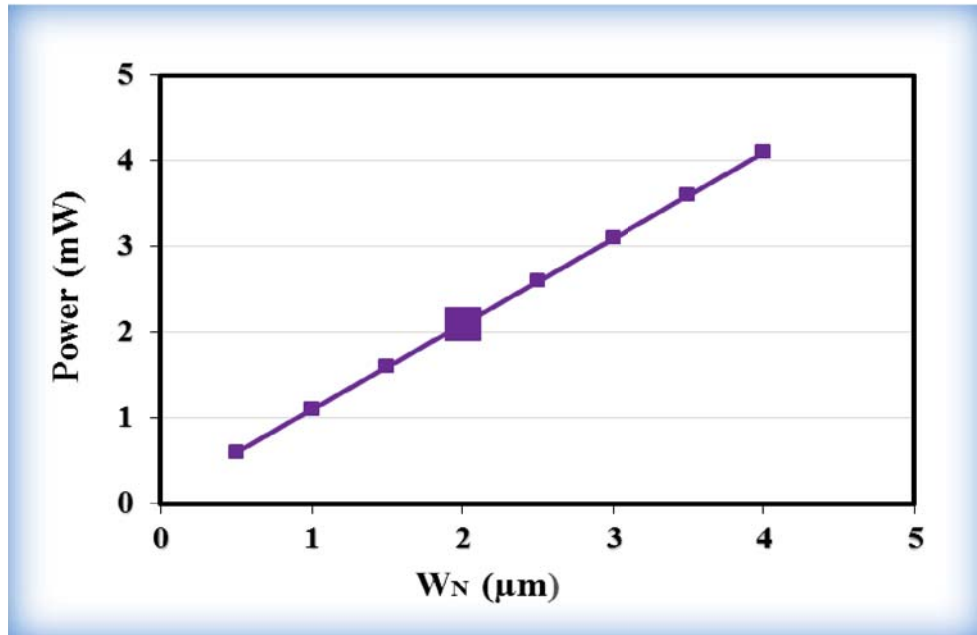


Figure 4.16. Power versus generalized width  $W_N$ .



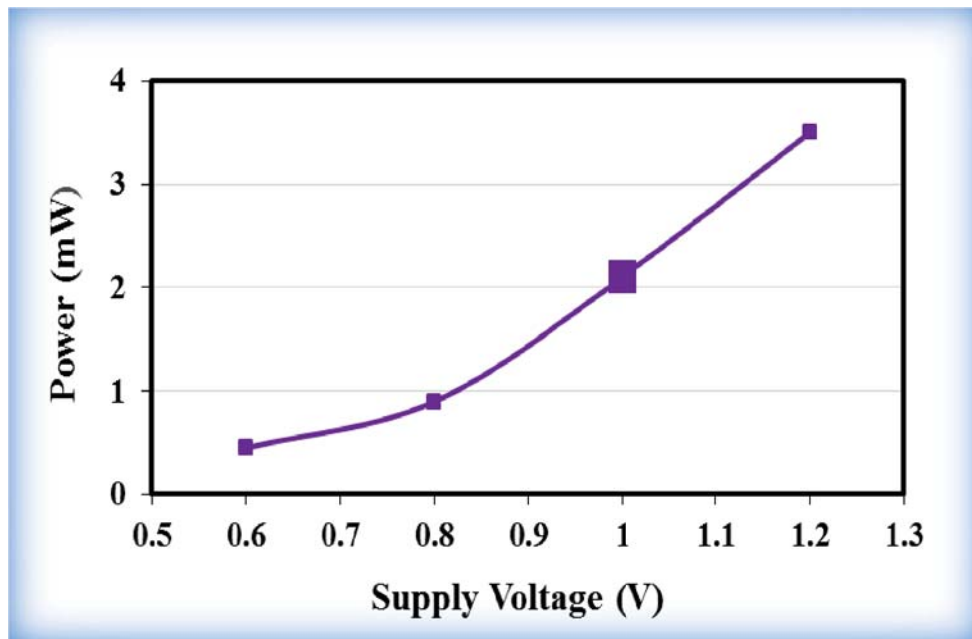


Figure 4.17. Power dissipation versus supply voltage of the FD circuit.

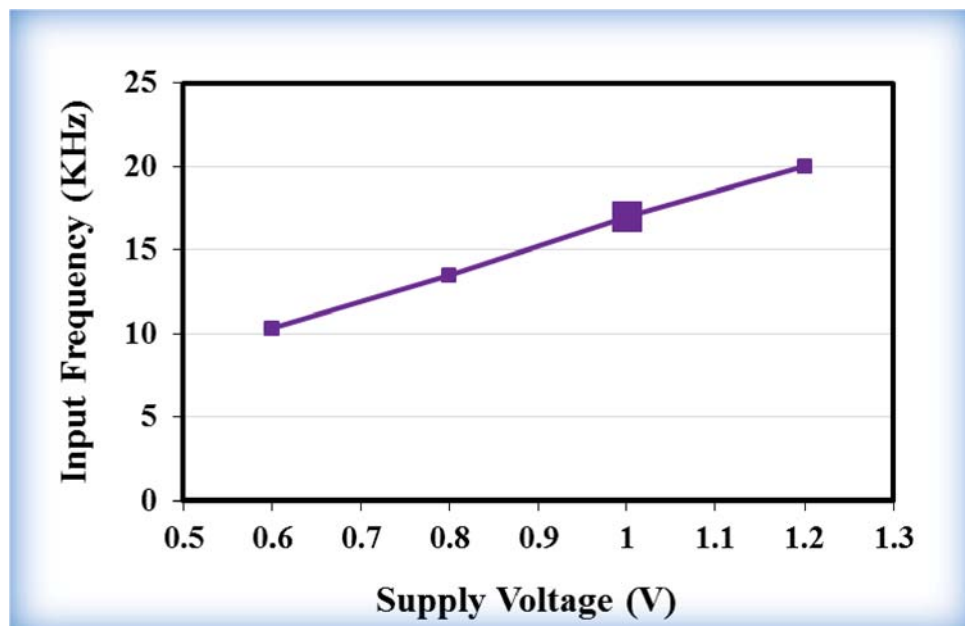


Figure 4.18. WFG<sub>ING</sub> frequency versus supply voltage.

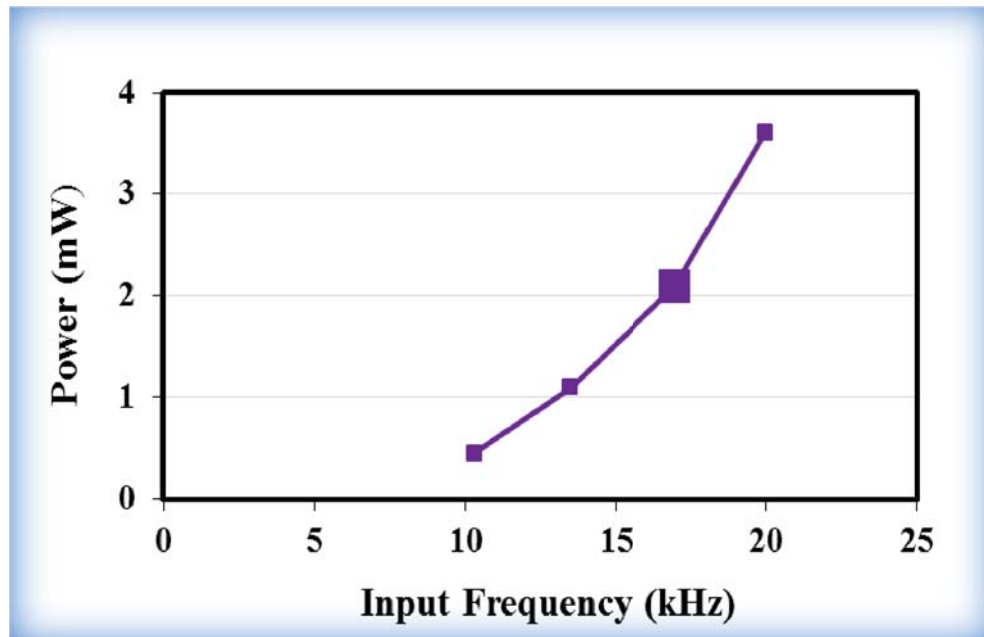


Figure 4.19. The simulated speed-power trade-off of the FD circuit.

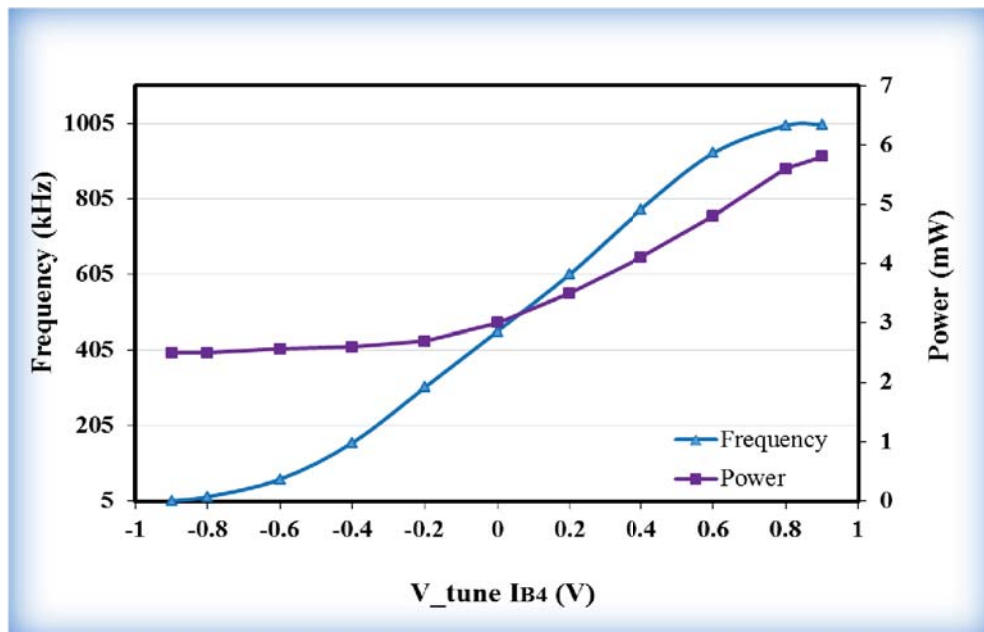


Figure 4.20. The simulation result for power and frequency versus  $V_{\text{tune}}$ .

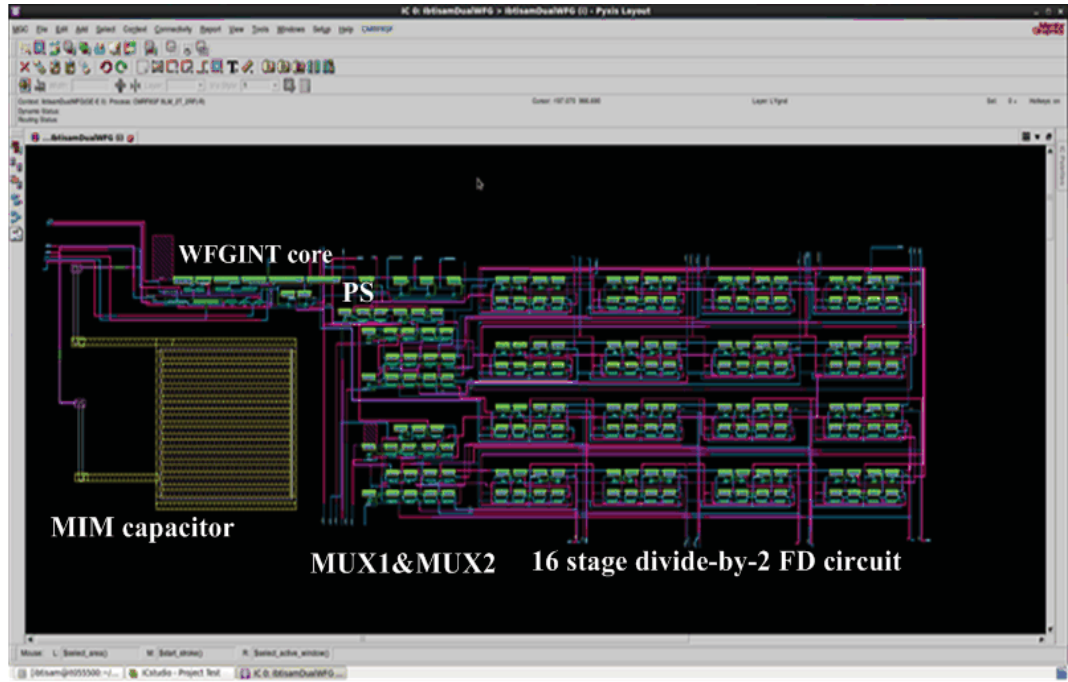
Table 4.2. Simulation results of the outputs of the dual band WFG<sub>INT</sub> designed circuit.

Parameters	WFG <sub>INT</sub>	Digital model
Lmin	0.24nm CMOS	0.13nm CMOS
Amplitude	1.5 V <sub>pp</sub>	1V <sub>pp</sub>
Core Frequency	17 kHz	17 kHz
Duty cycle	50 %	50 %
Output current source	I <sub>PP</sub> =164 $\mu$ A	
Period	58ns	
Slew rate	2.6 GV/ns	
Supply voltage	$\pm 1$ V	+1 V
Power consumption	0.457mW	2.1mW
Total active area	67.08 $\mu$ m <sup>2</sup>	183.84 $\mu$ m <sup>2</sup>

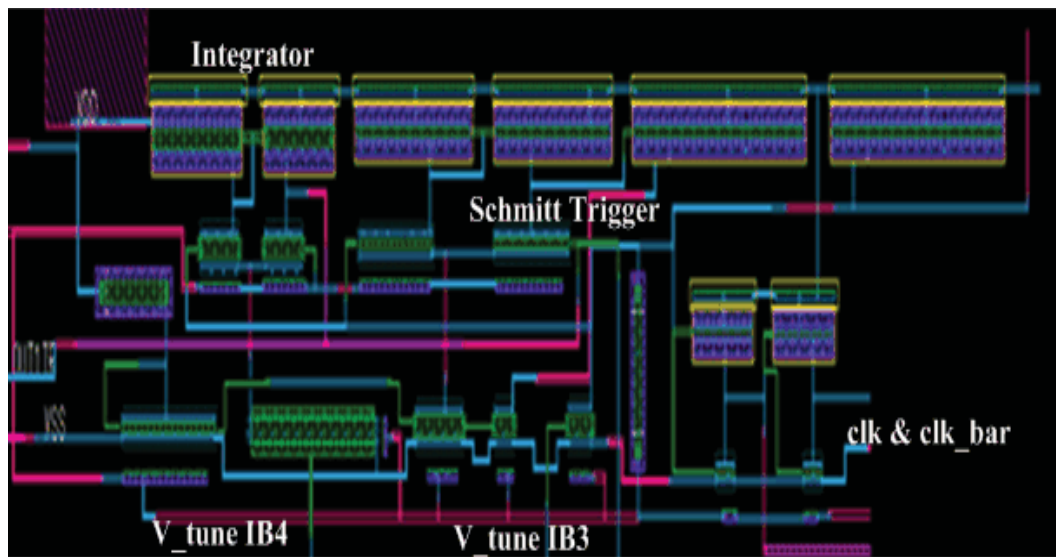
#### 4.7 Layout and Fabrication of The WFG<sub>INT</sub>

The layout of the designed circuit, has been implemented in 130-nm IBM (now GF) CMOS process technology on Mentor Graphics Pyxis CAD programme and were verified to function correctly. In order to optimize the layout for size, the proposed circuit is implemented, using full-custom design techniques utilizing MOSFETs at the lowest level with high regularity. To minimize the layout area of the designed circuit, the same layout procedure adopted in section (3.7) is applied. Considering the design rules, all routing was completed manually with verifying DRC. Each NMOS and PMOS device in analog and digital models is implemented individually with small layout area, and they are connected with a constant height. So, horizontal runs of metal are applied to provide  $VDD$ ,  $VSS$  and ground to the devices, which saves silicon area. The same rules are also used for the substrate and well. The importance of this is that power and ground, as well as substrate and well, are easily routed, with the ordinary arrangement of each device. The DRC and LVS checks were performed for each completed sub-cell and were passed. The active chip area of the complete circuit was 18426 $\mu$ m<sup>2</sup> (*including all interconnects*). The analog WFG<sub>INT</sub> including clk and clk\_bar (excluding the capacitor) occupied a small chip-area of 640 $\mu$ m<sup>2</sup>, and the on-chip capacitor of 10pF

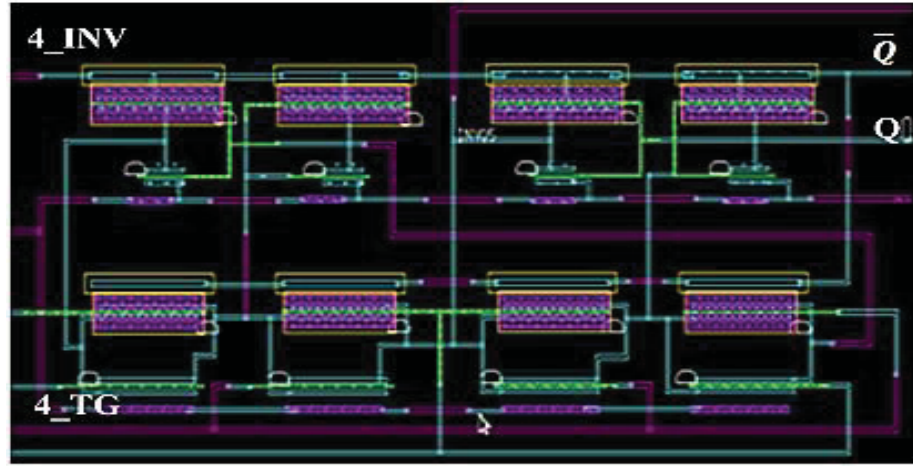
occupied about  $5460\mu\text{m}^2$  within it. The D-FF and MUX, occupied  $550\mu\text{m}^2$  and  $1647\mu\text{m}^2$  respectively, while the output stage including PS and the out of phase circuit occupied  $232\mu\text{m}^2$ . Separate supply and ground bond-pads were used for the analog and digital circuits in order to prevent noise and spikes that may affect the output signals. In addition, digital circuit blocks were isolated by high-resistance substrate enclosures to eliminate the substrate crosstalk. The on-chip current mirror resistor  $R_{ref}$  and the positive feedback resistor  $R$  were fabricated on a reasonably small silicon area employing high sheet resistance p+ polysilicon (*OPRRP*) resistors (with sheet resistance of  $1700\Omega/\square$ ). The load capacitor of the gm-C integrator was implemented as a metal-insulator-metal (MIM) capacitor to reduce thermal and parasitic effects. It is built between the *EI* and *LY* layers. *QY* and *LY* constitute, respectively, the top and bottom plate layers, while *FT* via is used for access to separate *EI* interconnect layers. Assuming square capacitor shapes ( $L=W$ ), the total area of the *QY* layer is calculated using estimates in (3.35) for the capacitance of a MIMCAP. Figure 4.21 (a), (b), (c) (d) and (e) shows the overall layout, (including the capacitor) for the dual-band (mixed-signal)  $\text{WFG}_{\text{INT}}$  circuit, the  $\text{WFG}_{\text{INT}}$  core circuit, D-FF, MUX, and PS circuit respectively, while Figure 4.22 illustrates the packaged microchip of the complete circuit. A prototype proposed circuit is fabricated in 130-nm IBM CMOS process technology using the American IC fabrication facility MOSIS. The microphotograph of the chip is shown in Figure 4.23. The analog and digital sub-blocks and the passive component (load capacitor) are labelled on the photo.



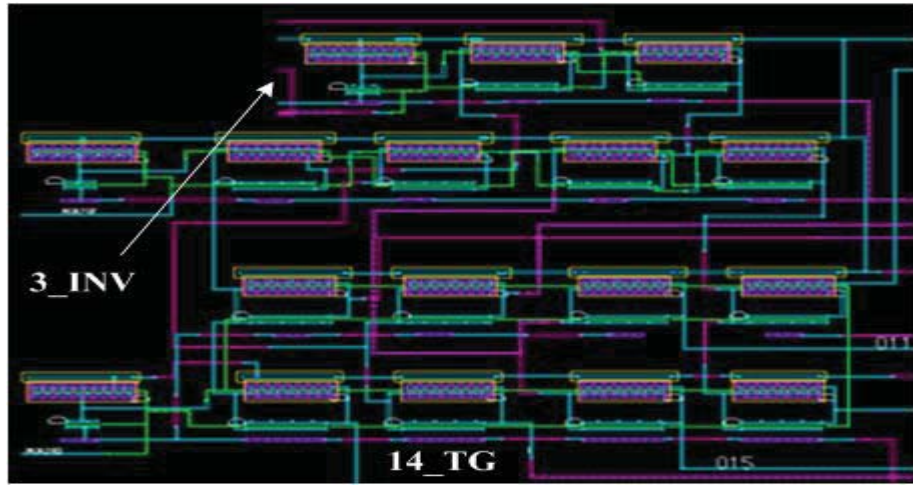
(a) A screen shot showing the overall layout (including the on-chip capacitor) of the (mixed-signal) dual-band WFG<sub>INT</sub> circuit.



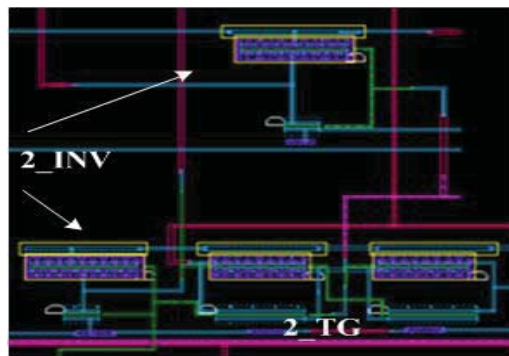
(b) A close view of the complete layout for the WFG<sub>INT</sub> core circuit including the clk and clk\_bar circuit.



(c) A close view of the complete layout for the D-FF circuit.



(d) A close view of the complete layout for the MUX1 circuit.



(e) A close view of the complete layout for the PS circuit.

Figure 4.21. The complete layout (including the capacitor) for the (mixed-signal) dual-band WFG<sub>INT</sub> circuit, (a) the overall layout of the mixed-signal WFG<sub>INT</sub> circuit, while (b) shows a close view of the WFG<sub>INT</sub> core circuit, (c) D-FF, (d) MUX1, and (e) PS circuit.



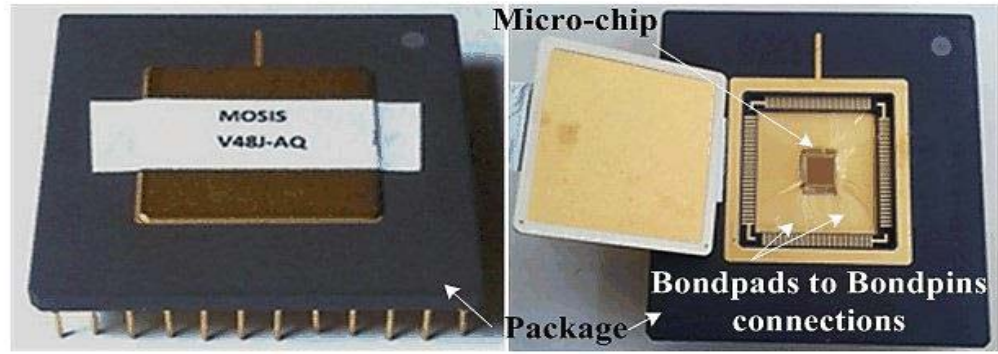


Figure 4.22. Package of the (mixed-signal) dual-band WFG<sub>INT</sub> circuit in PGA.

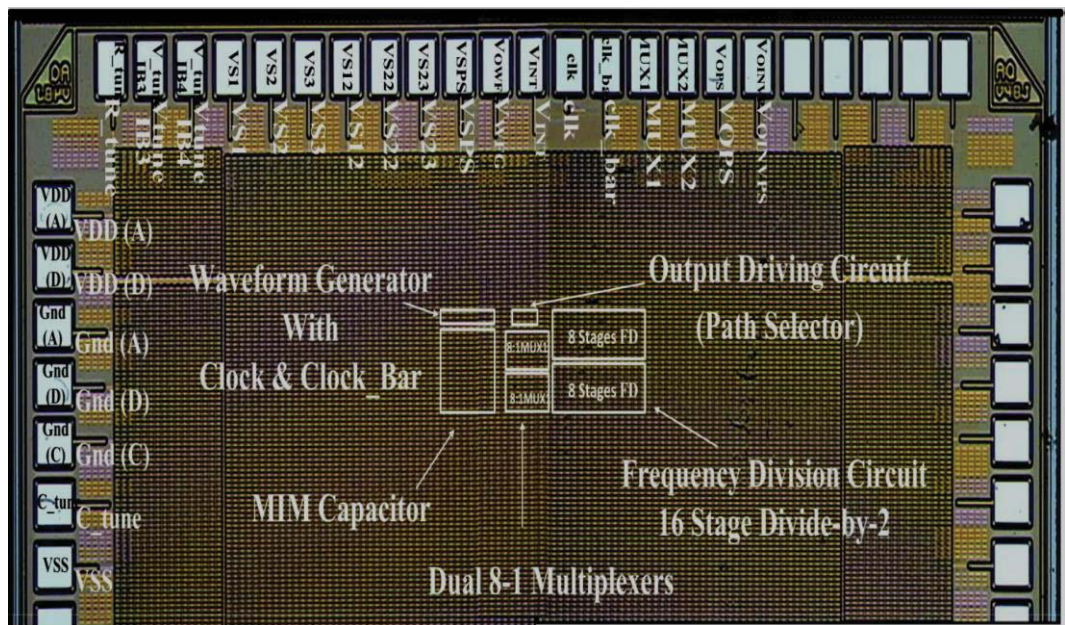


Figure 4.23. Chip photo-micrograph illustrates the location of the integrated (mixed-signal) dual-band WFG<sub>INT</sub> circuit.

#### 4.8 Experimental Results of The WFG<sub>INT</sub>

The experimental setup using the fabricated chip is shown in Figure 4.24. For undertaking measurements, the chip was mounted using a 15x15 matrix PGA kit socket, while the wiring connections were made through a solderless breadboard. Transient measurements were carried out using the Tektronix TBS1102B-EDU digital storage oscilloscope to evaluate signal quality and to calculate important signal characteristics.



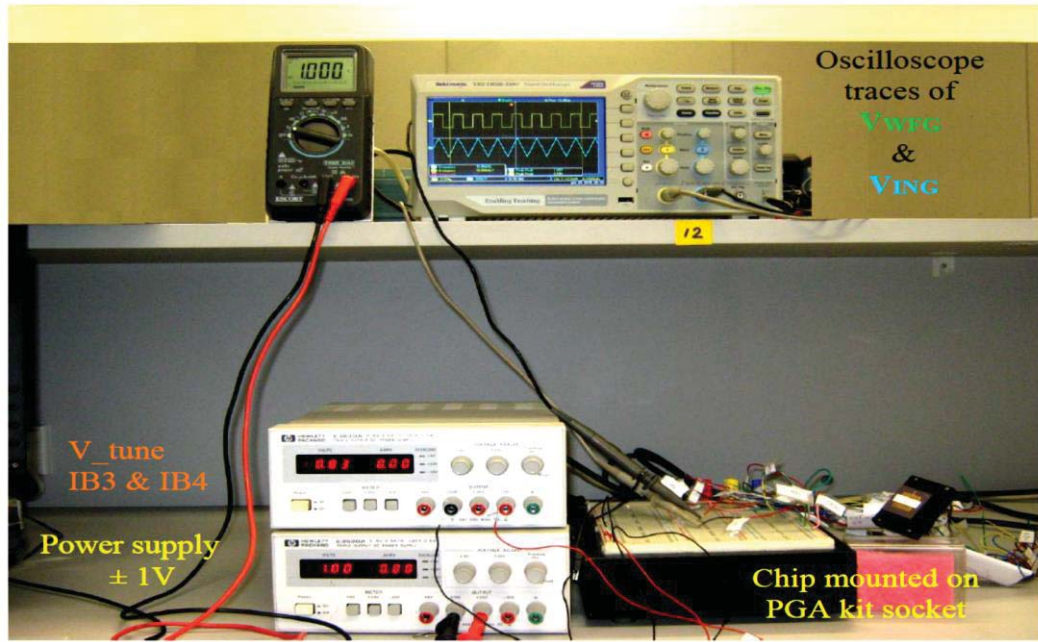
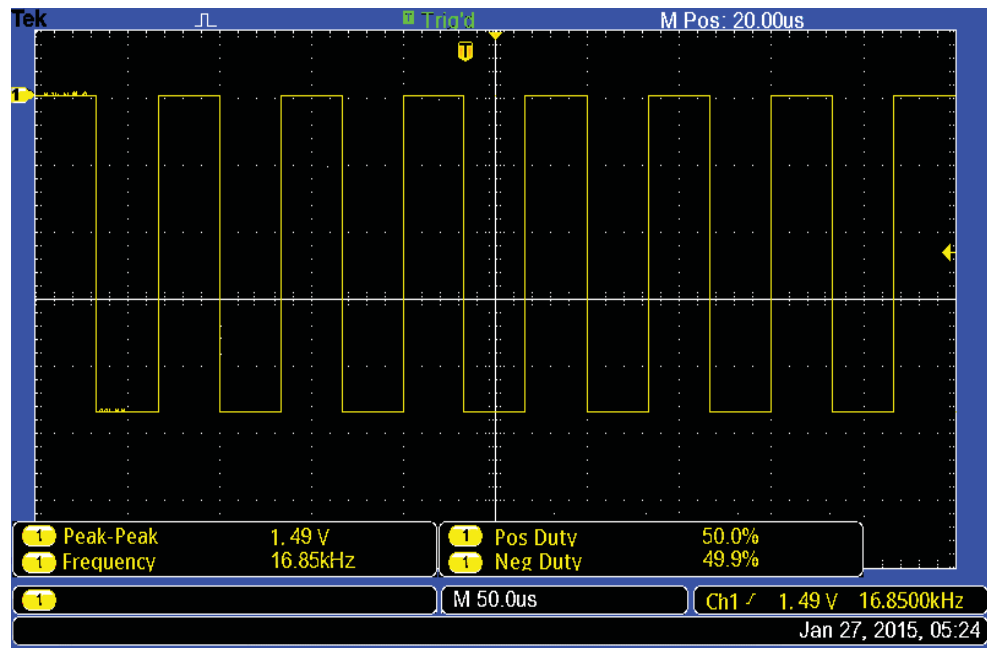
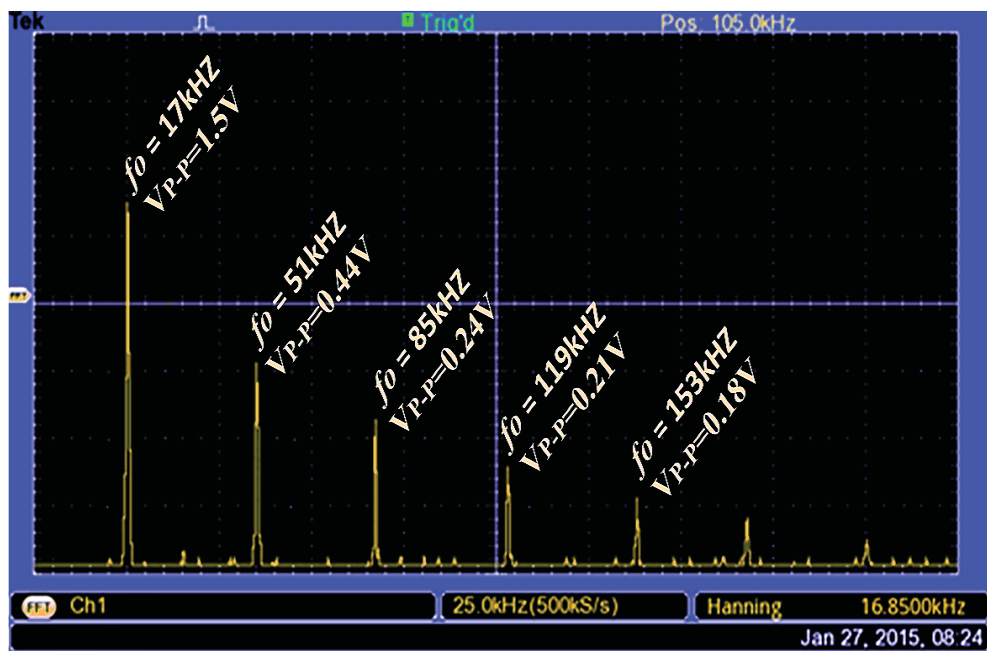


Figure 4.24. Experimental measurement set up for the fabricated oscillator.

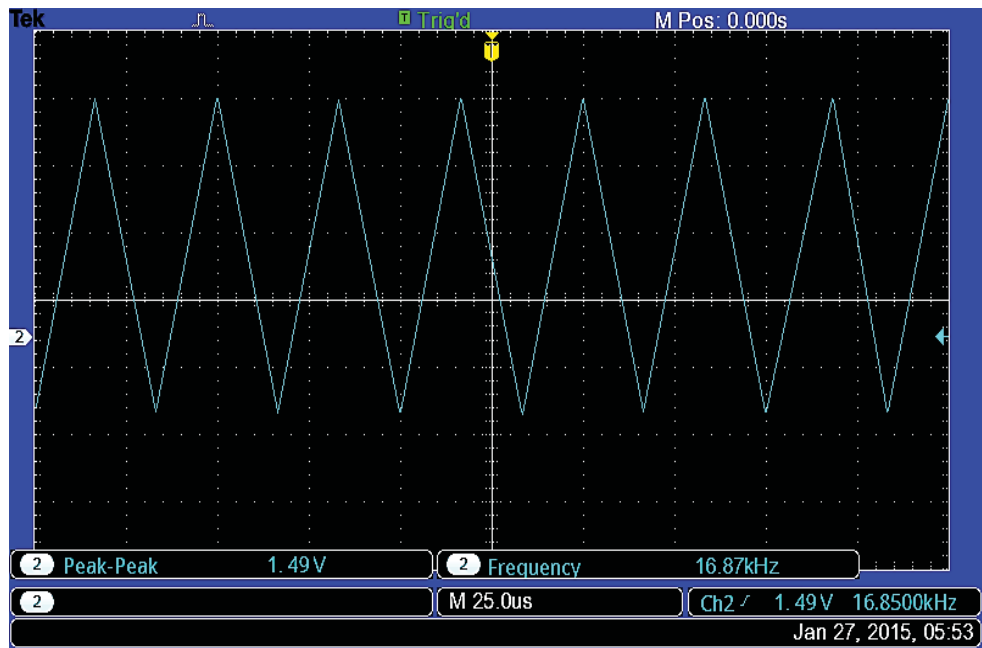
An oscilloscope trace of the output square waveform is presented in Figure 4.25 (a), while FFT of the time domain waveform is also performed simultaneously and displayed in Figure 4.25 (b). The triangular waveform signal, and the clk with clk\_bar signals (with rail-to-rail swing) is shown in Figure 4.25 (c) and Figure 4.25 (d) respectively. For analog  $WFG_{INT}$  measurement, the supply rail of  $\pm 1V$  was used, while all digital measurements are performed using  $+1V$ . The measured amplitude (P-P) and frequency for the core oscillator circuit are around  $1.49V$  and  $16.85kHz$  respectively, which closely matches the simulated profile values. The small variations between simulated and measured results are mostly due to slight process- related deviation of passive component values and OTA (and/or gm-cell) bias current imbalances. Usually, the frequency of most CMOS oscillators may diverge by a factor of two after fabrication, hence, the design step requires an adequate tuning range to ensure that the output frequency can be adjusted to the desired value. The fabricated circuit was tested in a simulation and experiment profile to determine the amplitude and frequency control behaviour. Amplitude and frequency of the proposed  $WFG_{ING}$  can be controlled independently, by adjusting  $R$  or through variation of the OTA bias current  $IB3$ , and by variation of the gm-cell bias current  $IB4$  respectively. Hence appropriate amplitude and frequency tuning range can be achieved to accommodate process and temperature variation as well as for the requirement of a specific application.



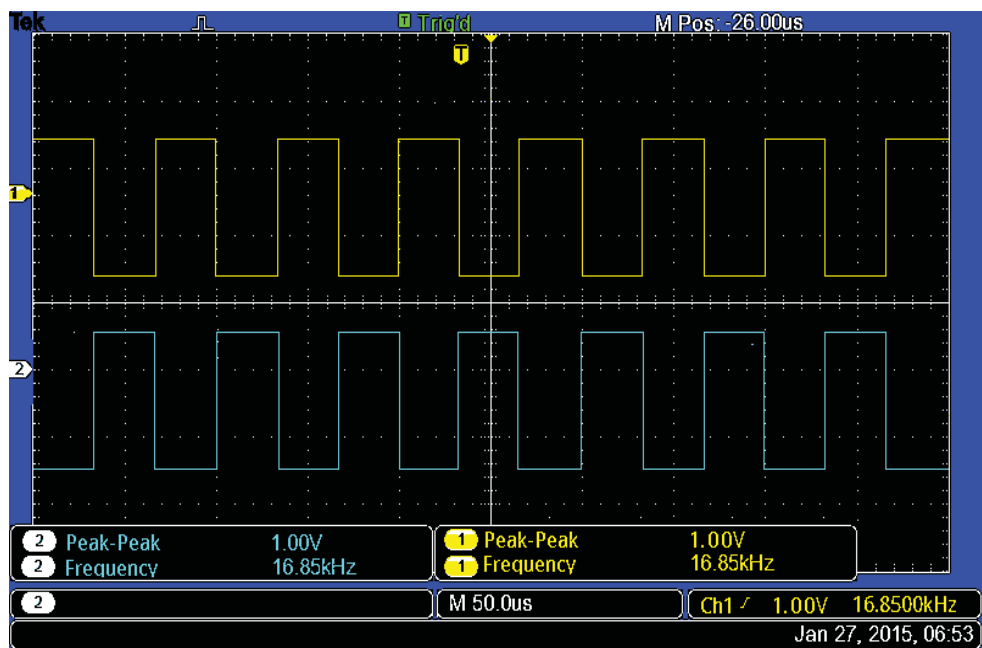
(a) An oscilloscope trace of the output square waveform of the core oscillator.



(b) An oscilloscope trace of the FFT spectrum analysis of the generated square waveform signal.



(c) An oscilloscope trace of the output triangular waveform of the integrator.

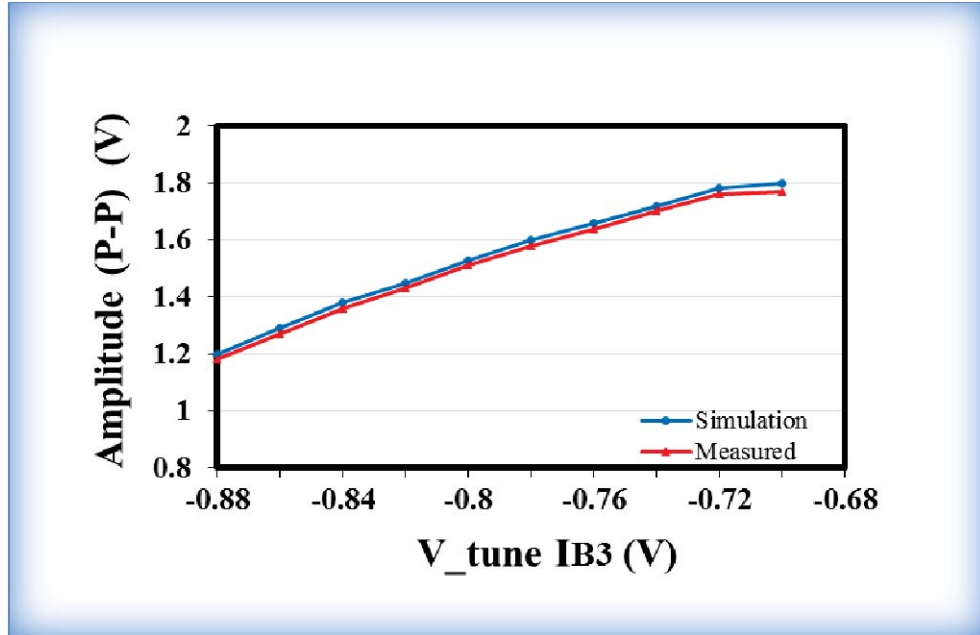


(d) An oscilloscope trace of the clock and clock\_bar translation outputs.

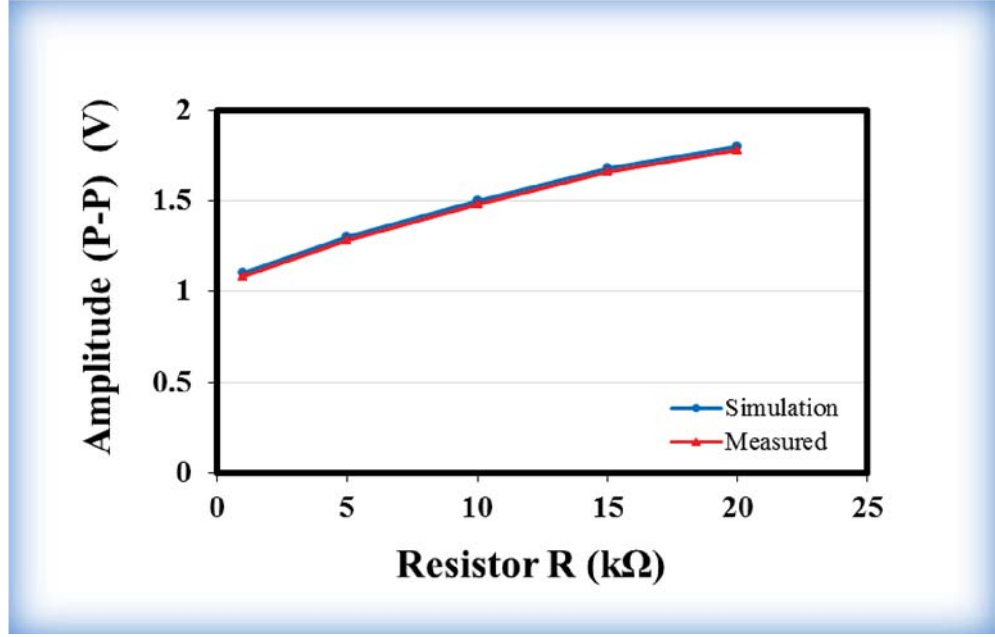
Figure 4.25. Measured chip outputs, (a) square waveform of the core WFG<sub>INT</sub>, (b) FFT spectrum analysis of the generated square waveform signal, (c) triangular waveform of the integrator, and (d) clock and clock\_bar translation outputs.

#### 4.8.1 Amplitude Control of The WFG<sub>INT</sub>

The chip was tested to determine the amplitude control behaviour. The peak-to-peak output voltage can be monotonically controlled by either the bias current  $IB3$  or the resistor  $R$  as per the theoretical analysis. Figure 4.26 (a) and (b) show the results of the measured amplitude control and its comparison with the simulation. For measurements,  $IB3$  variation is achieved through gate-voltage  $V_{\text{tune}}$  using direct DC voltage source and the variation of  $R$  through external resistance at the accessible terminal (I/O pad) to form a composite variable  $R$  element. The amplitude (P-P) of the measured square waveform varies from 1.2V to 1.8V (for fixed  $R=10\text{k}\Omega$ ) with  $IB3$  variation between  $20\mu\text{A}$  to  $60\mu\text{A}$  (equivalent  $V_{\text{tune}}$  variation between  $-0.88\text{V}$  to  $-0.695\text{V}$ ). On the other hand, amplitude (P-P) variation of 1.1V to 1.8V (for fixed  $IB3=33\mu\text{A}$ ) can be achieved with  $R$  variation between  $1\text{k}\Omega$  to  $20\text{k}\Omega$ . The simulated and measured profiles are almost co-incident. The results confirm that the output voltage of the WFG<sub>INT</sub> is controllable by the bias current  $IB3$  as well as by the resistor  $R$ .



(a) Amplitude (P-P) variation with  $V_{\text{tune}}$  bias current  $IB3$ .



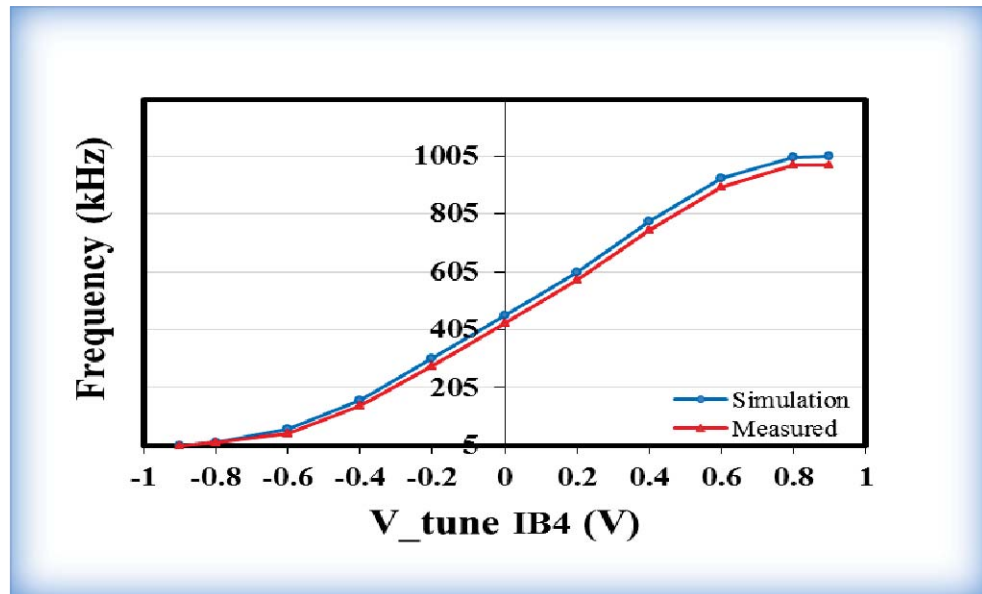
(b) Amplitude (P-P) variation with  $R$ .

Figure 4.26. Amplitude (P-P) variation comparing measured results and simulation of the core WFG<sub>INT</sub>, (a) with  $V_{\text{tune}}$  bias current  $IB3$ , and, (b) with  $R$ .

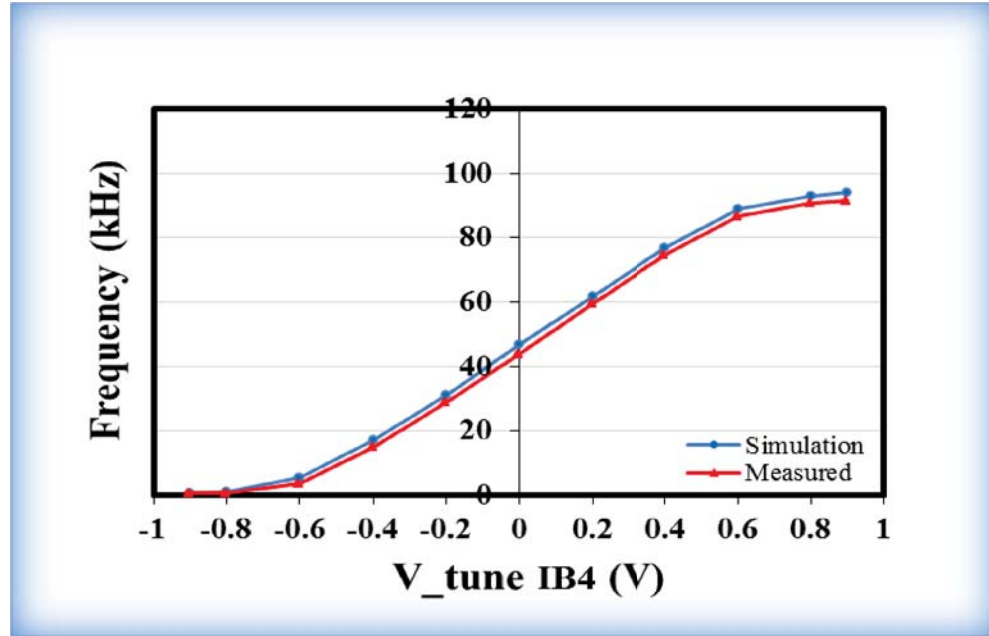
#### 4.8.2 Frequency Control of The WFG<sub>ING</sub>

The circuit was also tested to determine the frequency tunability. The output signal frequency can be controlled independently as per (4.26) by adjusting the bias current  $IB4$  of the gm-cell through tuning voltage ( $V_{\text{tune}}$ ) of the bias device M15. In particular, the bias voltage ( $V_{\text{tune}}$ ) for the integrator (STG4) is pre-set to  $-0.808\text{V}$ , with the on-chip load capacitor of the integrator fixed at  $10\text{pF}$ . The WFG<sub>ING</sub> in this setting generated a square/triangular waveform with oscillation frequency of around  $17\text{kHz}$ . In order to verify the tunability, with respect to the gm-C tuning, simulations and measurements have been performed with different load capacitors. As  $V_{\text{tune}}$  is varied in the range  $\pm 0.9\text{V}$ , tuning ranges of  $5.3\text{kHz}$ - $1003\text{kHz}$ ,  $0.58\text{kHz}$ - $94\text{kHz}$  and  $58\text{Hz}$ - $10.6\text{kHz}$  can be achieved for  $10\text{pF}$ ,  $100\text{pF}$  and  $1000\text{pF}$  respectively. The variation of  $C$  is achieved using external capacitors at the accessible terminal (I/O pad) to form composite variable  $C$  elements. Figure 4.27 (a), (b), and (c) depicts the plot of the oscillation frequency vs.  $V_{\text{tune}}$ . These results validate the design in a wide frequency range with good linear range between  $-0.6\text{V}$  to  $+0.6\text{V}$ . The small variations between simulated and measured results are attributable to fabrication process-related deviation

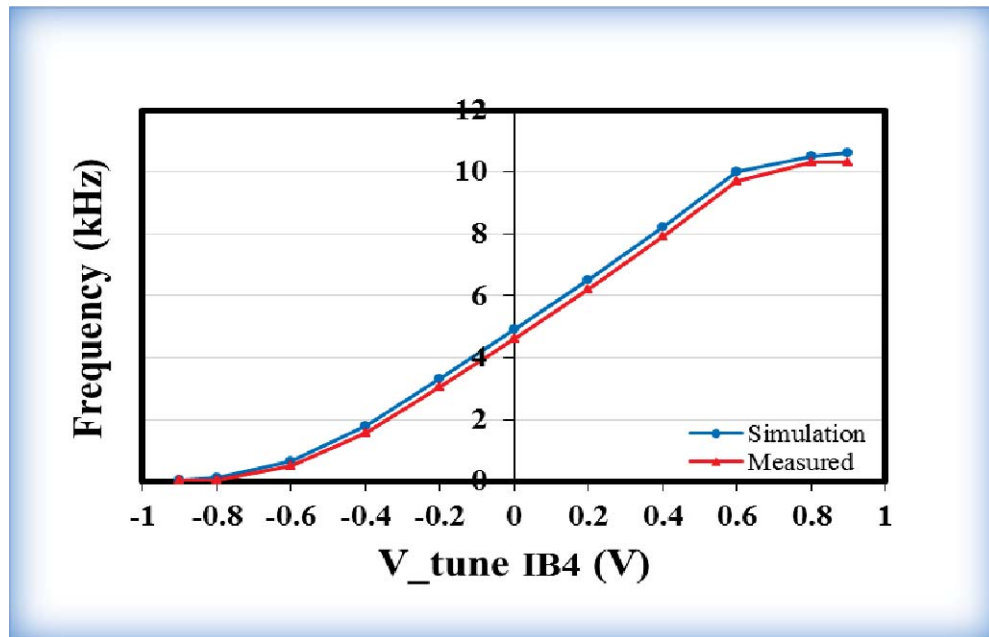
of passive components and also due to the output (and/or bias) DC current imbalances of the OTAs. For a bias voltage beyond  $\pm 0.6\text{V}$  the  $g_m$  of the integrator's differential pair (M7, M8) saturates since the tail device M15 enters the ohmic or the weak inversion region [58]. Hence the frequency variation also tends to saturate for  $V_{\text{tune}}$  beyond  $\pm 0.6\text{V}$ . On the other hand, a bias voltage above  $\pm 0.9\text{V}$  heralds the onset of signal distortions. These results indicate that a small DC bias current along with small  $W_{7,8}/L_{7,8}$  device ratio of the integrator, can accommodate a wide linear frequency tuning range along with low power consumption. Since the integrator frequency characteristic is determined by the  $g_m/C$  ratio, a wide tuning range can be achieved; in addition, process variation and temperature dependencies can be compensated by tuning the  $g_{m_{7,8}}$  of the integrator. Further, a much wider frequency range can also be provided through the FD digital block at the output of the PS circuit. For  $C=10\text{pF}$  the core  $\text{WFG}_{\text{INT}}$  can be tuned from 6.44kHz-to-1003kHz, and, in addition, a tuning range of 8.5kHz to 0.28Hz can be generated through the divide-by/2 FFs for the pre-set V-tune of  $-0.808\text{V}$ . As a result, the  $\text{WFG}_{\text{INT}}$  along with FD circuit provides two bands with a wide range of frequencies distributed from 6.44kHz-to-1003kHz (band I) and 0.1Hz to 502kHz (band II) which is extremely large. Table 4.3 summarizes the oscillator frequencies of the  $\text{WFG}_{\text{INT}}$  core (band I) for  $C=10\text{pF}$  with  $V_{\text{tune}}$  varied from  $-0.9\text{V}$  to  $+0.9\text{V}$  and the corresponding frequencies of the divide-by/2 FD circuit which can be digitally selected from 16 channels through the PS circuit (band II).



(a) Oscillation frequency vs. V-tune of the  $\text{WFG}_{\text{INT}}$  output signal for  $C=10\text{pF}$



(b) Oscillation frequency vs. V-tune of the WFG<sub>INT</sub> output signal for C=100pF



(c) Oscillation frequency vs. V-tune of the WFG<sub>INT</sub> output signal for C=1000pF

Figure 4.27. The measured profile values of the oscillation frequency vs. V-tune of the WFG<sub>INT</sub> output signal, compared with the simulation profile values and the related results for 10 pF, 100 pF and 1000 pF load capacitor values respectively.



Table 4.3. The tuning range of the oscillator frequency for the WFG<sub>INT</sub> core (band I) for C=10pF, with V-tune varied from -0.9V to +0.9V, and the equivalent oscillator frequency the circuit can provide, with 16 channel FD circuit (band II).

Tuning range of the oscillation frequency for C=10pF												
/2:Path selector (band II)	WFG <sub>INT</sub> core for V <sub>tune</sub> ± 0.9V (band I)											
	V <sub>tune</sub>	-0.9	-0.8	-0.6	-0.4	-0.2	0	0.2	0.4	0.6	0.8	0.9
	<i>f</i> (kHz)	6.44	17	63	160	204.8	455	605	777	927	995	1003
	<i>f</i> <sub>01</sub> (kHz)	3.22	8.5	31.5	80	102.4	228	303	389	464	497.5	502
	<i>f</i> <sub>02</sub> (kHz)	1.61	4.25	15.8	40	51.21	114	152	194	232	248.8	251
	<i>f</i> <sub>03</sub> (kHz)	0.81	2.12	7.9	20	25.6	57	76	97	116	124.4	126
	<i>f</i> <sub>04</sub> (kHz)	0.40	1.06	3.95	10	12.8	28.5	38	48.5	58	62.2	63
	<i>f</i> <sub>05</sub> (kHz)	0.2	0.53	1.98	5	6.4	14.25	19	24.25	29	31.1	31.5
	<i>f</i> <sub>06</sub> (kHz)	0.1	0.27	0.99	2.5	3.2	7.13	9.5	12.13	14.5	15.6	15.8
	<i>f</i> <sub>07</sub> (kHz)	0.05	0.132	0.495	1.25	1.6	3.57	4.75	6.1	7.3	7.8	7.9
	<i>f</i> <sub>08</sub> (kHz)	0.025	0.066	0.248	0.63	0.8	1.79	2.38	3.1	3.7	3.9	3.95
	<i>f</i> <sub>09</sub> (kHz)	0.013	0.033	0.124	0.32	0.4	0.895	1.19	1.55	1.85	1.95	1.98
	<i>f</i> <sub>10</sub> (Hz)	6.5	17	62	160	200	448	595	775	925	975	990
	<i>f</i> <sub>11</sub> (Hz)	3.2	8.5	31	80	100	224	298	388	463	487.5	495
	<i>f</i> <sub>12</sub> (Hz)	1.6	4.3	15.5	40	50	112	149	194	232	243.8	247.5
	<i>f</i> <sub>13</sub> (Hz)	0.8	2.2	7.75	20	25	56	74.5	97	116	122	123.8
	<i>f</i> <sub>14</sub> (Hz)	0.4	1.1	3.88	10	12.5	28	37.3	48.5	58	61	61.9
	<i>f</i> <sub>15</sub> (Hz)	0.2	0.55	1.94	5	6.25	14	18.7	24.3	29	30.5	30.95
	<i>f</i> <sub>16</sub> (Hz)	0.1	0.28	0.97	2.5	3.3	7	9.35	12.2	14.5	15.3	15.48

## 4.9 Optimization Flowchart of The WFG<sub>INT</sub>

Figure 4.28 illustrates and summarizes the design flowchart of the system. The circuit design process is comprised of defining circuit specifications and criteria, designing the topology, performing theoretical analyses and schematics, simulation and performance analyses, layout design, prototype fabrication, and finally, experimental testing and evaluation. The optimal design performances, transistor dimensions and passive component values for proposed analog WFG<sub>INT</sub> and the digital FD circuit are obtained, based on iterative simulation results. The required system specifications are the result of trade-offs made between performance, power, silicon area and cost. The design process parameters of WFG<sub>INT</sub>, clk and clk\_bar, D-FFs and MUX with PS circuits are specified in Step 3, Step 7 and Step 11, respectively. While Step 4, Step 8 and Step 12 obtain their optimal design constraint parameters based on iterative simulation results of the designed process parameters. Step 6, Step 10 and Step 14 check whether the designed circuits do function properly and comply with the required system specifications and the constraints. If the circuit performance test is not passed, the process returns to process parameters Steps (Step 3, Step 7 and Step 11) and then returns to the constraints parameters Steps (Step 4, Step 8 and Step 12). If it is passed, the process moves to the layout Step 15. If it is not passed, the process returns to Step 15. If it is passed, the designed layout moves to the prototype fabrication, Step 17, then the completed design circuit is sent to fabricate the chip. In Step 18, experimental test is set up and the experimental model of the electronic circuit is placed on a solderless breadboard to evaluate and verify the output signal of the fabricated chip, and compare its characteristics with the simulation results. If it passes, the process comes to an end.

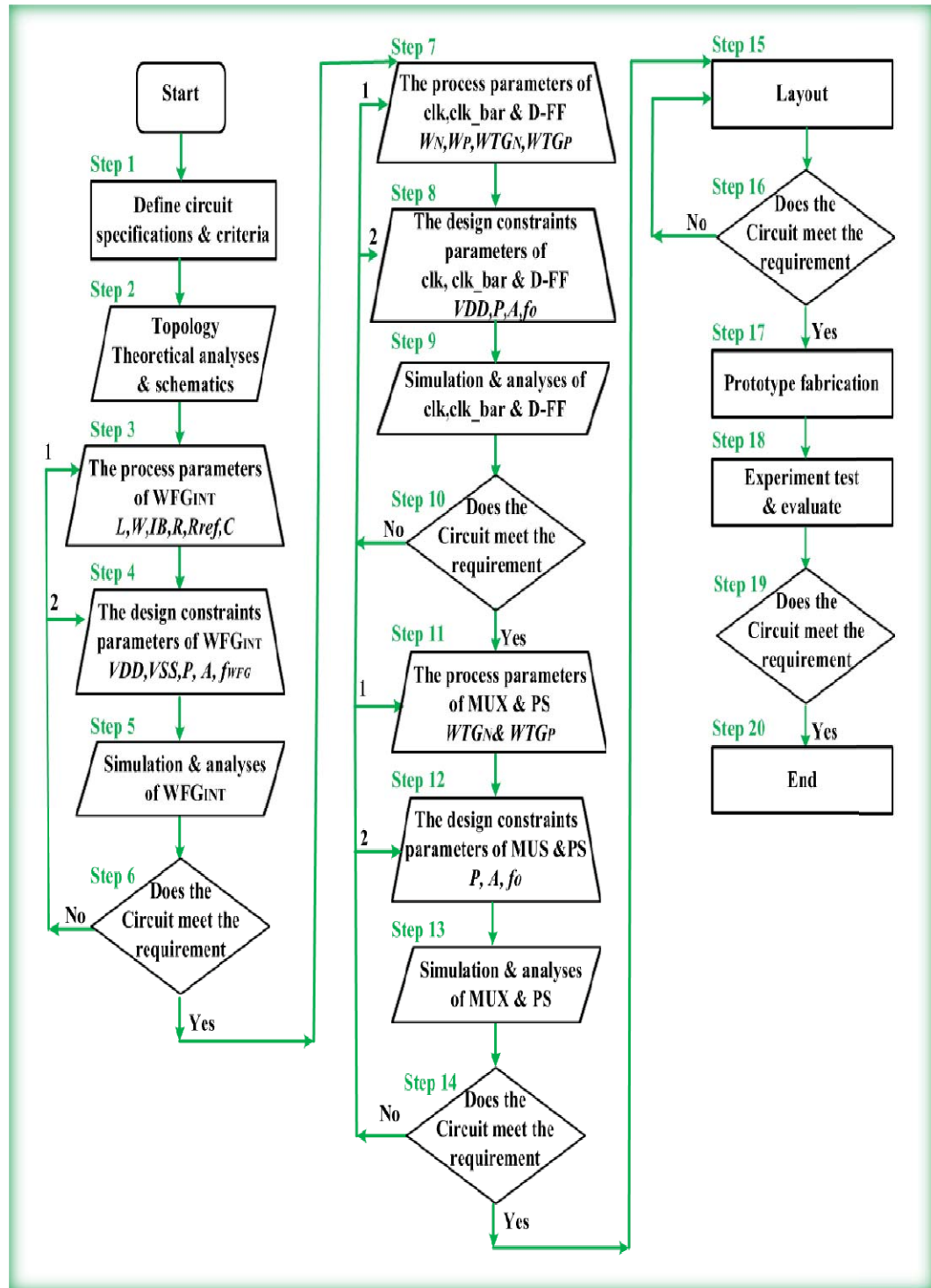


Figure 4.28. Optimization flowchart of the designed CMOS dual-band 16-channel mixed-signal waveform generator.

#### 4.10 Comparison of The WFG<sub>INT</sub> With ELF WFG and With Other Published WFG

A comparison of the fabricated WFG<sub>INT</sub> with ELF WFG of this work and with some recently reported literature [76, 86, 104, 106, 107, 116, 118] is provided in Table 4.4. Indeed, the fabricated WFG<sub>INT</sub> and ELF WFG of this work is state-of-the-art in terms of the low frequency design, a wide frequency tuning range and low micro-power consumption which compares well with the work of others. However, the fabricated WFG<sub>INT</sub> design, which is implemented fully on chip, utilizes a small resistor and small capacitor values to generate a low frequency output signal of 17kHz with lower power consumption compared to the two CMOS ELF WFGs, while for the two CMOS ELF WFG, ultralow frequency of 3.9Hz is achieved, utilizing off-chip large capacitor values to limit the overall passive element area. In addition the fabricated WFG<sub>INT</sub> can provide a wide frequency range with good linearity, and the oscillator frequency of the WFG<sub>INT</sub> core can be controlled independently and modified electronically by adjusting the bias current of the integrator building block. Comparing this with the ELF WFG, including the two CMOS ELF WFGs, wide frequency tuning is achieved only through the relaxation mechanism using  $R2$ , which is more suitable than using the bias current.

However, the fabricated WFG<sub>INT</sub> and the two CMOS ELF WFG are capable of providing a low oscillator frequency that utilizes a lower active and passive components account, with lower power consumption, compared to the previously reported waveform generator designs. Table 4.4 also shows a summary of the frequency tuning range with previously reported WFG designs, indicating that the fabricated WFG<sub>INT</sub> and the two CMOS ELF WFG design can provide a wider frequency tuning range than the reported WFG designs. The result clearly indicates that the proposed WFG<sub>INT</sub> design achieves the widest frequency range, as well as the lowest frequency which is digitally selectable. Also, the proposed design is fully CMOS integrated, achieving the most optimized power dissipation compared to the other designs in the table. It is evident that the fabricated WFG<sub>INT</sub> and ELF WFG of this work are simple and compact structures, considered as a power-efficient and small chip area solution, with low cost, for the longer battery life biomedical device, compared with a number of other architectures.



## 4.11 Conclusion

In this chapter, a novel mixed-signal low-power dual-band square/triangular waveform generator chip with a wide low-frequency tuning range has been presented. The proposed WFG<sub>INT</sub> based on a CM electronically tuneable relaxation oscillator comprising a hysteresis Schmitt Trigger and a timing gm-C integrator network circuit, along with a digital model utilizing divide/2 FD stages and PS output for driving an electrode, from 16 selectable channels. It has been designed and fabricated as an integrated solution at transistor level using 130-nm IBM CMOS technology with low supply voltage of  $\pm 1\text{V}$  for the core oscillator, while the digital model is designed to work at the lower supply voltage of only  $+1\text{V}$ . The WFG<sub>INT</sub> provides an output of around  $1.5\text{ V}_{\text{p-p}}$  at a nominal low oscillation frequency of  $17\text{ kHz}$  using small-size on-chip passive components with values of only  $10\text{ k}\Omega$  and  $10\text{ pF}$  for the positive feedback resistor and load capacitor respectively, to reduce the chip area. A model for a  $10\text{ pF}$  MIM capacitor has been designed to optimize the on-chip capacitor dimension and function. With a low frequencies timing network that is realized by implementing the gm-C integrator approach, the demand is reduced to that of designing an integrator with small  $gm$  and small capacitor value, to eliminate the need for large resistors and capacitors. The tuning of the gm-C integrator which utilizes the bias current to the frequency scale gm-C integrator is also promising and is achieved with simple tuning circuitry. Accordingly, the gm-C integrator approach is the most preferred for a fully implemented electronically tuneable circuit. The prevailing advantage of the gm-C technique is that its  $gm$  can be designed using a small  $(W/L)$  ratio for low frequency applications and can be controlled directly by the biasing current.

The robustness of the WFG<sub>INT</sub> circuit was investigated, the results indicating ideal circuit performance. Simulations and measurement results validate the designed circuit capability to work in a wide amplitude and frequency range. The amplitude (P-P) variation of  $1.1\text{V}$  to  $1.8\text{V}$  and  $1.2\text{V}$  to  $1.8\text{V}$  can be achieved with  $R$  and  $IB3$  variation between  $1\text{ k}\Omega$  to  $20\text{ k}\Omega$  and  $20\mu\text{A}$  to  $60\mu\text{A}$  respectively. The oscillator frequency of the WFG<sub>INT</sub> core (band I) can be tuned electronically from  $6.44\text{ kHz}$  up to  $1003\text{ kHz}$  with good linearity, by adjusting the DC bias current, while a lower frequency range (band II) of  $8.5\text{ kHz}$  to  $0.28\text{ Hz}$  can be produced by using divide /2 stages for the pre-set  $V_{\text{tune}}$  of  $-0.808\text{V}$ . As a result, the WFG<sub>INT</sub> core and the FD circuit generate two bands

with a wide range of frequencies distributed from 6.44 to 1003kHz (band I) and 0.1Hz to 502kHz (band II), which is extremely large. This ideal connection can be precisely switched in the fastest possible time.

The design of the device sizes and biasing currents of the WFG<sub>INT</sub> as well as the FD circuit is selected to meet certain design requirements, including low speed, low power, and a large output swing with small silicon area. The optimal design performances, transistor dimensions and passive component values for the proposed analog WFG<sub>INT</sub> and the digital FD circuit are the result of trade-offs made between performance, power, and silicon area. Predominantly, to minimize power and silicon area consumption of the WFG<sub>INT</sub>, low biasing currents and minimum size devices are used, while the power and silicon area of the CMOS logic gate is scaled up or down simply by using the “ratioid” technique and by modifying the  $W/L$  ratios of the NMOS and PMOS transistors respectively. Taking the size and the regularity of the implemented device into account, to optimize the layout for size, and to minimize the chip area, remarkably low power consumption of only 2.557mW was achieved and area occupation of only 18426 $\mu\text{m}^2$ , showing that this approach steers the design more appropriately towards the attainment of miniaturization and energy efficiency in the high density VLSI design. The circuit provides square/triangular waveforms along with its complementary signal for low-frequency electrical stimulation applications. This low power WFG is particularly important for battery-operated biomedical devices, enabling the reduction of the overall system cost. This novel mixed-signal dual-band WFG<sub>INT</sub> is published in IEEE Access Journal. The published manuscript is included in the Appendices section of this thesis. Bio-electric stimulation experimentation using this WFG<sub>INT</sub> can be carried out through an active electrode in contact with low-resistance skin surface. The design analysis and fabrication of the active electrode will be presented in the next chapter.



## **Chapter 5**

# **Design Criteria, Implementation and Fabrication of A Low-Power CMOS Active-Electrode-Pair for Low-Frequency Multi-channel Biomedical Stimulation**

### **5.1 Introduction**

The concept of this project is to develop a non-invasive electro-medical treatment device which can generate, control and deliver an appropriate mild electrical current in a specifically controlled fashion, using an electrode, through the low-resistance skin surface to a patient's blood. This concept involves the interface between the electronic signal and the biological components and how electronic devices and circuitry directly communicate with the electroactive biomolecule system. Living organisms manifest naturally inherent electrical activity which is a common feature of biological cells and tissues. Therefore, the interfacing of electronic devices with biomolecules is used to transmit signals through the conductive skin. For that to be possible, it is important that the interface between the electronic systems and the biological is effective, with the control of the electronic device acting on the biological media in order to produce an effective signal transfer. The electrode is an important component in biomedical applications providing signal-transfer between the biomedical device and the living body, using the conductivity of the skin; it is, therefore, necessary for the communication network between the biomedical device and the body. The energy transfer from electronic interaction with bio-molecules at the electrode interface is used to transmit signals through the conductive skin. In most electro-bio-stimulation applications voltage or current is introduced through electrode contact with the skin.

Skin impedance is the primary factor that affects the flow of the applied electrical signal to the body; overcoming this impedance is important in such applications. The skin comprises three layers: epidermis, dermis and subcutaneous layer as shown in Figure 5.1. The most important layer is the epidermis output layer that contains the Stratum Corneum (SC) which is the foremost contact with the electrode. It

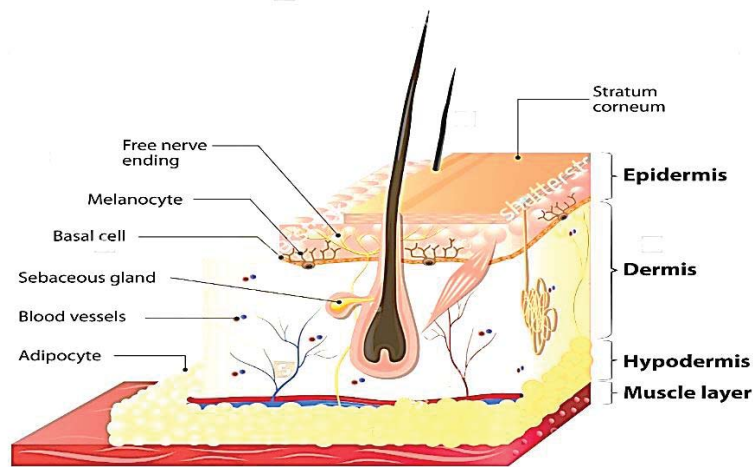


Figure 5.1. A schematic of the cross-section of human skin showing the various layers within skin [201].

consists of dead cells, and thus acts as a barrier to electrical activity. The deep skin layer is composed of living cells that divide and grow, consisting mainly of blood vessels (which provide blood to the epidermis), the nerves responsible for sensations, and a liquid comparable to an electrolyte, constituting an electrically conductive layer [202]. An early electrical model to study the intact skin impedance in response to an electrical signal, was developed in [203-205] and the linear equivalent electrical model to study skin response to a constant square wave DC voltage stimulation pulse was developed in [206-208] as shown in Figure. 5.2 (a).  $R_p$  and  $C_p$  represent the resistance and capacitance of the intact skin impedance. The series resistor  $R_s$  attempts to model the resistance of the various conductive tissues in the core. Figure 5.2 (b) shows the current flowing through the untreated skin in response to a square pulse voltaic stimulation. The response is an initial current spike, which is a capacitive charging current, due to the fast rising edge of the voltage pulse. Once the capacitance is fully charged, it decays to a value limited by the  $R_s + R_p$ . This study demonstrated that when the SC is removed, the frequency dependent parallel combination of  $R_p$  and  $C_p$  ( $X_p = 1/2\pi f C_p$ ) is almost eliminated, and the series resistance  $R_s$  tends to dominate. Thus the output current in Figure 5.2. (c) is mostly limited by  $R_s$  only; it is a square wave with a higher peak than that obtained with untreated skin. Skin preparation, therefore, can decrease the low frequency skin impedance, while it has not much effect on the high frequency skin impedance (due to capacitive shorting).

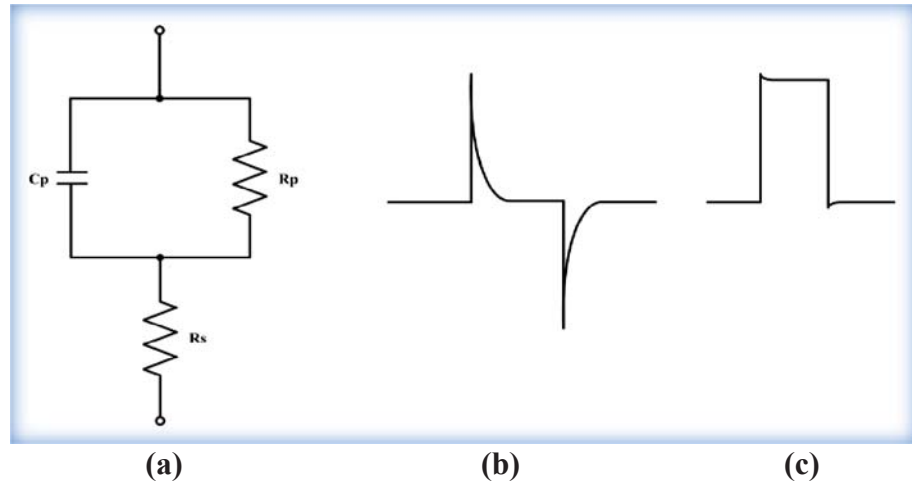


Fig.5.2. Current response of skin to the application of a square-wave voltage pulse, (a) skin electrical model, parallel components  $R_p$  and  $C_p$  models the resistance and capacitance of the intact skin impedance, while the series element  $R_s$  models the resistance of the conductive deep tissue (skin core), (b) response of intact-skin, the initial current spike through the untreated skin, and (c) response after Stratum Corneum is removed (treated skin), whereby  $R_p$  and  $C_p$  is almost eliminated, the series resistance  $R_s$  now dominates, and a square wave current pulse with a higher peak than that with untreated skin is obtained [209].

This study also demonstrated that the skin impedance is inversely proportional to the contact area, with a different value for wet and dry skin. For sweaty or saline-soaked skin with a large electrode–skin contact area, the low frequency skin-impedance is typically  $1000\Omega$ , with the internal (core) skin impedance in the range of  $500$  to  $700\Omega$  [209]. However, since skin is a composite of different types of cells, and is affected considerably by environmental and physiological factors, the skin impedance is nonlinear and time-variant. Hence, using conductive gel that induces high ion concentration, the resistive skin impedance can be reduced, while, using a large contact area ( $A$ ) along with a small electrode separation ( $d$ ) the capacitive skin impedance ( $C = \epsilon A/d$ ) can be reduced [210] ; thus eliminating the need for abrasion of the SC. As previously mentioned in section (2.9) the conventional electrode is a common transducer which uses simple surface electrodes and a passive metallic disc with wire connected to the bio-signal amplifier. The conventional passive electrodes have a significant detrimental effect on the purity of signal transmission, because the external

interference with the signal line involves the electrode wire (and its movement) and the power line interference. Another drawback of using passive electrodes is that a short circuit may occur between adjacent electrodes. A good quality signal can be transmitted by using an active electrode with buffer amplifier, located as close to the transducers as possible. This has advantages compared with the common passive electrode architecture and with reported active electrode approaches. The active electrode eliminates the problems arising from cable and environmental interference, while mounting the entire IC signal processing system, including signal source and active electrode circuitry, on the electrodes (transducers), makes the fabrication less complex and more compact by reducing the number of power supply lines and signal line wires, and minimizing the signal path between the electronics system and the patient's body.

The aim of this work is to design a compact high performance circuit for the signal buffering task, with low power drain, and to transmit a superior quality signal by shielding mains interference. In addition to the buffering task, simple buffer architecture with the desired attributes that have a small transistor count, while achieving large driving capability at low power consumption, is also an attractive feature of the proposed active electrode circuit. On the other hand, an appropriate electrical signal can be applied to the body in two modes: monophasic or biphasic. This is dependent on the applications. However biphasic mode would fulfil the requirements of this research project and the FDA clinical criteria requiring equal positive and negative charge to the electrode, so that no DC charge is accumulated on the body, since imbalance in net charge can produce toxic effects in the tissue [3].

The source input stimulation signal can be in digital or analog mode. However, in analog mode, different signal-shapes, such as exponential, triangular and square waveforms, can be applied for a particular biomedical application. A portable biomedical device for electrical stimulation requires state-of-the-art circuit implementation, with high performance and a low power active electrode IC to provide effective signal transfer. The main factors that are considered in this work in designing an active electrode are reliability, power consumption, electrode active area and the number of wires required for an effective signal transfer. This chapter presents an IC integrating two identical active electrode circuits employing buffer amplifiers that deliver appropriate biphasic square waveforms, so as to improve signal quality as well as ensure charge balancing on an electrode-skin site. In addition, it reduces the number

of wires required which results in an improved signal source localization. The outline of this chapter is as follows: section (5.2) presents the design criteria of a novel active electrode. An overview of the active electrode IC design and topology will be described in section (5.3). Simulation and performance analyses of the active electrode are presented in (5.4). Section (5.5) provides the layout and fabrication results. Conclusions are drawn in section 5.6.

## **5.2 Design Criteria for The Active Electrode**

The novelty of the proposed design is a compact active electrode employing an adaptively biased buffer, fabricated in 130-nm CMOS, with overall low power dissipation. The present movement in the designed active electrode circuit is to:

1. Use new 130-nm CMOS technology with low supply voltage of only 1.2V.
2. The present design employs adaptive bias current technique, to provide an appropriate large output current driving capability and to reduce power consumption which is compatible with the requirement of the biomedical applications of this work. Another advantage of using adaptive technique is that the negative feedback in the buffer circuit with adaptive biasing can work like control switches that prevent the flow of the output current from becoming very large.
3. Decrease the numbers of MOSFETs devices to reduce chip area without degrading the performance of the circuit. The designed buffer circuit is compact using nine MOSFETs transistors including the output stage that provides large output current with respect to the reported buffer structures.
4. The designed buffer circuit can be used for two modes of operation, monophasic or biphasic mode.
5. The complete processed two chips of signal-processing circuitry, involving the mixed-signal WFG<sub>INT</sub>, two identical active electrodes, power supply circuitry with free energy solar rechargeable battery, and biological interfacing device will be mounted together on a custom-designed printed-circuit board (PCB) if wire bonding is available. The goal is to lay the complete electronics system as closely as possible to the body thus a good quality signal can be transmitted, by reducing the sensitivity to cable and environmental interference. Mounting all IC signal-processing circuitry

on the electrodes (transducers) to complete the encapsulated bio-medical device with electrode contacts features, makes it easy and quick to attach and remove from the skin.

### 5.3 Circuit Design and Topology of The Active Electrode

The schematic diagram of the proposed CMOS active electrode, designed in 130-nm CMOS, and the buffer circuit symbol representing the voltage follower active electrode circuit is shown in Figure 5.3 (a) and (b).

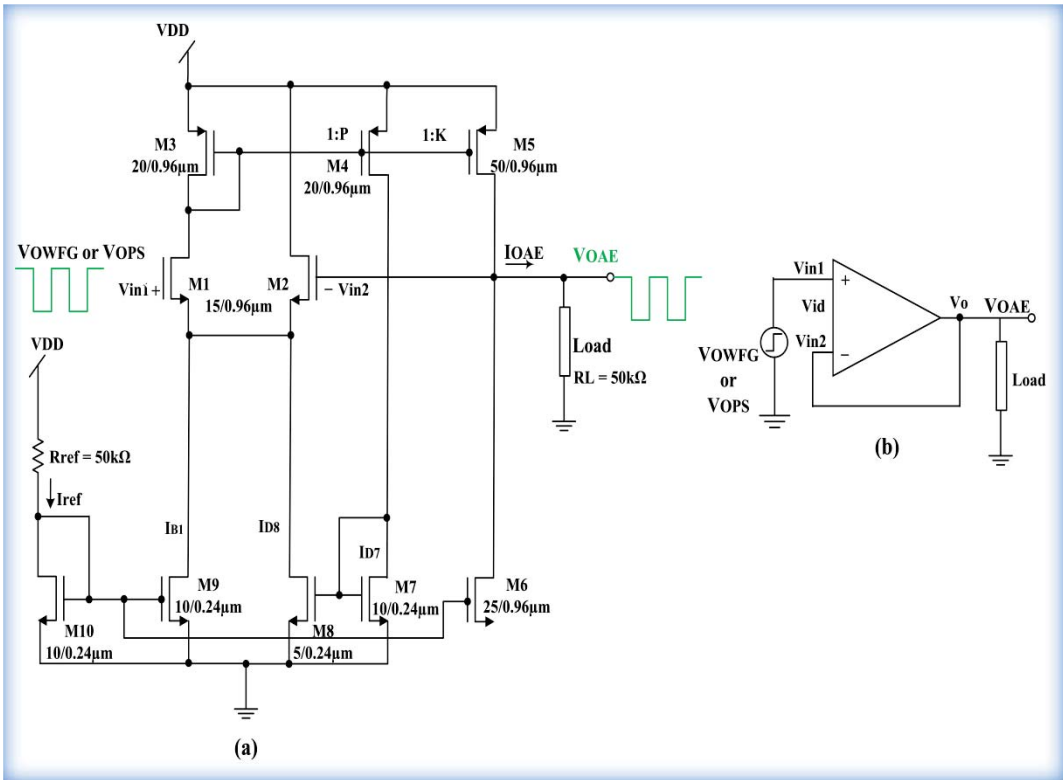


Figure 5.3. Proposed adaptive biased CMOS active electrode circuit, (a) circuit implementation, with input stage bias current set dynamically by two mechanisms, first, by the simple current mirror and secondly, by applying adaptive biasing, and (b) equivalent circuit representing the voltage follower active electrode circuit.

Each active electrode is realized as a CMOS buffer circuit, based on an adaptive voltage follower amplifier. It is configured from a NMOS differential input pair [M1, M2] along with a PMOS diode load M3. Its output ( $V_{OAE}$ ) is connected back to the gate of M2 to form a unity gain voltage follower. The output stage consists of PMOS mirror device M5 reflecting current from PMOS M3 (with a mirror factor  $K$ ), and, loaded by the current source NMOS device, M6. Bias current for the input stage is set dynamically by two mechanisms: first, by the simple current mirror configuration formed by resistor  $R_{ref}$  and NMOS devices [M10, M9], and secondly, by applying an adaptive biasing configuration formed by PMOS mirror pair [M3, M4] (with a mirror factor  $P$ ) in conjunction with an NMOS recycling mirror pair [M7, M8]. The differential pair's DC tail current is just  $IBI$  while the adaptive biasing current is  $ID8$ . The designed buffer circuit, using this adaptive biasing, can source a large current to drive the electrode element with low power consumption.

### 5.3.1 Active Electrode Circuit Analysis

The buffer circuit in Figure 5.3 (b) shows that  $V_{in1} - V_{id} = V_o$ , along a KVL loop. Considering close-to-ideal behaviour (very large input impedance),  $V_{id}$  is equal to zero, so that,  $V_{in1} = V_o$ , and the closed loop gain is  $A_v = 1$ . The buffer circuit that provides unity gain has infinite input resistance and low output resistance, can thus provide impedance and DC level translation, with no loss of signal voltage level [52]. Since the composite electrode-skin impedance varies with electrode material, size and environment [186], a buffer with adaptive biasing configuration can provide an appropriate large variable current at the output stage to drive the load [66]. In order to deliver a large output current, biasing current  $IB$  must be made larger for a larger input voltage [59]. The input voltage ( $V_{in1}$ ) is considered loaded by the output of the dual-band waveform generator (WFG<sub>INT</sub>) that was previously developed in chapter 4 for this research project, whose 16 selectable channels can be used for a monophasic or biphasic active electrode signal. The basic concept of an adaptively biased circuit can be explained through Figure 5.3 (a). As a unity gain buffer amplifier, its output  $V_{OAE}$  is connected to the inverting input  $V_{in2}$  and the input signal is applied through the non-inverting terminal  $V_{in1}$ . In normal operation without the use of adaptive biasing circuit and without signal input, the maximum output current the circuit can deliver is limited to  $K \cdot (IBI/2)$ , and the slew rate,  $SR = K \cdot (IBI/2 \text{ C})$  with  $C$  being a composite capacitive



output load. When  $V_{in1}$  increases by a large  $\Delta V$ , M2 turns off and M1 is carrying most of the bias current. In order to deliver a large output current,  $IB1$  or the current mirror ratio  $K$  must be increased. An increase in  $IB1$  leads to an increase in power dissipation, while a large  $K$  value results in a device with a large gate area and hence a large die area [58]. There is thus a trade-off, and an adaptive bias circuit with an appropriately small  $K$  value, can be employed to boost the delivered output current. If  $V_{in1}$  and  $V_{OAE}$  are equal, the current that flows into M1 and M2 is  $= IB1 + ID8$ . When the circuit experiences a large  $\Delta V$  at  $V_{in1}$ , it automatically boosts the bias current that can be harnessed. Suppose initially,  $V_{in1}$  is high, and the circuit senses a large  $\Delta V$ , M1 is then carrying most of the bias current and consequently the current through M1 reaches a maximum. Since the diode-connected M3 carries the same current as M1, the current mirror [M3, M4] forces  $ID3=ID4$  (for  $P=1$ ). It follows that  $ID7$  is also increased. This leads to an increase in the drain current,  $ID8$ , of M8 due to the current mirror action of [M7, M8] and is thus recycled as an increased biasing current which sinks (pulls down) the source voltage of the input pair [M1, M2]. Consequently, the current that is delivered to the output through the mirror action of [M3, M5] is significantly enhanced. The circuit can thus source large output current to drive the load. Sourcing a large output driving current can also be partly achieved by enlarging the width of the output stage device M5 (increasing  $K$ ). For driving capacitive loads, choosing an appropriate value for  $K$  can eliminate any slew-rate limitations. It is worthwhile to mention here that in the case of a large bias current, M1 along with the devices M3-M8 remains in saturation, while this current recycling continues, and increases by mirror factor  $K$ , resulting in a large output current. As  $V_{OAE}$  rises, the differential input voltage  $V_{id}$  ( $V_{id} = V_{in1} - V_{OAE}$ ) will decrease until  $V_{in2}$  eventually approaches  $V_{in1}$ ; the circuit then returns from slewing to linear operation, using the unity-gain negative feedback path of the buffer. With rising  $V_{OAE}$  ( $V_{in2}$ ), however, proportionate bias current gets diverted into M2 from M1 resulting in a reduced mirror current into M5 via the mirror pair [M3, M5]. The adaptively biased buffer circuit thus works also as an output current control mechanism. However, if the biasing current is increased too much, the gain of the differential input pair may decrease and become insufficient. The closed loop gain of the buffer configuration is well known, and for large open loop gain ( $A_V$ ) it can be given by,

$$A_{closed} = 1 - \frac{1}{A_V} \approx 1 \quad (5.1)$$

While, the  $A_V$  of the buffer circuit in Figure 5.3 (a), can be approximately derived as follows,

$$i_{out} = K \cdot i_{D1} = \frac{K \cdot g_{m1} \cdot V_{in}}{2} \quad (5.2)$$

Where,  $V_{in} = V_{in1} - V_{in2}$ , Since,

$$\frac{i_{D1}}{V_{in}} = \frac{g_{m1}}{2} \quad (5.3)$$

And,

$$\frac{i_{out}}{V_{in}} = \frac{K \cdot g_{m1}}{2} \quad (5.4)$$

So,

$$A_V = \frac{i_{out}}{V_{in}} \cdot R_{out} = \frac{K \cdot g_{m1}}{2} \cdot r_{o5} // r_{o6} \quad (5.5)$$

Where,  $g_{m1} = \sqrt{\mu_n C_{ox} \frac{W1}{L1} I_{D1}}$ , is the trans-conductance of M1, and  $R_{out} = r_{o5} // r_{o6}$  is the overall output impedance of the open loop circuit. Since the buffer circuit utilizes voltage (parallel) feedback at the output, the closed-loop output impedance  $R_{closed}$  of the active electrode buffer can be given by,

$$R_{closed} = \frac{R_{out}}{1+A_V} = \frac{r_{o5} // r_{o6}}{1 + \frac{K \cdot g_{m1}}{2} \cdot r_{o5} // r_{o6}} \approx \frac{2}{g_{m1}} \quad (5.6)$$

Equation (5.6) showing that the closed-loop output impedance is independent of the open-loop output impedance. For a specific design, this allows for implementing a high gain buffer circuit by increasing the open loop output impedance, while still realizing the required closed-loop output impedance for matching with the load. The open loop gain is directly proportional to the  $g_{m1}$  and  $r_{o5} // r_{o6}$ , while the closed-loop output impedance is inversely proportional to  $g_{m1}$ , as per (5.5) and (5.6) respectively. The trade-offs that occur are many, increasing the bias current and using small channel width devices, the open loop gain goes down while the unity gain frequency increases. On the other hand, using long channel length results in a larger open loop output resistance ( $r_{o} \propto L$ ) and hence, the desired large open loop gain, with low speed, can be

achieved. Thus, using large channel length for both M5 and M6, in conjunction with reasonable width for M1, both the open loop gain as well as the closed-loop output impedance can be optimized for the active electrode buffer. This shows that the adaptive biasing technique enables freedom in device sizing for a chosen bias current, so as to provide desired large output current, high open loop voltage gain, and reasonable output impedance along with low power consumption. Hence, the iterative simulation technique can be employed with possible sets of  $W$ ,  $L$  and  $IB$  (bias current) to optimize the performance of the designed active electrode circuit.

## 5.4 Simulation And Performance Analyses of The Active Electrode

The proposed active electrode-pair based on Figure 5.3 has been designed and simulated in 130-nm CMOS process technology with the supply voltage of 1.2V on Mentor Graphics Pyxis version 10. To achieve low power consumption and small silicon area, optimized device sizes and low supply voltage were utilized. An appropriate bias current was also considered for the device-size optimization in order to achieve high open-loop gain and low-frequency design, along-with the desired output current and output impedance. In order to analyze the performance, the  $WFG_{INT}$  output ( $V_{OPS}$  or  $V_{WFG}$ ) is applied to drive the active electrode. Based on an iterative simulation technique, optimal dimensions for devices in the differential pair and the current mirrors is achieved, as well as, an optimally small stand-by bias current. The devices [M1, M2] are sized by considering the open loop gain and the output impedances of the active electrode buffer. The widths for [M1, M2] are chosen to be  $W1=W2=15\mu\text{m}$ , along with reasonably large channel length  $L1=L2=0.96\mu\text{m}$ . The PMOS current mirror devices [M3, M4] are designed to have  $L3=L4=0.96\mu\text{m}$ , while a large channel width of  $W3=W4=20\mu\text{m}$  is chosen to minimize the value of  $V_{GS3,4}$ , resulting in a higher output-swing head-room. Also, using wide MOSFETs lowers the minimum voltage required  $|V_{DS} = V_{GS} - V_{TH}|$  to keep it in saturation at the cost of somewhat increased layout area [58]. Since a large output current is desired, the width of M5 is made larger than  $W3$  with  $W5 = 50\mu\text{m}$ , to account for the correspondingly larger mirror factor. This also decreased bandwidth due to the increase in parasitic capacitance that is associated with the buffer circuit output node [66]. M6 was chosen to have  $W6=25\mu\text{m}$ , which would be half of  $W5$ , due to the difference in the trans-conductance parameter ( $\mu_n C_{ox}$ ). On the

other hand, as per (5.5), using large channel lengths of  $L5 = L6 = 0.96 \mu\text{m}$  would increase the open loop output impedance which enhances the open loop gain. The current mirror [M7, M8] which harnesses additional bias current through M4 is sized to have  $L7 = L8 = 0.24 \mu\text{m}$ , while the widths are sized as  $W7 = 10 \mu\text{m}$  and  $W8 = 5 \mu\text{m}$ , respectively. The standby bias current mirror [M9, M10] is chosen to have  $W9 = W10 = 10 \mu\text{m}$ , and,  $L9 = L10 = 0.24 \mu\text{m}$ . By setting  $R_{ref}$  to  $50 \text{k}\Omega$  or  $10 \text{k}\Omega$ , and based on simulation, the bias current  $I_{B1}$  through [M9, M10] is around  $24 \mu\text{A}$  or  $120 \mu\text{A}$ , and the adaptive current  $I_{D8}$  is about  $34 \mu\text{A}$  or  $80 \mu\text{A}$ , while the load transistor M6 can provide bias current of around  $60 \mu\text{A}$  or  $300 \mu\text{A}$  respectively. On loading, when an input signal is applied (at  $V_{DD} = 1.2 \text{V}$  oxide breakdown limit), the active electrode buffer can provide output current of around  $145 \mu\text{A}$  or  $450 \mu\text{A}$  while consuming  $100.8 \mu\text{W}$  or  $504 \mu\text{W}$  respectively. In addition, the buffer provides a gain of  $\approx 1$  (using peak-to-peak signal voltages) by setting  $R_{ref}$  to  $50 \text{k}\Omega$ , and it is reduced to  $0.950$  by setting  $R_{ref}$  to  $10 \text{k}\Omega$ ; which is a trade-off of gain accuracy with resistor area. Figure 5.4 shows the simulated transient response of the active electrode circuit to a  $+1 \text{V}$  input pulse of  $100 \text{ ms}$  using load  $R_L$  of  $50 \text{ k}\Omega$ . For the electrical characterization, a large load of  $100 \text{k}\Omega$  was also used to verify the circuit performance under worst-case conditions.

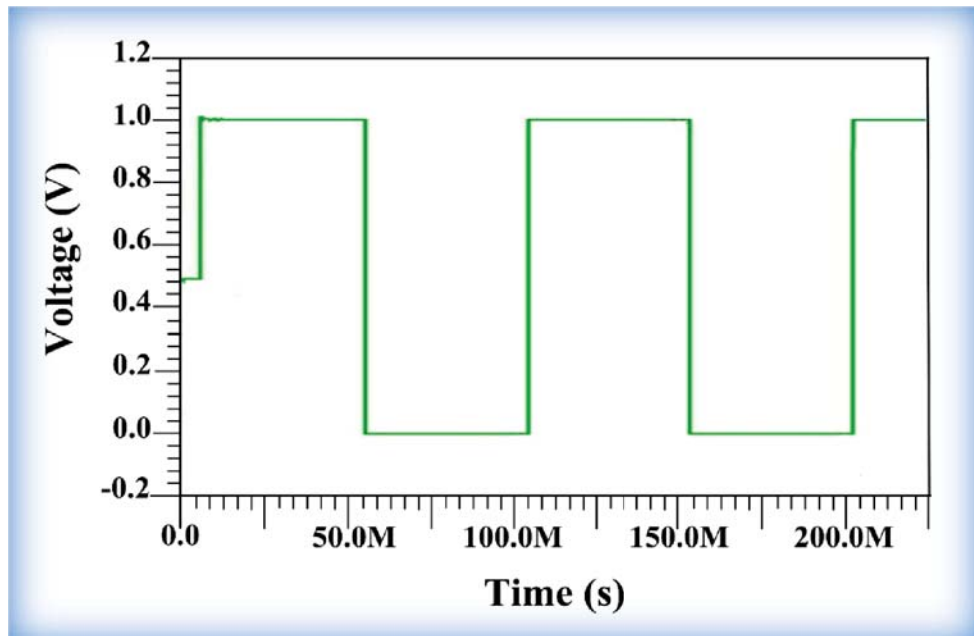


Figure 5.4. Simulated transient response of individual active electrode buffer to an input square-wave pulse of a  $100 \text{ ms}$  duration and  $+1 \text{V}$  amplitude (the  $V_{OPS}$  output of the PS in chapter 4) for  $R_L = 50 \text{k}\Omega$ .

The designed buffer is capable of providing high gain and high output current using new nm CMOS technology of 130-nm with the low supply voltage of only 1.2V, which is a distinctive design challenge.

To evaluate the performance based on analysis of the output waveform through an active electrode to the load which represents the equivalent skin contact impedance, the output of the WFG<sub>ING</sub> ( $V_{WFG}$  or  $V_{OPS}$ ) and its complementary pulse with 16 selected channels (band II) are fed into two identical active electrode circuits. Thus the load is driven in a differential fashion, using complementary active electrode circuits as shown in Figure 5.5. The performance requirement is to transmit a biphasic low frequency square waveform signal and deliver (at skin-electrode interface) a square waveform with an appropriate peak.

As previously mentioned in (section 5.1), since the composite skin impedance is nonlinear, time-variant, and consists of different variable impedance elements, it can be reduced and stabilized by improving the electrode-skin interface contact using high conductive gels as well as by increasing the contact area with the electrode (transducers). A square wave is delivered such that a higher peak can then be obtained, without removal of the Stratum Corneum. The voltage applied across the skin can be represented by the current flowing through a small resistor. Based on this assumption, the skin contact impedance can be modeled by the floating load resistor  $RL$  across the electrodes. Figure 5.6 (a) and (b), shows a biphasic square-wave stimulation pulse delivered to a 50 k $\Omega$  resistive load. The output voltage  $V_{out}$  swings in the range  $\approx \pm 1V$ :  $V_{out} \approx +1$  when  $V_{in}$  is high, and  $V_{out} \approx -1$  when  $V_{in}$  is low. This circuit can provide output current of about  $\pm 40 \mu A$  (peak-to-peak output current,  $I_{p-p}$ ) on  $\pm 1V$  stimulus, which is enough for the target application. The output voltage-swing is limited by the 130-nm technology that is used in this work. The monophasic performance of the active electrode circuit is also evaluated using a square waveform signal with 16 selected channels (band II), and the integrator triangle waveform signal (band I) with a wide range of frequencies. The output voltage  $V_{out}$  follows the input voltage and swings between  $\approx 0$  to  $+1V$ . The circuit can provide output current of around  $+16\mu A$ , for the same 50k $\Omega$  load resistor  $RL$  in a grounded configuration (connected in series to the output).

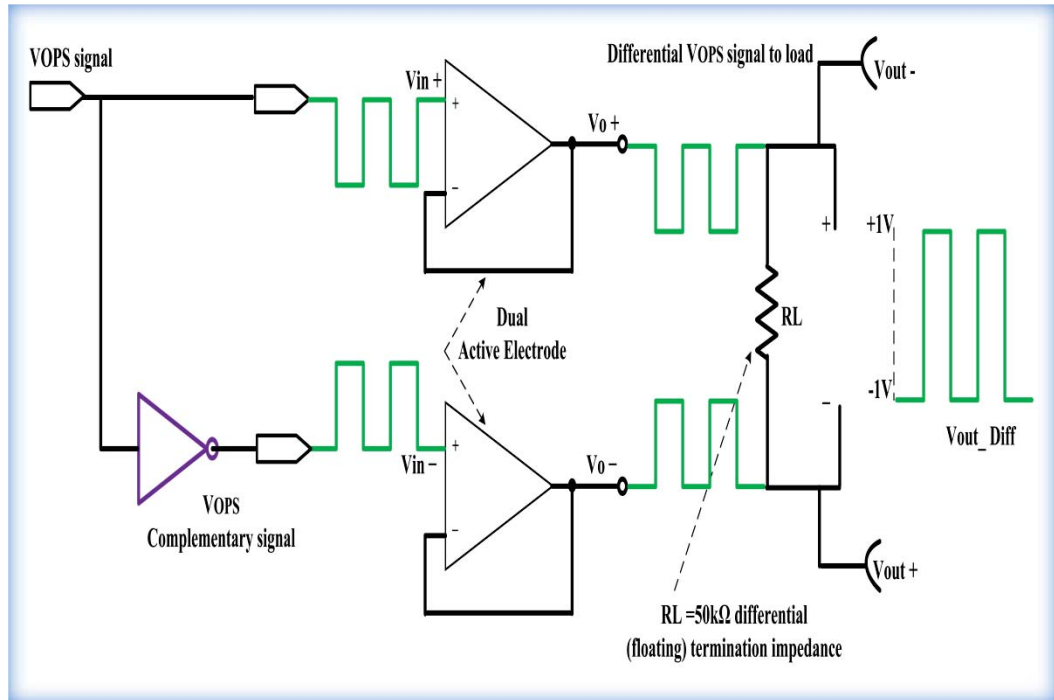
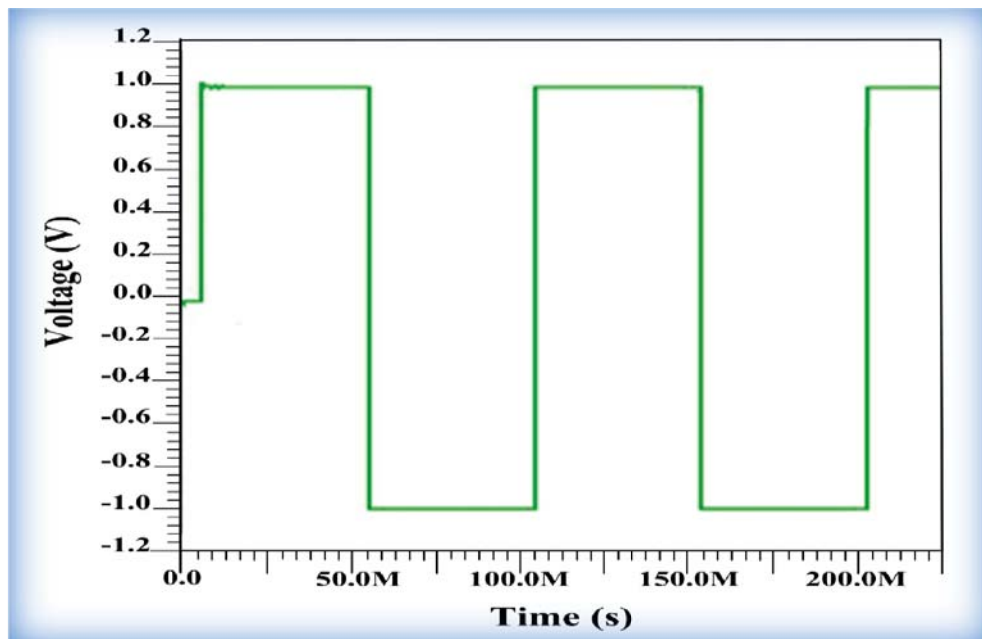
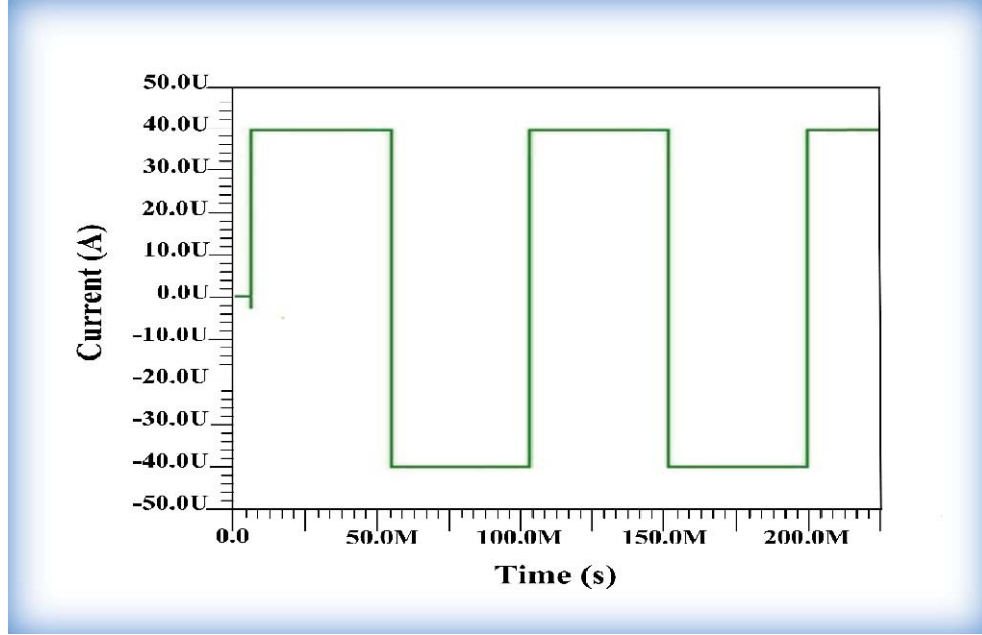


Figure 5.5. The configuration for bio-potentials signals application, employing two identical active electrodes. The  $V_{OPS}$  pulse output of the PS (chapter 4) and its complementary signal are fed to the dual active electrode inputs in order to drive differential  $V_{OPS}$  signal to load resistor  $R_L = 50k\Omega$  in a differential fashion equivalent to skin impedance.



(a)  $\pm 1V$  differential output voltage.



(b)  $\pm 40\mu\text{A}$  differential output current.

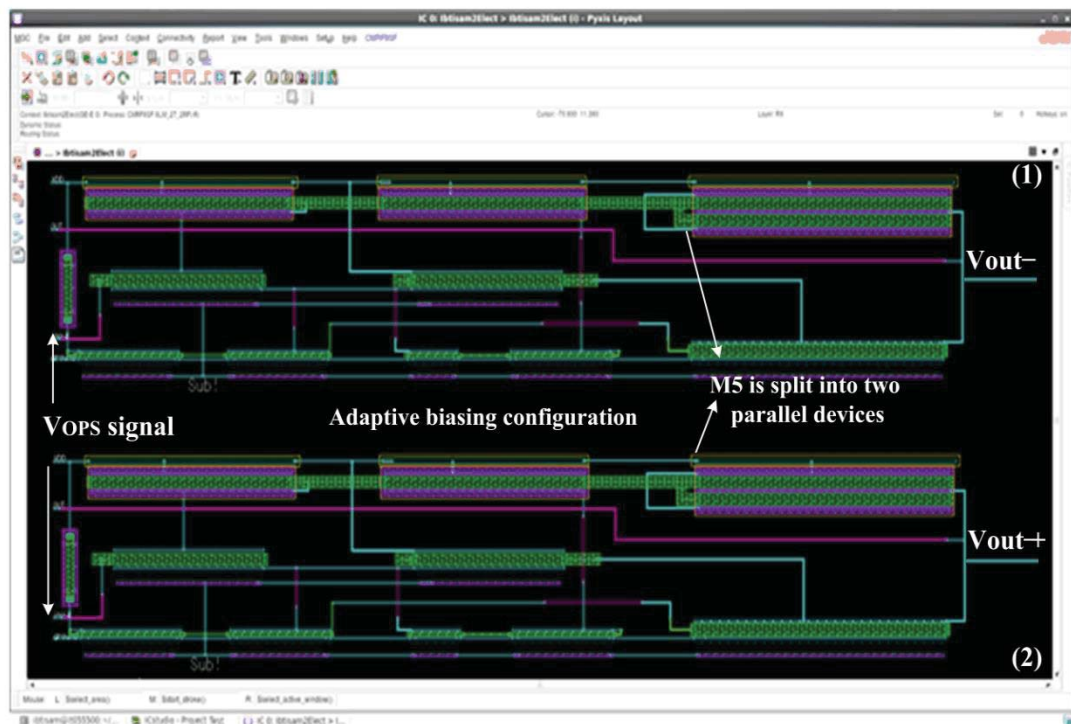
Figure 5.6. Simulated transient response of the dual active electrode circuit driving a  $50\text{k}\Omega$  floating load in a differential fashion displaying a transmitted bi-phase square waveform with, (a) approximately  $\pm 1\text{V}$  differential output voltage, and (b)  $\pm 40\mu\text{A}$  differential output current.

## 5.5 Layout and Fabrication of The Active Electrode

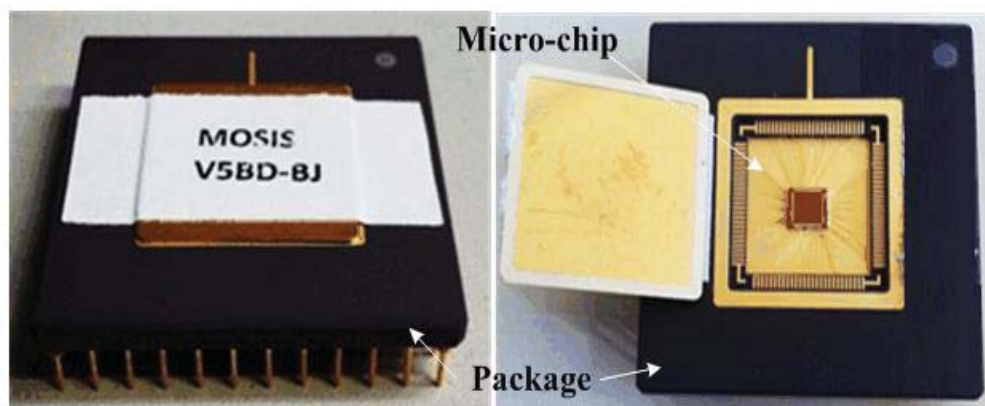
A prototype of the proposed active electrode circuit was fabricated in Global Foundries (GF) 8RF-DM 130-nm CMOS process through MOSIS. The dual electrode differential design occupies small chip-area of only  $2936.23\mu\text{m}^2$  ( $2 \times 1468.12\mu\text{m}^2$ , i.e. around  $0.00294\text{ mm}^2$ ). To minimize the thermal-gate resistance noise of the large devices, fingered poly-silicon gates are laid out. Thus, M5 is split into two parallel devices  $25\mu\text{m} / 0.96\mu\text{m}$  each, ensuring that the fingers are symmetrical. All devices are oriented in the same direction in order to yield better matching and minimized offsets [58]. The on-chip resistor  $R_{ref}$  is implemented using a p+ polysilicon OPRRP resistor (with sheet resistance of  $1700\Omega/\text{square}$ ) in this 130-nm CMOS process; the M1 metal layer is routed as the contact to the OPRRP resistor terminals [72]. To minimize the layout area, horizontal runs of metal are applied to provide



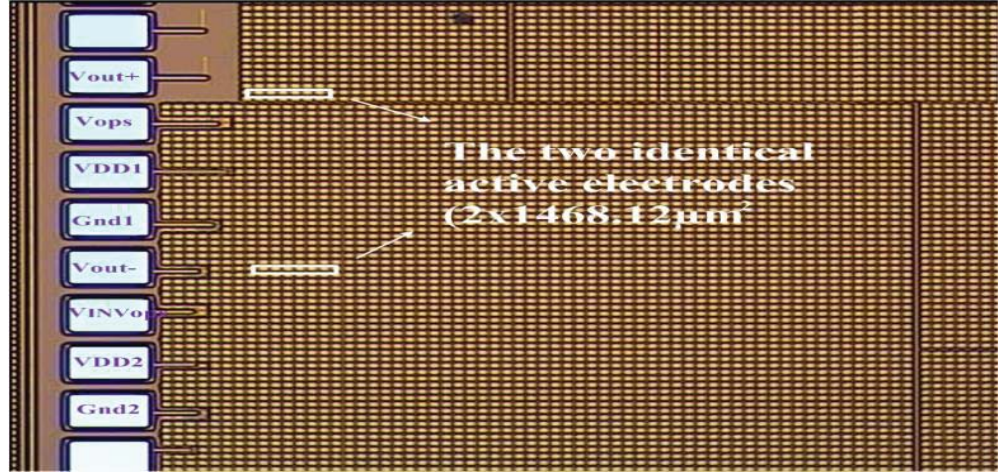
power and ground, as well as substrate contact, and are easily routed with an ordinal arrangement to each device. The DRC and LVS checks were passed for each completed sub-cell block. Figure 5.7 (a), (b), and (c) illustrates their layout, the package and microphotograph of the fabricated die, respectively.



(a) Complete layout for the two identical active electrode circuits.



(b) Package of CMOS active electrodes microchip.



(c) Chip photo-micrograph illustrates the location of the integrated two identical active electrodes.

Figure 5.7. The fabricated die of the two identical active electrode circuits. (a) layout, (b) Package of CMOS active electrodes microchip, and (c) chip photo-micrograph of the fabricated die.

### 5.5.1 Experiment Results of The Active Electrode

Transient measurements were carried out using the digital oscilloscope Tektronix TBS1102B-EDU. For measurements, the chip was housed in a 15x15 matrix PGA kit socket, with the wire connections emanating through a solder-less breadboard. In order to analyse the active electrode buffer's performance, the output ( $V_{WFG}$  or  $V_{OPS}$ ) of the electrode driving circuit of the previously fabricated 16-channel waveform generator (in chapter 4), and its complementary signal can be employed to drive the resistor load (skin equivalent load) through the active electrode buffer. The experimental set-up and the oscilloscope traces of the output waveform signal for the dual active electrode circuit are shown in Figure 5.8 and Figure 5.9 respectively. The two identical active electrodes have a 1Vp-p square wave voltage input (and its complementary) with a variable frequency in the range of 1Hz to 10kHz. A bi-phasic 2Vp-p square waveform has thus been effectively injected into a 50k $\Omega$  resistive load, as shown in Figure 5.9. The measured output amplitude (P-P) across the load was around 1.98V (at 9.84Hz), hence, the peak-to-peak output current,  $I_{p-p}$  around  $\pm 39.6\mu A$ . The small variation from simulation is mostly due to the fabrication process and also due to the tolerance of the off-chip load resistor compared to the simulated load.

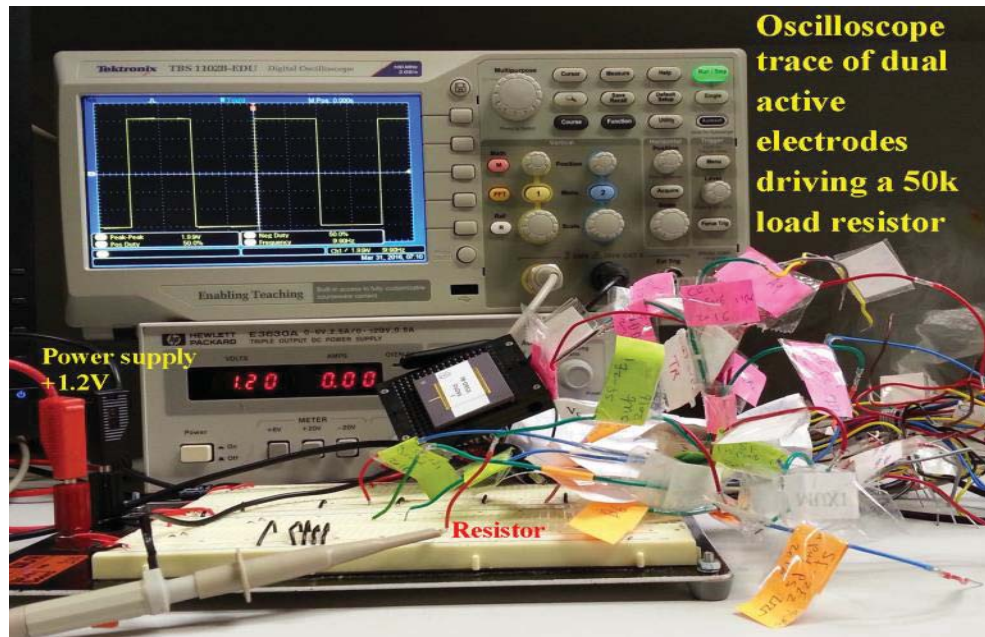


Figure 5.8. Experimental set-up for the active electrode chip output waveform measurements. The photo shows the oscilloscope, power supply, and, the chip housed in matrix PGA kit socket with labelled wire connections emanating through a solder-less breadboard and loaded with off-chip resistor (skin impedance equivalent load).

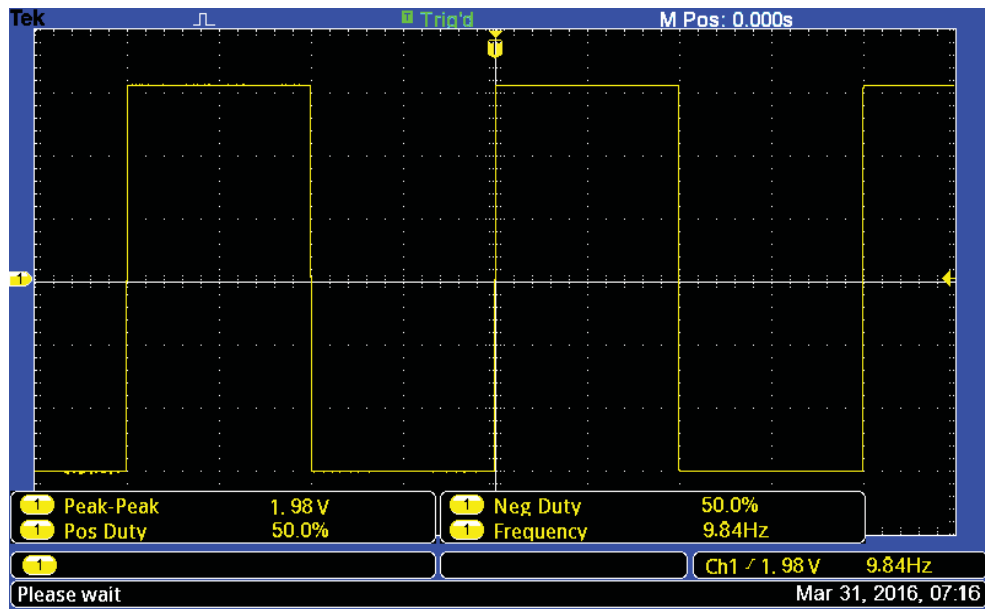


Figure 5.9. Oscilloscope trace of the differential output waveform signal of the dual identical active electrode circuits. A measured output voltage amplitude (peak-to-peak) of around 1.98V (at 9.84Hz) is displayed, indicating that the bi-phasic 2Vp-p square waveform input have been effectively injected into the 50 k $\Omega$  floating resistive load.

Table 5.1 summarizes the design performance of the proposed active electrode as well as comparing these values with some recently reported designs in literature [174, 186-188, 190]. The designed buffer circuit utilizes fewer MOSFET devices, uses a lower supply voltage of just +1.2V, and can provide an acceptable output current sourcing of around 145 $\mu$ A, using the adaptive biasing configuration. In addition, it consumes lower power of only 100.8  $\mu$ W compared to the previously reported buffer circuit designs. Although the buffer in [186], implemented with a class-AB output provides 1mA output current, it is based on a high supply voltage of +5V and consumes power of 150  $\mu$ W in standby mode, when there is no signal loading. Furthermore, the device count does not include the bias circuit transistors. The performance in terms of power consumption has been significantly improved with respect to all the other designs in the table. The buffer also provides the necessary input-to-output impedance transformation for effective signal transmission. The fabricated circuit is to be employed principally for non-invasive transmission of bipolar biphasic square waveform signal at the skin-electrode interface with high signal integrity for biomedical stimulation.

The complete electro-medical circuitry, including the WFG<sub>ING</sub> and the identical dual active electrodes circuit along with any external components can be mounted together, on PCB with platinum electrodes (transducers) directly soldered on the top of the PCB. This minimizes the signal path between the WFG<sub>ING</sub>, the two active electrodes, and the body, hence reduces interference and also makes the fabricated device compact. Figure 5.10 displays such a proposed proto-type electro-bio-stimulation system using (a) mixed-signal CMOS WFG<sub>ING</sub> (IC1), (b) the active electrode-pair (IC2), and, (c) solar panel charged regulated power-supply. The complete encapsulated bio-medical device with electrode contacts is depicted in Figure 5.10 (d). The circuit in Figure 5.10 (c) utilizes a solar panel along with an adjustable IC voltage regulator circuit to provide the required stable voltage to the three batteries. The circuit uses capacitor C (0.1 $\mu$ F) to protect from the static discharge, while the two diodes D1, D2 are used to protect from the reverse polarity by preventing the discharge of batteries. As this bio-electronic system is state-of-the-art in terms of low power, low cost and miniaturisation it could be suitable for use in both implantable and non-invasive biomedical system applications. But this process requires wire bonding to mount the fabricated chip on PCB; unfortunately, this process is not available at this time, so this process will be left to future work.



Table 5.1. Performance and comparison of the proposed active electrode with the previous reported publications.

Parameters	Reference					
	[186]	[187]	[174]	[188]	[190]	This work
Technology	0.6 $\mu$ m CMOS	0.6 $\mu$ m CMOS	0.35 $\mu$ m AMS	45nm CMOS	0.35 $\mu$ m CMOS	0.13 $\mu$ m CMOS
Kind of device & Technique	OTA+class-AB output stage	OTA+class-AB output stage	Two stages OTAs	Class-AB amplifier	Two stages OTAs	OTA+ adaptive bias current
Amplitude	-	-	-	-	$\pm 2.3$	1Vpp
Transistor account	8 <sup>1</sup>	13	5 <sup>1</sup>	22	19	9
Output current	1mA	300 $\mu$ A <sup>3</sup>	-	40mA	-	145 $\mu$ A
Supply voltage	+5V	+5V	-	+3V	$\pm 2.5V$	+1.2V
Power consumption	150 $\mu$ W <sup>2</sup>	150 $\mu$ W <sup>3</sup> 245 $\mu$ W <sup>4</sup>	1mW	-	-	100.8 $\mu$ W
Year	2006	2010	2011	2013	2015	2017

<sup>1</sup>Bias transistor not applied, <sup>2</sup>standby mode <sup>3</sup>Current mode, <sup>4</sup>Voltage mode.

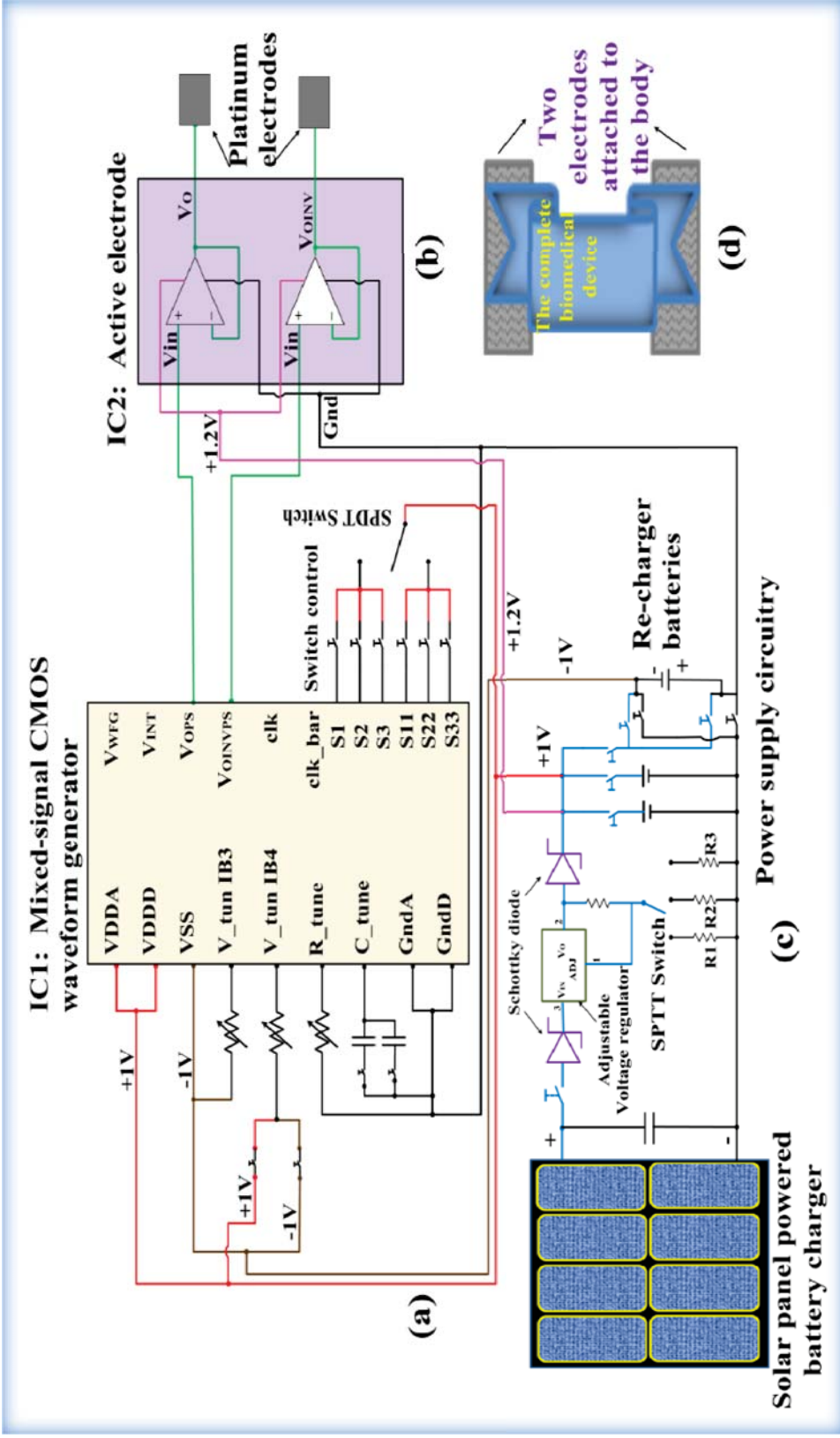


Figure 5.10. A proposed proto-type electro-bio-stimulation system using the fabricated active electrode-pair complete with (a) mixed-signal CMOS waveform generator, WFG<sub>ING</sub> (IC1 in chapter 4), (b) the active electrode-pair (IC2), and, (c) solar panel charged regulated power-supply. The complete encapsulated bio-medical device with electrode contacts is shown in (d).

## 5.6 Conclusion

The aim of this work is to transfer electrical signals in a specifically controlled fashion through the electroactive biomolecular tissue. This chapter presents an active electrode buffer to transfer low-frequency electrical signals through the electroactive biomolecular tissue without impact on signal integrity. The buffer is a compact active electrode-pair which provides the biphasic square waveform output signal. The individual active electrode realizes a buffer circuit, based on an adaptive voltage follower using a 130-nm CMOS technology, which can also be used to provide monophasic square/triangle waveform output signals. The analysis and design of a CMOS buffer circuit has been introduced. An adaptive biasing technique is used to increase the output current in an efficient way, and to reduce the overall power consumption. The simulation results indicate that the buffer circuit architecture implemented can provide gain of about  $\approx 1V_{p-p}$  and delivers output current of about  $145\mu A$  with power dissipation of only  $100.8\mu W$ , using  $+1.2V$  supply voltage. The proposed buffer circuit consumes a small silicon area of about  $0.00294\text{ mm}^2$ , compatible with high-integration. The two identical active electrode circuits swing between  $\approx \pm 1\text{ V}$ , and provide output current of about  $40 \pm \mu A$   $I_{p-p}$ , when driving a load resistor of  $50\text{ k}\Omega$  in a differential fashion, using a complementary active electrode circuit. The functionality of the two designed circuits, according to the required specifications, has been verified. The measured results are also provided; these are mainly close to the simulation, with only a small deviation from simulation values due to the fabrication process. This system is a new implementation of the low-power analog CMOS active electrode circuit for battery-operated biomedical devices. A proto-type system design using the fabricated active-electrode buffer is also proposed. It is state-of-the-art in terms of low power and miniaturization that comply with requirements for bioelectronics systems suitable for implantable and non-invasive biomedical devices. This analog CMOS active electrode circuit is published in Microelectronics Journal. The published manuscript is included in the Appendices section of this thesis.



## **Chapter 6**

# **In Vitro Biological Experiment Design And Performance To Investigate The Effect of Low Frequencies Electrical Pulses on The Human Blood Cells**

### **6.1 Introduction**

Electro-stimulation, which stimulates reactions to heal various pains or disorders and for disease treatment, has been known to have an important influence on living systems. It can influence the cell function by inducing various types of responses which may enhance [211, 212] or inhibit [213, 214] various cellular functions. This depends on the type and intensity of the electro force (electrical or electromagnetic), frequency, the type of waveform and pulse duration that induce different interacting kinds and levels of energies. An external electrical force, that interacts with electro-active biological cells, altering the membrane potential that controls cellular activities, has been shown to enhance cellular function [215], resulting in: conformational changes of the pore proteins, enzymes and phase transitions of membranes, ionic pumping across the cell membranes and structural rearrangement, due to ion displacement in response to an electrical force. These interactions are due to the presence of conductivity and permittivity properties in the biological cells, tissues, blood and protein [1, 43, 216]. The biological state of the target cells determines the kind and degree of the response. Infected cells could induce change in electrical charges on the cell surface, resulting in alterations in the electrical potential of the cell membrane, the structures of membranes, the intercellular mineral content (of sodium, calcium, etc.), energy production, and hence, its functions as compared to normal cells [47]. The effect on infected lymphocytes, however, comprising complex interactions, depends on the cell function state. Several studies have demonstrated that electro forces can influence the immune responses of animals and humans by inducing different immune response elements that enhance the production of antiviral substances [213, 215, 217, 218]. Since the 18th century many notable inventions and studies, have shown how to provide direct electrical energy to a patient's blood to deactivate all types of pathogens, as an alternative to therapeutic drugs [219-221]. They used, in their electrical treatment, either

high voltage, high frequency waves in the range of 750 kHz to 3 GHz or high AC current to destroy the pathogens inside the human body, but they did not clearly explain the facts behind this effect. Modern studies have used multigenic HIV-1 DNA-based vaccine injected intramuscularly by in vivo electroporation (EP) with high voltage, in healthy volunteers, to protect against a life threatening illness, to which the immune system might not respond, due to the ineffectiveness of the EP procedure [222], and hence, EP requires an advanced technique with complex apparatus [223].

However, the effect of a low frequency electrical field on the underlying mechanism involving protein–protein interaction between the host cells and HIV-1, as an active treatment, has not yet been employed and explained. Proteins are involved in cells communicating and mediating different signals, conducting events from the extracellular to the intracellular. These signals are essential for most of the cellular processes and can induce conformation change in the cell proteins which stimulates reactions that affect the function of many other proteins that are involved in several diseases [224]. Regarding signal transfer, CD4 receptor, co-receptors CCR5, as well as the nuclear pore complex (NPC) component proteins which involve nucleoporin 135 (Nup153) of the lymphatic system, are an essential kind of target for HIV-1 infection and development of AIDS. HIV-1 infection and replication is characterized by directly infected CD4<sup>+</sup> T cells and utilizes surface cell CCR5 proteins for the specific binding process and entry. This process involves protein-protein interaction, predominantly by charge-charge interaction and conformation changes [25, 225, 226]; this plays an important role in the binding process, to sustain interactions with the target cell and control their activity and thus mediate its life cycle replication. The HIV-1 particles which are important for replication then traffic from the cellular periphery to the desired regions of host DNA within the nucleus [227], utilizing its nuclear transport factor Nup153 proteins; this causes progressive reduction and death of the CD4<sup>+</sup> T cells, resulting in AIDS. HIV-1 infection, therefore, is considered as a cytopathic viral infection and study efforts were focused on the analysis of the specific biology of the virus within the host cell, in order to be used for HIV-1 therapy. Consequently, the research consideration has focused on immune-based therapies, antibodies that target host proteins, such as the use of combinations of co-receptor binding inhibitors, nucleoside inhibitors, reverse transcriptase inhibitors, and protease inhibitors, for most active anti-HIV-1 therapy; these inhibitors became the drugs of choice in the

pharmacological approach for HIV-1 patients [228]. Currently, protein engineering has been applied to induce mutant targeting, and blocking the binding steps, and other host cell cellular co-factors that are involved directly or indirectly in the viral replication cycle [2, 229]. Several studies therefore, have been focused in this area to identify the epitopes that are recognized by specific HIV-1 antibodies, and to provide detailed data about immunodominant and neutralizing epitopes [225]. In this chapter the effect of low frequency electrical force on cell surface expression of CD4 and CCR5, and on the binding activities of CCR5 N-terminal domain regions, as well as on Nup153 distribution, one of the NPC components, will be investigated in in-vitro. This specific interactions process that involves alignment and polarization of polar and charged protein molecules, in response to an applied low frequency external electrical field, to stimulate immune responses, can be utilized as a useful mechanism to induce enhancement and inhibition effects, prompting conformational changes for a period of time and preventing interaction with HIV-1. A given pulse can induce a short-term, or a long-term antiviral state, disturbing the HIV-1-host cell interaction, and producing a marked effect which could become the basis of in vivo anti-HIV-1 therapy. Thus, the next section presents a brief analysis of CCR5 protein's structure and predominantly its charged epitope that mediates interaction within the predominantly charged HIV-1 envelope protein. It will also describe the NPCs features and its important Nup153 that facilitates the passage of the high-weight HIV-1 molecule infecting viral particle pre-integration complex (PIC) and the viral RNA, respectively, through NPCs within nuclear envelopes. This review will provide specific details on electrostatic charge-charge interactions determining the interaction between the predominantly HIV-1 protein regions and the predominant protein regions of host cell CCR5 and NPCs, which is important to support the concept of this research project. The outline of this chapter is as follows: section (6.2) presents the co-receptor, CCR5, its protein structure, and it's negatively charged dominant epitopes which mediate interaction within the positively charged dominant HIV-1 envelope protein. The NPC features and the Nup153 component protein, important for bidirectional macromolecular transport of HIV-1 particles between the cytoplasm and the nucleus, will be described in section (6.3). Frequency-dependent polarization is presented in (6.4). Section (6.5) provides in vitro biological tests. Results will be delivered in section (6.6). Valuable findings will be discussed in section (6.7). Conclusions are drawn in section (6.8).

## 6.2 Chemokine Receptor CCR5

The fusion and entry of HIV-1 into the host cell begins with the binding of the envelope glycoprotein, gp120, to its primary host cell receptor CD4. Consequently, and according to the stage of the infection, HIV-1 has to bind to the chemokine receptor (co-receptor), CCR5, for R5 viruses in the early stage; clinically, in the latent stage of the disease, this is important for replication [230]; however, the co-receptor CXCR4 for X4 viruses is only important in a later stage, when there is a decrease in CD4 cell count and the disease is progressing to AIDS [231]. These co-receptors mediate both HIV-1 entry and disease development, thus they were used as targets to block HIV-1 entry and infection [232]. Therefore, co-receptor antagonists become attractive candidates for anti-HIV drug therapy. Co-receptor inhibitors including maraviroc (MVC), aplaviroc, vicriviroc, schering C (SCH-C), TAK-779, Plerixafor and AMD11070, all of which interact with charged amino acids, inducing conformational changes in specific regions of the co-receptors, have been used clinically for HIV-1 treatment [230, 233-236]. In fact, HIV-1 viruses resistant to these co-receptor inhibitors, have been known in patients, when mutation in the HIV-1 viral envelope protein allows it to detect the drug-bound conformation of the co-receptor bond, hence is able to enter cells using drug-bound CCR5 [237-239]. Up to now, it is unknown how the HIV-1 virus adjusts its CD4 and co-receptor binding properties to resist inhibition, while protecting its replicative capacity [25]. Since 1996, it has been known that co-receptor CCR5 plays an important role in the HIV-1 replication and its fusion co-factors in the early stages of viral infections [240, 241]. It is also predominant in host-to-host transmission and regulates trafficking and functions of the host cells [228]. The co-receptor, CCR5, is expressed in several immune cell populations including monocyte/macrophages, and dendritic cells that express high levels of CCR5 on their cell surface; and in T-cells, and natural killer (NK) cells; in nonimmune cell populations: in endothelium, epithelium, vascular smooth muscle and fibroblasts, also in microglia, neurons and astrocytes in the central nervous system [242]. It can bind to various ligands and mediate a different range of effects [243] that play key roles in AIDS, cardiovascular disease, diabetes, hypertension, and a variety of sensory and mental disorders [244].

### 6.2.1 CCR5 Protein Structure

Typically, CCR5 is a large family of G protein-coupled receptors. Figure 6.1 shows the protein structure of CCR5, which contains 352 amino acids.

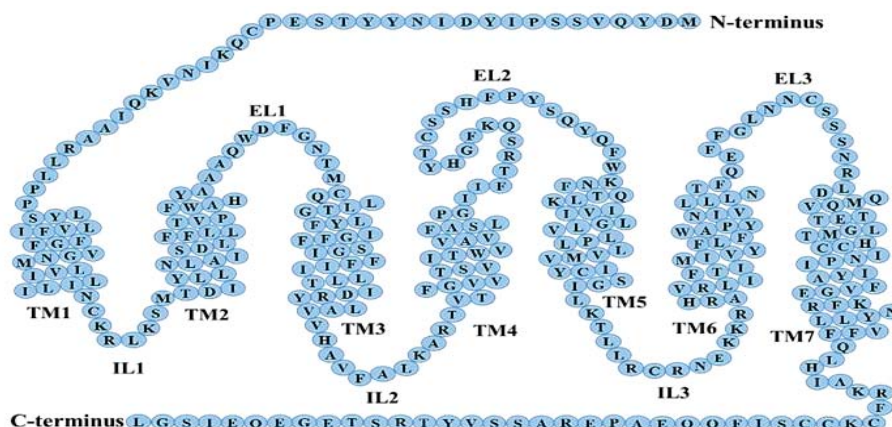


Figure 6.1. Protein structure of co-receptor CCR5 and its sequence. The image outlines the residues of N-terminus, and C-terminus, residues of the 7-TM region and of the extracellular (EL) and intracellular loop (IL) regions respectively. The featured model is a sketch based on the CCR5 model from [245].

The CCR5 protein comprises an amino terminal (N-terminal), a single polypeptide chain that is folded into seven transmembrane domains (TM) connected by relatively hydrophilic loops on the extracellular and cytoplasmic surfaces, three extracellular loops (EL), three intracellular loops (IL) and a carboxyl tail (C-terminal regions). These proteins are combinations of conserved, specific motifs of charged or hydrophobic regions, and are considered important for the functional response of the CCR5 and for the HIV-1 binding activity [246]. Direct effects on CCR5 proteins could be the major mechanism that prevents the virus from binding on the cell. Blocking CCR5 by conformation change of co-receptor proteins, therefore, prevents viral envelope protein binding and entry into the host cells. Hence, CCR5 inhibitors, based on conformation changes of the CCR5 involving amino acid sequence modifications in the CCR5-binding site, become the targets of anti-HIV-1 approaches. These inhibitors can alter the interaction with the HIV-1 envelope protein gp120 [245] and have been used to develop pharmacological agents able to inhibit viral entry and infection in the early stages [24, 25, 31, 230, 238, 246-252]. Thus many studies have attempted to

identify the regions and specific amino acid residues in the N-terminus and/or second extracellular loop regions of CCR5 that interact with the viral gp120 protein. These studies demonstrated that mutations of CCR5, by substituting amino acid in the amino-terminal segment of CCR5 that involves CCR5-HIV-1 interaction and binding, could prevent HIV-1 fusion and entry [245, 253, 254].

However, several investigations demonstrated that the N-terminal regions of the CCR5 assists with the third variable region (V3 loop) of the gp120 of the HIV-1, allowing the virus to use CCR5 efficiently and so increasing its fusion and replication effectiveness [25]. The V3 loop - CCR5 interaction promotes conformational changes in gp120 and separation of gp41 from gp120 [228]. Consequently, gp41 unfolds, and its hydrophobic fusion peptide is embedded into the host cell membrane, which allows the final fusion step to take place [255]. The study by Emmanuel G. *et al.* [256] showed that the predicted co-receptor binding surface on gp120 has a hydrophobic core, enclosed by a positively charged boundary, and is composed of conserved and variable residues, mostly located in the V3 loop. They also demonstrated that specific amino acids within the CCR5 N-terminal (amino acids 2 to 31), comprising the negatively charged, as well as tyrosine residues, are vital for CCR5-mediated fusion and entry of R5 and R5X4 HIV-1 strains. Zhong, P. *et al.* [28] have shown that the overall positive charge of the V3 loop is interconnected with the CXCR4 or CCR5. Thus the charge-charge interactions of the V3 loop and CXCR4 or CCR5 are considered the key factors that mediate HIV-1 fusion with the host cells. Blanpainet *et al.* [257] also showed in their study that a number of N-terminal residues were involved in gp120 binding and co-receptor function, suggesting that residues with negative charge in the CCR5 N-terminal could directly interact with the positively charged residues of the V3-loop. Earlier, the study by Farzan *et al.* [253] showed that the N-terminal site of CCR5 is rich in tyrosine (Y) and acidic amino acids, which mediate the link between gp120 and CCR5, and are, therefore, essential in HIV-1 infection and binding. They also reported that when regions rich in acidic amino acids, increase the net negative charge of N-terminal mediating interactions with HIV-1, and when modified by sulfate to add extra negative charges, this could increase the binding ability [258]. They then demonstrated that mutant amino acids in this region, in which neutral residue is included for most of the charged N-terminal domains, could reduce or may prevent the HIV-1 binding and entry. Monoclonal antibodies (mAbs), such as 3A9 and 5C7, targeting host protein to



recognize epitopes in the N-terminal of CCR5, were used in their assay [253]. Liu *et al.* [259] also reported in their study that in the first step of binding, the acidic region (the negatively charged) in N-terminal of CCR5 interacts with the basic region (the positively charged) in the gp120 prompting conformational changes in the N-terminal, mediating HIV-1 fusion by the V3-loop.

Later, Dimitrios *et al.* [226] showed in their study the electrostatic potentials may play a role in a V3-CCR5 interaction, involving the interaction of the V3 peptides containing 7 basic residues (4 Arg, 2 His, 1 Lys) and two acidic residues (Asp and Glu), that the predominantly positively charged residues of V3 are more responsive to interaction with the CCR5 N-terminal domain than the other CCR5 extracellular domains (ECL), due to its length and the domination of its negative electrostatic potential. They also showed that the N-terminal and ECL1 domains are more negative than the ECL2 and ECL3 domains and possibly more compliant to binding with the V3-loop of gp120. They have then proposed that charge-charge interactions determine the interaction between the predominantly positive V3-loop and the predominantly negative N-terminal peptide of CCR5, thus electrostatics drives recognition and binding activities. It is reasonable to assume, therefore, that the attractive interactions between positively charged proteins of the V3-loop at certain critical locations of the negatively charged proteins of CCR5 N-terminal could contribute to the stability of the binding. Christoph *et al.* [29] also reported in their study that mAb 3A9 that recognize the conformational epitopes on CCR5 at the N-terminus, can block HIV-1 entry, and the mutation of the N-terminal motif Y<sup>10</sup>D<sup>11</sup> prevented HIV-1 entry into transfected cells, as with CCR5 and for CCRR5/CXCR4 HIV-1 types. They then demonstrated that the conformational contact sites of CCR5 with the mAb 3A9 represent sites on CCR5 that are essential for HIV-1 entry. John C. *et al.* [238] supported the previous studies, and demonstrated that residues within the CCR5 N-terminus domain were critical for the ability of the maraviroc MVC-resistant virus to use drug-bound CCR5 as a co-receptor for entry. They showed that the conformation of the CCR5 N-terminus did not seem to be intensely altered by drugs, since they found that CCR5 N-terminus-specific mAbs 3A9 and CTC5 was still able to bind with identical efficiencies to drug-free or drug-bound receptors. They then reported that the tyrosine mutants Y<sup>10</sup>, Y<sup>14</sup>, and Y<sup>15</sup> strongly inhibited the ability of the resistant viral envelope to use the drug-bound receptor, while, the D<sup>11</sup> mutation strongly reduced infection.



A recent study by Himanshu *et al.* [24], demonstrated that the V3 loop form a hydrogen bond with the polar amino acid residues glutamine (Q4) in the N-terminals of CCR5; this is considered the most critical factor in adaptation to low level CCR5 in some viral strains. In pharmacological approaches, however, mapping protein interactions, and protein engineering, additions or substitutions of a few charged amino acid residues at the termini of these extracellular terminal domains are used to alter the net charge and induce conformation change that blocks the HIV-1 interaction with the host cell receptor thereby preventing HIV-1 viral fusion and entry [2].

However, it is evident from all of the above studies that the interactions between the N-terminal of co-receptor CCR5 and the V3-loop, is predominantly by charge-charge interactions, which plays an important role in the binding process. Polar and charged protein-protein interfaces within the CCR5 are therefore, involved in many HIV-1 viral cellular processes. This interface can be fully mediated by the negatively charged N-terminal domains. Charged amino acids residues of CCR5 N-terminal domains can mediate the V3-loop binding to the host cell receptor and induce conformational changes to control their protein function and stimulate different signals that facilitate HIV-1 viral fusion and entry. These signals are vital for viral cellular processes and viral replication [40].

Interestingly, since this binding process is characteristically dominated by electrostatics charge-charge interactions [226], the redistribution of the charge in the CCR5 N-terminal domain in response to an external electrical field can induce conformation changes of its proteins. Therefore, a low frequency electrical field can be utilized to inhibit HIV-1 infections and ligand binding affinity. Alternation of the predominantly polar and charged amino acids of CCR5 N-terminal domains, in response to a low frequency electrical field, is used in this research project to investigate the CCR5 N-terminal binding activities utilizing antibody 3A9 that recognizes the epitope in the N-terminal domain of CCR5.

### **6.3 The Nuclear pore complex (NPC)**

The steps of the HIV-1 replication involve translocation (import and export events) of the infecting viral particle that is securely regulated within the nucleus host, which provides a distinctive environment for replication as well as expression of its

genome. The HIV-1 life cycle is therefore, accomplished by utilizing host nuclear transport components to enable the import and export and passage of their large molecular infecting viral particle pre-integration complex (PIC) and the viral RNA, through nuclear envelopes and across the nuclear membrane. For both PIC import and RNA export, the question here is what are the facts behind the transport of a high weight molecule through nuclear pores? This essential process of nucleocytoplasmic transport occurs through the nuclear pores. The nuclear pores comprise a specific macromolecular assembly, characterising the nuclear pore complex that allows passive nucleocytoplasmic passage of ions and small molecules (molecular mass  $M \sim 20\text{--}40$  kDa, diameter  $\sim 5\text{--}9$  nm). The passage of larger proteins and RNA ( $M > 40$  kDa up to  $\sim 25$  MDa, diameter of up to  $\sim 40$  nm) [260] resulting in the fusion of the inner and outer nuclear membranes [261] requires transporters, hence, binding to specific nuclear transport components, to overcome the permeability barrier of the NPC. Thus the nuclear envelope, including NPCs, is the selective barrier against the translocation of the high weight molecule (cargos) between the nucleus and cytoplasm, facilitated by the transporters, Importins and Exportins Karyopherin- $\beta$  (Kap) family of proteins [262] that attach to certain signals and carry the cargos through the NPCs [260]. Kaps carry proteins and protein/RNA complexes comprising nuclear localization signals (NLSs) and/or nuclear export signals (NESs) [263, 264] within their polypeptide chains and these direct nucleocytoplasmic traffic and facilitate a particular direction (in or out of the nucleus) along the route of passage [27] through the NPC [265]. Thus the NLSs prompt nuclear import when bound to cytoplasmic receptor proteins (importins/kap) and they are equivalent to the NESs that prompt rapid nuclear export when fused to Exportins Kap; both facilitate translocation through the NPC [262]. This process of translocation is completed by sequence interactions of Kap complex with different nuclear cellular proteins in NPCs called nucleoporin (Nup) [263, 266].

The NPCs are therefore, sole facilitators of bidirectional macromolecular transport between the cytoplasm and the nucleus. They are  $\sim 100\text{--}120$  nm in diameter with a central transport channel, measuring  $> 40$  nm in diameter, which allows for the passage of large macromolecular proteins and RNA through the nuclear envelope [267, 268]. The central channel is embedded within the pore, linking the inner nuclear membrane to the outer nuclear membrane. The NPC is a large 50MDa macromolecular structure, consisting of 30 different proteins termed nucleoporins (Nups) such as Nup88,

Nup214, Nup358, Nup62, Nup58, Nup54, Nup50, Nup93, Nup96, Nup98, Nup205 and Nup153 [265], that are arranged in an eightfold radial symmetry, to form a number of substructures, including the central channel in which the nucleocytoplasmic transport occurs [265, 269] as well as the attached cytoplasmic filaments and nuclear basket substructures [26]. Figure 6.2 shows the NPCs structure.

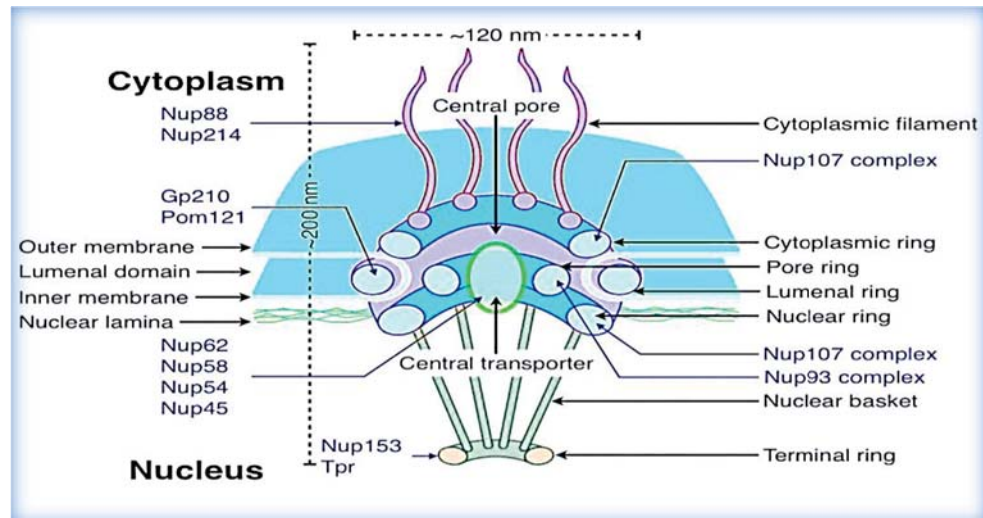


Figure 6.2. Nuclear pore complex structure [268].

Around 30% of Nups proteins are rich in phenylalanine-glycine (FG) repeat domains within their amino acid (AA) sequence [270], hence, they are termed FG Nups, generally observed as FxF, FxFG, GLFG [271] or PxFG patterns [270]. These FG Nups line the central channel of the NPC, as well as the cytoplasmic and nuclear openings [272] and direct the selective passage of large macromolecules through the pore. Actually, these FG Nups proteins are dynamic components and highly flexible structures, characterized as intrinsically disordered proteins [273]. Its sequences, which are comprised of FG repeats, that are associated with amino acid linkers, regulate the formation of an FG Nups network at the centre of the NPC. They act together with translocating particles to arrange the permeability barrier and organize the selective translocation through the NPC [260]. This FG sequence is considered the main driving force responsible for the active translocation of cargos through the NPC and characterized as a selective barrier transport mechanism [274, 275]. High weight

molecules with large diameter are required to be transported by specific members of the Kap family carrier proteins that are able to interact with the FG-based permeability barrier [263, 276]. Recent studies have shown the importance of sequence composition of FG Nups. A specific distribution of the polar residues, FG motifs and like charged regions (positive or negative charge) of the charged residues in the sequences of FG Nups, determines the formation of FG Nups network at the centre of the NPC [260]. Therefore, the FG Nups' network and their rearranged structure, being responsible for regulation of nucleocytoplasmic traffic in the NPC, change the composition in these sequences; this impacts considerably on the distribution of FG Nups inside the pore [260, 273, 277, 278]. The specific patterns in the FG Nups sequences, however, play a key role in the regulation of the distribution of FG Nups inside the pore, and nucleocytoplasmic transport mostly depends on distinct structures hidden in the sequences comprising FG Nups [274, 279].

The disordered manners of FG Nup are favoured to the degree that they fulfil the function of an FG Nup and play a key role in nucleocytoplasmic transport [270, 279]. Their charged disordered regions comprise a fraction of charged amino acid (AAs) and a specific localization of a high density of charged residues, promoting electrostatic interactions that regulate the formation of the FG network at the centre of the NPC, which could be a key factor in the whole selective mechanism for NPC transport [260, 273]. This amino acid that is associated with FG-repeats has been shown to be functionally important in their actions, resulting in collapsed or extended coil which may possibly provide a permeability barrier, depending on the percentage of charged and hydrophobic residues [280]. However, momentary electrostatic interactions between transporters (cargo complexes) and disordered domains of FG Nups are necessary for selective transport, and are considered the main driving forces that stimulate active translocation of cargos through the NPC [281]. Electrostatic repulsion between like charges of like charge regions can also act as a regulatory mechanism that maintains the central network of FG Nups in a certain radius of the central transporter [260]. The interaction of the FG Nups with specific nuclear transport receptors (NTRs) including NLSs or NESs on proteins that are targeted for import or export, respectively, therefore, mediates the passage of NTRs-cargos, the high weight macromolecules, through the central channel of the NPCs [263, 282, 283].

However, not all domains of FG Nups have a high density of charged residues which may possess specific functionalities for different regions of each FG Nup [260]. The sequences of some of the FG Nups have two functional domains; the straight highly charged domain, and a compact structure FG domain that forms the central network of FG Nups. The highly charged domain is responsible for bringing the FG domain near the central axis of the pore, to act as a hydrophobic core, interacting with the cargo complex, mediating the active transportation and passage through the NPC [280].

One of the highly dynamic components of the NPC is the FG Nup153 that is enriched in FG repeats and is localized specifically to the distal ring of the NPC basket (Figure 6.2) which has a specific role in nucleocytoplasmic import as well export events [267]. FG Nup153 has an important role in nuclear import [284], and export [27] of large macromolecular proteins and RNA, that is mediated by the interaction of several regions of FG Nup153 with import and export receptors [285]. FG Nup153 therefore, plays an important role in the import and export of the large molecular infecting HIV-1 viral particle into the host cells.

The long FG Nup153 has high degrees of topological complexity, distribution of high and low charged amino acids (AA) in their disordered domains, and low degrees of polarity [273] with hydrophobic residues. It displays a heterogeneous tripartite structure that comprises three different domains as shown in Figure 6.3, the N-terminal domain enriched in FxFG-repeats (F is phenylalanine AA, x is any AA, 609 AA and six FG motifs) which are attached to the nuclear rim of the NPC and contain motifs that are important for targeting the protein to the NPC. Its C-terminal is large (200 nm long), unfolded, rich in FG (896–1475 AA, containing 25 of the FG motifs) thus it possesses a highly flexible structure [286].

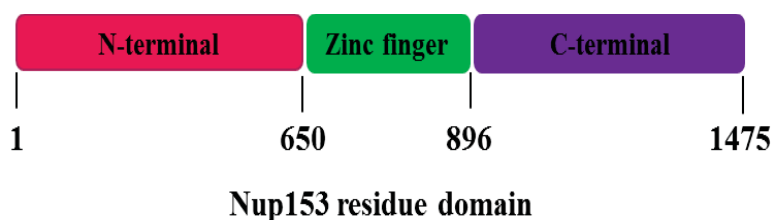


Figure 6.3. A heterogeneous tripartite structure of FG Nup153, comprises three different domains, N-terminal domain, zinc finger domain, and C-terminal domain based on Nup153 model from [26].

It reaches through to the cytoplasmic side of the NPC channel [287], and is directly involved in the trafficking of import complexes into the nucleus as well as the exporting of mRNA [288]. It mostly consists of PxFG- repeats (P is Proline AA), and polar N+Q-rich residues along the sequence, in which N and Q are polar side chains, AAs, Asparagine and Glutamine respectively [270], while the sequence of its middle region is more complex and contains many AA (x) (610–895), with four zinc fingers and two FG motifs [286, 289]. It resides at the distal ring, [287] and has four motifs, each containing a single zinc ion between two cysteine residues (Cys2-Cys2). The zinc finger domain binds to the DNA suggesting that it is important in the efficiency of DNA nucleocytoplasmic transport [267, 290].

The role of FG Nup153 in translocation through the NPC has been well recognised, due to the fact that the large amino acid residues of its C-terminal domain with its FG-repeats provides flexibility within the NPC, since it can be identified at the nuclear basket and even at the cytoplasmic periphery of the central pore [287]. In addition, the nuclear import and export receptors interact with several regions of FG Nup153, therefore FG Nup153 is known to be important for both nuclear import and nuclear export. The importance of FG Nup153 in nuclear import is confirmed by the recognition that the Importin Kap family of transport receptors bridges a link between FG Nup153 and NLS cargo-receptor complexes to mediate import [283, 285]. On the other hand, one of the peripheral pore structures that has an important role in nuclear export is the basket structure of the pore. The flexible structure of the basket allows large ribonucleoproteins (RNPs) entrance to the central transporter through a rearrangement of the distal ring during nuclear export [261]. As shown in Figure 6.2, FG Nup153 is the only FG Nup that is close to the surface of this basket [261, 291], signifying that FG Nup153 is actually one of the first FG Nup pores in which RNA or protein are meeting during export [27]. The importance of FG Nup153 in nuclear export of RNAs is due to the fact that the Exportin Kap family transport receptors link the FG Nup153 and NES cargo-receptor complexes to mediate export. The importance of FG Nup153 in nuclear export is confirmed when antibodies to inhibit Nup153, injected into *Xenopus* oocytes, block the export of mRNA, and nuclear RNA, indicating a need for FG Nup153 in the export of several classes of RNAs [27].

Interestingly, the HIV-1 virus is therefore incapable of passing (import or export) the large macromolecular infecting viral particle into the host independently of



nuclear transport components, particularly, FGNup153. The steps of the HIV-1 replication started with the entry of the large infecting viral particle, PIC [292, 293] into the host nucleus; this requires active translocation into the nucleus. This is obtained within the specific interaction of the viral particle proteins with the nucleoprotein complexes that are controlled by the core of the infecting viral particle. HIV-1 infects cells by utilizing host nuclear transport components to enable the passage of their large particles through nuclear envelopes and across the nuclear membrane via nuclear pore complexes (NPCs) [294]. Various studies have showed that host cell factors are important in the HIV-1 particle nuclear import and they investigated the need for certain cellular proteins of HIV-1 particle nuclear import, which involve pathways in the viral life cycle, comprising nuclear transport proteins Nup98 [295], importin 7 [296], and nuclear transport proteins TNPO3 in viral integration (a Kap family protein, which imports multiple proteins into the nucleus) [293] and the major essential proteins of the NPC, nucleoporins Nup358/RanBP2, Nup214 and Nup153 [297, 298]. Some studies [298] demonstrated that FGNup153, RanBP2 and Nup214 have importance in the nuclear import of the infecting viral particle, whereas others have demonstrated that FGNup153 has a potential role during HIV-1 PIC sub-viral particle nuclear import. HIV-1 Vpr is able to bind N-terminal domain (448–634AA) of the FGNup153 [299] and HIV-1 IN particle that binds directly with the FxFG-rich C-terminal domain of FGNup153, acting like the Kap Importins family of proteins [288]. This suggests that HIV-1 sub-viral particles can gain access to the nucleus by interacting directly with the NPC through the binding to FGNup153 domain terminals in the absence of import factors and motivate the transport of the viral cDNA into the nucleus. However, HIV-1 requires cellular FGNup153 for the nuclear import of infecting viral particles. Importantly, FGNup153 during HIV-1 particle nuclear import has been mapped to the HIV-1 capsid protein and FGNup153 interaction, and depletion of FGNup153 expression inhibits HIV-1 infection, by inhibiting nuclear import and blocking HIV-1 infection, compared to the infection of control cells [227, 300]. Kenneth A. *et al.* [26] showed that a direct interaction between the HIV-1 capsid proteins, CA N-terminal domain and the FG-repeat enriched FGNup153 C-terminal domain enhances the HIV-1 PIC nuclear import. They also identified both of the domain residues that are important for binding and viral infectivity. They showed that mutation of the HIV-1 CA N-terminal domain residue Asn57, Lys70, or Asn74, disturbs the binding to the



FGNup153 C-terminal protein. This study however, reported that each of the FG motifs of Nup153 C-terminal has some affinity for the CA N-terminal. FGNup153 C-terminal attachment to the CA N-terminal domain through phenylalanine, as well as adjacent residues such as glycine, forms hydrogen bonds with CA residue Asn57, as well as adjacent polar side-chains. Eliminating residues 896 to 1045 of FGNup153 C-terminal domain showed considerably diminished binding. This finding shows that the HIV-1 nuclear trafficking mechanism and viral control of an essential cellular process through FGNup153-CA interaction, and disorder or depletion of FGNup153, can disturb multiple steps, such as intranuclear trafficking and integration site selection.

The HIV-1 virus also has a mechanism that utilizes a cellular protein export pathway, allowing the transport of unspliced late viral mRNA transcripts to the cytoplasm [301]. The virus proteins are encoded by large, intron-containing mRNA transcripts that are usually reserved in the nucleus [302]. The export process of viral RNA is therefore facilitated by the viral RNA-binding protein, Rev, existing in all unspliced viral transcripts [303]. The viral Rev protein comprises 116 amino acids with two important functional domains, the N-terminal domain which has the arginine-rich motif required for RNA binding, while the C-terminal domain has several leucine residues (sequence LQLPPLERLTLD) which is considered the effector domain factor, that acts similarly to the nuclear export signal NES, allowing Rev to shuttle between the nucleus and the cytoplasm [304, 305], prompting rapid nuclear export when binding to a target protein [306, 307]. Thus, mutation of these leucines to alanine inhibits the export ability of viral proteins that are needed to control the biological cell activity for the replication of the HIV-1 life cycle [307]. However, the effector domain of Rev alters in order to mimic a cellular NES, letting the virus utilize a cellular protein export pathway that mediates the transport of unspliced viral transcripts by interacting with FGNup of the NPC [302]. The region of the host cellular protein that interacts with the Rev effector domain comprises repeats of the two amino acids phenylalanine and glycine (FG repeats) [308]. Several studies have investigated the interaction of cellular NES with the repeat regions of various Nup components of NPC and compared these with the functional wild-type Rev effector domain [302]. They used various Nup proteins including Nup153 and Nup98 that are located on the nucleoplasmic side of the NPC [290, 309], the pore membrane protein, rat protein Pom121 [310], and two other proteins, Nup159 [311] and Nup214, that are located at the cytoplasmic face of the NPC

[312, 313]. They then reported that FG Nup153 and FG Nup214 of the Nup proteins interact directly and strongly with the functional wild-type Rev effector domains [302] at different concentrations, and did not interact with the Rev mutants that remove single leucine residues at positions 78 and 83 of the Rev NES, respectively. Katharine S. *et al.* [314] also demonstrated that FG Nup153 is actually involved in the mechanisms of protein and RNA in nuclear export, as well as in the HIV-1 Rev protein export pathway. This study reported that FG Nup153 is also important in the nuclear import activities as shown in Figure 6.4.

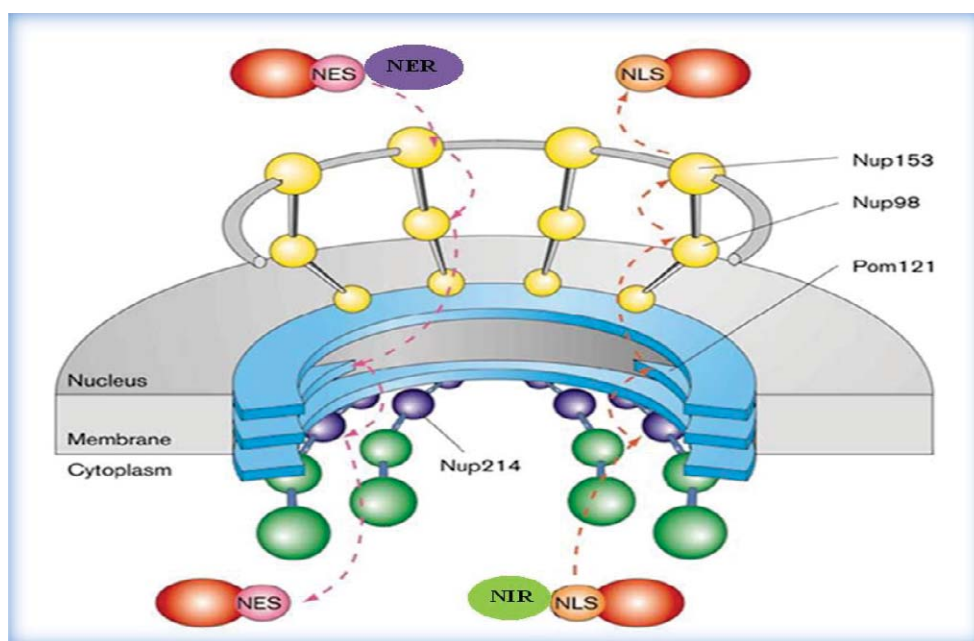


Figure 6.4. Nuclear pore complex model for protein import and export of large macromolecular proteins that are recognised by nuclear transport receptors (NTRs) and passage them through the central channel. FG Nup153 are attached to the nuclear rim of the NPC and are important in the import (orange) and export (pink) events of the cargo complex. NIR and NER are the Nuclear Kap/Importin and Kap/Exportin receptors that are connected to the NLS and NES respectively [302].

It can be concluded from the above studies that NPCs, particularly FG Nup153, are the key factors in the HIV-1 replication, which provide the gateway for the viral import and export activities that enhance the HIV-1 replication, hence, depletion of the nucleopore components, can reduce the HIV-1 infection efficiency. High weight

molecular HIV-1 infected particles are imported and exported via an active process through the NPC, by interaction of the HIV-1 domain particles that bond directly with the FxFG-rich C-terminal domain of FG Nup153 and act as a Kap cargo complex Importins and Exportins proteins family. This involves signals, cellular factors, and functional NPC through a conformational change of the Nup complex [315] and in particular, the repeat regions FG motifs of Nup153 C-terminal that are involved simultaneously in binding NLS-containing complexes for import and NES-containing proteins for export [302]. Therefore, this specific transport mechanism could be disturbed, for a short period of time, by electrostatic interactions between external low frequency electrical pulses and the FG Nup153 domains, establishing effective and temporary permeability barriers across the NPCs, which could inhibit the reorganization of NPCs and hence, import and export of high weight molecular HIV-1 particles. To examine this, in this research project, the distribution of FG Nup153 in response to electrical stimulation, is investigated using immunofluorescence technique with a fluorescent labelled antibody mAb Nup153.

## 6.4 Frequency–Dependent Polarization

Generally, proteins that build-up amino acid are dynamic molecular, considered heterogeneous due to the extensive presence of various conductivities and permittivity [36]. This is due to the presence of different charge distributions, involving the polar and charged molecules in its structure which allow proteins to assemble with other proteins with a large conformation change, undergoing structural rearrangements in response to intercellular signalling and extracellular signals. The predominant charged groups carboxyl ( $\text{COO}^-$ ) and amino ( $\text{NH}_3^+$ ) in the proteins' structures possess dielectric properties, due to the presence of dipole moment,  $\mu = q \cdot d$ , (the product of the charge  $q$  and the charge separation  $d$ ). In addition, these ionisable groups, in solution, make a strong electrostatic interaction which possesses another dipole moment. The linking peptide bond is also polar, but has restricted motion, thus it displays a small effective dipole moment [316]. The different compositions of the side chains also possess different charge distributions such as in a polar amino acid (tyrosine (Y), glutamine (Q), serine (S), asparagine (N), threonine (T), and cysteine (C), negatively charged as in acidic amino acid (aspartic (D) and glutamic (E)), and positively charged

as in basic amino acid (lysine (K) [21, 316]. Consequently, when an external field is applied, the randomly orientated polar molecules of the protein and the positively and negatively charged molecules within the protein rotate, move, align and polarize, and are redistributed in response to the electrical force, producing an internal dipole with internal electrical field, opposite to the external electrical field.

The degree of polarization is dependent on the magnitude of the applied electrical field and, hence, the temperature, as well as on its oscillation frequency. When the applied electrical field ( $E$ ) is increased, the polarization ( $P = \epsilon_0 (\epsilon_r - 1) E$ ) of the proteins increases, (where  $\epsilon_0$  is the permittivity of free space and  $\epsilon_r$  is the relative permittivity of the material) [45]. Considering proteins as dielectric materials [43], however, electrical breakdown takes place when the maximum or high electrical field is applied on dielectric materials exceeds the dielectric strength. This arises when a given voltage is applied for a long period of time, so that the dielectric constant is reduced, due to the generation of sufficiently high temperature that disturbs the orientation of the dipoles and hence, dielectric materials are incapable of reaching a state of thermal equilibrium [44, 317]. Similarly, if the electrical force involves pulses with a different frequency range, polarization will then follow the oscillation characteristic of the electric field. At very low frequencies, proteins possess a large low frequency permittivity, because the dipole presence in proteins has enough time to align and polarize in response to the applied electrical field, before its change in direction. At intermediate frequencies, the dipole movement decreases, and does not have enough time to follow the changing direction of the electrical field, so that the polarization of the dipoles decreases. At very high frequencies, the dipoles do not have enough time to align, are totally unable to respond to the applied electrical field, and polarize, causing dielectric heating, and hence, dielectric loss takes place. In this stage, the proteins lose their charge storage ability and behave like a non-polar dielectric. This behaviour follows the Debye dispersion that is characterized by the relaxation time  $\tau$ , [1, 216] which can be given by:

$$\epsilon'(\omega) = \epsilon_{\infty} + \frac{(\epsilon_s - \epsilon_{\infty})}{1 + \omega^2 \tau^2} \quad (6.1)$$

$$\epsilon''(\omega) = \frac{(\epsilon_s - \epsilon_{\infty}) \omega \tau}{1 + \omega^2 \tau^2} \quad (6.2)$$

Where,  $\varepsilon'$  is the permittivity,  $\varepsilon''$  is the dielectric loss,  $\varepsilon_s$  is the low-frequency relative permittivity,  $\varepsilon_\infty$  is the high-frequency relative permittivity and  $\omega$  is the angular frequency. Relaxation time is a function of the frequency in which the time required for the polarisation diminishes exponentially and vanishes, and the dipoles return to their original random orientation, if the relaxation time is equal to the rate of oscillating frequency, resulting in minimum dielectric loss; whereas, when the rate of oscillating frequency is faster than the relaxation time, the polarization no longer follows the oscillating frequency, causing a rapid drop in dipole polarization, resulting in maximum dielectric loss. The dipole therefore, remains frozen, with no effective contribution to the dielectric constant, resulting in energy absorption and dissipated as heat [318]. Schwarz showed that the dipole polarizability of the biological material is frequency-dependent and can be given by,

$$\alpha = \frac{\alpha_o}{1+j\omega\tau} \quad (6.3)$$

Where,  $\alpha$  is the dipole polarizability and  $\alpha_o$  is the low frequency polarizability which normally occurs in a low frequency region. Very small dielectric dispersion was observed at the relatively low frequency of (<1Hz), whereas high dielectric dispersion was observed at the relatively high frequency of (100KHz to 20 GHz) [1]. However, local variation of the dielectric properties of proteins is important for the biological function of a protein [45, 216]. Therefore, when a given frequency electrical pulse is applied, the redistribution and alignment of the protein charged molecules and their polar molecules, in response to an applied external electrical field, can be a useful mechanism that interrupts the communication between the HIV-1 virus and the host cell. Since HIV-1 viral attachment and fusion, and the passage of its large macromolecular infected particles and its RNA through NPC, require stable and sustained interactions with the target cell, the HIV-1 virus cannot conjugate with the target cells, disturbing its life cycle, leading to inactivation signal-induced virus death. Thus useful effects of low frequency and low voltage electrical stimulation of human blood, inducing conformation change to enhance immune activity or inhibit interaction between HIV-1 and the host cell, for a period of time, will be investigated in the next section.

## **6.5 In Vitro Biological tests**

As previously mentioned all bioelectrochemistry experiments were done with human Ethics (SOA 16/12) considered and approved by the Massey University Human Ethics Committee. A copy of the Ethic approval has been provided in Appendix A.

### **6.5.1 Materials and Procedure**

#### **1. Blood**

Freshly sourced human leukocyte-rich buffy coat sample from a healthy volunteer is obtained from New Zealand Blood Bank Services (NZBS). The buffy coat sample is supplemented with Anticoagulant Citrate Phosphate Dextrose Solution (CPD) for clotting preservation. It is used for the low frequency electrical stimulation test on cell surface receptor CD4, co-receptors CCR5 and on the binding activities of CCR5 N-terminal domain, as well as on the distribution of FGNup153, using fluorescent labelled antibodies CD4, CCR5, 3A9 and Nup153, utilizing immunofluorescence microscopy. Buffy coat rich-leukocyte samples were used in this experiment, since CCR5 are expressed on various leukocyte subsets [319].

#### **2. Immunological Reagent and Materials**

The following fluorescence antibodies (Abs) and materials were purchased by Massey University from Medi'Ray New Zealand Ltd; conjugated Ab FITC anti-human CCR5 (Cat: 313705), conjugated Ab Alexa Fluor 488 anti-human CD4 (Cat: 317419), purified primary antibody against CCR5 N-terminal, unconjugated Ab 3A9 (Cat: 634501) and conjugated Ab Alexa Fluor 488 Goat anti-mouse IgG (Cat: 405319 ). Cell fixation buffer 4% Paraformaldehyde (PFA) (Cat: 420801), plastic coverslips (No.: BAH446900000), glass slides (No.: S8400-1PAK), Poly-L-lysine coating solution (No.: P4707), and anti-fade mounting medium fluoroshield (No.: F6937) were purchased from Sigma Aldrich. Whereas purified primary antibody against NPC proteins, unconjugated anti-Nup 153 (Cat: 906201), conjugated Ab Alexa Fluor 555 Goat anti-mouse IgG (Cat: 405324) and 4'6-diamidino-2-phenylindole (DAPI) (Cat: 422801); were personally procured (kind gift from the researcher herself) from Medi'Ray New Zealand Ltd, along with 3 glass chambers 3cm in diameter, forceps to mounting the coverslips, and clear finger nail polish to seal the coverslips on slide. The Phosphate

buffer saline (1X PBS) and Serums, hydrochloric acid (HCl) acid, Ethanol and methanol were a kind gift from the Human Nutrition lab building 27, Massey University Albany campus along with all experimental apparatus such as beakers, Parafilm, polypropylene tubes, 1mL pipette, 100 $\mu$ L pipette, 20 $\mu$ L pipette, 2 $\mu$ L pipette and their pipette tips, for which the researcher is very grateful.

### 3. The Electrical Test Chamber.

The electrical test chamber was developed by the researcher herself in the lab using a 30ml capacity glass chamber 3cm in diameter, with two stainless steel wire electrodes and were autoclaved for the electrical test. Flat electrodes were used, to obtain a uniform electrical field intensity over the blood sample. The electrode material was chosen to satisfy three requirements: (1) electrical conductivity (2) corrosion resistance and (3) cost. Figure 6.5 shows the electrical test glass chamber with stainless steel wire electrodes.

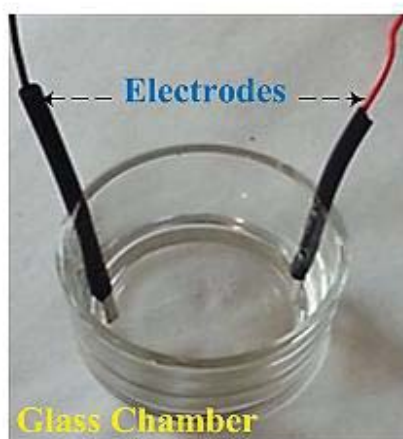


Figure 6.5. The electrical test glass chamber with stainless steel wire electrodes.



### 6.5.2 Electrical Simulation Procedure

Buffy coat samples were exposed for 2h to low frequency bipolar square waveform pulses of 5Hz, 10Hz and 1000kHz with applied voltage of 1V in the electrical test chamber in Figure 6.5. Electric fields and current are then produced through the two electrodes in direct contact with the blood samples. The low frequency square waveform pulses with 1V were applied, using a square WFG, with variable frequencies. Since the experiment was performed in the blood experiments lab, due to the safety and health rules, the WFG that was used for the biology test was built by the researcher using a discrete circuit, instead of the one developed in this research project. Accordingly, the output of the electric pulse that was supposed to be observed by an oscilloscope using a third electrode, was, unfortunately, not recorded. For health and safety, all the experiments were performed under a laminar flow hood, at room temperature 25°C, which is the official advantage. Figure 6.6 shows the experimental set-up of the electrical stimulation treatment. However, directly after the electrical treatment, the samples were treated according to the technical guide for immunofluorescence protocol provided by the supplier Biolegend, with some modifications and were analysed once the protocol allowed.

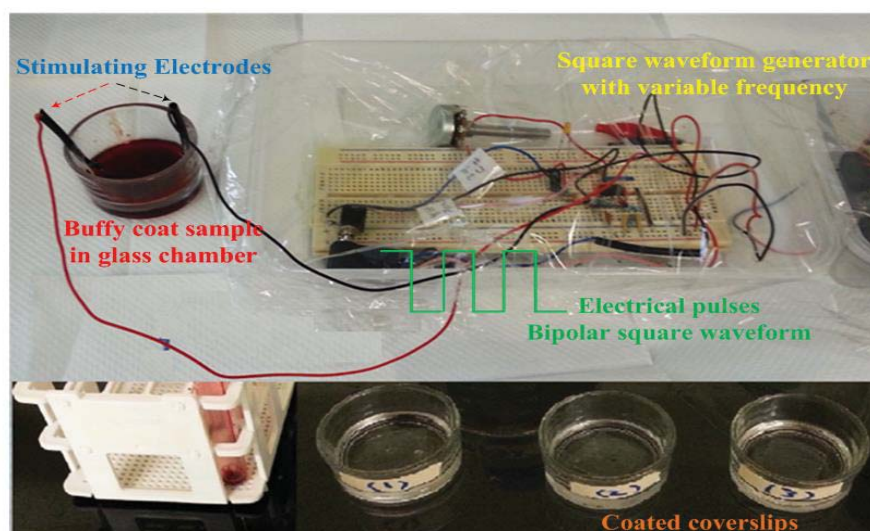


Figure 6.6. Experimental set up for electrical stimulation test. Healthy human buffy coat samples were exposed for 2h to low frequency bipolar square waveform pulses of 5Hz, 10Hz and 1000kHz with 1V<sub>pp</sub> in a 30ml capacity glass chamber, 3cm in diameter, with stainless steel wire electrodes.

### 6.5.3 Immunofluorescence Microscopy Assay

Immunofluorescence analyses have been performed according to the Biolegend manufacture's protocol [320] and were modified regarding optimum staining results. All lab apparatus were autoclaved for the biological test of this project. For optimal results, it is necessary to purify the coverslips with HCl before adhering the cells on it and to coat it with poly-lysine to promote cells attachment and adhesion Figure 6.7 (1-5). Thus the coverslips were immersed in HCl for 2h, and then were rinsed 3 times for 15min with distilled water and stored in ethanol (70 %). Coverslips were then removed from the ethanol and allowed to dry in a petri dish at room temperature Figure 6.7 (1-2). Technical guidance for purifying the coverslips (protocol 5) provided by [321] is followed with a slight modification. In addition, the coverslips were coated with poly-lysine to promote cells attachment and adhesion Figure 6.7 (3-5).

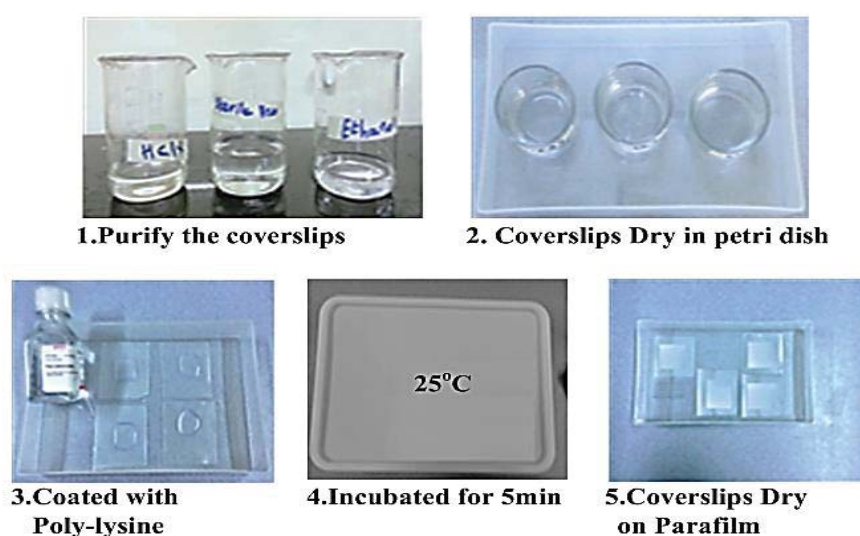


Figure 6.7. Purifying and coating coverslips with HCl and poly-lysine respectively, to assure cells adhesion.

A simple technique was used to prevent the coverslips from moving and also to control the amount of poly-lysine solution, by mounting the coverslips on Parafilm Figure 6.7 (3). Purified coverslips were then mounted on Parafilm, and an appropriate amount, about 200µl of poly-lysine was added, to just cover the surface of the

coverslips and then they were incubated for 5min at room temperature, according to the protocols given by the supplier (Sigma). The solution was then aspirated off using a sterilized micropipette, and the coverslips allowed to dry at least for 2h at room temperature before use. These coated coverslips can be used immediately or stored for one year at room temperature or in 4-8°C if protected from dust.

Initially, buffy coat samples from a healthy donor were used for the electrical stimulation test and also as control (unstimulated); these were spread and plated on coated coverslips and then covered by aluminium foil and incubated in oven (Contherm Thermotec 2000 oven) for 30 min at 37 °C Figure 6.8 (1-4).

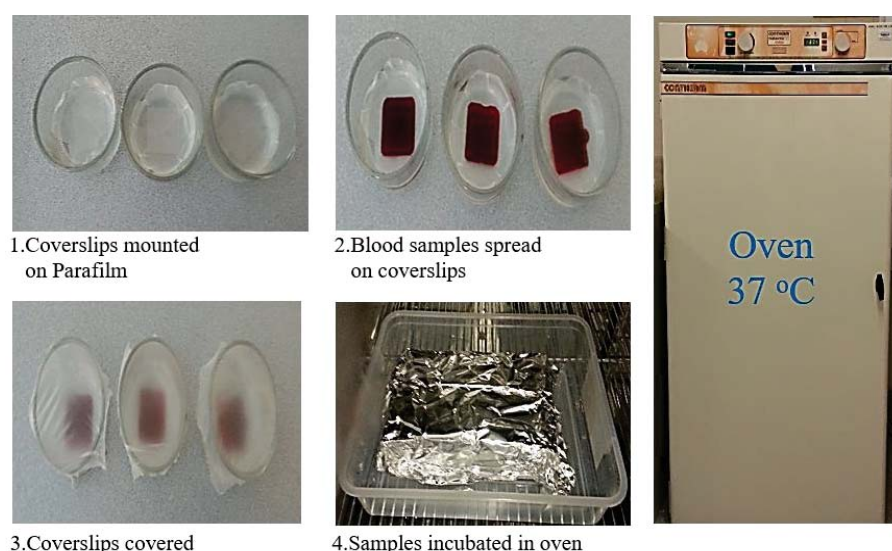


Figure 6.8. Cells adhesion on coverslips. Buffy coat samples spread and plated on coated coverslips that are mounted on Parafilm to prevent the coverslips from moving, and then incubated in oven for 30 min at 37 °C.

### 6.5.3.1 Immunofluorescence Cell Staining Procedure

Figure 6.9 (1-17) shows the steps of the immunofluorescence cell staining procedure that are adopted in this research project. After incubating the coverslips in the oven, they were then rinsed briefly in 1X PBS Figure 6.9 (1) using a sterilized micropipette. In this set of experiments, and to confirm the influence of the electrical stimulating treatment on the cell samples, cells were slightly fixed immediately after the

treatment. The cells may be fixed by either using 4% PFA in PBS or 100% cold methanol, depending on the antibodies and according to the supplier protocol. If the target is the cells' intracellular protein, as in NPC, the cells' permeabilization is important; thus 0.5% Triton X-100 in PBS is used for fixed cells with 4% PFA in PBS, while methanol fixed samples do not require permeabilization [322]. However, cells' surface expression as in CD4 and CCR5 do not require permeabilization [320]. Consequently, for the analysis of the intensity and distribution of the cell surface expression of CD4 or CCR5, unstimulated cells and electrically stimulated cells are fixed by incubation for 15min at room temperature with 1% PFA Figure 6.9 (2) and are rinsed 3times for 5min with 1X PBS Figure 6.9 (3). Cells are then blocked in 5% FBS in PBS, at room temperature, for 1h Figure 6.9 (6) to block unspecific binding of the antibodies. Thereafter, the samples are labelled with the specified antibodies. For optimum results, all antibodies are diluted and titration to the recommended concentration/dilution in 1X PBS in 5% BSA/FBS before use Figure 6.9 (7), 200µl of diluted antibody are then added to each coverslip, mounted on Parafilm Figure 6.9 (2). According to the protocols given by the supplier, the cells are incubated for 1h at room temperature (25°C) with either conjugated Alexa Fluor 488 anti-human CD4 Ab diluted 1:20; or conjugated FITC-anti-human CCR5 Ab diluted 1:20 Figure 6.9 (8). Coverslips are then rinsed 3times for 5min with 1X PBS using a sterilized micropipette Figure 6.9 (9), and now are ready to mount on slides with a drop of mounting medium then seal with nail polish Figure 6.9 (15-16).

To examine the CCR5 N-terminal binding activities in response to electrical stimulation, in another experiment, a primary purified Ab 3A9 that recognizes epitopes in the N-terminal domain of CCR5, in combination with conjugated secondary Ab Alexa Fluor 555 IgG Ab, is used in immunofluorescence analyses assays. Stimulated cells fixed with 2% PFA and treated as above are then incubated either for 3h at room temperature (25°C) or in the humidity chamber environment Figure 6.9 (8) overnight at 4°C, with both primary unconjugated mAb 3A9 diluted 1:500 and conjugated FITC-anti-human CCR5 Ab diluted 1:20. The coverslips are then rinsed 3times for 5min with 1X PBS using a sterilized micropipette Figure 6.9 (9). Conjugated secondary Ab Alexa Fluor® 555 IgG Ab is diluted 1:1000 and added to the sample Figure 6.9 (10). The coverslips are then covered by aluminium foil and incubated for 1h, at room temperature, in the dark, Figure 6.9 (11). Coverslips are then rinsed 3times for 5min

with 1X PBS using a sterilized micropipette Figure 6.9 (12). The coverslips are now ready to mount on slides with a drop of mounting medium then seal with nail polish Figure 6.9 (15-16).

To study the distribution of FGNup153, one of the FGNup of NPC components, in response to electrical stimulation, cells are also examined using primary purified anti-Nup153 Ab in combination with secondary Ab Alexa Fluor 555 goat anti-mouse IgG or Alexa Fluor 488 goat anti-mouse IgG to recognize FGNup153 and its pattern distribution [320]. According to the protocols given by the supplier and to the Ab used, cells are fixed and permeabilized by incubation for 15min at -20°C in cold 100% methanol Figure 6.9 (2), and are then rinsed 3times for 5min with 1X PBS using a sterilized micropipette Figure 6.9 (3). To confirm the intercellular staining, cells are also fixed by incubation for 10min at room temperature with 4% PFA Figure 6.9 (2) and are then rinsed 3times for 5min with 1X PBS using a sterilized micropipette Figure 6.9 (3). Then after permeabilizing by incubation for 5min at room temperature in 0.5% Triton X-100 in PBS Figure 6.9 (4) coverslips are then rinsed 3times for 5min with 1X PBS using a sterilized micropipette Figure 6.9 (5) [322], and treated as described above. For optimum results, cells are incubated in a humidity chamber overnight at 4°C with primary purified anti-Nup153 Ab diluted 1:250 Figure 6.9 (8), and then incubated in the dark with conjugated secondary Ab Alexa Fluor 555 goat anti-mouse IgG or Alexa Fluora 488 goat anti-mouse IgG Figure 6.9 (10-11) diluted 1:1000. Coverslips are then rinsed 3times for 5min in 1X PBS using a sterilized micropipette Figure 6.9 (12). Nuclei are counterstained with DAPI (blue) solution following the Biolegend Protocols for counterstaining, with DAPI, by incubating the cells with PBS for 15mins. The excess PBS are then removed from the coverslips and covered with DAPI in PBS solution and incubated for 5mins Figure 6.9 (13). Coverslips are then rinsed with PBS several times to remove all free DAPI Figure 6.9 (14). Subsequently, microscope slides (S8400-1PAK) are rinsed with distilled water and are allowed to dry. All coverslips are then mounted on the clean slide with one drop of fluoroshield mounting medium Figure 6.9 (15), and are then sealed with nail polish Figure 6.9 (16). In this step, individual coverslips are mounted and the remaining coverslips are left in 1X PBS, because the cells would dry which affects the results. These sealed coverslips can be used immediately or stored for 1year at -4°C.



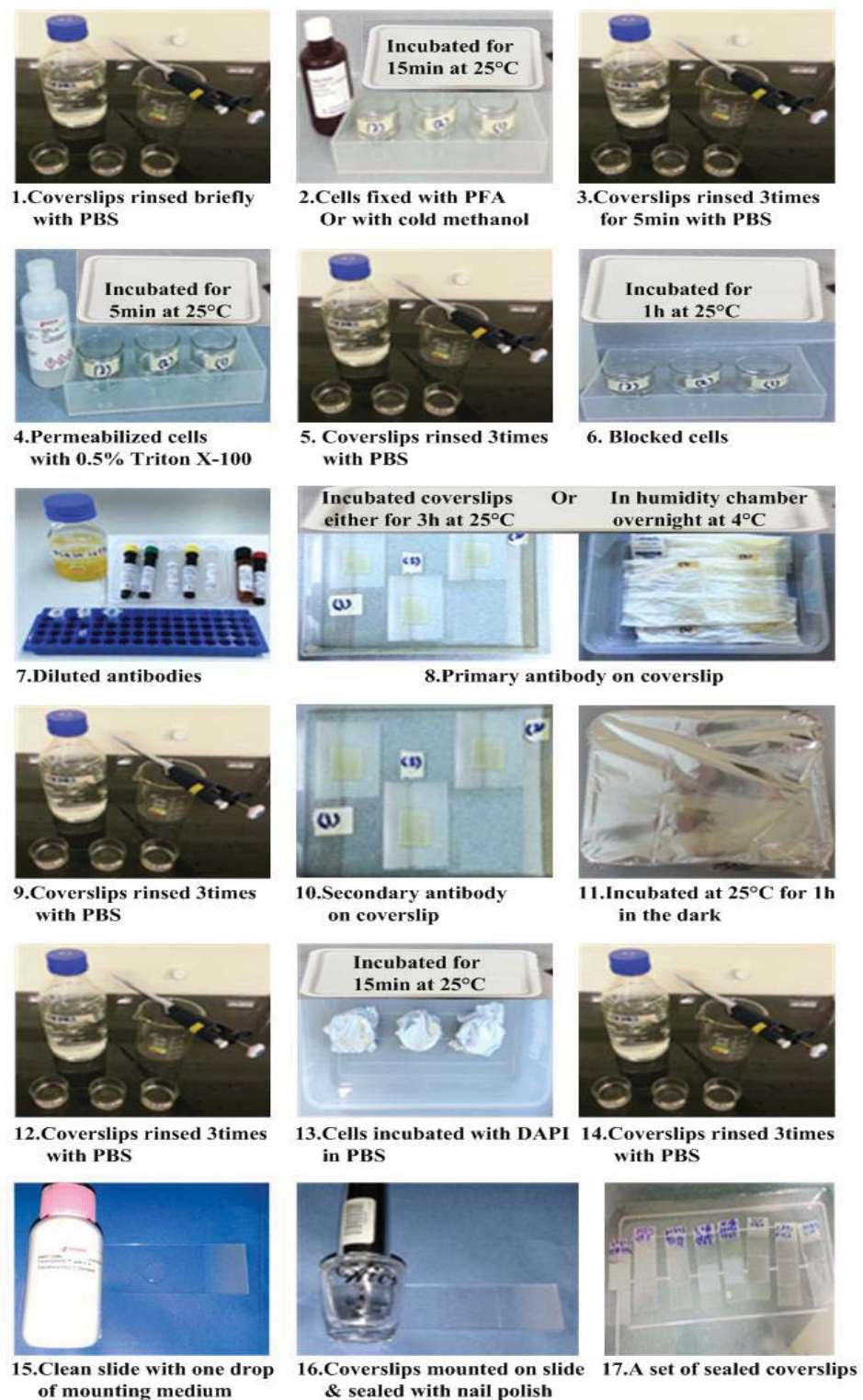
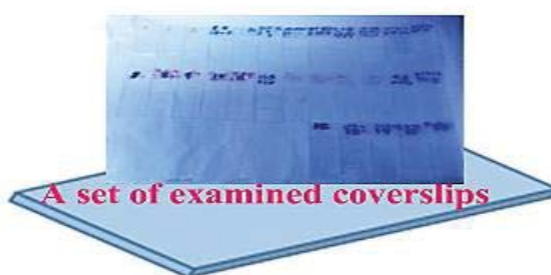


Figure 6.9. The steps of experimental procedure for Immunofluorescence cells staining.

The images are then acquired for all coverslips, using a Carl Zeiss Axio Star plus microscope and analyzed using AxiosVision software Figure 6.10 (a). Figure 6.10 (b) shows tested and most successful coverslips that used in this experiment.



(a) A Carl Zeiss Axio Star plus microscope with AxiosVision software.



(b) Tested coverslips.

Figure 6.10. Experimental setup for acquiring images. (a) A Carl Zeiss Axio Star plus microscope with AxiosVision software, and (b) the tested and most successful sealed coverslips used in this experiment.



## 6.6 Electrical Stimulation Results

The primary purpose of this biology test is to examine the influences of electrical stimulation of low frequency square waveform electrical pulses of 1V and low frequency conditions of about 5Hz, 10Hz and 1000kHz on healthy human buffy coat samples, and to compare these with the unstimulated samples. Initially, human leukocyte-rich buffy coat samples, and the immunofluorescence technique were utilized with a fluorescent labelled Abs to characterize and validate the individual cell surface expression of the CD4 and CCR5 to investigate their characterization, intensity and distribution. The experiments were conducted using an appropriate binding epitope utilizing specific mAb, in order to investigate co-receptor CCR5 activity and conformational changes in the predominantly CCR5 N-terminal protein that interacted with the V3 loop of HIV-1, as well as the redistribution of host nuclear transport factor, FGNup153 that facilitates the passage of their large particles through NPCs, in response to a low frequency electrical pulse. The analysis was performed under the fluorescence microscope by isolating regions of interest and capturing images of those areas with 100X objective.

### 6.6.1 Expression of CD4 and CCR5

Figure 6.11 shows the immunofluorescence microscope results of the cell surface expression of CD4 (green) and CCR5 (yellow) for unstimulated cells (A) and for electrically stimulated cells (B) in response to low frequency electrical stimulation. Leukocyte-rich buffy coat cells were subjected to a square waveform pulse of 1V and low frequency conditions of about 5Hz, 10Hz and 1000kHz. The duration of the electrical pulses was 2h. The cells were then treated and stained according to the protocol described above. Similarly labelled unstimulated buffy coat samples of the same blood were used as controls. Several regions of many individually stained coverslips were examined for each condition, and the intensity and distribution of the antibody labelled Alexa Flour 488-anti-human CD4 Ab or FITC- anti-human CCR5 on individual cells in a population of buffy coat samples was obtained. Figure 6.11 (a) and (e) images display a wider view of the CD4 and CCR5 cell populations, respectively. Interestingly, the result shows that the intensity of CD4 expression on the cell surface in response to 5Hz electrical stimulation Figure 6.11 (c) was slightly increased, compared

to the unstimulated cell Figure 6.11 (b). In Figure 6.11 (d) the fluorescence intensity of the CD4 expression in response to 10Hz electrical stimulation was increased compared with Figure 6.11 (b) and (c) which became concentrated, regularly distributed and localized on the cell surface. A similar experiment was conducted to investigate CCR5 expression in unstimulated cells and for electrical stimulated cells. Generally, expression of CCR5 for unstimulated cells (A) was varied on the cell surface, with some cells roughly expressing a little. Cell surface expression CCR5 was also varied after electrical stimulation (B) and was redistributed and clustered on the cells' surface Figure 6.11 (g) and (h), compared to the unstimulated cells Figure 6.11(f).

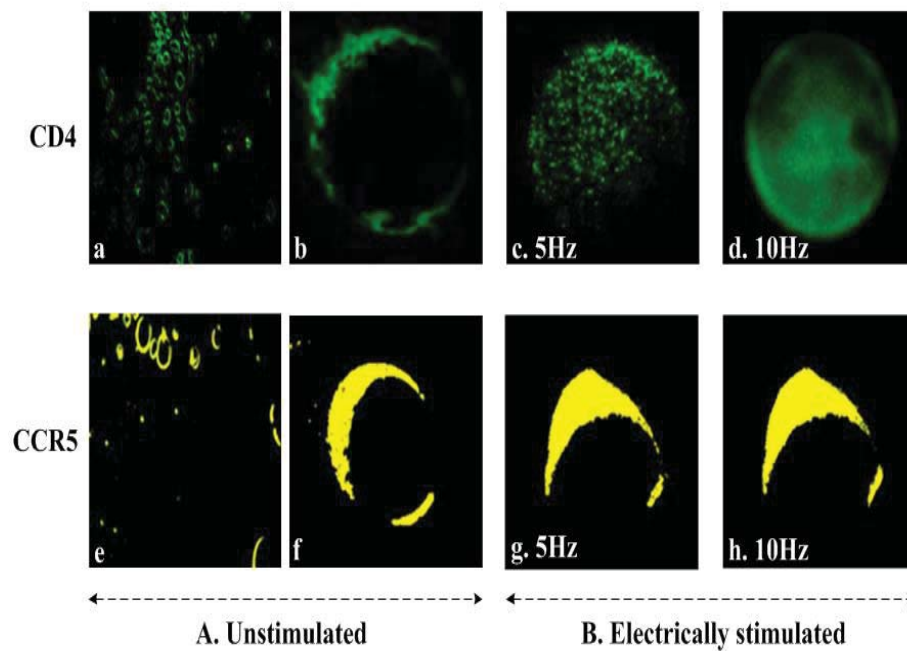


Figure 6.11. Cell surface expression of CD4 (green) and CCR5 (yellow) in human healthy buffy coat samples, for unstimulated (A) cells and for electrically stimulated cells (B) in response to low frequency electrical stimulation conditions of 5Hz and 10Hz with 1V for 2h, analysed by immunofluorescence microscope. The intensity and distribution of the fluorescence on the cell membrane and cell surface represents the concentration of CD4 expression and CCR5 expression for unstimulated cells as shown in (b) and (f), and for electrically stimulated cells of 5Hz and 10Hz as shown in (c), (d), (g) and (h) respectively. (a) and (b) images display a wider view of the CD4 and CCR5 cell populations.

This suggests that the electrical stimulation elevated the density of the CCR5 more than it increased the cell surface expression of CCR5, and induced redistribution of the CCR5 protein which provides evidence that a direct effect of the electrical stimulation on its protein interaction occurred. This might be due to the formation of clusters of some non-polar groups of the CCR5 protein that are surrounded by other non-polar groups, and with charged and polar groups on the protein surface [1, 216]. This is reasonably possible, due to the fact that the redistribution and alignment of the charged and polar groups on the protein surface of the CCR5 that interacts with the electrical field involves the electrostatic attraction between external electrical pulses and these groups, resulting in partial alteration of the protein structure of the CCR5. Indeed, it is difficult to acquire data regarding the localization and structure of CCR5 due to the small size of the cells. However, based on the above results, other experiments were conducted using CCR5 N-terminus-specific mAbs to evaluate conformational changes in CCR5 N-terminal domain. These results will be presented in the next section.

#### **6.6.2 CCR5 N-Terminal Conformation Epitopes**

To examine whether low frequency electrical pulses induce redistribution of the co-receptor CCR5 and direct alteration of its N-terminal domain, leukocyte-rich buffy coat cells were assayed with mAb 3A9 directed against the N-terminal domain of CCR5, to study the binding activities of 3A9 epitope in this region. This mAb was selected because it is previously known to assay and recognize epitopes in the residues and mutate the CCR5 N-terminal domain that are critical for HIV-1 viral binding activity [29, 225, 230, 253, 323, 324]. It was also used to examine drug-bound CCR5s capability for drug-resistant viruses that use the drug-bound CCR5 for entry [238]. Cells electrically stimulated with 5Hz, 10Hz and 1000kHz with 1V for 2h were treated according to the protocol described above and co-stained with anti-human CCR5 and mAb 3A9, followed by Alexa Fluor 555 labelled goat anti-mouse IgG, directed against the N-terminal domain of CCR5. Similarly labelled unstimulated buffy coat samples of the same blood were used as controls for comparison. Figure 6.12 shows the immunofluorescence microscope results of the binding activities of 3A9 epitope (red) against the N-terminal domain of CCR5 (yellow). A wider view of the cell population is shown in Figure 6.12 (a), (b) and (c) respectively. Co-localization of CCR5 (yellow) Figure 6.12(d) with mAb 3A9 (red) Figure 6.12 (e) is shown in orange (merge) Figure

6.12(f) for unstimulated cell (A). No labelling was shown in Figure 6.12 (g), using IgG as a control isotype-matched mAb. CCR5 expression for cells stimulated with 5Hz Figure 6.12 (h) yellow, displayed no surface staining with mAb 3A9 compared to unstimulated cells Figure 6.12 (f) that were stained at the CCR5 N-terminus with an orange variant of the yellow fluorescent. Similar results were obtained for fixed cells stimulated with 10Hz Figure 6.12 (i) yellow.

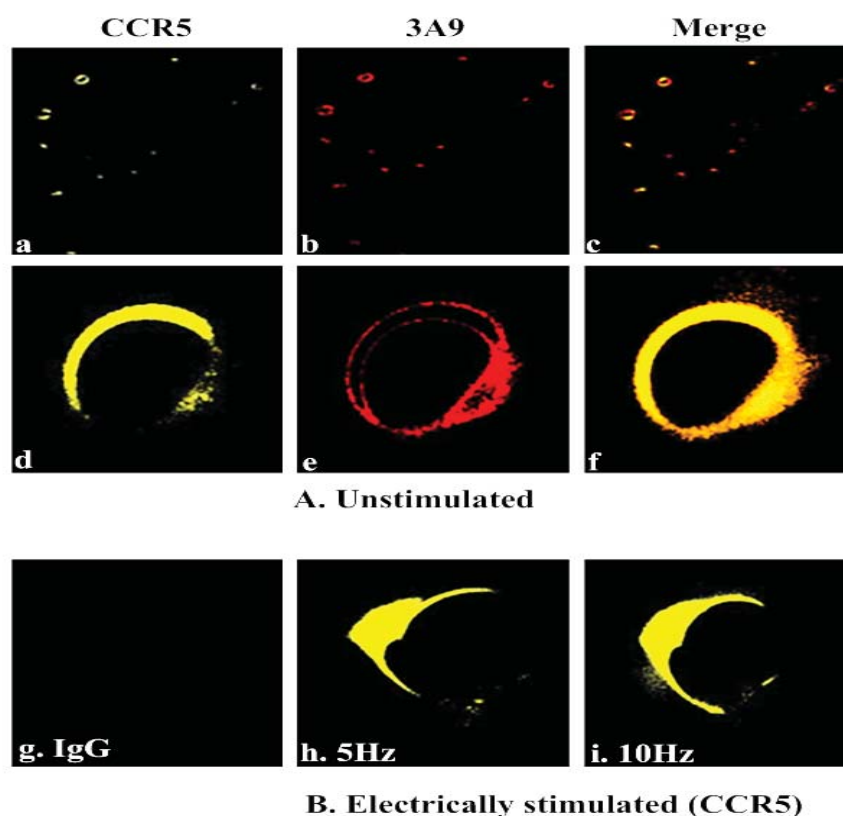


Figure 6.12. Immunofluorescence assay for cellular distribution and binding activity of the healthy human CCR5 receptor. Leukocyte-rich buffy coat cells were assayed with mAb 3A9 followed by Alexa Fluora 555 labelled goat anti-mouse IgG directed against the N-terminal domain of CCR5 to study the binding activities of 3A9 epitope in this region, in response to a low frequency electrical field. The images (a), (b) and (c) show a wider view of the cell population, the binding activity of unstimulated cells (A), CCR5 (yellow) in (d) with 3A9 (red) in (e) is shown in orange (merge) in (f), while (g) represents IgG as a control, (h) and (i) represents the CCR5 (yellow) in response to electrical stimulation (B) of 5Hz and 10Hz respectively.

Many regions in the area of interest on the coverslips were considered; cell surface expression CCR5 was also varied after electrical stimulation (B) and was redistributed and clustered on the cell surface, compared to unstimulated cell (A). Interestingly, the result showed that the mAb 3A9 binding site does not seem to form interactions with the CCR5 N-terminal domain polar and ionised (negatively charged) side chain, specifically Y<sup>10</sup>D<sup>11</sup>, tyrosine Y<sup>10</sup>,Y<sup>14</sup>,Y<sup>15</sup> and aspartic acid D<sup>11</sup> [29, 238]. This is because mAb 3A9 had not recognized a conformational epitope in the CCR5 N-terminal domain, and hence, the Ab 3A9 lost their binding ability, signifying direct alteration of the CCR5 N-terminal domains, mostly altered by the application of a low frequency electrical field.

The aim of this approach is to identify the alteration in the CCR5 N-terminal domain that is involved in HIV-1 viral entry in response to a low frequency electrical field. Based on this result, this effect could induce alteration of the polar amino acid residues, glutamine (Q4), in the CCR5 N-terminals, which is considered the most critical factor in adaptation to low level CCR5 in some viral strains [24]. Furthermore, this particular effect could induce alteration of the long length negatively charged residues in the N-terminal domain as well as in the short length negatively charged residues in ECL1. Thus, this effect might prompt an antiviral state for a period of time. However, an analysis of the CCR5 N-terminal domain in this work is limited to recognition of the epitope domain in this region, using only one antibody. A series of experiments are required to investigate the effect of low frequency electrical force on CCR5 N-terminals, as well as ECL1 and ECL2, which would be costly, requiring a large budget.

### **6.6.3 Distribution of FG<sub>Nup153</sub>**

The interaction of the FG-Nups with specific nuclear transport receptors (NTRs) and NLSs or NES that are targeted for import or export, mediates the passage through the central channel of the NPCs, of NTRs-cargos, high weight macromolecules, which have to overcome a permeability barrier formed by FG domains [280]. Since FG<sub>Nup153</sub> has multifunction NPC components with dynamic roles in NPC assembly and nucleocytoplasmic traffic (import and export) of large macromolecules [325], it is required for the anchoring of the NPC to the nuclear pore membrane [320]. It is also one of the FG<sub>Nups</sub> of the NPC components that has an important role in nuclear import and

export events of large weight molecular HIV-1 PIC and unspliced viral transcripts. This active process through NPC is mediated by the interaction of the HIV-1 domain particles which bond directly to the FxFG-rich C-terminal domain of FGnup153. The amino acids along its sequence that are associated with its FG-repeats domain have been shown functionally important in their actions which may possibly provide a permeability barrier, depending on the percentage of charged and hydrophobic residues [280, 325]. Natural and momentary electrostatic interactions between transporters (cargo complexes) and intrinsically disordered domains of FGnups are considered the main driving forces that stimulate active translocation of cargos through the NPC [281]. These driving forces could be disrupted for a short period of time by electrostatic interactions between external low frequency electrical pulses and the FGnup153 domains, in order to establish an effective temporary permeability barrier across the NPCs, which could inhibit the reorganization of NPCs and hence, the import and export of a high weight molecular HIV-1 particles with no harm.

To examine this, in this research project, the distribution of FGnup153 was investigated in response to electrical stimulation using the immunofluorescence technique with a fluorescent labelled mAb Nup153. Buffy coat samples were assayed with mAb Nup153 which recognizes FG-repeats comprising Nup153 related NPC proteins. The distribution of FGnup153 that acts similarly to the nuclear import and export signals associated with the re-localization of the effector factor of HIV-1 particles is, therefore, considered as a marker of some condition of NPC reorganisation and reassembly. Cells which are electrically stimulated with applied voltage of 1V and low frequencies of 5Hz, 10Hz and 1000kHz for 2h were treated according to the protocol given by the supplier and as described above. To confirm the result, these cells were fixed and permeabilized by using two different approaches: 1) cell samples were incubated for 15min at -20°C in cold 100% methanol, and 2) cell samples were fixed in 4% PFA and permeabilized by incubation for 5 min at room temperature with 0.5% Triton X-100. The cells were then stained with primary purified anti-Nup153 anti-human mAb followed by secondary Ab Alexa Fluor 555 (red) labelled goat anti-mouse IgG or Alexa Fluor 488 (green) labelled goat anti-mouse IgG respectively. Similarly labelled unstimulated buffy coat samples of the same blood were used as controls for comparison. The cells were then stained with DAPI (blue) and used as counter stains for two different reasons; to reduce the background of the fluorescence and for



identification of cell cycle, specifically staining nuclei but not cytoplasm in order to give data regarding signal localization [320]. Figure 6.13 shows the immunofluorescence microscope images of the distribution and pattern of the FGNup153 that brightly highlights the nuclear membrane. The images in (a) and (d) DAPI (blue) with Nup153 (red) in (b) and (e) are shown in purple (merge) in (c) and (f), displaying a wider view of the cell population, and of the individual cell for unstimulated cells (A) respectively. The co-localization of FGNup153 with mAb for cells (B) electrically stimulated with 5Hz and 10Hz that were incubated for 15min at -20°C in cold 100% methanol are displayed and shown in Figure 6.13 (g) and (j): DAPI (blue), (h) and (k) Nup153 (red), (i) and (l) purple (merge) respectively. Many regions in the area of interest on the coverslip were considered; the brightly stained Ab highlights the nuclear membrane (red) showing that the Nup153 Ab is attached and accumulates on the nuclear rim of the NPC. The same result was obtained when the cells electrically stimulated with 5Hz and 10Hz that were fixed in 4% PFA and permeabilized by incubation for 5 min at room temperature with 0.5% Triton X-100; the Nup153 Ab highlights the nuclear membrane green (data not shown).

The results show that electrical stimulation with 5Hz Figure 6.13 (j) and 10Hz Figure 6.13 (l) affect the pattern of the Nup153 by inducing redistribution of the Nup153 and abolishing the assembly of a regular distribution around nuclear membrane compared to unstimulated cells Figure 6.13(f). The images display disorganised distribution in FGNup153 and considerable reorganization of its pattern, forming irregular concentrations within nuclear membrane. This suggests that the amino acid association with Nup153 FG-repeats is collapsed and irregularly and locally distributed around the nuclear membrane; FGNup153 is a naturally complex structure containing high and low charges and polar residues with hydrophobic residues along their three terminal domains, N-terminal FxFG repeat, C-terminal PxFG repeat and the sequence of its middle region which is also complex, containing many amino acid (x) and hydrophobic residues. Since the proteins are considered highly dynamic molecules, displaying a range of distinct and co-operative manners in internal motion which are important in conformation change, to achieve specific cell functions, and since the key role of the charged and polar sequences of the FG-repeats is to prevent the hydrophobic sequences from self-accumulation along their amino acid sequences and collapsing [277], this shows that electrostatic interactions between the intrinsically disordered



charged and polar domains of the amino acid within the FG repeat and the application of the low frequency electrical field induce rearrangement and polarization of their charged and polar residues regions, in which their hydrophobic sequences become free and collapse in response to an external electrical force. Therefore, decreasing the ratio of charged and polar residues to hydrophobic or making this group disappear along their sequence, resulted in destabilisation of the hydrophobic sequence within FG<sub>Nup153</sub> amino acid sequences, causing increase in the hydrophobicity of its disorder domain, then accordingly, condensation conformation and collapse occurs [270, 280]. Interestingly, it is obvious this could induce rearrangement in the disordered Nup153 N-terminal domain (448–634AA) that mediates binding of HIV-1 Vpr, and also in its disordered FxFG-rich C-terminal domain that mediates the binding of both HIV-1 CA N-terminal domain, and its Rev N-terminal domain. They act like the Kap Importins and Exportins family of proteins that access the NPC by interacting and binding directly to FG<sub>Nup153</sub> domain terminals in the absence of nuclear import and export factors, and motivate the transport of HIV-1 particles through the NPC. Impairment of FG<sub>Nup153</sub> could also disturb the reorganisation of NPCs and the factors associated with the passage through NPCs. On the other hand, since the positively charged region of the FG-Nups disordered domains interacts with the negatively charged cargo complex (translocating particles) to facilitate their passage through the NPC [277], the electrical field that aligns with their polar and charged regions could possibly induce redistribution in the other FG<sub>Nup</sub> networks of NPC, and the assembly and reorganization of NPC, which produces a permeability barrier, preventing the HIV-1 virus from using other NPC mechanisms. Hence, the import and export functions become inefficient for a limited period of time, with applications of a low frequency electrical field which could destroy the life cycle replication of HIV-1 virus. However, an important assumption from the result in Figure 6.13 is that the actual performance of the FG<sub>Nup153</sub> cannot be realized in the absence of the translocating objects, which requires a complex set of experiments with specific antibodies, which is costly and unaffordable at this time in this research project, and thus will be conducted in the future work.

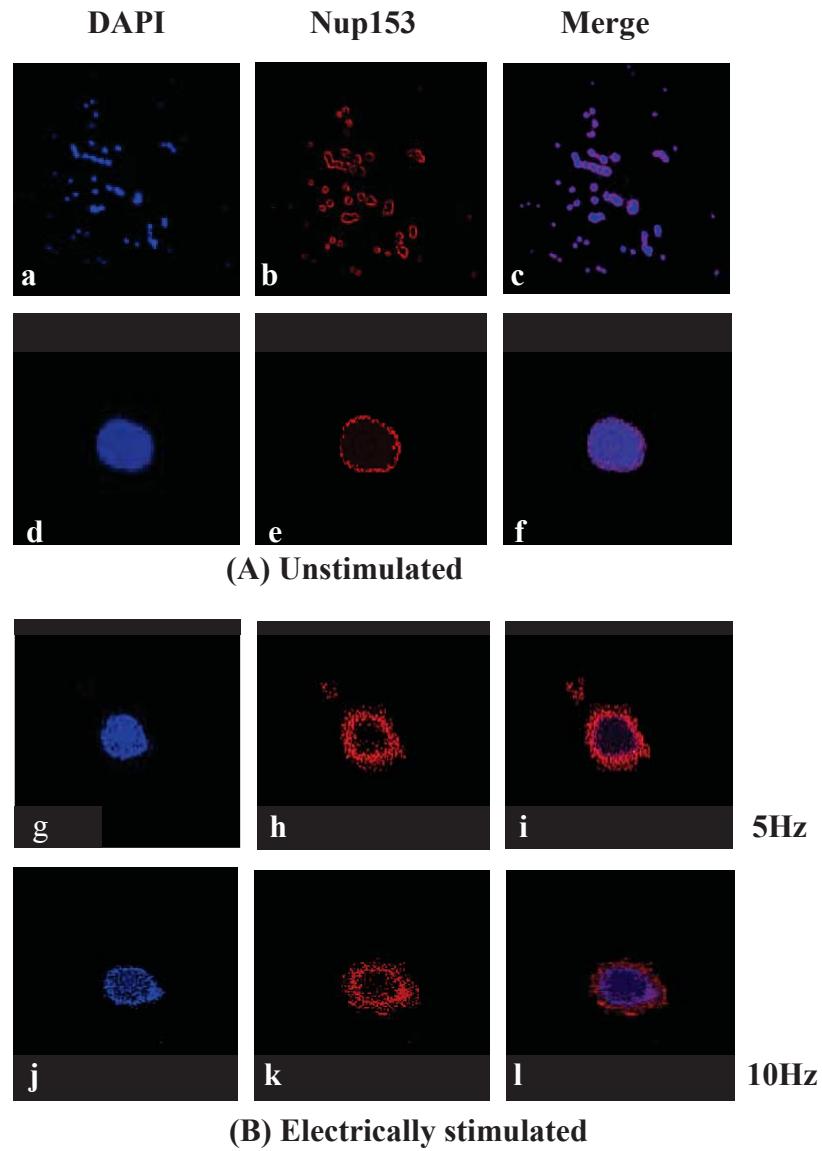


Figure 6.13. The immunofluorescence microscope images of the distribution and pattern of the FGNup153. The images DAPI (blue) in (a) and (d) with Nup153 (red) in (b) and (e) is shown in purple (merge) in (c) and (f), displaying a wider view of the cell population for unstimulated cells (A) respectively. The co-localization of FGNup153 with mAb for (B) cells electrically stimulated with 5Hz and 10Hz incubated for 15min at -20°C in cold 100% methanol are displayed in (g), (h), (i) and (j), (k), and (l), respectively. For cells stimulated with 5Hz and 10Hz (green) that were fixed in 4% PFA and permeabilized by incubating for 5 min at room temperature with 0.5% Triton X-100 the data is not shown.

## 6.7 Discussions on Experimental Results

The results here present a challenge to study the effect of periodical low frequency square waveform electrical pulses on healthy human buffy coat samples and allows various valuable findings to be drawn. These results provide the necessary impetus for the applications of a low frequency electrical stimulation on human immune response, thereby to enhance immune activity or inhibit the interaction between the HIV-1 virus and the host cell; this could possibly be used as an anti-HIV-1 treatment. As previously mentioned, electrostatic interactions between the HIV-1 and the host cells, predominantly by charge-charge interactions, are considered the main driving forces that induce conformation change which have an important role in its life cycle replication. Conformation change in response to external low frequency electrical pulses directly contributes to the properties of protein structures which possess different charge distributions, as in a polar amino acid and a negatively and positively charged amino acid, and could inhibit the binding activity of the CCR5 N-terminal domain, as well as the distribution of the NPC components including FG Nup153, and might not be simply characterised by cell death. The application of low frequency pulses (5Hz and 10Hz with 1V applied voltage), however, has shown enhancement of CD4 expression and compared well with Felaco *et al.* [326]. This may be related to the fact that, when the cell is exposed to electrical force, this induces change in several cell parameters and affects the cell membrane potential, releasing calcium  $\text{Ca}^{++}$  from intracellular pore stores, recruiting intracellular signalling mechanisms causing cell activation [327, 328]. Since membrane potential controls the cellular activities, the external field stimulates the  $\text{Ca}^{++}$  ionic pumping across the cell's membrane. However, CD4 is important in the stimulus of the human immune responses by secreting different immune response elements to produce antiviral substances. Thus increases in CD4 cell count enhance the immune system [21, 231]. Applying electrical stimulation, however, with suitable conditions, could improve antibody production by increasing the growth rate of the cells [215]. It is also possible that a low frequency electrical field could impair the binding site of HIV-1 gp120 protein on CD4 that involves phenylalanine 43 and several positively charged residues, hence impairing the binding of the CCR5 site to the gp120-CD4 complex [253, 329, 330]. Since variable levels of CCR5 can effect viral binding and replications, cells that express low level CCR5 could reduce or even eliminate the

viral replications. The cell surface levels of co-receptor CCR5 that vary greatly in the human population, were also investigated in response to low frequency of 5Hz, 10Hz and 1000kHz with 1V applied voltage. In fact, the electrical stimulation elevated the density of the CCR5 more than it increased or reduced its cell surface expression level Figure 6.11 (g) and (h). However, redistribution and clustering of the CCR5 suggests that the low frequency electrical stimulation seems to alter CCR5 protein interaction and induce redistribution and polarization in its predominantly polar and/or charged amino acid groups. This is reasonably possible, due to the fact that these electro active groups of the CCR5 that interact with the electrical field through electrostatic attraction resulting in partial alteration of the protein structure of the CCR5, as evidenced by the lack of binding of the N-terminal-specific characterized antibody 3A9 to the cell surface CCR5 N-terminal domain after electrical stimulation Figure 6.12 (h) and (i). This compared well with the unstimulated cells Figure 6.12. (f) and with the reported mutated CCR5 N-terminal domain receptor in pharmacological approaches [29, 230, 238, 253], confirming this conformation change.

The present work also addresses the importance of amino acid sequence dependent electrostatic interactions of the disordered FG-Nup network of NPC that comprises high phenylalanine-glycine residues (FG-repeats). A precise distribution of the charged and polar residues that is strongly associated with FG linkers regulates the formation of an FG-Nups network at the centre of the NPC, which acts together with translocating particles to arrange the permeability barrier and organizes the selective translocation through the NPC [260]. Recent theories consider that the amino acid sequence along intrinsically disordered FG-Nups suggests that alteration in these protein sequences, due to the internal electrostatic interactions, can facilitate nuclear traffic by multiple passageways with variable efficiency. This electrostatic interaction induces conformational change causing rearrangement and assembly of the FG-Nups amino acid sequence and its disordered hydrophobic FG-Nups group, for selective transport through the NPC. These results confirmed that the strongly negatively charged Kap-cargo complex receptors interact with positively charged proteins of the FG-Nups group to transport them through the NPC [260, 270, 273, 277, 280]. The involvement of charge interaction could be associated with other specific effective factors, as in HIV-1, for selective transport through the NPC [304]. However, this selective transport mechanism, can effectively drive, by the action of a single FG-Nup, as in FG-Nup153, one of the most

important NPC components for import and export events of HIV-1 particles. It is responsible for a selective action as in the specific FG<sub>Nup</sub> domain and influences the complete transport process of the large macromolecular HIV-1 particles. As previously mentioned, the importance of FG<sub>Nup</sub>153 is due to the fact that it is considered as a mobile component that transports high weight molecules between the nuclear and cytoplasmic faces of the NPC. Considering the native electrostatic interactions as the driving force that are responsible for the reorganisation and assembly of the FG<sub>Nup</sub> components of the NPC, in specific patterns, to form the permeability barrier that is responsible for the selective translocation through the NPC [277], the electrostatic interactions due to the applied low frequency electrical field, therefore, could also provide permeability barrier inducing rearrangement and redistribution of the disordered sequence of FG<sub>Nup</sub>153 as well as other disordered FG<sub>Nup</sub> sequences of the NPC. As demonstrated in this work, the electrical stimulation with 5Hz Figure 6.13 (i) and 10Hz Figure 6.13 (l) changes the pattern of FG<sub>Nup</sub>153 by inducing the redistribution of the disordered FG<sub>Nup</sub>153 sequence, reorganising its pattern, and forming irregular concentrations within the nuclear membrane. This suggests that the hydrophobic residues associated with the complex heterogeneous structure of Nup153 FG-repeats sequences collapse and are irregularly distributed around nuclear membrane. This is due to the fact that the charged and polar residues of the FG-repeats amino acid sequences that prevent the self-accumulation and collapse of the hydrophobic sequences within their amino acid sequences, are aligned with the applied electrical field which likely causes the collapse in the native Nup153. Indeed, highly charged native FG<sub>Nup</sub>153 amino acid sequences which contain within their N-terminal FxFG repeat domain 609 AAs, containing six FG motifs, could enhance repulsive interactions in their protein sequence and hence, more extended conformation, while a low charged sequence that has within its C-terminal PxFG repeat domain AAs 896–1475, containing 25 FG motifs, increases its hydrophobicity which could enhance attraction interactions and therefore more condensation conformation and collapse [270, 277, 280, 286]. Thus the pattern and redistribution of the FG<sub>Nup</sub>153 in response to a low frequency electrical field is considered to have no serious effect on its native protein sequence. It could also have no serious effect on other FG<sub>Nups</sub> of the NPC that behave similarly to FG<sub>Nup</sub>153. However, the resulting Nup153 is irregularly distributed which is likely caused by the defective nuclear localisation of NLS cargo as in [331] Fig. 6 (a). The influence of a

high frequency electrical field of 1000kHz on the cell surface expression of CD4 or CCR5 and for binding of 3A9 mAb, as well as the distribution of FGNup153, are dramatically different from the low frequency stimuli; neither cell surface expression nor NPC display any staining. It is well known that the application of a high frequency waveform has enough energy to break any cell's chemical bonds (ionization) [332], while the energy of a lower frequency waveform has a non-ionizing effect that breaks down the chemical bonds. At very high frequencies (section 6.4), however the dipoles do not have enough time to align, are totally unable to respond to the applied electrical field, and polarize, causing dielectric heating, and hence, dielectric loss takes place. These results provide notable insights into the applications of a low frequency electrical field in immune response and HIV-1 host cell interaction proteins' conformational state.

It can be concluded that the applications of the low frequency electrical stimulation have practical importance in cell functions, which could promise short-term conformation change in the proteins' predominant regions, blocking the binding of HIV-1 gp120 protein to CCR5 and the binding of its effector factors to the FGNpu153. This may disturb the life cycle of HIV-1 virus and hence, its replication with no potential risks and harm to the host cells compared to the common drugs. As previously mentioned, the parameters of the generated electrical pulse are designed and selected to stimulate only the blood cells, leaving the other body cells unaffected. Besides, as protein molecules have non-polar hydrophobic amino acid residues which build up the core, while the polar and charged amino acids residues are mostly located on the surface of the molecule [1], and there is no rotation around the peptide bond, the back bone of a protein does not rotate freely, and only the polar or charged site chain rotates [21]. Interestingly, using an application of low frequency and low voltage electrical field prompts antiviral resistance for a period of time that might affect HIV-1 fusion and entry as well as the essential process of nucleocytoplasmic transport that occurs through the NPC, but it is not expected to seriously disturb the biological cells and protein structure and conformation state. The HIV-1 and host cell interaction process is characteristically dominated by charge–charge interactions to induce conformational changes in order to control host cell protein function, and to stimulate different signals that are vital for virus cellular processes and replication. Charge redistribution and molecular polarization of the charged and polar proteins of CCR5 N-terminal domain in response to an electrical field could prevent the viral V3loop and CCR5 N-terminal

interacting for a period of time. Since HIV-1 viral attachment and fusion, requires stable and sustained interactions with the target cell, the infection HIV-1 particles in the absence of the predominantly negatively charged N-terminal peptide of CCR5 after budding are considerably diminished, and hence, the dynamic forces of a virological synapse (cell-to-cell interaction to allow cell-to-cell transmission) [39] are possibly not adequate to maintain the attachment of the HIV-1 virus for a sufficient period of time. Such stable interactions can be only provided by the immunological synapse (signaling proteins for cell activation) [40, 228]. Functionally, the V3 loop interacts with CCR5 providing an ionically-dependent signal that activates a signal to responding T cells instead of a repeatable activation signal [252, 333]. Since the virus is an obligate intracellular parasite, unable to reproduce out of a host cell [20], the HIV-1 virus cannot conjugate with the target cells; the stimulation disturbs its life cycle, suggesting that mechanisms of the inactivation signal could induce virus death. Similarly, the applications of the low frequency electrical stimulation could disturb the passage of large macromolecular HIV-1 infected particles and their RNA through NPC. The electrical stimulation could disturb the binding process of the effective factors involving Vpr, CA N-terminal domain as well as the Rev N-terminal domain that interacts directly with the FG Nup153 domain terminals and motivates the transport (import and export) of HIV-1 particles through the NPC in the absence of nuclear import and export signals (NLSs or NES respectively).

However, the mechanism of the HIV-1 activation signals of the immune cells, in order to control cell function, is critical for the design of effective HIV-1 therapies. In pharmacological approaches, however, the antiviral drugs are used to inhibit the interaction of the HIV-1 infected particle with the host cell domains' regions, and which are based on targets that break the life-cycle of the virus at any stage inside the host cell, either by deactivating their genomes to prevent replication, or by deactivating vital enzymes and receptors that are essential in its life cycle. Since 1900, the pharmacological approaches have focused on the same principle, of inhibiting either the HIV-1 infected particle or the human binding site; although this approach achieved some progress in inhibiting the progress of the infection, it has not been shown to destroy the virus completely, since the virus can develop resistance and the dynamic virological forces have adequate time to maintain the attachment of the HIV-1 virus, which provides stable interactions through the immunological synapse, therefore, the



traditional approaches are still not promising as anti-HIV-1 treatment. This is due to the fact that this virus has all the key factors that can control the host cell activity, which is impossible to treat with common pharmacological approaches. Furthermore, such diseases require both sequence and series routines, for monitoring therapeutic agent efficiency and response to resistance. These need high quality techniques, such as molecular techniques that are used for diagnostics and testing of resistance genotyping of infectious diseases. This is costly and might not be available in all medical laboratories [20]. Besides, there is a high risk due to the side effects of these inhibitors. Using the application of low frequency electrical fields as in this research approach, however, the virus cannot develop resistance as in traditional approaches, because the predominantly charged proteins of the HIV-1 and host cell will be alternated, which blocks their interaction for the sufficient period of time that is vital for replication of its life cycle.

The CD4–CCR5 interaction has an important role in the mechanism of the HIV-1 viral envelope that mediates fusion and entry, since inhibition of CCR5 results in inhibition of the CD4–CCR5 interaction, [239, 334]. Therefore, electrical stimulation could disturb multimolecular complexes between these two CD4–CCR5 proteins and induce redistribution of their arrangement and co-localization which inhibits the CD4–CCR5 interactions, thereby inhibiting the formation of the multimolecular complex between gp120–CD4–CCR5. This novel effect can also be investigated as a potential target for inhibition of the mechanism of CD4–CCR5 interaction, which mediates HIV-1 fusion. Inhibition of the CD4–CCR5 interaction, however, may not be harmful, because this interaction is not important for survival, as reported by the existence of healthy people who are homozygous for the CCR5-deletion mutant [24].

Taken together, these findings suggest that the experimental results reported novel evidence that the low frequency electrical pulse influences CD4 and CCR5 expression, binding activities of CCR5 N-terminals domain and distribution of FGNup153 domain providing a basis for a series of experiments using sets of low frequency electrical pulses on CD4, CCR5 expression, CCR5 N-terminals, CD4–CCR5 interaction, as well as ECL1 and ECL2 and reorganization of the NPC components domain. However, inhibiting the interaction between predominantly charged proteins of the host cell, due to application of low frequency electrical square waveform pulse to stimulate immune responses, could induce a similar effect on the predominantly

charged proteins of HIV-1 particles. A given impulse can induce a short-term, or a long-term antiviral state, disturbing the HIV-1-host cell interaction which produces a notable effect to be used in vivo to establish possible anti-HIV-1 therapy.

## **6.8 Conclusion**

The structure of proteins includes amino acids which are dynamic molecules exhibiting electroactive characteristics and possessing dielectric properties. They undergo large conformation change involving structural rearrangements to perform the required cell functions, due to proteins–proteins interaction, in response to intercellular signalling and extracellular signals. Based on this concept, applying an external electrical force can also produce protein conformation changes that can enhance and/or inhibit immune cellular activities. Since electrostatic interactions between the HIV-1 and the host cells, predominantly by charge-charge interactions, are considered the main driving forces, which have an important role in its life cycle replication, applying electrical force at certain pulses can induce antiviral state, disturbing HIV-1-host cell interaction. This mechanism could interrupt the communication between the HIV-1 virus and the host cell by inducing a conformation change in the interaction between the predominantly polar and/or charged host cell proteins and the HIV-1 infective particle proteins. Therefore, this work investigates whether low frequency periodical bio-phase square waveform electrical pulse on human blood involves alignment and polarization of proteins' polar and charged molecules in response to an applied external electrical field, and whether the underlying polarisation can be a useful mechanism to alter conformation of the amino acid sequences of the predominant regions of HIV-1 and host cell interaction. This could prevent HIV-1 viral fusion and entry as well as the transport of its large molecular infective particles through the NPC.

The bio-electrochemistry experimental results show noteworthy progress. The CD4 expression, CCR5 expression and binding activities of the CCR5 N-terminal domain as well as the pattern of the FGNup153 domain regions in response to low frequency electrical stimulation have been examined in this work using immunofluorescence assay. The result showed an enhancement in CD4 expression, the key factor that is involved in activation and production of antiviral substances. Selection of the specific mAb mentioned above, 3A9, that is specific for the CCR5 N-terminal

domain which has the most contact residues for HIV-1 gp120 that mediates fusion and entry was mainly appropriate. The result showed that mAb 3A9 does not seem to form interactions with the polar and charged CCR5 N-terminal domain binding site suggesting that the low frequency electrical stimulation induces conformation change in the CCR5 proteins. The pattern of the FG Nup153 is altered by the application of a low frequency electrical field causing irregular distributions which likely causes the collapse in the native Nup153.

The electrical stimulation approach of this work that predominantly by electrostatic interaction between the external electrical field and the electro active biological molecule therefore can affect the underlying mechanism of the interaction between the virus and the domain regions of the host cells by stopping this interaction for a sufficient period of time; the dynamic forces of a virological synapse (cell-to-cell interaction to allow cell-to-cell transmission) are possibly not adequate to maintain the attachment of the HIV-1 virus. Such stable interactions can only be provided by the immunological synapse (signaling proteins for cell activation). Thus the HIV-1 virus cannot conjugate with the target cells, so that the HIV-1 virus cannot mutate and develop resistance in the absence of the host cell proteins, thus disturbing its life cycle. This suggests that the mechanisms of the inactivation signal can induce virus death and disappearance, with no side effects. This action is impossible to achieve in the pharmacological approaches, due to the fact that the virus has a mechanism that utilizes a cellular protein and all the key factors that can control the host cell activity; thus it is impossible to treat with common antiviral therapy. Besides, the low frequency electrical stimulation can also enhance the cell functions without dielectric loss, and dielectric breakdown takes place. Thus it has no serious effects on the typical biological protein conformation and could prompt anti-HIV-1 treatment. The low frequency electrical stimulation can, therefore, enhance the cell functions and could promise anti-HIV-1 treatment without disturbing the typical biological protein conformation as well as blood cell activities and their function. Although serious investigations are required in order to fully use the application of low frequency electrical pulses in vivo in the real world, for treatment, the result is promising and provides the necessary motivation for the applications of low frequency electrical stimulation on human immune response, which might offer important antiviral therapy against the most devastating pathogen in human history.

## **Chapter 7**

### **Conclusion**

#### **7.1 Summary**

The electroactive features of the biological cells have inspired many electronic engineers around the world to investigate the electronic characteristics of biological materials and have become useful elements for developing smart biomedical integrated circuit solutions for electro-medical treatment devices that are implanted within the body and for non-invasive devices. These devices use the application of an electric field to stimulate reactions that restore normal cell functions and activate the biological cells to recover from a disorder or disease and to improve patients' lives. It has potential for treating a variety of chronic diseases that have significant social and economic effects. It could be particularly useful when therapeutic drugs become ineffective and cannot be replaced, as in untreatable HIV-1 disease that mutates and develops drug resistance. Basically, current advances on protein-protein interaction research, which are dominated by electrostatic interactions which are considered the main driving forces that have a key role in the development of the disease state in the body, encourage the development of a novel electro-medical treatment device, based on understanding of the mechanisms underlying disease processes. Specifically, the interaction between the HIV-1 and the host cell, which is predominantly protein charge-charge interaction, is an attractive target to investigate in this work using such an approach.

In this doctoral research, the initial focus of the research attempts, therefore, is to obtain a fundamental understanding of biomedical integrated circuit design and its interaction with the biological materials and how this could be utilized for novel electro-medical treatment devices and applications. Hence, the research project combines advances in new CMOS technology for integrated circuit design and understanding of the electrically conductive body medium, as well as disease states, to develop the concept and to design and fabricate a novel non-invasive biomedical device, capable of communicating with body tissue and cells for biomedical treatment benefits. An analogous aim is the characterization of the generated signal in-vitro to investigate the effect of low frequency periodical bio-phase square waveform and low voltage electrical pulse on human blood to stimulate potential reaction in its cellular activities,

to induce a short-term, or a long-term antiviral state to establish HIV-1 treatment in vivo. This chapter concludes the research outcomes of this research project.

The thesis introduces (chapter 1) the importance of the design of smart electro-medical treatment devices, both implanted and non-invasive, for treating disorder and disease, to overcome the deficiencies of several conventional medical treatments in order to restore health, and extend life. Since the design of a device for electro-medical treatment depends on the condition of the disorder or disease, the relevant disease and the demand for alternative treatment of disease such as HIV-1, with its enormous psychological burden and related healthcare-associated infections and costs, has been introduced. The interaction of the HIV-1 virus and the host cell that develops slowly in the human blood cells (lymphocytes) predominantly through protein charge – charge interaction, is introduced in this chapter. Since proteins are involved in cell communication which mediates different electrochemical signals conducting events from the extracellular to the intracellular, they are therefore, the key factor that continues rearranging and folding their structure into a variety of three dimensions in response to these electrochemical signals to control almost all cellular processes and perform various cell functions. Proteins that display a heterogeneous structure have various conductivities and permittivity (determining the interaction with the electrical field) and possess dielectric properties with a large conformation change, undergoing structural rearrangements in response to electrochemical signals. Applying an external electrical force with corresponding possible complex biological effects which change the charge distribution of the active predominant protein molecules, can also induce conformation change inhibiting the interaction of the HIV-1 virus and the host cell. Since the notable feature of this electrical stimulation is its cellular specificity, the device and the parameters of the generated electrical pulse are designed and selected to stimulate only the blood, leaving other tissues unaffected. This encourages the researcher to develop a concept to investigate the effect of an application of a periodical low frequency bipolar square waveform signal and low voltage electrical field on human blood in vitro, to induce enhancement and/or inhibition effect on protein dominant regions. These effects could induce an antiviral state for a period of time, but are not expected to seriously disturb the biological protein structure and its conformation state, with no evidence for any harmful effect on human blood; this is promising for the conception of HIV-1 treatment in vivo. Hence, an appropriate non-

invasive device is proposed and developed in this research project. Since blood cells are naturally electrically conductive, the development device is a WFG design to generate and deliver the required signal and communicate with human blood through the conductivity of the patient's skin cells, utilizing an active electrode. The proposed device can generate, control and deliver an appropriate low frequency and low voltage pulse via electrode applied to the relevant location through the low-resistance skin surface to a patient's blood, with no harm. Therefore, an overview of this project system model, design, theory and approaches (chapter 2) includes the WFG, an active electrode as well as biological theoretical analyses and bioelectrochemistry experimental design, performs and discussions on experimental results are presented (chapter 6).

After carefully investigating the WFG architectures and a detailed literature related to the research project to compare different topologies, analog WFG implementation utilizing an OTA is chosen, due to its high performance and flexibility (Chapter 2). The most interesting property in this type of circuit, is that the transconductance  $g_m$  of the CMOS OTA can be controlled by the biasing current, and hence, can be designed to achieve a wide tuneable range of frequencies, by varying bias current. To optimize the proposed WFG circuit performance, with low power signal processing systems, novel relaxation oscillators, comprising a hysteresis Schmitt Trigger with two relaxation timing networks, is presented. Based on the relaxation timing network, two WFG approaches have been developed and fabricated in this research project for comparison (Chapter 3 and Chapter 4, respectively). A new theoretical model and analysis is also developed to determine the key factors and the controllable variable parameters as well as component sizing for low power, low frequency and small chip area WFG circuit design, and to determine the trade-off between gain and frequency. Sufficient low frequency gain with desired low speed, is achieved by using a device with a long channel length  $L$ , resulting in larger output resistance and hence, large gain. The  $C_{gs} = (2/3)WLC_{ox}$  of the MOSFET devices is also increased considerably, enhancing the reduction of its intrinsic frequency. While using a small  $(V_{GS} - V_{THN})$ , and hence, small DC drain biasing current, this enhances the low frequency gain, reducing the intrinsic frequencies of the MOSFET devices, and thus significantly reducing power consumption. Since the overall gain of the multiple-stage operational amplifier is equal to the product of all the stages, cascaded gain topology, with adequate DC gain per stage, is used in the proposed Schmitt Trigger

circuits to increase the gain and the output swing requirement, without consuming extra overdrive, hence, reducing supply voltage. The circuit operation and the new mathematical derivations related to gain, frequency, duty cycle and the controllable variables of the two WFGs are described, as well as their amplitude and frequency control behaviour, and compared well with simulation and measurement results. Advanced physical design that defines the physical size and performance of the circuit is also introduced to optimize the layout of the designed IC circuits for chip fabrication. The layout of the proposed IC circuits of this research project has been implemented in 130-nm IBM CMOS process technology on Mentor Graphics Pyxis CAD programme.

The ELF WFG circuit (chapter 3) however, comprises a novel compact hysteresis Schmitt Trigger based on positive feedback and a relaxation timing network utilizing an RC circuit with its applications for a novel CMOS ultra-low-power, ELF WFG design. The ELF WFG has been designed and fabricated using 2.5-V devices available in 130-nm IBM CMOS technology with a  $\pm 1.2$  V voltage supply to generate a predictable bi-phase square/ exponential waveform signal. Using the same topology, two sets of device dimensions and circuit components are designed and fabricated for comparing relative performance, silicon area and power dissipation. The first ELF WFG design consumes  $691\mu\text{W}$ , while the second ELF WFG design consumes  $943\mu\text{W}$  using the same voltage supply. ELF oscillation is achieved for the two designs, being about 3.95 Hz and 3.90 Hz, respectively, with negligible waveform distortion. The two design circuits can also generate MLF, around 100Hz, with small-size on-chip designed capacitors of values 40pF and 2.3nF, respectively. The first ELF WFG design is found to provide overall optimal performance compared to the second ELF WFG design, at the expense of higher silicon area, using large value integrated resistor. A novel concept of employing a combination of the different types available of on-chip p+ polysilicon resistors in the 130-nm IBM CMOS process, is used to fully implement the large integrated resistors. This ELF oscillation, with low-power performance ELF WFG design, is a multipurpose waveform generator that can generate a square/exponential waveform enabling the circuit to be used in many micro-power biomedical applications.

The second WFG<sub>INT</sub> circuit (chapter 4) is a novel dual-band low-power mixed-signal IC design with wide-range low-frequency tuning-range, utilizing a hysteresis Schmitt Trigger with a gm-C integrator relaxation timing network along with a digital frequency-divider system. The three stage hysteresis Schmitt trigger is a device-size



modified version of the first ELF WFG circuit in chapter 3. The configuration of the WFG<sub>INT</sub> exhibits good linearity and relatively low temperature sensitivity, using only four stages, along with one small-size on-chip designed passive components of values 10 k $\Omega$  and 10pF. A novel hybrid frequency tuning technique, composed of two models, the **analog model** (electronically adjusting the bias current of integrator) and the **digital model** (frequency divider) are developed and implemented for a wide frequency tuning range. For an appropriate low frequency WFG<sub>INT</sub> design, and to reduce power consumption and optimize the silicon area, a novel mathematical model for component sizing of the proposed WFG<sub>INT</sub> design is derivative. Due to the low supply voltage in today's nano-metric CMOS technologies adopted in this work, combined with the wide tuning range, a small chip area and a low power consumption target, the integrator of this waveform generator is a simple first order gm-C integrator building block (STG4) which has been used to perform three tasks; **(1) the timing network, (2) for low frequency design, and (3) for the electronically tuneable WFG<sub>INT</sub> circuit (band I).** Although a first order gm-C integrator building block is proposed, the novelty of the gm-C integrator design, is that the design parameters of its  $gm$  are carefully chosen based on a new mathematical model developed to satisfy the low frequency requirements and to provide a wide frequency tuning range (band I). An active gm-C integrator is implemented in CMOS process technology to operate at very low frequencies, implying very low  $gm_{7,8}$  values, without the need for large capacitor values. The oscillation frequency of the core WFG<sub>INT</sub>, can be also varied linearly over a wide range through the choice of the size of the integrator input pair M7, and M8. The results indicate that a small DC bias current along with the small  $W_{7,8}/L_{7,8}$  device ratio of the integrator, can accommodate a wide linear frequency tuning range along with low power consumption. Since the integrator frequency characteristic is determined by the gm/C ratio, a wide tuning range can be achieved, and in addition, PVT dependencies can also be compensated by tuning the  $gm$  of the integrator. The oscillation frequency of the core WFG<sub>INT</sub> can, therefore, be linearly controlled by the bias current of the gm-C integrator through a smart and simple tuning gate-voltage ( $V_{tune}$ ) that is driven by a single NMOS current source, without requiring an extra complex and complicated circuit.

A digital FD model is also developed and implemented by cascading 16 stages of divide-by-2 FFs. Energy efficient TGs are used to realize TGMSDFF. Two 8-to-1

Multiplexers (MUX1 and MUX2), along with a PS, are also developed and implemented to select FD outputs for driving an electrode from 16 selectable channels (band II). Power consumption and die area are optimized by appropriate device sizing. The completed circuit is fabricated using Global Foundries (GF) 8RF-DM 130nm CMOS process, with a supply voltage of  $\pm 1V$  for the analog oscillator circuit and  $+1V$  for logic circuits. The WFG<sub>INT</sub> core generates square and triangular waveforms with a target frequency of around 17kHz and peak-to-peak output voltage of around 1.5V. The WFG<sub>INT</sub> core (band I) can be tuned in the range of 6.44kHz - 1003kHz through bias current adjustment of gm-C integrator, while a lower frequency (band II), in the range of 0.1 Hz to 502 kHz, can be provided digitally through a divide-by-2 stage. As a result, the WFG<sub>INT</sub> along with the FD circuit provides two bands with a wide range of frequencies which is extremely large. The total power consumption was only 2.557mW while occupying a total silicon-area of only 18426  $\mu\text{m}^2$ . The optimization flowchart of the designed CMOS dual-band WFG<sub>INT</sub> including circuit design process performance in this work is introduced at the end of chapter 4. The optimal design performances, transistor dimensions and passive component values for the proposed analog WFG<sub>INT</sub> and the digital FD circuit are then obtained, based on iterative simulation results. The required system specifications are the result of trade-offs made between performance, power, silicon area and cost. The complete designed WFG<sub>INT</sub> circuit is also a multipurpose waveform generator providing square and triangular waveforms along with their square waveform complementary signals, for low frequency and micro-power biomedical electrical stimulation applications. Subsequently, a low distortion sinusoidal wave shape can be generated by removing the higher harmonics through the low pass filtering of the triangular wave shape.

A comparison of the fabricated waveform generators WFG<sub>INT</sub> with WFG<sub>RC</sub> of this work and with some recently reported literature is provided in Table 4.4. The fabricated WFG<sub>INT</sub> design, which is implemented fully on chip, utilizes a small resistor and small capacitor values to generate a low frequency output signal of 17kHz with lower power consumption, compared well with the two CMOS ELF WFGs, while for the two CMOS ELF WFG, ELF of 3.9Hz is achieved, utilizing off-chip large capacitor values to limit the overall passive element area. In addition the fabricated WFG<sub>INT</sub> can provide a wide frequency range with good linearity, and the oscillator frequency of the WFG<sub>INT</sub> core can be controlled independently and modified electronically by adjusting

the bias current of the integrator building block. Comparing this with the two CMOS ELF WFG, wide frequency tuning is achieved only through the relaxation mechanism using R2, which is more suitable than using the bias current. However, the fabricated WFG<sub>INT</sub> and the two CMOS ELF WFG are capable of providing a low oscillator frequency which utilizes a lower active and passive components account, with lower power consumption, compared to the previously reported WFG architectures. They are simple and compact structures, considered as a power efficient and small chip area solution for a biomedical device application.

A novel CMOS active electrode-pair (chapter 5) for electro-bio-stimulation with high signal integrity is being proposed and developed in this research project. Since the aim of this work is to transfer electrical signal in a specifically controlled fashion through the electroactive biomolecule tissue, an active electrode is, therefore, designed and implemented to provide biphasic square waveform output signals to overcome the deficiencies of using a passive electrode. The active electrode employs a buffer circuit based on an adaptive voltage follower to increase the output current in an efficient way, while minimizing the overall power consumption. The active electrode-pair circuit was fabricated in a 130-nm CMOS process using a low supply-voltage of +1.2V, consuming only 100.8 $\mu$ W. It occupies a small chip-area of around 2936.23  $\mu\text{m}^2$  (2x1468.12  $\mu\text{m}^2$ ). It can deliver bi-phase square waveform signals from 16 selectable low-frequency channels. The individual active electrode can also be used to deliver mono-phase square waveform output signals.

However, the complete processed chip of the signal-processing circuitry, including the dual-band WFG<sub>INT</sub> with ultra-wide low-frequency tuning-range and the active electrode-pair circuit, with the required external components, are supposed to be gathered and mounted together, on a PCB, with two platinum-passive electrodes directly soldered on the top of the PCB, to build the complete encapsulated bio-medical device with electrode contacts. Mounting all IC signal sources and the active electrode on the electrodes (transducers) will minimize the signal path between the WFG, the two active electrodes, and the body, and reduce interference. For low cost and low power consumption, a free energy solar panel charged and regulated power-supply is also included for the rechargeable battery of the system. But this process requires wire bonding to mount the fabricated chip on a PCB; unfortunately, this process is not available at this time, so this process will be left to future work. Only the theoretical

model, with the schematic diagram of the complete circuits of the proposed biomedical device and the complete encapsulated bio-medical device with electrode contacts is provided in this research project (chapter 5).

After carefully studying the interaction of the HIV-1 virus and the host cell (chapter 6), theoretical analysis, experiment design and performance are carried out in in-vitro environments to examine the influences of low frequency and low voltage periodical bi-phase square waveform electrical pulses on human blood, utilizing the immunofluorescence microscopy technique. The results provide motivation for the applications of low frequency electrical stimulation on human immune response, thereby enhancing or inhibiting predominantly immune activity that can be used in vivo as an anti-HIV-1 viral treatment. Two main aspects could encourage the use of electro-medical treatment; **(1)** stimulating the natural healing, and **(2)** inducing biological effects in which change in the charge distribution of the biologically active molecules takes place: disturbing the virus-host cell interaction and hence, the virus life cycle, leading to inactivation signal-induced virus death and disappearance. As demonstrated in this work, the application of low frequency 5Hz and 10Hz with 1V applied voltage, however, has shown enhancement of the CD4 expression and increases the CD4 cell count, which is important for stimulating the human immune responses by secretion of different immune response elements to produce antiviral substances. This may be related to the fact that, when cell exposure to electrical force induces change in several cell parameters and affects the cell membrane potential, releasing calcium  $\text{Ca}^{++}$  from the intracellular pore stores, this recruits intracellular signalling mechanisms causing cell activation. Redistribution of the CCR5, in response to low frequency electrical stimulation, is due to the fact that a low frequency electrical field could induce polarization in its predominantly polar or/and charged amino acid, causing change in the charge distribution of the active protein molecules which could induce conformation change, as evidenced the inability of N-terminus-specific antibody 3A9 to bind to cell surface CCR5 N-terminal domain, after electrical stimulation, compared with unstimulated cells and with the reported mutated CCR5 N-terminal domain receptor in pharmacological approaches. The 3A9 mAb is chosen in this work to recognize epitopes in the residues and the mutate the CCR5 N-terminal domain as well as for drug-bound CCR5 as a co-receptor for entry which is critical for HIV-1 viral binding activity. The aim of this approach is to identify the alteration in the CCR5 N-terminal domain that is

involved in HIV-1 viral fusion and entry in response to a low frequency electrical field, and to compare this to the pharmacological approach. Similarly, electro-stimulation could induce alteration of the polar amino acid residues' glutamine (Q4) in the CCR5 N-terminals, which is considered the most critical factor in adaptation to low level CCR5, in some viral strains. The pharmacological approach using a protein engineering technique, makes a small mutation in a single amino acid within the assumed epitopes, to make additions or substitutions of a few charged amino acid residues at the termini of the charged CCR5N-terminal domains, to reduce the HIV-1 binding and entry. Thus the virus can mutate and develop resistance easily, and use alternative binding and entry mechanisms, while electro-stimulation could disturb the interaction between the HIV-1 and the host cells, hence the virus cannot mutate and develop resistance easily, and use alternative binding and entry mechanisms.

Considering the native electrostatic interactions as the driving force that are responsible for the reorganisation and assembly of the FGnup components of the NPC in specific patterns, to form the permeability barrier that is responsible for the selective translocation through the NPC, the electrostatic interactions due to the applied low frequency electrical field, therefore, could also provide a permeability barrier, prevents the import and export of large macromolecule HIV-1 particles through the NPC in the absence of nuclear import and export signals. This is by redistribution of the FGnup disorder sequence of the NPC and of the FGnup153, which is one of the NPC components that have an important role in nuclear import and export events of a large weight molecular HIV-1 PIC and the viral RNA, respectively. As demonstrated in this work, the electrical stimulation with low frequency pulse changes the pattern of FGnup153 by inducing redistribution of the FGnup153 disorder sequence, reorganising its pattern, forming irregular concentrations within the nuclear membrane similarly to the behaviour of native FGnup153 amino acid sequences. Thus the pattern and redistribution of the FGnup153 in response to a low frequency electrical field is therefore, considered to have no serious effect on its native sequences. However, the influence of a high frequency electrical field on the cell surface expression of CD4 or CCR5 and for binding activities of 3A9 mAb, as well as the distribution of FGnup 153, are dramatically different, as both cell surface and NPC component display no staining. It is well known that the application of a high frequency waveform has enough energy to break any cell's chemical bonds (ionization). The main challenge in this work,

however, was to determine the charge-charge interactions and binding region of the CCR5 and redistribution of the FGNup153 in a more specific way without the specialised equipment such as x-ray crystallography, which would be preferable, in order to investigate the three-dimensional structure of a complex arrangement. Thus the activities of the underlying mechanism are investigated utilizing immunofluorescence microscopy technique, and accurate results are obtained with relatively low cost. The results therefore, demonstrated that the applications of the low frequency electrical stimulation, have practical importance in cell functions which could promise short-term conformation change in the protein predominant regions, blocking the binding of HIV-1 gp120 protein to CCR5 and the binding of its effector factors to the FGNup153.

However, in response to the low frequency electrical force, given the heterogeneous structure of the proteins, the consequent frequency-dependent polarization involves the orientation and polarization of its randomly orientated polar molecule and the redistribution of the positively and negatively charged molecules within the protein, which makes them rotate, move, align and polarize. Interference polarization within proteins disturbs the interaction between both sides of the predominantly charged and/or polar host cell proteins, and of the HIV-1 infective particles; this can be a useful mechanism to interrupt the communication between HIV-1 virus and the host cell. This could induce an antiviral state for a period of time, due to the fact that the electrical signals will alter the net charge and induce conformation change that blocks the interaction between the virus and the biological cell system for a period of time. This prevents the virus from achieving sustained stable connection with biological cells. This disturbs the life cycle of the HIV-1 virus and hence, its replication, with no potential risks and harm to the host cells, compared to the common drugs.

However, the results suggest that inhibiting the interaction between the predominantly charged proteins of the host cell due to application of low frequency electrical square waveform pulse could also induce similar effects on the predominantly charged proteins of HIV-1 particles. In particular, the electrical stimulation approach of this research project, that uses square waveform with wide pulses, stop the interaction between the virus and the domain regions of the host cells for a sufficient period of time, so that the HIV-1 virus cannot mutate and develop resistance in the absence of the host cell as in traditional pharmaceutical approaches. Thus the HIV-1 virus cannot conjugate with the target cells, so that they are unable to reproduce out of the host. The



HIV-1 virus will then vanish. This action is impossible to achieve using the pharmacological approaches, which are used to lower the HIV-1 level, by temporarily blocking the replication of the HIV-1 virus, because the virus has a mechanism that utilizes a cellular protein, and all the key factors that can control the host cell activity. These allow the virus to detect the drug-bound conformation of the host cell protein domain regions and to use an alternative cellular protein for replication; this makes it impossible to treat with common approaches (section 6.2).

Using the application of periodical low frequency bipolar square waveform signal and low voltage electrical field can, therefore, induce an enhancement and/or inhibition effect, prompting an antiviral state for a period of time, but is not expected to seriously disturb the host cell protein structure and its conformation state. As previously mentioned in Chapter 1, since there is no rotation around the peptide bond, the back bone of the protein does not rotate freely and only the polar or charged site chains rotate. The parameters of the generated electrical pulse are designed and selected carefully to stimulate only the blood cells, leaving other tissues unaffected. Since disease can disrupt the biochemical systems in biological cells, this inhibits the normal protein synthesis in lymphocytes; however, applying certain stimulation frequencies can enhance the biochemical parameters of the blood and normalize protein synthesis in lymphocytes. The movement of the charged molecule and the free ions, in response to an applied external electrical field, can also be a useful mechanism to induce an action comparable to the normal cell endogenous electrical field which is important in biological processes, such as wound healing and tissue regeneration. Besides, waveforms with certain stimulation frequencies can interact with the periodical intrinsic oscillators of the biological cell networks, which enhances their intrinsic oscillatory activity, an essential process in the living organism that enhances cell communication. The low frequency condition electrical stimulation (5Hz and 10Hz with applied voltage of 1V) can enhance the cell functions without dielectric loss and dielectric breakdown takes place. At very low frequencies, however, proteins possess a large low frequency permittivity, because the dipole presence in proteins has enough time to align and polarize in response to the applied electrical field, before its change in direction. At very high frequencies, the dipoles do not have enough time to align, are totally unable to respond to the applied electrical field, and polarize, causing dielectric heating, and hence, dielectric loss takes place. The low frequency electrical stimulation can



therefore, enhances the cell functions and could prompting anti-HIV-1 treatment with no seriously disturb the typical biological proteins conformation as well as blood cells activities and its function. Moreover, the low cost is due to the use of a low power non-invasive electronic device including a WFG with active electrode-pair in this research project.

The development device in this research project is expected to allow HIV-1 patients to receive regular treatment at any time until HIV-1 viruses are removed from their bodies, with no harm and maintaining the lower treatment cost compared with that of the conventional therapy. The electro-medical therapy might help the wider population of HIV-1 patients, particularly patients with low income, to have effective treatment and live longer, as well as to reduce the psychological burden and related healthcare-associated infections and costs. Although further investigations are required in order to fully use the application of low frequency electrical stimulation in vivo for treatment, the result is promising and provides the foundation for the application of low frequency electrical stimulation on human immune response, which might offer important antiviral therapy against the most devastating pathogen in human history.

Energy-efficient CMOS technology that has scaled-down device dimensions therefore, can be utilized for the design of precision biomedical integrated-circuit solution for battery-operated biomedical devices for treating a variety of chronic conditions. It can establish the requirements for bioelectronics devices to function compatibly with the biological cell. The structure of the devices and the design are required to be simple, and in biomedical cases, the cost of devices can be reduced by the imposed simplification; the smaller the structure, the smaller the energy source. The proposed WFGs with the active electrode-pair building block on chip circuit solutions, using new 130-nm CMOS technology, has enhanced the development of the novel biomedical integrated-circuit solution for a low power battery-operated system that is portable, light-weight, and miniaturized, which can be used for non-invasive and for implanted electro-medical treatment devices.

## 7.2 Contributions of This Doctoral Research

This project has two phases: 1. develop a biological concept with a biomedical integrated circuit design solution, for a non-invasive biomedical electro treatment device, 2. Theoretical analysis and design of a bioelectrochemistry experiment to investigate the effect of the designed electrical signal on the underlying mechanism of HIV1-and host cell interaction domain regions. The contributions of this doctoral research can be summarized into the following categories:

1. **Development of two novel WFGs in the new 130-nm CMOS** technology utilizing a novel relaxation oscillator with two relaxation timing networks. Based on this, a new hysteresis Schmitt Trigger with applications for a novel CMOS ultra-low-power and for ELF WFGs, along with an RC relaxation timing and gm-C integrator network circuit, for multipurpose signal source WFGs with controllable amplitude and frequency, are presented. These are capable of providing continuous dynamic power to meet the demand for light-weight, low cost and energy-efficient circuit solutions for battery-operated biomedical devices. The present movement in the new topology for the proposed circuits design is to: (1) provide a solution for the problem of long-term power consumption in biomedical devices, (2) decrease the number of MOSFET active devices to reduce the supply voltage, chip area and cost, (3) reduce the passive element to eliminate the temperature sensitivity issues without limiting the performance of the circuit, and (4) one of the important characteristics of the design is using cascaded topology to achieve high gain and maximum output swing, with a reduced series arrangement of transistors, to reduce loss in overdrive voltage.
2. **Development of a new theoretical model** and derivative of a novel mathematical model to determine the controllable variable parameters as well as component sizing for high gain, low frequency, low power, and small chip area WFG circuit design and also to study the trade-off between these important parameters.
3. **Development of a novel concept employing** a combination of the different types available of on-chip p+ polysilicon resistors in the 130-nm IBM CMOS process, in order to fully implement the large integrated resistors. Combining such resistances helps to improve the accuracy of the integrated precision resistors, by achieving a

lower process-dependent variation in the resistance value along with optimized area, rather than using a single homogeneous resistor of the same value and area.

4. **Development of a novel hybrid frequency tuning technique** composed of two models implemented for a wide frequency tuning range:
  - a) **Analog model**, comprising a first order electronically adjustable gm-C integrator using a mathematical model to design its  $gm$  parameters to perform three tasks; (1) the timing network, (2) for low frequency design, and (3) for the electronically tuneable WFG<sub>INT</sub> circuit (band I), linearly controlled by the bias current of the gm-C integrator through a smart and simple tuning gate-voltage ( $V_{tune}$ ) that is driven by a single NMOS current source, without requiring an extra complex and complicated circuit.
  - b) **Digital model**, comprising a frequency divider which provides square waveform signals with its complementary signal, from 16 selectable low-frequency channels. Based on this a novel low power miniaturized dual-band WFG with ultra-wide low-frequency tuning range is developed for biomedical electrical stimulation therapy.
5. **Development of small-size on-chip capacitors** with low capacitance. The single MIM capacitor (MIMCAP) is designed by adding a thin layer of the different types of metal available in the CMOS8RF Design Manual.
6. **Development and optimizing of a novel buffer circuit** based on an adaptive voltage follower for a novel low power active electrode-pair integrated circuit design in order to provide bi-phasic low frequencies simultaneous multichannel signals for biomedical applications. The individual active electrode can also be used to deliver mono-phase square/triangular waveform output signals.
7. **Development of the theoretical model** of the complete signal-processing circuitry, by mounting all IC signal source and the active electrode on the electrodes (transducers). This involves the schematic diagram of the proposed prototype electro-bio-stimulation system, including the fabricated mixed signal CMOS WFG<sub>INT</sub> with the active electrode-pair and a free energy solar-panel-charged regulated power-supply on the PCB, with the complete encapsulated bio-medical device with electrode contacts. This is to reduce the circuit complexity by eliminating the number of wires used for practical daily use. The novelty of the development biomedical device of this research project is that it is a free energy novel mixed-signal dual-band

square/triangular chip, state-of-the-art in terms of the low frequency design, a wide frequency tuning range, miniaturization, and multipurpose signal source WFG, which can be used as the basis of inexpensive function generators that provide square, triangle, and sine wave outputs for bioelectronics systems with micro-power consumption and hence, low cost, for the long life battery-operated biomedical device. The proposed electro-medical device is capable of providing continuous dynamic power with good performance that can be suitable for use with implantable and non-invasive biomedical systems applications. It is also designed to provide non-ionizing effect electrical energy to the body.

**Development of applications.** Applications of the generated periodical low frequency bi-phase square waveform signal on human blood have been demonstrated in this work. This can be a useful mechanism that interrupts the infectious association (communication) between the HIV-1 virus and the host cell. These electrically induced protein transformations can be used as blood-cell treatment and as anti-HIV-1 electro-therapy. Thus, the biological project concept with the theoretical analysis and the design of the bio-electrochemistry experiment to examine the concept of this research project in-vitro environments as well as the biological experiment results provide important data about the underlying mechanism of HIV1-and host cell interaction. In particular, the protein charge-charge interaction between HIV-1 and the host cell predominant regions provides important documented facts that could lead to the use of electrical stimulation in vivo to establish possible ant-HIV-1 therapy targets against the most devastating pathogen in human history.

Overall, the development of knowledge about the electrical properties of the biological system and disease state and the concept of this project that can be used effectively and safely for the treatment of untreatable disease. The advances in bioelectronics technology, as in new CMOS technology, provide practical solutions for advanced technological electro-medical treatment devices. This project also demonstrates how to design a device to be used effectively for electro medical treatment to overcome the difficulties of pharmaceutical therapeutic approaches which cannot produce drugs to fight against the viral cycle, without harming the human hosts. Based on the above approach, the study of the biological system and the underlying mechanism of the disease, from an engineering point of view, is considered a novel contribution that can be used to develop an alternative medical treatment for such

untreatable diseases. This opens a new way to meet the demand for treating a variety of diseases and disorders. This doctoral research is not only of academic interest but also of high relevance for medical applications. This research project therefore, is considered highly beneficial in the development of knowledge in advanced technology for electro-medical treatment devices, their design, structure and applications in the medical treatment to restore health, and extend life, and for future growth in the biotechnology industry, therefore beneficial for the patients, physicians and for humanity.

### **7.3 Recommendations for Future Research**

The work presented in this research project is focused on the development of a non-invasive biomedical device. Advances in bioelectronics technology, involving the new technology of integrated circuit design and bio-electrochemistry science, have contributed to this research project which describes how these can be utilised for biomedical treatment benefits. Further work is required for the use of such electro-medical treatment technology in the real world, in vivo, including the following:

1. The two CMOS ELF WFG that are developed in chapter 3 can be fully integrated on chip to generate MLF around 100Hz using the small development capacitor values of 40pF and 2.3nF for the first and the second design, respectively, while R2 is fixed. The WFG<sub>RC</sub> could be used as multipurpose signal source WFG, with applications of implantable and non-invasive biomedical systems applications. The design therefore, needs further refinement and testing with the proposed FD system and active electrode-pair circuits.
2. The complete processed chip of the signal-processing circuitry includes the proposed mixed-signal WFG<sub>INT</sub> with dual-band wide-range frequency oscillations and the FD system, the active electrode-pair circuit with the required external components and solar panel charged regulated power-supply which need to be mounted together, on a PCB with two platinum-passive electrodes directly soldered on the top of the active electrode PCB. The completed free energy bio-medical device system of this work can be, therefore, encapsulated with electrode contacts. This will minimize the signal path between the WFG<sub>INT</sub>, the two active electrodes, and the body, and hence, reduce interference. It can also be utilized in vivo for electro medical treatment test

and use. The goal of this device design is to lay the complete electronics system as closely as possible to the body to overcome the connectivity problem, and to improve the purity of signal transmission by reducing problems related to transmission of signals through wire (and its movement) including power line interference.

3. Although, the designed active electrode-pair is integrated individually on a different die for the purpose of using them with the development mixed-signal WFG<sub>INT</sub> and with any electro stimulation biomedical devices. The proposed mixed-signal WFG<sub>INT</sub> combines the dual-band wide-range frequency oscillations WFG<sub>INT</sub> and the active electrode-pair circuit which can be explored further by integrating them on the same die, in one complex IC chip, with readout circuitry to display information. As the design complexity and the required output signal precision for specific tasks increases, the device size, power consumption and hence, the cost of the biomedical device increases, which creates a design challenge. However, a smart architecture requires a state-of-the-art design, in terms of low power and miniaturization, involving a topological circuit design to implement multiple functions in the system, and to advance energy-efficient new technological devices for fabricating such complex systems. The completed proposed biomedical integrated circuits design could be, therefore, implemented utilizing the latest nano-meter CMOS technology to further minimize the system size and to reduce power consumption without compromising performance. Low frequency WFGs utilizing relaxation oscillators have distinctive design challenges when using short channel CMOS technology, while having many interesting applications in biomedical applications. In addition, the applications of the development of low power multipurpose signal source WFG with controllable amplitude and frequency, as in this work, can be extended for use with a wide range of applications, as in analog signal generation, signal processing, and communication. They can be used either as stand-alone signal sources or as a part of system.
4. The bio-electrochemistry applications of the low frequency electrical force can be expanded to examine the concept of this research project involving the underlying molecular mechanism of HIV-1 and host-cell interactions domains with many different frequency signal ranges in an in vitro environment and then in vivo, in the real world; these experiments could include: (1) CD4, CCR5 expression, CD4–CCR5 interaction, CCR5 N-terminals domain including the polar amino acid residues

glutamine (Q4) that is considered the most critical factor in adaptation to low level CCR5 in some viral strains, as well as in ECL1 and ECL2 domain regions, (2) NPC and its FGNup153 domain component. The actual performance of the FGNup153 can be realized by translocating objects which require a complex set of experiments with specific antibodies, and (3) Human cells transfected with HIV-1 can also be studied with application of low frequency electrical stimulation.

5. The charge-charge interactions in response to low frequency electrical force can be investigated using another specific technique for comparison, such as using x-ray crystallography, the technique that is normally used to determine protein structures and to investigate the three-dimensional structure of molecules, including proteins, at atomic resolution level; Nuclear magnetic resonance (NMR) spectroscopy to examine the structure of small molecules, and of small proteins or protein domains and dynamical information can be extracted to determine protein structures [335]; mass spectrometry to study interacting proteins; Surface plasmon resonance (SPR) technique to investigate protein-protein dynamic interactions, how slowly or rapidly molecular complexes assemble and break down over time, and how low frequency electrical force can affect these interactions [336]; Time domain dielectric spectrometer (TDDS) to study the dynamic dielectric properties of blood cells transfected with HIV-1 virus and for normal cells in response to a low frequency electrical force [36]. Raman spectroscopy for sample testing and analyses [337].
6. The non-invasive device developed in this work needs to be tested on human volunteers who carry the HIV-1 virus. This requires ethical approval, and a laboratory with specialised techniques to study the effects of low-frequency electrical pulse on the interaction of the virus with the host cell and on its lifecycle, as well as the immune response. This work could extend to examine the viability and long-term effects of the device.
7. Furthermore, the applications profile of the developed electro-medical-treatment device technology can be expanded. Prospective applications might include influenza virus, since if new epidemics break out, they could kill millions of people. Besides, the proposed device can be explored and characterized further to induce electroporation effect for cancer treatment. The concept and the techniques therefore, need to be characterized to establish the requirements for electronics devices to function compatibly with the biological cell to suit such application.



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**Appendix A.**  
**Supplementary Documents**



Date: 13 April 2016

Dear Ibtisam Abbas

**Re: Ethics Notification - SOA 16/12 - New Application  
Biomedical Integrated Circuit Design for Electrotherapy Device**

Thank you for the above application that was considered by the Massey University Human Ethics Committee: **Human Ethics Southern A Committee** at their meeting held on **Tuesday, 12 April, 2016**. On behalf of the Committee I am pleased to advise you that the ethics of your application are approved.

Approval is for three years. If this project has not been completed within three years from the date of this letter, reapproval must be requested.

If the nature, content, location, procedures or personnel of your approved application change, please advise the Secretary of the Committee.

Yours sincerely

Dr Brian Finch  
Chair, Human Ethics Chairs' Committee and Director (Research Ethics)

**Research Ethics Office, Research and Enterprise**

Massey University, Private Bag 11 222, Palmerston North, 4442, New Zealand T 06 951 6841; 06 95106840  
E [humanethics@massey.ac.nz](mailto:humanethics@massey.ac.nz); [animaethics@massey.ac.nz](mailto:animaethics@massey.ac.nz); [gtc@massey.ac.nz](mailto:gtc@massey.ac.nz)



## List of Publications

### 1. Journal Publications

- 1.1 I. A. Abbas Al-Darkazly and S. M. R. Hasan, "A Waveform Generator Circuit For Extra Low-Frequency CMOS Micro-Power Applications," *Int. J. Circ. Theo. Appl.*, vol.44, no.2, pp.266-279, Feb. 2016.
- 1.2 I. A. Abbas Al-Darkazly and S. M. R. Hasan, "Dual-Band Waveform Generator With Ultra-Wide Low-Frequency Tuning- Range," *IEEE Access J.*, vol.4, pp.3169-318, July 2016.
- 1.3 I. A. Abbas Al-Darkazly and S. M. R. Hasan, "Optimized Low-Power CMOS Active-Electrode-Pair for Low-Frequency Multi-channel Biomedical Stimulation" *In Elsevier, Microelectronics J.*, vol.66, pp.18-24 May 2017.

### 2. Manuscript Under Preparation

- 2.1 I. A. Abbas Al-Darkazly and S. M. R. Hasan, "On Conformational Change in Homo-sapien Blood-cells Proteins Through LF Pulse Stimulation to Transform Immune Activity."

### 3. Conference Publications

- 3.1 I. A. Abbas Al-Darkazly and S. M. Rezaul Hasan, "A Power Efficient CMOS Cascode Current Mirror To Supply Independent Biasing For Low Voltage Applications," In Int. Conf. 20th Electronics New Zealand (ENZCON), Auckland 2013.



**MASSEY UNIVERSITY**  
GRADUATE RESEARCH SCHOOL

**STATEMENT OF CONTRIBUTION  
TO DOCTORAL THESIS CONTAINING PUBLICATIONS**

(To appear at the end of each thesis chapter/section/appendix submitted as an article/paper or collected as an appendix at the end of the thesis)

We, the candidate and the candidate's Principal Supervisor, certify that all co-authors have consented to their work being included in the thesis and they have accepted the candidate's contribution as indicated below in the *Statement of Originality*.

**Name of Candidate:** Ibtisam Abbas

**Name/Title of Principal Supervisor:** Dr. S. M. R. Rezaul Hasan

**Name of Published Research Output and full reference:**

I. A. Abbas Al-Darkazly and S. M. R. Hasan, "A Waveform Generator Circuit For Extra Low-Frequency CMOS Micro-Power Applications," Int. J. Circ. Theo. Appl., vol.44, no.2, pp.266-279, Feb. 2016.

**In which Chapter is the Published Work:** Chapter 3

Please indicate either:

- The percentage of the Published Work that was contributed by the candidate:  
and / or
- Describe the contribution that the candidate has made to the Published Work:

The research work was carried out by Ibtisam Abbas under the supervision of the principal supervisor Dr. S. M. R. Rezaul Hasan

  
 \_\_\_\_\_  
 Candidate's Signature

25/05/2017

Date

  
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 Principal Supervisor's signature

25/05/2017

Date



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**Name of Published Research Output and full reference:**

1.3 I. A. Abbas Al-Darkazly and S. M. R. Hasan, "Optimized Low-Power CMOS Active-Electrode-Pair for Low-Frequency Multi-channel Biomedical Stimulation," In Elsevier, Microelectronics J. vol. 66, pp. 18-24, May 2017.

**In which Chapter is the Published Work:** Chapter 5

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25/05/2017

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**Name of Published Research Output and full reference:**

I. A. Abbas Al-Darkazly and S. M. R. Hasan, "On Conformational Change in Homo-sapien Blood-cells Proteins Through LF Pulse Stimulation to Transform Immune Activity." [Paper under review]

**In which Chapter is the Published Work:** Chapter 6 [Manuscript under preparation]

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**STATEMENT OF CONTRIBUTION  
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We, the candidate and the candidate's Principal Supervisor, certify that all co-authors have consented to their work being included in the thesis and they have accepted the candidate's contribution as indicated below in the *Statement of Originality*.

**Name of Candidate:** Ibtisam Abbas

**Name/Title of Principal Supervisor:** Dr. S. M. R. Rezaul Hasan

**Name of Published Research Output and full reference:**

I. A. Abbas Al-Darkazly and S. M. Rezaul Hasan, "A Power Efficient CMOS Cascode Current Mirror To Supply Independent Biasing For Low Voltage Applications," In Int. Conf. 20th Electronics New Zealand (ENZCON), Auckland 2013.

**In which Chapter is the Published Work:** Conference Publications

Please indicate either:

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Date

  
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 Principal Supervisor's signature

25/05/2017

Date

# *A Power Efficient CMOS Cascode Current Mirror to supply independent biasing for Low Voltage Applications*

Ibtisam A. Abbas Al-Darkazly<sup>1</sup> and S.M.Rezaul Hasan<sup>2</sup>

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**Abstract**—In this paper, a power efficient CMOS cascode current mirror configuration with minimum headroom to supply independent biasing is presented. A simple scheme is used to reduce supply voltage, power and the chip area. The cascode current mirror circuit has been implemented in 0.13 $\mu$ m CMOS technology using Mentor Graphics Pyxis. It can provide a multiple bias current to many segments of a more complex circuit. The circuit was stimulated and tested with various supply voltages of  $\pm 1V$ ,  $\pm 900mV$  and  $\pm 850mV$  for comparison. The  $\pm 850mV$  approach consumed 2.435mW compared to the  $\pm 900mV$  and  $\pm 1V$  approaches which consumed 4.176mW and 16.526mW respectively. As a result high current mirror accuracy is realized. This low voltage topology enables the circuits to be used in many low voltage and low power CMOS applications.

**Keywords**—Cascode Current Mirror; Independent biasing; Multiple Bias Current; Headroom Voltage.

## I. INTRODUCTION

A Power efficient current mirror with independent biasing and high accuracy is an extremely important technique in analog circuit design. It is useful in all kinds of systems; sensing, communicating, controlling, and wireless biomedical systems particularly, in systems that need to be portable and which operate with a long life time battery, and their overall cost is a strong function of the size of the system and the cost of the battery [1]. Therefore, reducing power consumption has a practical importance in the design and development of low cost, small size, light-weight and energy-efficient CMOS circuit solutions for such systems. Since a fundamental circuit of any CMOS device is a biasing current, and typical applications require multiple current sources to deliver bias current to more complex circuit, thus utilizing bias current topology with independent supply voltage in such applications can significantly reduce power consumption. Bias circuit requires a suitable scheme for a highly linear device.

This paper presents a new and simple topology in the design of CMOS biasing circuits based on low voltage cascode current mirror with independent supply voltage. Since this type requires external biasing, a copy of the reference current is converted to voltage and used to bias the proposed circuit. The outline of this paper is as follows. In section II, a brief

background is given. In section III, circuit design and implementation are discussed. Simulation results and layout are given in section IV and V, whereas conclusion drawn in section VI.

## II. BACKGROUND

A conventional bias circuit for MOSFET uses a simple resistive divider to establish a gate source bias [2]. In practice, this topology is not accurate, especially if the device is biased with low overdrive voltage, because the overdrive voltage is a function of VDD and the output current depends on process and temperature. MOSFET operating in saturation mode acts as a current source used in combination with current mirrors as an alternative solution for a biasing circuit. It is based on copying current to one or several current sources from one stable reference current. Current mirror configuration in Fig.1 that provides accurate current copying is controlled by the device ratios (W/L) only and is independent of process and temperature, where W and L are the width and length of the MOSFET. It requires minimum headroom and consumes low power [3]. But the actual output current is slightly mismatched because of channel length modulation ( $\lambda \neq 0$ ), particularly for minimum length transistors that utilize minimum width. To improve the match between the two currents, a simple cascode current mirror in Fig.2 is used to eliminate the effect of channel length modulation. This technique will force the drain to source voltage VDS2 to be equal to VDS1 (and equal to the gate source voltage VGS1), increasing the output resistance of the cascode current mirror which provides identical copying current. The main drawback of the simple cascode topologies is the increase in the minimum required voltage in order for all MOSFETs to remain in the saturation region, which reduces the output voltage swing [4].

Low voltage cascode current mirror architecture can be used, but requires a slightly higher supply voltage than the simple cascode current mirror. Also reference current (IRef) is required with additional circuitry such as self-biased beta-multiplier current reference. One of the drawbacks of such reference circuit is that undesirable operating point occurs when zero current flow in the circuit. A start-up circuit should always be used when using the beta multiplier, which requires



The diagram shows a current mirror circuit. A reference current  $I_{Ref}$  flows from a  $VDD$  supply through a resistor and a PMOS transistor  $M1$  to ground. The gate of  $M1$  is connected to its drain. This gate is also connected to the gate of a second PMOS transistor  $M2$ . The source of  $M2$  is connected to a load resistor and a current source  $I_{out}$  flowing downwards. The drain of  $M2$  is connected to ground. The width-to-length ratios are labeled as  $(W/L)_1$  for  $M1$  and  $(W/L)_2$  for  $M2$ .

The diagram shows a differential pair circuit with four NMOS transistors: M1, M2, M3, and M4. The gates of M1 and M2 are connected to a common bias voltage. The gates of M3 and M4 are connected to a common bias voltage. The sources of M1 and M2 are connected to a common tail node, which is connected to ground through a tail current source. The sources of M3 and M4 are connected to a common tail node, which is connected to ground through a tail current source. The drains of M1 and M2 are connected to a common output node, which is connected to ground through a load resistor. The drains of M3 and M4 are connected to a common output node, which is connected to ground through a load resistor. The circuit is labeled with  $V_{DD}$ ,  $I_{Ref}$ ,  $I_{out}$ , and  $(W/L)$  ratios for each transistor.

The schematic diagram of the proposed low voltage CMOS cascode current mirror with independent supply voltage is shown in Fig.3. The circuit employs an N-MOS cascode current mirror with minimum headroom voltage topology along with a P-MOS active current mirror to provide independent supply voltage. In this particular case, multiple currents are generated from one reference current, and the current mirrors operate from the same reference current. The circuit uses a small resistor with diode connected MOSFET to generate a reference current ( $I_{Ref}$ ). By mirroring the  $I_{Ref}$  current in M6 through M7 and in M5 through M3 can provide the operating bias for M1, M2 and M3, M4 respectively. The design employs the same length ( $L$ ) for all of the transistors, by simply sizing the width ( $W$ ) of the MOSFET transistors, can adjust the output current. The circuit topology gives the designer an additional degree of freedom in adjusting the output current mirror by aspect ratio ( $W/L$ ).

$$r_{out} = g_{m2} r_{o2} r_{o4} \quad (1)$$

where  $g_{m2}$  and  $r_o$  are the transconductance and small-signal output impedance of transistors, which is higher than in the simple current mirror. To understand the operation of the N-MOS cascode current mirror, normally, the drain of M1 and M2 are held at the same potential, which is  $V_{GS}$  or  $\sqrt{2I_{REF}/\beta} + V_{THN}$ , where  $\beta = \mu_n \text{ Cox } W/L$ , and  $V_{THN}$  is the N-MOS threshold voltage. And the voltage on the M2 before it starts to

enter the triode region can be as low as  $\sqrt{(2I_{Ref}/\beta)}$ . Realizing this, consider the wide-swing N-MOS cascode current mirror in Fig. 3, which means the minimum voltage across the current mirror is  $2\sqrt{(2I_{Ref}/\beta)}$ , the sum of the excess gate voltage of M2 and M4. Since M1, M2, M3, M4 have the same W/L ratio ( $\beta_1 = \beta_2$ ). Understanding that the gate source voltage ( $V_{GS}$ ) of M1 and M2 is  $\sqrt{(2I_{Ref}/\beta)} + V_{THN}$ . It is beneficial to keep M2's drain at  $\sqrt{(2I_{Ref}/\beta)}$  for wide-swing operation [8]. Therefore, the gate voltage of M3, M4 must be  $2\sqrt{(2I_{Ref}/\beta)} + V_{THN}$ , to generate this voltage by carefully scaling the width of M5 which is 1/2 of the size of N-MOS cascode current mirror widths and forcing  $I_{Ref}$  via the diode connected M5. In order to keep M1, M2 from entering the triode region and the output resistance from decreasing, the size of M5 can be further decreased. The cost is an increase in the minimum allowable voltage ( $V_{out}$ ) across M2, M4 [3].

The N-MOS cascode current mirror operates as a current source with high output impedance and accurate value that can be used for high accuracy applications. The P-MOS current mirror provides multiple biasing circuits and also can be used as a current source.

#### IV. SIMULATION RESULTS AND DISCUSSION

The simulations results were run for 0.13 $\mu$ m CMOS process technology and were obtained using Mentor Graphics Pyxis CAD [10]. The circuits generate and provide multiple output current with a low supply voltage. The design values for the active and passive element of the circuit were chosen depending on the specific operation and power consumption constraints. A total of 10 transistors were implemented for the low voltage cascode current mirrors and biasing current mirrors. The transistor dimensions are shown in Table I. A resistor of sufficiently small value of 7k $\Omega$  was chosen to set the reference current which can easily be realized in integrated circuit form. The circuit was simulated and tested with various supply voltages of  $\pm 1V$ ,  $\pm 900mV$ ,  $\pm 850mV$ , and  $\pm 800mV$  for comparison, thereby allowing the precise supply voltage approach with low power consumption to be used. The study and analysis of the characteristics of the designed circuit it also enabled. Fig. 4, 5, 6 and 7 show the simulated transient response of the reference current ( $I_{Ref}$ ), output current ( $I_{out2}$ ), of the N-MOS cascode current mirror, the output current of the P-MOS current mirrors ( $I_{out1}$ ,  $I_{out3}$ ,  $I_{out4}$ ) and the output voltage ( $V_{out}$ ) for different values of the supply voltage. In each approach the circuit functions correctly with a high accuracy. The circuit parameters were developed for the design and simulated for comparison is summarized in Table II. The  $\pm 850mV$  approach consumed 2.435mW compared with the  $\pm 900mV$  and  $\pm 1V$  approaches which consumed 4.176mW, and 16.526mW respectively. Note that an interesting simulation to run at this point is to confirm that the design still function correctly with small supply voltage down to  $\pm 800mV$  and consumed only 1.823mW. In practice the  $\pm 800mV$  current mirror approach is unattractive for low current applications, because its output has some distortion. Then this current mirror approach will not be used. The desired  $I_{Ref}$ ,  $I_{out1}$ ,  $I_{out2}$ ,  $I_{out3}$ ,  $I_{out4}$  for the low power current mirror approaches  $\pm 850mV$  are about 107 $\mu A$ , 213 $\mu A$ , 185 $\mu A$ , 612 $\mu A$  and 921 $\mu A$ . And the output voltage ( $V_{out2}$ ) is about 801.89 mV for the N-

MOS cascode current mirror and 850mV for the rest. Generally, In each case, the result of the circuit performance was significant comparable to the replica scheme in some of the reported reference [5][7][8].

#### V. LAYOUT

Fig. 8 shows the layout of the proposed circuit which is designed using 130nm IBM CMOS technology. The design occupies a small microchip area of only 316.274  $\mu m^2$ . On-chip resistor OP P+ Polysilicon resistor (opppres) was used for implementing fully integrated resistor. The layout circuit will be tested after fabricate the chip.

TABLE I. TRANSISTOR DIMENSIONS OF THE PROPOSED CIRCUIT

Transistor	(W / L) $\mu m / \mu m$
M1=M2 = M3 = M4	5 / 0.13
M5	2.5 / 0.13
M6	4 / 0.13
M7	5 / 0.13
M8	7 / 0.13
M9	20 / 0.13
M10	30 / 0.13

TABLE II. SIMULATION RESULT VALUES FOR VARIOUS SUPPLY VOLTAGES OF THE PROPOSED CIRCUIT

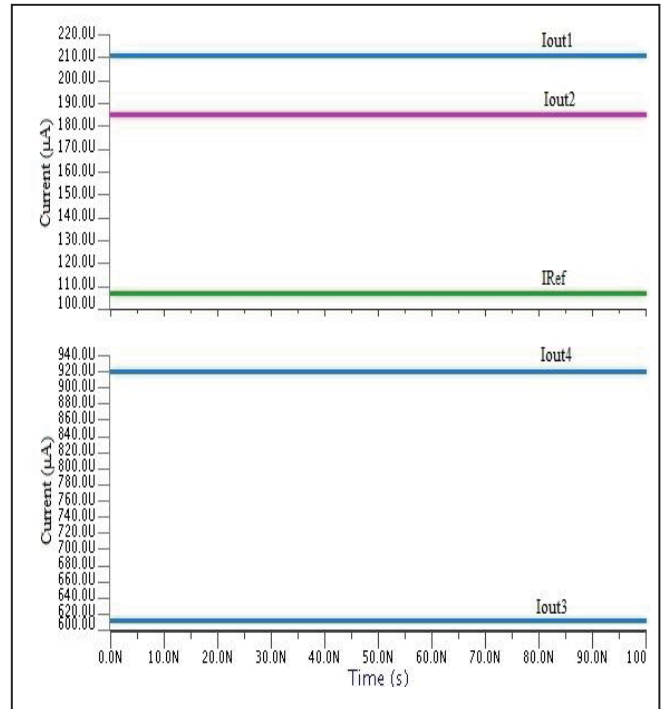
Parameter	Values			
Supply Voltage (VDD)	$\pm 1V$	$\pm 900mV$	$\pm 850 mV$	$\pm 800mV$
Reference Current ( $I_{Ref}$ )	134 $\mu A$	117 $\mu A$	107 $\mu A$	97 $\mu A$
Output Current ( $I_{out1}$ )	272 $\mu A$	233 $\mu A$	213 $\mu A$	187 $\mu A$
Output Current ( $I_{out2}$ )	238 $\mu A$	205 $\mu A$	185 $\mu A$	163 $\mu A$
Output Current ( $I_{out3}$ )	0.78mA	670 $\mu A$	612 $\mu A$	545 $\mu A$
Output Current ( $I_{out4}$ )	1.18mA	1.02 mA	921 $\mu A$	821 $\mu A$
Output Voltage ( $V_{out1}$ )	1V	900 mV	850 mV	799.99mV
Output Voltage ( $V_{out2}$ )	818.56mV	811.6mV	801.89mV	782mV
Output Voltage ( $V_{out3}$ )	1V	900mV	850mV	799.99mV
Output Voltage ( $V_{out4}$ )	1V	900mV	850mV	799.99mV
Power Consumption	16.526 mW	4.176 mW	2.435 mW	1.823 mW

## VI. CONCLUSION

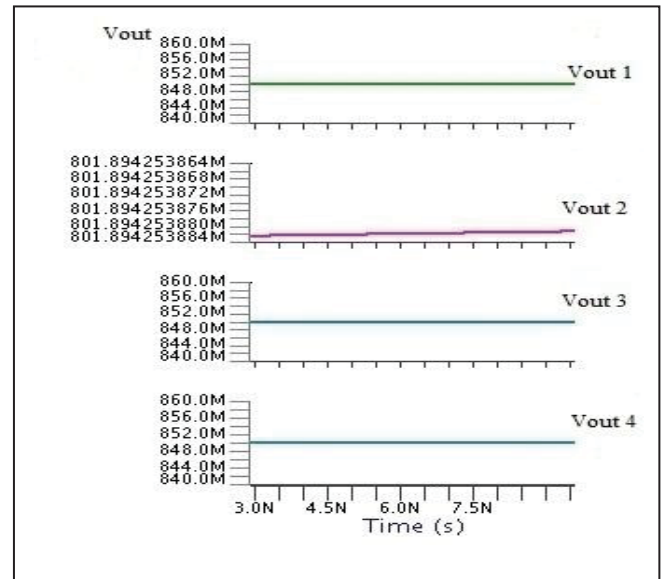
The design of low power and a wide output swing based on cascode current mirror have been presented. A new approach was developed in this work. The circuit employs N-MOS cascode current mirror with a P-MOS active current mirror topology to generate independent biasing and to provide multiple output current with a low supply voltage. The circuit was stimulated and tested with various supply voltages for comparison. The  $\pm 850\text{mV}$  approach consumed power of  $2.435\text{mW}$  compared to other approaches. However, the proposed low voltage current mirrors would be appropriate for various wide ranges of power efficient and low voltage biomedical applications.

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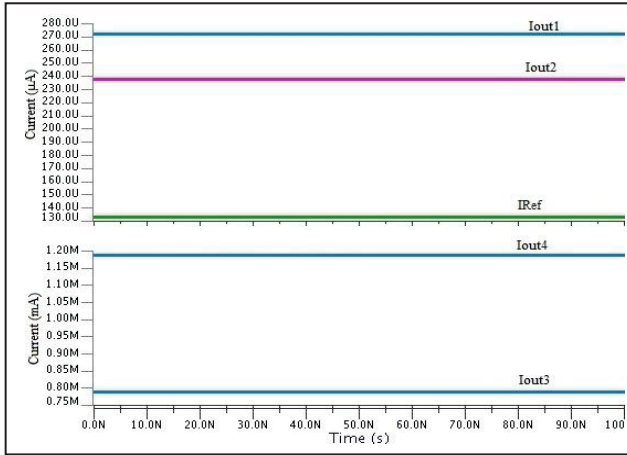


1.Current (IRef & Iout).

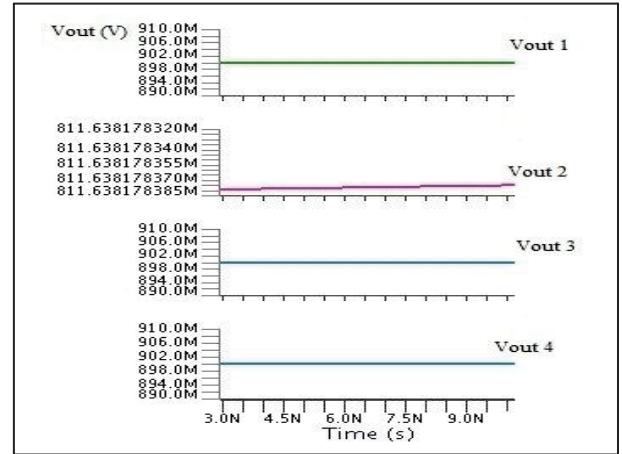


2.Output voltage (Vout).

Figure 4. The simulated transient response for  $V_{DD} = \pm 850\text{mV}$ .

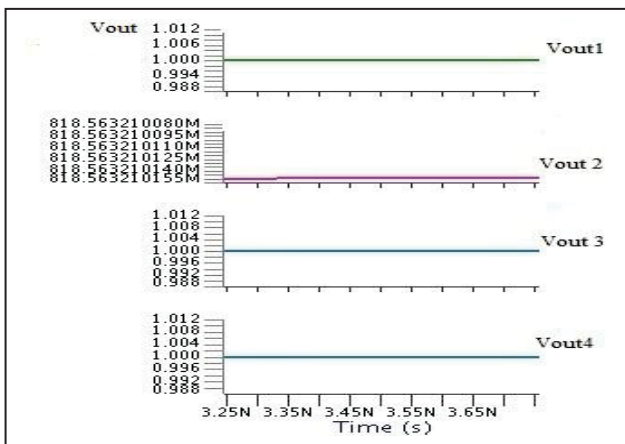


1. Current (IRef & Iout)



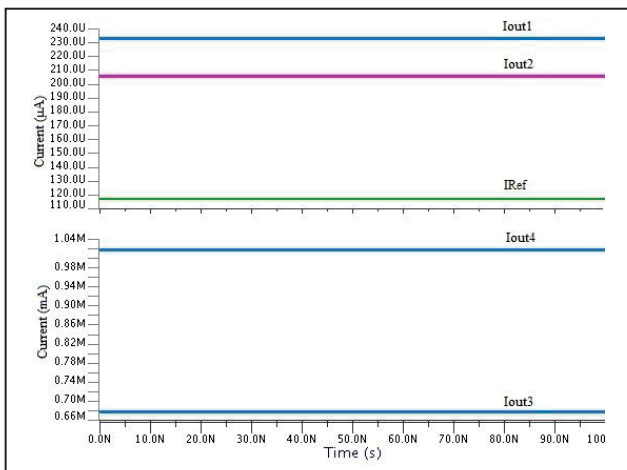
2. Output voltage (Vout).

Figure 6. The simulated transient response for  $V_{DD} = \pm 900\text{mV}$



2. Output voltage (Vout).

Figure 5. The simulated transient response for  $V_{DD} = \pm 1\text{V}$



1. Current (IRef & Iout)

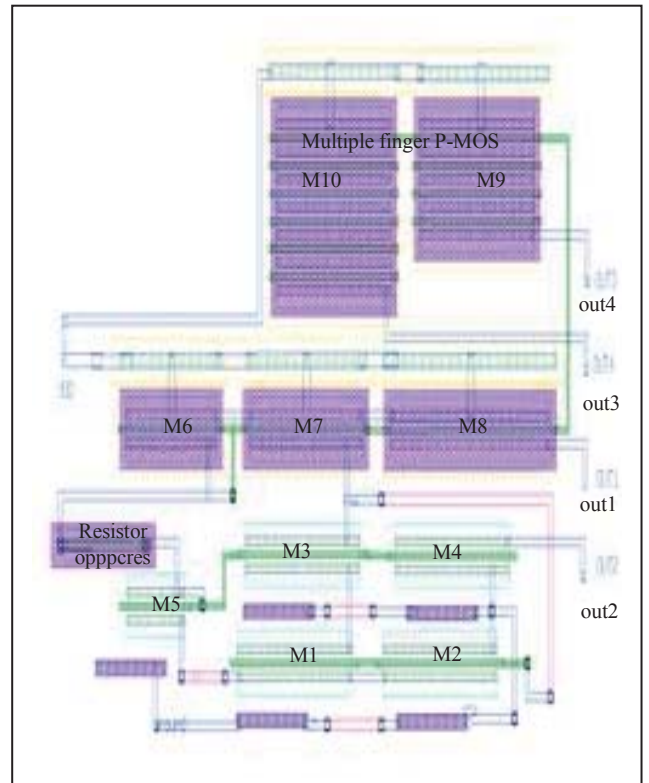


Figure 8. Layout of the proposed circuit