Depletion and Harvesting Thermal Energy from Actuator Arm Electronics in Hard Disk Drives

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Di Wu

School of Engineering and Advanced Technology,

Massey University, Albany

New Zealand

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Abstract

In recent years, thermally assistive magnetic recording (TAMR) has been applied on actuator arm electronics (AE) in hard disk drive (HDD). When HDD operates, temperature of the AE chip inside enclosure can be as high as 80-100 ºC, primary caused by processing and conditioning of magnetic signals and heated by wasted mechanical energy in form of thermal energy. To guarantee reliability of electronic device, AE chip junction temperature should be maintained at a relatively low level, which requires novel depletion of thermal energy. There are generally two methods to manage the thermal dissipation of chips. One is to follow existing approaches that conduct the thermal energy from the topside of the chip to a heat sink through a conductive paste, or other mediums. The other way is to dissipate the heat from the inner surface of the chip to a heat sink through silicon substrate.

In this thesis, thermal analysis of AE chip junction temperature is presented and discussed. Depletion of thermal energy generated by the AE chip will be characterized among several thermal management configurations. Then, a thermal resistance network model is established for AE chip junction temperature to ambient. The thermal resistance network is based on heat transfer paths from the chip to ambient. Every thermal resistance in the network can be calculated by analytical expression. The accuracy of the presented model will be also proven through comparing the results of mathematic model and simulation. Finally, based on the thermal analysis and managements, design of a novel active thermal energy harvester to transform the wasted energy into electrical energy will be presented. Finite element analysis (FEA) software is used to simulate piezoelectric characteristics of the thermal energy harvester.

Acknowledgements

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Chapter 1

Introduction

1.1 Problem Description

To achieve magnetic recording densities of more than 1 Tb/in^2 for hard disk drives (HDD), one of the key research and development focuses in recent years is on thermally assistive magnetic recording (TAMR). While most research focus is placed on dynamics of head-disk interface spacing and corresponding material characteristics of ultra-thin lubricant, not much has been given to integration perspective in ensuring the realization of technology. With the TAMR technology, lubricant needs to be heated to allow sliders to fly lower so as to ensure enhancement of magnetic recording strength. It is reported from laboratory measurements [1] that reliability issues have been raised for actuator arm electronics with TAMR technology. The actuator arm electronics (AE) are commonly integrated in form a silicon chip located on flexible cable side attached to a rotary actuator in a HDD. When HDD operates, temperature of the AE chip inside enclosure can be as high as 80-100ºC, primary caused by processing and conditioning of magnetic signals and heated by wasted mechanical energy in form of thermal energy.

1.2 Thermal management

To guarantee the reliability of electronic device, AE chip junction temperature to ambient should be maintained at a relatively low level, which requires novel depletion of thermal energy. There exist rich literatures on thermal management for flip chip packaging. As shown in Fig 1.1, several thermal enhancing techniques including copper heat spreader,

thermal pads, metallic lid and heat sink were examined to enhance the thermal performance of flip chip [2]. Attaching a copper heat spreader on the die back side significantly increases heat flow dissipation to air from 1.5% to 43%, which results in a 32% reduction in junction-to-air thermal resistance (Rja). This enhancement can be further improved by adding soft pads in between the substrate and the heat spreader. This technique not only increases the back side heat flow from 43% to 82%, also creates an additional conduction path to help heat spreading in the substrate. This dual heat transfer path makes the second method (combining heat spreader and soft pads) one of the best enhancing techniques. With a heat sink attached on the metallic lid, due to the dramatic increase in heat transfer area, it creates the best improvement with a 50% reduction in Rja. However, the associated issues on cost, limited space and reliability need to be considered.

A packaging technology interconnecting flip-chip solder attached chips on a silicon substrate has been developed at AT&T Bell Laboratories [3]. This technology, which is referred to as Advanced VLSI Packaging (AVP), will impact electronic system designs by decreasing size, weight, and power, while increasing performance and reliability. The thermal management approach of AVP is to dissipate chip power through the silicon substrate to a heat sink or other packaging levels. Lee and Ghaffari analyzed thermal performance of typical packaging assemblies affected by thermal vias, solder bump heights, high-power I/O drives and chip sizes [4]. Figure 1.2 shows the side view of the heat transfer model configuration of AVP structure.

Micro-channel heat sink, as an integrated part of silicon based electronic device, is another solution to depletion of thermal energy from chips. Yogendra Joshi et al studied stacked micro-channel heat sinks for micro-electronic cooling [5]. A schematic of the stacked micro-channels is shown in Fig 1.3. They effectively reduced thermal resistance of the stacked micro-channel heat sinks through optimizing the aspect ratio, fin width and the channel to fin width ratio and pumping power.

A thermal solution for flip chip preamp die on flex applications was presented via a new

flex design [6]. Fig 1.4 shows schematic cross-sections of a standard preamp flex assembly and the improved thermal design flex assembly. This new design incorporates an opening in the flex circuit under the center region of the preamp die thus removing the low thermal conductivity flex materials and exposing the aluminum stiffener plate. The surface of the aluminum stiffener plate is modified by zincation followed by electrolytic Ni, immersion Sn plating. This provides a solderable surface that readily forms a metallurgical bond with solder. Thermal solder bumps that are of order 3X the volume of the electrical bumps are added to the center region of the preamp die which resides above the opening in the flex circuit. Through experiments, this new design has a 50-60% improvement in thermal resistance between the die and the stiffener plate as compared to the conventional design.

1.3 Literature of micro heat engines

Microelectromechanical systems, or commonly called MEMS, are often used as part of sensors, actuators, and electrical and mechanical systems on a silicon substrate through microfabrication technology. MEMS are made up of components between 1 to 100 micrometers in size and MEMS devices generally range in size from 20 micrometers to a millimeter. They have been proven to be a key enabling technology of developments in areas such as transportation, telecommunications and health care. The most significant advantage of MEMS is their ability to communicate easily with electrical elements in semiconductor chips. Other advantages include small size, lower power consumption, lower cost, increased reliability and higher precision. Recently, new types of thermomechanic heat engines are commonly applied for thermal energy harvesting at microscale.

Huesgen et al designed a micro heat engine which is self-starting and self-regulating as shown in Fig 1.5 [7-8]. Its operation principle is based on a cavity filled with a liquid–gas phase-change working fluid that performs a self-controlled reciprocating motion between a heat source and a heat sink. A bistable buckling membrane generates the respective upward

and downward driving forces upon expansion and contraction of the working fluid. Heat transfer into the engine chamber causes thermal expansion of the working fluid in 'down-state'. Due to the strongly nonlinear behavior of the bistable membrane, the engine chamber snaps into the 'up-state' when a defined threshold pressure is exceeded in the engine chamber. Then, heat is rejected to the heat sink and the working fluid pressure drops. When the pressure falls below a negative threshold, the engine chamber moves downward again.

Ujihara et al proposed a thermal energy harvester, based on a second-order phase transition of a soft ferromagnetic material as shown in Fig 1.6 [9]. In this device, a ferromagnetic material plate performs a reciprocating motion between a heat source and a heat sink. Thereby, a permanent magnet attracts the plate to the heat source. The plate becomes paramagnetic above the Curie temperature and is then pulled back to the heat sink by mechanical springs. The oscillation frequency depends on the temperature difference applied.

1.4 Piezoelectric applications in MEMS

The need for miniaturized power sources for MEMS and microelectronics devices has long been recognized. Piezoactuation is one of the most common mechanisms for actuation and sensing in micro electromechanical system devices. Piezoelectric thin films which are proposed as a means to convert mechanical to electrical energy have been employed in several applications including various micro manipulation tools, fluid transport, accelerometers, and ultrasonic transducers. In all of these applications, a piezoelectric film is deposited on a substrate of certain geometry, commonly a cantilever beam or a membrane. In general, ferroelectric materials have been the materials of choice for piezoelectric applications as they exhibit the highest piezoelectric constants and electromechanical coupling factors necessary to produce electrical energy efficiently. Besides, the ability to pole ferroelectrics in any desired direction offers a great advantage in

design flexibility. Among the available ferroelectric materials, lead zirconate titanate (PZT), $Pb(Zr_xTi_{1-x})O_3$, is the most popular due to its superior dielectric constant, piezoelectric constants, and thermal stability.

Richards et al designed a dynamic micro heat engine at Washington State University. The micro engine is shown in Fig 1.7. The engine consists of a cavity, filled with a liquid-gas phase-change working fluid. In this engine, thermal power is converted to mechanical power through the use of a novel thermodynamic cycle [10-13]. Mechanical power is then converted into electrical power through the use of a thin-film piezoelectric membrane generator. Periodic heating and cooling caused an oscillation of a thin membrane for electrical power generation. The behavior of the thin-film PZT membranes operated at high deflections and strains has also been studied [14].

Based on aforementioned micro heat engine, a new thermodynamic cycle on the micro-scale has been presented. This new cycle is the result of resonant operation and cycle work production from a MEMS-based micro-heat engine. The engine shown in Fig 1.8 is constructed of two thin membranes surrounding a cavity filled with working fluid [15]. This new thermodynamic cycle is shown to include nearly constant volume pressure increase, expansion, heat rejection, and compression components. A thermal switch is integrated with the micro-engine to control heat rejection. The micro-engine is shown to produce up to 6.7 μW of cyclic mechanical power when operated on this cycle. Micro-engine natural frequency is shown to vary from 90 to 140 Hz. The micro engine is shown to operate across a low temperature gradient of 1.5 °C.

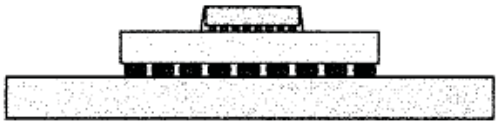
1.5 Organization of this thesis

Based on aforementioned literature, this thesis develops two types of thermal solutions for AE chip in HDD. This section provides a brief overview of Chapter 2, Chapter 3 and Chapter 4.

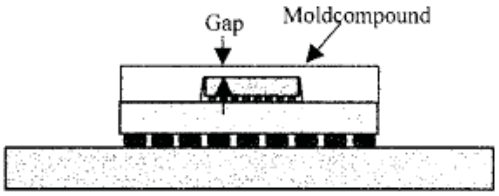
Chapter 2 presents a thermal solution for AE Chip via a new flex design. Depletion of thermal energy generated by the AE chip will be characterized among several thermal management configurations.

Chapter 3 describes a thermal resistance network model for calculating arm electronics chip junction temperature to ambient. The thermal resistance network is based on heat transfer paths from chip to ambient. It will be demonstrated that the proposed model can be used to predict AE chip junction temperature accurately.

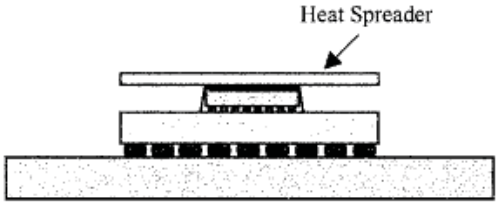
Chapter 4 shows a design of a novel active thermal energy harvester to transform the wasted energy into electrical energy. The conversion from mechanical to electrical energy will be simulated using ANSYS software.



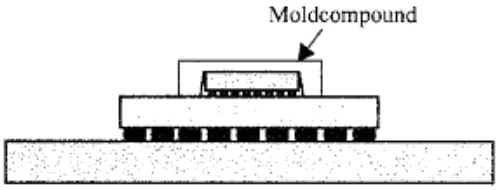
Type 0 No enhancement



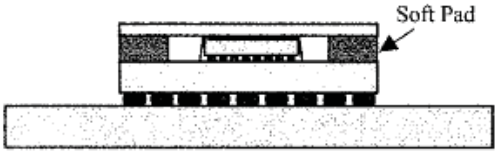
Type 4 (a)(b) With moldcompound (varying gap in the moldcompound)



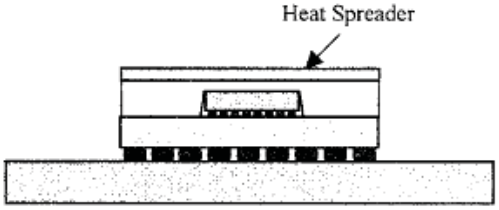
Type 1 With copper heat spreader (varying thickness from 0.3 to 2.0 mm)



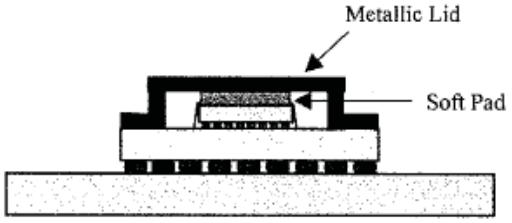
Type 4 (c) With moldcompound (varying percentage of coverage, 26%)



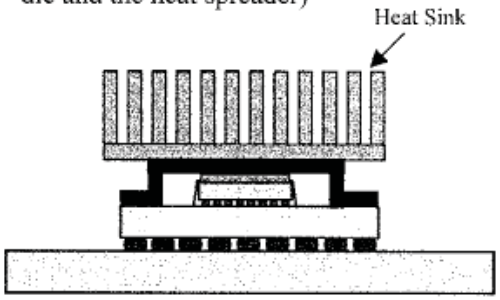
Type 2 With copper heat spreader and soft pad



Type 5 With moldcompound and copper heat spreader (varying gap between the die and the heat spreader)



Type 3 With metallic lid (aluminum or copper)



Type 6 With metallic lid and heat sink (aluminum)

Fig 1.1 - Illustrations of different thermal enhancing techniques

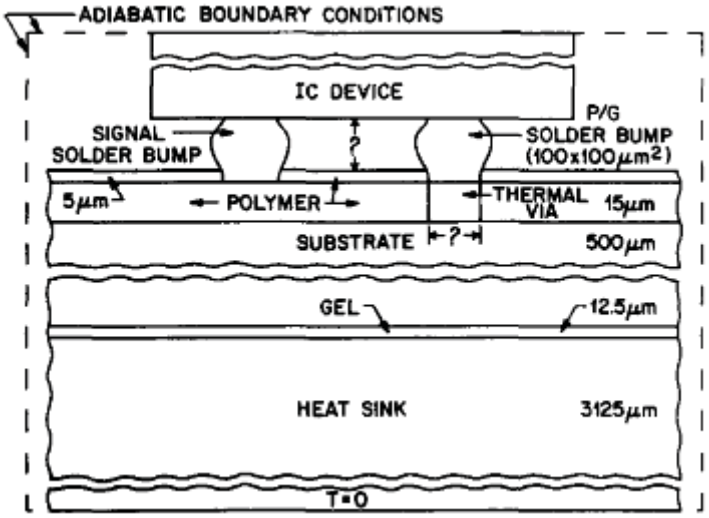


Fig 1.2 - Cross-sectional view of the heat transfer model configuration

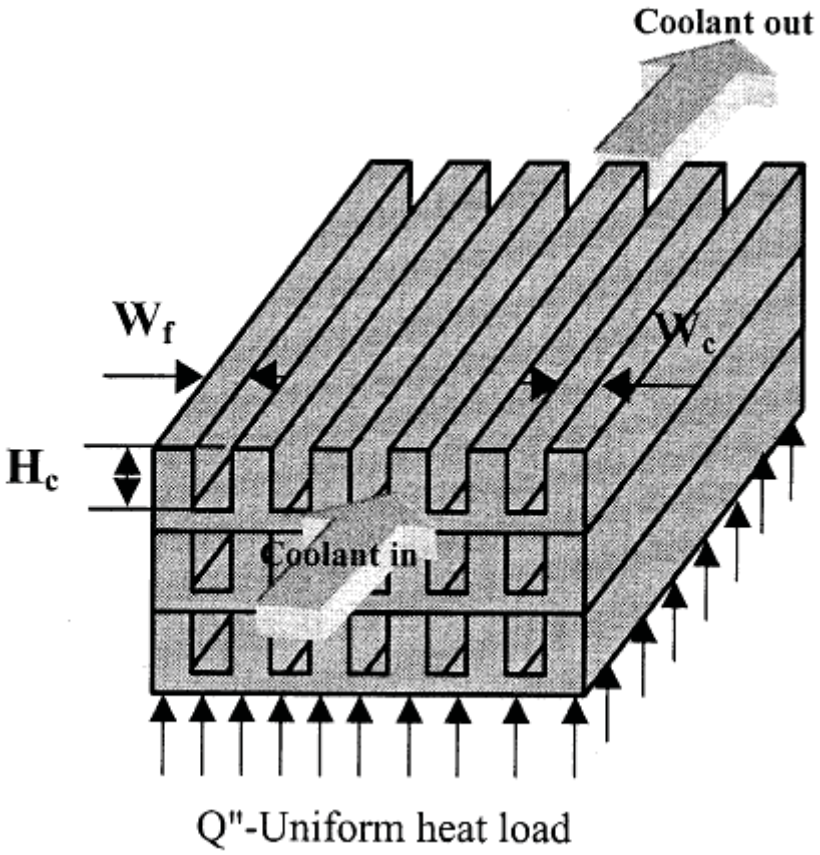


Fig 1.3 - Three-dimensional stack of micro-channels

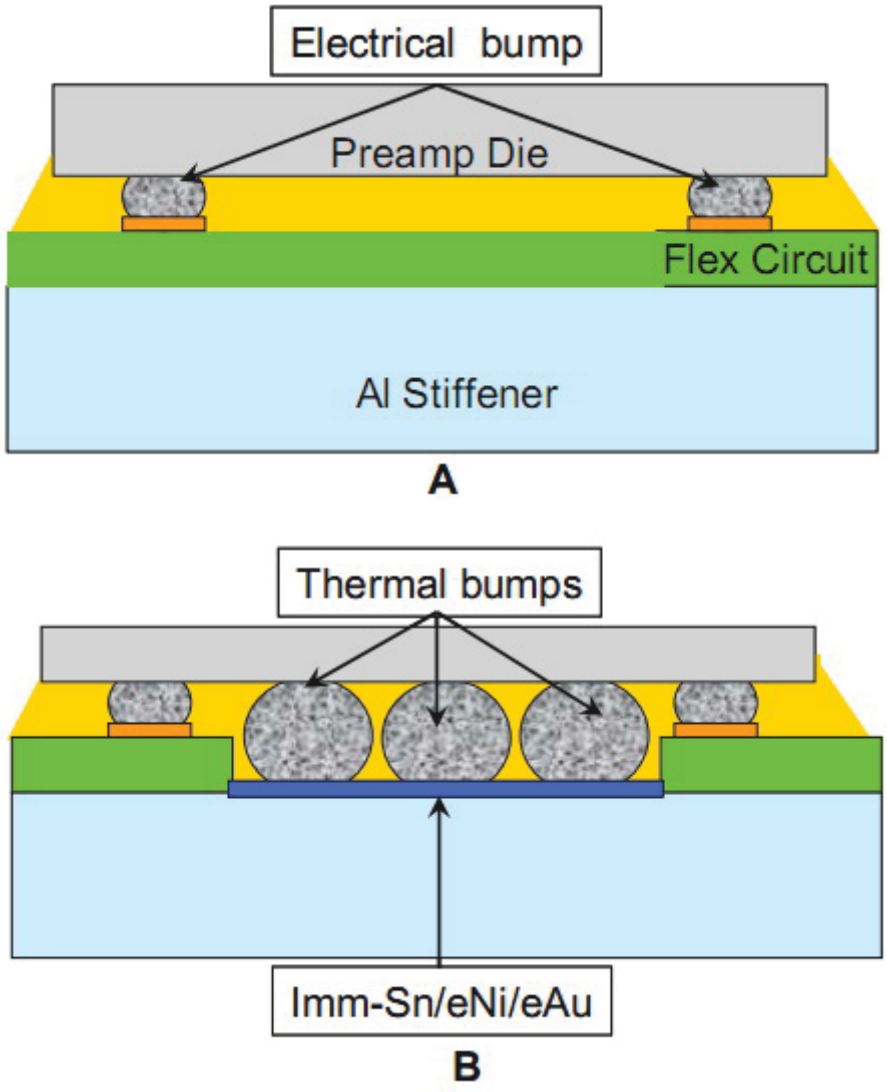


Fig 1.4 - Schematic cross-sections of standard preamp flex assembly (A) and improved thermal design flex assembly (B)

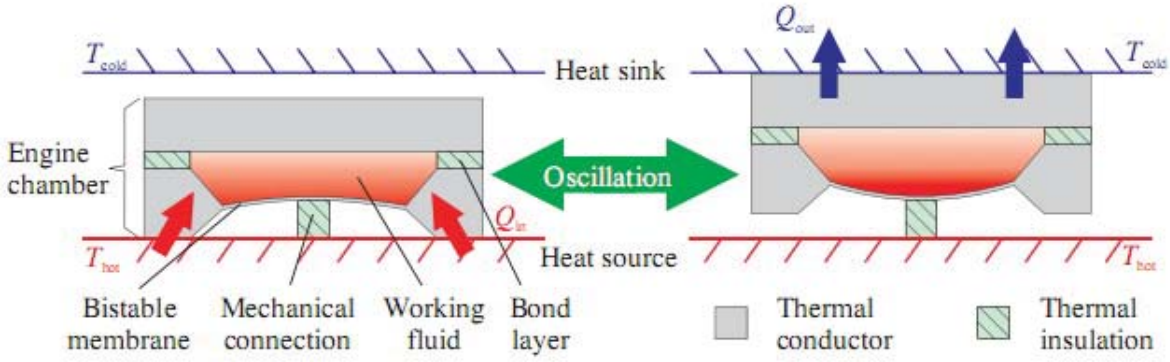


Fig 1.5 - Schematic cross-sectional view of the micro heat engine: (a) in 'down-state' and (b) in 'up-state'

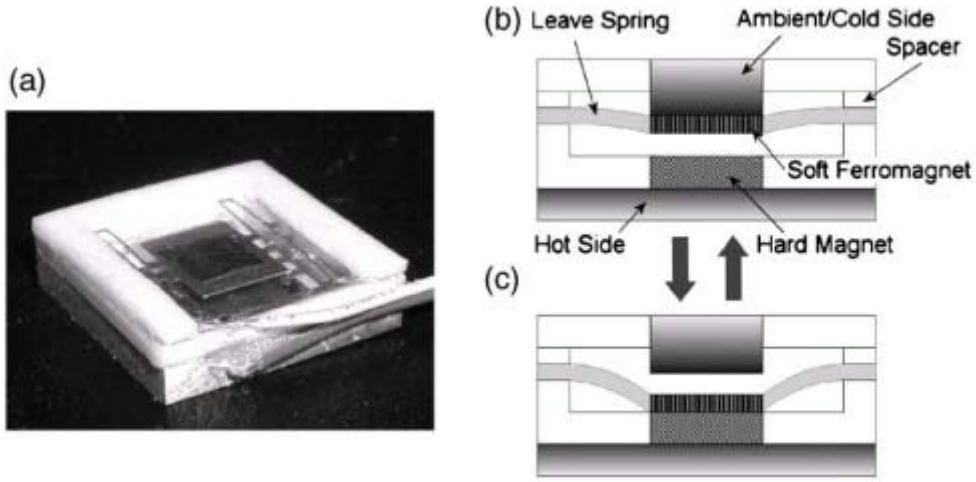


Fig 1.6 - (a) Actual device, (b) cross section during cooling, and (c) cross section during heating

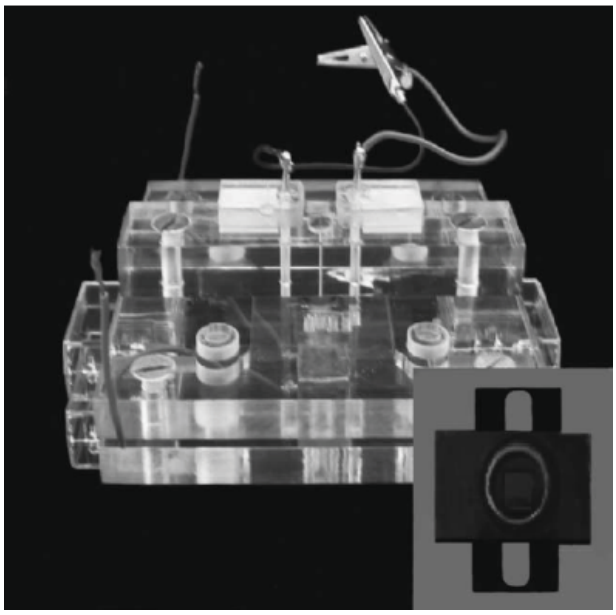


Fig 1.7 - Photograph of micro heat engine with inset showing top view of engine

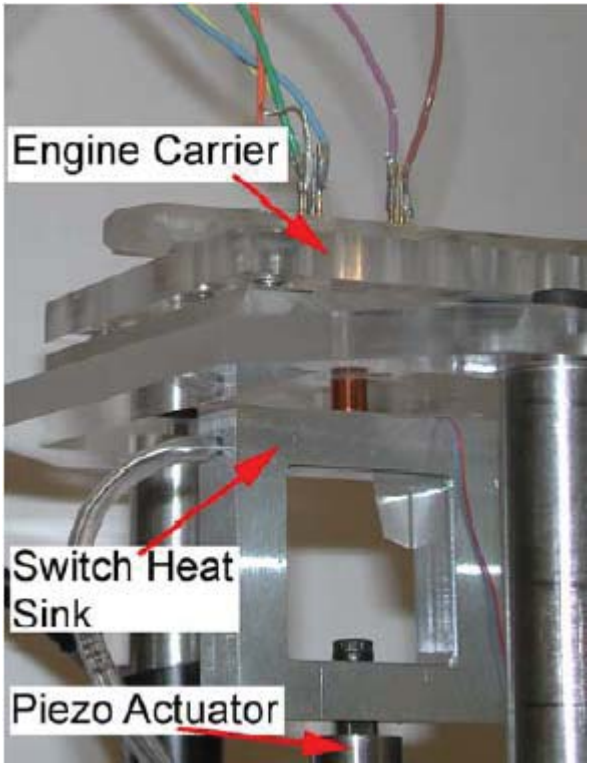


Fig 1.8 - Assembled engine and thermal switch

Chapter 2

Analysis of thermal energy depletion

2.1 Description of solid model

Flip chip devices utilize solder bumps to interconnect the silicon integrated circuit die and the package substrate or circuit board. The solder bumps provide both the electrical and mechanical connection between the die and the substrate or board. In addition the solder bump provides a relatively high thermal conductivity heat transfer path from the die to the substrate or board metal layers.

In a commercial 3.5-inch hard disk drive shown in Fig 2.1, Hard disk drive applications utilize high power preamp to amplify the electrical signals from the head of the actuator arm as it moves across the rotating platters. To maximize performance it is desirable to locate the preamp as close as possible to the actuator head, where the read and write functions occur. This is achieved by mounting the AE chip preamp to a flex circuit. The AE chip end of the flex circuit is attached to the actuator arm and the opposite end of the flex circuit is connected to the stationary drive chassis. The flex circuit consists of a copper metallized polyimide tape that is connected to a stiffener plate. Adhesive layers are utilized to attach the Cu metal to the polyimide tape and to attach the polyimide tape to the stiffener plate. The stiffener plate, commonly made of aluminum, provides mechanical support for the AE chip as well as a mating surface for connection to the actuator arm.

In the baseline case as what one can observe in most HDDs, the thermal energy of AE chip is mainly depleted to the actuator arm through solder bumps with little contribution from the otherwise conductive underfill material and flex cable layers. The underfill material and

flex cable layers have very low thermal conductivity, k ~ <1 W/mK, making them highly resistive to heat flow. Unfortunately, the reliability and ultimately the performance of the AE chip and the bump interconnect degrades as the temperature is increased. Thus the lack of air or liquid cooling often leads to a trade off in die size, performance, and reliability.

As contrast to the baseline design, a solid model as illustrated in Fig 2.2 was built using Solidworks from which several thermal finite element analyses [16] were conducted. The model consists of an actuator arm and a flex cable heat sink made of aluminum material covered by flex cable layers and an AE chip interconnected to the flex cable by solder bumps and underfill material, and a solid plate-like copper structure. As illustrated in Fig 2.3(a), the copper plate is extruded from the aluminum heat sink and is directly contacted with the inner surface of AE chip. The improved thermal design provides a direct thermal connection from the AE chip to the aluminum stiffener plate through the copper plate. Materials properties and dimensions of the aforementioned components are based on components extracted from a commercial 3.5-inch hard disk drive. In the present finite element models, it is assumed that cooling via air flow over the backside of the AE chip is typically not possible. Thus, thermal energy generated by the AE chip can only be dissipated via conductive heat transfer mechanism through flex cable, heat sink and the actuator component into ambient atmosphere. Effect of air flow from disk rotation for forced convective heat transfer is assumed to be negligible.

2.2 Depletion of thermal energy

Depletion of thermal energy generated by the AE chip is discussed in this section in the context of thermal management design over flex cable heat sink. Detailed FEA heat transfer was simulated in steady-state condition. In this model all interfaces (connection between the copper plate and the Al stiffener, the copper plate and the AE chip) were assumed to be ideal thermal interfaces (no thermal loss at any interface). From finite element simulations as shown in Fig 2.4, steady-state temperature rising of the AE chip is in general a liner

function of uniform heat source power generated inside the chip. Starting from ambient temperature of 27ºC, without the copper plate and with uniform 2 Watts of power generated by the AE chip, the temperature rising can be up to 60 degree resulting in about 85ºC at the AE chip. With increasing copper plate area, the temperature rising is found to be monotonically decreased. As compared to the 0% coverage case, up to 50% reduction of temperature rising at each supply power can be achieved when 80% of AE chip is contacted with the copper plate.

Depending location where power generation unit is embedded, heat source power distribution is often found to be non-uniform concentrated in most chips. Effect of heat source locations on the depletion of thermal energy by the copper plate was investigated by using two heat source locations, namely at the centre and at the corner as illustrated in Fig 2.3(b) and (c), respectively. At ambient temperature of 27 ºC, Fig 2.5 and Fig 2.6 show plots of temperature rising of AE chip versus power of chip when heat source is at the centre and at the corner, respectively. Plots are shown for different copper area coverage. With 2 Watts of power generated by the AE chip, it is can be seen from Fig 2.5 that there is a dramatic decrease of temperature rising from 62 ºC to 41 ºC when copper area coverage increases from 0 to 20%. While there are small changes of temperature rising, when the copper area coverage changes from 40%, 60% to 80%. From Fig 2.6, with 2 Watts of power generation of the AE chip, we can see that the temperature rising decreases monotonically when the copper area coverage increases from 0, 20%, 40% to 60%, and there is a remarkable reduction of temperature rising with the copper area coverage changing from 20% to 40%. It is also interesting to find that the temperature rising increases when the copper area coverage increases from 60% to 80%.

Defining thermal resistance relating maximum junction temperature to air as indication of thermal energy depletion efficiency is shown in Table 2.1. The thermal resistance, R_{ja}, was calculated using the equation (1):

$$R_{ja} = (T_j - T_a)/Q \quad (1)$$

Where T_j is the maximum junction temperature of the AE chip, T_a is the ambient temperature, and Q is the power of the AE chip.

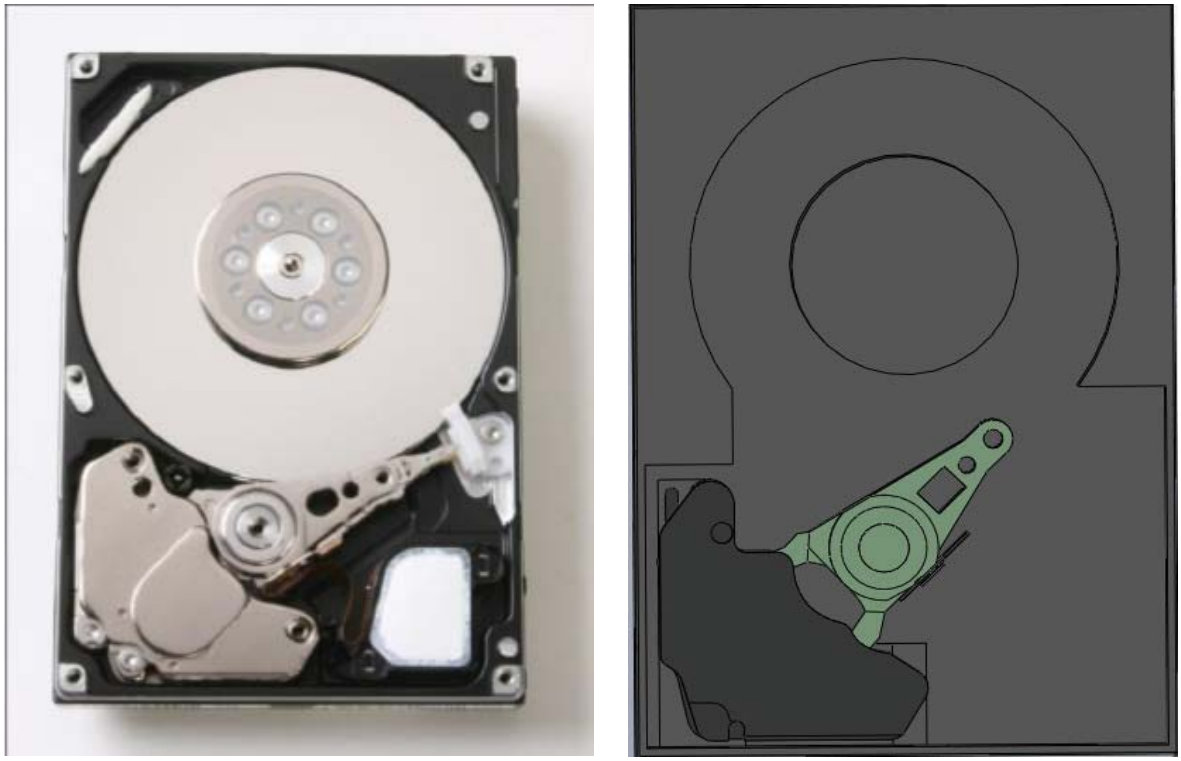
Table 2.1 summarizes the thermal resistances data for the uniform heat source, the centre heat source and the corner heat source. It is found that one needs to customize placement of the copper plate according to the location of heat source to achieve optimized thermal energy depletion from AE chip. It is interesting to note that by concentrating heat source at the centre, Type (2) cases, thermal resistance decreases as compared to Type 1 when varying copper area coverage from 20%, 40% to 60%. The third type shows that heat source is equally distributed in a quarter of the chip volume at the corner. In this case, thermal resistance increases dramatically as compared to Type 1 when copper area coverage is 0 and 20%. While there are small changes between Type1 and Type 3 when copper area coverage changes from 40% to 80%. In general, it is not effective to dissipate thermal energy when the heat source is placed at the corner, it is possible the reason that the copper plate is placed underneath the center region of the AE chip.

The degree of thermal dissipation can be also related to different locations and volumes of heat source in the chip. Fig 2.7 shows changes of dimension and location of heat source. With copper area being set at 80% of AE chip and power of the chip being 2Watts, it is observed as shown in Fig 2.8 that AE temperature rising can be optimized if the heat source unit can be placed at the centre, Fig 2.7(a) case, or at the quarter centre, Fig 2.7(c) of the chip.

2.3 Chapter summary

Based on the standard thermal design of hard disk drive, a new thermal solution for AE chip preamp was discussed in this chapter. A solid plate-like copper structure is extruded from the aluminum heat sink and is directly contacted with the inner surface of AE chip. The structure of the model in hard disk drive was built using Solidworks software. The

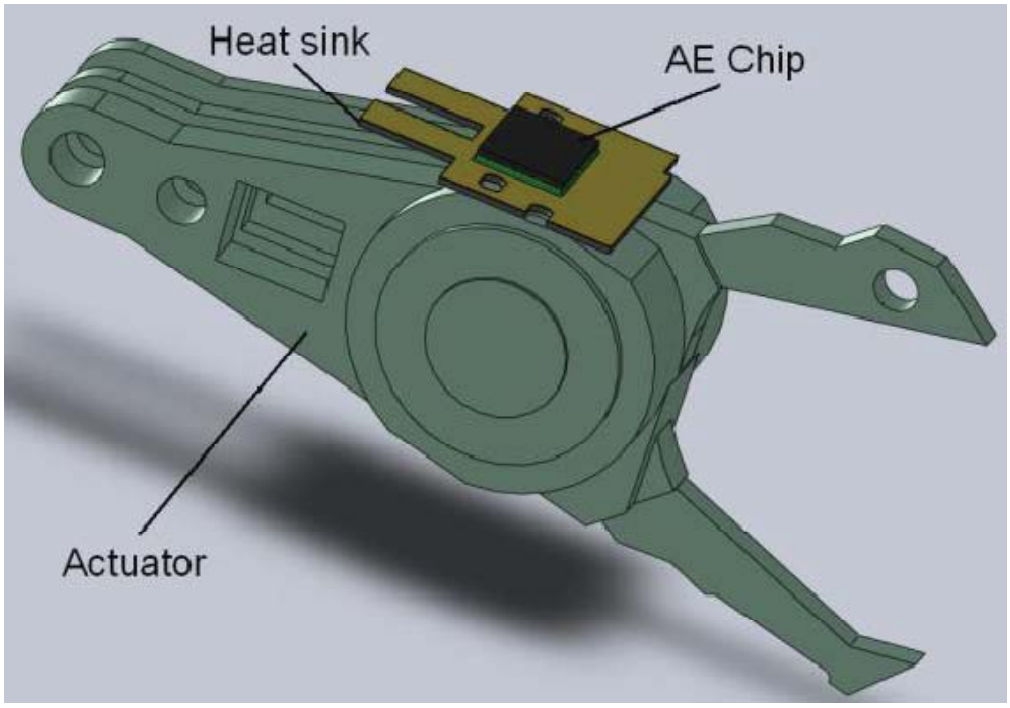
depletion of thermal energy from HDD AE chip was simulated in paper parametric studies of placement and dimension of copper plates as well as location of heat source in the chip. It is found that by concentrating heat source at the centre, AE chip junction temperature decreases as compared to uniform heat source when varying copper area coverage from 20%, 40% to 60%. Because the copper plate is placed underneath the center region of the AE chip, the depletion of thermal energy is not desirable when the heat source is placed at the corner. So, when heat source distribution is non-uniform one needs to customize placement of the copper plate to reach better heat depletion rate.



(a) Photograph (b) solid model

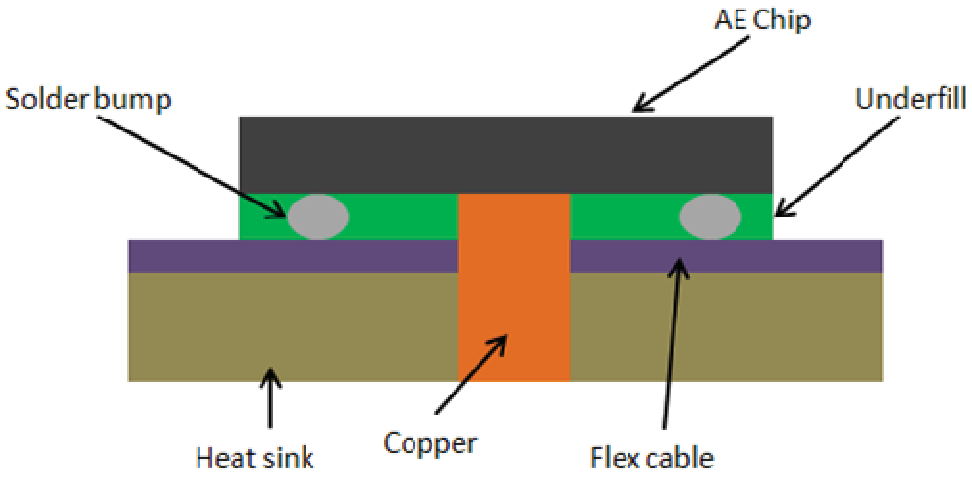
Fig 2.1 - 3.5-inch hard disk drive

(a) Photograph

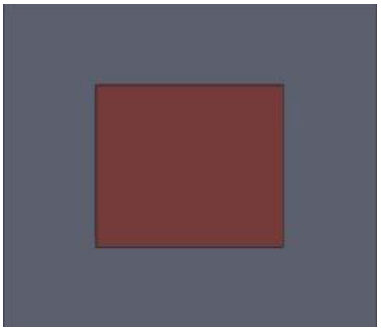


(b) Solid model

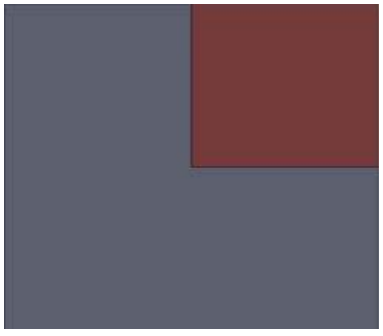
Fig 2.2 - Actuator arm electronics system showing location of AE chip on flex cable heat sink



(a)



(b)



(c)

Fig 2.3 - Schematics showing copper location, (a) and two different heat source locations, (b) and (c)

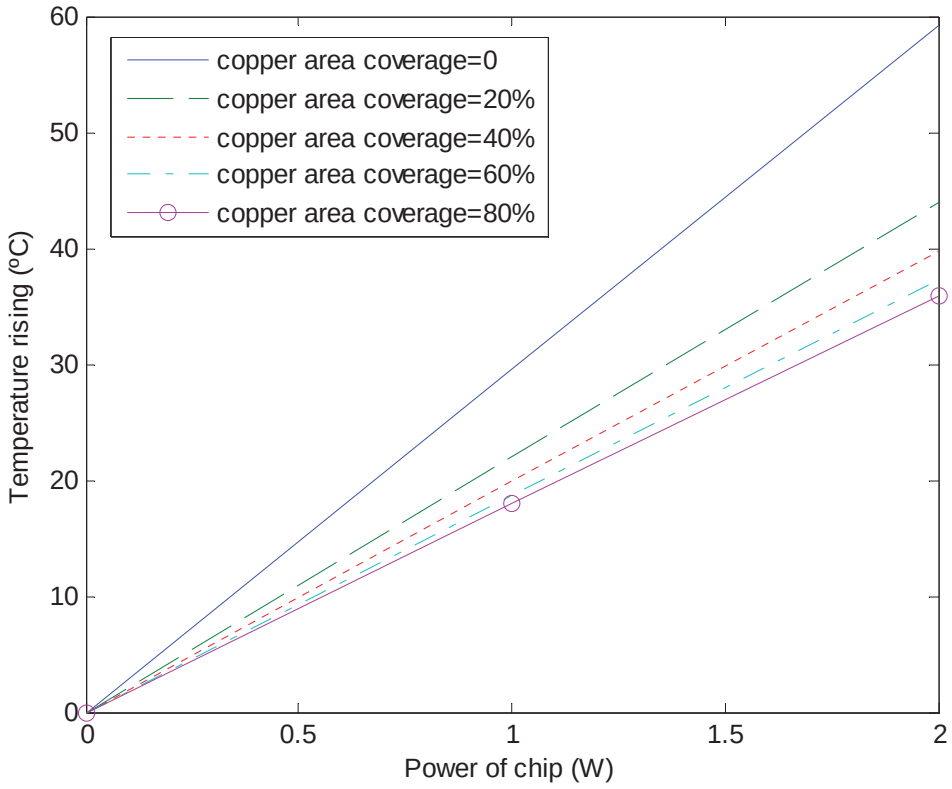


Fig 2.4 - Temperature rising as a function of uniform source power

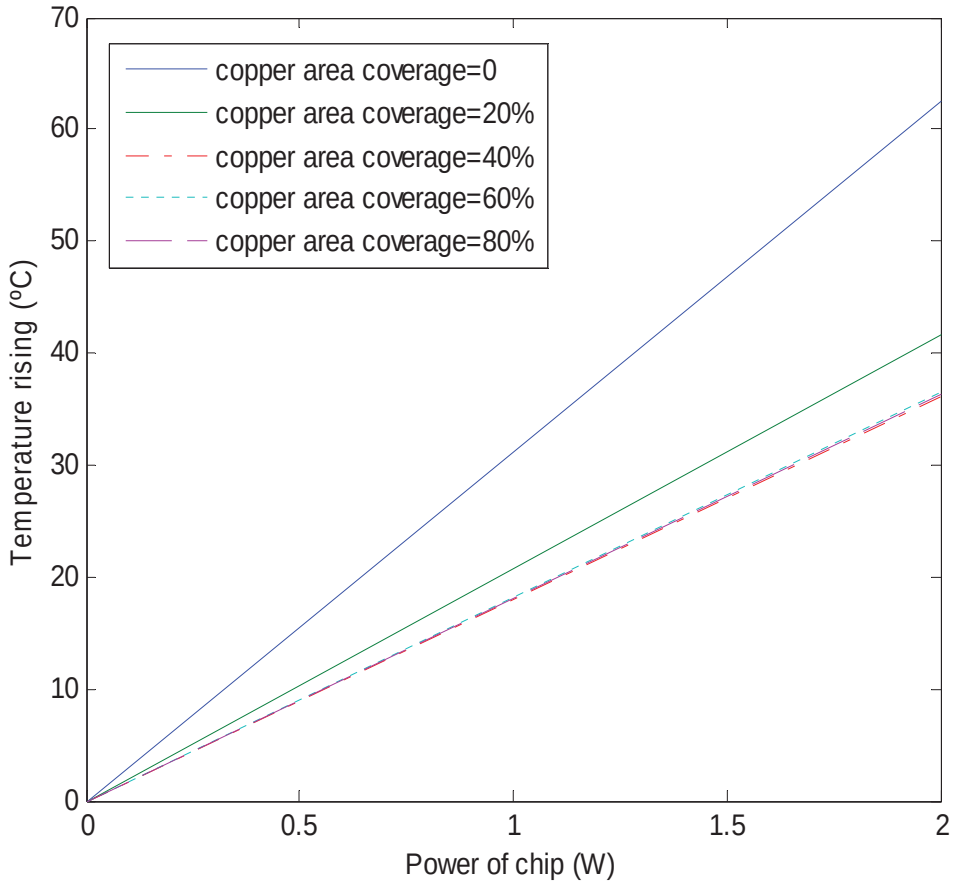


Fig 2.5 - Temperature rising as a function of center source power

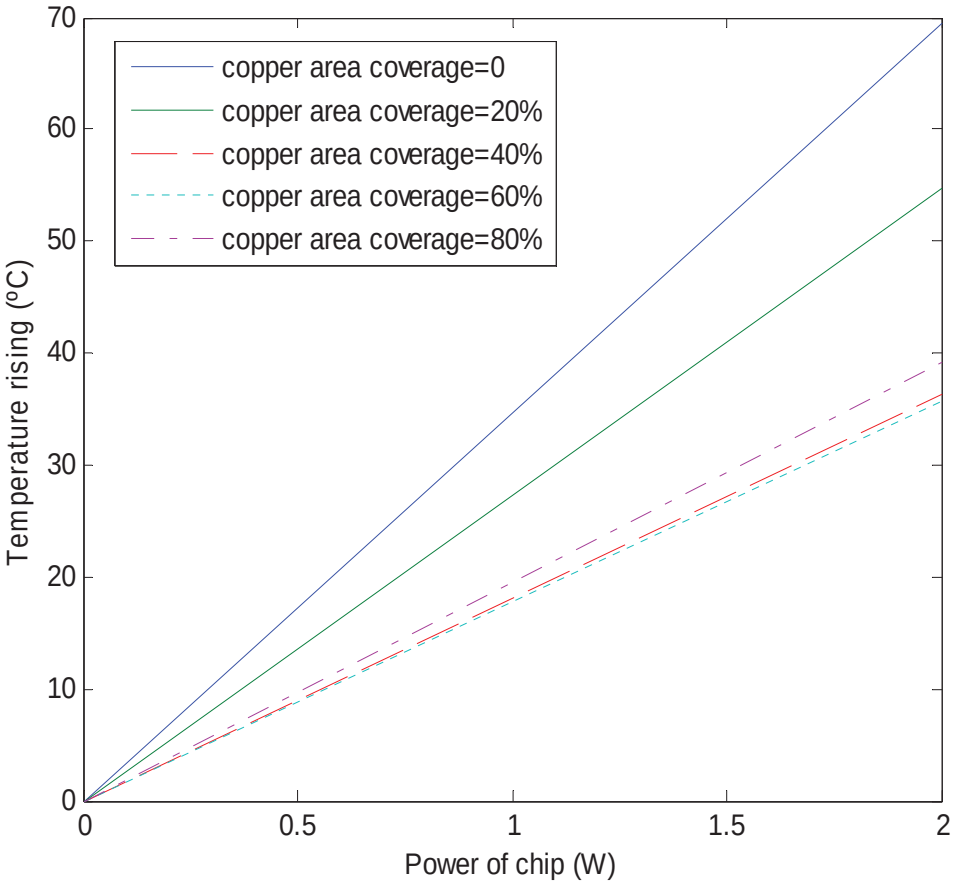


Fig 2.6 - Temperature rising as a function of corner source power

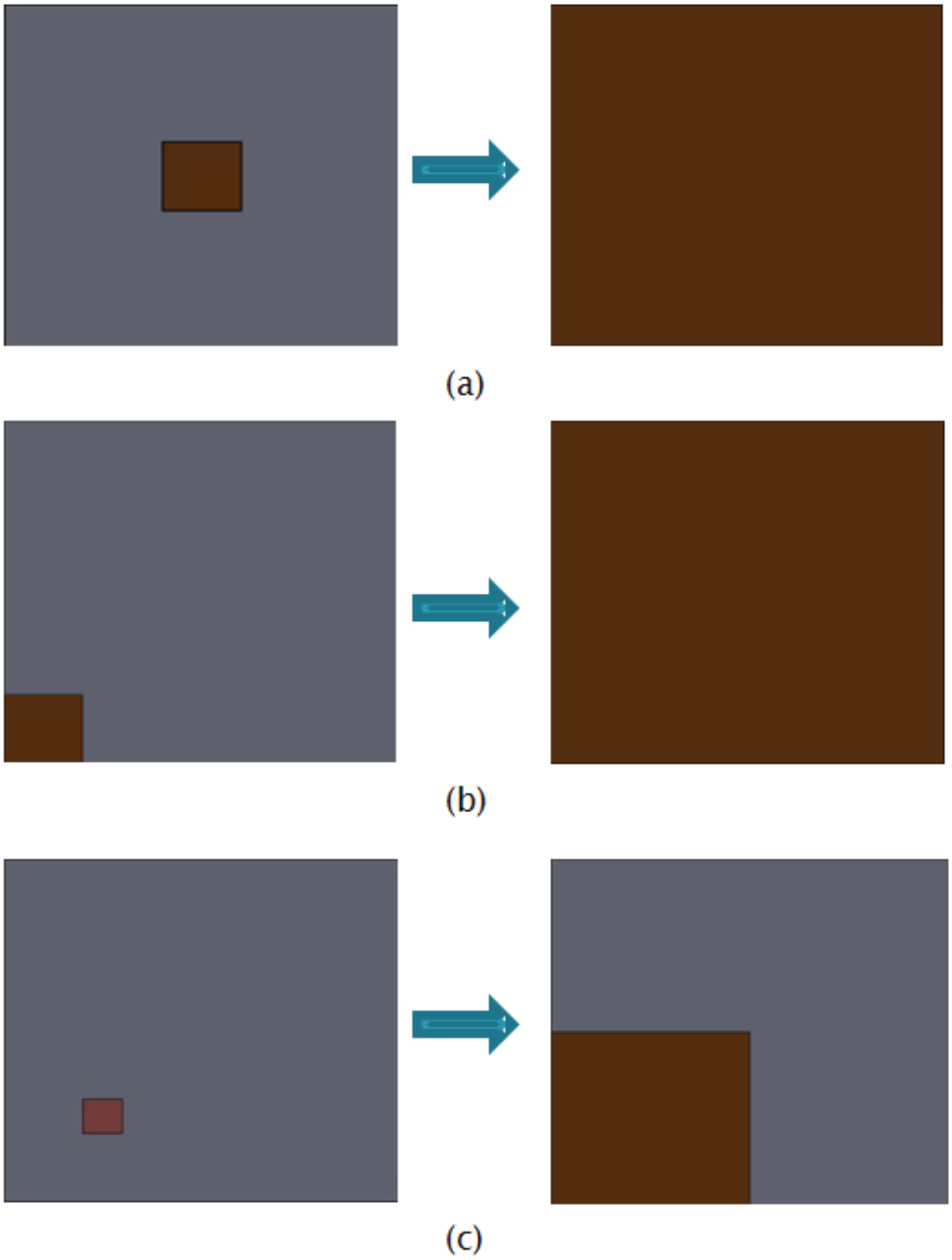


Fig 2.7 Changes of dimension and location of heat source

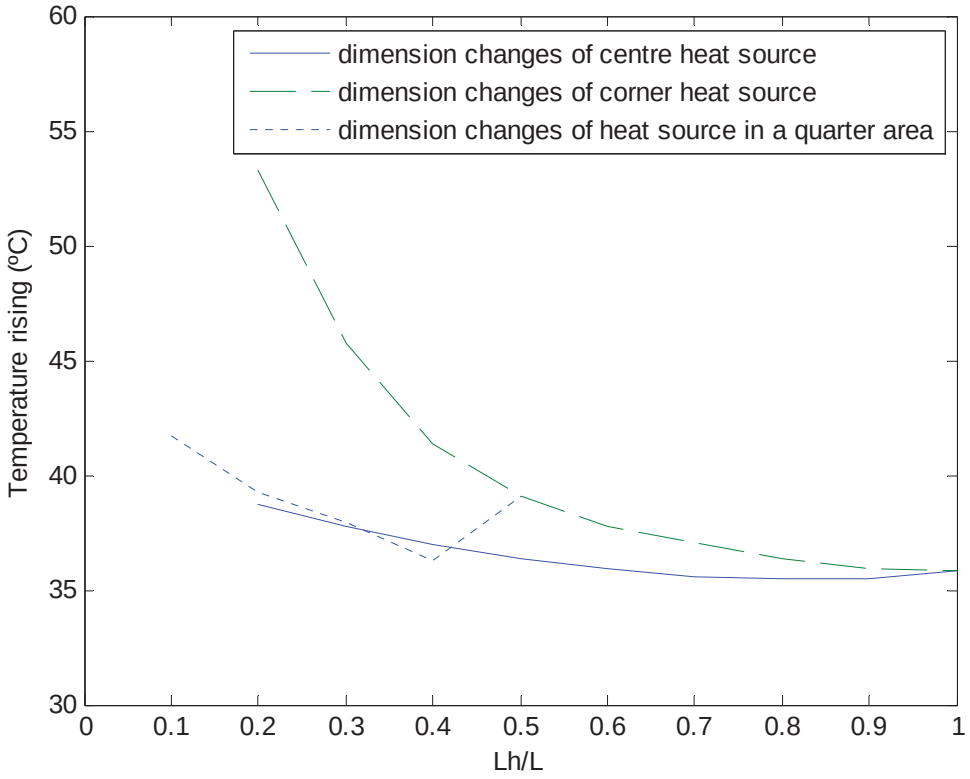


Fig 2.8 - Temperature rising as a function of dimension ratio of heat source (Lh) to chip (L)

Table 2.1 - Comparison of Thermal Dissipation

Type No.	Description	Thermal Resistance (K/W)
1(a)	Uniform heat source distribution, without copper	29.59
1(b)	Uniform heat source distribution, with 20% copper coverage	21.94
1(c)	Uniform heat source distribution, with 40% copper area coverage	19.86
1(d)	Uniform heat source distribution, with 60% copper area coverage	18.64
1(e)	Uniform heat source distribution, with 80% copper area coverage	17.90
2(a)	Heat source concentrates at the centre, without copper	31.23
2(b)	Heat source concentrates at the centre, with 20% copper area coverage	20.78
2(c)	Heat source concentrates at the centre, with 40% copper area coverage	18.10
2(d)	Heat source concentrates at the centre, with 60% copper area coverage	18.26
2(e)	Heat source concentrates at the centre, with 80% copper area coverage	18.18
3(a)	Heat source concentrates at the corner, without copper	34.77
3(b)	Heat source concentrates at the corner, with 20% copper area coverage	27.43
3(c)	Heat source concentrates at the corner, with 40% copper area coverage	18.16
3(d)	Heat source concentrates at the corner, with 60% copper area coverage	17.88
3(e)	Heat source concentrates at the corner, with 80% copper area coverage	19.55

Chapter 3

Analytical thermal resistance model of heat transfer

3.1 Model development

To reduce the time of obtaining temperature of AE chip preamp in hard disk drive and improve the efficiency of electronic device design, it is of significance to establish an analytical thermal model for analyzing and calculating the temperature of AE chip preamp. Fig 3.1 shows a typical cross section of chip packaging which contains AE chip, solder bumps, flex cable layer, aluminum heat sink and a solid-like copper structure. The copper plate is extruded from the aluminum heat sink and is directly contacted with the inner surface of AE chip. In steady-state, the thermal energy generated by AE chip dissipates to ambient mainly in two paths: (1) part of the heat flows from the chip to the aluminum heat sink through the solder bumps and the flex cable layer, and then transfers to ambient from the bottom surface of the aluminum heat sink; (2) the rest heat flows from the chip to the copper and then separates into two parts: one transfers to ambient directly from the bottom surface of the copper, the other one spreads from the copper into flex cable layer and aluminum heat sink, and finally transfers to ambient from the bottom surface of the aluminum heat sink. According to the two paths of thermal energy dissipation from the chip to ambient, the thermal resistance network is established as shown in Fig 3.2.

R_s is thermal conductivity resistance of solder bumps. R_{c2} is one-dimensional conductivity resistance of the copper embedded in aluminum heat sink layer and R_{c1} is resistance of the rest part of the copper. R_{cf} and R_{ca} are thermal spreading resistances from the copper to flex cable and heat sink, respectively. R_a is one-dimensional conductivity resistances of the

aluminum heat sink. R_{sf} is thermal spreading resistance and one-dimensional conductivity resistance of the flex cable. R_{cm} is resistance between the bottom surface of the copper and ambient. R_{am} is resistance between the bottom surface of the aluminum heat sink and ambient.

The specific analytical calculation of every thermal resistance in Fig 3.2 will be discussed in the following parts respectively.

3.1.1 Calculation of R_{ca}, R_{cm}, R_{am} and R_a

There exists a thermal spreading resistance expression for calculating spreading resistance of isotropic plate with central heat source and edge adiabatic [17]. In present case, the equivalent heat source is not located on top surface of the heat sink and part of the heat sink is replaced by the copper, so an equivalent heat transfer coefficient at the bottom surface of the heat sink for calculating spreading resistance should be found. It is supposed that heat transfers from heat sink to ambient by convection with heat transfer coefficient h_{e1}. h_{e1} is given as:

$$h_{e1}=\frac{h(c_1d_1-c_2d_2)}{c_1d_1} \tag{2}$$

The spreading resistance from copper to heat sink R_{ca} is calculated by the following expression which shows the relationships with the geometric and thermal parameters of the system according to the notations in Fig 3.3:

$$\begin{aligned} R_{ca}=&\frac{1}{2c_2^2c_1d_1k_a}\sum_{m=1}^{\infty}\frac{\sin^2(c_2\delta_m)}{\delta_m^3}\cdot\varphi(\delta_m)\\ &+\frac{1}{2d_2^2c_1d_1k_a}\sum_{n=1}^{\infty}\frac{\sin^2(d_2\lambda_n)}{\lambda_n^3}\cdot\varphi(\lambda_n)\\ &+\frac{1}{c_2^2d_2^2c_1d_1k_a}\sum_{m=1}^{\infty}\sum_{n=1}^{\infty}\frac{\sin^2(c_2\delta_m)\sin^2(d_2\lambda_n)}{\delta_m^2\lambda_n^2\beta_{m,n}}\cdot\varphi(\beta_{m,n}) \end{aligned} \tag{3}$$

Where

$$\lambda_n = n\pi/d_1, \quad \delta_m = m\pi/c_1, \quad \beta_{m,n} = \sqrt{\delta_m^2 + \lambda_n^2} \tag{4}$$

$$\varphi(\zeta) = \frac{(e^{2\zeta t_a}+1)\zeta - (1-e^{2\zeta t_a})h_{e1}/k_a}{(e^{2\zeta t_a}-1)\zeta + (1+e^{2\zeta t_a})h_{e1}/k_a} \tag{5}$$

The thermal resistance between the bottom surface of copper and ambient R_{cm} is given by:

$$R_{cm} = \frac{1}{4hc_2d_2} \tag{6}$$

The thermal resistance between the bottom surface of heat sink and ambient R_{am} is given by:

$$R_{am} = \frac{1}{4h(c_1d_1 - c_2d_2)} \tag{7}$$

The one-dimensional thermal resistance of heat sink R_a is given as

$$R_a = \frac{t_a}{4k_a(c_1d_1 - c_2d_2)} \tag{8}$$

3.1.2 Calculation of R_{sf} and R_{cf}

Generally, solder bumps in chip packaging are arrayed around the copper plate. Since solder bumps are arranged to be close to each other, the areas where solder bumps are bonded on can be simplified to heat source as shaded part s_1 shown in Fig 3.4. The shaded part s_1 in Fig 3.4 is the areas where solder bumps are located on flex cable.

Heat coming from the solder bumps conducts and spreads onto the flex cable, then transfers to the heat sink. The thermal spreading resistance R_{sf} from the areas where the solder bumps are bonded on to the flex cable can be considered as spreading resistance of multiple heat sources [18] and is calculated from the following general expression according to the

notions in Fig 3.4:

$$R_{tf}=\sum_{i=1}^{4}\frac{L_i W_i}{\sum_{i=1}^{4} L_i W_i}(A_0^i+2\sum_{m=1}^{\infty}A_m^i\frac{\cos(\lambda c_1)\sin(\lambda c_3)}{2\lambda c_3}$$
$$+2\sum_{n=1}^{\infty}A_n^i\frac{\cos(\delta d_1)\sin(\delta d_3)}{2\delta d_3}$$
$$+4\sum_{m=1}^{\infty}\sum_{n=1}^{\infty}A_{mn}^i\frac{\cos(\delta d_1)\sin(\delta d_3)\cos(\lambda c_1)\sin(\lambda c_3)}{4\lambda\delta c_3 d_3})$$
$$-(R_{am}+R_a) \quad (9)$$

Where

$$A_0^i=\frac{1}{4c_1d_1}(\frac{t_f}{k_f}+\frac{1}{h_{e2}}) \quad (10)$$

$$A_m^i=\frac{\cos(\lambda x_i)\sin((1/2)\lambda L_i)}{c_1 d_1 L_i k_f \lambda^2 \phi(\lambda)} \quad (11)$$

$$A_n^i=\frac{\cos(\delta y_i)\sin((1/2)\delta W_i)}{c_1 d_1 W_i k_f \delta^2 \phi(\delta)} \quad (12)$$

$$A_{mn}^i=\frac{4\cos(\lambda x_i)\sin((1/2)\lambda L_i)\cos(\delta y_i)\sin((1/2)\delta W_i)}{c_1 d_1 L_i W_i k_f \beta\lambda\delta \phi(\beta)} \quad (13)$$

Where

$\lambda=\frac{m\pi}{2c_1}$, $\delta=\frac{n\pi}{2d_1}$, $\beta=\sqrt{\lambda^2+\delta^2}$, and:

$$\phi(\xi)=\frac{\xi\sinh(\xi t_f)+h_{e2}/k_f\cosh(\xi t_f)}{\xi\cosh(\xi t_f)+h_{e2}/k_f\sinh(\xi t_f)} \quad (14)$$

$$x_1=c_1-\frac{c_4+c_3}{2}, \quad x_2=c_1+\frac{c_4+c_3}{2} \quad (15)$$

$$x_3, x_4 = c_1 \quad (16)$$

$$y_1, y_2 = d_1 \quad (17)$$

$$y_3=d_1-\frac{d_4+d_3}{2},\quad y_4=d_1+\frac{d_4+d_3}{2} \tag{18}$$

$$L_1,L_2=c_3-c_4,\quad W_1,W_2=2d_4 \tag{19}$$

$$L_3,L_4=2c_3,\quad W_3,W_4=d_3-d_4 \tag{20}$$

h_{e2} is the equivalent heat transfer coefficient at the bottom surface of the flex cable and is given as:

$$h_{e2}=\frac{1}{4(R_{am}+R_a)c_1d_1} \tag{21}$$

R_{cf} can be calculated in a similar way as R_{ca}.

3.1.3 Calculation of R_{c1}, R_{c2} and R_s

In the model, a solder bump is assumed to be equivalent to a cube with a side length of 0.1 mm. Thermal resistance of solder bump is given by:

$$R_{sb}=\frac{L}{k_sL^2} \tag{22}$$

Where k_s is the thermal conductivity of solder bump, and L is the side length of cube.

Heat flows through solder bumps in parallel. Therefore, the total thermal resistance of solder bumps is:

$$R_s=\frac{R_{sb}}{N} \tag{23}$$

R_{c2} is one-dimensional conductivity resistance of the copper embedded in aluminum heat sink layer and R_{c1} is resistance of the rest part of the copper. According to the notes of Fig 3.3 and Fig 3.4, R_{c1}, R_{c2} are calculated as follows:

$$R_{c1} = \frac{t_f + L}{4k_c c_2 d_2} \tag{24}$$

$$R_{c2} = \frac{t_a}{4k_c c_2 d_2} \tag{25}$$

Where k_c is the thermal conductivity of the copper.

3.1.4 Calculation of AE chip junction temperature

The total thermal resistance R_{total} between AE chip and ambient is calculated using Matlab according to the resistance network shown in Fig 3.2. The AE chip junction temperature to ambient is defined as:

$$T_m = R_{total} Q + T_a \tag{26}$$

Where Q is the power generated by the AE chip and T_a is the ambient temperature.

3.2 Analysis of mathematical model

To demonstrate the feasibility of the aforementioned model, the AE chip junction temperature is predicted with different copper plate coverage areas by the mathematical model. A solid model with the same dimensions was built using Solidworks to simulate the AE chip junction temperature under the same thermal conditions. The accuracy of the presented model is proven through comparing the simulation data with the predicted ones.

The dimensions and thermal parameters of the system are listed in Table 3.1. Table 3.2 shows the differences between AE chip temperatures calculated by the presented model and the ones obtained by simulations. c_2/c is the ratio of side lengths of copper to AE chip. T_m is

AE chip junction temperature calculated by the presented model and T_s is AE chip temperature obtained by simulation. The error shown in Table 3.2 is defined as:

$$\text{error}=\frac{T_m - T_s}{T_s}\times 100\% \tag{27}$$

It is found that the errors in Table 3.2 are all around 6% and the error decreases as the copper area coverage increases. This trend gives a guide that the copper plate is the key factor which takes significance impact on the AE chip junction temperature to ambient.

3.3 Chapter summary

In this chapter, an analytical thermal resistance network model for predicting the AE chip junction temperature with uniform heat source has been developed. The thermal resistance network was established based on heat dissipation paths from the AE chip to ambient. The proposed model was applied to predict the AE chip junction temperature under the thermal conditions described in Chapter 2. Comparing the data obtained by the presented model and simulation, it is found that the proposed model predicted the AE chip junction temperature in good accuracy. As each resistance in the network has an analytical solution, the proposed model can help find what the key factors influencing the AE chip junction temperature in hard disk drive are. This provides an optimization method to chip packaging design for good thermal management.

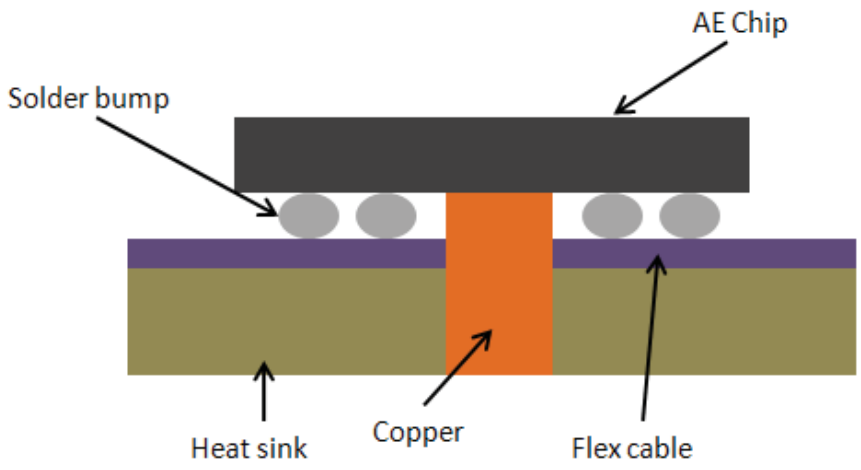


Fig 3.1 - Cross section of a typical chip packaging

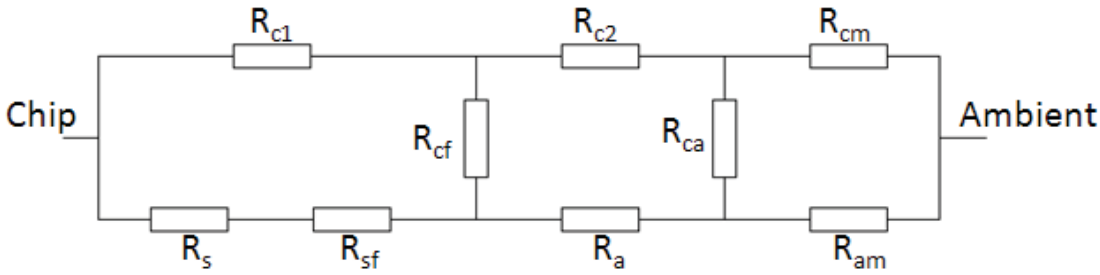


Fig 3.2 - Thermal resistance network of the typical chip packaging

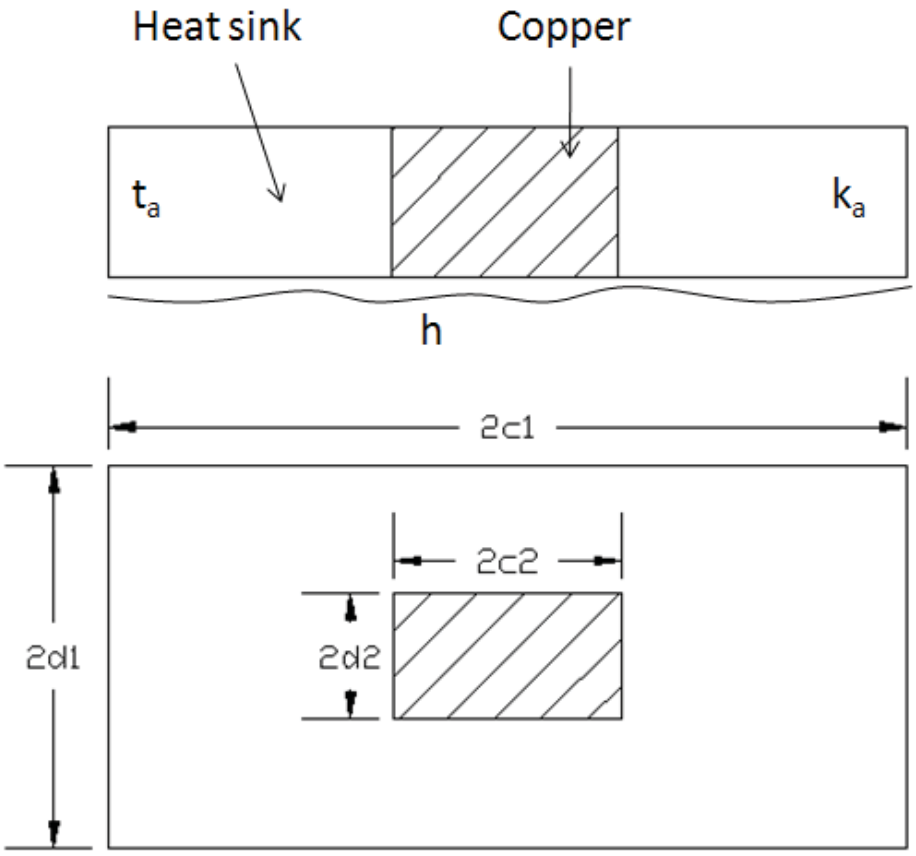


Fig 3.3 - Top figure: section view of heat sink layer,

bottom figure: bottom view of heat sink layer

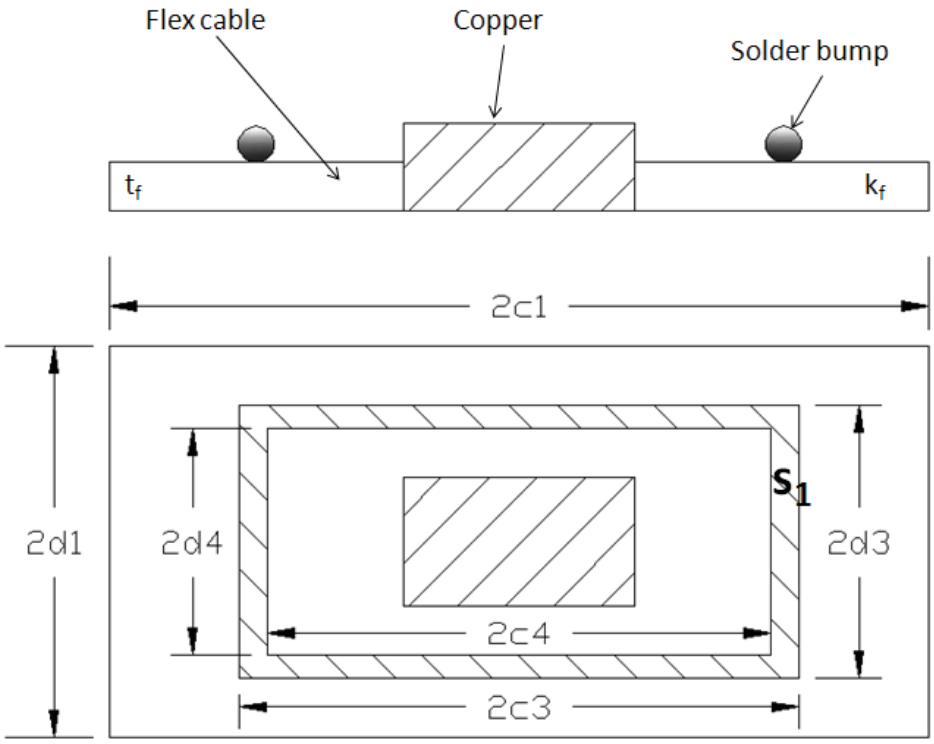


Fig 3.4 – solder bumps and flex cable with copper embedded in,

Top figure: section view, bottom figure: top view

Table 3.1 - Dimensions and thermal parameters of the system

Parameter	Symbol	Value
Solder bumps		
Length (mm)	L	0.1
Bumps number	N	82
Thermal conductivity (W/m K)	k_s	50
AE chip		
Length (mm)	2c	4.6
Width (mm)	2d	4
Flex cable		
Length (mm)	$2c_1$	9.2
Width (mm)	$2d_1$	4.6
Thickness (mm)	t_f	0.05
Thermal conductivity (W/m K)	k_f	0.4
Aluminum heat sink		
Length (mm)	$2c_1$	9.2
Width (mm)	$2d_1$	4.6
Thickness (mm)	t_a	0.3
Thermal conductivity (W/m K)	k_a	209
Copper		
Thickness (mm)	t_c	0.45
Thermal conductivity (W/m K)	k_c	390
Simplified structure - heat source s_1		
Length 1 (mm)	$2c_3$	4.5
Width 1 (mm)	$2d_3$	3.9
Length 2 (mm)	$2c_4$	4.3
Width 2 (mm)	$2d_4$	3.7
Heat transfer coefficient at bottom surface of heat sink (W/m^2 K)	h	1509
Ambient temperature (ºC)	T_a	27
Power of AE chip (W)	Q	2

Table 3.2 - Comparison of data obtained by the present model and simulation

c_2/c	T_m (ºC)	T_s (ºC)	T_m-T_s (ºC)	Error (%)
20%	65.64	70.88	-5.24	-7.39
40%	62.43	66.71	-4.28	-6.42
60%	60.66	64.27	-3.61	-5.62
80%	59.51	62.80	-3.29	-5.24

Chapter 4

Piezoelectricity and its use in micro-thermal energy harvester

4.1 Fundamentals of piezoelectricity

Lead zirconate titanate $PbZr_{1-x}Ti_xO_3$ (PZT) is the piezoelectric material used in this study because of its excellent piezoelectric properties. PZT has the desired perovskite structure ABO_3, shown in Fig 4.1, in cubic, tetragonal, and rhombohedral forms, depending on the temperature and composition. Piezoelectric substance can produce an electric charge when a mechanical stress is applied (the substance is squeezed or stretched). Conversely, a mechanical deformation (the substance shrinks or expands) is produced when an electric field is applied. However, only the non-cubic forms exhibit piezoelectric behavior. To explain this, we have to look at the individual molecules that make up the crystal. Each molecule has a polarization, one end is more negatively charged and the other end is positively charged, and is called a dipole. This is a result of the atoms that make up the molecule and the way the molecules are shaped. The polar axis is an imaginary line that runs through the center of both charges on the molecule. In a monocrystal the polar axes of all of the dipoles lie in one direction. The crystal is said to be symmetrical because if you were to cut the crystal at any point, the resultant polar axes of the two pieces would lie in the same direction as the original. In a polycrystal, there are different regions within the material that have a different polar axis. It is asymmetrical because there is no point at which the crystal could be cut that would leave the two remaining pieces with the same resultant polar axis. Fig 4.2 illustrates this concept. In order to produce the piezoelectric effect, the polycrystal is heated under the application of a strong electric field. The heat allows the molecules to move more freely and the electric field forces all of the dipoles in

the crystal to line up and face in nearly the same direction, shown in Fig 4.3. Those dipoles will remain oriented to some degree when that field is removed.

4.2 Design of micro-thermal energy harvester

Based on the thermal analyses presented in previous sections, a MEMS based, piezoelectric micro-thermal energy harvester similar to the micro heat engine was designed and placed on top of the AE chip. Fig 4.4 shows the configurations of the AE chip thermal energy harvester. The top membrane of the engine is a thin film piezoelectric membrane generator. The cavity surrounded by the membrane generator and the bottom silicon substrate is filled with working liquid or gas. When heat is conducted into this device through the bottom substrate, the working fluid or gas would evaporate or expand, which results in the expansion of the top PZT membrane, converting mechanical energy into electrical energy via strain. When temperature inside HDD decreases as HDD slowing down, the residual heat in the cavity can be removed slowly to ambient and then the membrane restores to its original dimension.

A power supply can be constructed from a single unit-cell engine or an array of many unit-cell engines combined together. This design gives great flexibility in assembling energy conversion devices. Combined in parallel, the unit-cell engines would be driven by the same temperature difference. Combined in series, the unit-cell engines would form a cascade so that each unit-cell engine would be driven by a fraction of the total temperature difference across the entire cascade.

4.3 Fabrication of piezoelectric membrane

A prototype unit-cell micro-thermal energy harvester is fabricated of three components: a silicon membrane with thin film piezoelectric generator, a middle spacer in which there is working fluid and a silicon substrate. The piezoelectric material used in the thin film

membrane generator is lead zirconate titanate (PZT).

The top of a prototype thermal energy harvester consists of a piezoelectric membrane generator. The form of the thin-film piezoelectric membrane generator is a simple two-dimensional sandwich structure similar to that form in MEMS pressure and ultrasonic transducer. Fig 4.5 shows a cross section of the piezoelectric membrane generator, which is composed of a silicon membrane, a bottom platinum electrode, a thin-film of piezoelectric ceramic PZT and a top gold electrode. Piezoelectric membrane is fabricated by first bulk micromachining silicon membranes and then depositing a thin-film generator stack on the membranes. There exist rich literatures about the fabrication of piezoelectric membrane generator [19-22].

The substrate for the piezoelectric membrane generator is a (100) silicon wafer. Basically, the fabrication of piezoelectric membrane involves building a silicon membrane with electrode PZT layers on top. To fabricate silicon membranes, anisotropic wet etching is utilized with a boron etch stop. This approach allows for control of the membrane thickness by accurate control of boron diffusion into one side of the wafer. Oxide layers are grown on both sides of the silicon wafer using wet oxidation at a temperature of 1050 °C. A solution of buffered oxide etch (BOE) is then used to remove the oxide layer from the front side of the substrate. A boron soak was carried out to diffuse high concentrations of boron into the exposed silicon using planar boron disks at a temperature of 1125 °C for 1 hour. This step serves as an etch stop to control the thickness of the silicon membrane. Borosilicate glass that forms on the surface of the boron-doped wafers is then removed using BOE. A subsequent sacrificial low temperature thermal oxide is grown at 850 °C. This oxide layer is removed using BOE, and then a final thermal oxide is grown at 850 °C for 3 hours. The first sacrificial oxide is grown and removed to lower the residual stress induced by the high boron concentration near the surface of the wafer. The oxide layer that finally grows over the entire substrate acts as an insulating layer between the piezoelectric stack and the underlying conductive borondoped silicon layer. The oxide layer also acts as an etch mask during the wet etch process to create the membranes.

Standard photolithography techniques are used to define the square membrane geometry on the backside of the wafer using a negative photoresist. The wafers were then etched with the anisotropic silicon etchant ethylenediamine pyrocatechol (EDP) at 110 °C for 5.5 hours to form square pyramidal cavity in the silicon wafer. The boron etch stop controls resulting membrane thickness. Currently membranes with thicknesses between 1.0 and 3.0 μm are fabricated. Membrane side lengths range from 1.45 to 4.0 mm. Fig 4.6 is a flow chart for the membrane processing [19-20]. The thickness of the membrane could be measured using SEM (Scanning Electron Microscope).

The silicon membranes serve as a substrate on which to fabricate the generator stack shown in Fig 4.5. The bottom electrode consisting of 20 nm adhesion layer of titanium and 180 nm of platinum, which are deposited using an electron beam evaporation to the topside of the wafer. PZT is then spun onto the platinum in a sol–gel process. After each layer of PZT (90 nm per layer) is spun onto the wafer, it is pyrolized at 450 ºC for 2 min. After each third layer of PZT is deposited, the total stack of PZT is crystallized at 700 ºC for 10 min. By building up successive layers of PZT, stacks ranging in thickness from 90 nm to 3 μm can be readily achieved. A top electrode consisting of 5 nm of TiW followed by 325 nm of gold is deposited on the PZT using dc sputtering. Photolithography and a wet etch are used to pattern the top electrodes and PZT. Fig 4.7 illustrates the processing sequence. The generator wafers are then diced into 10mm × 18 mm die, each containing a single membrane generator. In the present thesis, membrane generator with a side length of 2.0 mm and a thickness of 3.9 μm (2.3 μm of silicon and 1.6 mm of PZT) is used.

The bottom of a prototype thermal energy harvester is a silicon substrate which is used as a heat transfer media. The substrate is diced into 10 mm × 18 mm die that is the same dimensions as the piezoelectric membrane generator described previously.

This engine is assembled by sealing a working fluid into a cavity formed between the silicon substrate and piezoelectric membrane generator. A spacer cut from 60 μm thick semiconductor tape is applied to the engine. The spacer, defined as a 10 mm^2 with a 4 mm^2

hole, is placed concentric with the perimeter of the PZT membrane generator. The silicon substrate is then centered below the membrane generator.

4.4 Finite element analysis

In order to analyze the piezoelectric characteristics of PZT membrane generator, finite element analysis was conducted using ANSYS which has the function of piezoelectric simulation. The side length of the laminate is 2 mm, and the mechanical properties of each layer are listed in Table 4.1. The piezoelectric stiffness coefficients matrix, electric permittivity and piezoelectric stress coefficients matrix for PZT layer are listed below:

$$[c] = \begin{bmatrix} 126 & 79.5 & 84.1 & 0 & 0 & 0 \\ 79.5 & 126 & 84.1 & 0 & 0 & 0 \\ 84.1 & 84.1 & 126 & 0 & 0 & 0 \\ 0 & 0 & 0 & 23.0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 23.0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 23.3 \end{bmatrix} \text{ (GPa)} \tag{28}$$

$$[\varepsilon] = \begin{bmatrix} 1.503 & 0 & 0 \\ 0 & 1.503 & 0 \\ 0 & 0 & 1.3 \end{bmatrix} 10^{-8} \text{ (F/m)} \tag{29}$$

$$[e] = \begin{bmatrix} 0 & 0 & 0 & 0 & 17 & 0 \\ 0 & 0 & 0 & 17 & 0 & 0 \\ -6.5 & -6.5 & 23.3 & 0 & 0 & 0 \end{bmatrix}^t \text{ (C/m}^2\text{)} \tag{30}$$

The strain generated in the PZT layer during membrane deflection is an important parameter to the output voltage. In this analysis, two different element types were adopted to characterize different layers in this device. Solid46 element type which is an 8-nodes structural element and has the capability of modeling the layered solid was used to model elastic layers of Pt, Ti, SiO_2 and Si. Using this element type helped modeling of four solid

layers in one element layer. Piezoelectric layer was modeled using Solid5 element type which is an 8-nodes element and has the capability of modeling three-dimensional piezoelectric field. Since the gold layer which is used for electrode is much smaller than other layers, this six-layer laminate was simplified into piezoelectric layer and composites layer for simulation.

Because the thickness of multi-layer diaphragm is much thinner than its other dimensions, a large amount of elements are needed in the laminar plane and the substrate, leading to a huge cost of CPU time, and large requirement on memory and HDD space of computer. Hence, simplified models were employed in the analysis for the purpose of saving CPU [23]. According to the structure characteristics of the device, the center square laminar diaphragm with dimensions of 2 mm × 2 mm was adapted and the surrounding film and substrate were neglected in the model simplification. The square diaphragm was regarded as a laminated plate in the analysis. Clamped boundary condition for four edges is shown in Figure 4.8(a).

The model was meshed using brick sweep method as seen in Fig 4.8(b). The element size was set to give 100 divisions along the sides of the membrane and there was one element through the thickness of each layer, resulting in 20,000 elements. A static pressure-deflection curve for the membrane generator used in the analysis is shown in Fig 4.9. When applying 10 kPa pressure on the membrane, the deformation of the membrane generator is shown in Fig 4.10. The distributions of strain and electrical potentials on the bottom surface of the PZT layer are shown in Fig 4.11 and Fig 4.12, respectively. It could be seen that the maximum electrical potential and strain are near the edge of the PZT membrane. In order to obtain maximum electrical energy, assuming Au electrode is placed at the location as shown in Fig 4.13. Fig 4.14 shows the effect of electrode size on the average voltage, where L is the side length of the membrane, and Le and W are the side length and the side width of the electrode, respectively. It is found that the average voltage decreases as Le and W increase.

To generate more deformation on the PZT membrane, the deflection of the centre line of the laminate was restricted as shown in Fig 4.15. Assuming Au electrode covers the whole surface of the PZT layer, open circuit voltage versus pressure applied to the laminate is shown in Fig 4.16. Type 1 indicates that there is not restriction of deflection on the surface of the laminate. Type 2 and Type 3 indicate that there are constrained displacements on the laminate as shown in (a) and (b) of Fig 4.15, respectively. It is found that more deformation on the PZT membrane can't increase output of electrical energy.

4.5 Chapter summary

This chapter first explained the structure of piezoelectric material and the concept of piezoelectric effect. Then, with thermal managements designed in Chapter 2, a novel micro-thermal energy harvester was described. The engine consists of a thin film piezoelectric membrane generator, a silicon substrate and a cavity filled with working fluid. The thermal energy harvester can convert wasted thermal energy from AE chip into electrical energy and has implications in enhancing AE chip reliability as well as energy conservation. Finally, based on the structure of the thermal energy harvester, a simplified model was built to simulate piezoelectric characteristics of the membrane generator. Through finite element analysis for laminates with a piezoelectric layer, it is found the maximum electrical potential is generated near the edge of the membrane and the relationship between average voltage output and electrode size has also been obtained. With the same electrode coverage, more deformation on the laminate can't increase output of electrical energy.

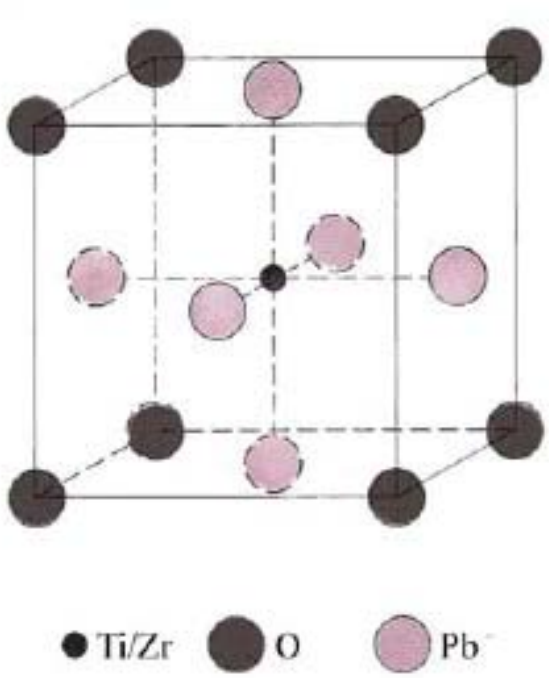
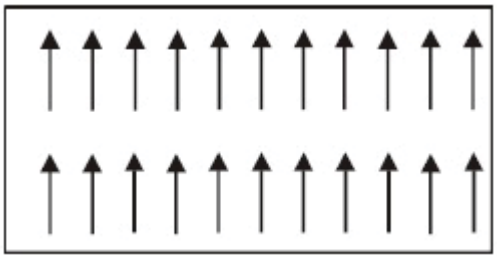
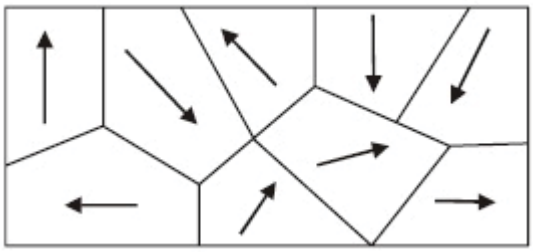


Fig 4.1 - The perovskite crystal structure

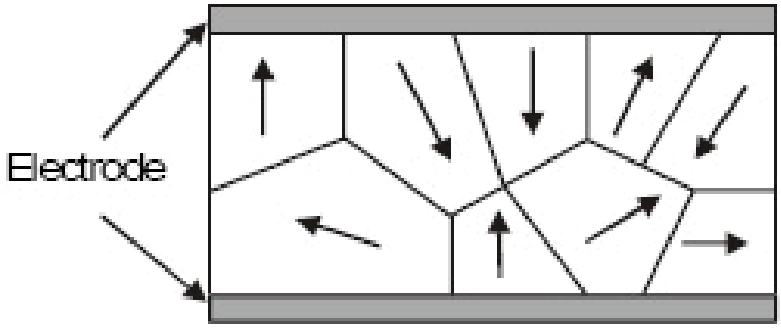


(a) Monocrystal with single polar axis

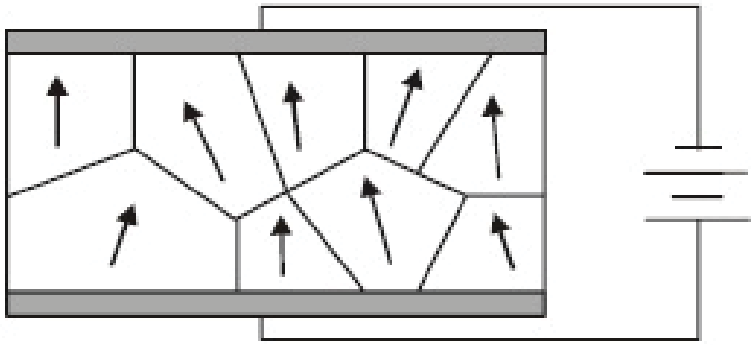


(b) Polycrystal with random polar axis

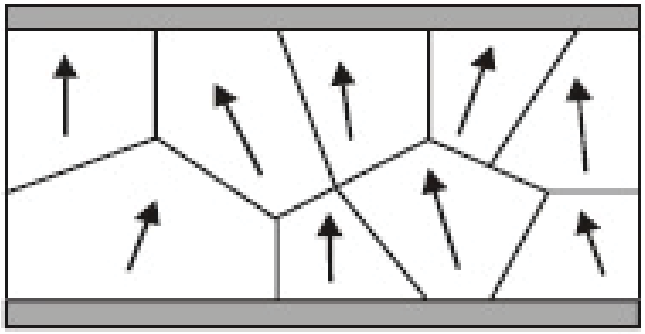
Fig 4.2 - Mono vs Poly Crystals



(a) Random dipole



(b) Polarization



(c) Surviving polarity

Fig 4.3 - Polarization of ceramic material to generate piezoelectric effect

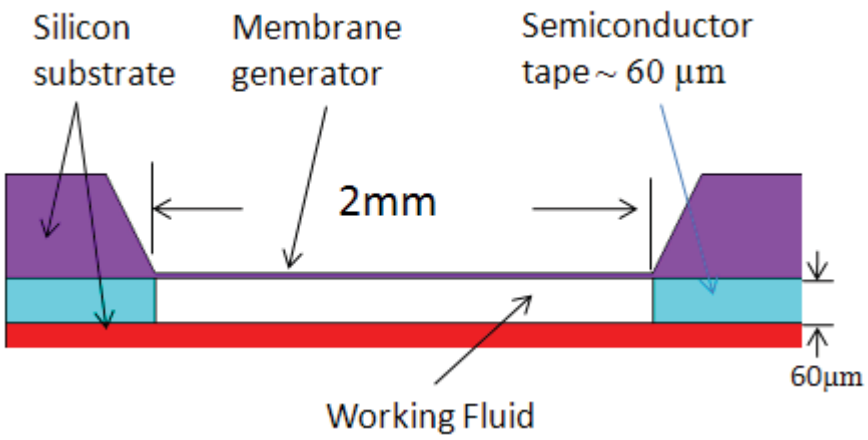


Fig 4.4 - Cross section of thermal energy harvester

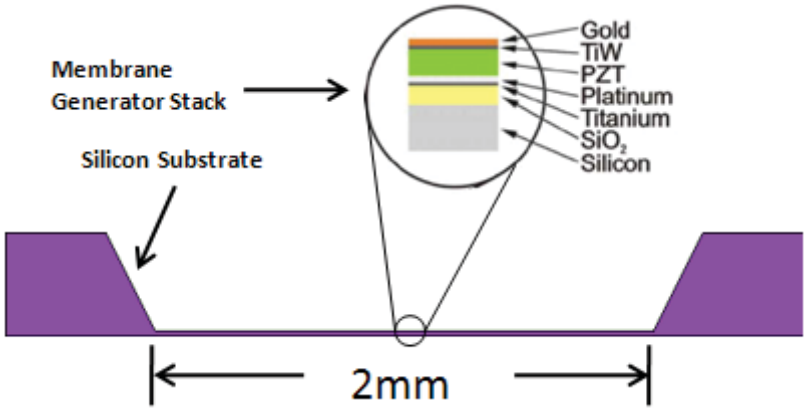


Fig 4.5 - Fabrication of the piezoelectric membrane generator

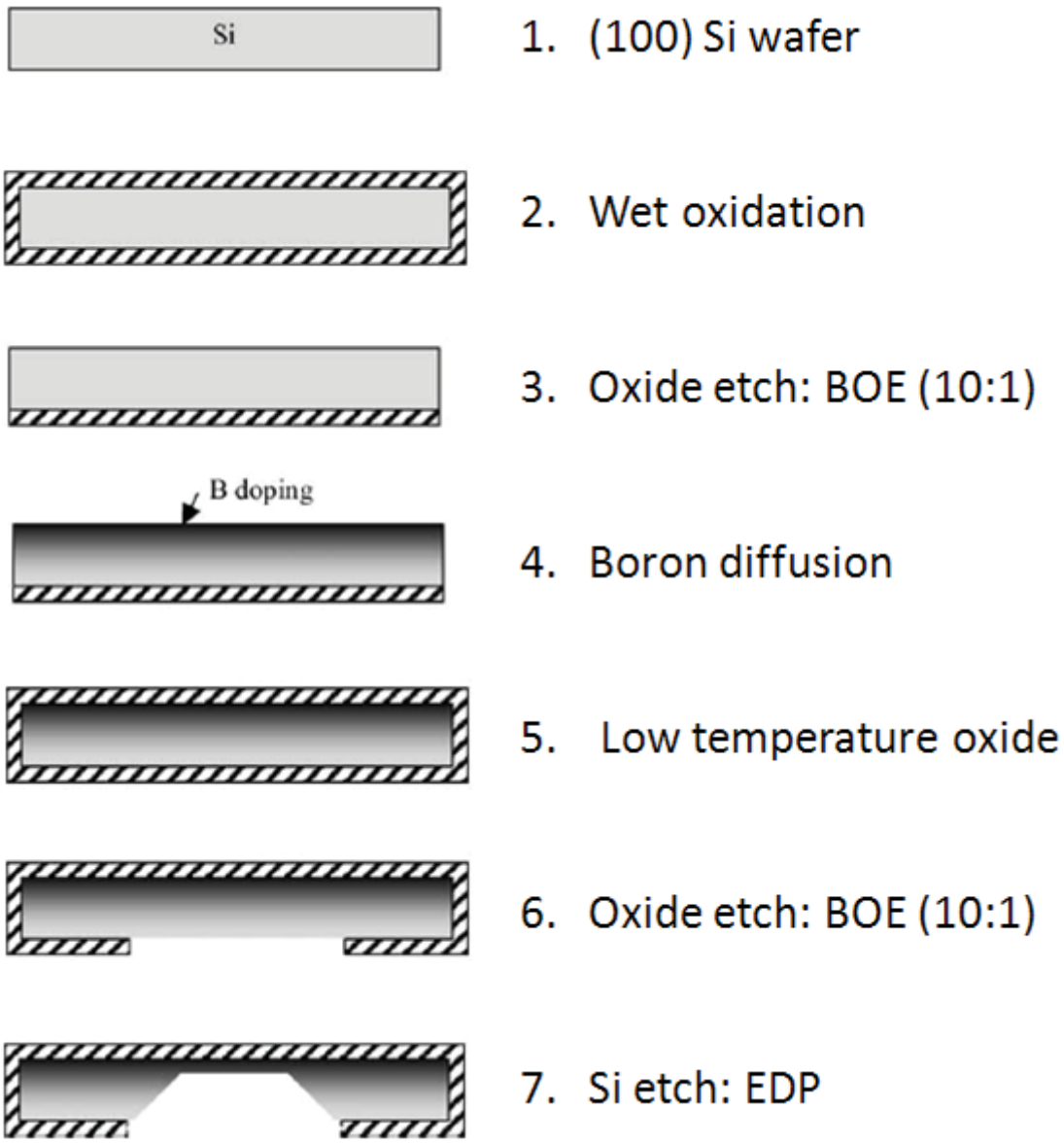


Fig 4.6 - Schematic flow chart of silicon membrane fabrication

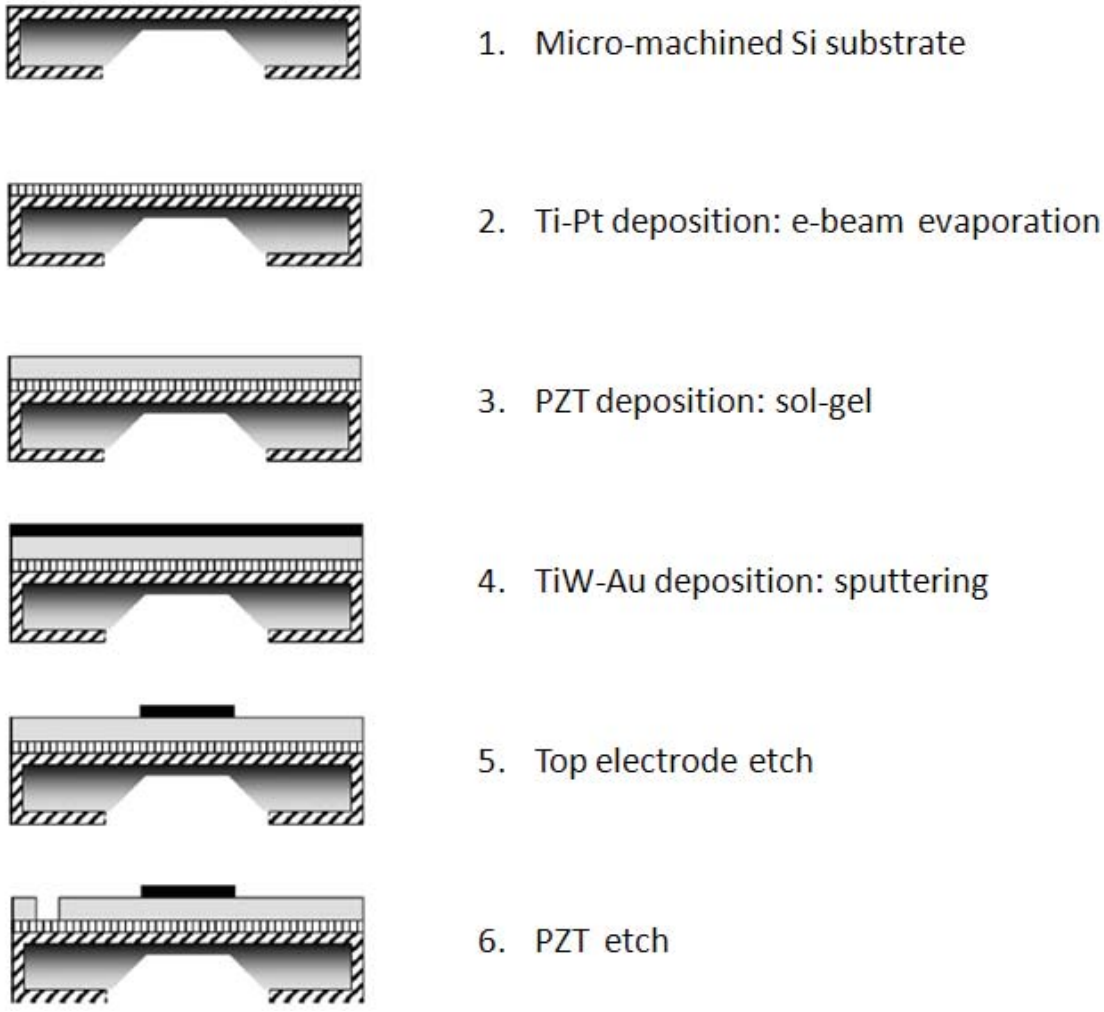
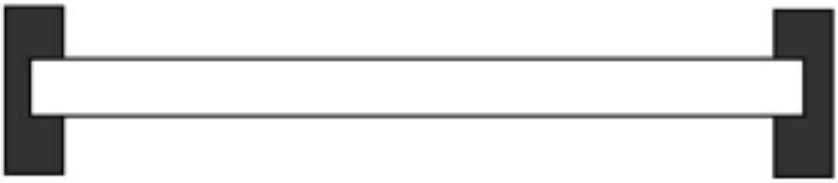
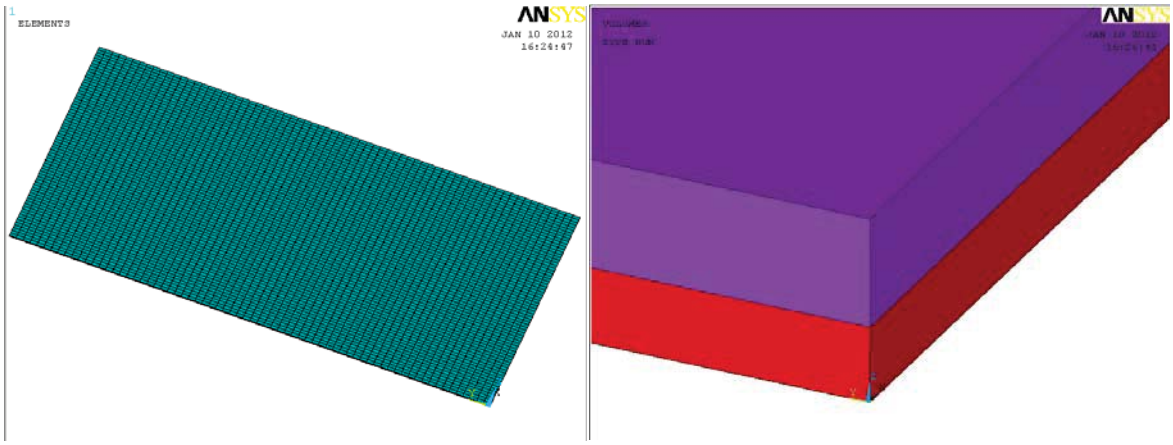


Fig 4.7 - schematic flow chart for the fabrication of the PZT membrane from a micromachined substrate



(a)



(b) (c)

Fig 4.8 – (a) Clamped boundary condition, FEA model of membrane structure (b) complete mesh, (c) close up of membrane structure

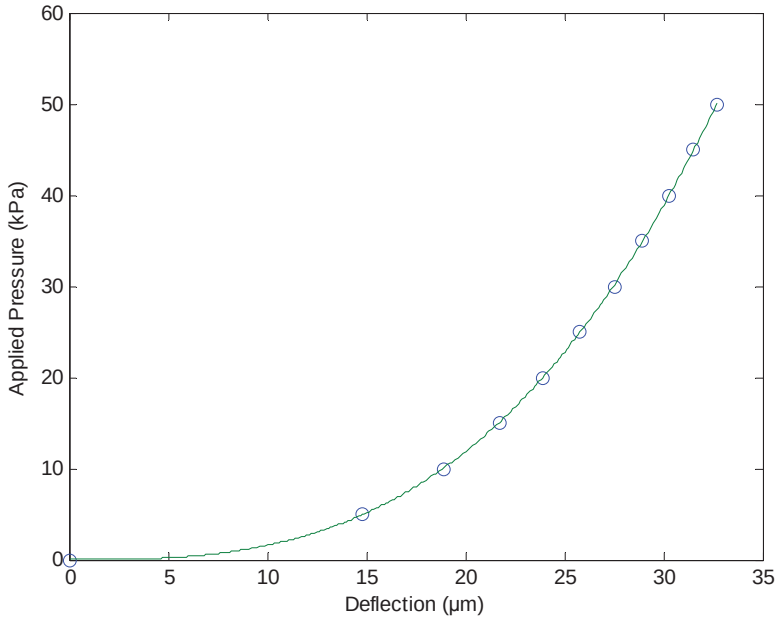


Fig 4.9 - Static pressure-deflection curve for a 2mm membrane generator

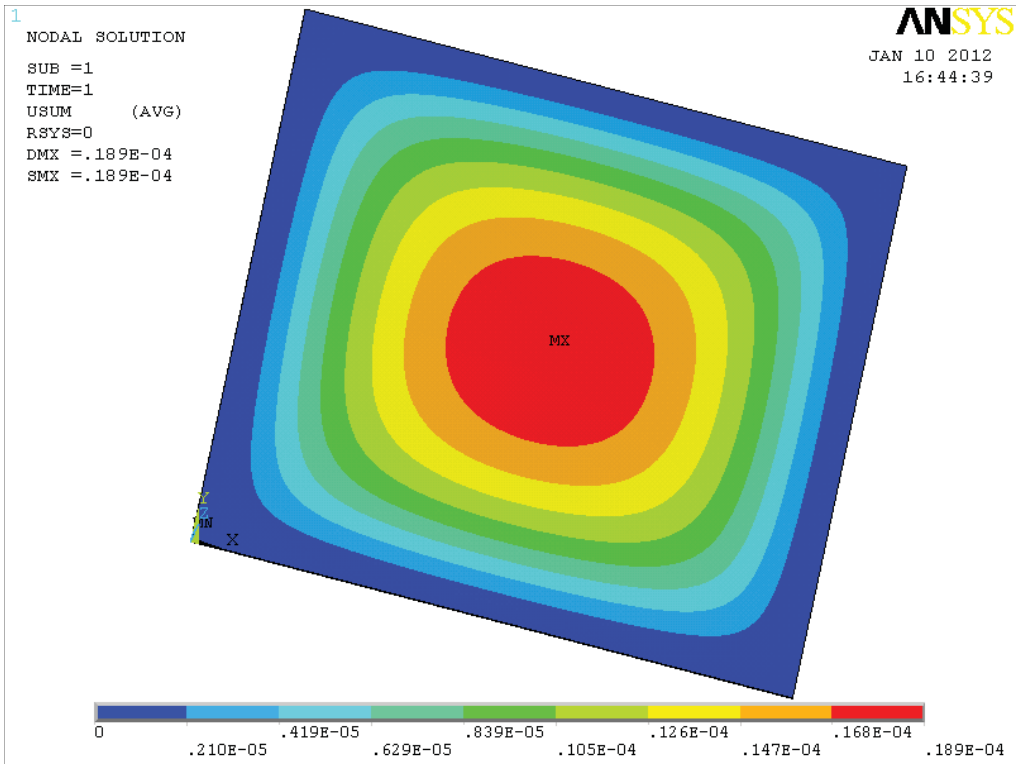


Fig 4.10 - Deformation of the membrane generator

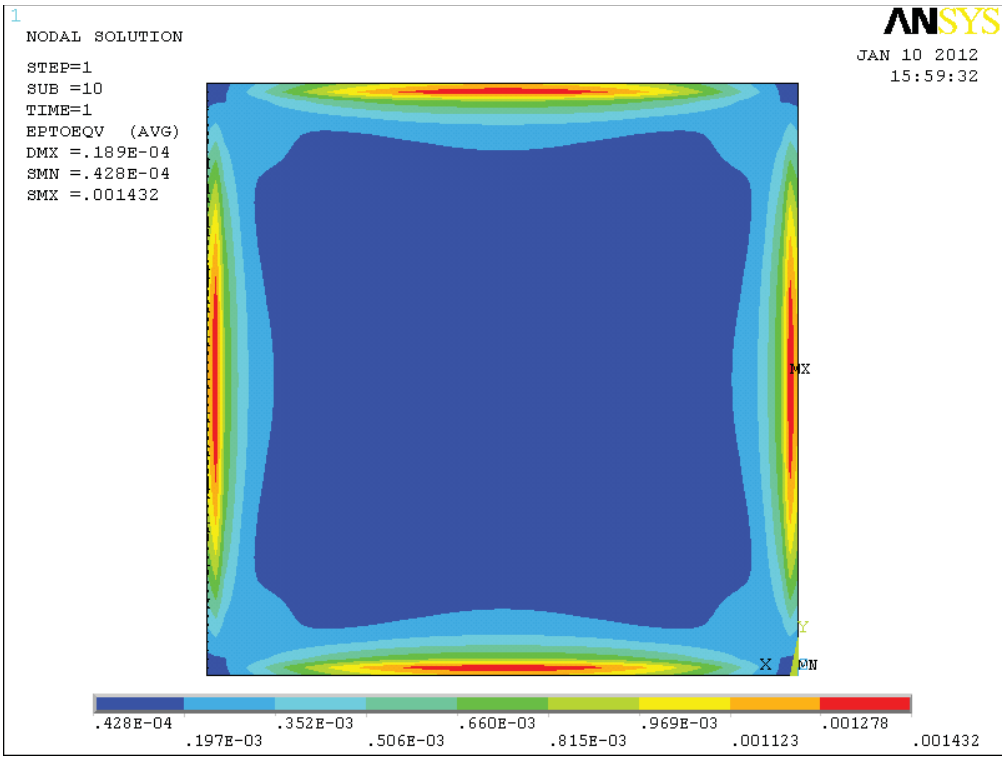


Fig 4.11 - Strain distribution of the PZT membrane surface

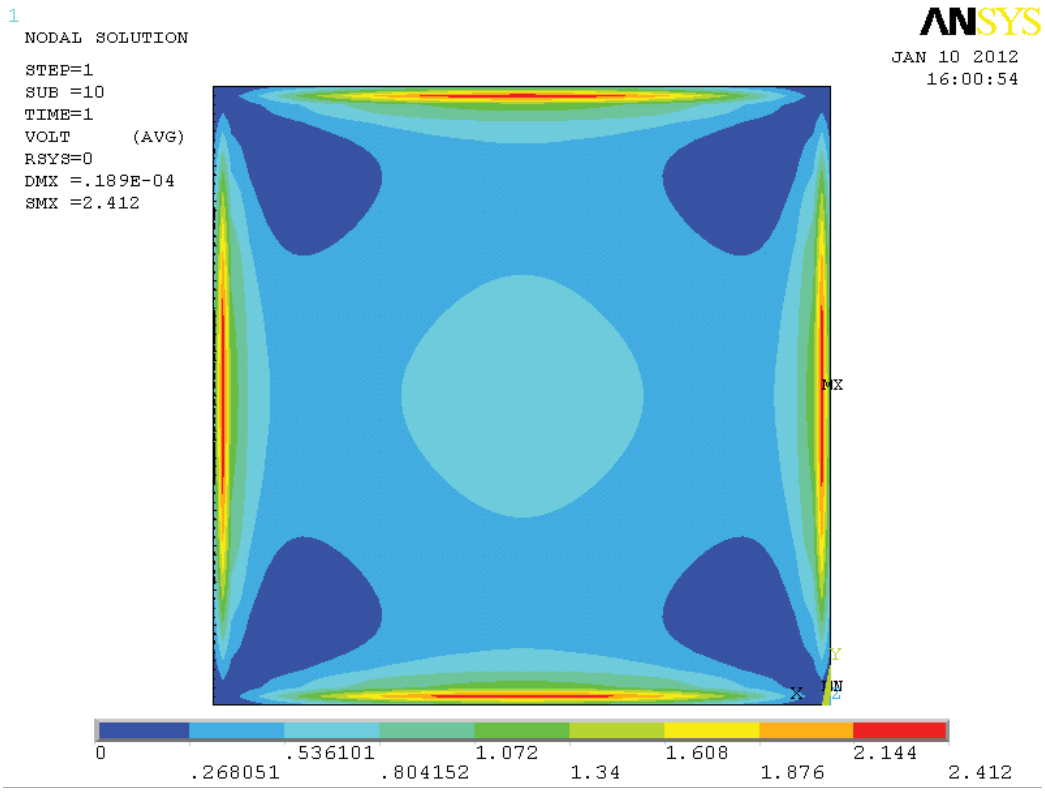


Fig 4.12 - Electrical potential distribution of the PZT membrane surface

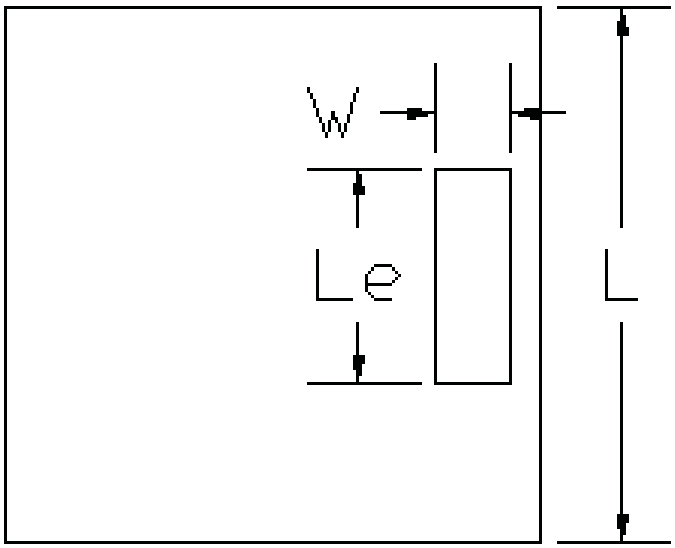


Fig 4.13 - Electrode location

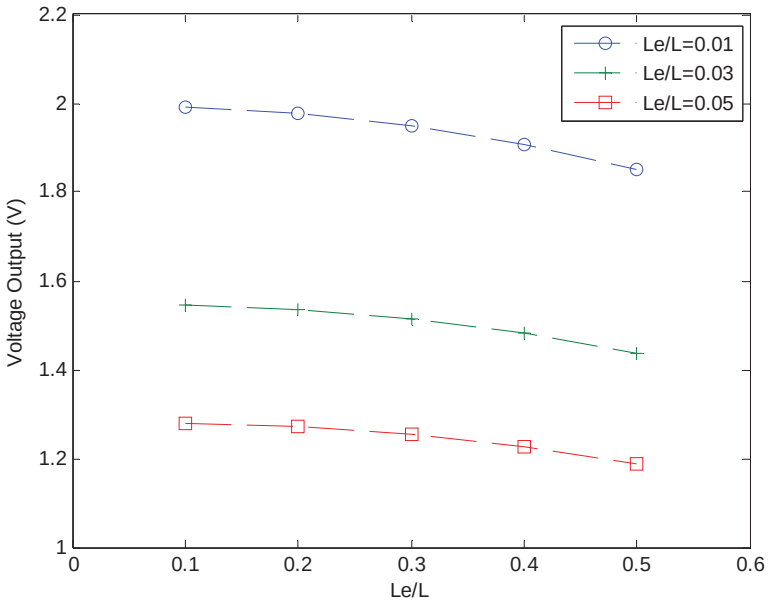
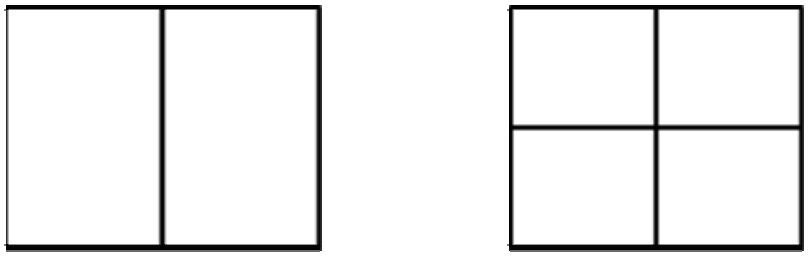


Fig 4.14 - Average voltage versus different electrode sizes



(a) (b)

Fig 4.15 - Laminate

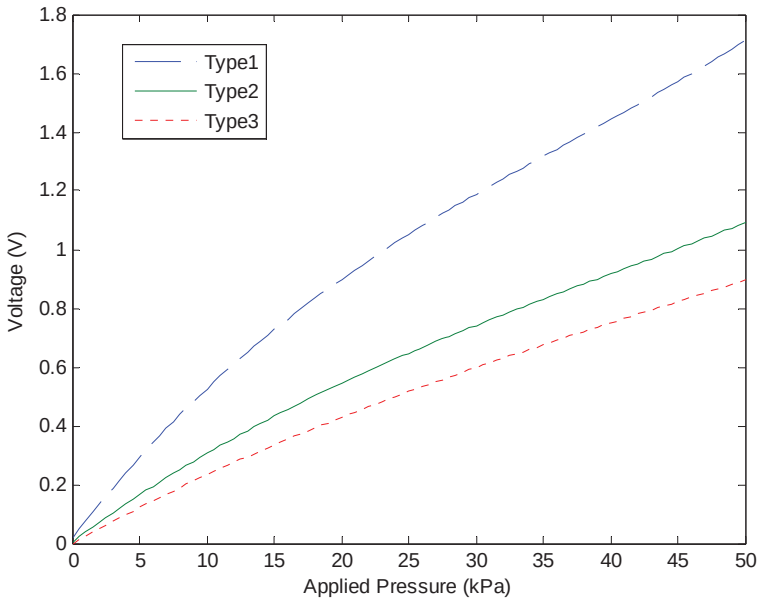


Fig 4.16 - Voltage output as a function of pressure

Table 4.1 - Mechanical properties

Layer	Elastic Modulus, E (GN/m^2)	Poisson Ratio, v	Layer Thickness, t (μm)
Si	160	0.27	2.00
SiO_2	72.1	0.17	0.10
Ti	129	0.32	0.02
Pt	203	0.39	0.18
PZT	74.7	0.25	1.60

Chapter 5

Summary

5.1 Conclusions and contributions

Thermal energy management of AE chip preamp in HDD is important to guarantee reliability of electronic device. Specific conclusions and contributions of this thesis are listed below.

- A new thermal solution for AE chip preamp was discussed using Solidworks software to build solid model. A solid plate-like copper structure is extruded from the aluminum heat sink and is directly contacted with the inner surface of AE chip. The depletion of thermal energy from HDD AE chip was simulated in paper parametric studies of placement and dimension of copper plates as well as location of heat source in the chip. It is found that by concentrating heat source at the centre, thermal resistance decreases as compared to uniform heat source when varying copper area coverage from 20%, 40% to 60%. Because the copper plate is placed underneath the center region of the AE chip, the depletion of thermal energy is not desirable when the heat source is placed at the corner. So, when heat source distribution is non-uniform one needs to customize placement of the copper plate to reach better heat depletion rate.

- An analytical thermal resistance network model for predicting the AE chip junction temperature with uniform heat source has been developed. The thermal resistance network was established based on heat dissipation paths from the AE chip to ambient. The proposed model was applied to predict the AE chip junction temperature under the thermal conditions described in Chapter 2. Comparing the data obtained by the

presented model and simulation, it is found that the proposed model predicted the AE chip junction temperature in good accuracy. As each resistance in the network has an analytical solution, the proposed model can help find what the key factors influencing the AE chip junction temperature in hard disk drive are. This provides an optimization method to chip packaging design for good thermal management.

- With the optimized placement and design of copper plate, a novel PZT-based energy harvester was proposed to convert wasted thermal energy from AE chip into electrical energy. This engine has implications in enhancing AE chip reliability as well as energy conservation. Based on the structure of the thermal energy harvester, a simplified model was built to simulate piezoelectric characteristics of the membrane generator. Through finite element analysis for the membrane generator with a piezoelectric layer, it is found that the maximum electrical potential is generated near the edge of the membrane, and location and dimension of electrode can influence voltage output. With the same electrode area coverage, more deformation on the laminate can't increase voltage output.

5.2 Future work

In this thesis, the thermal analysis of AE chip junction temperature with several thermal management configurations was studied using finite element software. Experimental setup could be built to measure the temperature of AE chip under the same thermal managements as the model in Chapter 2. The accuracy of the presented model can be proven by comparing the experimental data with the simulation ones. Due to the shortage of experimental equipments, the PZT-based energy harvester has not been fabricated. This engine could also be fabricated to study the effectiveness of converting wasted thermal energy from AE chip into electrical energy in future work.

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Appendix A

The finite element analysis in Chapter 4 was simulated using Ansys software and the GUI codes are shown below:

```
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/TITLE, PIEZOELECTRIC

/NOPR
/PMETH,OFF,1
KEYW,PR_SET,1
KEYW,PR_STRUC,1
KEYW,PR_ELMAG,1
KEYW,MAGELC,1
/COM,
/COM,    Structural
/COM,    Electric

/PREP7
ET,1,SOLID5                          ! 3-D coupled-field brick, piezo option
KEYOPT,1,1,3
KEYOPT,1,3,0
KEYOPT,1,5,0
ET,2,SOLID46
KEYOPT,2,2,0
KEYOPT,2,2,0
KEYOPT,2,1,0
KEYOPT,2,3,0
KEYOPT,2,4,0
KEYOPT,2,5,0
KEYOPT,2,6,0
KEYOPT,2,8,1
KEYOPT,2,9,0
KEYOPT,2,10,0

TB,ANEL,1,1,21,0                     ! Anisotropic elastic stiffness, N/m^2
TBTEMP,0
TBDATA,,1.26e11,7.95e10,8.41e10,0,0,0
TBDATA,,1.26e11,8.41e10,0,0,0,1.26e11
TBDATA,,0,0,0,2.3e10,0,0
TBDATA,,2.3e10,0,2.33e10,,,
```

```
TB,PIEZ,1,,,1                          ! Piezoelectric stress coefficients, C/m^2
TBMODIF,1,1,0
TBMODIF,1,2,0
TBMODIF,1,3,-2.3652e-10
TBMODIF,2,1,0
TBMODIF,2,2,0
TBMODIF,2,3,-2.3652e-10
TBMODIF,3,1,0
TBMODIF,3,2,0
TBMODIF,3,3,5.0066e-10
TBMODIF,4,1,0
TBMODIF,4,2,0
TBMODIF,4,3,0
TBMODIF,5,1,0
TBMODIF,5,2,7.3913e-10
TBMODIF,5,3,0
TBMODIF,6,1,7.3913e-10
TBMODIF,6,2,0
TBMODIF,6,3,0
MPTEMP,,,,,,,,
MPTEMP,1,0                             ! Electric permittivity, F/m
MPDATA,PERX,1,,1.503e-8
MPDATA,PERY,1,,1.503e-8
MPDATA,PERZ,1,,1.3e-8
MPTEMP,,,,,,,,
MPTEMP,1,0
MPDATA,EX,2,,203e9                     ! Young's modulus, N/m^2
MPDATA,PRXY,2,,0.39                    ! Poisson's ratio
MPTEMP,,,,,,,,
MPTEMP,1,0
MPDATA,EX,3,,129e9
MPDATA,PRXY,3,,0.32
MPTEMP,,,,,,,,
MPTEMP,1,0
MPDATA,EX,4,,72.1e9
MPDATA,PRXY,4,,0.17
MPTEMP,,,,,,,,
MPTEMP,1,0
MPDATA,EX,5,,160e9
MPDATA,PRXY,5,,0.27

*SET,_RC_SET,1,                       ! Real constants
R,1
RMODIF,1,1,4,0,0,0
```

```
RMODIF,1,7,0
RMODIF,1,13,2,0,0.18e-6,3,0,0.02e-6,
RMODIF,1,19,4,0,0.1e-6,5,0,2e-6,

BLOCK,0,0.002,0,0.002,0,1.6e-6,                ! Define volume
BLOCK,0,0.002,0,0.002,1.6e-6,3.9e-006,
FLST,2,2,6,ORDE,2
FITEM,2,1
FITEM,2,-2
VGLUE,P51X
CM,_Y,VOLU
VSEL, , , ,          1                         ! Set element attributes
CM,_Y1,VOLU
CMSEL,S,_Y
CMSEL,S,_Y1
VATT,          1,          1,     1,          0
CMSEL,S,_Y
CMDELE,_Y
CMDELE,_Y1
CM,_Y,VOLU
VSEL, , , ,          3                         ! Set element attributes
CM,_Y1,VOLU
CMSEL,S,_Y
CMSEL,S,_Y1
VATT,          5,          1,     2,          0
CMSEL,S,_Y
CMDELE,_Y
CMDELE,_Y1

/PNUM,LINE,1
FLST,5,12,4,ORDE,4
FITEM,5,1
FITEM,5,-8
FITEM,5,17
FITEM,5,-20
CM,_Y,LINE
LSEL, , , ,P51X
CM,_Y1,LINE
CMSEL,,_Y
LESIZE,_Y1, , ,100, , , , ,1                   ! Define the number of element divisions
ESIZE,0.001,0,
FLST,5,2,6,ORDE,2
FITEM,5,1
FITEM,5,3
```

```
CM,_Y,VOLU                              ! Generate nodes and elements
VSEL, , , ,P51X
CM,_Y1,VOLU
CHKMSH,'VOLU'
CMSEL,S,_Y
VSWEEP,_Y1
CMDELE,_Y
CMDELE,_Y1
CMDELE,_Y2
VPLOT
/PNUM,AREA,1
/REPLOT
FINISH

/SOL
ANTYPE,0                                ! Static analysis
NLGEOM,1
NSUBST,10,11,0
TIME,1                                  ! Analysis time, s
FLST,2,8,5,ORDE,4
FITEM,2,3
FITEM,2,-6
FITEM,2,13
FITEM,2,-16
DA,P51X,UX,0
FLST,2,8,5,ORDE,4
FITEM,2,3
FITEM,2,-6
FITEM,2,13
FITEM,2,-16
DA,P51X,UY,0
FLST,2,8,5,ORDE,4
FITEM,2,3
FITEM,2,-6
FITEM,2,13
FITEM,2,-16
DA,P51X,UZ,0
FLST,2,1,5,ORDE,1
FITEM,2,1
SFA,P51X,1,PRES,10000
FLST,2,1,5,ORDE,1
FITEM,2,2
DA,P51X,VOLT,0                          ! Define bottom electrode
NLGEOM,1
```

```
NROPT,FULL, ,OFF
SSTIF,ON
TINTP,,0.25,0.5,0.5                ! Set time integration parameters piezo
ALLSEL,ALL                         analysis
/STATUS,SOLU
SOLVE
FINISH
```