# Novel $g_m$-boosted High Gain Transimpedance Amplifiers for Biomedical and Sensor Applications in 180nm CMOS Technology

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# Abstract

This research work introduces five novel $g_m$ -boosted transimpedance amplifiers (TIAs), which are (1) a $g_m$-boosted common-source with source-degeneration as a TIA, (2) a $g_m$-boosted inverter cascode TIA ($g_m$-boosted Inv-Cas TIA) using quasi-floating gate (QFG), (3) a $g_m$-boosted folded regulated cascode TIA ($g_m$-boosted RIC TIA) using QFG, (4) a $g_m$-boosted doubly folded push-pull TIA and (5) a $g_m$-boosted multiple-stage inductively peaked TIA. The transimpedance gain analysis is discussed for all the proposed TIAs. And the input referred noise power current spectral density of the last four topologies have been developed mathematically in this thesis. To demonstrate actual performance enhancement achieved circuit simulation results are also provided as verification. Each TIA is simulated with a 5 pF photodiode (PD) input capacitance and a 500 fF output capacitance. The simulation analysis consists of (1) a transient response of output voltage, (2) a transimpedance gain, (3) a -3 dB bandwidth, (4) an input referred noise current power spectral density, and (5) an eye diagram simulation using a $2^{31}$-1 pseudo random bit sequence (PRBS) data pattern as an input. A test chip implementing the $g_m$-boosted Inv-Cas TIA, $g_m$-boosted RIC TIA, and $g_m$-boosted multiple-stage inductively peaked TIA was fabricated using a 180nm CMOS process. Also, the microchip was tested by using a fabricated PCB and giving sinusoidal and square wave inputs. Finally, a detailed discussion is given on the experimental results section.

# Acknowledgements

First of all, I would like to express my deep and sincere appreciation to my research supervisor Associate Professor Rezaul Hasan for giving me the opportunity to conduct the research and providing insightful feedback during the planning and development of this research work. Without his enthusiastic encouragement, constructive suggestions and endless support, this work would not have been possible.

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# List of Abbreviations

| | |
|---|---|
| AC | Alternating Current |
| CMOS | Complementary Metal Oxide Semiconductor |
| DC | Direct Current |
| DIP | Dual In-line Package |
| DRC | Design Rule Check |
| FD - NIRS | Frequency domain - Near - Infrared Spectroscopy |
| IC | Integrated Circuit |
| LVS | Layout Versus Schematic |
| LIA | Lock-in Amplifier |
| DAQ | Data Acquisition Board |
| MEMS | Micro Electro Mechanical Systems |
| MOSFET | Metal - oxide - semiconductor Field-effect Transistor |
| NIRS | Near-Infrared Spectroscopy |
| NMOS | N-Type Metal - Oxide - Semiconductor |
| NMR | Nuclear Magnetic Resonance |
| OCT | Optical Coherence Tomography |
| PCB | Printed Circuit Board |
| PEX | Practices Extraction |
| PD | Photodiode |
| PMOS | P - Type Metal - Oxide - Semiconductor |
| PPG | Photoplethysmogram |
| PRBS | Pseudo Random Bit Sequence |
| QFG | Quasi-floating Gate |

| | |
|---|---|
| TIA | Transimpedance Amplifier |

# Chapter 1 Introduction

This chapter presents a brief review of modern CMOS transimpedance amplifiers (TIAs) including its definition, challenges, and expectations in different fields of TIA applications. This work's motivations and objectives, contributions to knowledge, and thesis outline are also discussed in this chapter.

## 1.1 Thesis Content

A transimpedance amplifier (TIA) is defined as a type of measurement device that senses a very weak current input signal and converts it to a measurable output voltage as a usable signal [1]. When current flows through a resistor, it also produces a voltage difference across the resistor. According to Ohms' Law, the value of voltage drop is proportional to current and resistance value. In other words, a resistor itself can be seen as a simple passive current to voltage converter. Ideally, suppose the input current does not change; as the resistor's value increases, the value of voltage across the resistor increases as well. However, this passive current to voltage converter would not work when the input current source is not ideal. As shown in Fig. 1.1, replacing the input current source with its Thevenin's equivalent voltage source with a series resistor $R_{in}$, causes the resistors $R_{in}$ and $R_{out}$ to be connected in series. Consequently, the voltage $v_{out}$ will be reduced if the current source is not ideal.

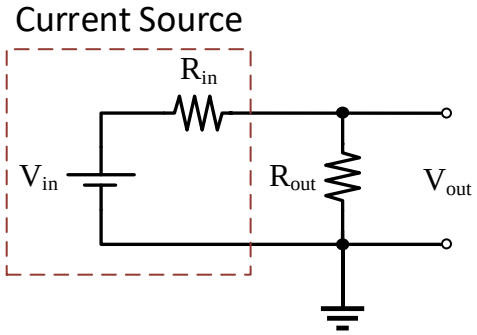



Fig. 1.1 Transformation from Norton current source to Thevenin voltage source.

On the other hand, a photodiode always contains unwanted capacitance as shown in Fig. 1.2. A time constant τ is proportional to the value of resistor $R$ and capacitor $C$ shown in equation (1.01). When the resistor's value increases, the transimpedance gain is high, but the time constant increases as well.

$$\tau = RC \tag{1.01}$$

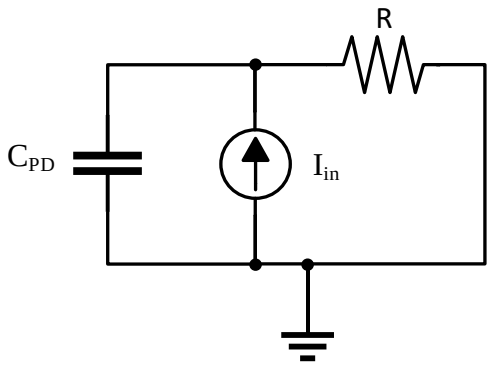



Fig. 1.2 Equivalent circuit of a photodiode.

All these factors impact the efficiency and accuracy of current to voltage conversion. Hence, TIA is considered to balance these imperfections. Historically, TIA design is a major area of interests within the field of photo-sensing-related functions such as optical receivers [2]. Over the past decades, most research in advanced TIAs shows the rapid development of their implementations in a wide range, such as biomedical sensor detectors for particles and radiation, miniaturised spectrometers for nuclear magnetic resonance (NMR), as well as inertial sensors such as Micro Electro Mechanical Systems (MEMS) accelerometers and gyroscopes [3],[4]. For different applications, their focusing parameters are different. The primary issue in biological sensors concerns high gain, low noise, and low power consumption with a small chip area due to the very weak detected biological signals [5]-[8]. However, the speed of signal processing for biomedical applications is not essential; it can be operated at significantly low frequencies. Taking a photoplethysmogram (PPG) blood pressure sensor for example, the average bandwidth is 5 kHz [9]. By contrast, wide bandwidth plays a critical role in optical communication systems which could be enhanced to multiple GHz range [3][10]. Therefore, it is necessary to clarify the constraints and requirements of different applications. The type of particular implementation is the dominant feature of choosing suitable TIA topologies and configuring the trade-off between parameters such as transimpedance gain, input referred noise, power consumption, and stability [3],[11].

## 1.2 Applications

Recent developments in healthcare fields have heightened the need for different CMOS-based biomedical devices such as blood pressure measuring devices using PPG, Optical Coherence Tomography (OCT), and functional Near-infrared Spectroscopy (NIRS) [12]. A large and

growing body of literature has recognised the importance of optoelectronics integrated circuit design. The working principle of the devices mentioned above is similar. In brief, a signal is emitted to human tissues and the reflected signal is detected by a photodiode that converts the optical power into an electrical current. Then the electrical current is converted to a voltage by TIA. Typically, it is followed by a post-amplifier and an output buffer in the biomedical devices.

### 1.21 Blood Pressure Measuring Devices

Hypertension (high blood pressure) is a major risk for heart attack, stroke, kidney disease and others without any symptoms. 7.6 million people have died of high blood pressure worldwide per year without any symptoms, about 13.5% of the total [13]. Measuring blood pressure routinely is an effective way to prevent and control hypertension. Recent studies suggest that measuring blood pressure at home routinely is necessary to prevent patients from serious organ damage by providing more accurate data [14]. As a low-cost and no supervision-required device, a PPG sensor is widely used in wearable blood pressure measurement devices [15]-[19]. Fig. 1.3 shows a block structure of a cuffless blood pressure device using a PPG sensor containing an LED and a photodiode receiver to detect the blood pressure wave traveling through the arteries [20]. The LEDs contact human skin and emit lights as a light source. Then the lights shine through human skin, bones, venous blood, and other tissues. PPG receiver collects the weak optical signal from reflected lights by a large-area photodiode indicating the blood volume and heart rate based on the fundamental frequency [21]. The PPG signal consists of AC and DC components. Only the AC component is synchronized with the heartbeat related to the blood pulsatile in the artery [22]. Thus, a high gain and low noise TIA has followed by the photodiode to convert and amplify the weak photocurrent to a strong electrical voltage [23] as well as to reject the DC photocurrent [24][25]. Usually, the photocurrent varies from a few nA to several uA [23], [16]. TIA plays a critical role in the PPG receiver sensors because it decides the receiver's sensitivity and bandwidth. The major bottleneck of TIA is caused by the large-area photodiode which creates a high parasitic capacitance. And the parasitic capacitance limits the gain, bandwidth, noise performance and power consumption [23].

Fig. 1.3 A block structure of an optical PPG blood pressure measurement [16].

### 1.22 Optical Coherence Tomography

Optical coherence tomography (OCT) is a non-invasive micrometre-scale cross-sectional imaging technology in biomedical systems that generates a false colour of live biological tissues in real-time to measure the thickness [26]-[29]. OCT applications have widely been used in many different biomedical fields such as Ophthalmology, Dermatology, Gastroenterology, Dentistry, Cardiology, Urology and etc [30]-[33]. Fig. 1.4 shows a block diagram of an OCT system. Firstly, a fiber coupler divides the light from a light source into the reference arm and sample arm. Then the reflected lights from the reference mirror and sample are combined by the fiber coupler. The combined lights are then detected by the on-chip photodiode that converts optical power into photocurrent. Finally, a voltage signal that TIA converts is demodulated and sampled by a lock-in amplifier (LIA) and data acquisition board (DAQ), then the signal is displayed on the screen [33].

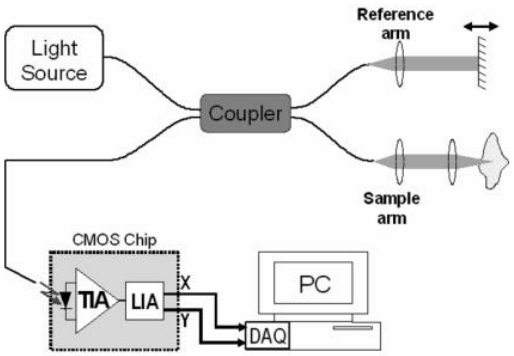



Fig. 1.4 A block diagram of an OCT system [33].

### 1.23 Near-Infrared Spectroscopy

Near-infrared spectroscopy (NIRS) is another example of optoelectronics integrated circuit design for biomedical and sensor applications. It relies on multiple near-infrared wavelengths from 650nm to 950nm in tissues to the physiological properties of the brain, such as hemoglobin, oxy-hemoglobin and cytochrome c-oxidase [34]-[36]. Fig. 1.5 shows a block diagram of an FD-NIRS (frequency domain) system. A signal is generated by the sinusoidal source to the laser driver. The laser driver then emits a NIR light signal through the skull and the optical receiver detects and amplifies the reflected weak light signal [37].

NIRS is essential for a wide range of biomedical applications such as imaging brain function [38][39], prediction of epilepsy seizure [40], muscle metabolism assessment for chronic obstructive lung disease [41], [42] and identification of vulnerable periods for neurological injury during paediatric cardiac surgery [43]. The most crucial feature of NIRS is that it is no harm to humans and people can be exposed to it for a long time [44]. Research shows that the maximum reflected optical power from tissues is one microwatt [45]. Therefore, high sensitivity is required for NIRS devices and the optical receiver front end. Also, the system is expected to be a small chip area, low power consumption and optical power for safety reasons [37].

Fig. 1.5 A block diagram of an FD-NIRS system [37].

## 1.3 Thesis Objective

This research was undertaken to design integrated CMOS high gain TIAs and evaluate their performances. The objectives involved in this thesis are:

1. Review relevant existing literatures on biomedical and sensor applications, and identify the expectations of TIAs for these applications. Analyse the shortage or lack of previous research and recognise the potential improvement and development.
2. Referring to knowledge and information from objective one, explore and develop advanced methodologies for circuit design.
3. Run several simulations on proposed integrated circuits to achieve the targets using a 180nm standard CMOS technology with 1.8V DC supply voltage. Create layout masks, then test the performance by extracting the netlist underlying the layout in DRC, LVS and PEX simulations.
4. Evaluate the performance of each design and compare them with published designs. Acknowledge the limitation and make recommendations for further research work.

## 1.4 Contributions to Knowledge

This thesis contributes in many ways to the understanding of $g_m$-boosted high gain, low noise and low power consumption TIAs for biomedical and sensor applications. The essential contributions to knowledge can be illustrated by:

1. Discussing the complete small-signal mid-band operation of a novel $g_m$-boosted common-source with source-degeneration and its configuration as a TIA.
2. Presenting three novel design methodologies for high-gain, low-power and low noise $g_m$-boosted TIAs consisting of modified $g_m$-boosted Inverter cascode TIA, $g_m$-boosted folded regulated Inverter cascode TIA, and $g_m$-boosted doubly folded push-pull TIA.
3. Developing a novel methodology for single-ended to differential conversion.
4. Investigating and analysing a design of bandwidth extension for $g_m$-boosted voltage-current feedback TIA.
5. Enhancing the ability to derive the mid-band gain and input referred noise mathematically.
6. Comparison among the proposed TIAs and providing suggestions on their performance and applications.

## 1.5 Thesis Outline

The structure of the thesis takes the form of nine chapters. Chapter two discusses the $g_m$-boosted common-source with source degeneration and its configuration as a transimpedance amplifier. Chapter 3-6 present (1) $g_m$-boosted Inv-Cas TIA, (2) $g_m$-boosted RIC TIA, (3) $g_m$-boosted doubly folded push-pull TIA and (4) $g_m$-boosting multiple-stage inductively peaked TIA including their mathematical analysis, simulation results, and layout designs. Chapter seven illustrates the performance of each TIA and provides their comparisons. Chapter eight lists and analyses the experimental results of the fabricated microchip. Finally, chapter nine concludes the overview finding of the thesis and the limitations of the current study.

# Chapter 2 $g_m$-boosted Common Source with Source Degeneration as a Transimpedance Amplifier

The common-source with source-degeneration is well known in analog CMOS integrated circuits and is discussed in detail in text-books [46]-[50] and other avenues. It is implemented in numerous building blocks for signal conditioning and for boosting the output-impedance of analog circuits. Improvement of its intrinsic-gain and output-impedance can further enhance the performance of such analog building blocks. In this context, the implementation and comprehensive small-signal mid-band characteristics of a $g_m$-boosted common-source amplifier with source-degeneration is investigated in this work. The full circuit analysis of a $g_m$-boosted common-source amplifier with source-degeneration or its trans-impedance amplifier derivative has not been reported before. A basic $g_m$-boosted common-source with source-degeneration was introduced in [47] but without comprehensive small-signal analysis. The $g_m$-boosting technique has been employed in many analog building blocks such as transconductance-amplifiers [51], transimpedance-amplifiers [52], RF-frontend LNA [53], RF mixers [54], sensor instrumentation amplifier [55] and so forth. In several recent articles, *using a simplified inspection technique* [56] the second author reported many CMOS $g_m$-boosted topologies which were analysed providing their complete mid-band gain derivation, which was not available before. This paper explores the behaviour of the $g_m$-boosted common-source stage with source-degeneration using this simplified inspection technique. Elementary Norton's and Thevenin's source transformations [57] along with suitable conversion of dependent current-sources into simple conductors/resistors [56], [58] is employed for a "pictorial" and simplified determination of mid-band gain expressions. Progressively simplified small-signal circuits are employed which eliminates the use of complicated nodal or mesh analysis in extracting elegant expressions. The paper also discusses the structural transformation of the $g_m$-boosted common-source with source-degeneration into a transimpedance-amplifier for sensing and detection applications. In order to provide a verification of the design enhancements achieved by the $g_m$-boosted common-source with source-degeneration, comparison with the ordinary common-source with source-degeneration is also provided through circuit simulations. Overall, this paper fully explores the $g_m$-boosted common-source with source-degeneration and provides new "pictorial" transformation based mid-band derivations with an underlying tutorial flavour. Standard symbols [46], [47], [49], [50] are employed for all the MOSFET parameters in the small-signal analysis following the general convention for electronic circuit analysis. As a note on the use of well-defined composite current/voltage notations [59], it is to be mentioned that,

all the voltages and currents in lower-case alphabets along-with upper-case subscripts are quantities containing both a large-signal DC-bias and a small-signal (AC) fluctuation superimposed on it. Also, all the upper-case voltage/current notations along-with upper-case subscripts are DC quantities. Further, all the lower-case voltage/current notations along-with lower-case subscripts are AC quantities.

## 2.1 Transconductance Boosted Common-source with Source-degeneration and its Inspection based Mid-band Analysis

The topology and the simplified progressive "pictorial" inspection-based analysis of the $g_m$-boosted common-source with source-degeneration stage is discussed below. A differential amplifier with gain "A" is used in a negative feed-back loop around the gate and the source of the NMOS amplifier device M1. The equivalent topologies of the $g_m$-boosted common-source with source-degeneration using current-sources or resistors is shown in Fig. 2.1. The $g_m$-boosting differential-amplifier with gain "A" is considered to have high input-impedance (similar to that of an ideal operational amplifier [57]) so that there is no current flowing into its terminals at mid-band frequencies. The input to the common-source stage is applied through the positive (non-inverting) terminal of the $g_m$-boosting amplifier which also contains the DC-bias (common-mode) input. This common-mode voltage is equal to the DC-bias voltage at the negative (inverting) terminal of the $g_m$-boosting amplifier which is the same as the DC-voltage at the source of M1. The gate of the common-source device M1 is biased by the DC level at the output of the $g_m$-boosting differential amplifier.

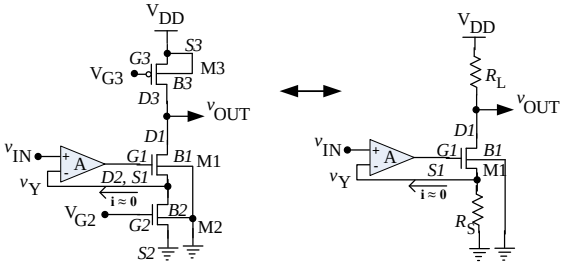



Fig. 2.1 Equivalent forms with current-source or resistive degeneration and load.

The AC equivalent circuit is shown in the Fig. 2.2. The negative feed-back termination can be verified as follows: If there is a slight increase in the voltage at the source of M1 that will result in a slight decrease in the voltage at the gate of M1(small-signal voltage at the output of the differential-amplifier) and as a consequence the drain-current of M1 will reduce. Because of

the reduced drain current the voltage at the source of M1 will reduce slightly thus opposing the previous increase, and hence, imparting stable operation.

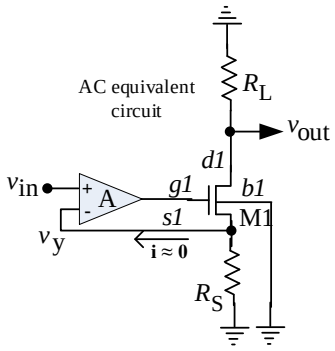



Fig. 2.2 AC equivalent circuit.

Fig. 2.3 depicts the small-signal mid-band equivalent circuit for the $g_m$-boosted common-source with source-degeneration with the gate *g1* at a small-signal voltage of $A(v_{in}-v_y)$. Usually at this stage, circuit analysis equations (simultaneous nodal or mesh equations) are employed to determine the mid-band gain using Fig. 2.3. Instead, a progressive "pictorial" based method [56], [58] is used here in determining the mid-band gain.

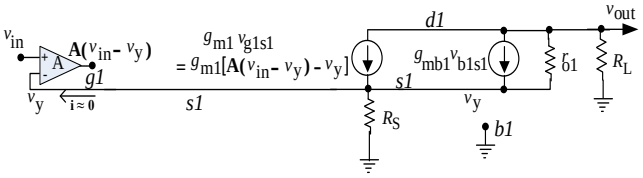



Fig. 2.3 Small-signal equivalent circuit.

Following on, in Fig. 2.4 (a) the output of the $g_m$-boosted common-source with source-degeneration is AC-shorted to ground in order to find the $G_m$ of the Norton amplifier model [58]. In the next diagram, in Fig. 2.4 (b) the small-signal equivalent model for Fig. 2.4 (a) is shown which can be used for finding the $G_m$ of the $g_m$-boosted common-source with source-degeneration.

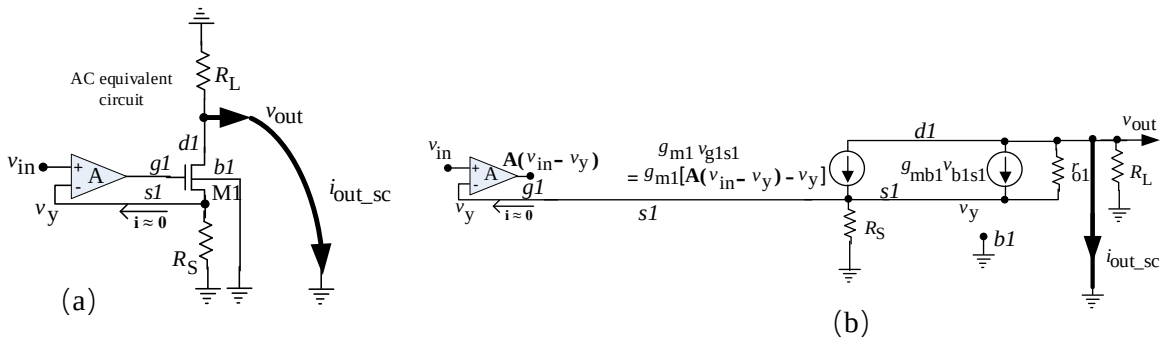



Fig. 2.4 (a) AC equivalent circuit with output AC-shorted to ground, and, (b) small-signal equivalent circuit with output shorted to ground.

Following on in Fig. 2.5 the transconductance current-source is partitioned into two current-sources for the purpose of simplification. It is easily observed now that $-g_{m1}(A+1)v_y$ and $g_{mb1}v_{b1s1}$ are current-sources due the same voltage $(0-v_y)$ across them (with voltages at *b1* and *s1* being zero and $v_y$ respectively).

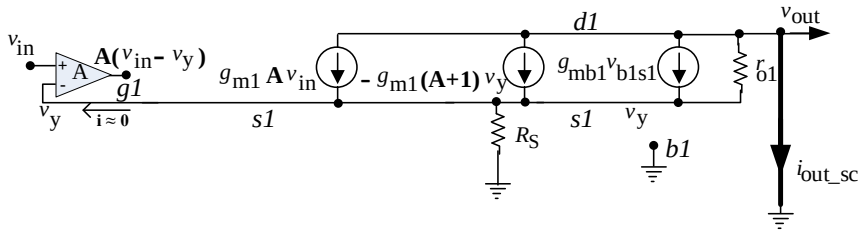



Fig. 2.5 The output shorted small signal equivalent circuit with the transconductance current-source partitioned into two.

Voltage-dependent current-sources that are due to the voltage across themselves can be converted into a simple resistor/conductor [56], [58] which is shown "pictorially" in the two-step circuit equivalence and transformation diagrams in Fig. 2.6 (a) and Fig. 2.6 (b).

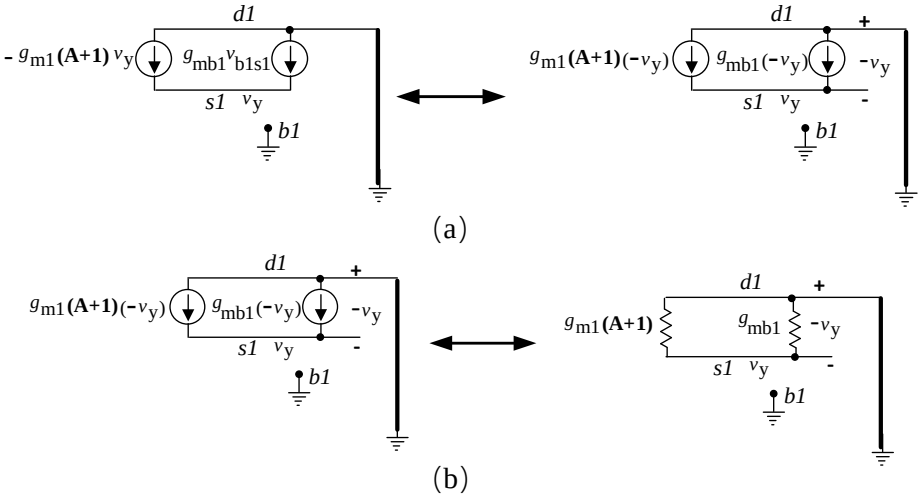



Fig. 2.6 (a) the first-step in the transformation of the current-sources $-g_{m1}(A+1)v_y$ and $g_{mb1}v_{b1s1}$, and, (b) the second-step in the transformation of $-g_{m1}(A+1)v_y$ and $g_{mb1}v_{b1s1}$ into conductors $g_{m1}(A+1)$ and $g_{mb1}$ respectively

The final simplified form of this transformation from Fig. 2.6 (b) is next incorporated into Fig. 2.7 where $-g_{m1}(A+1)v_y$ and $g_{mb1}v_{b1s1}$ are reduced to just two conductors of values $g_{m1}(A+1)$ and $g_{mb1}$ respectively. Also, in Fig. 2.7 it is evident that the current-source current $g_{m1}Av_{in}$ is divided into four parts flowing into the conductors $(1/R_S)$, $g_{m1}(A+1)$, $g_{mb1}$ and $(1/r_{o1})$. Further it is easily observed that the short circuit output current $i_{out\_sc}$ is equal and opposite to the part of $g_{m1}Av_{in}$ flowing through $R_S$.

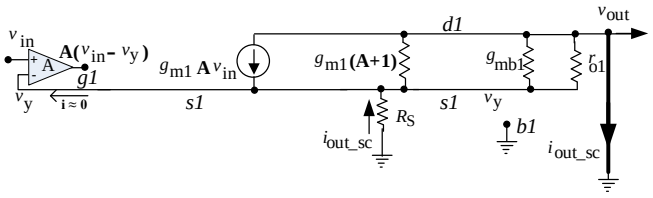



Fig. 2.7 The final equivalent circuit simplified by incorporating $g_{m1}(A+1)$ and $g_{mb1}$ as replacements for $-g_{m1}(A+1)v_y$ and $g_{mb1}v_{b1s1}$ respectively.

Hence, by employing the simple current-division formula in Fig. 2.7,

$$i_{out\_sc} = -g_{m1} A v_{in} \frac{\frac{1}{g_{mb1}+(A+1)g_{m1}+\frac{1}{r_{o1}}}}{R_S + \frac{1}{g_{mb1}+(A+1)g_{m1}+\frac{1}{r_{o1}}}} \tag{2.01}$$

Or,

$$\frac{i_{out\_sc}}{v_{in}} = -g_{m1} A \frac{\frac{1}{g_{mb1}+(A+1)g_{m1}+\frac{1}{r_{o1}}}}{R_S + \frac{1}{g_{mb1}+(A+1)g_{m1}+\frac{1}{r_{o1}}}} \tag{2.02}$$

By rationalizing the above right-hand-side expression,

$$G_m = -g_{m1} A \frac{r_{o1}}{R_S r_{o1} g_{mb1} + R_S (A+1) g_{m1} r_{o1} + R_S + r_{o1}} \tag{2.03}$$

Next, "pictorial" transformations for finding the Rout of the $g_m$-boosted common-source with source-degeneration stage's Norton amplifier model is provided. In Fig. 2.8 the input is AC short-circuited to find the Rout.

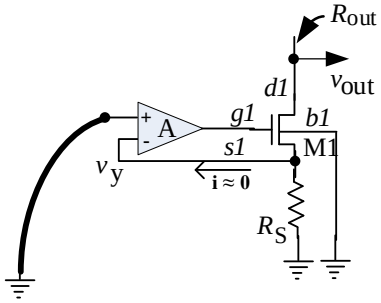



Fig. 2.8 AC equivalent circuit with input shorted to AC ground.

Fig. 2.9 (a) and (b) shows the successively simplified AC small-signal model of the input short-circuited $g_m$-boosted common-source with source-degeneration stage.

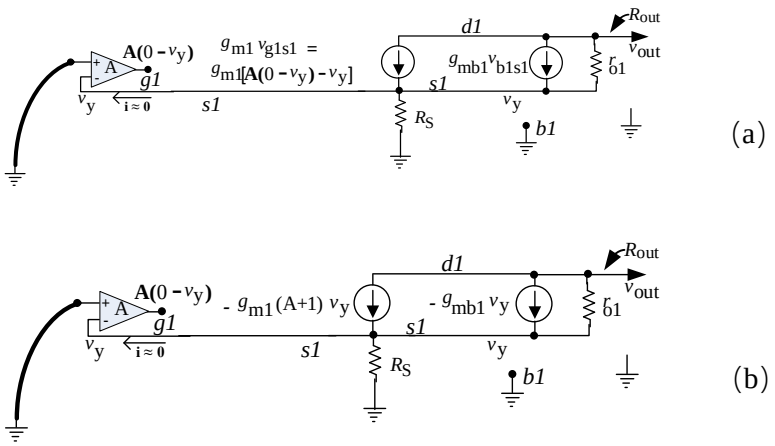



Fig. 2.9 (a) small-signal equivalent circuit of the input shorted amplifier, and, (b) further simplification of the circuit in (a).

Next, in Fig. 2.10, the two dependent current sources being due to the same voltage $v_y$ are accumulated into one current-source along with an inversion of the direction of the arrow to account for the negative values of the two current-courses.

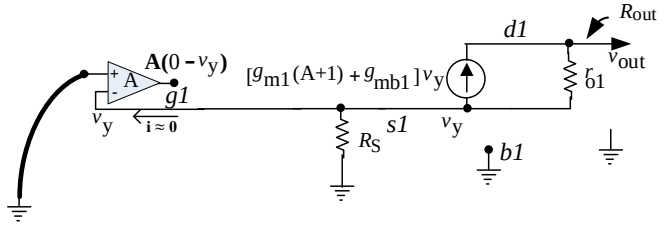



Fig. 2.10 Merging the $g_m$-boosted trans-conductance and the body trans-conductance current-sources and inversion of the current direction.

Finally, in Fig. 2.11 the Norton current-source with parallel resistance ro1 is converted into a Thevenin's voltage-source with a series resistance ro1. Rout can now be easily determined from Fig. 2.11 by dividing the total small-signal (AC) voltage from the output terminal to ground by the small-signal (AC) loop current ($i_{loop} = v_y/R_S$) flowing along the loop shown by the curved line with the arrow.

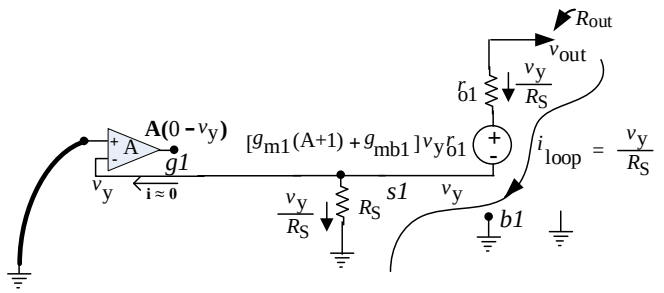



Fig. 2.11 Conversion of the merged Norton circuit into the Thevenin's form.

Hence, the $R_{\text{out}}$ can be found in just two steps as,

$$v_{\text{out}} = \frac{v_{\text{y}}}{R_S} r_{\text{o1}} + [(\text{A}+1)g_{\text{m1}} + g_{\text{mb1}}]v_{\text{y}} r_{\text{o1}} + v_{\text{y}} \tag{2.04}$$

And,

$$R_{\text{out}} = \frac{v_{\text{out}}}{i_{\text{loop}}} = \frac{\frac{v_{\text{y}}}{R_S} r_{\text{o1}} + [(\text{A}+1)g_{\text{m1}} + g_{\text{mb1}}]v_{\text{y}} r_{\text{o1}} + v_{\text{y}}}{\frac{v_{\text{y}}}{R_S}} \tag{2.05}$$

Or,

$$R_{\text{out}} = R_S r_{\text{o1}} g_{\text{mb1}} + R_S(\text{A}+1)g_{\text{m1}} r_{\text{o1}} + R_S + r_{\text{o1}} \tag{2.06}$$

Finally, using equations (2.03) and (2.06) the no-load (intrinsic) gain of the $g_{\text{m}}$-boosted common-source with source-degeneration stage (determined by employing an ideal current-source load) is given by,

$$\begin{aligned} \text{A}_{\text{V}}^{\text{no-load}} &= G_{\text{m}} R_{\text{out}} \\ &= -g_{\text{m1}}\,\text{A}\,\frac{r_{\text{o1}}}{R_S r_{\text{o1}} g_{\text{mb1}} + R_S(\text{A}+1)g_{\text{m1}} r_{\text{o1}} + R_S + r_{\text{o1}}} \\ &\quad \times R_S r_{\text{o1}} g_{\text{mb1}} + R_S(\text{A}+1)g_{\text{m1}} r_{\text{o1}} + R_S + r_{\text{o1}} \\ &= -g_{\text{m1}}\,\text{A}\,r_{\text{o1}} \end{aligned} \tag{2.07}$$

So, the intrinsic-gain is increased by a factor of "$\text{A}$" compared to the ordinary common-source with source-degeneration. For a finite load $R_{\text{L}}$ instead of an ideal current-source load the gain is given by,

$$\text{A}_{\text{V}}^{\text{finite-load}} = G_{\text{m}}(R_{\text{out}} \,||\, R_{\text{L}}) \tag{2.08}$$

Or,

$$\text{A}_{\text{V}}^{\text{finite-load}} = -\frac{g_{\text{m1}}\,\text{A}\,r_{\text{o1}} R_{\text{L}}}{R_{\text{L}} + R_S r_{\text{o1}} g_{\text{mb1}} + R_S(\text{A}+1)g_{\text{m1}} r_{\text{o1}} + R_S + r_{\text{o1}}} \tag{2.09}$$

## 2.2 Transconductance Boosted Common-source with Source-degeneration as a Transimpedance Amplifier

Transimpedance amplifiers (TIAs) are one of the most important analog signal conditioning circuits particularly for meeting challenging current-sensing specifications in today's exploding sensor and biomedical applications. This is in addition to the traditional broad-band

opto-electronic storage and communication applications employing inductive bandwidth enhancements. Any amplifier topology can be configured to operate as a transimpedance amplifier. Here we investigate the transimpedance amplifier configuration of the $g_m$-boosted common-source with source degeneration which has not been reported before. Fig. 2.12 shows the standard common-source with source-degeneration converted into a TIA employing a current-feedback resistor $R_F$ and an input current signal $i_{in}$ to produce a sensed output voltage. Here $R_F$ also provides the drain feed-back DC-bias at the gate of M1. This drain-feedback biasing allows the device M1 to be in strong-inversion saturation by maintaining a suitable $V_{DS}$ ($=V_{GS}$) so that $V_{DS} > (V_{GS}-V_{TH})$.

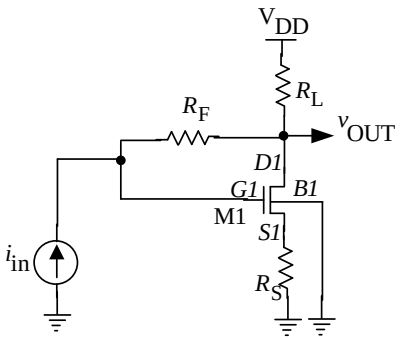



Fig. 2.12 A common-source with source-degeneration wired-up in a transimpedance-amplifier configuration.

However, in case of the $g_m$-boosted common-source with source-degeneration such drain feed-back biasing will not work. This is because the DC-bias voltages at the input terminals of the $g_m$-boosting differential-amplifier are equal (common-mode voltage) and drain feed-back biasing will result in the $V_{DS}$ of M1 to be zero and consequently M1 will be driven into the triode region. Hence, a novel biasing scheme is provided for the proper operation of the $g_m$-boosted common-source with source-degeneration in a TIA configuration as shown in the Fig. 2.13.

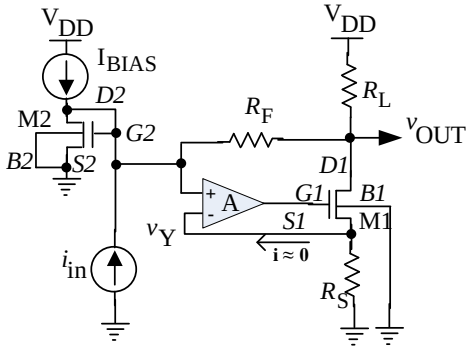



Fig. 2.13 A $g_m$-boosted common-source with source-degeneration stage configured for operation as a transimpedance amplifier with bias-circuit for proper operation as a current feed-back amplifier

An appropriate current $I_{BIAS}$ is forced through the diode connected device M2 which independently sets the DC-voltage at the positive terminal of the $g_m$-boosting amplifier to the DC-voltage $V_Y$ at the negative terminal (the common-mode voltage). Thus, the DC-voltage at the drain of M1 can be relaxed to be set at an appropriate higher value in order to keep M1 in saturation. In addition, the small-signal feedback current through $R_F$ can conveniently add algebraically to the small-signal input current $i_{in}$ at the positive terminal of the $g_m$-boosting amplifier thus providing closed loop current feed-back operation. Next, the Fig. 2.14 shows the AC equivalent circuit of the TIA where the bias circuit presents the small-signal impedance ( $R_{eq\_bias}$ ) given by,

$$R_{eq\_bias} = \frac{1}{g_{m2} + \frac{1}{r_{o2}}} \tag{2.10}$$

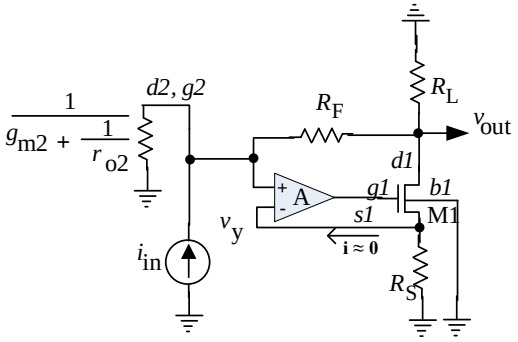



Fig. 2.14 AC equivalent circuit of a $g_m$-boosted common-source with source-degeneration stage configured for operation as a transimpedance amplifier.

The open-loop AC equivalent circuit for determining the loop-gain and the closed-loop transimpedance gain is shown in the Fig. 2.15 which is the $g_m$-boosted common-source with source-degeneration topology.

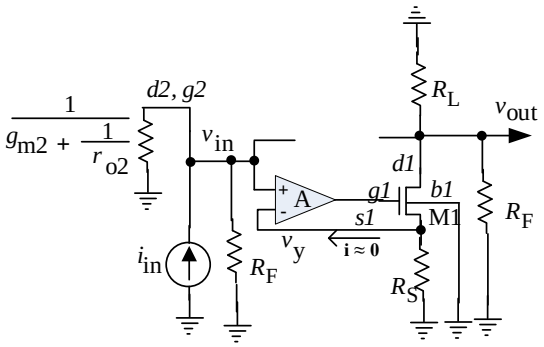



Fig. 2.15 the open-loop circuit for determining the loop-gain and the closed-loop transimpedance gain.

This circuit is obtained employing a 2-port Y-model for the feed-back path [47] so that the admittance parameters are $Y_{11}=1/R_F$ and $Y_{22}=1/R_F$ for the open-loop feed-forward transimpedance amplifier (with the effect of feed-back loading). Also, the feed-back factor, β is given by the admittance parameter, $Y_{21}=1/R_F$. It has input-voltage $v_{in}$ corresponding to the input-current $i_{in}$, and the output-voltage $v_{out}$ as shown in the figure along with a load resistance $R'_L$ (=$R_L$//$R_F$). Hence, employing equation (2. 09),

$$A_V^{\text{open-loop}} = \frac{v_{out}}{v_{in}} = -\frac{g_{m1} A r_{o1}(R_L // R_F)}{(R_L // R_F) + R_S r_{o1} g_{mb1} + R_S (A+1) g_{m1} r_{o1} + R_S + r_{o1}} \tag{2.11}$$

Where, $v_{in}$ the equivalent small-signal voltage at the positive terminal of the $g_m$-boosting amplifier is given by,

$$v_{in} = i_{in} \frac{1}{g_{m2} + \frac{1}{r_{o2}} + \frac{1}{R_F}} \tag{2.12}$$

Hence, the open-loop transimpedance gain is given by,

$$Z_{TIA}^{\text{open-loop}} = -\frac{g_{m1} A r_{o1}(R_L // R_F)\left(\frac{1}{g_{m2} + \frac{1}{r_{o2}} + \frac{1}{R_F}}\right)}{(R_L // R_F) + R_S r_{o1} g_{mb1} + R_S (A+1) g_{m1} r_{o1} + R_S + r_{o1}} \tag{2.13}$$

And, the closed loop transimpedance gain is given by,

$$Z_{TIA}^{\text{closed-loop}} = -\frac{\dfrac{g_{m1} A r_{o1}(R_L // R_F)\left(\frac{1}{g_{m2} + \frac{1}{r_{o2}} + \frac{1}{R_F}}\right)}{(R_L // R_F) + R_S r_{o1} g_{mb1} + R_S (A+1) g_{m1} r_{o1} + R_S + r_{o1}}}{1 + \frac{1}{R_F} \dfrac{g_{m1} A r_{o1}(R_L // R_F)\left(\frac{1}{g_{m2} + \frac{1}{r_{o2}} + \frac{1}{R_F}}\right)}{(R_L // R_F) + R_S r_{o1} g_{mb1} + R_S (A+1) g_{m1} r_{o1} + R_S + r_{o1}}} \tag{2.14}$$

Where, the standard feed-back factor, $\beta=1/R_F$.

### 2.3 Performance Verification through Simulation Results

Simulations were carried-out on Cadence for the presented circuits employing a 1.8V power supply, current-source load and resistive source-degeneration. Similar device sizes and component values were employed for the corresponding transistors and resistors for the $g_m$-

boosted and the non $g_m$-boosted (basic) amplifiers for their performance comparisons. Fig. 2.16 shows the $g_m$-boosted common-source with source-degeneration stage for simulation along-with the transistor-level diagram of the $g_m$-boosting amplifier. The device-sizes and component values were as follows, for M1 W/L = 2µm/0.2µm, for M2 W/L = 2µm/0.370µm, for M3 and M4 W/L = 2.8µm/0.220µm, for M5 and M6 W/L = 6µm/0.220µm, for the tail device M7 W/L = 4.4µm/0.180µm and finally $R_S$ = 10k. The bias voltages $V_{G2}$ and $V_{G7}$ were respectively 695mV and 590mV, while the common-mode DC input voltage at $v_{IN}$ was 701 mV.

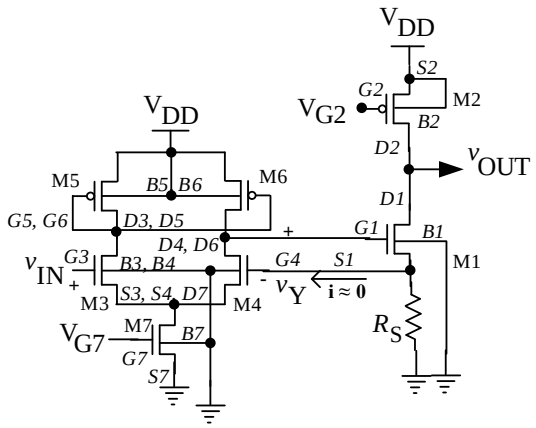



Fig. 2.16 A $g_m$-boosted common-source with source-degeneration stage for simulation

Fig. 2.17 shows that the voltage gain of the $g_m$-boosted common-source with source-degeneration stage is much higher compared to that for the common-source with source-degeneration stage without $g_m$ boosting for similar size of gain device, load device and source-degeneration resistor.

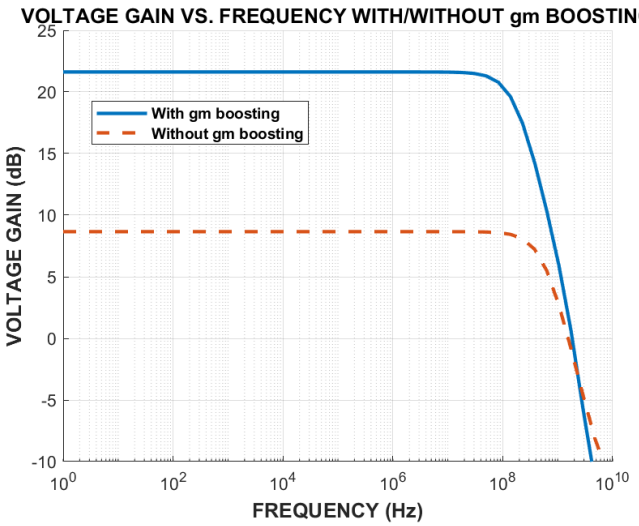



Fig. 2.17 Comparison of the voltage gain of common-source with source-degeneration, with and without $g_m$-boosting.

Next, Fig. 2.18 shows a comparison of the voltage gain of common-source with source-degeneration, with and without $g_m$-boosting with increasing value of a finite resistive load $R_L$. With increasing finite load resistance $R_L$ the gain of the amplifier approaches towards the intrinsic-gain of the amplifier. Hence, in agreement with the expression for the intrinsic-gain of the ordinary common-source with source-degeneration ($g_m r_o$) compared to that of the $g_m$-boosted common-source with source-degeneration ($Ag_m r_o$) given by equation (2.07) the gain increases rapidly with $R_L$ in case of the $g_m$-boosting. This verifies the gain enhancement achieved by employing the $g_m$-boosting.

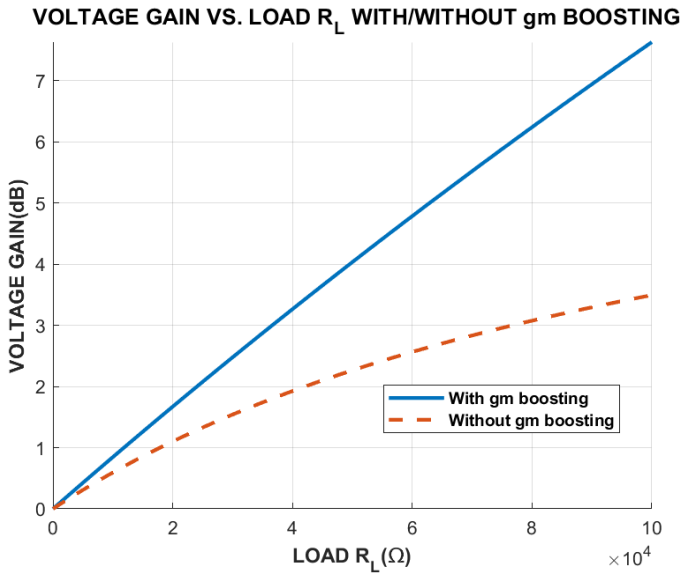



Fig 2.18 Comparison of the voltage-gain of common-source with source-degeneration, with and without $g_m$-boosting with increasing value of a finite resistive load RL.

Next, Fig. 2.19 shows the TIA configuration of the $g_m$-boosted common-source with source-degeneration for simulation along-with the transistor-level diagram of the $g_m$-boosting amplifier. The device-sizes and component values were as follows, for M1 W/L = 2.7µm/0.180µm, for M2 W/L = 5.5µm/0.220µm, for M3 and M4 W/L = 2.8µm/0.220µm, for M5 and M6 W/L = 6µm/0.220µm, for the tail device M7 W/L = 4.4µm/0.180µm, for the bias device M8 W/L = 3.5µm/0.180µm, the source-degeneration $R_S$ = 6k and the feed-back resistor $R_F$ = 1k. Also, the bias current $I_{BIAS}$ = 15 µA and the bias voltages $V_{G2}$ and $V_{G7}$ are respectively 800mV and 590 mV.

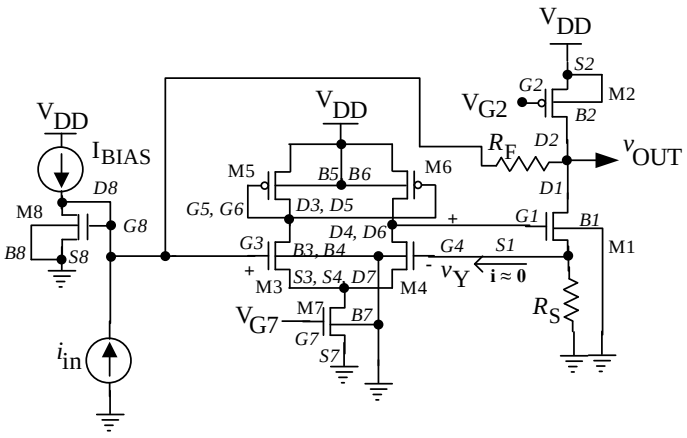



Fig. 2.19 A TIA configuration of the $g_m$-boosted common-source with source-degeneration for simulation.

Fig. 2.20 shows the comparison of the transimpedance gain of the TIA configuration of common-source with source-degeneration, with and without $g_m$-boosting. It is clearly seen that the voltage-gain of the $g_m$-boosted common-source with source-degeneration TIA is much higher compared to that for the ordinary common-source with source degeneration TIA without $g_m$-boosting for similar size of gain device, load device, feed-back resistor and source-degeneration resistor.

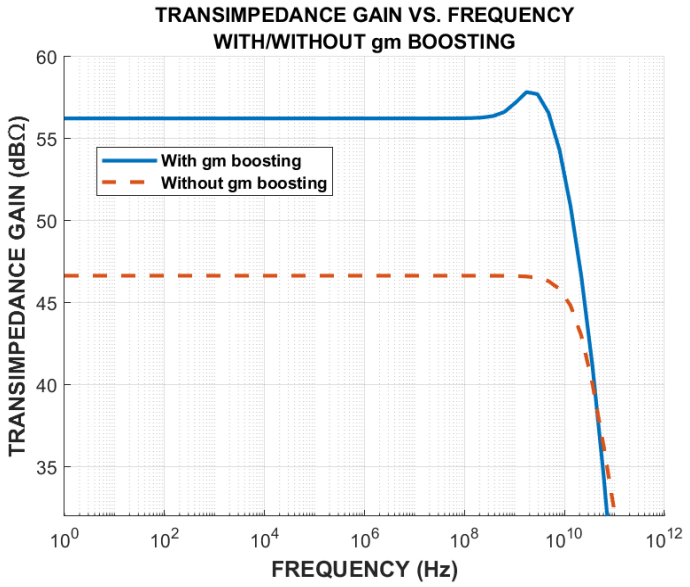



Fig. 2.20 Comparison of the transimpedance gain of the TIA configuration of common-source with source-degeneration, with and without $g_m$-boosting.

# Chapter 3 $g_m$-boosted Inverter Cascode Transimpedance Amplifier

This chapter illustrates the $g_m$-boosted inverter cascode TIA ($g_m$-boosted Inv-Cas TIA) using a quasi-floating gate (QFG) design. Theoretical analysis such as its mid-band gain and noise analysis are developed. And its simulation results indicated the transimpedance gain is 145.8 dB with a -3-dB bandwidth of 5.31 kHz. The input referred noise current spectral density is below 4.23 pA/sqrt (Hz). Eye diagram simulation using -123dBm input photodiode current signal and a $2^{31}$-1 pseudo random bit sequence data pattern shows an eye opening of 90% at 3kbit/s.

## 3.1 Topology of $g_m$-boosted Inv-Cas TIA

The proposed $g_m$-boosted Inv-Cas TIA structure is presented in Fig. 3.2 and its biasing circuit is shown in Fig. 3.1. It was developed from Inv-Cas TIA with $g_m$-boosting and two additional DC biasing voltage circuits which extremely increased the open loop transimpedance gain and reduced the space occupied. Two differential amplifiers with gain "$A_1$" and "$A_2$" are added around the gate and source of the cascode transistors M2 and M3. Traditional Inv-Cas TIA relays on a current-feedback resistor $R_F$ to provides the drain feed-back DC-bias at transistors M1 and M4. Here, two additional biasing circuits supply DC-voltages to M1 and M4 independently. Appropriate DC-voltages are chosen to force M1 and M4 to be in a strong saturation region. Therefore, the DC-voltages at the drain of M2 and M3 can be relaxed instead of making it appropriate to bias M1 and M4 in saturation. Also, two capacitors are added to separate the DC voltages and only allow the AC signal to across. This structure is named quasi-floating gate (QFG) which allows large signal swings [60], [61]. Thus, the small-signal feedback current through $R_F$ can be added algebraically to the small-signal input current $i_{in}$.

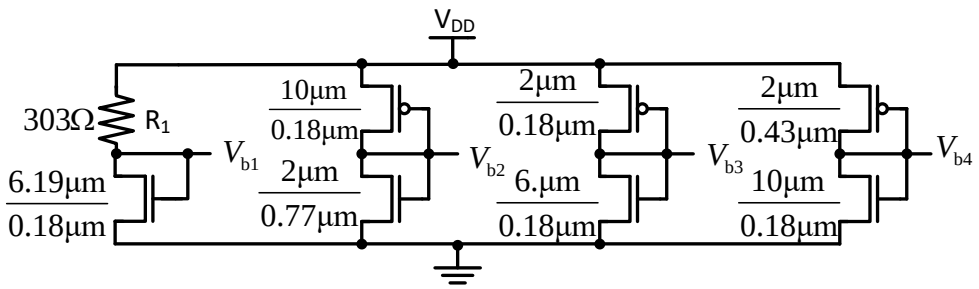



Fig. 3.1 A biasing circuit of $g_m$-boosted Inv-Cas TIA circuit design.

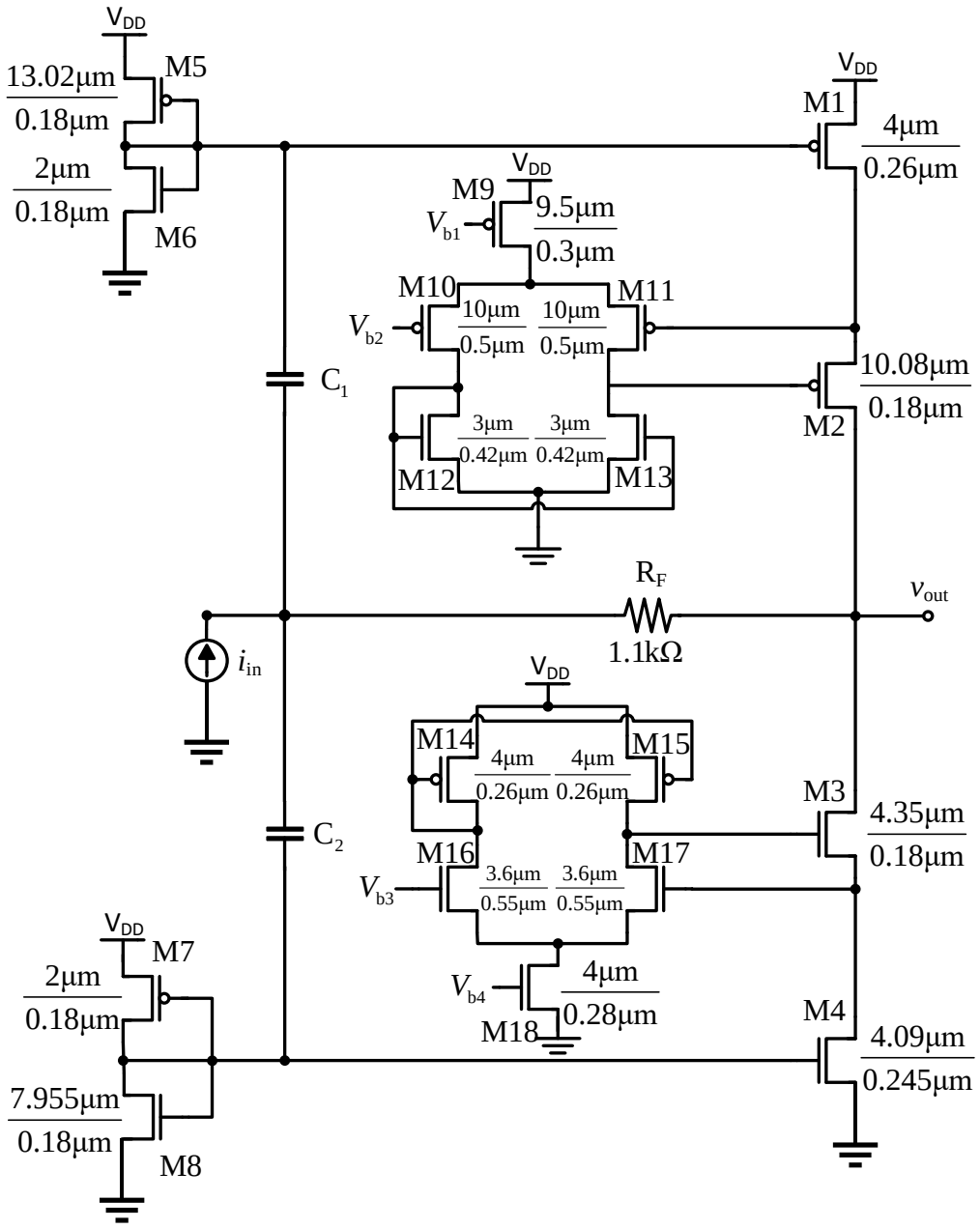



Fig. 3.2 Schematic of proposed $g_m$-boosted Inv-Cas TIA.

## 3.2 Analysis of Mid-band Transimpedance Gain

To analyse the transimpedance gain of the proposed $g_m$-boosted Inv-Cas TIA, the open-loop AC equivalent circuit of the proposed $g_m$-boosted Inv-Cas TIA is provided in Fig. 3.3 and the $g_m$-boosters are replaced by triangle symbols. All the DC power supply $V_{dd}$ and DC-bias of $g_m$-booster are AC grounded. The capacitors act as short. Also, the feedback factor β can be written as 1/ $R_F$.

$$\beta = \frac{1}{R_F} \tag{3.01}$$

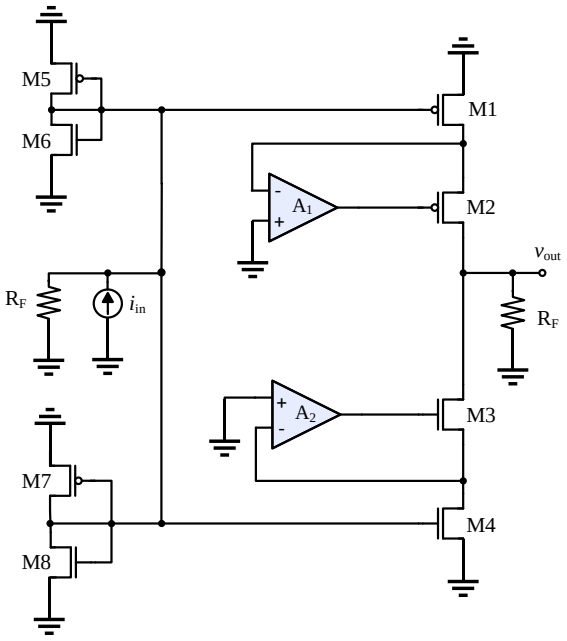



Fig. 3.3 Open-loop AC equivalent circuit for proposed $g_m$-boosted Inv-Cas TIA.

Two $g_m$ booster circuits are replaced by triangle symbols with gain $A_1$ and $A_2$ to simplify the circuit. Next, the transistors of bias circuits are diode-connected and transistors M5, M6, M7 and M8 can be simply represented by resistors ($1/g_m$) with the voltage across themselves [58]. Thus, the equivalent small signal of the bias circuits is shown in Fig. 3.4 and the impedances are given by,

$$R_{eq\_bias1} = \frac{1}{\frac{1}{g_{m5}} + \frac{1}{g_{m6}}} \tag{3.02}$$

$$R_{eq\_bias2} = \frac{1}{\frac{1}{g_{m7}} + \frac{1}{g_{m8}}} \tag{3.03}$$

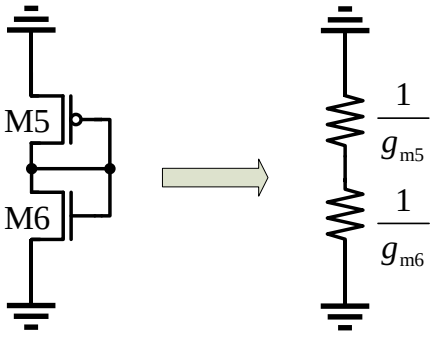



Fig. 3.4 AC equivalent circuit for bias circuit.

The simplified open-loop AC equivalent circuit for determining the loop-gain and the closed-loop transimpedance gain is shown in Fig. 3.5. The transistors M1, M2 and M3, M4 are broken into two cascode structure circuits in parallel. A full derivative of the NMOS transistors part is

presented below. As these two circuits are the same, the result can be simply applied to the PMOS transistors part. In addition, the small-signal equivalent circuit of the NMOS cascode circuit is presented in Fig 3.6. The negative terminal is considered to have no current flowing from $v_y$ at mid-band frequency because the input impedance of the differential amplifier with gain "A" is very high. The voltage at the gate of transistor M3 is expressed as,

$$\begin{aligned}&(0-v_y)A_2\\&=-A_2v_y\end{aligned} \tag{3.04}$$

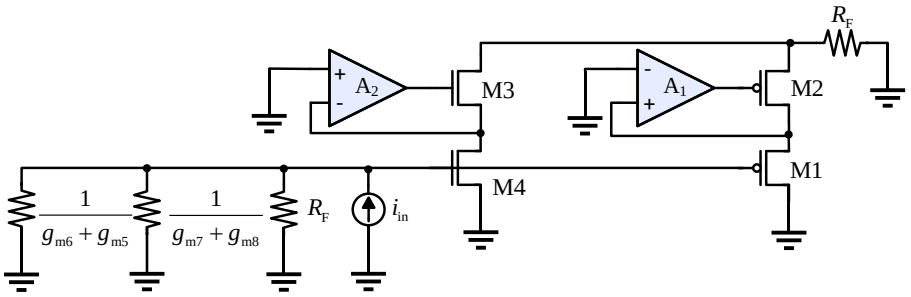



Fig. 3.5 A simplified open-loop AC equivalent circuit.

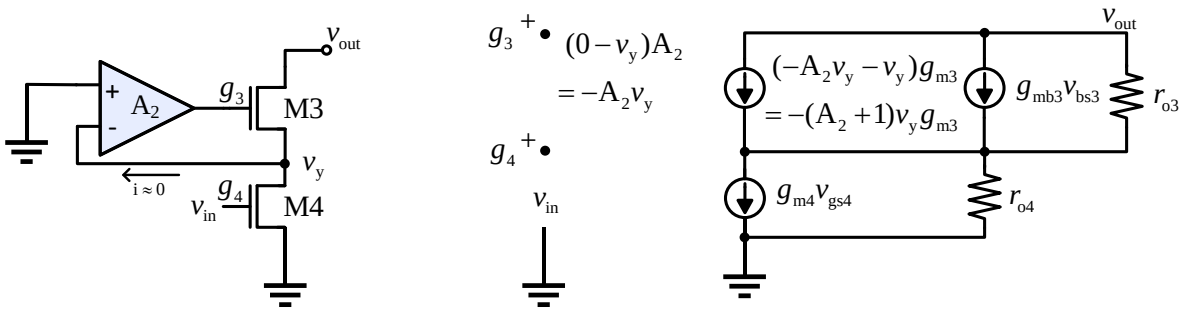



Fig. 3.6 A small-signal equivalent circuit.

Next, the mid-band transimpedance gain can be simply derivatised using a double short-circuit method to find out the composite trans-conductance $G_m$ and the composite output impedance $R_{out}$. And the gain is given by,

$$A_v = G_m R_{out} \tag{3.05}$$

And the trans-conductance $G_m$ can be expressed by,

$$G_m = \frac{i_{out}}{v_{in}} \tag{3.06}$$

As shown in Fig. 3.7, the output is shorted to ground with a capacitor to find out the $i_{out}$. The transconductance of transistor M3 can be seen as that $g_{m3}$ is boosted to $(A_2+1)g_{m3}$ and $v_{gs1}$ becomes $-v_y$. In fact, the voltage at the gate of transistor M3 is at an AC ground [56]. As a result,

the transconductance and body-effect trans-conductance current source are replaced by a resistor $1/g_{m3}$ and a body-effect resistor $1/g_{mb3}$.

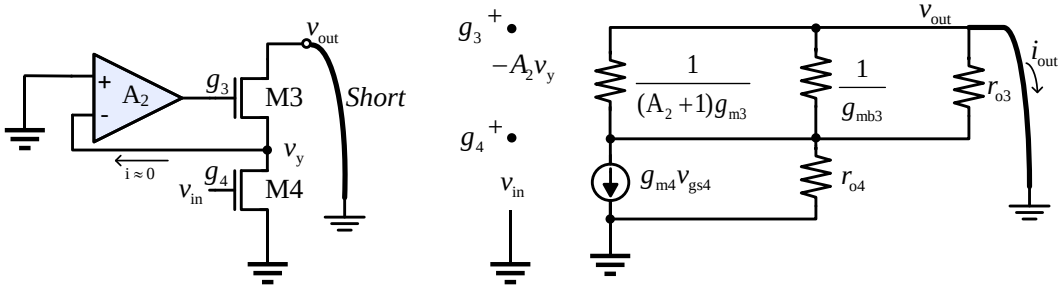



Fig. 3.7 An output short circuit analysis to determine $G_m$.

In Fig. 3.8, the equivalent resistors from transistor M3 are merged into one and the Norton current source of transistor M4 is converted to its Thevenin equivalent circuit. Now, the output current of the circuit is simply given in equation (3.07).

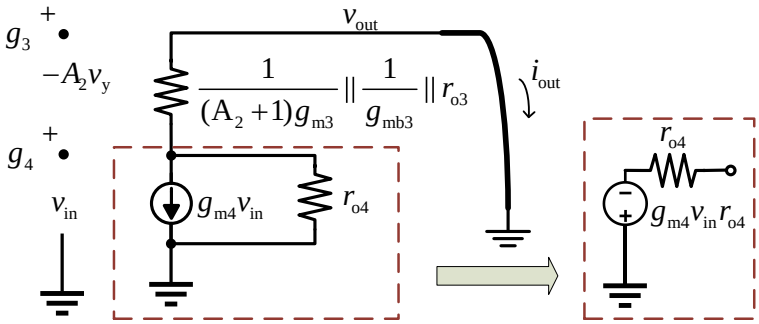



Fig. 3.8 Conversion from Norton current source into Thevenin equivalent circuit.

$$i_{out} = -\frac{g_{m4}v_{in}r_{o4}}{r_{o4} + \dfrac{1}{(A+1)g_{m3}} \| \dfrac{1}{g_{mb3}} \| r_{o3}} \tag{3.07}$$

Simplifying,

$$\begin{aligned} i_{out} &= -\frac{g_{m4}v_{in}r_{o4}}{r_{o4} + \dfrac{1}{(A+1)g_{m3} \| g_{mb3} \| \dfrac{1}{r_{o3}}}} \\ &= -\frac{g_{m4}v_{in}r_{o4}\left[(A+1)g_{m3} + g_{mb3} + \dfrac{1}{r_{o3}}\right]}{r_{o4}\left[(A+1)g_{m3} + g_{mb3} + \dfrac{1}{r_{o3}}\right] + 1} \\ &= -\frac{g_{m4}v_{in}r_{o4}\left\{\left[(A+1)g_{m3} + g_{mb3}\right]r_{o3} + 1\right\}}{r_{o4} + r_{o4}\left[(A+1)g_{m3} + g_{mb3}\right]r_{o3} + r_{o3}} \end{aligned} \tag{3.08}$$

Changing sides and rationalizing,

$$\begin{aligned} G_{m1} &= \frac{i_{out}}{v_{in}} \\ &= -\frac{g_{m4}r_{o4}\left\{\left[(A+1)g_{m3}+g_{mb3}\right]r_{o3}+1\right\}}{r_{o4}+r_{o4}\left[(A+1)g_{m3}+g_{mb3}\right]r_{o3}+r_{o3}} \end{aligned} \tag{3.09}$$

To find $R_{out}$, the cascode input at the gate of M4 is shorted by an AC grounding capacitor. Fig. 3.9 depicts the small-signal model of the circuit after shorting the input. The trans-conductor current source of M4 is eliminated and only resistor $r_{o4}$ is left. Now, the small-signal model of the circuit is the same as a simple common source with source degeneration. In addition, because of $v_y = v_{s3}$, the trans-conductance and body effect trans-conductance current sources can merge into one.

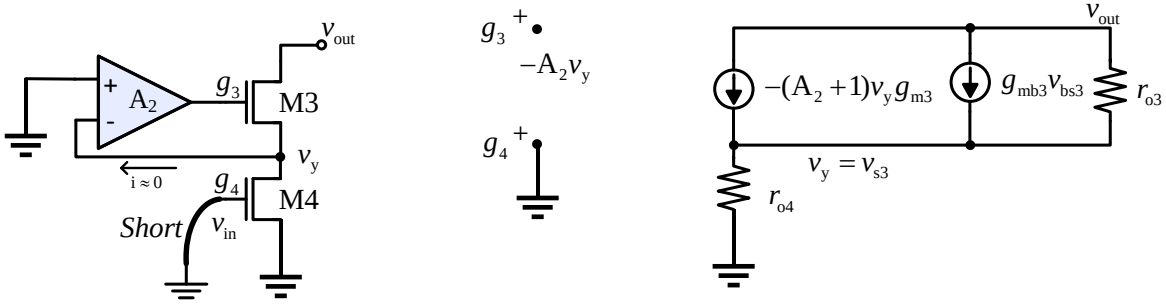



Fig. 3.9 Input short circuit analysis to determine Rout.

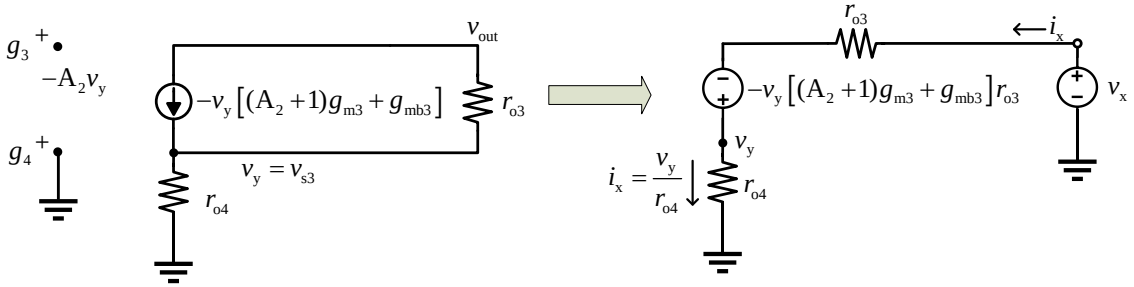



Fig. 3.10 Conversion from Norton current source into Thevenin voltage source.

Fig. 3.10 shows the conversion from Norton current source into Thevenin voltage source. The output impedance $R_{out}$ can be found by incremental KVL, dividing the total small-signal voltage from the drain terminal to ground by the small-signal current flowing out the drain (equation 3.09).

$$R_{out1} = \frac{v_x}{i_x} \tag{3.10}$$

$R_{out}$ can be written as,

$$R_{out1} = \frac{v_y + v_y\left[(A+1)g_{m3} + g_{mb3}\right]r_{o3} + \frac{v_y}{r_{o4}}r_{o3}}{\frac{v_y}{r_{o4}}} \tag{3.11}$$

After rationalizing,

$$R_{out1} = r_{o4} + r_{o4}\left[(A+1)g_{m3} + g_{mb3}\right]r_{o3} + r_{o3} \tag{3.12}$$

Similarly, the small-signal analysis procedures can be directly applied to the PMOS cascode structure (M1 and M2). The composite trans-conductance is given by,

$$G_{m2} = -\frac{g_{m1}r_{o1}\left\{\left[(A+1)g_{m2} + g_{mb2}\right]r_{o2} + 1\right\}}{r_{o1} + r_{o1}\left[(A+1)g_{m2} + g_{mb2}\right]r_{o2} + r_{o2}} \tag{3.13}$$

Also, the output impedance of transistors M1 and M2 is given by,

$$R_{out2} = r_{o1} + r_{o1}\left[(A+1)g_{m2} + g_{mb2}\right]r_{o2} + r_{o2} \tag{3.14}$$

Finally, the small-signal equivalent circuit of the proposed $g_m$-boosted Inv-Cas TIA is simplified as shown in Fig. 3.11. The mid-band open-loop transimpedance gain of the small-signal is given by,

$$Z_{open} = \frac{v_{out}}{i_{in}} \tag{3.15}$$

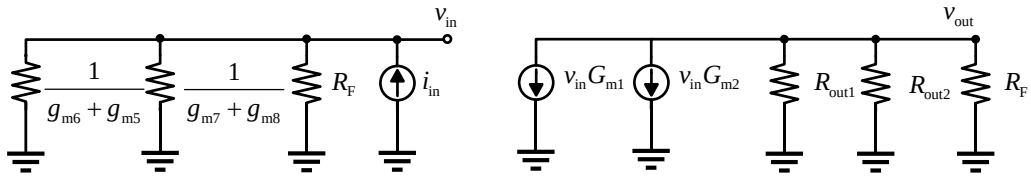



Fig. 3.11 Final simplified open-loop AC equivalent circuit.

From the left part of Fig. 3.11, the input voltage $v_{in}$ at the gate is proportional to the total resistance and the current $i_{in}$ across it, which is given by,

$$v_{in} = i_{in}\left(\frac{1}{g_{m5}+g_{m6}} \| \frac{1}{g_{m7}+g_{m8}} \| R_F\right) \tag{3.16}$$

Simplifying,

$$\begin{aligned} v_{in} &= i_{in}\frac{1}{g_{m5}+g_{m6}+g_{m7}+g_{m8}+\frac{1}{R_F}} \\ &= i_{in}\left(g_{m5}+g_{m6}+g_{m7}+g_{m8}+\frac{1}{R_F}\right) \end{aligned} \tag{3.17}$$

Changing sides,

$$i_{\text{in}} = v_{\text{in}}(g_{\text{m5}} + g_{\text{m6}} + g_{\text{m7}} + g_{\text{m8}} + \frac{1}{R_{\text{F}}}) \tag{3.18}$$

For the right part of Fig. 3.11, the composite trans-conductance current source $v_{\text{in}}G_{\text{m1}}$ and $v_{\text{in}}G_{\text{m2}}$ can be merged into one by inspection. Then following the same procedure as utilized for equation (3.15), the output voltage $v_{\text{out}}$ is given by,

$$v_{\text{out}} = v_{\text{in}}(G_{\text{m1}} + G_{\text{m2}})(R_{\text{out1}} \,||\, R_{\text{out2}} \,||\, R_{\text{F}}) \tag{3.19}$$

Following equation (3.14), the open-loop transimpedance gain is given by,

$$Z_{\text{open}} = \frac{(G_{\text{m1}} + G_{\text{m2}})(R_{\text{out1}} \,||\, R_{\text{out2}} \,||\, R_{\text{F}})}{g_{\text{m5}} + g_{\text{m6}} + g_{\text{m7}} + g_{\text{m8}} + \frac{1}{R_{\text{F}}}} \tag{3.20}$$

Where the composite trans-conductance $G_{\text{m1}}$, $G_{\text{m2}}$ and the composite output impedance $R_{\text{out1}}$, $R_{\text{out2}}$ are derivatised in previous equations.

In the end, the closed-loop transimpedance gain of the proposed $g_{\text{m}}$-boosted Inv-Cas TIA can be quantified by [47],

$$\begin{aligned} Z_{\text{closed}} &= \frac{Z_{\text{open}}}{1 + \beta Z_{\text{open}}} \\ &= \frac{\dfrac{(G_{\text{m1}} + G_{\text{m2}})(R_{\text{out1}} \,||\, R_{\text{out2}} \,||\, R_{\text{F}})}{g_{\text{m5}} + g_{\text{m6}} + g_{\text{m7}} + g_{\text{m8}} + \frac{1}{R_{\text{F}}}}}{1 + \dfrac{1}{R_{\text{F}}} \dfrac{(G_{\text{m1}} + G_{\text{m2}})(R_{\text{out1}} \,||\, R_{\text{out2}} \,||\, R_{\text{F}})}{g_{\text{m5}} + g_{\text{m6}} + g_{\text{m7}} + g_{\text{m8}} + \frac{1}{R_{\text{F}}}}} \end{aligned} \tag{3.21}$$

Simplifying and rationalizing,

$$Z_{\text{closed}} = \frac{R_{\text{F}}(G_{\text{m1}} + G_{\text{m2}})(R_{\text{out1}} \,||\, R_{\text{out2}} \,||\, R_{\text{F}})}{R_{\text{F}}(g_{\text{m5}} + g_{\text{m6}} + g_{\text{m7}} + g_{\text{m8}}) + (G_{\text{m1}} + G_{\text{m2}})(R_{\text{out1}} \,||\, R_{\text{out2}} \,||\, R_{\text{F}}) + 1} \tag{3.22}$$

## 3.3 Input Referred Noise Analysis

Considering only thermal noise of resistors and drain-current noise of MOSFET devices, the input referred noise current spectral density of the $g_m$-boosted Inv-Cas TIA is expressed in Fig. 3.12 using noise inserted circuit diagram [62],[63], where the thermal noise can be expressed by a current source connected between drain and source for the MOSFET devices operating in saturation region[47]. Drain current noise power density for MOSFET and thermal current noise power density for resistor are given by [64],

$$\overline{i^2_{n,in}} = 4KT\frac{\gamma}{\alpha}g_m \tag{3.23}$$

$$\overline{i^2_{n,r}} = 4KT\frac{1}{R} \tag{3.24}$$

Where γ and α are noise dependant parameters on the channel length of the MOSFET.

Thus, the noise current power spectral density of MOSFETs and resistor in Fig 3.12 can be written as,

$$\overline{i^2_{n,m1}} = 4KT\frac{\gamma_1}{\alpha_1}g_{m1} \tag{3.25}$$

$$\overline{i^2_{n,m2}} = 4KT\frac{\gamma_2}{\alpha_2}g_{m2} \tag{3.26}$$

$$\overline{i^2_{n,m3}} = 4KT\frac{\gamma_3}{\alpha_3}g_{m3} \tag{3.27}$$

$$\overline{i^2_{n,m4}} = 4KT\frac{\gamma_4}{\alpha_4}g_{m4} \tag{3.28}$$

$$\overline{i^2_{n,m5}} = 4KT\frac{\gamma_5}{\alpha_5}g_{m5} \tag{3.29}$$

$$\overline{i^2_{n,m6}} = 4KT\frac{\gamma_6}{\alpha_6}g_{m6} \tag{3.30}$$

$$\overline{i^2_{n,m7}} = 4KT\frac{\gamma_7}{\alpha_7}g_{m7} \tag{3.31}$$

$$\overline{i^2_{n,m8}} = 4KT\frac{\gamma_8}{\alpha_8}g_{m8} \tag{3.32}$$

$$\overline{i^2_{n,m9}} = 4KT\frac{\gamma_9}{\alpha_9}g_{m9} \tag{3.33}$$

$$\overline{i^2_{\text{n,m10}}} = 4KT\frac{\gamma_{10}}{\alpha_{10}}g_{\text{m10}} \tag{3.34}$$

$$\overline{i^2_{\text{n,m11}}} = 4KT\frac{\gamma_{11}}{\alpha_{11}}g_{\text{m11}} \tag{3.35}$$

$$\overline{i^2_{\text{n,m12}}} = 4KT\frac{\gamma_{12}}{\alpha_{12}}g_{\text{m12}} \tag{3.36}$$

$$\overline{i^2_{\text{n,m13}}} = 4KT\frac{\gamma_{13}}{\alpha_{13}}g_{\text{m13}} \tag{3.37}$$

$$\overline{i^2_{\text{n,m14}}} = 4KT\frac{\gamma_{14}}{\alpha_{14}}g_{\text{m14}} \tag{3.38}$$

$$\overline{i^2_{\text{n,m15}}} = 4KT\frac{\gamma_{15}}{\alpha_{15}}g_{\text{m15}} \tag{3.39}$$

$$\overline{i^2_{\text{n,m16}}} = 4KT\frac{\gamma_{16}}{\alpha_{16}}g_{\text{m16}} \tag{3.40}$$

$$\overline{i^2_{\text{n,m17}}} = 4KT\frac{\gamma_{17}}{\alpha_{17}}g_{\text{m17}} \tag{3.41}$$

$$\overline{i^2_{\text{n,m18}}} = 4KT\frac{\gamma_{18}}{\alpha_{18}}g_{\text{m18}} \tag{3.42}$$

$$\overline{i^2_{\text{n,r}_\text{F}}} = 4KT\frac{1}{R_\text{F}} \tag{3.43}$$

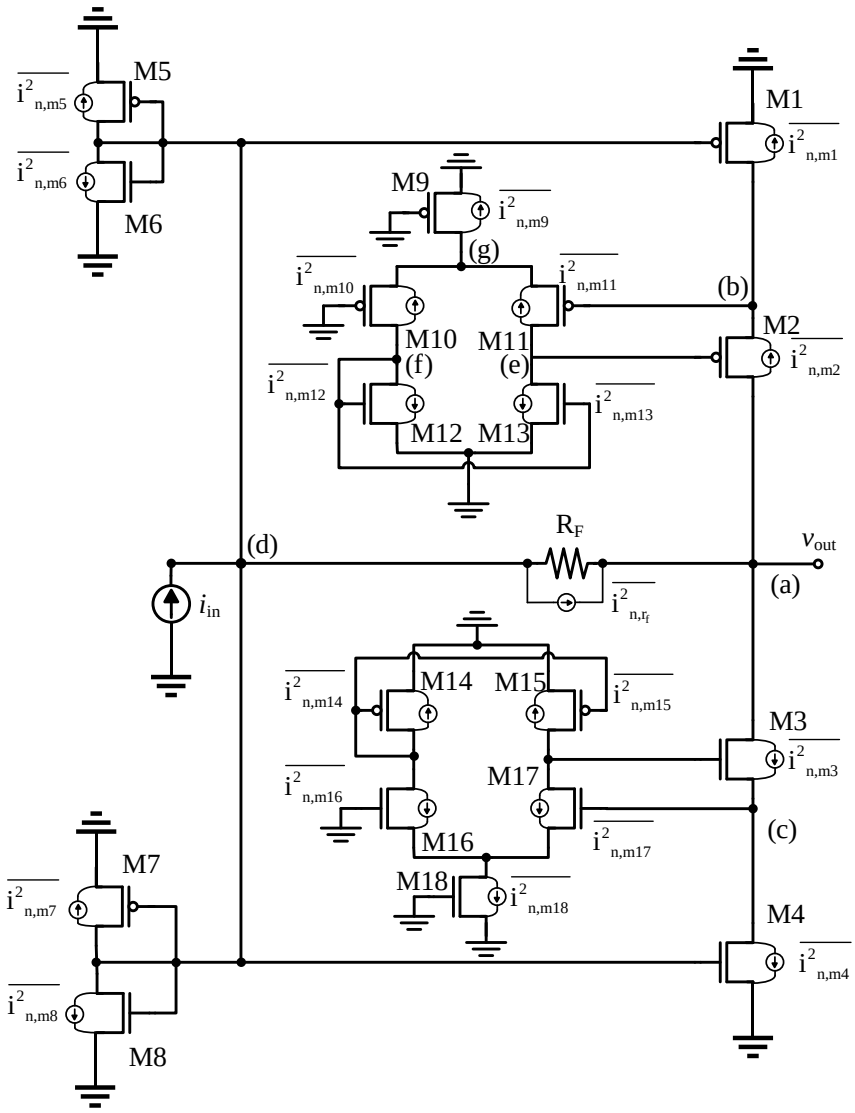



Fig. 3.12 Noise inserted (noise perturbed) circuit diagram of CMOS $g_m$-boosted Inv-Cas TIA.

Next, the noise current arriving at point (a) splits into two equal components $\frac{\sqrt{\overline{i^2_{n,r_F}}}}{2}$, so the noise current power spectral density due to $R_f$ at the drain of M2 is given by,

$$\left(\frac{\sqrt{\overline{i^2_{n,r_F}}}}{2}\right)^2 = \frac{\overline{i^2_{n,r_F}}}{4} \tag{3.44}$$

For common gate devices, the current noise produced by the load at the drain can be referred to the source directly. But their drain current noise cannot be referred to the source input directly; it is referred as voltage noise power to the gate node [62]. Since M2 is the common-gate stage of the cascode, this can be referred to the source of M2 at point (b). And the noise voltage power spectral density referred to the gate M2 at point (e) is given by,

$$\overline{v^2_{\text{n,in-e}}} = \overline{i^2_{n,m2}}\left(\frac{1}{g_{\text{m2}}}\right)^2 \tag{3.45}$$

Thus, the input referred noise power current spectral density across M11 can be written as,

$$\overline{i^2_{\text{n,in-e}}} = \overline{v^2_{\text{n,in-e}}}(2\pi f)^2(C_{\text{gd11}} + C_{\text{db11}} + C_{\text{gd13}} + C_{\text{db13}})^2 \tag{3.46}$$

Similarly, the noise voltage power spectral density referred to M12 and M13 at point (f) is given by,

$$\overline{v^2_{\text{n,in-f}}} = \overline{i^2_{n,m12}}\left(\frac{1}{g_{\text{m12}}}\right)^2 + \overline{i^2_{n,m13}}\left(\frac{1}{g_{\text{m13}}}\right)^2 \tag{3.47}$$

And noise current power spectral density referred to the source of M10 can be found by,

$$\overline{i^2_{\text{n,in-f}}} = \overline{v^2_{\text{n,in-f}}}(2\pi f)^2(C_{\text{gd10}} + C_{\text{db10}} + C_{\text{gd12}} + C_{\text{db12}})^2 \tag{3.48}$$

Hence, the total input referred noise current power spectral density at point (g) is the sum of the noise current at point (e), (f) and M9,

$$\overline{i^2_{\text{n,in-g}}} = \overline{i^2_{\text{n,in-e}}} + \overline{i^2_{\text{n,in-f}}} + \overline{i^2_{\text{n,in-9}}} \tag{3.49}$$

Accordingly, the total noise voltage and current power spectral density referred to the gate of M11 at point (b) is given by,

$$\overline{v^2_{\text{n,in-b}}} = \overline{i^2_{\text{n,in-g}}}\left(\frac{1}{g_{\text{m10}}} + \frac{1}{g_{\text{m11}}}\right)^2 + \overline{i^2_{\text{n,m11}}}\left(\frac{1}{g_{\text{m11}}}\right)^2 \tag{3.50}$$

$$\overline{i^2_{\text{n,in-b}}} = \frac{\overline{i^2_{\text{n,r}_\text{f}}}}{4} + \overline{v^2_{\text{n,in-b}}}\left(2\pi f\right)^2(C_{\text{gd1}} + C_{\text{db1}} + C_{\text{gs2}} + C_{\text{bs2}})^2 \tag{3.51}$$

The input referred noise of the bottom half circuit can be found in the same way as mentioned above. Thus, the total input referred noise voltage and current power spectral density at point (d) are given by,

$$\begin{aligned}\overline{v^2_{\text{n,in-d}}} = {} & \overline{i^2_{\text{n,m5}}}\left(\frac{1}{g_{\text{m5}}}\right)^2 + \overline{i^2_{\text{n,m6}}}\left(\frac{1}{g_{\text{m6}}}\right)^2 + \overline{i^2_{\text{n,in-b}}}\left(\frac{1}{g_{\text{m1}}}\right)^2 + \overline{i^2_{\text{n,m1}}}\left(\frac{1}{g_{\text{m1}}}\right)^2 \\ & + \overline{i^2_{\text{n,in-c}}}\left(\frac{1}{g_{\text{m4}}}\right)^2 + \overline{i^2_{\text{n,m4}}}\left(\frac{1}{g_{\text{m4}}}\right)^2 + \overline{i^2_{\text{n,r}_\text{f}}}\left(R_{\text{F}}\right)^2\end{aligned} \tag{3.52}$$

$$\overline{i^2_{\text{n,in-d}}} = \overline{v^2_{\text{n,in-d}}}\left(2\pi f\right)^2 (C_{\text{gs5}} + C_{\text{db5}} + C_{\text{gs6}} + C_{\text{db6}} + C_{\text{gs8}} + C_{\text{db8}} + C_{\text{gs7}} + C_{\text{db7}} + C_{\text{gs1}} + C_{\text{gd1}} + C_{\text{gs4}} + C_{\text{gd4}})^2 \tag{3.53}$$

## 3.4 Simulation Results

Fig. 3.13 shows the transient sinusoidal response of proposed $g_{\text{m}}$-boosted Inv-Cas TIA for a nominal 5 kHz input signal. As shown in this figure, the peak-to-peak output voltage swing is around 28mV for a test input current of 1nA.

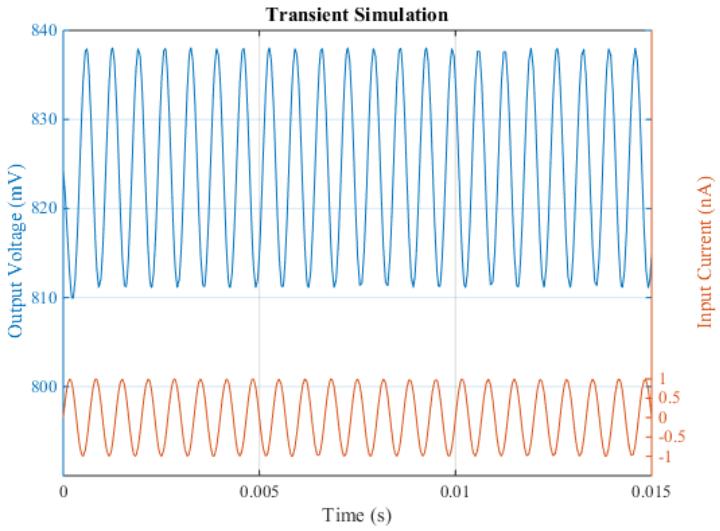



Fig. 3.13 A transient analyses simulation of $g_{\text{m}}$-boosted Inv-Cas TIA.

Fig. 3.14 shows that transimpedance gain of $g_{\text{m}}$-boosted Inv-Cas TIA with the transimpedance gain is around 145.8 dB and the -3 dB bandwidth is 5.31 kHz.

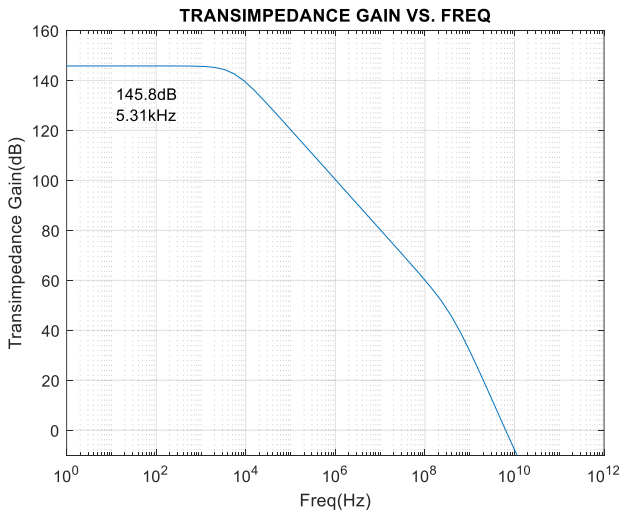



Fig. 3.14 AC analysis simulation of $g_{\text{m}}$-boosted Inv-Cas TIA.

Fig. 3.15 indicates the input referred noise current spectral density of $g_m$-boosted Inv-Cas TIA and the average output noise current spectral density is 4.23pA/sqrt(Hz) within the TIA bandwidth.

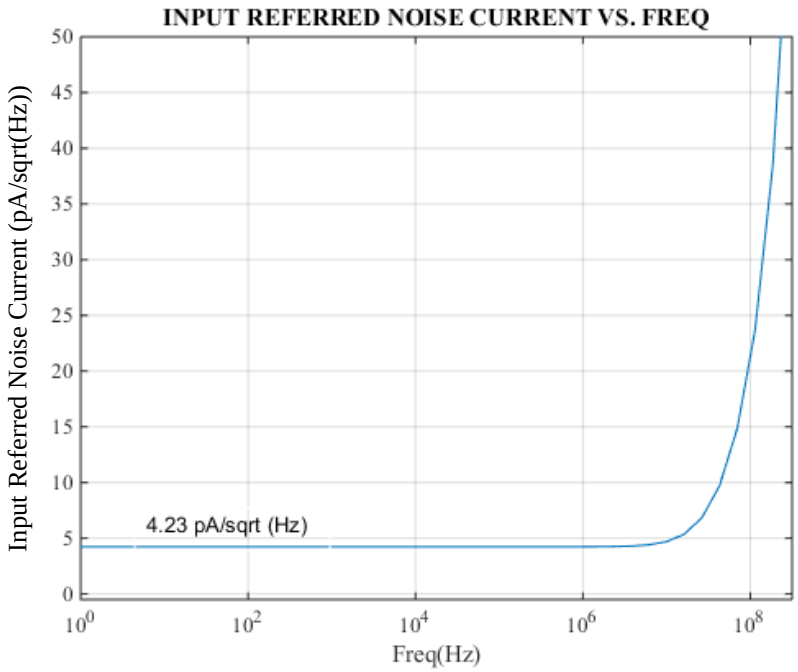



Fig. 3.15 Input referred noise current spectral density of $g_m$-boosted Inv-Cas TIA.

Fig. 3.16 shows the Eye diagram simulation using a -133dBm input current signal and a $2^{31}$-1 pseudo random bit sequence (PRBS) data pattern. The result displays an eye opening of 90% at 3 kbit/s.

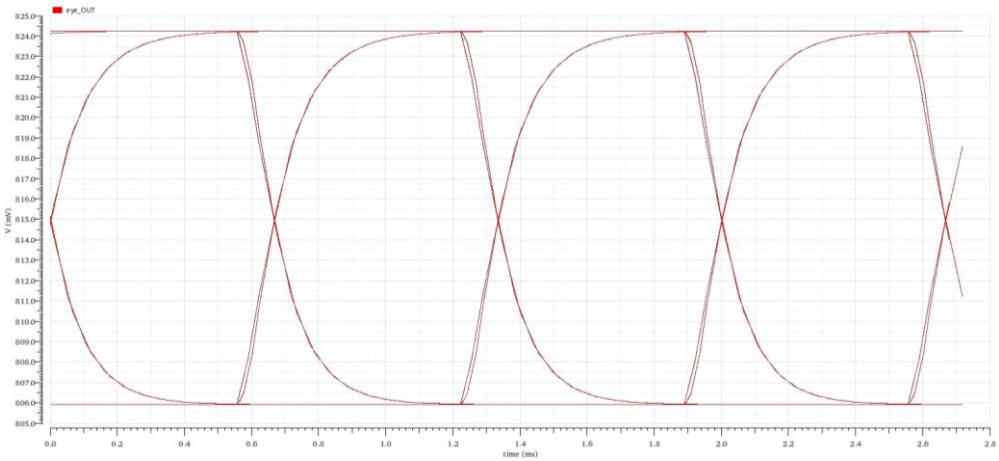


Fig. 3.16 Eye diagrams of $g_m$-boosted Inv-Cas TIA.

## 3.5 Layout

The layout design of the proposed $g_m$-boosted Inv-Cas TIA is presented in Fig. 3.17 which occupies 23.5 × 30.7 μm$^2$ of silicon area.

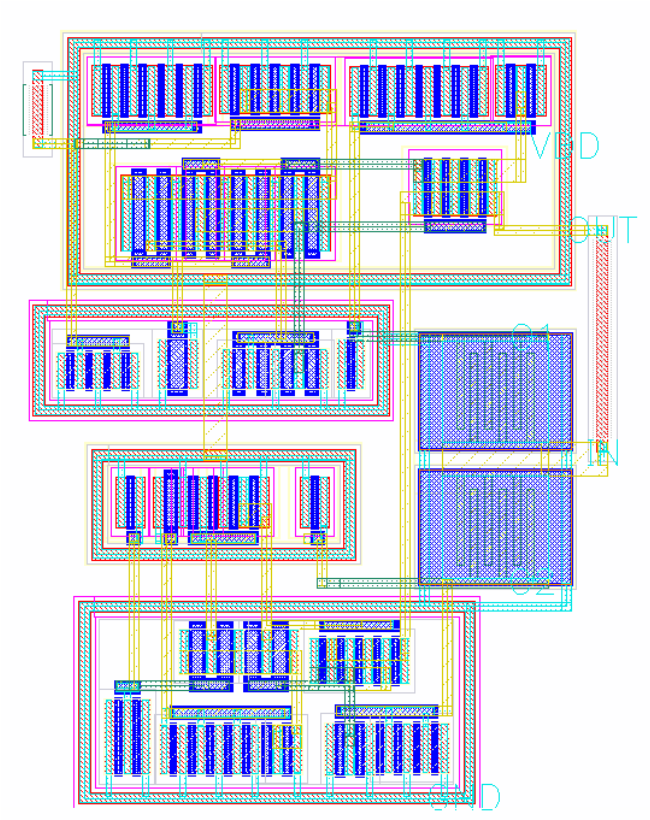



Fig. 3.17 Layout of $g_m$-boosted Inv-Cas TIA.

# Chapter 4 $g_m$-boosted Folded Regulated Inverter Cascode Transimpedance Amplifier

This chapter discusses a novel $g_m$-boosted folded regulated inverter cascode TIA ($g_m$-boosted RIC TIA) using quasi-floating gate (QFG) design. Theoretical analysis such as its gain and noise analysis are developed. And the simulation analysis shows the transimpedance gain is 145.5 dB with a -3 dB bandwidth of 5.4 kHz. The input referred noise current spectral density is below 8 pA/sqrt (Hz). Eye diagram simulation using -123dBm input photodiode current signal and a $2^{31}$-1 pseudo random bit sequence data pattern shows an eye opening of 95% at 3 kbit/s.

## 4.1 Topology of $g_m$-boosted RIC TIA

The schematic diagram and biasing circuit of the proposed $g_m$-boosted RIC TIA using QFG are shown in Fig. 4.2 and Fig. 4.1, respectively. Compared with $g_m$-boosted Inv-Cas TIA, the proposed $g_m$-boosted RIC TIA is the regulation of M2, M3 and M6, M7. Consequently, the transconductance of these transistors is increased by the gain of $g_m$-boosters "A1", "A2", "A5" and "A6". Additionally, two differential amplifiers with gain "A3" and "A4" are added to boost the transconductance of $g_m$-boosters "A5" and "A6" respectively.

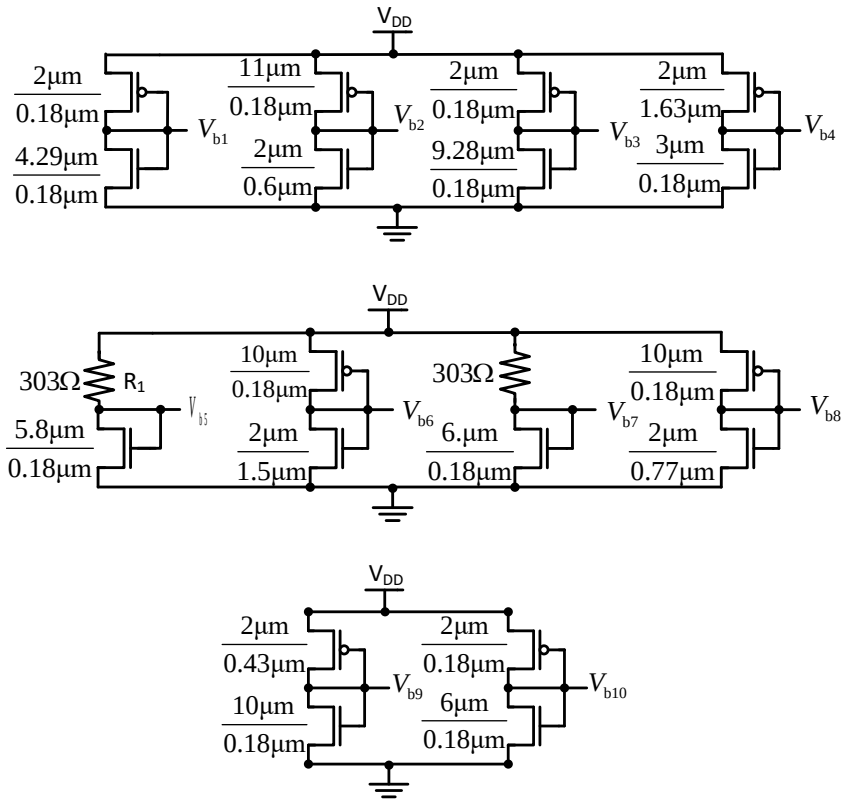



Fig. 4.1 Biasing circuit of $g_m$-boosted RIC TIA.

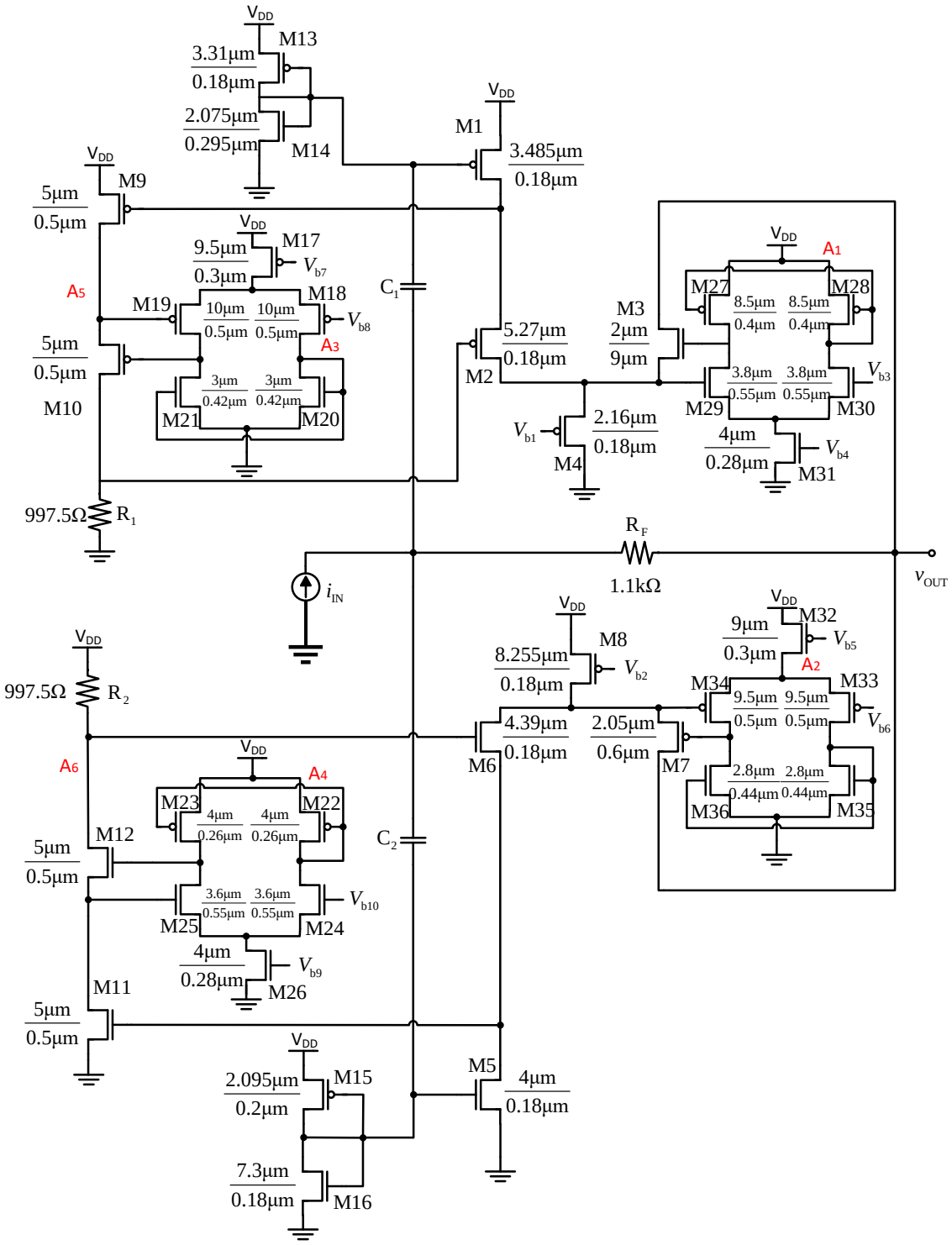



Fig. 4.2 Schematic of proposed $g_m$-boosted RIC TIA.

## 4.2 Analysis of Mid-band Transimpedance Gain

The open-loop mid-band gain $g_m$-boosted RIC TIA can be derived from Fig. 4.3 which shows the open-loop small-signal circuit with bias voltage and power supply at AC ground. Four differential amplifiers are replaced by triangle symbols "$A_1$", "$A_2$", "$A_3$" and "$A_4$". Furthermore, the capacitances act as a short circuit for mid-band transimpedance behaviour. And the feedback factor β is given by,

$$\beta = \frac{1}{R_F} \tag{4.01}$$

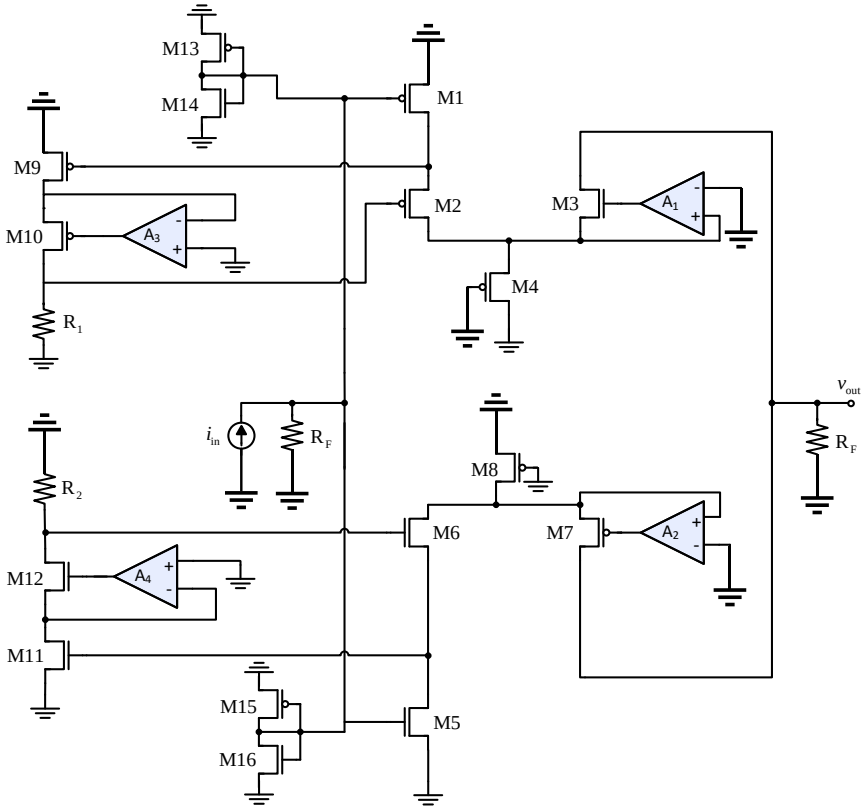



Fig. 4.3 Open-loop AC equivalent circuit of $g_m$-boosted RIC TIA.

Similarly, the small-signal analysis can be simplified by using the double short-circuit method to find out the composite transconductance $G_m$ of the $g_m$-boosted NMOS telescopic cascode [48]. Firstly, the output of $g_m$-boosted NMOS telescopic cascode with gate $g_{12}$ at a small signal voltage of $-A_4 v_y$ is AC shorted as shown in Fig. 4.4 and $R_2$ is shorted as well. In addition, the current flows into the negative terminal of a differential amplifier with gain "$A_4$" are almost negligible because the input impedance of it is very high [57]. From the previous small-signal analysis of $g_m$-boosted Inv-Cas TIA, the transconductance $G_m$ of $g_m$-boosted NMOS telescopic cascode can be written directly as,

$$G_{m1} = -\frac{g_{m11} r_{o11} \left\{ \left[ (A_4 + 1) g_{m12} + g_{mb12} \right] r_{o12} + 1 \right\}}{r_{o11} + r_{o11} \left[ (A_4 + 1) g_{m12} + g_{mb12} \right] r_{o12} + r_{o12}} \tag{4.02}$$

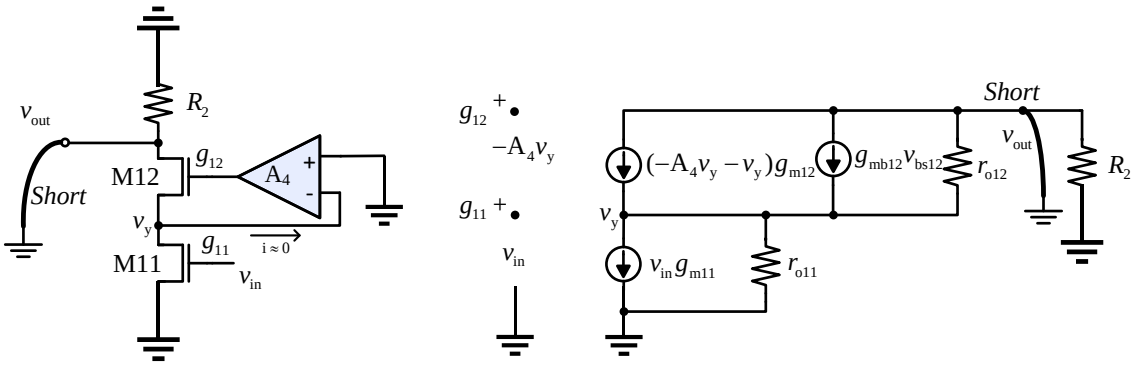



Fig. 4.4 Output short circuit analysis for $g_m$-boosted NMOS telescopic cascode.

To determine the $R_{out}$, Fig. 4.5 shows the AC equivalent circuit for $g_m$-boosted NMOS telescopic casecode with input AC ground shorted [57].

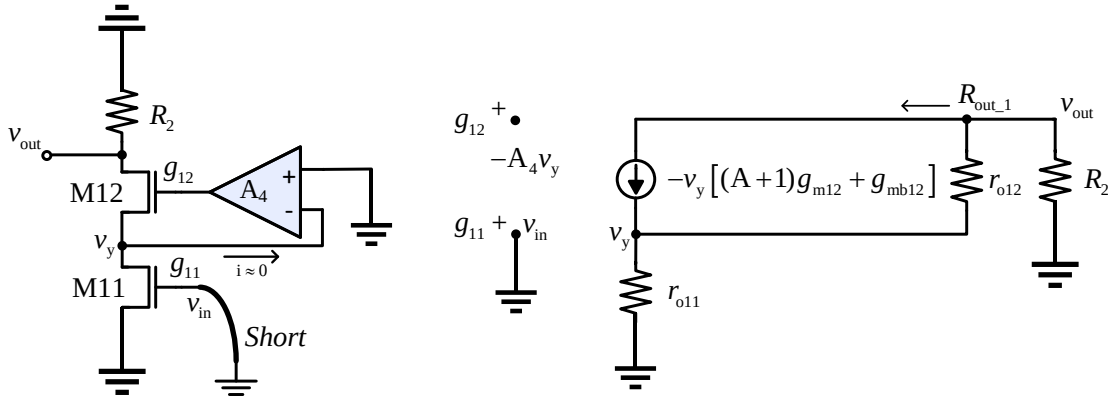



Fig. 4.5 Input short circuit analysis for $g_m$-boosted NMOS telescopic cascode.

From it, the value of output impedance $R_{out1}$ can be found as $R_{out\_1}$ and $R_2$ in parallel

$$R_{out1} = R_{out\_1} \,||\, R_2 \tag{4.03}$$

Following the same procedure for equation (3.11), the output impedance $R_{out1}$ is given by,

$$R_{out1} = \left\{ r_{o11} + r_{o11} \left[ (A_4 + 1) g_{m12} + g_{mb12} \right] r_{o12} + r_{o12} \right\} || \, R_2 \tag{4.04}$$

Then, the mid-band voltage gain $A_{v1}$ is determined by the product of equation (4.02) and (4.04) as,

$$v_{out} = v_{in} G_{m1} R_{out1} \tag{4.05}$$

After rationalizing,

$$A_{v1} = G_{m1} R_{out1} \tag{4.06}$$

Fig. 4.6 shows a $g_m$-boosted PMOS telescopic cascode structure, which is a reversal of the NMOS telescopic cascode in Fig. 3.5. Here, follow the same rule and in similarity with equations (4.02) and (4.04), the transconductance $G_{m2}$ and impedance $R_{out2}$ are given by,

$$G_{m2} = -\frac{g_{m9}r_{o9}\left\{\left[(A_3+1)g_{m10}+g_{mb10}\right]r_{o10}+1\right\}}{r_{o9}+r_{o9}\left[(A_3+1)g_{m10}+g_{mb10}\right]r_{o10}+r_{o10}} \tag{4.07}$$

$$R_{out2} = \left\{r_{o9}+r_{o9}\left[(A_3+1)g_{m10}+g_{mb10}\right]r_{o10}+r_{o10}\right\} \| R_{10} \tag{4.08}$$

$$A_{v2} = G_{m2}R_{out2} \tag{4.09}$$

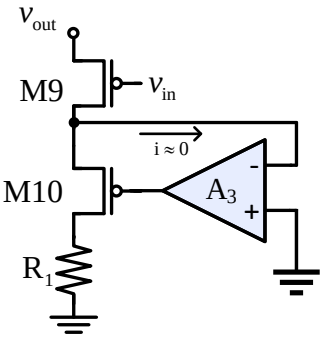



Fig. 4.6 AC equivalent circuit for $g_m$-boosted PMOS telescopic cascode.

Next, the whole structure of the $g_m$-boosted amplifier with gain "$A_5$" and "$A_6$" in Fig. 4.2 can be seen as two differential amplifiers with mid-band gain "$A_{v2}$" and "$A_{v1}$" respectively. To simplify the circuits, they are replaced by triangle symbols. Thus, the simplified left part of the proposed $g_m$-boosted RIC TIA can be illustrated in Fig. 4.7. Fig. 4.7 (a) shows the $g_m$-boosted PMOS cascode structure and its transconductance $G_{m3}$ and output impedance $R_{out3}$ are given by,

$$G_{m3} = -\frac{g_{m1}r_{o1}\left\{\left[(A_{v2}+1)g_{m2}+g_{mb2}\right]r_{o2}+1\right\}}{r_{o1}+r_{o1}\left[(A_{v2}+1)g_{m2}+g_{mb2}\right]r_{o2}+r_{o2}} \tag{4.10}$$

$$R_{out3} = r_{o1}+r_{o1}\left[(A_{v2}+1)g_{m2}+g_{mb2}\right]r_{o2}+r_{o2} \tag{4.11}$$

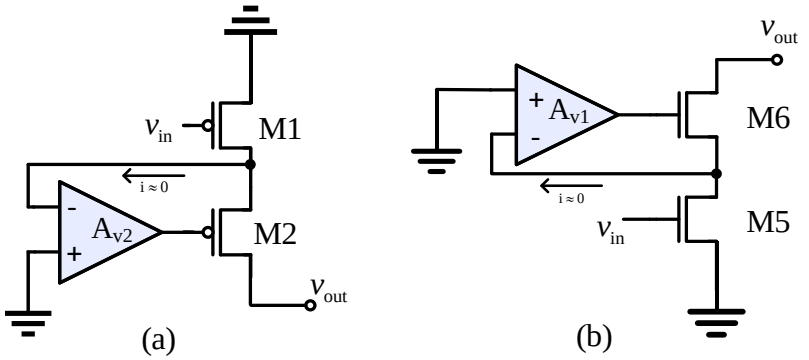



Fig. 4.7 Simplified AC equivalent circuit for left parts of $g_m$-boosted RIC TIA, (a) $g_m$-boosted PMOS cascode, (b) $g_m$-boosted NMOS cascode.

Fig. 4.7 (b) shows the $g_m$-boosted NMOS cascode structure and its transconductance $G_{m4}$ and output impedance $R_{out4}$ are given by,

$$G_{m4} = -\frac{g_{m5}r_{o5}\left\{\left[(A_{v1}+1)g_{m6}+g_{mb6}\right]r_{o6}+1\right\}}{r_{o5}+r_{o5}\left[(A_{v1}+1)g_{m6}+g_{mb6}\right]r_{o6}+r_{o6}} \tag{4.12}$$

$$R_{out4} = r_{o5}+r_{o5}\left[(A_{v1}+1)g_{m6}+g_{mb6}\right]r_{o6}+r_{o6} \tag{4.13}$$

As discussed in equations (3.02) and (3.03), the equivalent small-signal circuit of the bias circuit is shown in Fig. 3.8. And similarly, the impedances of bias circuits are given by,

$$R_{eq\_bias1} = \frac{1}{\frac{1}{g_{m13}}+\frac{1}{g_{m14}}} \tag{4.14}$$

$$R_{eq\_bias2} = \frac{1}{\frac{1}{g_{m15}}+\frac{1}{g_{m16}}} \tag{4.15}$$

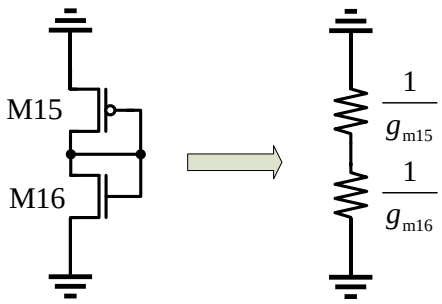



Fig. 4.8 Small signal for bias circuit.

Then, the input signal circuit of the proposed $g_m$-boosted RIC TIA is simplified in Fig. 4.9 and the input voltage can be written as,

$$v_{in} = i_{in}\left(R_{eq\_bias1} \,||\, R_{eq\_bias2} \,||\, R_F\right) \tag{4.16}$$

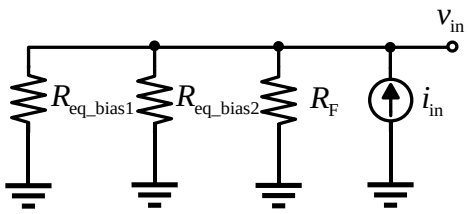



Fig. 4.9 Simplified input circuits.

Next, put the transconductance $G_{m3}$, $G_{m4}$ and output impedance $R_{out3}$, $R_{out4}$ back to the whole small-signal equivalent circuit of proposed $g_m$-boosted RIC TIA as shown in Fig. 4.10.

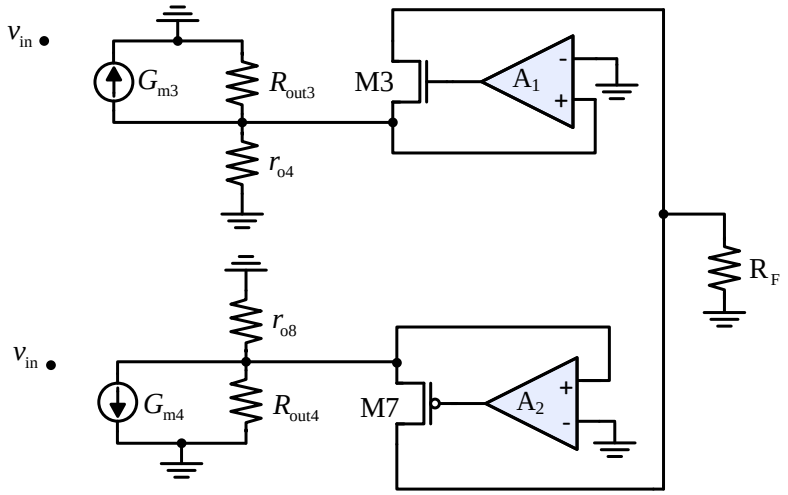



Fig. 4.10 Reduced form of the small-signal equivalent circuits for proposed $g_m$-boosted RIC TIA.

Since a dependent current source due to a voltage across itself can be replaced by a simple resistor [56]-[58], the left part in Fig. 4.10 is represented by equivalent composite transistors with transconductance $G_{m3}$, $G_{m4}$ and output impedance $\left(R_{out3} \| r_{o4}\right)$ and $\left(R_{out4} \| r_{o8}\right)$ as shown in Fig. 4.11.

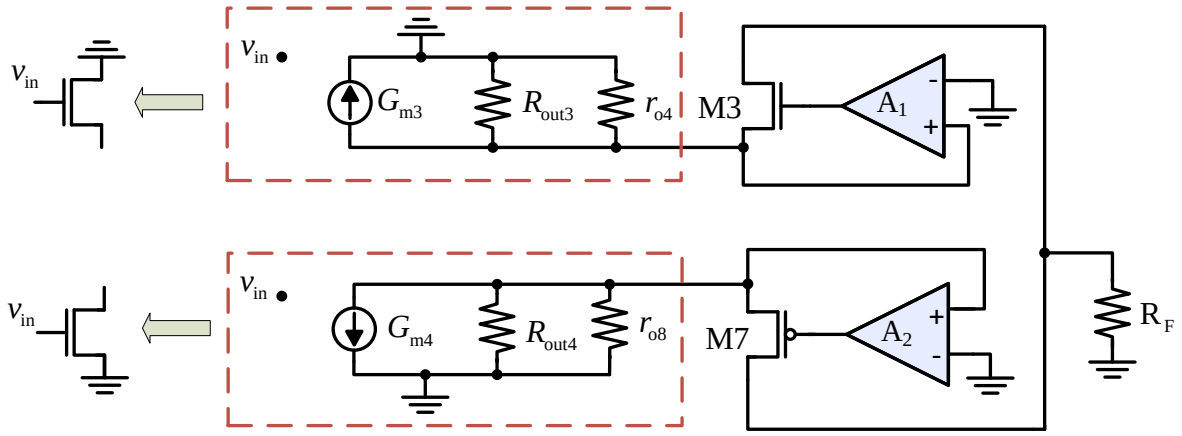



Fig. 4.11 Highly simplified small-signal equivalent circuits for proposed $g_m$-boosted RIC TIA.

Fig. 4.12 shows the equivalent circuit of $g_m$-boosted NMOS and PMOS cascode structure using a composite transistor model with transconductance $G_{m3}$, $G_{m4}$ and output impedance $(R_{out3} \| r_{o4})$ and $(R_{out4} \| r_{o8})$ respectively, so that, following the same approach as equation (4.02) and (4.04), the transconductance and output impedance are given by,

$$G_{m5} = -\frac{G_{m1}(R_{out1} \| r_{o4})\{[(A_1+1)g_{m3} + g_{mb3}]r_{o3}+1\}}{(R_{out1} \| r_{o4}) + (R_{out1} \| r_{o4})[(A_1+1)g_{m3} + g_{mb3}]r_{o3} + r_{o3}} \tag{4.17}$$

$$R_{out5} = (R_{out1} \| r_{o4}) + (R_{out1} \| r_{o4})[(A_1+1)g_{m3} + g_{mb3}]r_{o3} + r_{o3} \tag{4.18}$$

$$G_{m6} = -\frac{G_{m2}(R_{out2} \| r_{o8})\{[(A_2+1)g_{m7} + g_{mb7}]r_{o7}+1\}}{(R_{out2} \| r_{o8}) + (R_{out2} \| r_{o8})[(A_2+1)g_{m7} + g_{mb7}]r_{o7} + r_{o7}} \tag{4.19}$$

$$R_{out6} = (R_{out2} \| r_{o8}) + (R_{out2} \| r_{o8})[(A_2+1)g_{m7} + g_{mb7}]r_{o7} + r_{o7} \tag{4.20}$$

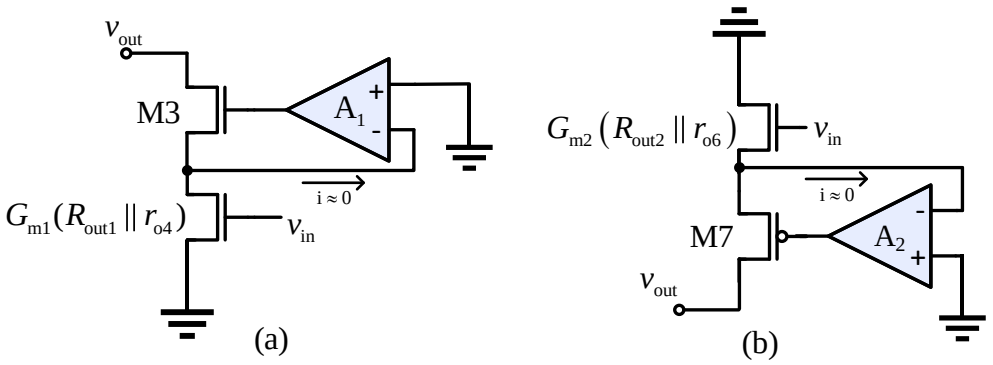



Fig. 4.12 Simplified small-signal model of $g_m$-boosted (a) NMOS and (b) PMOS cascode structure.

Here, the final reduced form of proposed $g_m$-boosted TIC TIA is presented in Fig. 4.13. And the output voltage is given by,

$$v_{out} = -v_{in}(G_{m5} + G_{m6})(R_{out5} \| R_{out6} \| R_F) \tag{4.21}$$

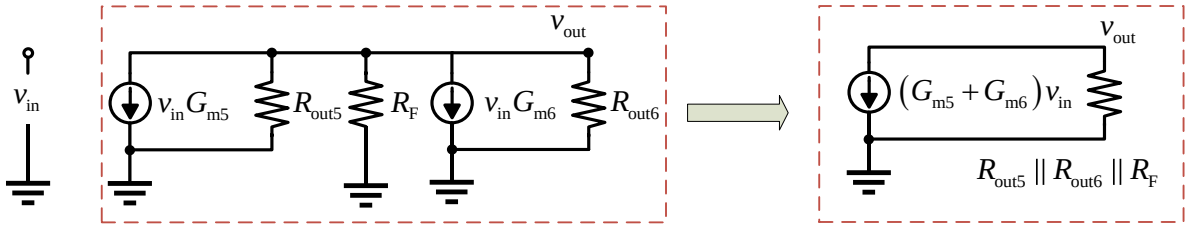



Fig. 4.13 Final reduced form of proposed $g_m$-boosted RIC TIA.

The open-loop gain of the proposed $g_m$-boosted RIC TIA is given by,

$$Z_{open} = \frac{v_{out}}{i_{in}} \tag{4.22}$$

From equation (4.16) and (4.21), the open-loop is now given by,

$$Z_{\text{open}} = \frac{-v_{\text{in}}(G_{\text{m5}} + G_{\text{m6}})(R_{\text{out5}} \parallel R_{\text{out6}} \parallel R_{\text{F}})}{\frac{v_{\text{in}}}{(R_{\text{eq\_bias1}} \parallel R_{\text{eq\_bias2}} \parallel R_{\text{F}})}} \tag{4.23}$$

After simplifying,

$$Z_{\text{open}} = \frac{(G_{\text{m5}} + G_{\text{m6}})(R_{\text{out5}} \parallel R_{\text{out6}} \parallel R_{\text{F}})}{R_{\text{eq\_bias1}} \parallel R_{\text{eq\_bias2}} \parallel R_{\text{F}}} \tag{4.24}$$

Where the composite trans-conductance $G_{\text{m5}}$, $G_{\text{m6}}$, the composite output impedance $R_{\text{out5}}$, Rout6 and equivalent resistor $R_{\text{eq\_bias1}}$ and $R_{\text{eq\_bias2}}$ are derivatised in previous equations.

Finally, the feedback factor β is discussed in equation (4.01) and then the closed-loop transimpedance gain of the proposed $g_{\text{m}}$-boosted RIC TIA can be quantified by,

$$\begin{aligned} Z_{\text{closed}} &= \frac{Z_{\text{open}}}{1+\beta Z_{\text{open}}} \\ &= \frac{\frac{(G_{\text{m5}} + G_{\text{m6}})(R_{\text{out5}} \parallel R_{\text{out6}} \parallel R_{\text{F}})}{R_{\text{eq\_bias1}} \parallel R_{\text{eq\_bias2}} \parallel R_{\text{F}}}}{1+\frac{1}{R_{\text{F}}}\frac{(G_{\text{m5}} + G_{\text{m6}})(R_{\text{out5}} \parallel R_{\text{out6}} \parallel R_{\text{F}})}{R_{\text{eq\_bias1}} \parallel R_{\text{eq\_bias2}} \parallel R_{\text{F}}}} \\ &== \frac{R_{\text{F}}(G_{\text{m5}} + G_{\text{m6}})(R_{\text{out5}} \parallel R_{\text{out6}} \parallel R_{\text{F}})}{R_{\text{F}}(R_{\text{out5}} \parallel R_{\text{out6}} \parallel R_{\text{F}}) + (G_{\text{m5}} + G_{\text{m6}})(R_{\text{out5}} \parallel R_{\text{out6}} \parallel R_{\text{F}})} \end{aligned} \tag{4.25}$$

## 4.3 Input Referred Noise Analysis

In this analysis, thermal noise is the only consideration, and shot noise as well as flicker noise is ignored. Fig. 4.14 shows the noise inserted (noise perturbed) circuit diagram for the proposed $g_{\text{m}}$-boosted RIC TIA [62], [63]. Following the same principle in equation (3.23) and (3.24), the noise current power density of MOSFETs and resistors in Fig. 4.24 is given by,

$$\overline{i^2_{\text{n,m1}}} = 4KT\frac{\gamma_1}{\alpha_1}g_{\text{m1}} \tag{4.26}$$

$$\overline{i^2_{\text{n,m2}}} = 4KT\frac{\gamma_2}{\alpha_2}g_{\text{m2}} \tag{4.27}$$

$$\overline{i^2_{\text{n,m3}}} = 4KT\frac{\gamma_3}{\alpha_3}g_{\text{m3}} \tag{4.28}$$

$$\overline{i^2_{\text{n,m4}}} = 4KT\frac{\gamma_4}{\alpha_4}g_{\text{m4}} \tag{4.29}$$

$$\overline{i^2_{n,m5}} = 4KT\frac{\gamma_5}{\alpha_5}g_{m5} \tag{4.30}$$

$$\overline{i^2_{n,m6}} = 4KT\frac{\gamma_6}{\alpha_6}g_{m6} \tag{4.31}$$

$$\overline{i^2_{n,m7}} = 4KT\frac{\gamma_7}{\alpha_7}g_{m7} \tag{4.32}$$

$$\overline{i^2_{n,m8}} = 4KT\frac{\gamma_8}{\alpha_8}g_{m8} \tag{4.33}$$

$$\overline{i^2_{n,m9}} = 4KT\frac{\gamma_9}{\alpha_9}g_{m9} \tag{4.34}$$

$$\overline{i^2_{n,m10}} = 4KT\frac{\gamma_{10}}{\alpha_{10}}g_{m10} \tag{4.35}$$

$$\overline{i^2_{n,m11}} = 4KT\frac{\gamma_{11}}{\alpha_{11}}g_{m11} \tag{4.36}$$

$$\overline{i^2_{n,m12}} = 4KT\frac{\gamma_{12}}{\alpha_{12}}g_{m12} \tag{4.37}$$

$$\overline{i^2_{n,m13}} = 4KT\frac{\gamma_{13}}{\alpha_{13}}g_{m13} \tag{4.38}$$

$$\overline{i^2_{n,m14}} = 4KT\frac{\gamma_{14}}{\alpha_{14}}g_{m14} \tag{4.39}$$

$$\overline{i^2_{n,m15}} = 4KT\frac{\gamma_{15}}{\alpha_{15}}g_{m15} \tag{4.40}$$

$$\overline{i^2_{n,m16}} = 4KT\frac{\gamma_{16}}{\alpha_{16}}g_{m16} \tag{4.41}$$

$$\overline{i^2_{n,m17}} = 4KT\frac{\gamma_{17}}{\alpha_{17}}g_{m17} \tag{4.42}$$

$$\overline{i^2_{n,m18}} = 4KT\frac{\gamma_{18}}{\alpha_{18}}g_{m18} \tag{4.43}$$

$$\overline{i^2_{n,m18}} = 4KT\frac{\gamma_{19}}{\alpha_{19}}g_{m19} \tag{4.44}$$

$$\overline{i^2_{n,m18}} = 4KT\frac{\gamma_{20}}{\alpha_{20}}g_{m20} \tag{4.45}$$

$$\overline{i^2_{\text{n,m18}}} = 4KT\frac{\gamma_{21}}{\alpha_{21}}g_{\text{m21}} \tag{4.46}$$

$$\overline{i^2_{\text{n,m18}}} = 4KT\frac{\gamma_{22}}{\alpha_{22}}g_{\text{m22}} \tag{4.47}$$

$$\overline{i^2_{\text{n,m18}}} = 4KT\frac{\gamma_{23}}{\alpha_{23}}g_{\text{m23}} \tag{4.48}$$

$$\overline{i^2_{\text{n,m18}}} = 4KT\frac{\gamma_{24}}{\alpha_{24}}g_{\text{m24}} \tag{4.49}$$

$$\overline{i^2_{\text{n,m18}}} = 4KT\frac{\gamma_{25}}{\alpha_{25}}g_{\text{m25}} \tag{4.50}$$

$$\overline{i^2_{\text{n,m18}}} = 4KT\frac{\gamma_{26}}{\alpha_{26}}g_{\text{m26}} \tag{4.51}$$

$$\overline{i^2_{\text{n,m18}}} = 4KT\frac{\gamma_{27}}{\alpha_{27}}g_{\text{m27}} \tag{4.52}$$

$$\overline{i^2_{\text{n,m18}}} = 4KT\frac{\gamma_{28}}{\alpha_{28}}g_{\text{m28}} \tag{4.53}$$

$$\overline{i^2_{\text{n,m18}}} = 4KT\frac{\gamma_{29}}{\alpha_{29}}g_{\text{m29}} \tag{4.54}$$

$$\overline{i^2_{\text{n,m18}}} = 4KT\frac{\gamma_{30}}{\alpha_{30}}g_{\text{m30}} \tag{4.55}$$

$$\overline{i^2_{\text{n,m18}}} = 4KT\frac{\gamma_{31}}{\alpha_{31}}g_{\text{m31}} \tag{4.56}$$

$$\overline{i^2_{\text{n,m18}}} = 4KT\frac{\gamma_{32}}{\alpha_{32}}g_{\text{m32}} \tag{4.57}$$

$$\overline{i^2_{\text{n,m18}}} = 4KT\frac{\gamma_{33}}{\alpha_{33}}g_{\text{m33}} \tag{4.58}$$

$$\overline{i^2_{\text{n,m18}}} = 4KT\frac{\gamma_{34}}{\alpha_{34}}g_{\text{m34}} \tag{4.59}$$

$$\overline{i^2_{\text{n,m18}}} = 4KT\frac{\gamma_{35}}{\alpha_{35}}g_{\text{m35}} \tag{4.60}$$

$$\overline{i^2_{\text{n,m18}}} = 4KT\frac{\gamma_{36}}{\alpha_{36}}g_{\text{m36}} \tag{4.61}$$

$$\overline{i^2_{n,r_F}} = 4KT\frac{1}{R_F} \tag{4.62}$$

$$\overline{i^2_{n,r_1}} = 4KT\frac{1}{R_1} \tag{4.63}$$

$$\overline{i^2_{n,r_2}} = 4KT\frac{1}{R_2} \tag{4.64}$$

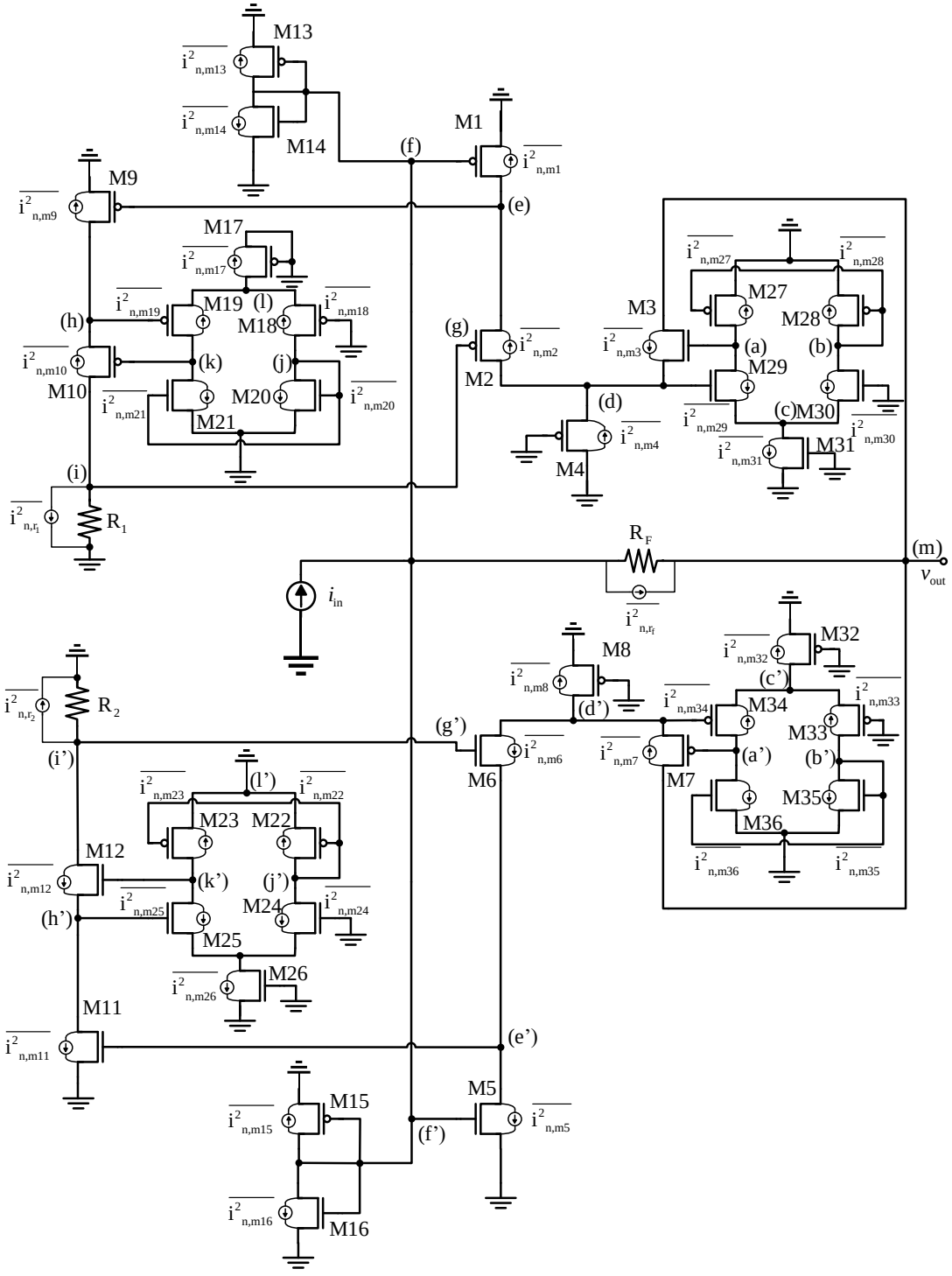



Fig. 4.14 Noise inserted (noise perturbed) circuit diagram of proposed $g_m$-boosted RIC TIA.

Next, the noise current arriving at point (a) splits into two equal components $\frac{\sqrt{\overline{i^2_{n,r_F}}}}{2}$, so the noise current power spectral density due to $R_f$ at drain of M2 is given by,

$$\left(\frac{\sqrt{\overline{i^2_{n,r_F}}}}{2}\right)^2 = \frac{\overline{i^2_{n,r_F}}}{4} \tag{4.65}$$

Next the noise voltage power spectral density referred to the gate of M3 at point (a) is given by,

$$\overline{v^2_{n,in\text{-}a}} = \frac{\overline{i^2_{n,in\text{-}a}}}{g^2_{m9}} \tag{4.66}$$

And the input referred noise current power spectral density across M29 can be written as,

$$\overline{i^2_{n,in\text{-}a}} = \overline{v^2_{n,in\text{-}a}}\left(2\pi f\right)^2\left(C_{gs3}+C_{gd3}+C_{gd27}+C_{ds27}+C_{gd29}+C_{ds29}\right)^2 \tag{4.67}$$

The input referred noise voltage power spectral density at point (b) is the sum of noise voltage power spectral density of M27 and M28 which is,

$$\overline{v^2_{n,in\text{-}b}} = \frac{\overline{i^2_{n,m27}}}{g^2_{m27}} + \frac{\overline{i^2_{n,m28}}}{g^2_{m28}} \tag{4.68}$$

Thus, the current power spectral density referred to the source of M30 at point (b) is given by,

$$\overline{i^2_{n,in\text{-}b}} = \overline{v^2_{n,in\text{-}b}}\left(2\pi f\right)^2\left(C_{gd28}+C_{db28}+C_{gd30}+C_{db30}\right)^2 \tag{4.69}$$

The input referred noise current pwoer spectral density at point (c) is the sum of the current power spectral density referred to the drain of M31 which is given by,

$$\overline{i^2_{n,in\text{-}c}} = \overline{i^2_{n,in\text{-}a}} + \overline{i^2_{n,in\text{-}b}} + \overline{i^2_{n,m31}} \tag{4.70}$$

From inspection, at point (d), the input noise voltage power spectral density can be written as,

$$\overline{v^2_{n,in\text{-}d}} = \overline{i^2_{n,in\text{-}c}}\frac{1}{\left(g_{m29}+g_{m30}\right)^2} + \frac{\overline{i^2_{n,m29}}}{g^2_{m29}} \tag{4.71}$$

And the input referred noise current power spectral density at point (d) is given by,

$$\overline{i^2_{n,in\text{-}d}} = \overline{v^2_{n,in\text{-}d}}\left(2\pi f\right)^2\left(C_{gs3}+C_{bs3}+C_{gs4}+C_{bs4}+C_{gd2}+C_{db2}\right)^2 + \overline{i^2_{n,m4}} + \frac{\overline{i^2_{n,r_f}}}{4} \tag{4.72}$$

Similar to equation (4.71) and (4.72), the input referred noise voltage power and current power spectral density referred to the gate of M10 at point (k) are given by,

$$\overline{v^2_{\text{n,in-k}}} = \frac{\overline{i^2_{\text{n,m10}}}}{g_{\text{m10}}{}^2} \tag{4.73}$$

$$\overline{i^2_{\text{n,in-k}}} = \overline{v^2_{\text{n,in-k}}}\left(2\pi f\right)^2\left(C_{\text{gd10}} + C_{\text{db10}} + C_{\text{gd21}} + C_{\text{db21}} + C_{\text{gd19}} + C_{\text{db19}}\right)^2 \tag{4.74}$$

Next, the total noise voltage and current power spectral density referred to the gate of M20 and M21 at point (j) is given by,

$$\overline{v^2_{\text{n,in-j}}} = \frac{\overline{i^2_{\text{n,m21}}}}{g_{\text{m21}}{}^2} + \frac{\overline{i^2_{\text{n,m20}}}}{g_{\text{m20}}{}^2} \tag{4.75}$$

$$\overline{i^2_{\text{n,in-j}}} = \overline{v^2_{\text{n,in-j}}}\left(2\pi f\right)^2\left(C_{\text{gd18}} + C_{\text{db18}} + C_{\text{gd20}} + C_{\text{db20}}\right)^2 \tag{4.76}$$

The total input referred noise current power spectral density at point (l) is the sum of the noise current power spectral density referred from point (k), (j) and transistor M17,

$$\overline{i^2_{\text{n,in-l}}} = \overline{i^2_{\text{n,in-k}}} + \overline{i^2_{\text{n,in-j}}} + \overline{i^2_{\text{n,m17}}} \tag{4.77}$$

Hence, the noise voltage power spectral density referred to the gate of M19 at point (h) is given by,

$$\overline{v^2_{\text{n,in-h}}} = \overline{i^2_{\text{n,in-h}}} \times \frac{1}{\left(g_{\text{m18}} + g_{\text{m19}}\right)^2} + \frac{\overline{i^2_{\text{n,m19}}}}{g_{\text{m19}}{}^2} \tag{4.78}$$

At point (i), the noise voltage power spectral density referred to the gate of M2, the drain of M9 and resistor $R_1$ is given by,

$$\overline{v^2_{\text{n,in-i}}} = \frac{\overline{i^2_{\text{n,m2}}}}{g_{\text{m2}}{}^2} + \overline{i^2_{\text{n,m19}}}R_1{}^2 \tag{4.79}$$

Accordingly, the input referred noise current power spectral density at point (i) is given by,

$$\overline{i^2_{\text{n,in-i}}} = \overline{v^2_{\text{n,in-i}}}\left[\frac{1}{R_1{}^2} + \left(2\pi f\right)^2\left(C_{\text{gd10}} + C_{\text{db10}} + C_{\text{gd2}} + C_{\text{db2}}\right)^2\right] \tag{4.80}$$

Therefore, the total input referred noise current power spectral density at point (h) can be written as,

$$\overline{i^2_{\text{n,in-h}}} = \overline{v^2_{\text{n,in-h}}}\left(2\pi f\right)^2\left(C_{\text{gs10}} + C_{\text{bs10}} + C_{\text{gd9}} + C_{\text{db9}}\right)^2 + \overline{i^2_{\text{n,in-i}}} \tag{4.81}$$

Next, the noise voltage and current power spectral density referred to the gate of M9 at point (e) is given by

$$\overline{v^2_{\text{n,in-e}}} = \frac{\overline{i^2_{\text{n,in-h}}}}{g_{\text{m9}}^2} + \frac{\overline{i^2_{\text{n,m9}}}}{g_{\text{m9}}^2} \tag{4.82}$$

$$\overline{i^2_{\text{n,in-e}}} = \overline{v^2_{\text{n,in-e}}}\left(2\pi f\right)^2\left(C_{\text{gd1}} + C_{\text{db1}} + C_{\text{gs2}} + C_{\text{bs2}}\right)^2 + \overline{i^2_{\text{n,in-d}}} \tag{4.83}$$

For the bottom half circuit, the input referred noise current power spectral density can be derived by the same procedures. And accumulating all the noise voltage power spectral densities at the input point (f),

$$\begin{aligned}\overline{v^2_{\text{n,in-f}}} &= \overline{v^2_{\text{n,in-e}}} + \overline{v^2_{\text{n,in-e'}}} + \overline{v^2_{\text{n,m1}}} + \overline{v^2_{\text{n,m5}}} + \overline{v^2_{\text{n,m13}}} + \overline{v^2_{\text{n,m14}}} + \overline{v^2_{\text{n,m15}}} + \overline{v^2_{\text{n,m16}}} \\ &= \frac{\overline{i^2_{\text{n,in-e}}}}{g_{\text{m1}}^2} + \frac{\overline{i^2_{\text{n,in-e'}}}}{g_{\text{m5}}^2} + \frac{\overline{i^2_{\text{n,m1}}}}{g_{\text{m1}}^2} + \frac{\overline{i^2_{\text{n,m5}}}}{g_{\text{m5}}^2} + \frac{\overline{i^2_{\text{n,m13}}}}{g_{\text{m13}}^2} + \frac{\overline{i^2_{\text{n,m14}}}}{g_{\text{m14}}^2} + \frac{\overline{i^2_{\text{n,m15}}}}{g_{\text{m15}}^2} + \frac{\overline{i^2_{\text{n,m16}}}}{g_{\text{m16}}^2}\end{aligned} \tag{4.84}$$

Finally, the total input referred noise current power spectral density is given by,

$$\overline{i^2_{\text{n,in-f}}} = \overline{v^2_{\text{n,in-f}}}\left[\frac{1}{R_{\text{F}}^2} + \left(2\pi f\right)^2\left(\begin{matrix}C_{\text{gd15}} + C_{\text{db15}} + C_{\text{gd16}} + C_{\text{db16}} + C_{\text{gd5}} + C_{\text{gs5}} \\ + C_{\text{gd13}} + C_{\text{db13}} + C_{\text{gd14}} + C_{\text{db14}} + C_{\text{gd1}} + C_{\text{gs1}}\end{matrix}\right)^2\right] + \overline{i^2_{\text{n,r}_{\text{F}}}} \tag{4.85}$$

## 4.4 Simulation Results

Fig. 4.15 shows the transient sinusoidal response of proposed $g_{\text{m}}$-boosted RIC TIA for a nominal 5 kHz input signal. As shown in this figure, the peak-to-peak output voltage swing is around 75mV for a test input current of 1nA.

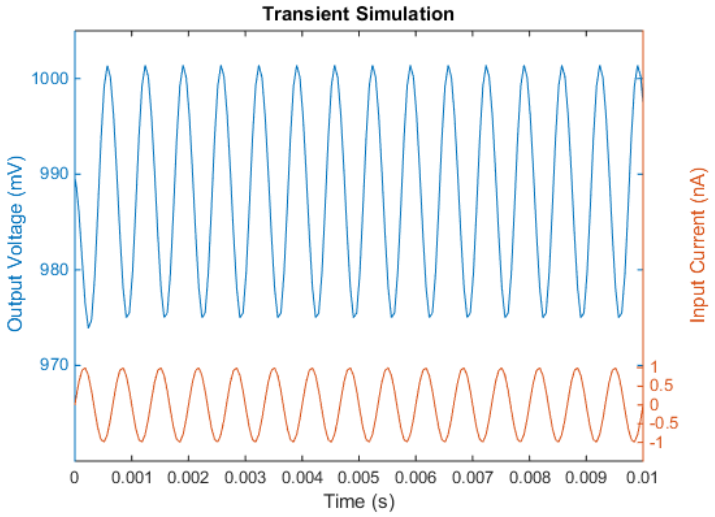



Fig. 4.15 Transient analysis simulation of $g_{\text{m}}$-boosted RIC TIA.

Fig. 4.16 shows that transimpedance gain of $g_m$-boosted RIC TIA with the magnitude of the transimpedance gain at around 73.71dB and its -3 dB bandwidth at 5.4 kHz

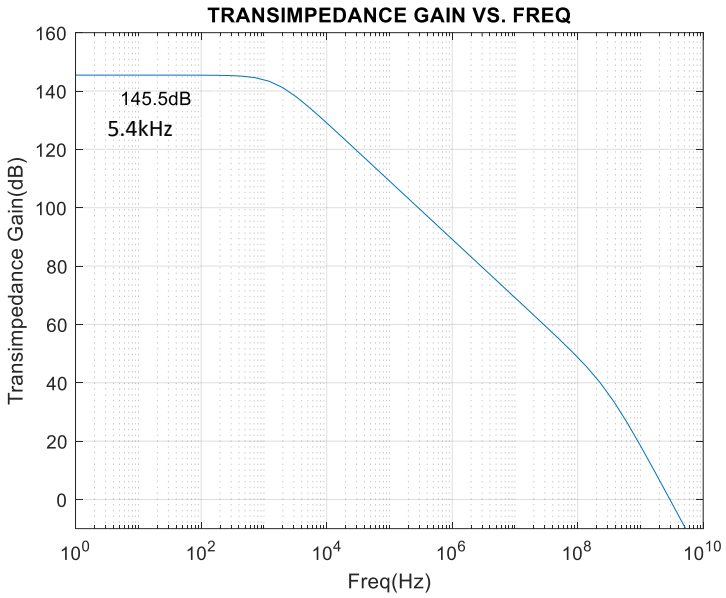



Fig. 4.16 AC analysis simulation of transimpedance gain for $g_m$-boosted RIC TIA.

Fig. 4.17 displays the input referred noise current spectral density function of $g_m$-boosted RIC TIA and the average is around 7.81 pA/sqrt (Hz) within the TIA bandwidth.

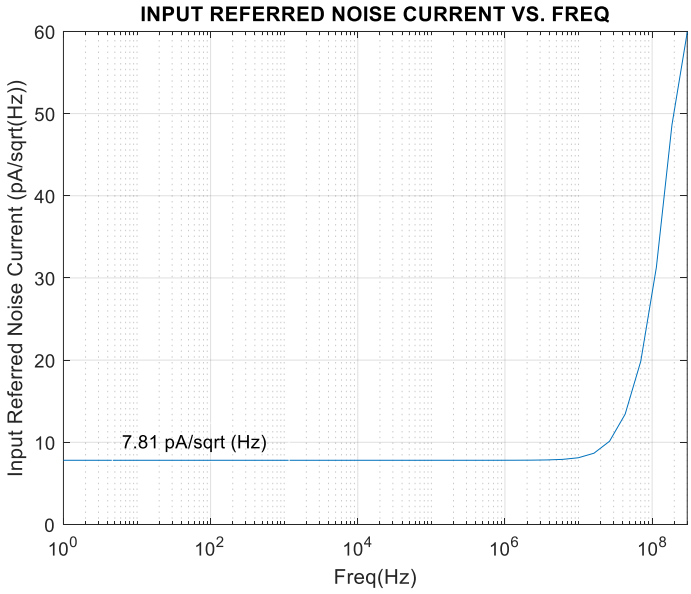



Fig. 4.17 Input referred noise current of $g_m$-boosted RIC TIA simulation result.

Fig. 4.18 shows the results of eye diagram simulations using -123 dBm input photodiode current signal and a $2^{31}$-1 pseudo random bit sequence (PRBS) data pattern. It displays an eye opening of 95% at 3 kbit/s.

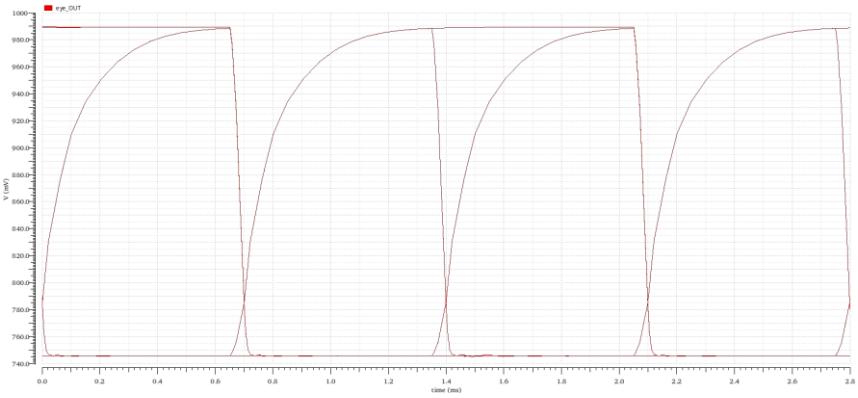


Fig. 4.18 Eye diagram of $g_m$-boosted RIC TIA.

## 4.5 Layout

Fig. 4.19 shows the masked layout for $g_m$-boosted RIC TIA which occupies 53.5 × 34.5 µm$^2$ of silicon area.

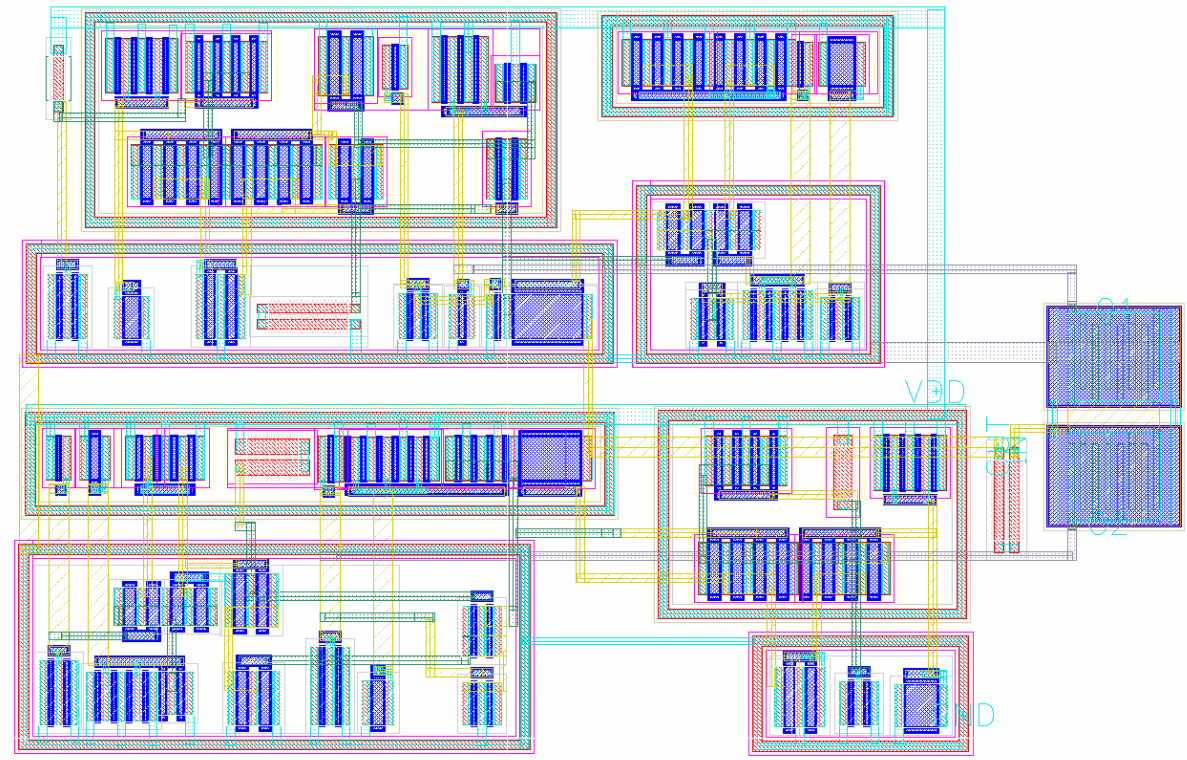



Fig. 4.19 Layout of $g_m$-boosted RIC TIA.

# Chapter 5 $g_m$-boosted Doubly Folded Push-pull Transimpedance Amplifier

This chapter presents a novel $g_m$-boosted doubly folded push-pull TIA ($g_m$-boosted doubly folded push-pull TIA) design. Theoretical foundations by way of gain and noise analysis are developed. The simulation results for the proposed TIA indicated a -3 dB bandwidth of 218 kHz with a transimpedance gain of 218 dB ohms. The input referred noise current spectral density is below 160 pA/sqrt (Hz). Eye diagram simulation using -229 dBm input photodiode current signal and a $2^{31}$-1 pseudo random bit sequence data pattern shows an eye opening of 90% at 100 kbit/s.

## 5.1 Topology of $g_m$-boosted Doubly Folded Push-pull TIA

To provide sufficient gain and wider bandwidth, a multiple-stage $g_m$-boosted doubly folded push-pull TIA is introduced in this chapter. The topology of the proposed $g_m$-boosted doubly folded push-pull TIA is shown in Fig. 5.2 and the details of $g_m$-boosting designs included in it are presented in Fig. 5.1. It consists of three stages: (1) a novel single-ended input to differential output conversion stage (also converts a current signal to voltage), (2) a $g_m$-boosted fully differential folded-cascode voltage amplifier stage, (3) a differential input to the single-ended output conversion stage. The first stage converts single-ended current input to differential voltage outputs and then the signals are amplified through a $g_m$-boosted fully differential folded-cascode amplifier with a very high gain. In the next stage, the signal comes through another folded-cascode amplifier and converts the differential signal to a single-ended signal by a push-pull structure.

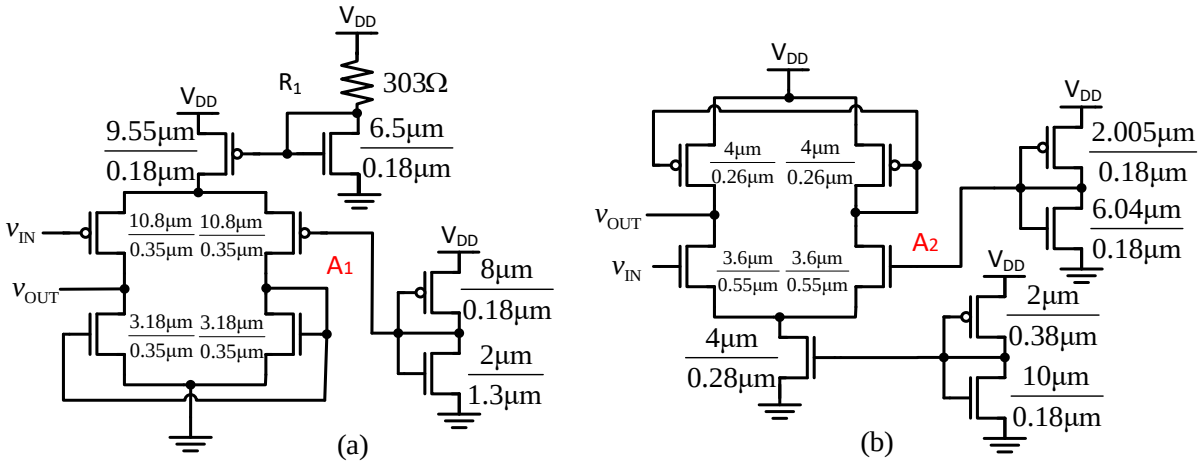



Fig. 5.1 $g_m$-boosting design for proposed $g_m$-boosted doubly folded push-pull TIA.

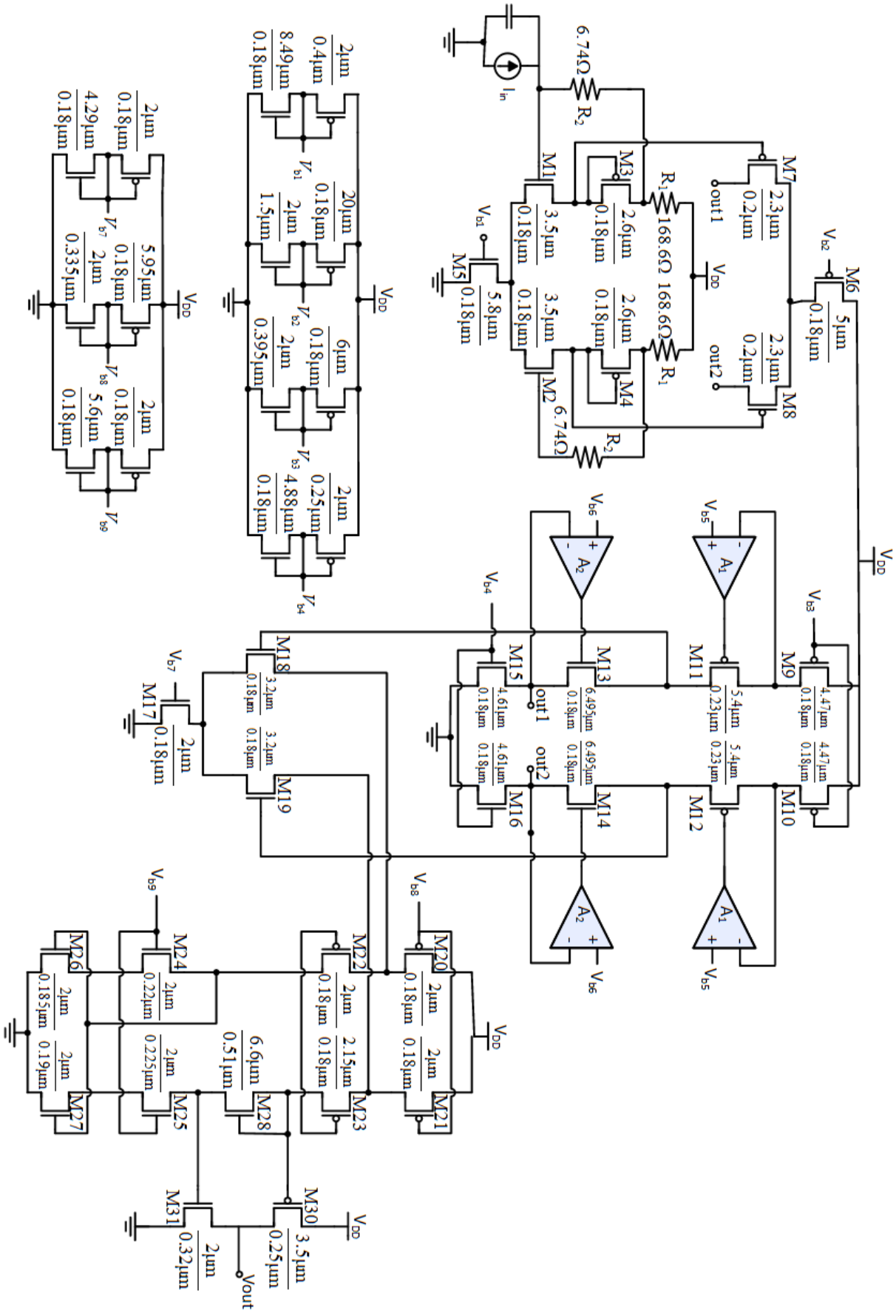



Fig. 5.2 Schematic of proposed $g_m$-boosted doubly folded push-pull TIA.

## 5.2 Analysis of Mid-band Transimpedance Gain

In this section, an analysis of the transimpedance gain of each stage is provided in detail and the overall gain is given by the product of the gain from individual stages.

### 5.2.1 Single-to-differential Converter (Current-to-voltage Converter)

The mid-band transimpedance gain of the single-to-differential converter can be derived from the AC equivalent circuit in Fig. 5.3 (a) where the power supply is shorted to ground for mid-band transimpedance behaviour and the direction of current flow is given by red arrows. Since the voltage at the drain of M5 does not change, it is actually a virtual ground for fully matched circuits [56]. Therefore, the AC equivalent circuit of the single-to-differential converter is separated into two halves in Fig. 5.3 (b) and (c), and the voltage at point $O_1$ and $O_2$ have the same magnitude but opposite sign.

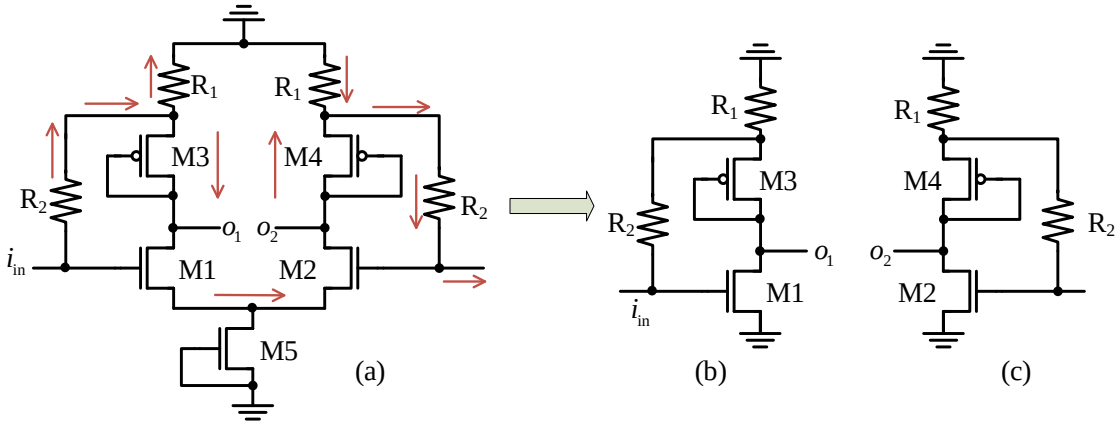



Fig. 5.3 (a) AC equivalent circuit of single-to-differential converter, (b), (c) AC equivalent half-circuits.

Take Fig. 5.3 (b) for example, the output of the left half circuit of the single-to-differential converter is AC shorted to ground to find out the transconductance $G_m$ in Fig. 5.4. Transistor M3 presents a PMOS diode load that is connected to low-supply rail (ground). Thus, the body effect transconductance current source becomes independent which can be neglected and the transconductance current source can be replaced by a simple resistor with conductance $g_m$ [58]. Next, finding the Thevenin equivalent circuit by inspection and the transconductance $G_m$ is given by,

$$G_m = -\frac{i_{out}}{v_{in}} = \frac{g_{m1}v_{in}}{v_{in}} = g_{m1} \tag{5.01}$$

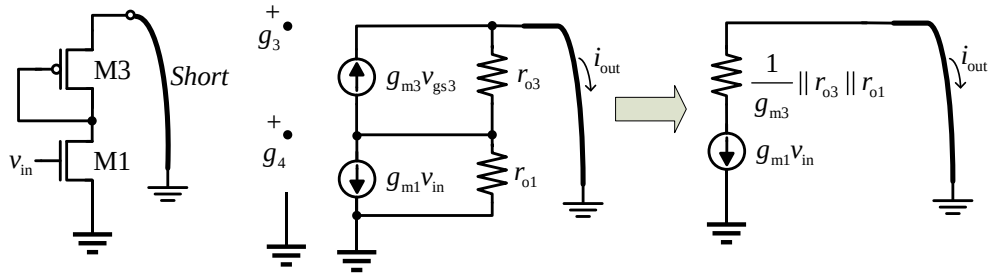



Fig. 5.4 Shorting the output of left half circuit of the single-to-differential converter to find the transconductance $G_m$.

The output impedance $R_{out}$ can be determined by shoring the input to ground as shown in Fig. 5.5 (a). The body effect current source is $g_{mb3}v_{bs3}$ and the voltage $v_{bs3}$ can be expressed by,

$$\begin{aligned} v_{bs3} &= v_{b3} - v_{s3} \\ &= 0 - v_{s3} = -v_{s3} \end{aligned} \tag{5.02}$$

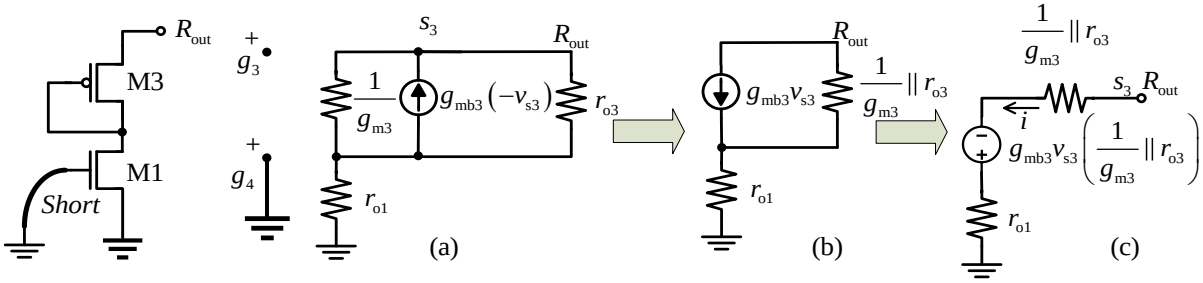



Fig. 5.5 (a)Shorting the input of left half circuit of single-to-differential converter to find the output impedance Rout, (b) simplified small signal equivalent circuit, (c) finding the Thevenin equivalent circuit.

Fig. 5.5 (b) shows the simplified small-signal equivalent circuit which merged the parallel resistor $\frac{1}{g_{m3}}$ and $r_{o3}$. Then, the circuit can be converted from the merged Norton circuit into Thevenin's form as shown in Fig. 5.5 (c). Assuming the current flow into from the source of M3 at point (s3) is $i$, the voltage at the point (s3) is given by,

$$v_{s3} = i \times \frac{1}{g_{m3} + \frac{1}{r_{o3}}} - g_{mb3}v_{s3}\left(\frac{1}{g_{m3} + \frac{1}{r_{o3}}}\right) + i \times r_{o1} \tag{5.03}$$

Changing sides,

$$v_{s3} + g_{mb3}v_{s3}\left(\frac{1}{g_{m3} + \frac{1}{r_{o3}}}\right) = i \times \left(\frac{1}{g_{m3} + \frac{1}{r_{o3}}} + r_{o1}\right) \tag{5.04}$$

Rationalizing, and the current $i$ is given by,

$$i = \frac{v_{s3}\left(1 + g_{mb3}\dfrac{1}{g_{m3} + \frac{1}{r_{o3}}}\right)}{\left(r_{o1} + \dfrac{1}{g_{m3} + \frac{1}{r_{o3}}}\right)} \tag{5.05}$$

Hence, the output impedance $R_{out}$ is given by,

$$\begin{aligned} R_{out} &= \frac{v_{s3}}{i} \\ &= \frac{r_{o1} + \dfrac{1}{g_{m3} + \frac{1}{r_{o3}}}}{1 + g_{mb3}\dfrac{1}{g_{m3} + \frac{1}{r_{o3}}}} \end{aligned} \tag{5.06}$$

From the previous calculation, the small-signal circuits in Fig. 5.3 (b) can be represented by an equivalent composite transistor with transconductance $G_m$ and output impedance $R_{out}$ as shown in Fig. 5.6 (a) and (b). The voltage gain $A_{vg_1s_3}$ in Fig. 5.6 (b) is given by,

$$A_{vg_1s_3} = G_m\left(R_1 \,||\, R_{out}\right) \tag{5.07}$$

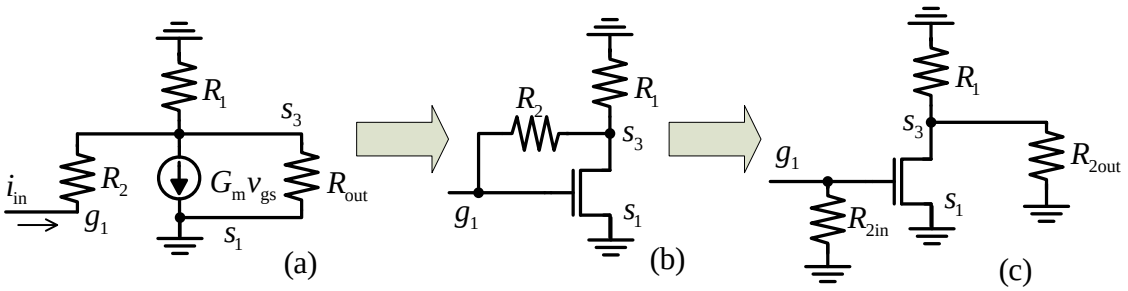



Fig. 5.6 (a) Highly simplified small-signal equivalent circuit for single-to-differential converter, (b) Simplified AC equivalent circuits from (a), (c) Using Miller's theorem to find the equivalent circuit.

According to Miller's Theorem, resistor $R_2$ can be replaced by two resistors $R_{2in}$ and $R_{2out}$ that connect the corresponding nodes to ground as shown in Fig. 5.6 (c). Hence, the resistors $R_{2in}$ and $R_{2out}$ is easy to find by,

$$\begin{aligned} R_{2in} &= \frac{R_2}{1 + A_{vg_1s_3}} \\ &= \frac{R_2}{1 + G_m\left(R_1 \,||\, R_{out}\right)} \end{aligned} \tag{5.08}$$

$$R_{2\text{out}} = \frac{R_2}{1 + \dfrac{1}{G_\text{m}\left(R_1 \,||\, R_{\text{out}}\right)}} \tag{5.09}$$

Next, decompose the equivalent composite transistor by the original transistors M1 and M3 as shown in Fig. 5.7 (a), (b). Fig. 5.7 (c) shows the AC equivalent circuit and small-signal equivalent circuit to find out the output impedance at the drain of transistor M3. Fig. 5.7 (d) and (e) are the conversation from Norton equivalent circuit to Thevenin equivalent circuit by inspection. Thus, from Fig. 5.7 (e), the current flows through the circuit is given by,

$$i = \frac{v_{\text{s3}}}{R_1 \,||\, R_{2\text{out}}} \tag{5.10}$$

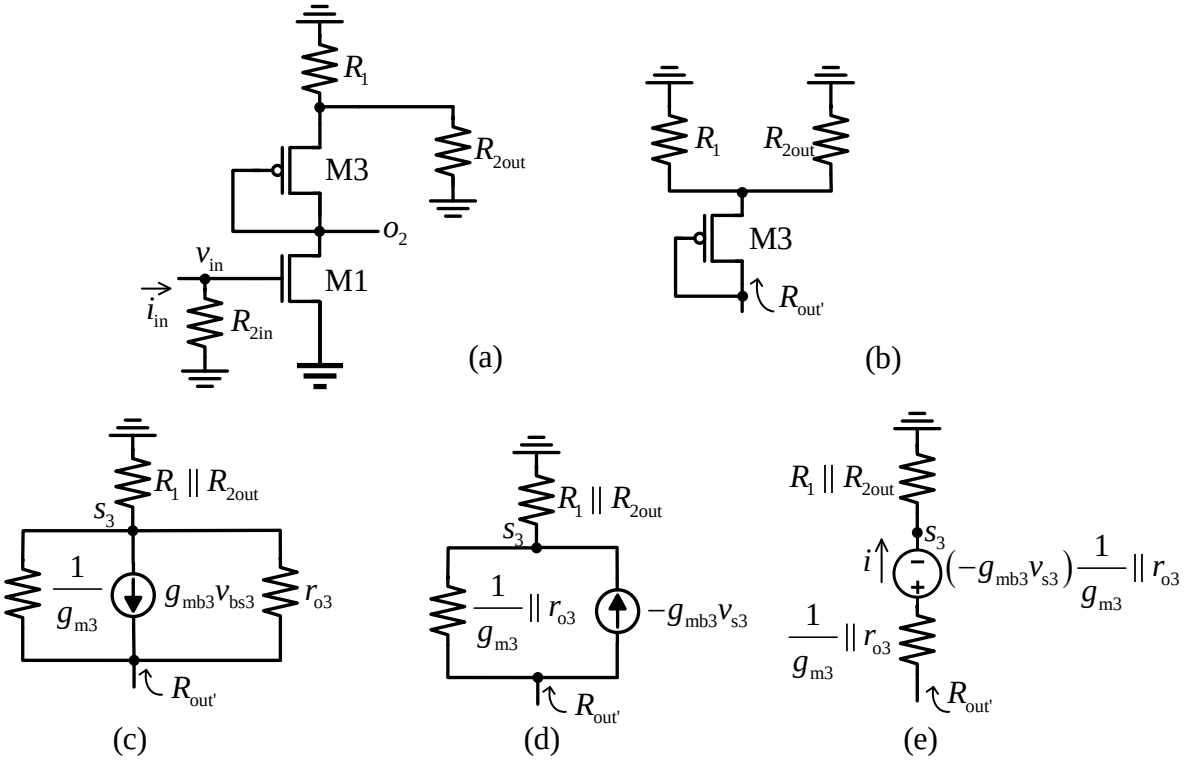



Fig. 5.7 (a) decomposing the composite transistor back to original transistors, (b) taking only the top circuit, (c) small-signal equivalent circuit of (b), (d) simplified small-signal equivalent circuit from(c), (e) finding the Thevenin equivalent circuit.

Also, the value of the voltage source in the Thevenin equivalent circuit from Fig. 5.7 (e) can be written as,

$$v = -g_{\text{mb3}} v_{\text{s3}} \left( \frac{1}{g_{\text{m3}} + \frac{1}{r_{\text{o3}}}} \right) \tag{5.11}$$

The total voltage at the drain of transistor M3 is the sum of the voltage across the resistors and voltage source, which is given by,

$$v_{out'} = i\frac{1}{g_{m3}+\frac{1}{r_{o3}}} + g_{mb3}v_{s3}\left(\frac{1}{g_{m3}+\frac{1}{r_{o3}}}\right) + v_{s3} \tag{5.12}$$

Hence, the output impedance is easy to find by,

$$\begin{aligned} R_{out'} &= \frac{v_{out'}}{i} \\ &= \frac{i\frac{1}{g_{m3}+\frac{1}{r_{o3}}} + g_{mb3}v_{s3}\left(\frac{1}{g_{m3}+\frac{1}{r_{o3}}}\right) + v_{s3}}{i} \\ &= \frac{\frac{v_{s3}}{R_1 \,||\, R_{2out}} \times \frac{1}{g_{m3}+\frac{1}{r_{o3}}} + g_{mb3}v_{s3}\left(\frac{1}{g_{m3}+\frac{1}{r_{o3}}}\right) + v_{s3}}{\frac{v_{s3}}{R_1 \,||\, R_{2out}}} \\ &= \frac{\frac{1}{R_1 \,||\, R_{2out}} \times \frac{1}{g_{m3}+\frac{1}{r_{o3}}} + g_{mb3}\left(\frac{1}{g_{m3}+\frac{1}{r_{o3}}}\right) + 1}{\frac{1}{R_1 \,||\, R_{2out}}} \\ &= \frac{1}{g_{m3}+\frac{1}{r_{o3}}} + g_{mb3}\frac{R_1 \,||\, R_{2out}}{g_{m3}+\frac{1}{r_{o3}}} + R_1 \,||\, R_{2out} \end{aligned} \tag{5.13}$$

Next, the AC equivalent circuit of half single-to-differential converter is simplified in Fig. 5.8. By inspection, the input voltage at the gate of transistor M1 is given by,

$$v_{in} = i_{in}R_{2in} \tag{5.14}$$

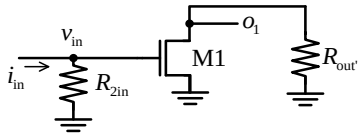



Fig. 5.8 Final simplified form of the half circuit of single-to-differential converter.

Next, the drain voltage at the common gate stage is given by,

$$v_{o1} = -g_{m1}v_{in}R_{out'} \tag{5.15}$$

After rationalizing,

$$\frac{v_{o1}}{v_{in}} = -g_{m1}R_{out'} \tag{5.16}$$

So that, the voltage at $O_1$ is given by,

$$v_{o1} = -g_{m1} i_{in} R_{2in} R_{out'} \tag{5.17}$$

Using equation (5.08) and (5.13),

$$v_{o1} = -g_{m1} i_{in} \frac{R_2}{1+\frac{1}{G_m\left(R_1 \| R_{out}\right)}} \left( \frac{1}{g_{m3}+\frac{1}{r_{o3}}} + g_{mb3} \frac{R_1 \| R_{2out}}{g_{m3}+\frac{1}{r_{o3}}} + R_1 \| R_{2out} \right) \tag{5.18}$$

Hence, the voltage at $O_2$ is given by,

$$\begin{aligned} v_{o2} &= v_{o1} = g_{m1} i_{in} R_{2in} R_{out'} \\ &= g_{m1} i_{in} \frac{R_2}{1+\frac{1}{G_m\left(R_1 \| R_{out}\right)}} \left( \frac{1}{g_{m3}+\frac{1}{r_{o3}}} + g_{mb3} \frac{R_1 \| R_{2out}}{g_{m3}+\frac{1}{r_{o3}}} + R_1 \| R_{2out} \right) \end{aligned} \tag{5.19}$$

Finally, the total transimpedance gain of the single-to-differential converter is given by,

$$\begin{aligned} A_{v1} &= \frac{v_{o1}-v_{o2}}{i_{in}} = -2 g_{m1} R_{2in} R_{out'} \\ &= -2 g_{m1} \frac{R_2}{1+\frac{1}{G_m\left(R_1 \| R_{out}\right)}} \left( \frac{1}{g_{m3}+\frac{1}{r_{o3}}} + g_{mb3} \frac{R_1 \| R_{2out}}{g_{m3}+\frac{1}{r_{o3}}} + R_1 \| R_{2out} \right) \end{aligned} \tag{5.20}$$

### 5.2.2 Middle Stage

The middle stage is a $g_m$-boosted fully differential folded-cascode voltage amplifier which provides high voltage gain. Fig. 5.10 shows the AC equivalent circuit of the middle stage that shorts the power supply and bias voltage to AC ground. The $g_m$-boosted amplifier structures are represented by triangle symbols "$A_1$"and "$A_2$". The output voltage of the proposed middle stage can be derived from the half circuit first which is shown in Fig. 5.10 (b). And the input voltage from the previous stage is given by,

$$v_{in} = \frac{v_{o1}-v_{o2}}{2} \tag{5.21}$$

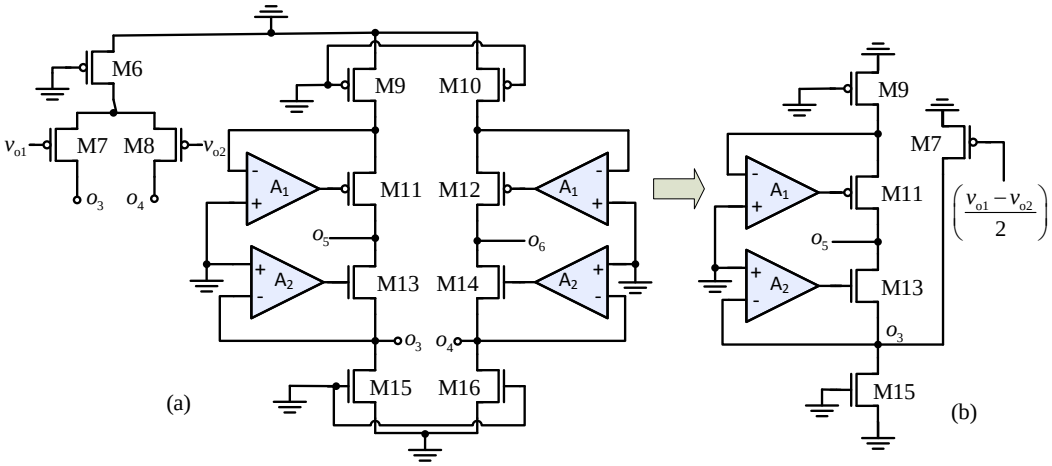



Fig. 5.9 (a) AC equivalent circuit of the middle stage, (b) AC half circuit.

Next, the output impedance of the PMOS current source load structure can be derived from Fig. 5.10 (a) and the value is given by,

$$R_{\text{out2}} = r_{\text{o9,10}} + r_{\text{o11,12}} + r_{\text{o9,10}}\left[g_{\text{m11,12}}\left(\text{A}_1 + 1\right) + g_{\text{mb11,12}}\right]r_{\text{o11,12}} \tag{5.22}$$

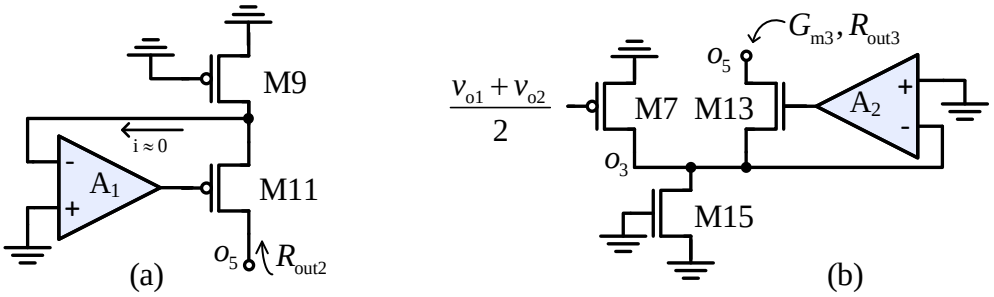



Fig. 5.10 (a) AC equivalent circuit of PMOS current source load, (b) AC equivalent circuit of NMOS telescopic folded cascode.

Similarly, the transconductance $G_{\text{m3}}$ of the bottom half, NMOS telescopic folded cascode of Fig. 5.9 (b) can be derived from Fig. 5.10 (b) which is given by,

$$G_{\text{m3}} = \frac{g_{\text{m7,8}}\left(r_{\text{o7,8}} \,\|\, r_{\text{o15,16}}\right)\left[\left\{\left(\text{A}_2 + 1\right)g_{\text{m13,14}} + g_{\text{mb13,14}}\right\}r_{\text{o13,14}} + 1\right]}{r_{\text{o13,14}}\left[\left(\text{A}_2 + 1\right)g_{\text{m13,14}} + g_{\text{mb13,14}}\right]\left(r_{\text{o15,16}} \,\|\, r_{\text{o7,8}}\right) + r_{\text{o13,14}} + \left(r_{\text{o15,16}} \,\|\, r_{\text{o7,8}}\right)} \tag{5.23}$$

And, the output impedance $R_{\text{out3}}$ is given by,

$$R_{\text{out3}} = r_{\text{o13,14}}\left[\left(\text{A}_2 + 1\right)g_{\text{m13,14}} + g_{\text{mb13,14}}\right]\left(r_{\text{o15,16}} \,\|\, r_{\text{o7,8}}\right) + r_{\text{o13,14}} + \left(r_{\text{o15,16}} \,\|\, r_{\text{o7,8}}\right) \tag{5.24}$$

Hence, the voltage gain $\text{A}_{\text{v2}}$ is given below,

$$\text{A}_{\text{v2}} = \frac{v_{\text{o5}} - v_{\text{o6}}}{v_{\text{o1}} - v_{\text{o2}}} = -G_{\text{m3}}\left(R_{\text{out3}} \,\|\, R_{\text{out2}}\right) \tag{5.25}$$

### 5.2.3 Final Stage

The third stage is to amplify the signal further and converts the differential signal to a single output. Fig. 5.11 (a) depicts the equivalent form of the third stage. By inspection, the left half circuit is similar to the second stage in Fig. 5.11 (b). Therefore, the transconductance $G_{m4}$ and output impedance $R_{out}$ telescopic folded cascode as shown in Fig. 5.11 (c) are given by,

$$G_{m4} = \frac{g_{m18,19}\left(r_{o18,19} \parallel r_{o20,21}\right)\left[\left(g_{m22,23} + g_{mb22,23}\right)r_{o22,23} + 1\right]}{\left(g_{m22,23} + g_{mb22,23}\right)r_{o22,23}\left(r_{o18,19} \parallel r_{o20,21}\right) + r_{o22,23} + \left(r_{o18,19} \parallel r_{o20,21}\right)} \tag{5.26}$$

$$R_{out4} = \left(g_{m22,23} + g_{mb22,23}\right)r_{o22,23}\left(r_{o18,19} \parallel r_{o20,21}\right) + r_{o22,23} + \left(r_{o18,19} \parallel r_{o20,21}\right) \tag{5.27}$$

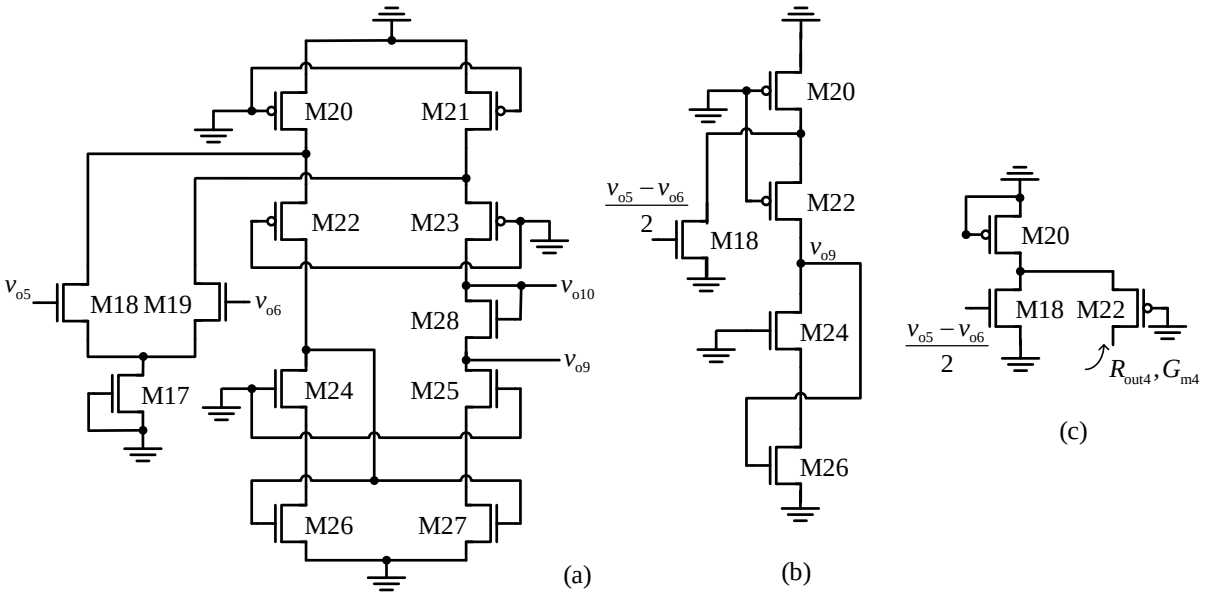



Fig. 5.11 (a) AC equivalent circuit of third stage of proposed $g_m$-boosted doubly folded push-pull TIA, (b) half circuit of third stage, (c) AC equivalent circuit of telescopic folded cascode.

Next, the right half circuit is a little different from the left half, but it can be seen as a telescopic folded cascode structure with a diode load in Fig. 5.12. Thus, the transconductance $G_{m5}$ and output impedance $R_{out5}$ at the drain of transistor M28 is the same as they are on the left side, which are given below,

$$G_{m5} = G_{m4} = \frac{g_{m18,19}\left(r_{o18,19} \parallel r_{o20,21}\right)\left[\left(g_{m22,23} + g_{mb22,23}\right)r_{o22,23} + 1\right]}{\left(g_{m22,23} + g_{mb22,23}\right)r_{o22,23}\left(r_{o18,19} \parallel r_{o20,21}\right) + r_{o22,23} + \left(r_{o18,19} \parallel r_{o20,21}\right)} \tag{5.28}$$

$$R_{out5} = R_{out4} = \left(g_{m22,23} + g_{mb22,23}\right)r_{o22,23}\left(r_{o18,19} \parallel r_{o20,21}\right) + r_{o22,23} + \left(r_{o18,19} \parallel r_{o20,21}\right) \tag{5.29}$$

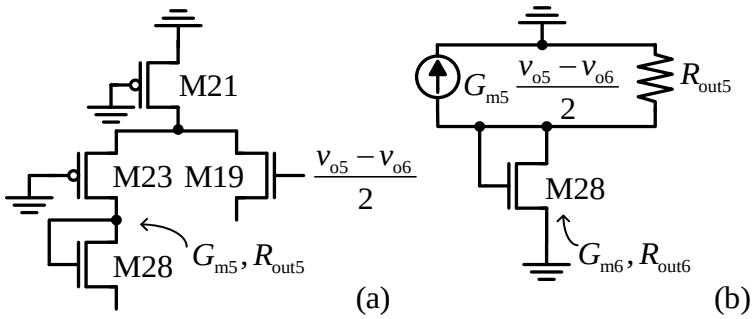



Fig. 5.12 (a) AC equivalent circuit of PMOS telescopic cascode with diode load of right half, (b) small-signal mid-band equivalent circuit of (a).

Firstly, short the input terminal to AC ground as shown in Fig. 5.13(b) to find out the transconductance $G_{m6}$ and output impedance $R_{out6}$ seen from transistor M28 (the small-signal mid-band circuit in Fig. 5.13(a)). Here, the circuit is simplified in Fig. 5.13 (c) because NMOS diode load is connected to AC ground and there is no dependent current source due to body-effect and the current source $g_{m28}v_{gs28}$ is a dependent current source due to itself, so it can be replaced by a resistor $\frac{1}{g_{m28}}$ [58].

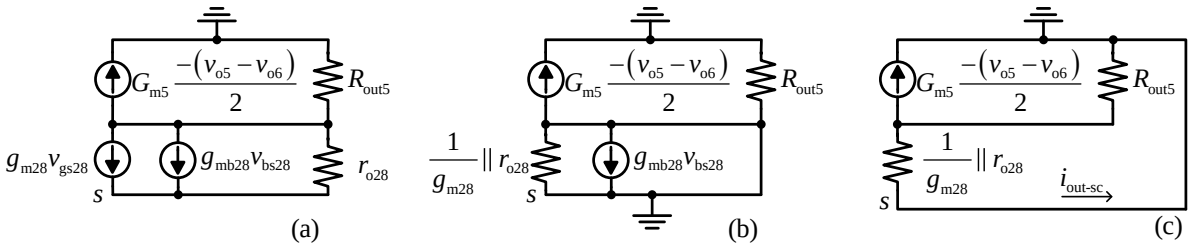



Fig. 5.13 (a) small-signal mid-band circuit of telescopic cascode with diode load, (b) shorting input to find $G_{m6}$, (c) simplified circuit.

Next, the current flows from the source of transistor M28 to ground is given by,

$$i_{out\text{-}sc} = -G_{m5}\left(\frac{v_{o5}-v_{o6}}{2}\right)\left(\frac{R_{out5}}{\left(\frac{1}{g_{m28}}+r_{o28}\right)+R_{out5}}\right) \tag{5.30}$$

Accordingly, the transconductance $G_{m6}$ can be written as,

$$G_{m6} = \frac{i_{out\text{-}sc}}{-\frac{v_{o5}-v_{o6}}{2}} \tag{5.31}$$

Using equation (5.30) and rationalizing,

$$\frac{i_{\text{out-sc}}}{\frac{v_{o5}-v_{o6}}{2}} = -G_{m5}\left(\frac{R_{out5}}{\left(\frac{1}{g_{m28}}+r_{o28}\right)+R_{out5}}\right) \tag{5.32}$$

Thus, the transconductance $G_{m6}$ is given by,

$$G_{m6} = G_{m5}\left(\frac{R_{out5}}{\left(\frac{1}{g_{m28}}+r_{o28}\right)+R_{out5}}\right) \tag{5.33}$$

The output impedance $R_{out6}$ can be found by shorting the input to ground such as set $\left(\frac{v_{o5}-v_{o6}}{2}\right)=0$ as shown in Fig. 5.14 (a) and the current source $g_{m28}v_{gs28}$ is represented by a resistor $\frac{1}{g_{m28}}$ for the same reason as explained previously. In Fig. 5.14 (b), the two resistors are express as one resistor $\frac{1}{g_{m28}} \| r_{o28}$. By inspection, the Norton equivalent circuit form is converted to Thevenin equivalent circuit in Fig. 5.14 (c) and the voltage at the source of M28 is given by,

$$v_{s28} = i\frac{1}{g_{m28}+\frac{1}{r_{o28}}} - \left(g_{mb28}v_{s28}\right)\frac{1}{g_{m28}+\frac{1}{r_{o28}}} + i\times R_{out5} \tag{5.34}$$

Changing sides and simplifying,

$$v_{s28}\left(1+g_{mb28}\frac{1}{g_{m28}+\frac{1}{r_{o28}}}\right) = i\left(\frac{1}{g_{m28}+\frac{1}{r_{o28}}}+R_{out5}\right) \tag{5.35}$$

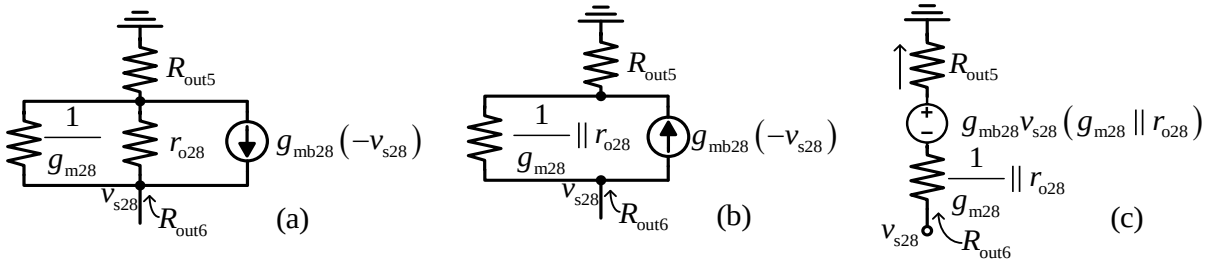



Fig. 5.14 (a) Shorting input to ground, (b) Merged the resistors, (c) Thevenin equivalent circuit.

Hence, the output impedance $R_{out6}$ can be found by incremental KVL, dividing the total small-signal voltage $v_{s28}$ using equation (5.35) by the small-signal current flowing out which is given by,

$$\begin{aligned} R_{out6} &= \frac{v_{s28}}{i} \\ &= \frac{R_{out5} + \dfrac{1}{g_{m28} + \frac{1}{r_{o28}}}}{1 + \dfrac{1}{g_{m28} + \frac{1}{r_{o28}}}} \end{aligned} \tag{5.36}$$

The next step is to determine the output impedance $R_{out7}$ of transistors M25, M27 and M28 as shown in Fig. 5.15 (a). The output impedance seen from the drain of the transistor is easy to find by,

$$R = \left(g_{m25} + g_{mb25}\right) r_{o25} r_{o27} + r_{o25} + r_{o27} \tag{5.37}$$

Therefore, $R_{out7}$ is a diode connection with a resistor $R$ as shown in Fig. 5.15 (b) and its small-signal equivalent circuit is presented in Fig. 5.15 (c). Similarly, the current source load in diode connection is replaced by a resistor $\dfrac{1}{g_{m28}}$ and simplified Norton equivalent form is converted to Thevenin equivalent circuits in Fig. 5.15 (d) and (e) respectively. According to KVL, the output impedance $R_{out7}$ is given by,

$$R_{out7} = \frac{\dfrac{v_{s28}}{R}\dfrac{1}{g_{m28} + \frac{1}{r_{o28}}} + v_{s28} + g_{mb28} v_{s28} \dfrac{1}{g_{m28} + \frac{1}{r_{o28}}}}{\dfrac{v_{s28}}{R}} \tag{5.38}$$

Simplifying,

$$R_{out7} = \frac{1}{g_{m28} + \frac{1}{r_{o28}}} + R + R\frac{1}{g_{m28} + \frac{1}{r_{o28}}} g_{mb28} \tag{5.39}$$

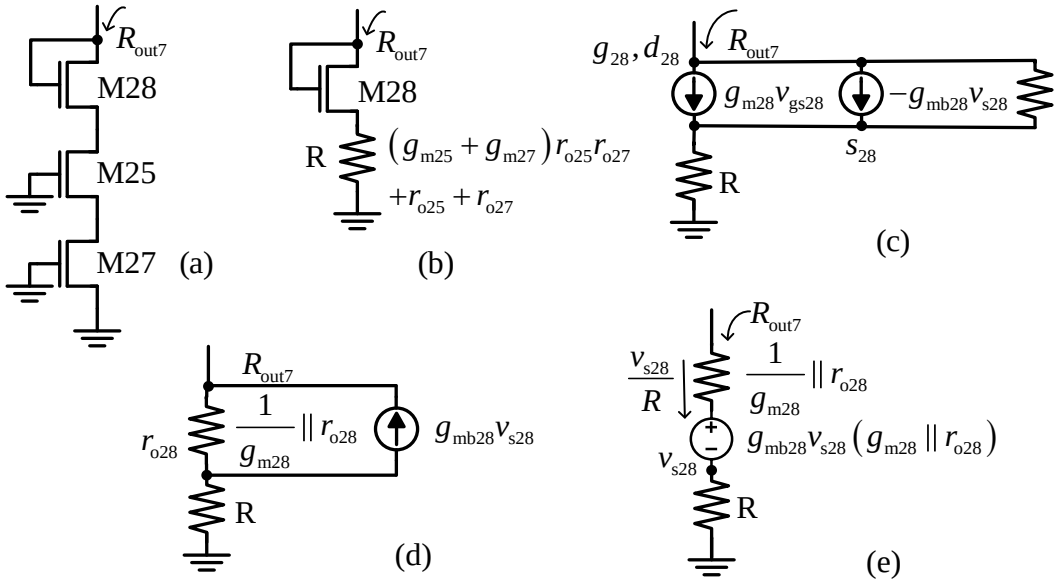



Fig. 5.15 (a) Output impedance of current source load with diode connection, (b) Simplified resistive load with diode connection, (c) Small-signal mid-band equivalent circuit of (b), (d) Simplified the diode connection, (e) Thevenin equivalent circuit.

Next, the output voltage can be derived from Fig. 5.16 which shows the high simplified small-signal mid-band equivalent circuit with a current source $G_{m4}\left(\frac{v_{o5}-v_{o6}}{2}\right)$ and $G_{m6}\left(-\frac{v_{o5}-v_{o6}}{2}\right)$, resistors $R_{out4}$ and $R_{out6}$ as well as active current-mirror load. The relationship between current $i_1$ and $i_2$ for current $i_0$ flowing out of the circuit at the point $O_9$ is given by,

$$\begin{aligned} i_0 &= i_1 - i_2 \\ &= G_{m4}\left(\frac{v_{o5}-v_{o6}}{2}\right) - G_{m6}\left(-\frac{v_{o5}-v_{o6}}{2}\right) \\ &= \left(G_{m4}+G_{m6}\right)\left(\frac{v_{o5}-v_{o6}}{2}\right) \end{aligned} \tag{5.40}$$

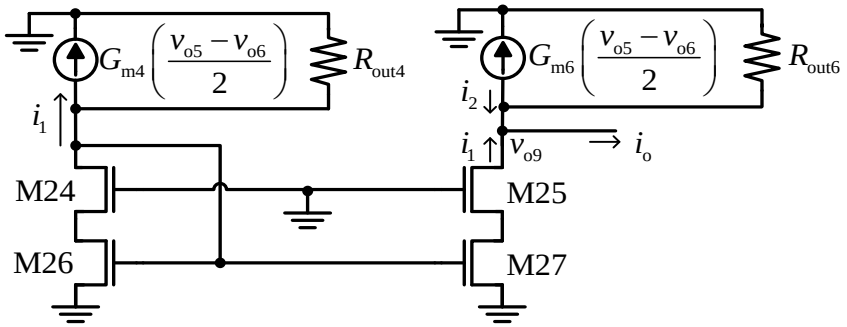



Fig. 5.16 Highly simplified small-signal mid-band equivalent third stage circuit.

Hence, the voltage at the output point $O_9$ is given by,

$$\begin{aligned} v_{o9} &= i_0 R_{\text{Load}} \\ &= \left(G_{m4} + G_{m6}\right)\left(\frac{v_{o5} - v_{o6}}{2}\right) \times R_{\text{out6}} \,||\left[\left(g_{m24,25} + g_{mb24,25}\right) r_{o24,25} r_{o26,27} + r_{o24,25} + r_{o26,27}\right] \end{aligned} \tag{5.41}$$

To find out the voltage at output point $O_{10}$, Fig. 5.17 (a) is the folded casecode structure which is the top circuit from the left-hand side of the proposed third stage. The circuit is the same with Fig. 5.11 (c), thus, the transconductance $G_{m8}$ and output resistor $R_{out8}$ are given by,

$$\begin{aligned} G_{m8} &= G_{m4} \\ &= \frac{g_{m18,19}\left(r_{o18,19} \,||\, r_{o20,21}\right)\left[\left(g_{m22,23} + g_{mb22,23}\right) r_{o22,23} + 1\right]}{\left(g_{m22,23} + g_{mb22,23}\right) r_{o22,23}\left(r_{o18,19} \,||\, r_{o20,21}\right) + r_{o22,23} + \left(r_{o18,19} \,||\, r_{o20,21}\right)} \end{aligned} \tag{5.42}$$

$$\begin{aligned} R_{out8} &= R_{out4} \\ &= \left(g_{m22,23} + g_{mb22,23}\right) r_{o22,23}\left(r_{o18,19} \,||\, r_{o20,21}\right) + r_{o22,23} + \left(r_{o18,19} \,||\, r_{o20,21}\right) \end{aligned} \tag{5.43}$$

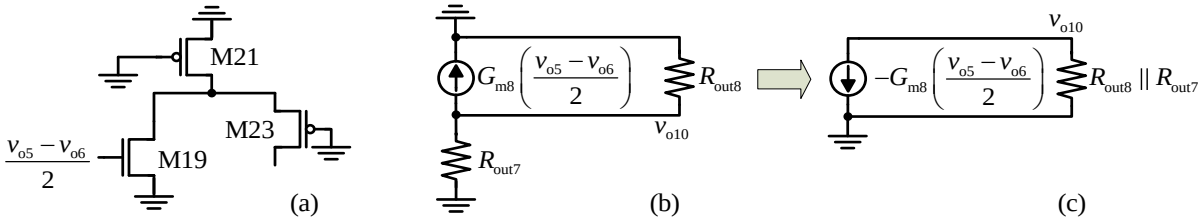



Fig. 5.17 (a) AC equivalent of folded cascode structure, (b) Small-signal mid-band equivalent circuit to find voltage at point $O_{10}$, (c) Simplified small-signal mid-band equivalent circuit of (b).

Then the small-signal mid-band equivalent circuit of the right half circuit is represented in Fig. 5.17 (b). Resistors $R_{out7}$ and $R_{out8}$ are in parallel and Fig. 5.17 (c) presents the simplified as Norton equivalent circuit. From it, the voltage at the output $O_{10}$ is given by,

$$v_{o10} = G_{m8}\left(\frac{v_{o5} - v_{o6}}{2}\right)\left(R_{out8} \,||\, R_{out7}\right) \tag{5.44}$$

The last step is a push-pull output stage. Its AC equivalent circuit and small-signal mid-band equivalent circuit are presented in Fig. 5.18 (a) and (b) respectively. The output voltage at this stage can be derived by a simplified circuit in Fig. 5.18 (c) which is given by,

$$v_{out} = -\left(g_{m30} v_{o10} + g_{m31} v_{o9}\right)\left(r_{o30} \,||\, r_{o31}\right) \tag{5.45}$$

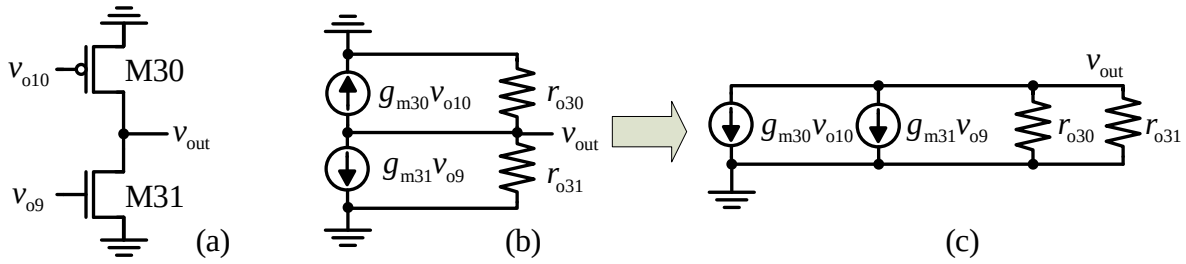



Fig. 5.18 (a) AC equivalent circuit of push-pull output stage, (b) small-signal mid-band equivalent circuit of (a), (c) simplified (b).

Therefore, the total voltage gain at the third stage is given by,

$$\mathrm{A_{v3}} = \frac{v_{out}}{v_{o5} - v_{o6}} \tag{5.46}$$

Using equation (5.45),

$$\mathrm{A_{v3}} = \frac{-\left(g_{m30}v_{o10} + g_{m31}v_{o9}\right)\left(r_{o30} \parallel r_{o31}\right)}{v_{o5} - v_{o6}} \tag{5.47}$$

Using equation (5.41) and (5.44),

$$\mathrm{A_{v3}} = \frac{-\left(\begin{array}{l} g_{m30}G_{m8}\left(\frac{v_{o5}-v_{o6}}{2}\right)\left(R_{out8} \parallel R_{out7}\right) + g_{m31}\left(G_{m4}+G_{m6}\right)\left(\frac{v_{o5}-v_{o6}}{2}\right) \\ \times R_{out6} \parallel \left[\left(g_{m24,25}+g_{mb24,25}\right) r_{o24,25} r_{o26,27} + r_{o24,25} + r_{o26,27}\right] \end{array}\right)\left(r_{o30} \parallel r_{o31}\right)}{v_{o5} - v_{o6}} \tag{5.48}$$

After simplifying,

$$\mathrm{A_{v3}} = \frac{1}{2}\left(r_{o30} \parallel r_{o31}\right)\left\{\begin{array}{l} g_{m30}G_{m8}\left(R_{out8} \parallel R_{out7}\right) + g_{m31}\left(G_{m4}+G_{m6}\right) \\ \times R_{out6} \parallel \left[\left(g_{m24,25}+g_{mb24,25}\right) r_{o24,25} r_{o26,27} + r_{o24,25} + r_{o26,27}\right] \end{array}\right\} \tag{5.49}$$

Hence, the total transimpedance gain is given by the product of the gain from each stage which is given below,

$$\mathrm{A_{v\_total}} = \mathrm{A_{v1}} \times \mathrm{A_{v2}} \times \mathrm{A_{v3}} \tag{5.50}$$

Using equation (5.20), (5.25) and (5.49),

$$\mathrm{A_{v\_total}} = g_{m1}\frac{R_2}{1 + \frac{1}{G_m\left(R_1 \parallel R_{out}\right)}}\left(\frac{1}{g_{m3} + \frac{1}{r_{o3}}} + g_{mb3}\frac{R_1 \parallel R_{2out}}{g_{m3} + \frac{1}{r_{o3}}} + R_1 \parallel R_{2out}\right) G_{m3}\left(R_{out3} \parallel R_{out2}\right)$$
$$\times \left(r_{o30} \parallel r_{o31}\right)\left\{\begin{array}{l} g_{m30}G_{m8}\left(R_{out8} \parallel R_{out7}\right) + g_{m31}\left(G_{m4}+G_{m6}\right) \\ \times R_{out6} \parallel \left[\left(g_{m24,25}+g_{mb24,25}\right) r_{o24,25} r_{o26,27} + r_{o24,25} + r_{o26,27}\right] \end{array}\right\} \tag{5.51}$$

## 5.3 Input Referred Noise Analysis

In this section, the input referred noise current spectral density of the proposed $g_m$-boosted doubly folded push-pull TIA can be derived theoretically using the noise inserted circuit diagram in Fig. 5.19 which only considers thermal noise of resistors and drain-current noise of MOSFET devices. By Following the same principle in equation (3.23) and (3.24), the noise current power density of MOSFETs and resistors in Fig. 5.19 is given by,

$$\overline{i^2_{n,m1}} = 4KT\frac{\gamma_1}{\alpha_1}g_{m1} \tag{5.52}$$

$$\overline{i^2_{n,m2}} = 4KT\frac{\gamma_2}{\alpha_2}g_{m2} \tag{5.53}$$

$$\overline{i^2_{n,m3}} = 4KT\frac{\gamma_3}{\alpha_3}g_{m3} \tag{5.54}$$

$$\overline{i^2_{n,m4}} = 4KT\frac{\gamma_4}{\alpha_4}g_{m4} \tag{5.55}$$

$$\overline{i^2_{n,m5}} = 4KT\frac{\gamma_5}{\alpha_5}g_{m5} \tag{5.56}$$

$$\overline{i^2_{n,m6}} = 4KT\frac{\gamma_6}{\alpha_6}g_{m6} \tag{5.57}$$

$$\overline{i^2_{n,m7}} = 4KT\frac{\gamma_7}{\alpha_7}g_{m7} \tag{5.58}$$

$$\overline{i^2_{n,m8}} = 4KT\frac{\gamma_8}{\alpha_8}g_{m8} \tag{5.59}$$

$$\overline{i^2_{n,m9}} = 4KT\frac{\gamma_9}{\alpha_9}g_{m9} \tag{5.60}$$

$$\overline{i^2_{n,m10}} = 4KT\frac{\gamma_{10}}{\alpha_{10}}g_{m10} \tag{5.61}$$

$$\overline{i^2_{n,m11}} = 4KT\frac{\gamma_{11}}{\alpha_{11}}g_{m11} \tag{5.62}$$

$$\overline{i^2_{n,m12}} = 4KT\frac{\gamma_{12}}{\alpha_{12}}g_{m12} \tag{5.63}$$

$$\overline{i^2_{\text{n,m13}}} = 4KT\frac{\gamma_{13}}{\alpha_{13}}g_{\text{m13}} \tag{5.64}$$

$$\overline{i^2_{\text{n,m14}}} = 4KT\frac{\gamma_{14}}{\alpha_{14}}g_{\text{m14}} \tag{5.65}$$

$$\overline{i^2_{\text{n,m15}}} = 4KT\frac{\gamma_{15}}{\alpha_{15}}g_{\text{m15}} \tag{5.66}$$

$$\overline{i^2_{\text{n,m16}}} = 4KT\frac{\gamma_{16}}{\alpha_{16}}g_{\text{m16}} \tag{5.67}$$

$$\overline{i^2_{\text{n,m17}}} = 4KT\frac{\gamma_{17}}{\alpha_{17}}g_{\text{m17}} \tag{5.68}$$

$$\overline{i^2_{\text{n,m18}}} = 4KT\frac{\gamma_{18}}{\alpha_{18}}g_{\text{m18}} \tag{5.69}$$

$$\overline{i^2_{\text{n,m19}}} = 4KT\frac{\gamma_{19}}{\alpha_{19}}g_{\text{m19}} \tag{5.70}$$

$$\overline{i^2_{\text{n,m20}}} = 4KT\frac{\gamma_{20}}{\alpha_{20}}g_{\text{m20}} \tag{5.71}$$

$$\overline{i^2_{\text{n,m21}}} = 4KT\frac{\gamma_{21}}{\alpha_{21}}g_{\text{m21}} \tag{5.72}$$

$$\overline{i^2_{\text{n,m22}}} = 4KT\frac{\gamma_{22}}{\alpha_{22}}g_{\text{m22}} \tag{5.73}$$

$$\overline{i^2_{\text{n,m23}}} = 4KT\frac{\gamma_{23}}{\alpha_{23}}g_{\text{m23}} \tag{5.74}$$

$$\overline{i^2_{\text{n,m24}}} = 4KT\frac{\gamma_{24}}{\alpha_{24}}g_{\text{m24}} \tag{5.75}$$

$$\overline{i^2_{\text{n,m25}}} = 4KT\frac{\gamma_{25}}{\alpha_{25}}g_{\text{m25}} \tag{5.76}$$

$$\overline{i^2_{\text{n,m26}}} = 4KT\frac{\gamma_{26}}{\alpha_{26}}g_{\text{m26}} \tag{5.77}$$

$$\overline{i^2_{\text{n,m27}}} = 4KT\frac{\gamma_{27}}{\alpha_{27}}g_{\text{m27}} \tag{5.78}$$

$$\overline{i^2_{n,m28}} = 4KT\frac{\gamma_{28}}{\alpha_{28}}g_{m28} \tag{5.79}$$

$$\overline{i^2_{n,m29}} = 4KT\frac{\gamma_{29}}{\alpha_{29}}g_{m29} \tag{5.80}$$

$$\overline{i^2_{n,m30}} = 4KT\frac{\gamma_{30}}{\alpha_{30}}g_{m30} \tag{5.81}$$

$$\overline{i^2_{n,m31}} = 4KT\frac{\gamma_{31}}{\alpha_{31}}g_{m31} \tag{5.82}$$

$$\overline{i^2_{n,m32}} = 4KT\frac{\gamma_{32}}{\alpha_{32}}g_{m32} \tag{5.83}$$

$$\overline{i^2_{n,m33}} = 4KT\frac{\gamma_{33}}{\alpha_{33}}g_{m33} \tag{5.84}$$

$$\overline{i^2_{n,m34}} = 4KT\frac{\gamma_{34}}{\alpha_{34}}g_{m34} \tag{5.85}$$

$$\overline{i^2_{n,m35}} = 4KT\frac{\gamma_{35}}{\alpha_{35}}g_{m35} \tag{5.86}$$

$$\overline{i^2_{n,m36}} = 4KT\frac{\gamma_{36}}{\alpha_{36}}g_{m36} \tag{5.87}$$

$$\overline{i^2_{n,m37}} = 4KT\frac{\gamma_{37}}{\alpha_{37}}g_{m37} \tag{5.88}$$

$$\overline{i^2_{n,m38}} = 4KT\frac{\gamma_{38}}{\alpha_{38}}g_{m38} \tag{5.89}$$

$$\overline{i^2_{n,m39}} = 4KT\frac{\gamma_{39}}{\alpha_{39}}g_{m39} \tag{5.90}$$

$$\overline{i^2_{n,m40}} = 4KT\frac{\gamma_{40}}{\alpha_{40}}g_{m40} \tag{5.91}$$

$$\overline{i^2_{n,m41}} = 4KT\frac{\gamma_{41}}{\alpha_{41}}g_{m41} \tag{5.92}$$

$$\overline{i^2_{n,m42}} = 4KT\frac{\gamma_{42}}{\alpha_{42}}g_{m42} \tag{5.93}$$

$$\overline{i^2_{\text{n,m43}}} = 4KT\frac{\gamma_{43}}{\alpha_{43}}g_{\text{m43}} \tag{5.94}$$

$$\overline{i^2_{\text{n,m44}}} = 4KT\frac{\gamma_{44}}{\alpha_{44}}g_{\text{m44}} \tag{5.95}$$

$$\overline{i^2_{\text{n,m45}}} = 4KT\frac{\gamma_{45}}{\alpha_{45}}g_{\text{m45}} \tag{5.96}$$

$$\overline{i^2_{\text{n,m46}}} = 4KT\frac{\gamma_{46}}{\alpha_{46}}g_{\text{m46}} \tag{5.97}$$

$$\overline{i^2_{\text{n,m47}}} = 4KT\frac{\gamma_{47}}{\alpha_{47}}g_{\text{m47}} \tag{5.98}$$

$$\overline{i^2_{\text{n,m48}}} = 4KT\frac{\gamma_{48}}{\alpha_{48}}g_{\text{m48}} \tag{5.49}$$

$$\overline{i^2_{\text{n,m49}}} = 4KT\frac{\gamma_{49}}{\alpha_{49}}g_{\text{m49}} \tag{5.50}$$

$$\overline{i^2_{\text{n,m50}}} = 4KT\frac{\gamma_{50}}{\alpha_{50}}g_{\text{m50}} \tag{5.51}$$

$$\overline{i^2_{\text{n,m51}}} = 4KT\frac{\gamma_{51}}{\alpha_{51}}g_{\text{m51}} \tag{5.52}$$

$$\overline{i^2_{\text{n,m52}}} = 4KT\frac{\gamma_{52}}{\alpha_{52}}g_{\text{m52}} \tag{5.53}$$

$$\overline{i^2_{\text{n,m53}}} = 4KT\frac{\gamma_{53}}{\alpha_{53}}g_{\text{m53}} \tag{5.54}$$

$$\overline{i^2_{\text{n,m54}}} = 4KT\frac{\gamma_{54}}{\alpha_{54}}g_{\text{m54}} \tag{5.55}$$

$$\overline{i^2_{\text{n,r}_{1a}}} = 4KT\frac{1}{R_{1a}} \tag{5.56}$$

$$\overline{i^2_{\text{n,r}_{1b}}} = 4KT\frac{1}{R_{1b}} \tag{5.57}$$

$$\overline{i^2_{\text{n,r}_{2a}}} = 4KT\frac{1}{R_{2a}} \tag{5.58}$$

$$\overline{i^2_{n,r_{2b}}} = 4KT\frac{1}{R_{2b}} \tag{5.59}$$

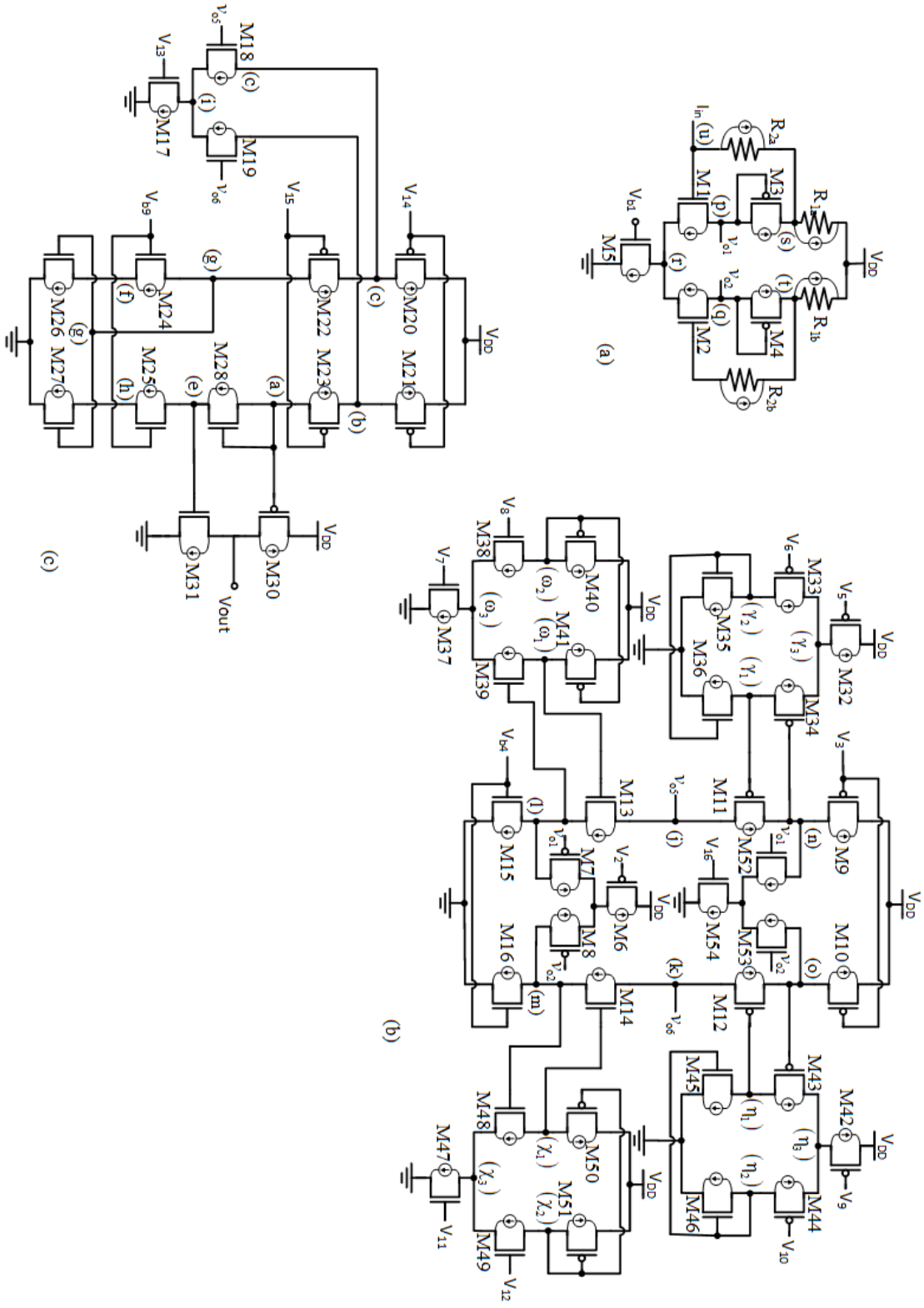



Fig. 5.19 Noise inserted (noise perturbed) diagram of the proposed $g_m$-boosted doubly folded push-pull TIA circuit, (a) single-ended to differential conversion stage, (b) $g_m$-boosted fully differential folded-cascode voltage amplifier stage, (c) differential input to single-ended output

Firstly, looking from the last stage at point (a), the input noise voltage power spectral density is the sum of the input noise voltage power spectral density referred to the gate of transistor M30 and M28 which is given by,

$$\overline{v^2_{\text{n,in-a}}} = \frac{\overline{i^2_{\text{n,m30}}}}{g^2_{\text{m30}}} + \frac{\overline{i^2_{\text{n,m28}}}}{g^2_{\text{m28}}} \tag{5.60}$$

And the input noise current spectral density across transistor M23 is given by,

$$\overline{i^2_{\text{n,in-a}}} = \overline{v^2_{\text{n,in-a}}} \left(2\pi f\right)^2 \left(C_{\text{dg23}} + C_{\text{db23}} + C_{\text{db28}} + C_{\text{dg30}} + C_{\text{gs30}}\right)^2 \tag{5.61}$$

At point (b), the input noise current spectral density is the sum of the input noise current spectral density at point (a) and from transistor M21,

$$\overline{i^2_{\text{n,in-b}}} = \overline{i^2_{\text{n,in-a}}} + \overline{i^2_{\text{n,in-m21}}} \tag{5.62}$$

Half the noise power at point (i), attributable to M19 source, the input noise current power spectral density is given by the sum of half input noise current power spectral density of transistor M17 and the input noise current power spectral density at point (b),

$$\begin{aligned} \frac{1}{2}\overline{i^2_{\text{n,in-i}}} &= \left(\frac{\sqrt{\overline{i^2_{\text{n,m17}}}}}{2}\right)^2 + \overline{i^2_{\text{n,in-b}}} \\ &= \frac{\overline{i^2_{\text{n,m17}}}}{4} + \overline{i^2_{\text{n,in-b}}} \end{aligned} \tag{5.63}$$

Then, at the point (k), the noise voltage power spectral density is the sum of its at point (i) and transistor M19, which is given by,

$$\overline{v^2_{\text{n,in-k}}} = \left(\frac{\overline{i^2_{\text{n,m17}}}}{4} + \overline{i^2_{\text{n,b}}}\right) \frac{1}{\left(g_{\text{m18}} + g_{\text{m19}}\right)^2} + \frac{\overline{i^2_{\text{n,m19}}}}{g^2_{\text{m19}}} \tag{5.64}$$

Here, half of this noise current power spectral density at point (k) is referred to the source of transistor M12 and the other half to transistor M14. Hence, the input noise current power spectral density at point (k) is given by,

$$\overline{i^2_{\text{n,in-k}}} = \overline{v^2_{\text{n,in-k}}} \left(2\pi f\right)^2 \left(C_{\text{gd12}} + C_{\text{db12}} + C_{\text{dg14}} + C_{\text{db14}} + C_{\text{gd19}} + C_{\text{gs19}}\right)^2 \tag{5.65}$$

And the input noise voltage power spectral density referred to the source of transistor M28 at point (e) is given by,

$$\overline{v^2_{\text{n,in-e}}} = \frac{\overline{i^2_{\text{n,m31}}}}{g^2_{\text{m31}}} \tag{5.66}$$

Thus, the input noise current power spectral density across transistor M25 can be written as,

$$\overline{i^2_{\text{n,in-e}}} = \overline{v^2_{\text{n,in-e}}}\left(2\pi f\right)^2\left(C_{\text{gd31}} + C_{\text{gs31}} + C_{\text{gs28}} + C_{\text{sb28}} + C_{\text{dg25}} + C_{\text{db25}}\right)^2 \tag{5.67}$$

Next, the total input noise current power spectral density at point (g) is the sum of the noise current power spectral density at point (e) and transistor M27,

$$\overline{i^2_{\text{n,in-h}}} = \overline{i^2_{\text{n,in-e}}} + \overline{i^2_{\text{n,m27}}} \tag{5.68}$$

And the total input noise voltage power spectral density at point (g) is given by the sum of noise current power spectral density across transistors M27 and M26,

$$\overline{v^2_{\text{n,in-g}}} = \frac{\overline{i^2_{\text{n,in-h}}}}{g^2_{\text{m27}}} + \frac{\overline{i^2_{\text{n,m26}}}}{g^2_{\text{m26}}} \tag{5.69}$$

The input referred noise voltage of transistor M24 and M25 as well as the low voltage cascode bias circuit are not in the path of the TIA input. Therefore, the input referred current power spectral density is given by,

$$\overline{i^2_{\text{n,in-g}}} = \overline{v^2_{\text{n,in-g}}}\left(2\pi f\right)^2\left(C_{\text{gs26}} + C_{\text{gd26}} + C_{\text{gs27}} + C_{\text{gd27}} + C_{\text{dg24}} + C_{\text{db24}} + C_{\text{dg22}} + C_{\text{db22}}\right)^2 \tag{5.70}$$

At the point (c), the input referred noise current spectral density is the sum of the current power spectral density referred to the drain of transistor M20 and at point (g) which is given by,

$$\overline{i^2_{\text{n,in-c}}} = \overline{i^2_{\text{n,in-g}}} + \overline{i^2_{\text{n,m20}}} \tag{5.71}$$

Next, half of the noise current power spectral density at point (i) attributable to M18 source is given by,

$$\frac{1}{2}\overline{i^2_{\text{n,in-i}}} = \left(\frac{\sqrt{\overline{i^2_{\text{n,m17}}}}}{2}\right)^2 + \overline{i^2_{\text{n,in-c}}} \tag{5.72}$$

Then the noise voltage power spectral density at point (j) is given by,

$$\overline{v^2_{\text{n,in-j}}} = \left(\frac{\overline{i^2_{\text{n,m17}}}}{4} + \overline{i^2_{\text{n,c}}}\right)\frac{1}{\left(g_{\text{m18}} + g_{\text{m19}}\right)^2} + \frac{\overline{i^2_{\text{n,m18}}}}{g^2_{\text{m18}}} \tag{5.73}$$

Noise of transistor M22 and M23 referred drain current to input is not in the path of the TIA input. It also cannot be referred to the source of the devices. Thus, the total noise current power spectral density at point (j) is given by,

$$\overline{i^2_{\text{n,in-j}}} = \overline{v^2_{\text{n,in-j}}}\left(2\pi f\right)^2\left(C_{\text{dg11}} + C_{\text{db11}} + C_{\text{dg13}} + C_{\text{db13}}\right)^2 \tag{5.74}$$

Half of this can be referred to the source of M11 and the other half to the source of M13. The noise voltage power spectral density referred to the gate of M13 at point ($\omega_1$) is given by,

$$\overline{v^2_{\text{n,in-}\omega1}} = \frac{\overline{i^2_{\text{n,m13}}}}{g^2_{\text{m13}}} \tag{5.75}$$

And its noise current spectral density referred to the gate of M13 at point ($\omega_1$) is given by,

$$\overline{i^2_{\text{n,in-}\omega1}} = \overline{v^2_{\text{n,in-}\omega1}} \left(2\pi f\right)^2 \left(C_{\text{gd41}} + C_{\text{db41}} + C_{\text{db39}} + C_{\text{dg39}} + C_{\text{dg13}} + C_{\text{gs13}}\right)^2 \tag{5.76}$$

Hence, the noise voltage power referred to the gate of M40 and M41 at point ($\omega_2$) is given by,

$$\overline{v^2_{\text{n,in-}\omega2}} = \frac{\overline{i^2_{\text{n,m41}}}}{g^2_{\text{m41}}} + \frac{\overline{i^2_{\text{n,m40}}}}{g^2_{\text{m40}}} \tag{5.77}$$

Accordingly, the input referred noise current power spectral density at point ($\omega_2$) is given by,

$$\overline{i^2_{\text{n,in-}\omega2}} = \overline{v^2_{\text{n,in-}\omega2}} \left(2\pi f\right)^2 \left(C_{\text{db40}} + C_{\text{gd41}} + C_{\text{gs41}} + C_{\text{dg38}} + C_{\text{db38}}\right)^2 \tag{5.78}$$

At the point of ($\omega_3$), the input referred noise current spectral density is the sum of it at transistor M37 and the point of ($\omega_1$) and ($\omega_2$),

$$\overline{i^2_{\text{n,in-}\omega3}} = \overline{i^2_{\text{n,in-}\omega1}} + \overline{i^2_{\text{n,in-}\omega2}} + \overline{i^2_{\text{n,m37}}} \tag{5.79}$$

From inspection, at point ($\omega_3$) from differential amplifier $A_2$, the input referred noise voltage power spectral density can be written as,

$$\overline{v^2_{\text{n,in-}\omega3}} = \frac{\overline{i^2_{\text{n,in-}\omega3}}}{\left(g_{\text{m38}} + g_{\text{m39}}\right)^2} \tag{5.80}$$

Thus, at point (l), the input noise voltage power spectral density from differential amplifier $A_2$ is given by,

$$\overline{v^2_{\text{n,in-l}}} = \overline{v^2_{\text{n,}\omega3}} + \frac{\overline{i^2_{\text{n,m39}}}}{g^2_{\text{m39}}} \tag{5.81}$$

And by inspection, the total input referred noise current power spectral density at point (l) is given by,

$$\overline{i^2_{\text{n,l}}} = \frac{\overline{i^2_{\text{n,in-j}}}}{2} + \overline{i^2_{\text{n,m15}}} + \overline{v^2_{\text{n,in-l}}}\left(2\pi f\right)^2\left(C_{\text{gs13}} + C_{\text{sb13}} + C_{\text{dg15}} + C_{\text{db15}} + C_{\text{gd39}} + C_{\text{gs39}}\right)^2 \quad (5.82)$$

Half of the input referred noise voltage power at point (p) of the PMOS cascode circuit is the sum of the input referred noise voltage power spectral density at point (l) and transistor M7 as well as a half from the transistor M6 because of allocating half of $\overline{i^2_{\text{n,m6}}}$ to left and another half to the right, which can be expressed by,

$$\frac{1}{2}\overline{v^2_{\text{n,in-p1}}} = \left(\overline{i^2_{\text{n,in-l}}} + \frac{1}{2}\overline{i^2_{\text{n,in-m6}}}\right)\frac{1}{\left(g_{\text{m7}} + g_{\text{m8}}\right)^2} + \frac{\overline{i^2_{\text{n,m7}}}}{g^2_{\text{m7}}} \quad (5.83)$$

Here, the input referred noise voltage power spectral density at point ($\chi_1$) is given by,

$$\overline{v^2_{\text{n,in-}\chi\text{1}}} = \frac{\overline{i^2_{\text{n,m14}}}}{g^2_{\text{m14}}} \quad (5.84)$$

And input referred noise current power spectral density at point ($\chi_1$) is given by,

$$\overline{i^2_{\text{n,in-}\chi\text{1}}} = \overline{v^2_{\text{n,in-}\chi\text{1}}}\left(2\pi f\right)^2\left(C_{\text{gd51}} + C_{\text{db51}} + C_{\text{db49}} + C_{\text{dg49}} + C_{\text{gd14}} + C_{\text{gs14}}\right)^2 \quad (5.85)$$

The input referred noise voltage power spectral density referred to the gate of M50 and M51 at point ($\chi_2$) is given by,

$$\overline{v^2_{\text{n,in-}\chi\text{2}}} = \frac{\overline{i^2_{\text{n,m51}}}}{g^2_{\text{m51}}} + \frac{\overline{i^2_{\text{n,m50}}}}{g^2_{\text{m50}}} \quad (5.86)$$

And input referred noise current power spectral density at point ($\chi_2$) is given by,

$$\overline{i^2_{\text{n,in-}\chi\text{2}}} = \overline{v^2_{\text{n,in-}\chi\text{2}}}\left(2\pi f\right)^2\left(C_{\text{dg48}} + C_{\text{db48}} + C_{\text{db50}} + C_{\text{dg51}} + C_{\text{gs51}}\right)^2 \quad (5.87)$$

Thus, the input noise current power spectral density at point ($\chi_3$) is the sum of it at transistor M47 and point ($\chi_1$) and ($\chi_2$),

$$\overline{i^2_{\text{n,in-}\chi\text{3}}} = \overline{i^2_{\text{n,in-}\chi\text{1}}} + \overline{i^2_{\text{n,in-}\chi\text{2}}} + \overline{i^2_{\text{n,m47}}} \quad (5.88)$$

From inspection, at point ($\chi_3$), the input referred noise voltage power spectral density can be written as,

$$\overline{v^2_{\text{n,in-}\chi3}} = \frac{\overline{i^2_{\text{n,in-}\chi3}}}{\left(g_{\text{m48}} + g_{\text{m49}}\right)^2} \tag{5.89}$$

At point (m), the input referred noise voltage power spectral density from differential $A_2$ is given by,

$$\overline{v^2_{\text{n,in-m}}} = \overline{v^2_{\text{n,in-}\chi3}} + \frac{\overline{i^2_{\text{n,m49}}}}{g^2_{\text{m49}}} \tag{5.90}$$

And the input referred noise current power spectral density at point (m) from differential $A_2$ is given by,

$$\overline{i^2_{\text{n,in-m}}} = \overline{v^2_{\text{n,in-m}}}\left(2\pi f\right)^2\left(C_{\text{gs14}} + C_{\text{sb14}} + C_{\text{dg16}} + C_{\text{db16}} + C_{\text{gd49}} + C_{\text{gs49}}\right)^2 \tag{5.91}$$

From inspection, the total input noise current spectral density at point (m) is given by,

$$\overline{i^2_{\text{n,m}}} = \overline{i^2_{\text{n,in-m}}} + \frac{1}{2}\overline{i^2_{\text{n,in-k}}} + \overline{i^2_{\text{n,m16}}} \tag{5.92}$$

Similar to equation (5.83), half of the input referred noise voltage power spectral density at point (q) of the PMOS cascode circuit can be directly written as,

$$\frac{1}{2}\overline{v^2_{\text{n,in-q1}}} = \left(\overline{i^2_{\text{n,in-m}}} + \frac{1}{2}\overline{i^2_{\text{n,m6}}}\right)\frac{1}{\left(g_{\text{m7}} + g_{\text{m8}}\right)^2} + \frac{\overline{i^2_{\text{n,m8}}}}{g^2_{\text{m8}}} \tag{5.93}$$

And the input referred noise voltage power spectral density at point ($\gamma_1$) is given by,

$$\overline{v^2_{\text{n,in-}\gamma1}} = \frac{\overline{i^2_{\text{n,m11}}}}{g^2_{\text{m11}}} \tag{5.94}$$

Thus, the input referred noise current power spectral density at point ($\gamma_1$) is given by,

$$\overline{i^2_{\text{n,in-}\gamma1}} = \overline{v^2_{\text{n,in-}\gamma1}}\left(2\pi f\right)^2\left(C_{\text{dg34}} + C_{\text{db34}} + C_{\text{db36}} + C_{\text{dg36}} + C_{\text{gs11}} + C_{\text{db11}}\right)^2 \tag{5.95}$$

Next, the noise voltage power spectral density referred to the gate of transistors M35 and M36 at point ($\gamma_2$) is given by,

$$\overline{v^2_{\text{n,in-}\gamma2}} = \frac{\overline{i^2_{\text{n,m35}}}}{g^2_{\text{m35}}} + \frac{\overline{i^2_{\text{n,m36}}}}{g^2_{\text{m36}}} \tag{5.96}$$

Accordingly, the input referred noise current power spectral density at point ( $\gamma_2$ ) is given below,

$$\overline{i^2_{\text{n,in-}\gamma 2}} = \overline{v^2_{\text{n,in-}\gamma 2}} \left(2\pi f\right)^2 \left(C_{\text{db35}} + C_{\text{gs36}} + C_{\text{gd36}} + C_{\text{dg33}} + C_{\text{dg33}} + C_{\text{db33}}\right)^2 \tag{5.97}$$

Therefore, the input noise current power spectral density at the point of ( $\gamma_3$ ) is the sum of it at transistor M32 and point ( $\gamma_1$ ) and ( $\gamma_2$ ),

$$\overline{i^2_{\text{n,in-}\gamma 3}} = \overline{i^2_{\text{n,in-}\gamma 1}} + \overline{i^2_{\text{n,in-}\gamma 2}} + \overline{i^2_{\text{n,m32}}} \tag{5.98}$$

And the input noise voltage power spectral density at point ( $\gamma_3$ ) is given,

$$\overline{v^2_{\text{n,in-}\gamma 3}} = \frac{\overline{i^2_{\text{n,in-}\gamma 3}}}{\left(g_{\text{m33}} + g_{\text{m34}}\right)^2} \tag{5.99}$$

Here, the input referred noise voltage power spectral density at point (m) from differential $A_2$ is the sum of them at point ( $\gamma_3$ ) and transistor M34 which is given below,

$$\overline{v^2_{\text{n,in-n}}} = \overline{v^2_{\text{n,in-}\gamma 3}} + \frac{\overline{i^2_{\text{n,m34}}}}{g^2_{\text{m34}}} \tag{5.100}$$

And the input noise current power spectral density at point (n) from differential $A_2$ is given by,

$$\overline{i^2_{\text{n,in-n}}} = \overline{v^2_{\text{n,in-n}}} \left(2\pi f\right)^2 \left(C_{\text{gs34}} + C_{\text{gd34}} + C_{\text{dg9}} + C_{\text{db9}} + C_{\text{sg11}} + C_{\text{sb11}}\right)^2 \tag{5.101}$$

By inspection, the total input referred noise current power at point (n) can be directly written as,

$$\overline{i^2_{\text{n,n}}} = \frac{\overline{i^2_{\text{n,in-j}}}}{2} + \overline{i^2_{\text{n,m9}}} + \overline{i^2_{\text{n,in-n}}} \tag{5.102}$$

Then, half of the input referred noise voltage power at point (p) of the NMOS folded cascode circuit can be directly written as,

$$\frac{1}{2}\overline{v^2_{\text{n,in-p2}}} = \left(\overline{i^2_{\text{n,in-n}}} + \frac{1}{2}\overline{i^2_{\text{n,in-m54}}}\right) \frac{1}{\left(g_{\text{m52}} + g_{\text{m53}}\right)^2} + \frac{\overline{i^2_{\text{n,m52}}}}{g^2_{\text{m52}}} \tag{5.103}$$

Next, the noise voltage power referred to the gate of M35 and M36 at point ( $\eta_1$ ) is given by,

$$\overline{v^2_{\text{n,in-}\eta 1}} = \frac{\overline{i^2_{\text{n,m12}}}}{g^2_{\text{m12}}} \tag{5.104}$$

And the input referred noise current power spectral density at point ( $\eta_1$ )is given by,

$$\overline{i^2_{\text{n,in-}\eta1}} = \overline{v^2_{\text{n,in-}\eta1}}\left(2\pi f\right)^2\left(C_{\text{gd43}} + C_{\text{db43}} + C_{\text{gd45}} + C_{\text{db45}} + C_{\text{gs12}} + C_{\text{gd12}}\right)^2 \tag{5.105}$$

The input referred noise voltage power spectral density referred to the gate of M45 and M46 at point ( $\eta_2$ ) is given by,

$$\overline{v^2_{\text{n,in-}\eta2}} = \frac{\overline{i^2_{\text{n,m45}}}}{g^2_{\text{m45}}} + \frac{\overline{i^2_{\text{n,m46}}}}{g^2_{\text{m46}}} \tag{5.106}$$

From the equation above, the input referred noise current power spectral density at point ( $\eta_2$ )is given by,

$$\overline{i^2_{\text{n,in-}\eta2}} = \overline{v^2_{\text{n,in-}\eta2}}\left(2\pi f\right)^2\left(C_{\text{db46}} + C_{\text{db44}} + C_{\text{dg45}} + C_{\text{gd45}}\right)^2 \tag{5.107}$$

Thus, the input referred noise current power spectral density at point ( $\eta_3$ ) is the sum of it at transistor M42 and point of ( $\eta_1$ ) and ( $\eta_2$ ),

$$\overline{i^2_{\text{n,}\eta3}} = \overline{i^2_{\text{n,in-}\eta1}} + \overline{i^2_{\text{n,in-}\eta2}} + \overline{i^2_{\text{n,m42}}} \tag{5.108}$$

And the input referred noise voltage power spectral density at point ( $\eta_3$ ) is given,

$$\overline{v^2_{\text{n,}\eta3}} = \frac{\overline{i^2_{\text{n,}\eta3}}}{\left(g_{\text{m43}} + g_{\text{m44}}\right)^2} \tag{5.109}$$

Next, the input referred noise voltage power spectral density at point (o) from differential $A_1$ is the sum of them at point ( $\eta_3$ ) and transistor M43 which is given below,

$$\overline{v^2_{\text{n,in-o}}} = \overline{v^2_{\text{n,}\eta3}} + \frac{\overline{i^2_{\text{n,m43}}}}{g^2_{\text{m43}}} \tag{5.110}$$

And the input referred noise current power spectral density at point (o) from differential $A_1$ is given by,

$$\overline{i^2_{\text{n,in-o}}} = \overline{v^2_{\text{n,in-o}}}\left(2\pi f\right)^2\left(C_{\text{sb12}} + C_{\text{sg12}} + C_{\text{dg10}} + C_{\text{db10}} + C_{\text{gs43}} + C_{\text{dg43}}\right)^2 \tag{5.111}$$

By inspection, the total input referred noise current power at point (n) can be directly written as,

$$\overline{i^2_{\text{n,o}}} = \overline{i^2_{\text{n,in-o}}} + \frac{1}{2}\overline{i^2_{\text{n,in-k}}} + \overline{i^2_{\text{n,m10}}} \tag{5.112}$$

Then, half of the input referred noise voltage power spectral density at point (q) of the NMOS folded cascode circuit can be directly written as,

$$\frac{1}{2}\overline{v^2_{\text{n,in-q2}}} = \left(\overline{i^2_{\text{n,o}}} + \frac{1}{2}\overline{i^2_{\text{n,m54}}}\right)\frac{1}{\left(g_{\text{m52}} + g_{\text{m53}}\right)^2} + \frac{\overline{i^2_{\text{n,m53}}}}{g^2_{\text{m53}}} \tag{5.113}$$

Then using equations (5.113) and (5.93), the total input referred noise voltage power spectral density at point (q) is given by,

$$\overline{v^2_{\text{n,in-q}}} = \frac{1}{2}\overline{v^2_{\text{n,in-q2}}} + \frac{1}{2}\overline{v^2_{\text{n,in-q1}}} \tag{5.114}$$

Also, using equations (5.103) and (5.83), the total input referred noise voltage power spectral density at point (p) is given by,

$$\overline{v^2_{\text{n,in-p}}} = \frac{1}{2}\overline{v^2_{\text{n,in-p2}}} + \frac{1}{2}\overline{v^2_{\text{n,in-p1}}} \tag{5.115}$$

And the input referred noise current power spectral density at point (p) can be found as,

$$\overline{i^2_{\text{n,in-p}}} = \overline{v^2_{\text{n,in-p}}}\left(2\pi f\right)^2\left(C_{\text{db3}} + C_{\text{db1}} + C_{\text{dg1}} + C_{\text{gs7}} + C_{\text{gd7}} + C_{\text{gs52}} + C_{\text{gd52}}\right)^2 \tag{5.116}$$

Now, move to stage one, at point (s), the input referred noise voltage power spectral density from resistor $R_{1a}$ and $R_{2a}$ can be written as,

$$\overline{v^2_{\text{n,s}}} = \overline{i^2_{\text{n,R1a}}} \times R^2_{\text{1a}} + \overline{i^2_{\text{n,R2a}}} \times R^2_{\text{2a}} \tag{5.117}$$

And the input noise voltage power spectral density produced by transistor M3 is given by,

$$\overline{v^2_{\text{n,in-m3-p}}} = \frac{\overline{i^2_{\text{n,m3}}}}{g^2_{\text{m3}}} \tag{5.118}$$

The input referred noise voltage spectral density at point (p) is the same as it at point (s),

$$\overline{v^2_{\text{n,p}}} = \overline{v^2_{\text{n,s}}} \tag{5.119}$$

And the input referred noise current spectral density at point (p) is given by,

$$\overline{i^2_{\text{n,p}}} = \overline{i^2_{\text{n,in-p}}} + \left(\overline{v^2_{\text{n,p}}} + \overline{v^2_{\text{n,in-m3-p}}}\right)\left(2\pi f\right)^2\begin{pmatrix} C_{\text{db3}} + C_{\text{db1}} + C_{\text{dg1}} + C_{\text{gs7}} \\ + C_{\text{gd7}} + C_{\text{gs52}} + C_{\text{gd52}} \end{pmatrix}^2 \tag{5.120}$$

Since a single-to-differential converter is symmetrical, the right half of the circuit is the same as the left half. Thus, the input referred noise voltage power spectral density from resistor $R_{1b}$ and $R_{2b}$ can be written as,

$$\overline{v^2_{\text{n,R1b,R2b}}} = \overline{i^2_{\text{n,R1b}}} \times R^2_{\text{1b}} + \overline{i^2_{\text{n,R2b}}} \times R^2_{\text{2b}} \tag{5.121}$$

Next, the noise voltage power spectral density referred to the gate of M2 is given by,

$$\overline{v^2_{\text{n,m2}}} = \frac{\overline{i^2_{\text{n,m2}}}}{g^2_{\text{m2}}} \tag{5.122}$$

Then the input noise current power spectral density referred to the gate of M2 is given by,

$$\overline{i^2_{\text{n,m2}}} = \overline{v^2_{\text{n,m2}}} \left(2\pi f\right)^2 \left(C_{\text{gd2}} + C_{\text{gs2}}\right)^2 \tag{5.123}$$

The input referred noise voltage power spectral density due to the noise current power of M2 across the resistor at point (t) can be presented as,

$$\overline{v^2_{\text{n,tm2}}} = \overline{i^2_{\text{n,m2}}} \times R^2_{\text{1b}} + \overline{i^2_{\text{n,m2}}} \times R^2_{\text{2b}} \tag{5.124}$$

Thus, the total input referred noise voltage power spectral density at point (t) is given by,

$$\overline{v^2_{\text{n,in-t}}} = \overline{v^2_{\text{n,R1b,R2b}}} + \overline{v^2_{\text{n,tm2}}} \tag{5.125}$$

And the input referred noise current power spectral density at point (q) is given by,

$$\overline{i^2_{\text{n,q}}} = \overline{v^2_{\text{n,t}}} \left(2\pi f\right)^2 \left(C_{\text{dg4}} + C_{\text{db4}} + C_{\text{db2}} + C_{\text{dg2}}\right)^2 \tag{5.126}$$

Hence, the total input referred noise current spectral density arrived at point (r) is the sum of it from transistor M5 and at the point (p) as well as (q),

$$\overline{i^2_{\text{n,r}}} = \overline{i^2_{\text{n,p}}} + \overline{i^2_{\text{n,q}}} + \overline{i^2_{\text{n,m5}}} \tag{5.127}$$

And the input noise voltage power spectral density at point (t) is given by,

$$\overline{v^2_{\text{n,r}}} = \overline{i^2_{\text{n,r}}} \frac{1}{\left(g_{\text{m1}} + g_{\text{m2}}\right)^2} \tag{5.128}$$

Therefore, the final input referred noise voltage and current power spectral density at point (u) is given by,

$$\overline{v^2_{\text{n,in-u}}} = \overline{v^2_{\text{n,r}}} + \frac{\overline{i^2_{\text{n,m1}}}}{g^2_{\text{m1}}} + \overline{i^2_{\text{n,R2a}}} \times R^2_{\text{2a}} \tag{5.129}$$

$$\overline{i^2_{\text{n,in-u}}} = \overline{v^2_{\text{n,in-u}}} \left[ \frac{1}{R^2_{\text{2a}}} + \left(2\pi f\right)^2 \left(C_{\text{gs1}} + C_{\text{gd1}}\right)^2 \right] \tag{5.130}$$

## 5.4 Simulation Results

Fig. 5.20 shows the transient sinusoidal response of the proposed single-to-differential converter. As be seen in this figure, the two outputs waveforms have a similar magnitude and opposite polarity.

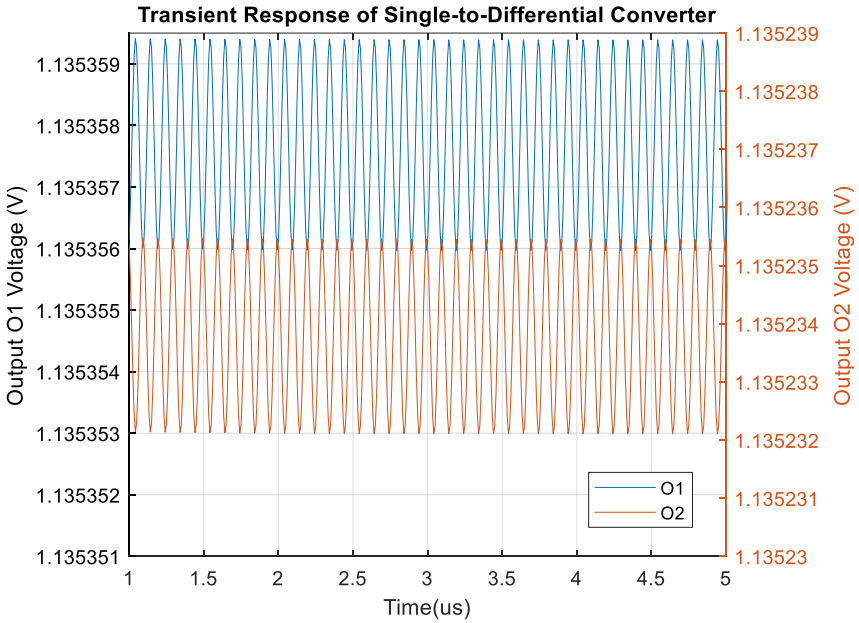



Fig. 5.20 Transient response of proposed single-to-differential converter.

Fig. 5.21 shows the transient sinusoidal response of proposed $g_m$-boosted doubly folded push-pull TIA for a nominal 10MHz input signal. As shown in this figure, the peak-to-peak output voltage swing is around 100mV for a test input current of 1nA.

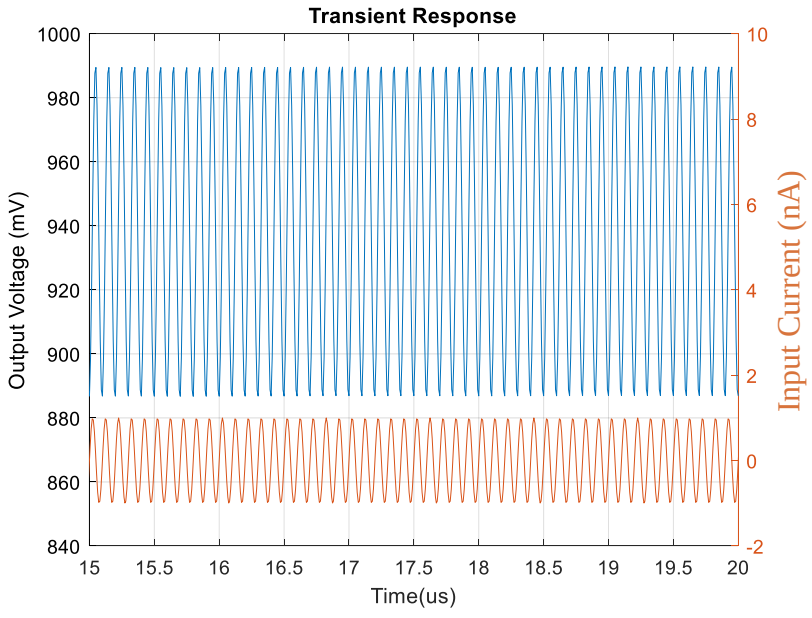



Fig. 5.21 Transient response of $g_m$-boosted doubly folded push-pull TIA.

Fig. 5.22 shows that transimpedance gain of $g_m$-boosted doubly folded push-pull TIA which is 217.8dB and its -3-dB bandwidth is 211kHz.

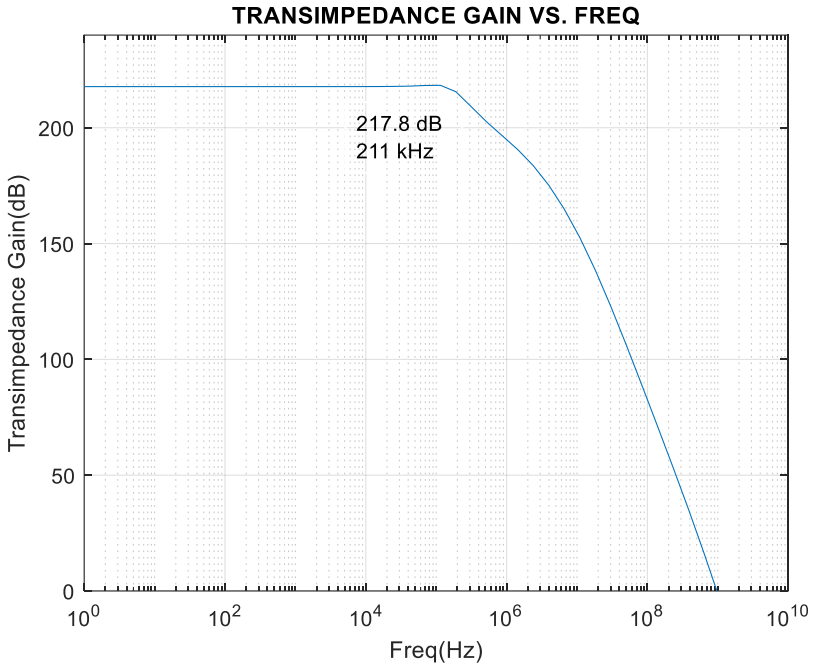



Fig. 5.22 AC analysis simulation of transimpedance gain for $g_m$-boosted doubly folded push-pull TIA.

Fig. 5.23 indicates the input referred noise current spectral density function of $g_m$-boosted doubly folded push-pull TIA and the average is around 159.8 pA/sqrt (Hz) within the TIA bandwidth.

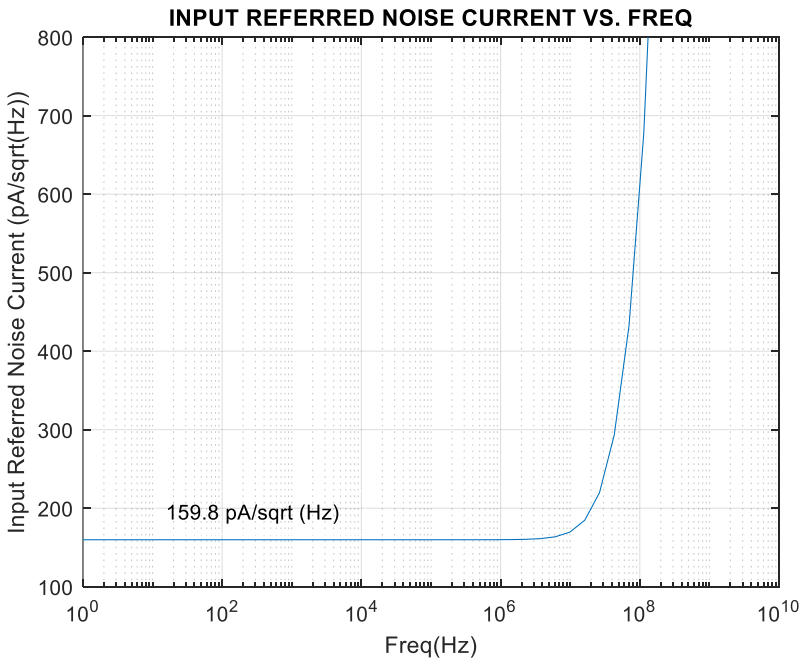



Fig. 5.23 Input referred noise current of $g_m$-boosted doubly folded push-pull TIA.

Fig. 5.24 shows the results of eye diagram simulations using -229 dBm input photodiode current signal and a $2^{31}$-1 pseudo random bit sequence (PRBS) data pattern. It displays an eye opening of 90% at 100kbit/s.

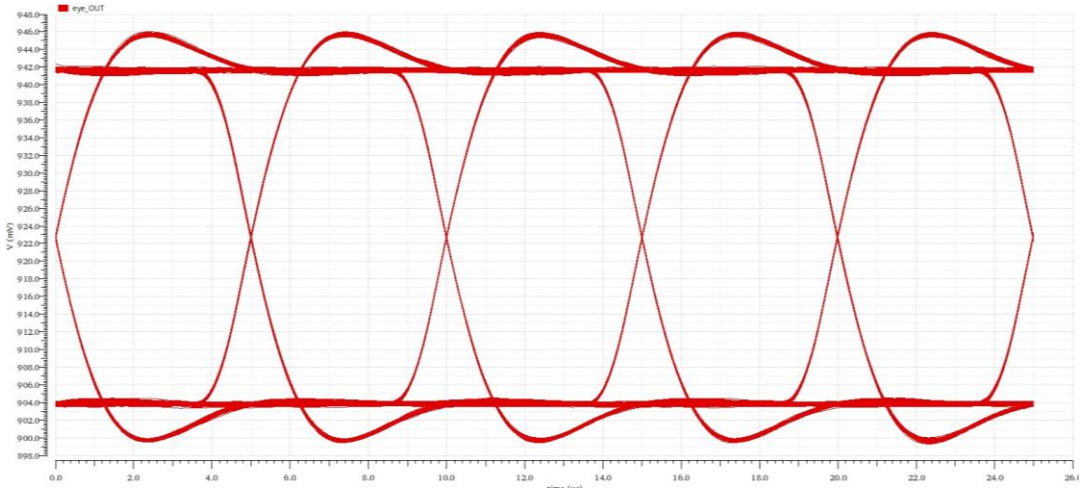



Fig. 5.24 Eye diagram of $g_m$-boosted doubly folded push-pull TIA.

## 5.5 Layout

Fig. 5.25 shows the masked layout for $g_m$-boosted doubly folded push-pull TIA which occupies 55 × 57 μm$^2$ of silicon area.

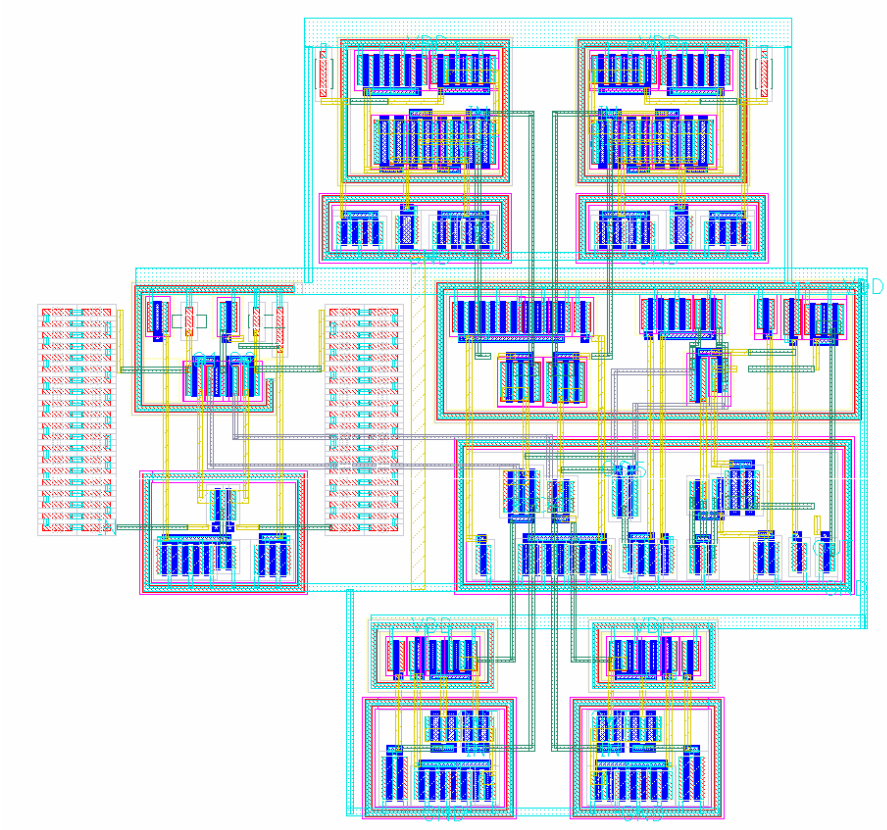


Fig. 5.25 Layout of $g_m$-boosted doubly folded push-pull TIA.

# Chapter 6 $g_m$-boosted Multiple Stage Transimpedance Amplifier with Bandwidth Extension

This chapter describes a novel $g_m$-boosted multiple stage TIA with bandwidth extension technique by adding an inductor. Theoretical analysis such as its gain and noise analysis are developed. And its simulation results indicated the transimpedance gain is 73.71 dB with a -3 dB bandwidth of 38.69 MHz. By adding the inductor, the -3 dB bandwidth has extended 17%. The input referred noise current spectral density is below 50 pA/sqrt (Hz). Eye diagram simulation using -123 dBm input photodiode current signal and a $2^{31}$-1 pseudo random bit sequence data pattern shows an eye opening of 95% at 15 Mbit/s.

## 6.1 Topology of $g_m$-boosted Multiple Stage Inductively Peaked TIA

The topology of the proposed $g_m$-boosted CG multiple stage TIA with inductive bandwidth extension technique and its bias voltage circuit are shown in Fig. 6.1 and Fig. 6.2. It consists of three stages: (a) a common gate transimpedance amplifier stage, (b) a $g_m$-boosted voltage gain stage consisting of a cascode stage and a cascode stage with inductive bandwidth extension technique and (c) a low-impedance source-follower stage. The input common gate stage has low noise and low input impedance which has a wide-band behaviour [66].

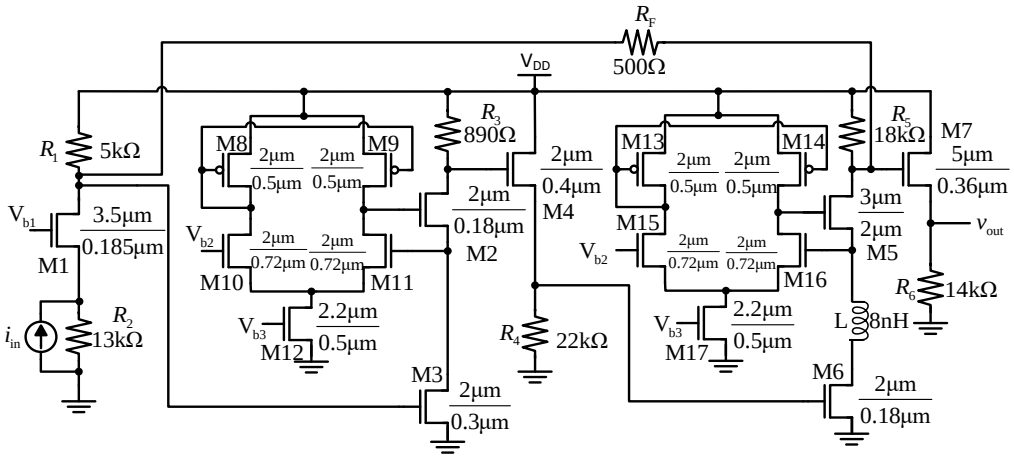



Fig. 6.1 Schematic of proposed $g_m$-boosted multiple stage inductively peaked TIA.

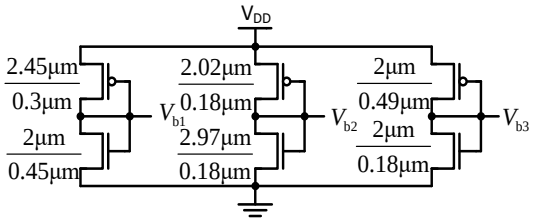



Fig. 6.2 Biasing circuit of $g_m$-boosted multiple stage inductively peaked TIA.

## 6.2 Analysis of Mid-band Transimpedance Gain

The open-loop mid-band gain of the $g_m$-boosted multiple stage inductively peaked TIA can be derived using an open-loop AC equivalent schematic in Fig. 6.3 with feedback loading effect [47]. To simplify the circuit, $g_m$-boosters are represented by triangle symbols with voltage gain $A_2$ and all the DC voltages are AC shorted to ground. In addition, the feedback factor β can be written as $1/ R_F$ [47].

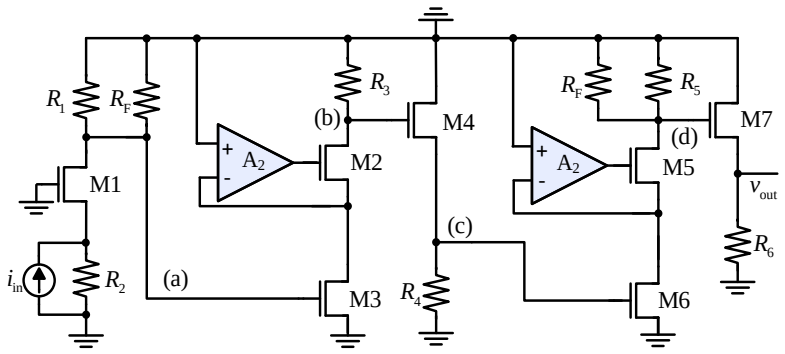



Fig. 6.3 Open-loop AC equivalent circuit for $g_m$-boosted multiple stage inductively peaked TIA.

For the input common gate stage, the output voltage at point (a) is given by,

$$v_{(a)} = i_{in} \frac{R_2}{R_2 + \dfrac{1}{g_{m1}} + R_1 \| R_F} \left( R_1 \| R_F \right) \tag{6.01}$$

Hence, the transimpedance gain of the first stage can be written as,

$$\frac{v_{(a)}}{i_{in}} = \frac{R_2 \left( R_1 \| R_F \right)}{R_2 + \dfrac{1}{g_{m1}} + R_1 \| R_F} \tag{6.02}$$

In the next $g_m$-boosted cascode stage, according to equations (3.12) and (3.13), the composite trans-conductance and output impedance is given by the equations below by inspection,

$$G_{m1} = -\frac{g_{m3} r_{o3} \left\{ \left[ \left( A_2 + 1 \right) g_{m2} + g_{mb2} \right] r_{o2} + 1 \right\}}{r_{o3} + r_{o3} \left[ \left( A_2 + 1 \right) g_{m2} + g_{mb2} \right] r_{o2} + r_{o2}} \tag{6.03}$$

$$R_{out1} = \left\{ r_{o3} + r_{o3} \left[ \left( A_2 + 1 \right) g_{m2} + g_{mb2} \right] r_{o2} + r_{o2} \right\} \| R_3 \tag{6.04}$$

Thus, the voltage gain from point (a) to (b) is given by the product of the transconductance $G_{m1}$ and output impedance $R_{out1}$,

$$\frac{v_{(b)}}{v_{(a)}} = G_{m1} R_{out1} \tag{6.05}$$

The next stage is a source follower, and the voltage gain can be written as [47],

$$\frac{v_{(c)}}{v_{(b)}} = -g_{m4}r_{o4} \tag{6.06}$$

Then it follows by a cascode stage, and the composite transconductance and output impedance are given by,

$$G_{m2} = -\frac{g_{m6}r_{o6}\left\{\left[\left(A_2+1\right)g_{m5}+g_{mb5}\right]r_{o5}+1\right\}}{r_{o6}+r_{o6}\left[\left(A_2+1\right)g_{m5}+g_{mb5}\right]r_{o5}+r_{o5}} \tag{6.07}$$

$$R_{out2} = \left\{r_{o6}+r_{o6}\left[\left(A_2+1\right)g_{m5}+g_{mb5}\right]r_{o5}+r_{o5}\right\} \| R_5 \| R_F \tag{6.08}$$

Therefore, the voltage gain from point (c) to point (d) is given by the product of transconductance $G_{m2}$ and output impedance $R_{out2}$,

$$\frac{v_{(d)}}{v_{(c)}} = G_{m2}R_{out2} \tag{6.09}$$

In the last output source follower stage, the voltage gain is following the same with equation (6.06) which is given by,

$$\frac{v_{out}}{v_{(d)}} = -g_{m7}r_{o7} \tag{6.10}$$

Thus, the open-loop mid-band transimpedance gain is the product of the gain from each stage which is given by,

$$\begin{aligned} Z_{open} &= \frac{v_{(a)}}{i_{in}}\frac{v_{(b)}}{v_{(a)}}\frac{v_{(c)}}{v_{(b)}}\frac{v_{(d)}}{v_{(c)}}\frac{v_{out}}{v_{(d)}} \\ &= \frac{R_2\left(R_1 \| R_F\right)}{R_2+\dfrac{1}{g_{m1}}+R_1 \| R_F}G_{m1}R_{out1}G_{m2}R_{out2}g_{m4}r_{o4}g_{m7}r_{o7} \end{aligned} \tag{6.11}$$

And the closed-loop gain is given by,

$$Z_{closed} = \frac{Z_{open}}{1+\beta Z_{open}} \tag{6.12}$$

Using equation (3.01) and (6.11),

$$Z_{\text{open}} = \frac{\dfrac{R_2\left(R_1 \| R_F\right)}{R_2 + \dfrac{1}{g_{m1}} + R_1 \| R_F} G_{m1} R_{out1} G_{m2} R_{out2} g_{m4} r_{o4} g_{m7} r_{o7}}{1 + \dfrac{1}{R_F} \dfrac{R_2\left(R_1 \| R_F\right)}{R_2 + \dfrac{1}{g_{m1}} + R_1 \| R_F} G_{m1} R_{out1} G_{m2} R_{out2} g_{m4} r_{o4} g_{m7} r_{o7}} \tag{6.13}$$

After simplification,

$$Z_{\text{open}} = \frac{R_F R_2\left(R_1 \| R_F\right) G_{m1} R_{out1} G_{m2} R_{out2} g_{m4} r_{o4} g_{m7} r_{o7}}{R_F\left(R_2 + \dfrac{1}{g_{m1}} + R_1 \| R_F\right) + R_2\left(R_1 \| R_F\right) G_{m1} R_{out1} G_{m2} R_{out2} g_{m4} r_{o4} g_{m7} r_{o7}} \tag{6.14}$$

## 6.3 Input Referred Noise Analysis

In this section, only considering the thermal noise, theoretical analysis of the input referred current spectral density of proposed TIA is discussed. Fig 6.4 shows the noise inserted (noise perturbed) circuit diagram for the proposed $g_m$-boosted multiple stage inductively peaked TIA. Following the same principle in equation (3.23) and (3.24), the noise current power density of MOSFETs and resistors from Fig. 6.4 are given below,

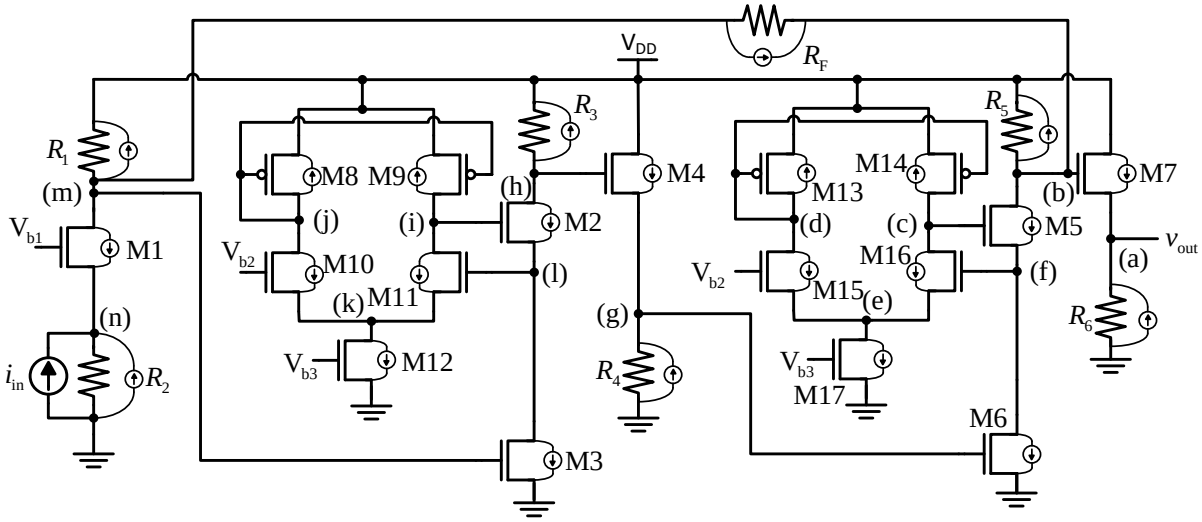



Fig. 6.4 Noise inserted (noise perturbed) circuit diagram of $g_m$-boosted multiple stage inductively peaked TIA.

$$\overline{i^2_{n,m1}} = 4KT\frac{\gamma_1}{\alpha_1} g_{m1} \tag{6.15}$$

$$\overline{i^2_{n,m2}} = 4KT\frac{\gamma_2}{\alpha_2}g_{m2} \tag{6.16}$$

$$\overline{i^2_{n,m3}} = 4KT\frac{\gamma_3}{\alpha_3}g_{m3} \tag{6.17}$$

$$\overline{i^2_{n,m4}} = 4KT\frac{\gamma_4}{\alpha_4}g_{m4} \tag{6.18}$$

$$\overline{i^2_{n,m5}} = 4KT\frac{\gamma_5}{\alpha_5}g_{m5} \tag{6.19}$$

$$\overline{i^2_{n,m6}} = 4KT\frac{\gamma_6}{\alpha_6}g_{m6} \tag{6.20}$$

$$\overline{i^2_{n,m7}} = 4KT\frac{\gamma_7}{\alpha_7}g_{m7} \tag{6.21}$$

$$\overline{i^2_{n,m8}} = 4KT\frac{\gamma_8}{\alpha_8}g_{m8} \tag{6.22}$$

$$\overline{i^2_{n,m9}} = 4KT\frac{\gamma_9}{\alpha_9}g_{m9} \tag{6.23}$$

$$\overline{i^2_{n,m10}} = 4KT\frac{\gamma_{10}}{\alpha_{10}}g_{m10} \tag{6.24}$$

$$\overline{i^2_{n,m11}} = 4KT\frac{\gamma_{11}}{\alpha_{11}}g_{m11} \tag{6.25}$$

$$\overline{i^2_{n,m12}} = 4KT\frac{\gamma_{12}}{\alpha_{12}}g_{m12} \tag{6.26}$$

$$\overline{i^2_{n,m13}} = 4KT\frac{\gamma_{13}}{\alpha_{13}}g_{m13} \tag{6.27}$$

$$\overline{i^2_{n,m14}} = 4KT\frac{\gamma_{14}}{\alpha_{14}}g_{m14} \tag{6.28}$$

$$\overline{i^2_{n,m15}} = 4KT\frac{\gamma_{15}}{\alpha_{15}}g_{m15} \tag{6.29}$$

$$\overline{i^2_{n,r_1}} = 4KT\frac{1}{R_1} \tag{6.30}$$

$$\overline{i^2_{\mathrm{n,r_2}}} = 4KT\frac{1}{R_2} \tag{6.31}$$

$$\overline{i^2_{\mathrm{n,r_3}}} = 4KT\frac{1}{R_3} \tag{6.32}$$

$$\overline{i^2_{\mathrm{n,r_4}}} = 4KT\frac{1}{R_4} \tag{6.33}$$

$$\overline{i^2_{\mathrm{n,r_5}}} = 4KT\frac{1}{R_5} \tag{6.34}$$

$$\overline{i^2_{\mathrm{n,r_6}}} = 4KT\frac{1}{R_6} \tag{6.35}$$

$$\overline{i^2_{\mathrm{n,r_F}}} = 4KT\frac{1}{R_\mathrm{F}} \tag{6.36}$$

Next, the input referred noise voltage power spectral density arrive at point (b) is the sum of noise voltage spectral densities referred to the gate of M2, from resistors $R_6$, $R_5$ and $R_\mathrm{F}$, which can be written as,

$$\overline{v^2_{\mathrm{n,in\text{-}b}}} = \frac{\overline{i^2_{\mathrm{n,m7}}}}{g^2_{\mathrm{m7}}} + \overline{i^2_{\mathrm{n,r_6}}} \times R^2{}_6 + \overline{i^2_{\mathrm{n,r_5}}} \times R^2{}_5 + \overline{i^2_{\mathrm{n,r_F}}} \times R^2{}_\mathrm{F} \tag{6.37}$$

And the input referred noise current power spectral density at point (b) is given by,

$$\overline{i^2_{\mathrm{n,in\text{-}b}}} = \overline{v^2_{\mathrm{n,in\text{-}b}}}\left[(2\pi f)^2\left(C_{\mathrm{gd7}} + C_{\mathrm{gs7}} + C_{\mathrm{gd5}} + C_{\mathrm{db5}}\right)^2 + \frac{1}{R^2_\mathrm{F}} + \frac{1}{R^2_5}\right] \tag{6.38}$$

The input referred voltage power spectral density referred to the gate of M5 is given by,

$$\overline{v^2_{\mathrm{n,in\text{-}c}}} = \frac{\overline{i^2_{\mathrm{n,m5}}}}{g^2_{\mathrm{m5}}} \tag{6.39}$$

Thus, the input referred current power spectral density at point (c) is given by,

$$\overline{i^2_{\mathrm{n,in\text{-}c}}} = \overline{v^2_{\mathrm{n,in\text{-}c}}}(2\pi f)^2\left(C_{\mathrm{gd14}} + C_{\mathrm{db14}} + C_{\mathrm{gd16}} + C_{\mathrm{db16}}\right)^2 \tag{6.40}$$

Next, the noise voltage power spectral density referred to M13 and M14 at point (d) is given by,

$$\overline{v^2_{\mathrm{n,in\text{-}d}}} = \frac{\overline{i^2_{\mathrm{n,m13}}}}{g^2_{\mathrm{m13}}} + \frac{\overline{i^2_{\mathrm{n,m14}}}}{g^2_{\mathrm{m14}}} \tag{6.41}$$

And the current power spectral density referred to the source of M13 can be found by,

$$\overline{i^2_{\text{n,in-d}}} = \overline{v^2_{\text{n,in-d}}}\left(2\pi f\right)^2\left(C_{\text{gd13}} + C_{\text{db13}} + C_{\text{gd15}} + C_{\text{db15}}\right)^2 \tag{6.42}$$

Hence, the total input referred noise current power spectral density at point (e) is the sum of the noise current power spectral density at point (c), (d) and M17,

$$\overline{i^2_{\text{n,in-e}}} = \overline{i^2_{\text{n,in-c}}} + \overline{i^2_{\text{n,in-d}}} + \overline{i^2_{\text{n,m17}}} \tag{6.43}$$

Thus, the total noise voltage and current power spectral density referred to the gate of M16 at point (f) are given by,

$$\overline{v^2_{\text{n,in-f}}} = \frac{\overline{i^2_{\text{n,in-e}}}}{g^2_{\text{m15}} + g^2_{\text{m16}}} + \frac{\overline{i^2_{\text{n,m16}}}}{g^2_{\text{m16}}} + \frac{\overline{i^2_{\text{n,in-b}}}}{g^2_{\text{m5}}} \tag{6.44}$$

$$\overline{i^2_{\text{n,in-f}}} = \overline{v^2_{\text{n,in-f}}}\left(2\pi f\right)^2\left(C_{\text{gs5}} + C_{\text{sb5}} + C_{\text{gd6}} + C_{\text{db6}} + C_{\text{gd16}} + C_{\text{gs16}}\right)^2 \tag{6.45}$$

Next, the noise voltage and current power spectral density referred to M6 at point (g) are given by,

$$\overline{v^2_{\text{n,in-g}}} = \frac{\overline{i^2_{\text{n,in-f}}}}{g^2_{\text{m6}}} + \frac{\overline{i^2_{\text{n,m6}}}}{g^2_{\text{m6}}} + \frac{\overline{i^2_{\text{n,m4}}}}{g^2_{\text{m4}}} + \overline{i^2_{\text{n,r}_4}} \times R^2_4 \tag{6.46}$$

$$\overline{i^2_{\text{n,in-g}}} = \overline{v^2_{\text{n,in-g}}}\left[\left(2\pi f\right)^2\left(C_{\text{gs4}} + C_{\text{sb4}} + C_{\text{gd6}} + C_{\text{gs6}}\right)^2 + \frac{1}{R^2_4}\right] \tag{6.47}$$

At point (h), the noise voltage and current power spectral density referred to M4 and from resistor $R_3$ are given by,

$$\overline{v^2_{\text{n,in-h}}} = \frac{\overline{i^2_{\text{n,in-g}}}}{g^2_{\text{m4}}} + \frac{\overline{i^2_{\text{n,m4}}}}{g^2_{\text{m4}}} + \overline{i^2_{\text{n,r}_3}} \times R^2_3 \tag{6.48}$$

$$\overline{i^2_{\text{n,in-h}}} = \overline{v^2_{\text{n,in-h}}}\left[\left(2\pi f\right)^2\left(C_{\text{gd2}} + C_{\text{db2}} + C_{\text{gd4}} + C_{\text{gs4}}\right)^2 + \frac{1}{R^2_3}\right] \tag{6.49}$$

And the input referred noise voltage and current power spectral density arriving at the source of M2 are given by,

$$\overline{v^2_{\text{n,in-i}}} = \frac{\overline{i^2_{\text{n,m2}}}}{g^2_{\text{m2}}} \tag{6.50}$$

$$\overline{i^2_{\text{n,in-i}}} = \overline{v^2_{\text{n,in-i}}}\left(2\pi f\right)^2\left(C_{\text{gd9}} + C_{\text{db9}} + C_{\text{gd11}} + C_{\text{db11}}\right)^2 \tag{6.51}$$

Similarly, the input referred noise voltage and current power spectral density referred to M8 and M9 at point (j) are given by,

$$\overline{v^2_{\text{n,in-j}}} = \frac{\overline{i^2_{\text{n,m8}}}}{g^2_{\text{m8}}} + \frac{\overline{i^2_{\text{n,m9}}}}{g^2_{\text{m9}}} \tag{6.52}$$

$$\overline{i^2_{\text{n,in-j}}} = \overline{v^2_{\text{n,in-j}}}\left(2\pi f\right)^2\left(C_{\text{gd8}} + C_{\text{db8}} + C_{\text{gd10}} + C_{\text{db10}}\right)^2 \tag{6.53}$$

Hence, the total input referred noise current power spectral density at point (k) is the sum of the noise current power at point (i), (j) and M12,

$$\overline{i^2_{\text{n,in-k}}} = \overline{i^2_{\text{n,in-i}}} + \overline{i^2_{\text{n,in-j}}} + \overline{i^2_{\text{n,m12}}} \tag{6.54}$$

Thus, the total input referred noise voltage and current power spectral density referred to the gate of M11 are given by,

$$\overline{v^2_{\text{n,in-l}}} = \frac{\overline{i^2_{\text{n,in-k}}}}{g^2_{\text{m10}} + g^2_{\text{m11}}} + \frac{\overline{i^2_{\text{n,m11}}}}{g^2_{\text{m11}}} + \frac{\overline{i^2_{\text{n,in-h}}}}{g^2_{\text{m2}}} \tag{6.55}$$

$$\overline{i^2_{\text{n,in-l}}} = \overline{v^2_{\text{n,in-l}}}\left(2\pi f\right)^2\left(C_{\text{gs2}} + C_{\text{sb2}} + C_{\text{gd3}} + C_{\text{db3}} + C_{\text{gd11}} + C_{\text{gs11}}\right)^2 \tag{6.56}$$

The input referred noise voltage and current power spectral density referred to M3 at point (m) are given by,

$$\overline{v^2_{\text{n,in-m}}} = \frac{\overline{i^2_{\text{n,m3}}}}{g^2_{\text{m3}}} + \frac{\overline{i^2_{\text{n,m3}}}}{g^2_{\text{m3}}} + \overline{i^2_{\text{n,r}_1}} \times \text{R}^2{}_1 + \overline{i^2_{\text{n,r}_\text{F}}} \times \text{R}^2{}_\text{F} \tag{6.57}$$

$$\overline{i^2_{\text{n,in-m}}} = \overline{v^2_{\text{n,in-m}}}\left[\left(2\pi f\right)^2\left(C_{\text{gd3}} + C_{\text{gs3}} + C_{\text{gd1}} + C_{\text{db1}}\right)^2 + \frac{1}{R^2_{\text{F}}} + \frac{1}{R^2_{1}}\right] \tag{6.58}$$

Finally, the input referred noise current power spectral density at point (n) can be written as,

$$\overline{i^2_{\text{n,in-n}}} = \overline{i^2_{\text{n,in-m}}} + \overline{i^2_{\text{n,r}_2}} \tag{6.59}$$

## 6.4 Simulation Results

Fig. 6.5 shows the transient sinusoidal response of proposed $g_m$-boosted multiple stage inductively peaked TIA for a nominal 10MHz input signal. As shown in this figure, the peak-to-peak output voltage swing is around 950nV for a test input current of 100nA.

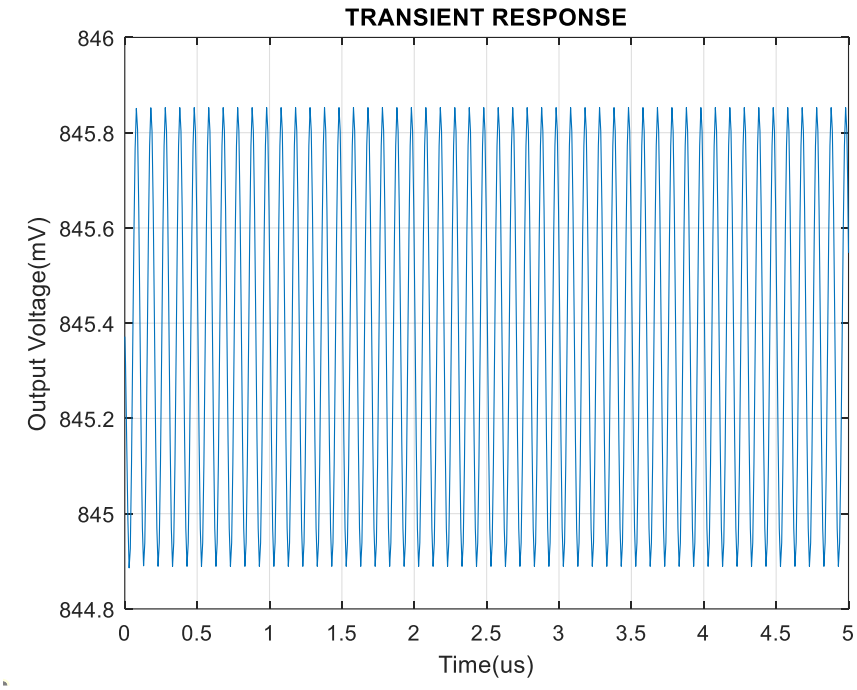



Fig. 6.5 Transient response of $g_m$-boosted multiple stage inductively peaked TIA.

Fig. 6.6 shows that transimpedance gain of $g_m$-boosted multiple stage TIA with an inductor is much higher than that for $g_m$-boosted multiple stage TIA without inductor for the same size of gain devices and load devices. As be seen from this figure, the magnitude of the transimpedance gain is around 73.71 dB. The -3 dB bandwidths of the proposed TIA with and without inductor are 38.69 MHz and 32.85 MHz respectively. Obviously, the -3 dB bandwidth has extended by 17% by adding the inductor.

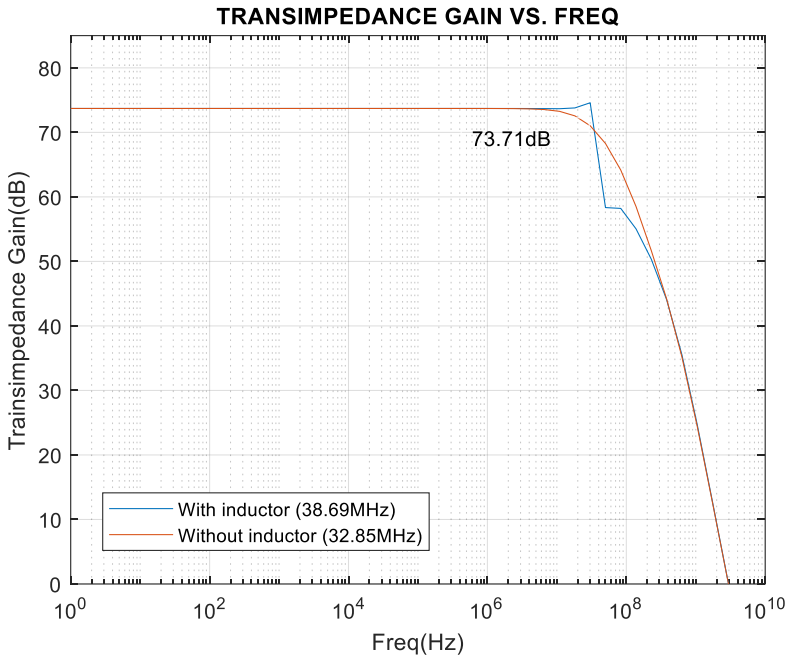



Fig. 6.6 Comparison of AC analysis simulation of transimpedance gain for $g_m$-boosted multiple stage TIA with/without inductor.

Fig. 6.7 indicates the input referred noise current power spectral density function of $g_m$-boosted multiple stage inductively peaked TIA and the average is around 47.71pA/sqrt (Hz) within the TIA bandwidth.

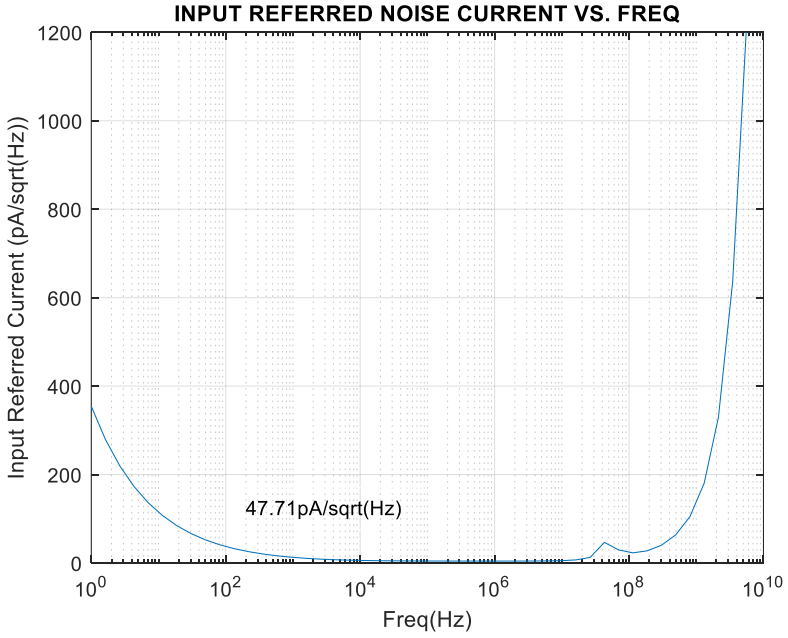



Fig. 6.7 Input referred noise current of $g_m$-boosted multiple stage inductively peaked TIA.

Fig. 6.8 shows the results of eye diagram simulations using -123 dBm input photodiode current signal and a $2^{31}$-1 pseudo random bit sequence (PRBS) data pattern. It displays an eye opening of 95% at 15 Mbit/s.

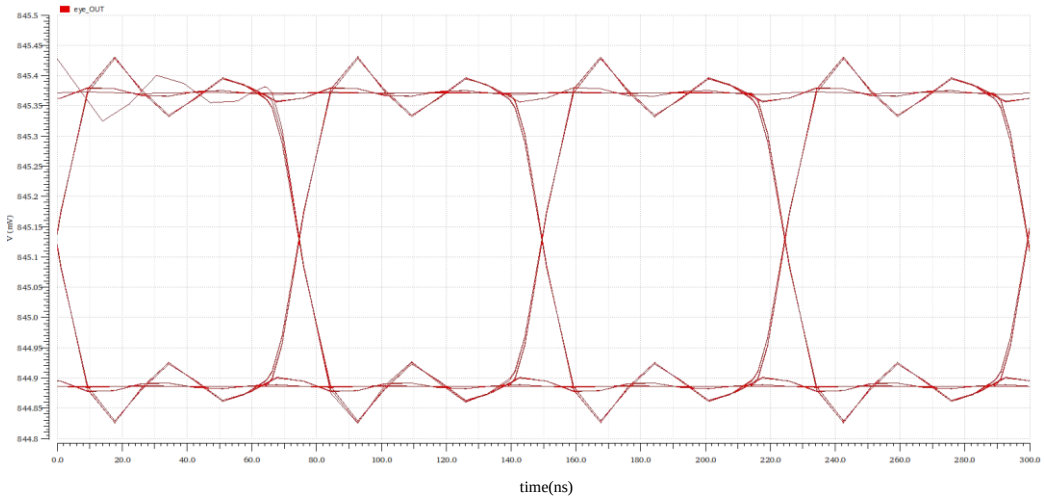



Fig. 6.8 Eye diagram of $g_m$-boosted multiple stage inductively peaked TIA.

## 6.5 Layout

Fig. 6.9 shows the masked layout for $g_m$-boosted multiple stage inductively peaked TIA which occupies 575 × 670 μm$^2$ of silicon area.

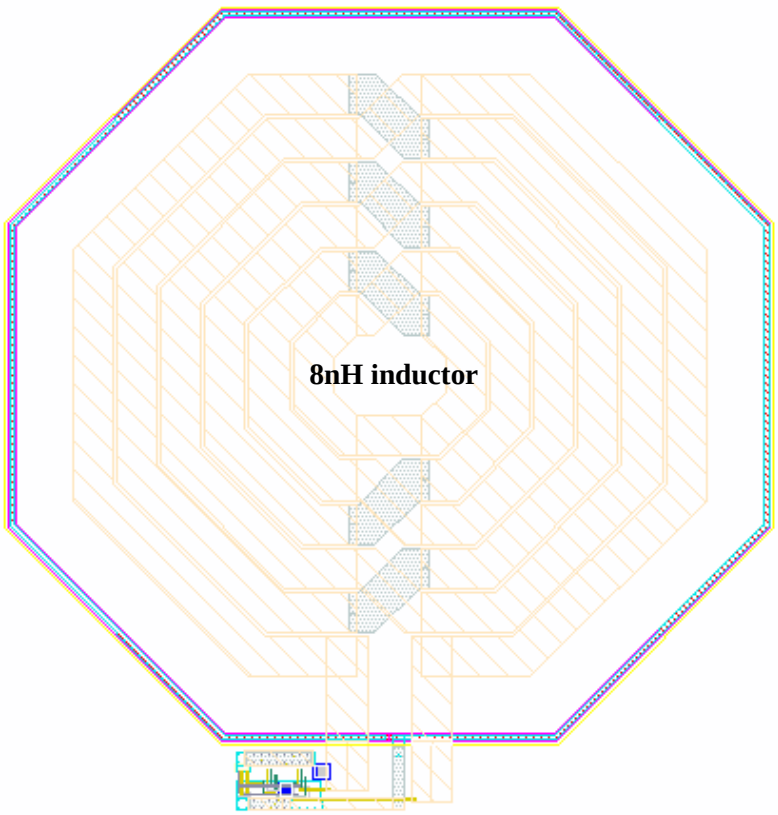



Fig. 6.9 Layout of $g_m$-boosted multiple stage inductively peaked TIA.

# Chapter 7 Comparison

The Figure of Meri is widely used in a comparison of the performance of CMOS TIA topologies [3][67][68] which is described as,

$$FoM = \frac{Gain(dB\Omega) \times BW(kHz) \times C(pF)}{Power(mW) \times InputNoise(pA/\sqrt{Hz})} \tag{7.01}$$

Where *Gain* is the transimpedance gain in dBΩ, *BW* is the bandwidth in kHZ, *C* is the photodiode capacitance in pF, *Power* is the power dissipation in mW and the *InputNoise* is the input current noise density in pA/sqrt(Hz).

Table 7.1 shows the comparison with the state of proposed $g_m$-boosted TIAs. Surprisingly, the $g_m$-boosted multiple stage inductively peaked TIA achieves the highest FoM and largest bandwidth at the expense of lower transimpedance gain and higher power consumption. The design of $g_m$-boosted Inv-Cas and RIC TIAs has similar performances as they provide higher gain, lower power consumption and lower noise. Compared between these two topologies, $g_m$-boosted Inv-Cas has slightly better input referred noise spectral density and smaller occupied space. Although $g_m$-boosted doubly folded push-pull offers the highest gain and bandwidth, the bad input noise current spectral density performance and high-power dissipation make it the lowest FoM.

As a result, $g_m$-boosted Inv-Cas TIA, $g_m$-boosted RIC TIA and $g_m$-boosted multiple stage inductively peaked TIA are selected to be fabricated.

Table 7.1 Comparison with the state of proposed $g_m$-boosted TIAs.

| $g_m$-boosted TIA | Inv-Cas | RIC | Doubly folded push-pull | Multiple stage inductively peaked |
|---|---|---|---|---|
| Gain (dBΩ) | 145.8 | 145.5 | 217.8 | 73.71 |
| BW (kHz) | 5.31 | 5.4 | 211 | 38690 |
| C (pF) | 5 | 5 | 5 | 5 |
| Power (mV) | 11.1 | 13.9 | 56.7 | 127.1 |
| Input Noise (pA/sqrt Hz) | 4.23 | 7.81 | 159.8 | 47.71 |
| FoM | 82.4 | 36.2 | 25.4 | 470.3 |
| Area Occupied ($\mu m^2$) | 721 | 1845 | 3135 | 385250 |

# Chapter 8 Experimental Results

## 8.1 Overall Layout

The $g_m$-boosted RIC TIA, $g_m$-boosted Inv-Cas TIA and $g$m-boosted multiple stage inductively peaked TIA are selected to be fabricated. Fig. 8.1 shows the overall layout for the selected TIA with a bound pad which indicates $g_m$-boosted RIC, $g_m$-boosted Inv-Cas TIA and $g_m$-boosted multiple stage inductively peaked TIA from left to right respectively. The size of the chip is $1.5mm \times 3.3mm$ which contains 28 pins.

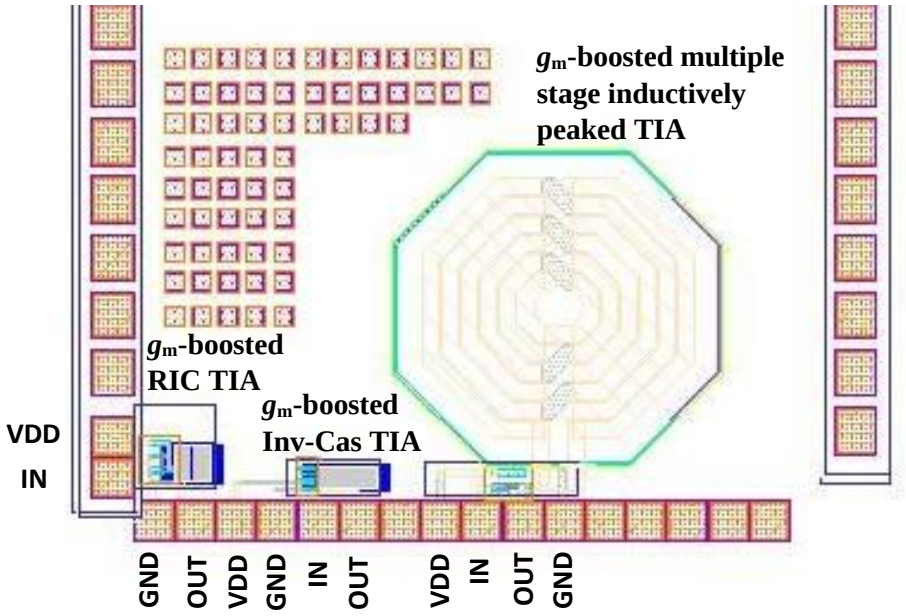



Fig. 8.1 Overall layout for the selected $g_m$-boosted TIA sitting in the chip.

Fig. 8.2 shows the bonding diagram for DIP 28 package for the packaging of the chip. The pins from 16 to 27 are occupied by the selected TIAs which is the same as the 12 pins shown in Fig. 8.1.

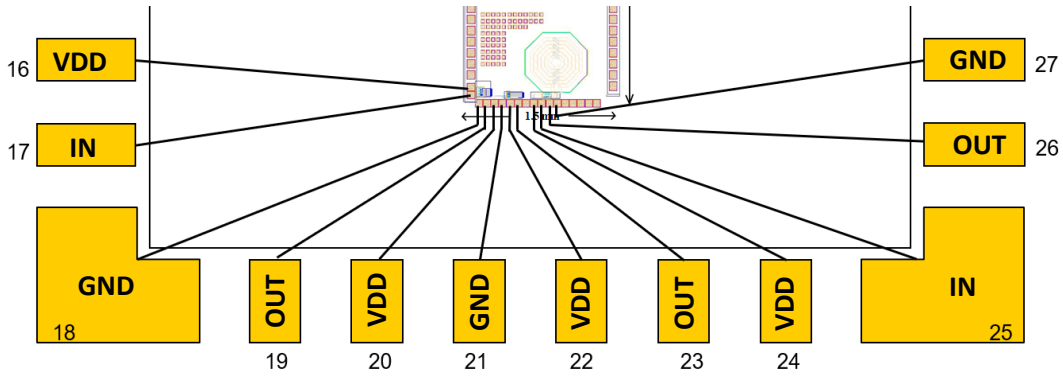



Fig. 8.2 Bonding diagram for the packaging of the chip.

## 8.2 DRC, LVS, and PEX Analysis

Before the layout is sent to be fabricated, there are three steps to check the performance of the designed layout. The major step is Design Rule Check (DRC) simulation to ensure that the chip layout design satisfies the physical design process, such as the space between each metal. Any violation of the design rule may result in a faulty chip. Furthermore, if DRC simulation is not passed, the chip cannot be accepted by the manufacturer. Next, Layout versus Schematic (LVS) verification is to compare the layout and schematics. It guarantees that the layout represents the circuit you desire to fabricate. The last step is Parasitic Extraction (PEX) analysis that calculates the parasitic effects from designed components and wires. It extracts the parasitic resistances, capacitances and inductances from the layout, and generates netlists to create an accurate model of the circuit to simulate the actual response. For analog circuits, the principal purpose is to make sure the designed circuit still function if the extra extracted parasites are applied.

## 8.3 Microphotographs of Fabricated Microchip

The whole design was sent to a foundry for fabrication and came back in February. A microphotograph 10X of the fabricated microchip is shown in Fig. 8.3. The marked layout areas from left to right are $g_m$-boosted RIC TIA, $g_m$-boosted Inv-Cas TIA, and $g_m$-boosted multiple stage inductively peaked TIA respectively. Fig. 8.4 is a microphotographs 20X showing the details of three selected $g_m$-boosted TIAs.

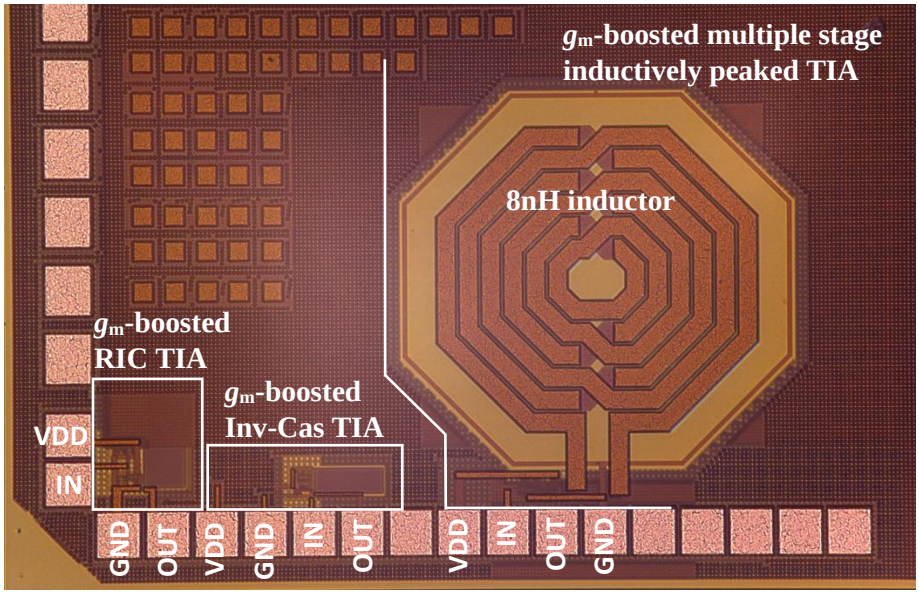
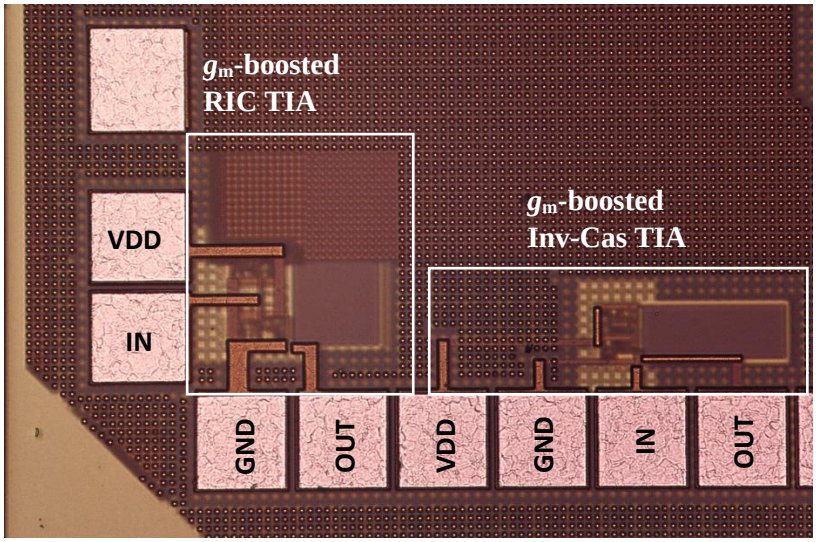
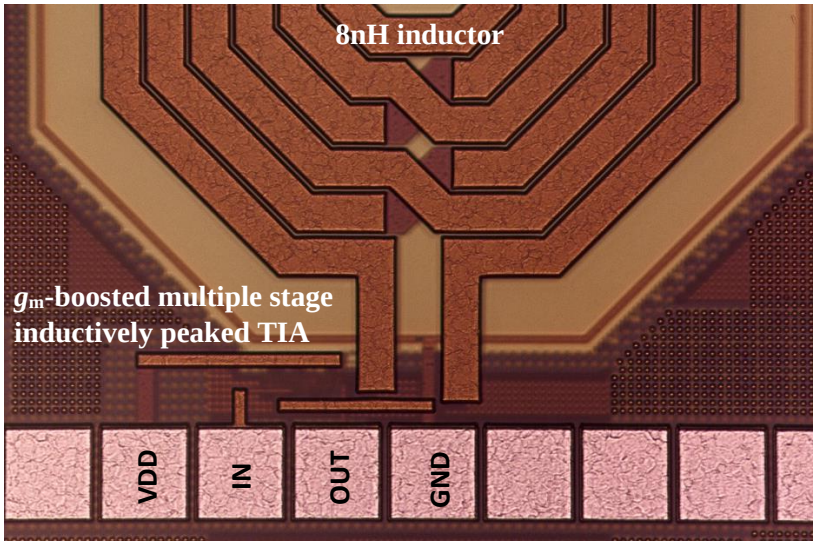



Fig. 8.3 Microphotograph 10X of selected $g_m$-boosted TIAs fabricated in 180nm CMOS technology.




(a)




(b)

Fig. 8.4 Microphotograph 20X showing the details of selected $g_m$-boosted TIAs fabricated in 180nm CMOS technology, (a) $g_m$-boosted RIC TIA (left) and $g_m$-boosted Inv-Cas TIA (right), and, (b) $g_m$-boosted multiple stage inductively peaked TIA.

## 8.4 Test Setup

A test setup of the fabricated microchip in the lab is shown in Fig. 8.5. The chip is mounted on a fabricated test PCB which is detailed in Fig. 8.6. The PCB's input is a voltage signal generated by Tektronix AFG3021C signal channel arbitrary/function generator. It passes to a current source IC LT3092EST#PBF. According to its datasheet, two resistors are connected to the pins IN and SET which program the value of output and the output current is given on the datasheet as below,

$$I_{\text{out}} = 10\mu A \frac{R_{\text{set}}}{R_{\text{out}}} \tag{8.01}$$

Thus, the desired output current is chosen as 10µA and the resistors $R_{\text{out}}$ and $R_{\text{set}}$ are selected to be 22kΩ because the datasheet states the reasonable starting level of $R_{\text{set}}$ is 22 kΩ. Thus, the input current is given by,

$$\begin{aligned} I_{\text{out}} &= 10\mu A \frac{22k\Omega}{22k\Omega} \\ &= 10\mu A \end{aligned} \tag{8.02}$$

The test PCB is powered with 1.8V voltage by Sinometer DC regulated power supply HY3003D-3. Then the amplified output voltage signal from the microchip is passed to a non-inverter buffer gate SN74LVC1G17DBVR. And the final output voltage signal is measured by a Tektronix TBS 1102b-EDU digital oscilloscope to display and analyse its waveform.

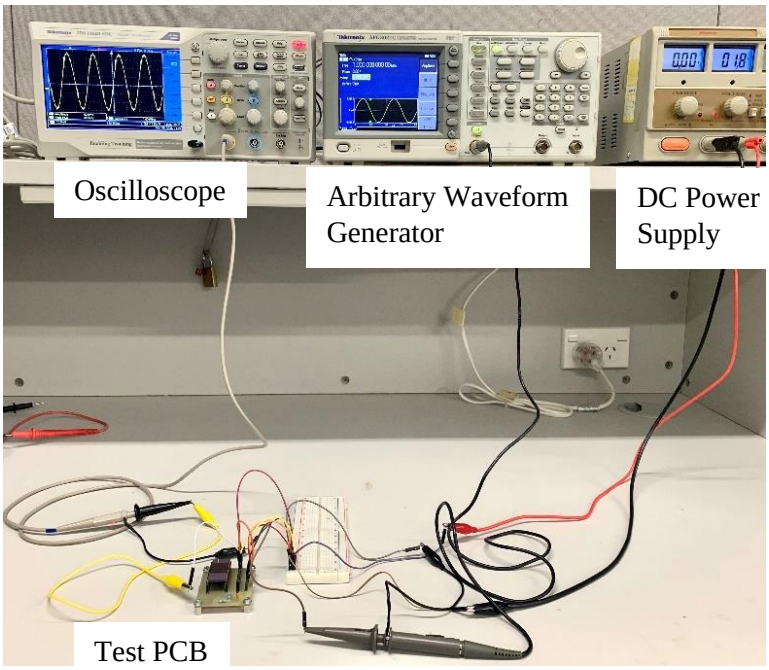
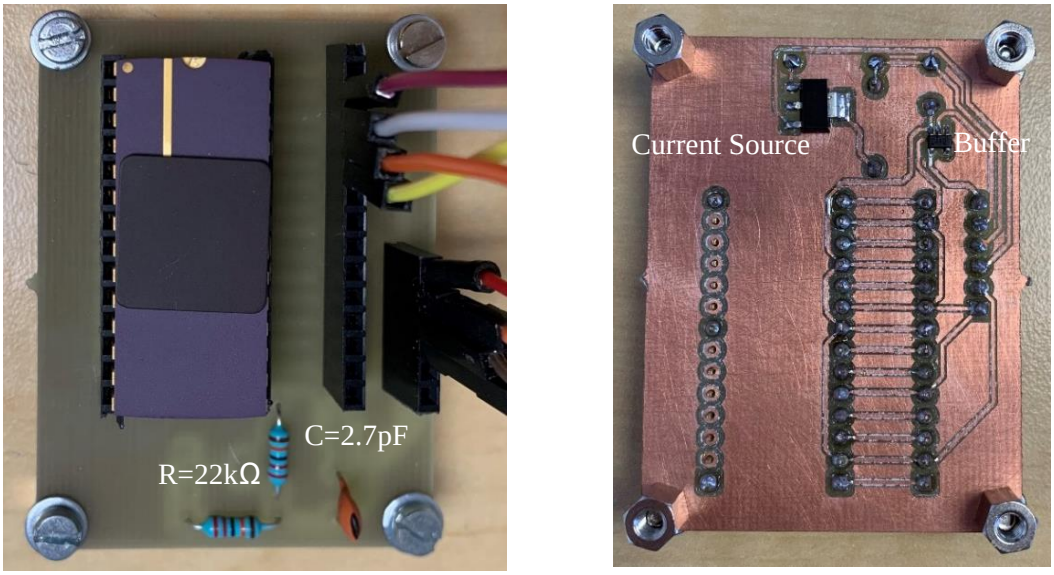



Fig. 8.5 The test setup of the microchip in the lab.




(a) (b)

Fig. 8.6 The details of test PCB, (a) Top side, and, (b) bottom side.

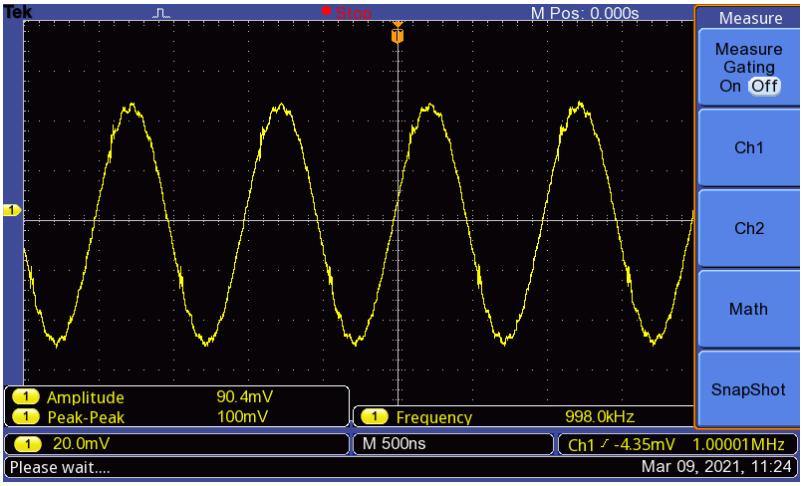
## 8.5 Test Results

The three selected TIAs are tested by two waveforms: sine wave and square wave, and the input current from the calculation in the previous section is 10 µA at 1 MHz.

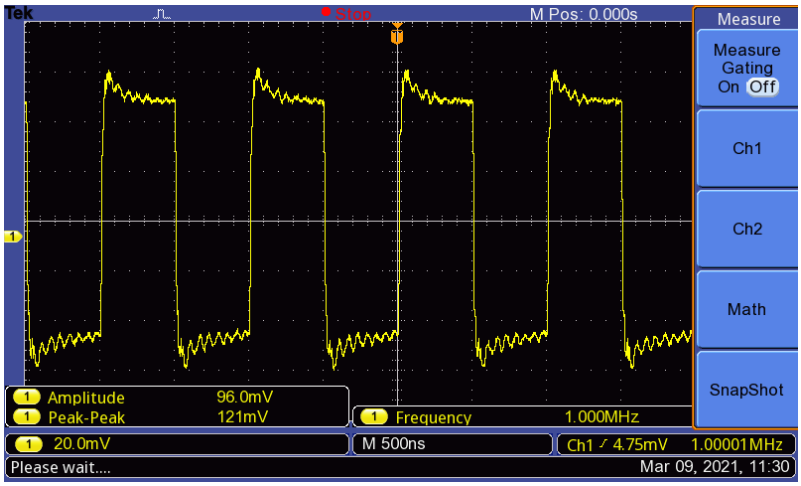
### 8.5.1 $g_m$-boosted Inv-Cas TIA

The test results of $g_m$-boosted Inv-Cas TIA are shown in Fig. 8.7. The peak-to peak-voltage from sine-wave and square-wave inputs are amplified to100 mV and 121 mV respectively. Thus, the transimpedance gain can be calculated by,

$$\begin{aligned} TransimpedanceGain &= 20\log\left(\frac{v_{out-peak-to-peak}}{i_{in-peak-to-peak}}\right) \\ &= 20\log\left(\frac{100mV}{10\mu A}\right) \\ &= 80dB \end{aligned} \tag{8.03}$$




(a)



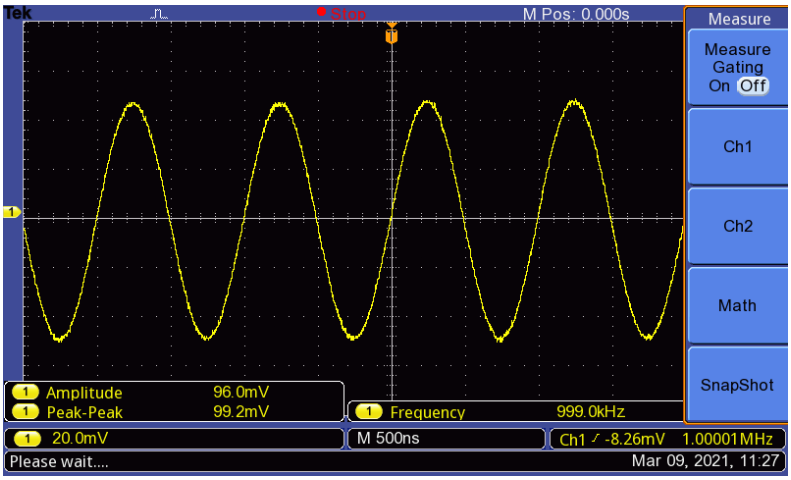

(b)

Fig. 8.7 $g_m$-boosted Inv-Cas TIA test results from oscilloscope, (a) Input signal as a sine wave, and (b) Input signal as a square wave.

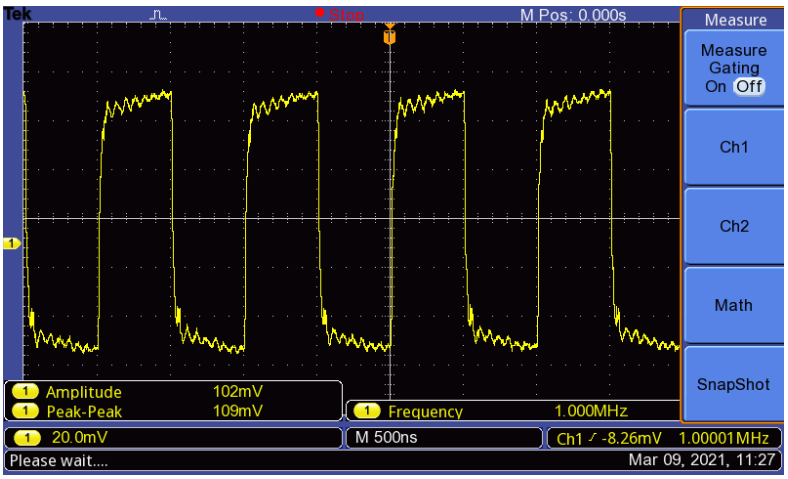
### 8.5.2 $g_m$-boosted RIC TIA

The test results of $g_m$-boosted RIC TIA are shown in Fig. 8.8. The peak-to peak-voltage from sine-wave and square-wave inputs are amplified to 99.2 mV and 109 mV respectively. Thus, the transimpedance gain can be calculated by,

$$\begin{aligned} TransimpedanceGain &= 20\log\left(\frac{v_{out-peak-to-peak}}{i_{in-peak-to-peak}}\right) \\ &= 20\log\left(\frac{99.2mV}{10\mu A}\right) \\ &= 79.9dB \end{aligned} \tag{8.04}$$




(a)



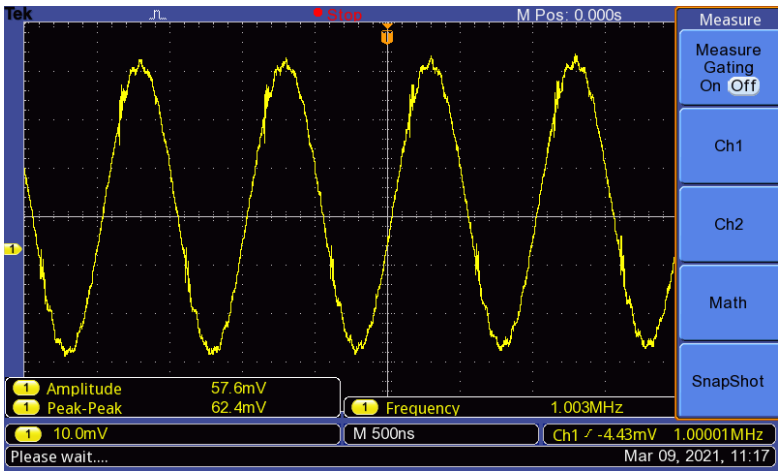

(b)

Fig. 8.8 $g_m$-boosted RIC TIA test results from oscilloscope, (a) Input signal as a sine wave, and (b) Input signal as a square wave.

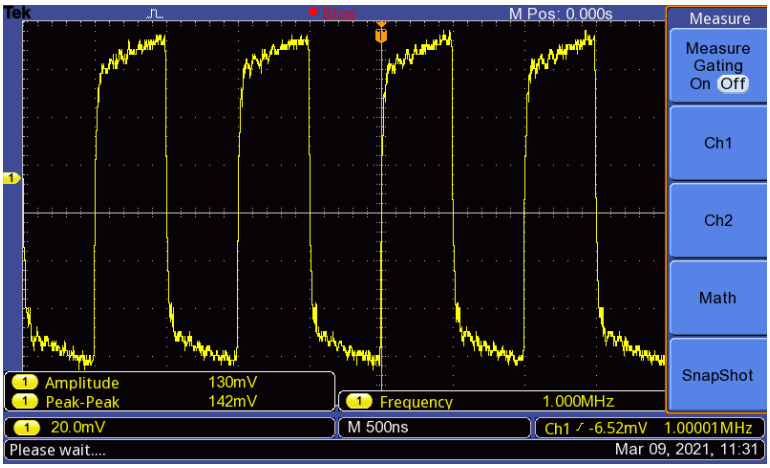
### 8.5.3 $g_m$-boosted Multiple Stage Inductively Peaked TIA

The test results of $g_m$-boosted multiple stage inductively peaked are shown in Fig. 8.9. The peak-to peak-voltage from sine-wave and square-wave inputs are amplified to 62 mV and 142mV respectively. Thus, the transimpedance gain can be calculated by,

$$\begin{aligned} TransimpedanceGain &= 20\log\left(\frac{v_{out-peak-to-peak}}{i_{in-peak-to-peak}}\right) \\ &= 20\log\left(\frac{62.4mV}{10\mu A}\right) \\ &= 75dB \end{aligned} \tag{8.05}$$




(a)




(b)

Fig. 8.9 $g_m$-boosted multiple stage inductively peaked TIA test results from oscilloscope, (a) Input signal as a sine wave, and (b) Input signal as a square wave.

# Chapter 9 Conclusion

In conclusion, five new topology designs of $g_m$-boosted TIA along with simulation and experimental results are presented using a 180nm CMOS technology for biomedical and sensor applications. A theoretical analysis of transimpedance gain and input referred noise current spectral density for all proposed topologies is provided and discussed in detail. After comparison, three of them are fabricated and tested in the lab successfully.

Details of a $g_m$-boosted common-source with source-degeneration stage and its new TIA configuration for transimpedance gain has been presented. Simulations indicate that as expected much higher gain is achievable using these structures employing the $g_m$-boosting gain "A". A biasing scheme is also provided to configure the $g_m$-boosted common-source with source-degeneration stage as a TIA without which the amplifying device would be driven into the triode region.

Besides, the $g_m$-boosted Inv-Cas TIA and $g_m$-boosted RIC TIA show excellent performance which achieves higher transimpedance gain, lower input referred noise current spectral density and low power consumption with reasonable bandwidth. These two are good fit for applications that require high sensitivity, low input referred noise and low power dissipation. Next, the $g_m$-boosted multiple-stage inductively peaked TIA shows the best performance FoM within the higher bandwidth. Furthermore, by using the inductive bandwidth extension technique, the bandwidth of the TIA has increased by 17%. And the $g_m$-boosted doubly folded push-pull TIA is an option for high gain and high bandwidth applications with limited input noise current and power consumption requirement. The experimental results are found to be reasonably close to the simulations.

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# Published Journal Article

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LETTER TO THE EDITOR | Full Access

# On the $g_m$-boosted common source with source degeneration and its configuration as a transimpedance amplifier

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## 1 INTRODUCTION

The common source with source degeneration is well known in analog CMOS integrated circuits and is discussed in detail in text-books[1-5] and other avenues. It is implemented in numerous building blocks for signal conditioning and for boosting the output impedance of analog circuits. Improvement of its intrinsic gain and output impedance can further enhance the performance of such analog building blocks. In this context, the implementation and comprehensive small-signal mid-band characteristics of a $g_m$-boosted common-source amplifier with source degeneration is investigated in this work. The full circuit analysis of a $g_m$-boosted common-source amplifier with source degeneration or its transimpedance amplifier (TIA) derivative has not been reported before. A basic $g_m$-boosted common source with source degeneration was introduced in literature[2] but without comprehensive small-signal analysis. The $g_m$-boosting technique has been employed in many analog building blocks such as transconductance amplifiers[6], TIAs[7], RF frontend LNA[8], RF mixers[9], sensor instrumentation amplifier,[10] and so forth. In several recent articles, *using a simplified inspection technique*,[11] the second author reported many CMOS $g_m$-boosted topologies, which were analyzed by providing their complete mid-band gain derivation, which was not available before. This paper explores the behavior of the $g_m$-boosted common-source stage with source degeneration using this *simplified inspection technique*. Elementary Norton's and Thevenin's source transformations[12] along with suitable conversion of dependent current sources into simple conductors/resistors[11, 13] is employed for a "pictorial" and simplified determination of mid-band gain expressions. Progressively simplified small-signal circuits are employed, which eliminates the use of complicated nodal or mesh analysis in extracting elegant expressions. The paper also discusses the structural transformation of the $g_m$-boosted common source with source degeneration into a TIA for sensing and detection applications. In order to provide a verification of the design enhancements achieved by the $g_m$-boosted common source with source degeneration, comparison with the ordinary common source with source degeneration is also provided through circuit simulations. Overall, this paper fully explores the $g_m$-boosted common source with source degeneration and provides new "pictorial" transformation-based mid-band derivations with an underlying tutorial flavor. Standard symbols[1, 2, 4, 5] are employed for all the MOSFET parameters in the

small-signal analysis following the general convention for electronic circuit analysis. As a note on the use of well-defined composite current/voltage notations[14], it is to be mentioned that all the voltages and currents in lowercase alphabets along with uppercase subscripts are quantities containing both a large-signal DC bias and a small-signal (AC) fluctuation superimposed on it. Also, all the uppercase voltage/current notations along with uppercase subscripts are DC quantities. Further, all the lowercase voltage/current notations along with lowercase subscripts are AC quantities.

## 2 TRANSCONDUCTANCE BOOSTED COMMON SOURCE WITH SOURCE DEGENERATION AND ITS INSPECTION-BASED MID-BAND ANALYSIS

Figure 1 shows the topology and the simplified progressive "pictorial" inspection-based analysis of the $g_m$-boosted common source with source-degeneration stage. A differential amplifier with gain $A$ is used in a negative feedback loop around the gate and the source of the NMOS amplifier device M1. The equivalent topologies of the $g_m$-boosted common source with source degeneration using current sources or resistors are shown in Figure 1A. The $g_m$-boosting differential amplifier with gain $A$ is considered to have high input impedance (similar to that of an ideal operational amplifier[12]) so that there is no current flowing into its terminals at mid-band frequencies. The input to the common-source stage is applied through the positive (non-inverting) terminal of the $g_m$-boosting amplifier that also contains the DC-bias (common-mode) input. This common-mode voltage is equal to the DC-bias voltage at the negative (inverting) terminal of the $g_m$-boosting amplifier, which is the same as the DC voltage at the source of M1. The gate of the common-source device M1 is biased by the DC level at the output of the $g_m$-boosting differential amplifier. The AC equivalent circuit is shown in Figure 1B. The negative feedback termination can be verified as follows: If there is a slight increase in the voltage at the source of M1 that will result in a slight decrease in the voltage at the gate of M1 (small-signal voltage at the output of the differential amplifier), as a consequence, the drain current of M1 will reduce. Because of the reduced drain current, the voltage at the source of M1 will reduce slightly, thus opposing the previous increase and imparting stable operation. Figure 1C depicts the small-signal mid-band equivalent circuit for the $g_m$-boosted common source with source degeneration with the gate *g1* at a small-signal voltage of $A$ ($v_{in} - v_y$). Usually at this stage, circuit analysis equations (simultaneous nodal or mesh equations) are employed to determine the mid-band gain using Figure 1C. Instead, a progressive "pictorial"-based method[11, 13] is used here in determining the mid-band gain. Following on, in Figure 1D, the output of the $g_m$-boosted common source with source degeneration is AC-shorted to ground in order to find the $G_m$ of the Norton amplifier model.[13] In the next diagram, in Figure 1E, the small-signal equivalent model for Figure 1D is shown, which can be used for finding the $G_m$ of the $g_m$-boosted common source with source degeneration. Following on, in Figure 1F, the transconductance current source is partitioned into two current sources for the purpose of simplification. It is easily observed now that $-g_{m1}(A + 1)v_y$ and $g_{mb1}v_{b1s1}$ are current sources due to the same voltage $(0 - v_y)$ across them

(with voltages at *b1* and *s1* being 0 and $v_y$, respectively). Voltage-dependent current sources that are due to the voltage across themselves can be converted into a simple resistor/conductor,[11, 13] which is shown "pictorially" in the two-step circuit equivalence and transformation diagrams in Figure 1G,H. The final simplified form of this transformation from Figure 1H is next incorporated into Figure 1I, where $-g_{m1}(A + 1)v_y$ and $g_{mb1}v_{b1s1}$ are reduced to just two conductors of values $g_{m1}(A + 1)$ and $g_{mb1}$, respectively. Also, in Figure 1I, it is evident that the current source $g_{m1}Av_{in}$ is divided into four parts flowing into the conductors: $(1/R_S)$, $g_{m1}(A + 1)$, $g_{mb1}$, and $(1/r_{o1})$. Further, it is easily observed that the short-circuit output current $i_{out\_sc}$ is equal and opposite to the part of $g_{m1}Av_{in}$ flowing through $R_S$.

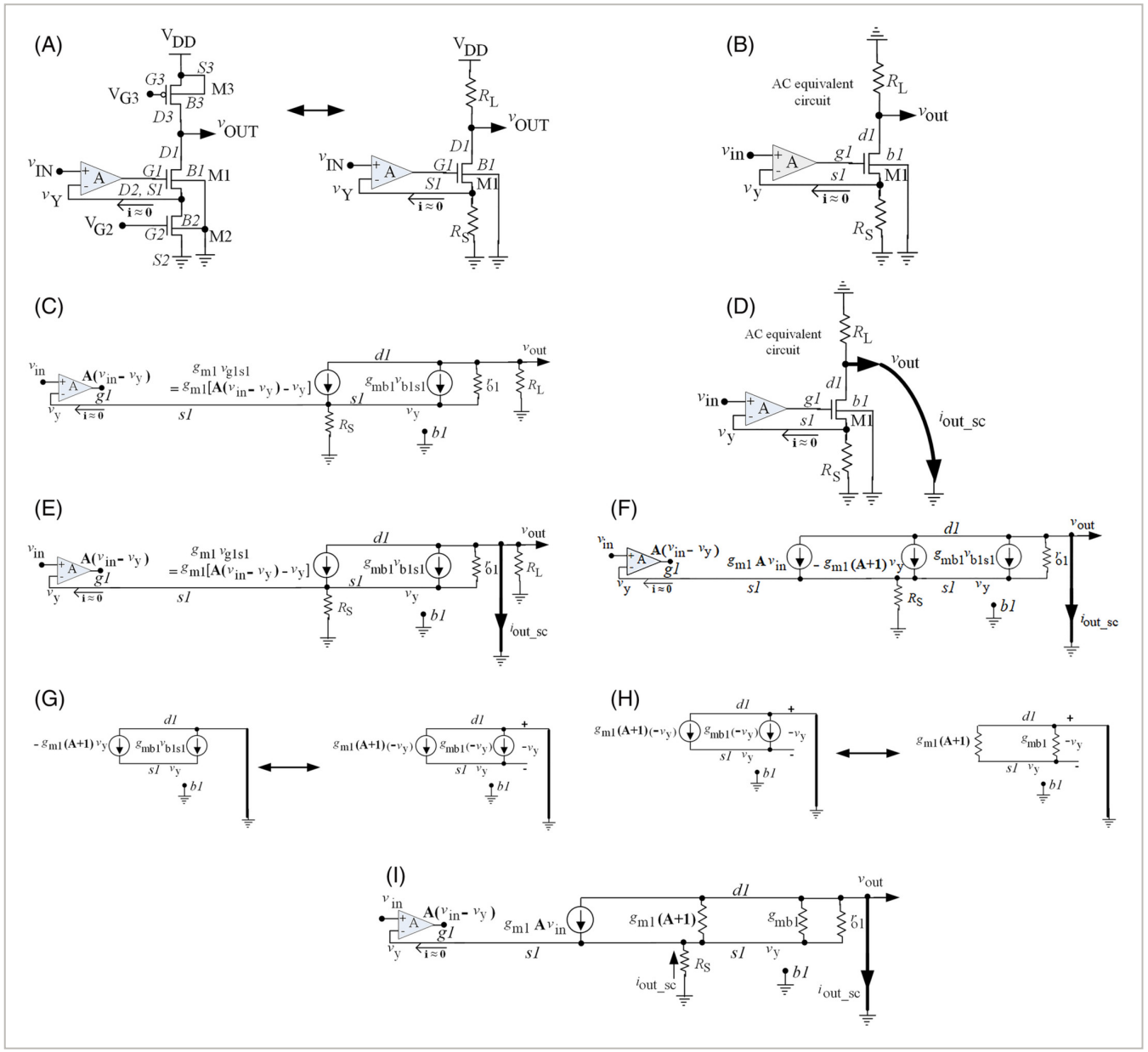


**FIGURE 1**

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Circuit topology and successive inspection-based "pictorial" analysis of the $g_m$-boosted common source with source degeneration to find $G_m$: (A) equivalent forms with current source or resistive degeneration and load; (B) AC equivalent circuit; (C) small-signal equivalent circuit; (D) AC equivalent circuit with output AC-shorted to ground; (E) small-signal

equivalent circuit with output shorted to ground; (F) the output-shorted small-signal equivalent circuit with the transconductance current source partitioned into two; (G) the first step in the transformation of the current sources $-g_{m1}(A+1)v_y$ and $g_{mb1}v_{b1s1}$; (H) the second step in the transformation of $-g_{m1}(A+1)v_y$ and $g_{mb1}v_{b1s1}$ into conductors $g_{m1}(A+1)$ and $g_{mb1}$ respectively; and (I) the final equivalent circuit simplified by incorporating $g_{m1}(A+1)$ and $g_{mb1}$ as replacements for $-g_{m1}(A+1)v_y$ and $g_{mb1}v_{b1s1}$, respectively

Hence, by employing the simple current-division formula in Figure 1I,

$$i_{out\_sc} = -g_{m1}Av_{in}\frac{\frac{1}{g_{mb1}+(A+1)g_{m1}+\frac{1}{r_{o1}}}}{R_S+\frac{1}{g_{mb1}+(A+1)g_{m1}+\frac{1}{r_{o1}}}} \tag{1}$$

or,

$$\frac{i_{out\_sc}}{v_{in}} = -g_{m1}A\frac{\frac{1}{g_{mb1}+(A+1)g_{m1}+\frac{1}{r_{o1}}}}{R_S+\frac{1}{g_{mb1}+(A+1)g_{m1}+\frac{1}{r_{o1}}}} \tag{2}$$

By rationalizing the above right-hand-side expression,

$$G_m = -g_{m1}A\frac{r_{o1}}{R_S r_{o1} g_{mb1} + R_S(A+1)g_{m1}r_{o1} + R_S + r_{o1}} \tag{3}$$

Next, Figure 2 shows the "pictorial" transformations for finding the $R_{out}$ of the $g_m$-boosted common source with source-degeneration stage's Norton amplifier model. In Figure 2A, the input is AC short-circuited to find the $R_{out}$. Figure 2B,C shows the successively simplified AC small-signal model of the input short-circuited $g_m$-boosted common source with source-degeneration stage. Next, in Figure 2D, the two dependent current sources being due to the same voltage $v_y$ are accumulated into one current source along with an inversion of the direction of the arrow to account for the negative values of the two current courses. Finally, in Figure 2E, the Norton current source with parallel resistance $r_{o1}$ is converted into a Thevenin's voltage source with a series resistance $r_{o1}$. $R_{out}$ can now be easily determined

from Figure 2E by dividing the total small-signal (AC) voltage from the output terminal to ground by the small-signal (AC) loop current ($i_{loop} = v_y/R_S$) flowing along the loop shown by the curved line with the arrow.

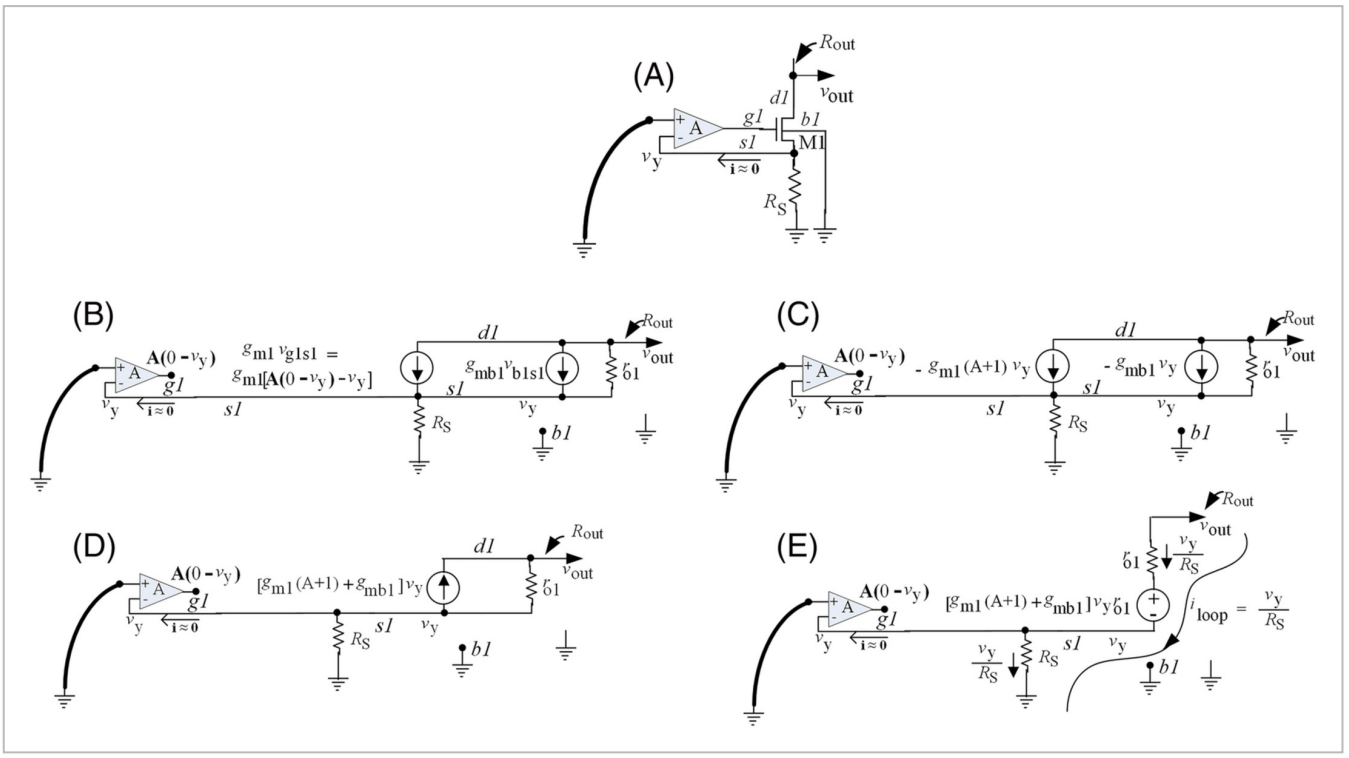


**FIGURE 2**

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Finding the $R_{out}$ of the Norton amplifier model for the $g_m$-boosted common source with source degeneration: (A) AC equivalent circuit with input shorted to AC ground, (B) small-signal equivalent circuit of the input-shorted amplifier, (C) further simplification of the circuit in (B), (D) merging the $g_m$-boosted transconductance and the body transconductance current sources and inversion of the current direction, and (E) conversion of the merged Norton circuit into Thevenin's form

Hence, the $R_{out}$ can be found in just two steps as

$$v_{out} = \frac{v_y}{R_S} r_{o1} + [(A+1)g_{m1} + g_{mb1}]v_y r_{o1} + v_y \tag{4}$$

and

$$R_{\text{out}} = \frac{v_{\text{out}}}{i_{\text{loop}}} = \frac{\frac{v_y}{R_S} r_{o1} + [(A+1)g_{m1} + g_{mb1}]v_y r_{o1} + v_y}{\frac{v_y}{R_S}}$$

(5)

or,

$$R_{\text{out}} = R_S r_{o1} g_{mb1} + R_S(A+1)g_{m1} r_{o1} + R_S + r_{o1}$$

(6)

Finally, using Equations 3 and 6, the no-load (intrinsic) gain of the $g_m$-boosted common source with source-degeneration stage (determined by employing an ideal current-source load) is given by

$$A_V^{\text{no-load}} = G_m R_{\text{out}}$$

(7)

$$= -g_{m1} A \frac{r_{o1}}{R_S r_{o1} g_{mb1} + R_S(A+1)g_{m1} r_{o1} + R_S + r_{o1}} \times R_S r_{o1} g_{mb1} + R_S(A+1)g_{m1} r_{o1} + R_S + r_{o1}$$

(8)

$$= -g_{m1} A r_{o1}$$

(9)

So, the intrinsic gain is increased by a factor of $A$ compared to the ordinary common source with source degeneration. For a finite load $R_L$ instead of an ideal current-source load, the gain is given by

$$A_V^{\text{finite-load}} = G_m(R_{\text{out}} // R_L)$$

(10)

or,

$$A_V^{\text{finite}-\text{load}} = -\frac{g_{m1}Ar_{o1}R_L}{R_L + R_S r_{o1} g_{mb1} + R_S(A+1)g_{m1}r_{o1} + R_S + r_{o1}}$$

(11)

# 3 TRANSCONDUCTANCE BOOSTED COMMON SOURCE WITH SOURCE DEGENERATION AS A TIA

TIAs are one of the most important analog signal conditioning circuits particularly for meeting challenging current-sensing specifications in today's exploding sensor and biomedical applications. This is in addition to the traditional broadband optoelectronic storage and communication applications employing inductive bandwidth enhancements. Any amplifier topology can be configured to operate as a TIA. Here, we investigate the TIA configuration of the $g_m$-boosted common source with source degeneration, which has not been reported before. Figure 3 shows the standard common source with source degeneration converted into a TIA employing a current-feedback resistor $R_F$ and an input current signal $i_{in}$ to produce a sensed output voltage. Here, $R_F$ also provides the drain-feedback DC bias at the gate of M1. This drain-feedback biasing allows the device M1 to be in strong inversion saturation by maintaining a suitable $V_{DS}$ (= $V_{GS}$) so that $V_{DS} > (V_{GS} - V_{TH})$. However, in the case of the $g_m$-boosted common source with source degeneration, such drain-feedback biasing will not work. This is because the DC-bias voltages at the input terminals of the $g_m$-boosting differential amplifier are equal (common-mode voltage) and drain-feedback biasing will result in the $V_{DS}$ of M1 to be 0 and consequently M1 will be driven into the triode region. Hence, a novel biasing scheme is provided for the proper operation of the $g_m$-boosted common source with source degeneration in a TIA configuration as shown in Figure 4A. An appropriate current $I_{BIAS}$ is forced through the diode-connected device M2, which independently sets the DC voltage at the positive terminal of the $g_m$-boosting amplifier to the DC voltage $V_Y$ at the negative terminal (the common-mode voltage). Thus, the DC voltage at the drain of M1 can be relaxed to be set at an appropriate higher value in order to keep M1 in saturation. In addition, the small-signal feedback current through $R_F$ can conveniently add algebraically to the small-signal input current $i_{in}$ at the positive terminal of the $g_m$-boosting amplifier, thus providing closed-loop current-feedback operation. Next, Figure 4B shows the AC equivalent circuit of the TIA where the bias circuit presents the small-signal impedance ($R_{eq\_bias}$) given by

$$R_{\text{eq\_bias}} = \frac{1}{g_{m2} + \frac{1}{r_{o2}}}$$

(12)

The open-loop AC equivalent circuit for determining the loop gain and the closed-loop transimpedance gain is shown in Figure 4C, which is the $g_m$-boosted common source with source-degeneration topology. This circuit is obtained employing a two-port Y model for the feedback path[2] so that the admittance parameters are $Y_{11} = 1/R_F$ and $Y_{22} = 1/R_F$ for the open-loop feedforward TIA (with the effect of feedback loading). Also, the feedback factor $\beta$ is given by the admittance parameter $Y_{21} = 1/R_F$. It has input voltage $v_{in}$ corresponding to the input current $i_{in}$ and the output voltage $v_{out}$ as shown in the figure along with a load resistance $R'_L$ (= $R_L/R_F$). Hence, employing Equation 11,

$$A_V^{\text{open-loop}} = \frac{v_{out}}{v_{in}} = -\frac{g_{m1} A r_{o1} (R_L // R_F)}{(R_L // R_F) + R_S r_{o1} g_{mb1} + R_S (A+1) g_{m1} r_{o1} + R_S + r_{o1}}$$

(13)

where $v_{in}$, the equivalent small-signal voltage at the positive terminal of the $g_m$-boosting amplifier, is given by

$$v_{in} = i_{in} \frac{1}{g_{m2} + \frac{1}{r_{o2}} + \frac{1}{R_F}}$$

(14)

Hence, the open-loop transimpedance gain is given by

$$Z_{\text{TIA}}^{\text{open-loop}} = -\frac{g_{m1} A r_{o1} (R_L // R_F) \left( \frac{1}{g_{m2} + \frac{1}{r_{o2}} + \frac{1}{R_F}} \right)}{(R_L // R_F) + R_S r_{o1} g_{mb1} + R_S (A+1) g_{m1} r_{o1} + R_S + r_{o1}}$$

(15)

And the closed-loop transimpedance gain is given by

$$Z_{\mathrm{TIA}}^{\mathrm{closed-loop}} = -\frac{g_{m1}Ar_{o1}(R_L//R_F)\left(\frac{1}{g_{m2}+\frac{1}{r_{o2}}+\frac{1}{R_F}}\right)}{(R_L//R_F)+R_S r_{o1} g_{mb1}+R_S(A+1)g_{m1}r_{o1}+R_S+r_{o1}}}{1+\frac{1}{R_F}\frac{g_{m1}Ar_{o1}(R_L//R_F)\left(\frac{1}{g_{m2}+\frac{1}{r_{o2}}+\frac{1}{R_F}}\right)}{(R_L//R_F)+R_S r_{o1} g_{mb1}+R_S(A+1)g_{m1}r_{o1}+R_S+r_{o1}}} \quad (16)$$

where the standard feedback factor $\beta = 1/R_F$.

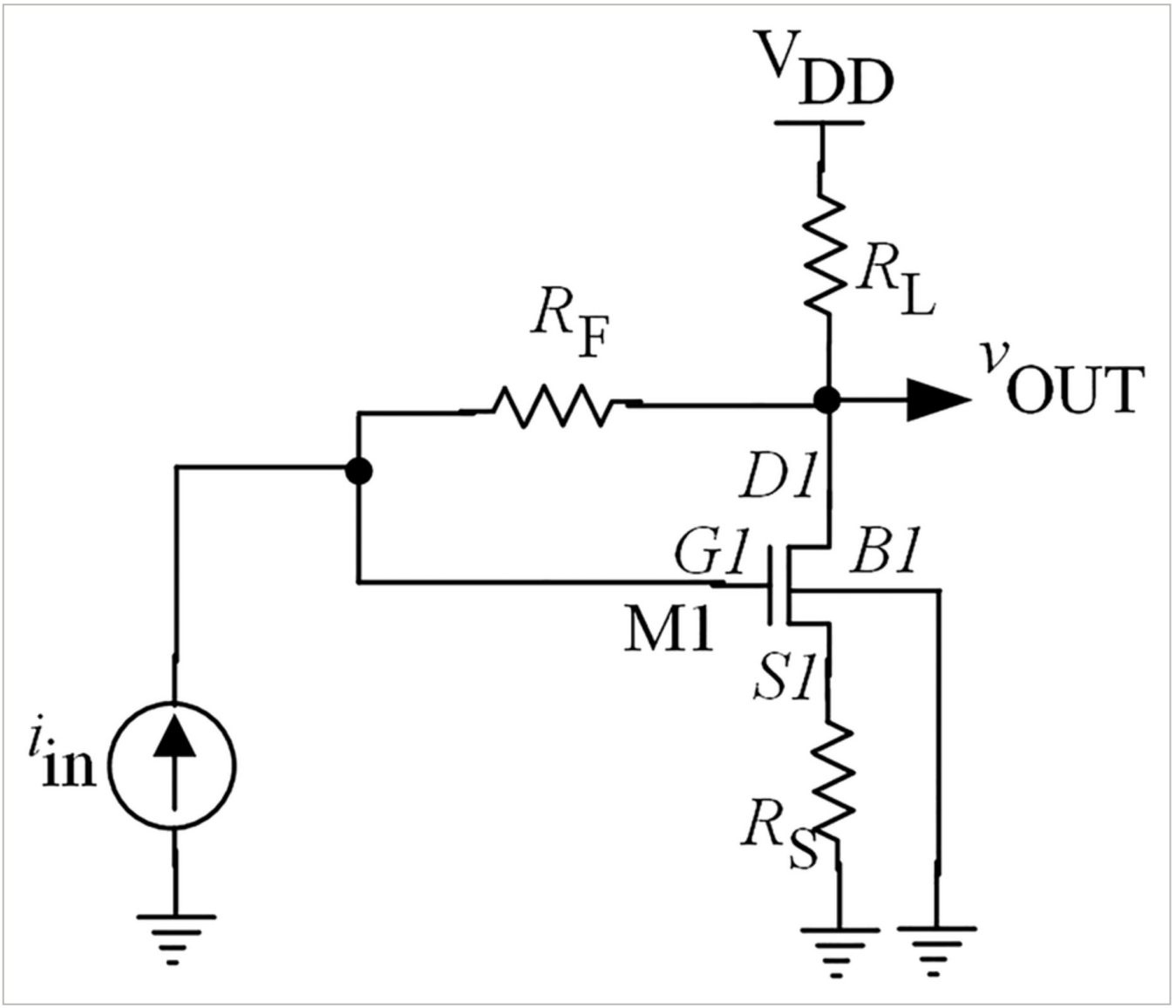


**FIGURE 3**

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A common source with source degeneration wired up in a transimpedance amplifier configuration

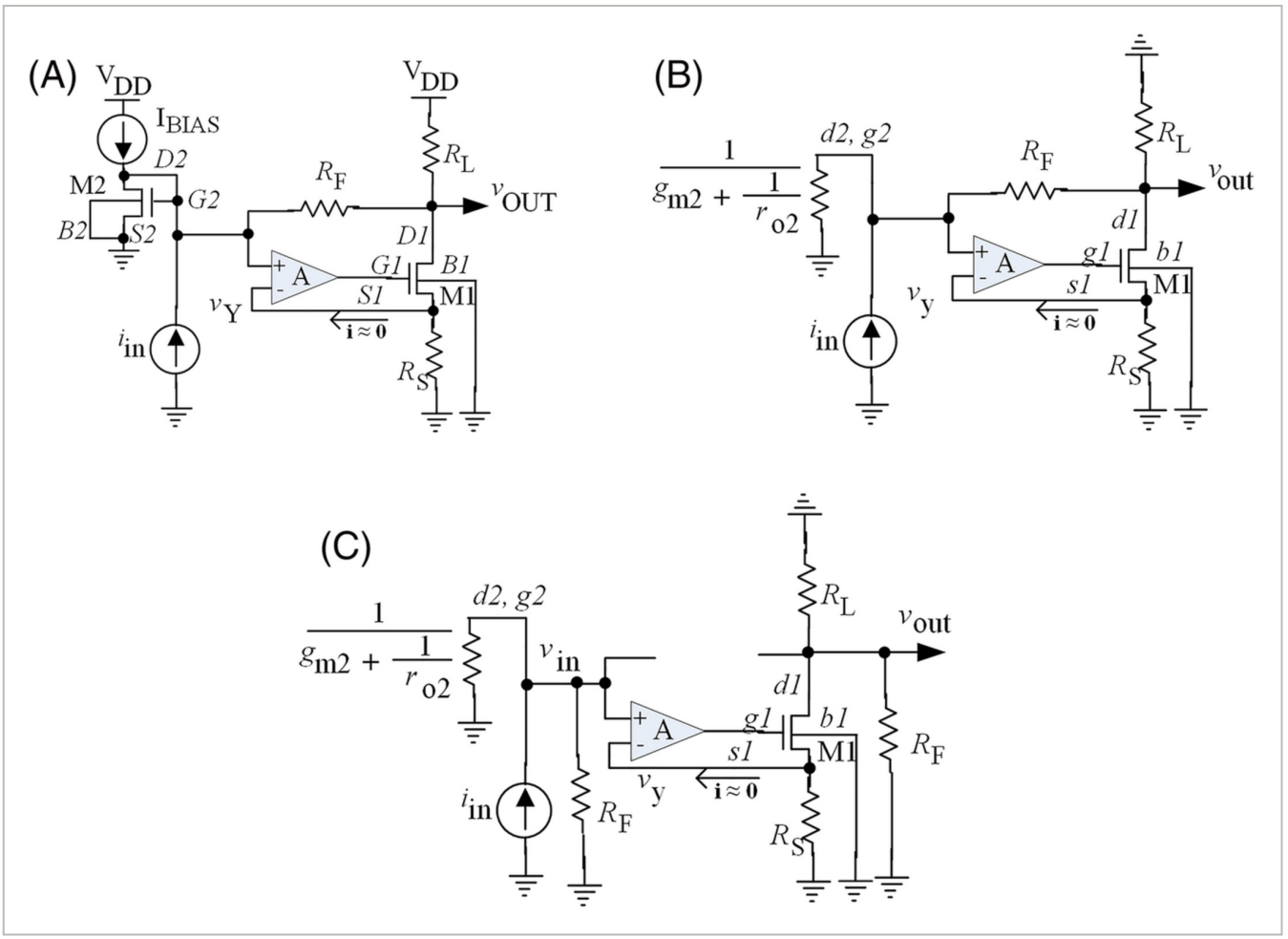


**FIGURE 4**

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A $g_m$-boosted common source with source-degeneration stage configured for operation as a transimpedance amplifier, (A) with bias circuit for proper operation as a current-feedback amplifier, (B) its AC equivalent circuit, and (C) the open-loop circuit for determining the loop gain and the closed-loop transimpedance gain

# 4 PERFORMANCE VERIFICATION THROUGH SIMULATION RESULTS

Simulations were carried out on Cadence for the presented circuits employing a 1.8-V power supply, current-source load and resistive source degeneration. Similar device sizes and component values were employed for the corresponding transistors and resistors for the $g_m$-boosted and the non-$g_m$-boosted (basic) amplifiers for their performance comparisons. Figure 5A shows the $g_m$-boosted common source with source-degeneration stage for simulation along with the transistor-level diagram of the $g_m$-boosting amplifier. The device sizes and component values were as follows: W/L = 2 μm/0.2 μm for M1, W/L = 2 μm/0.370 μm for M2, W/L = 2.8 μm/0.220 μm for M3 and M4, W/L = 6 μm/0.220 μm for M5 and M6, W/L = 4.4 μm/0.180 μm for the tail device M7, and finally, $R_S$ = 10 k. The bias voltages $V_{G2}$ and $V_{G7}$ were 695 and 590 mV, respectively, whereas the common-mode DC input voltage at $v_{in}$ was 701 mV. Figure 6 shows that the voltage gain of the $g_m$-boosted common source with source-

degeneration stage is much higher compared with that for the common source with source-degeneration stage without $g_m$ boosting for similar size of gain device, load device, and source-degeneration resistor. Next, Figure 7 shows a comparison of the voltage gain of common source with source degeneration, with and without $g_m$ boosting with increasing value of a finite resistive load $R_L$. With increasing finite load resistance $R_L$, the gain of the amplifier approaches toward the intrinsic gain of the amplifier. Hence, in agreement with the expression for the intrinsic gain of the ordinary common source with source degeneration ($g_m r_o$) compared with that of the $g_m$-boosted common source with source degeneration ($Ag_m r_o$) given by Equation 9, the gain increases rapidly with $R_L$ in the case of the $g_m$ boosting. This verifies the gain enhancement achieved by employing the $g_m$ boosting.

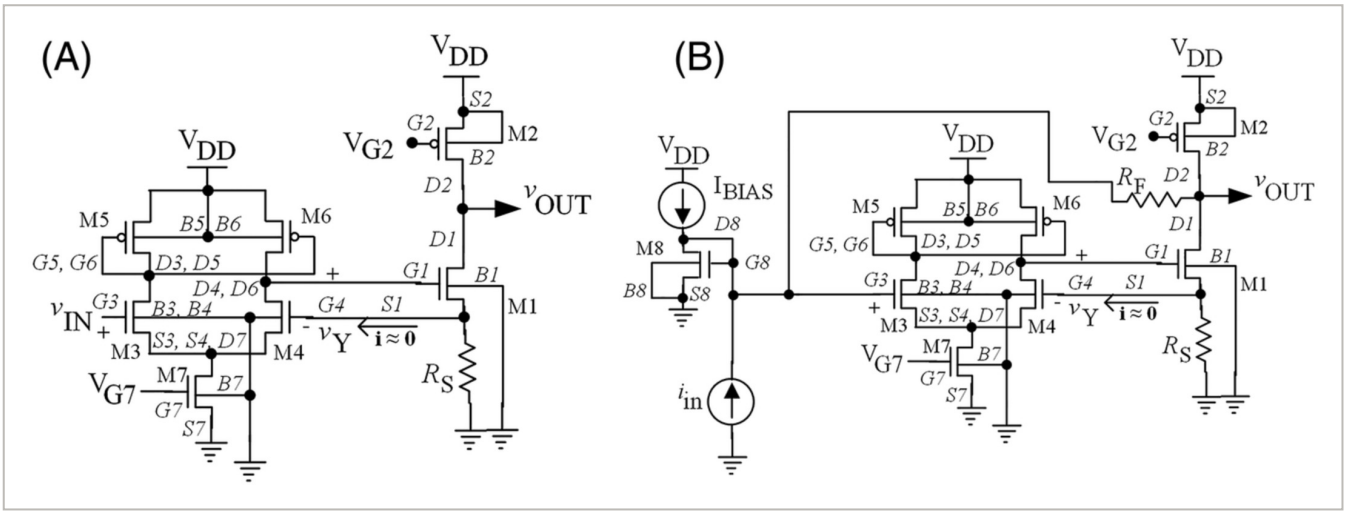


**FIGURE 5**

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(A) A $g_m$-boosted common source with source-degeneration stage for simulation and (B) a TIA configuration of the $g_m$-boosted common source with source degeneration for simulation

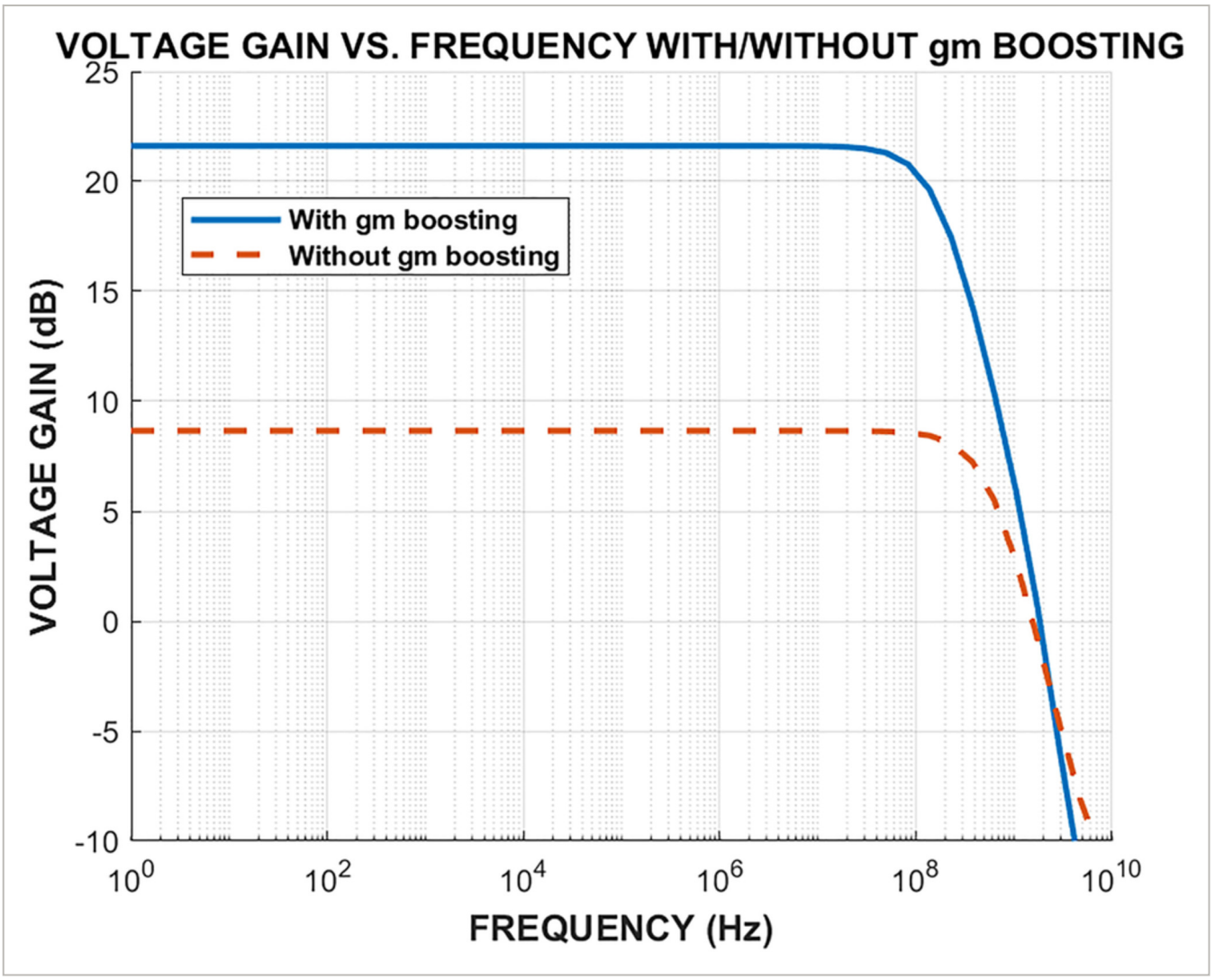


**FIGURE 6**

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Comparison of the voltage gain of common source with source degeneration, with and without $g_m$ boosting

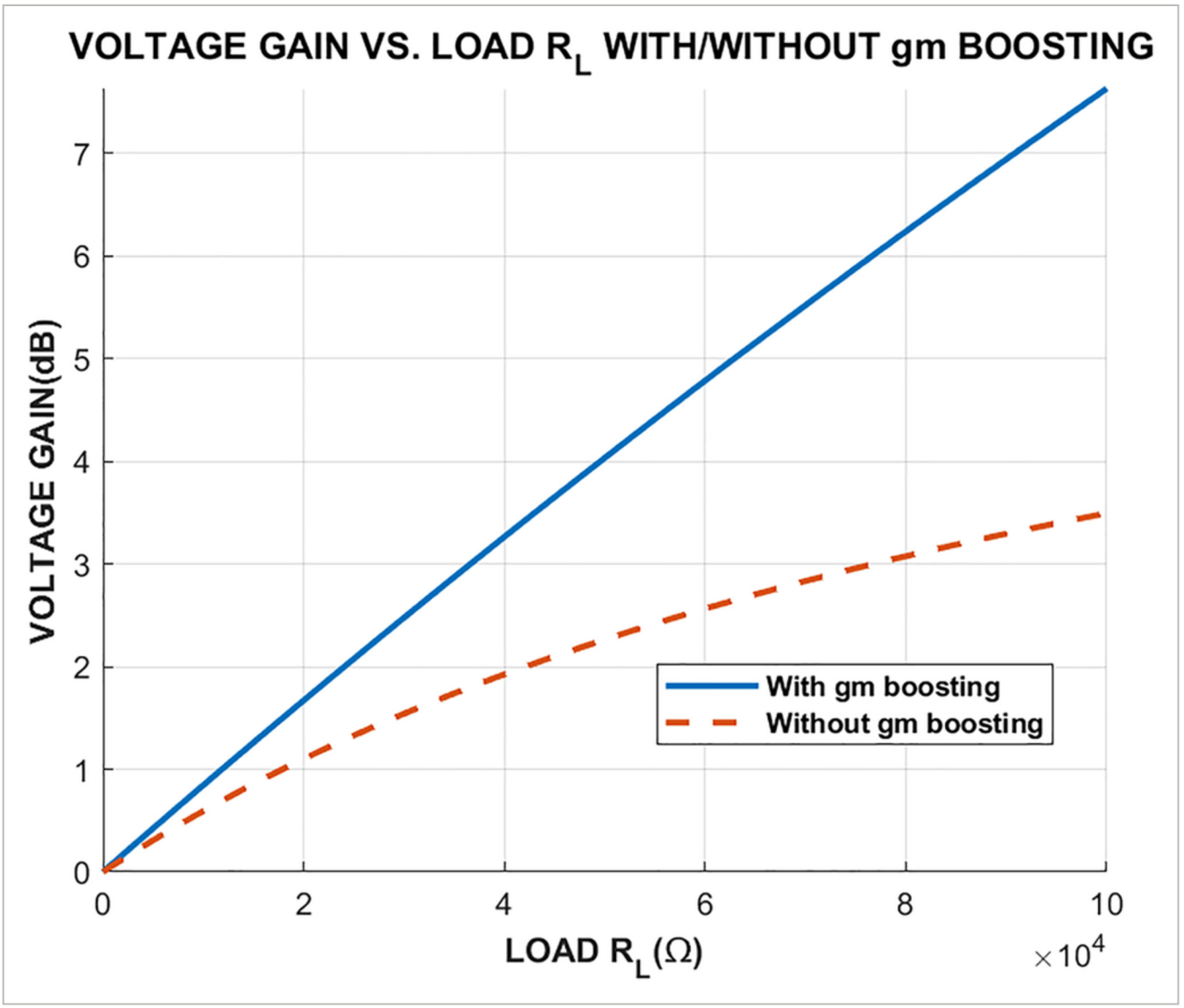


**FIGURE 7**

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Comparison of the voltage gain of common source with source degeneration, with and without $g_m$ boosting with increasing value of a finite resistive load $R_L$

Next, Figure 5B shows the TIA configuration of the $g_m$-boosted common source with source degeneration for simulation along with the transistor-level diagram of the $g_m$-boosting amplifier. The device sizes and component values were as follows: W/L = 2.7 μm/0.180 μm for M1, W/L = 5.5 μm/0.220 μm for M2, W/L = 2.8 μm/0.220 μm for M3 and M4, W/L = 6 μm/0.220 μm for M5 and M6, W/L = 4.4 μm/0.180 μm for the tail device M7, W/L = 3.5 μm/0.180 μm for the bias device M8, the source degeneration $R_S$ = 6 k, and the feedback resistor $R_F$ = 1 k. Also, the bias current $I_{BIAS}$ = 15 μA and the bias voltages $V_{G2}$ and $V_{G7}$ are respectively 800 mV and 590 mV. Figure 8 shows the comparison of the transimpedance gain of the TIA configuration of common source with source degeneration, with and without $g_m$ boosting. It is clearly seen that the voltage gain of the $g_m$-boosted common source with source-degeneration TIA is much higher compared with that for the ordinary common source with source-degeneration

TIA without $g_m$ boosting for similar size of gain device, load device, feedback resistor, and source-degeneration resistor.

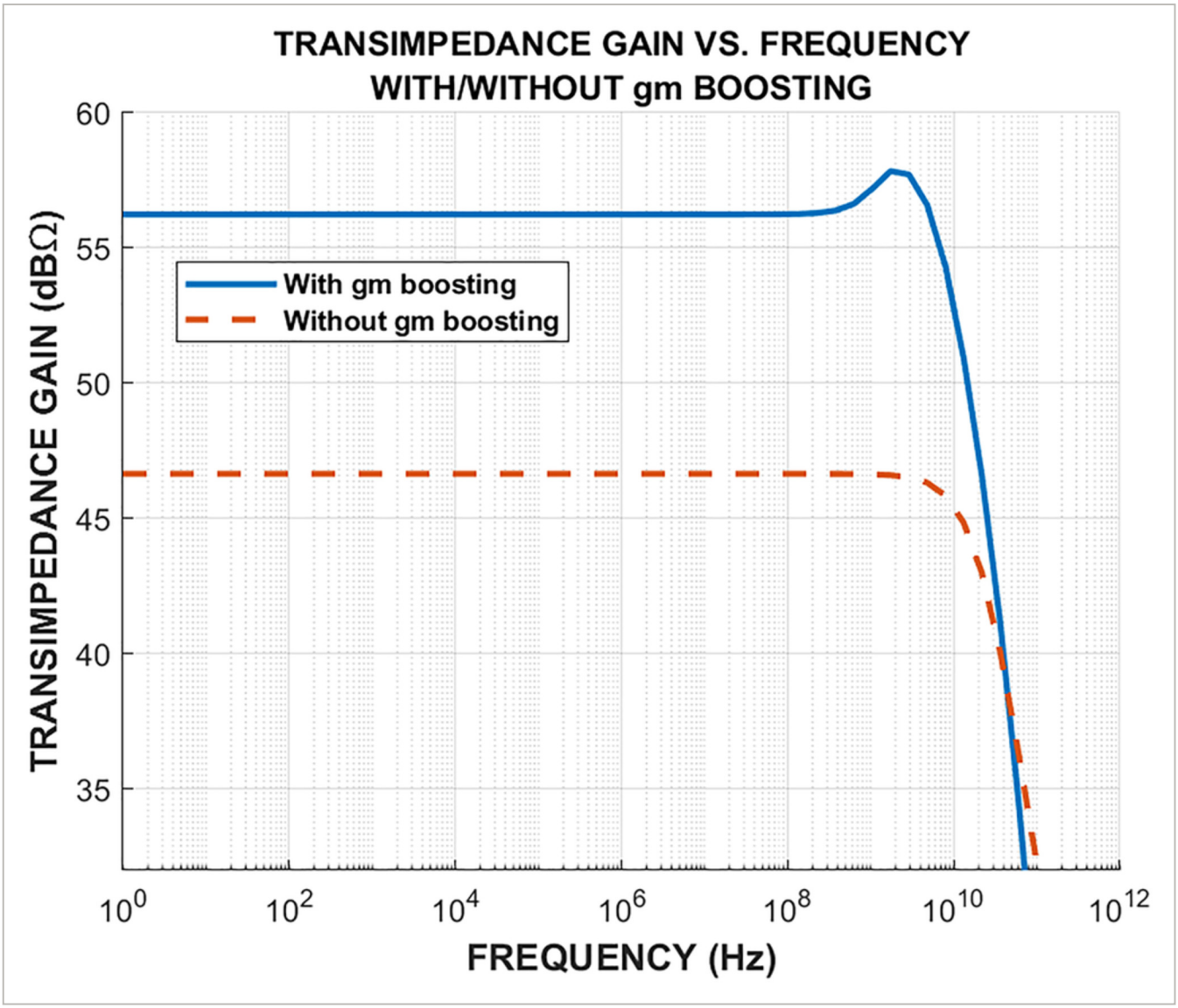


**FIGURE 8**

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Comparison of the transimpedance gain of the TIA configuration of common source with source degeneration, with and without $g_m$ boosting

# 5 CONCLUSION

Details of a $g_m$-boosted common source with source-degeneration stage and its new TIA configuration for transimpedance gain have been presented. Simplified inspection-based small-signal analysis is provided for these structures that do not require the solution of any simultaneous nodal or mesh equations. Simulations indicate that as expected, much higher gain is achievable using these structures employing the $g_m$-boosting gain $A$. A biasing scheme is also provided to configure the $g_m$-boosted common source with source-

degeneration stage as a TIA without which the amplifying device would be driven into the triode region.

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## DATA AVAILABILITY STATEMENT

Data sharing is not applicable for this article, and hence research data are not shared.

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