Exploring the Implementation of JPEG Compression on FPGA

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Abstract

This thesis presents an implementation of JPEG compression on a Field Programmable Gate Array (FPGA) as the data are streamed from a camera. The goal was to minimise the usage of logic resources of the FPGA and the latency at each stage of the JPEG compression. The modules of these architectures are fully pipelined to enable continuous operation on streamed data. The designed architectures are detailed in this thesis and they were described in Handel-C. The correctness of each JPEG module implemented on Handel-C was validated using MATLAB.

The software and hardware based algorithms did result in small differences in the compressed images as a result of simplifying the arithmetic in hardware. However, these differences were small, with no discernible difference in image quality between hardware and software compressed images.

The JPEG compression algorithm has been successfully implemented and tested on Altera DE2-115 development board. Improvements were made by minimising the latency, and increasing the performance. Final implementation also showed that implementing a quantisation module in three stage pipeline fashion and using FPGA multipliers for 1D-DCT and 2D-DCT can significantly drop the logic resources and increase the performance speed. The proposed JPEG compressor architecture has a latency of 114 clock cycles plus 7 image rows and has a maximum clock speed of 55.77MHz. The results obtained from this implementation were very satisfactory.

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