Increasing the Spectral Efficiency of Continuous Phase Modulation Applied to Digital Microwave Radio: A Resource Efficient FPGA Receiver Implementation

A thesis presented in partial fulfilment of the
requirements for the degree of

Master of Engineering
in
Electronics and Computer Systems
Engineering

at Massey University, Palmerston North,
New Zealand

Andrew B. Bridger
B.E. (Hons 1)

November 2, 2009

Abstract

In modern point to point microwave radio systems used to backhaul cellular voice and data traffic, quadrature amplitude modulation (QAM) is the norm. These systems require a highly linear power amplifier which is expensive and has relatively low power efficiency. Recently, continuous phase modulation (CPM) has been deployed in this market. The CPM transmitted waveform has a constant envelope and so a non-linear RF power amplifier can be used. This significantly reduces cost and improves power efficiency.

Two important disadvantages of CPM are receiver complexity and inferior spectral efficiency compared to QAM. This thesis demonstrates a 50% spectral efficiency improvement over an existing CPM configuration without loss of detection efficiency. This is achieved by moving to coherent demodulation and extending the duration of the CPM phase pulse to 3 symbol periods.

This new CPM configuration of h=1/4, M=4, L=3, is evaluated against ETSI requirements for a 28 MHz channel carrying 24 E1 circuits. Simulation of the receiver floating point model demonstrates all requirements are met. The detection efficiency requirement is exceeded by 4.7 dB. Carrier recovery, phase and timing synchronisation are assumed to be ideal.

The 50% increased symbol rate, coherent reception and a longer smoother phase pulse, conspire to increase receiver complexity substantially. The Viterbi algorithm is used to perform maximum-likelihood detection resulting in a 128 state trellis. This application has a stringent cost requirement that limits the implementation target to a Field Programmable Gate Array (FPGA) costing less than US$30. To demonstrate this demanding cost target is met, the two most computationally expensive receiver functions, the branch metric unit and path metric processing unit, are implemented in VHDL and targeted to a Xilinx Spartan 3A-DSP 1800 FPGA. The implementation uses 67% of the available logic resources, thus meeting the cost requirement.

The branch metric unit is implemented using a distributed arithmetic technique that performs the equivalent of 27.6 giga-multiplies/s, consuming only 23% of the available FPGA logic cells. This is very efficient compared to a conventional approach using all the FPGA's embedded multipliers which combined can only achieve 21 giga-multiplies/s.

The Viterbi path metric processing unit is implemented using a more conventional state-parallel architecture. To reduce state metric routing complexity, states are grouped into radix-4 units comprising dual add-compare-select (ACS) units. By utilising a spare cycle in the deep ACS pipeline, each ACS unit processes two output state metrics, thus halving the number of ACS units required. This implementation uses 44% of the available FPGA resources and meets timing at 204.5 MHz, exceeding the throughput requirement of 54 Mbit/s.

Acknowledgements

I would like to acknowledge and thank those who have helped me during my research and made it all possible.

This thesis was completed under a Technology Industry Fellowship (TIF) Education scholarship in conjunction with Harris Stratex Networks (NZ) LTD and Massey University. This support from FRST is much appreciated.

A big thanks to Dr Philip Secker, my project mentor from Harris Stratex Networks, for his role in kick starting the project and securing funding from FRST and Harris Stratex Networks. Also for taking the time out from a busy schedule to offer guidance, read my long emails and answer my many questions throughout the year, and provide feedback on this thesis.

I would like to thank Harris Stratex Networks for their commitment to the project in the form of Philip's time and a stipend contribution.

Many thanks to Dr Xiang Gui, my academic supervisor in Palmerston North, for his time spent listening and offering guidance during our weekly progress meetings, for ensuring I had access to the university's resources I needed, and for taking the time to review my thesis.

I would also like to thank Dr Edmund Lai, my co-supervisor based in Wellington, for his wise words, excellent thesis writing resources on his website, and for taking the time to provide feedback on my thesis.

Colin Plaw and Patrick Rynhart helped me with VPN access to the university labs and ensured I had access to a source code repository. Managing all the material created throughout the year would have been much much harder without it, thank you.

To my parents, Mum, Dad, Ma and Baba, thank you for all your encouragement and support, and for all the dinners that have been cooked for me over the last 6 months while I have been writing up this thesis. Also, thank you Mum for proof reading the whole thesis.

Finally, a very special thank you to my lovely wife Mandira, for convincing me to pursue my FPGA and digital signal processing passion in the form of a Masters in Engineering. Thank you for your constant encouragement and understanding during the thesis writeup phase.

Contents

List of Figures

List of Tables

Glossary

ACI	Adjacent Channel Interference
ACS	Add-Compare-Select
ACSU	Add-Compare-Select Unit
ADC	Analog to Digital Converter
AGC	Automatic Gain Control
ASIC	Application Specific Integrated Circuit
ASSP	Application Specific Standard Product
AWGN	Additive White Gaussian Noise
BER	Bit Error Rate
BMU	Branch Metric Unit
BRAM	Block Random Access Memory
CCI	Co-Channel Interference
CFO	Carrier Frequency Offset
CPFSK	Continuous Phase Frequency Shift Keying
CPM	Continuous Phase Modulation
DA	Distributed Arithmetic
DALUT	Distributed Arithmetic Look-Up Table
DSP	Digital Signal Processor
DUT	Device Under Test
ETSI	European Telecommunications Standards Institute
FEC	Forward Error Correction
FPGA	Field Programmable Gate Array
GMSK	Gaussian Minimum Shift Keying
IF	Intermediate Frequency
LC	Logic Cell
LUT	Look-Up Table
ML	Maximum-Likelihood
MLSD	Maximum-Likelihood Sequence Detector

MSK Minimum Shift Keying

PAM Pulse Amplitude Modulation
PSD Power Spectral Density

QAM Quadrature Amplitude Modulation

RC Raised Cosine
REC Rectangular
RF Radio Frequency
RLOC Relative Location
RSL Received Signal Level

SER Symbol Error Rate
SMU Survivor Management Unit
SNR Signal to Noise Ratio
SRAM Static Random Access Memory
SRC Spectrally Raised Cosine
STA Static Timing Analysis

TFM Tamed Frequency Modulation

UHF Ultra-High Frequency

VHDL VHSIC hardware description language
VHSIC Very-High-Speed Integrated Circuit
VME VERSA-module Europe