An Analysis of the Influences of Power Electronics Devices on Fundamental Frequency Front Ends

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Abstract

New power electronics devices like Fundamental Frequency Front Ends (F3E) reduce procurement costs by eliminating or reducing the intermediate capacitors usually found on the DC-side of modern rectifier-inverter combinations. This cost-saving measure, however, eliminates the quasi-decoupling of rectifier and inverter; whereas interactions between rectifier and inverter could be neglected in most applications. These interactions are relevant to the correct function and operation of the whole application in case of reduced intermediate capacitors. Without the decoupling of rectifier and inverter, the inverter input currents will be passed on to the rectifier, and ultimately, will be discernible on the power grid. As a result, the input currents of the appliance will deviate greatly from the idealised sinusoidal waveform. To reduce this effect, an input filter is used, which in turn might interact with other power electronics devices connected to the same power grid.

To date, the scope of the rectifier inverter and the F3E third-party equipment interactions has not been sufficiently investigated. An examination with real devices is impractical due to the wide range of configurations possible and the potential harm to the equipment itself. In this study, the simulation models of the devices involved and the power grid connecting different appliances were developed. A theoretical analysis to identify possible areas of impaired or disturbed operation was undertaken. The areas identified were then analysed using the computer models developed. The simulation results, electrical currents, and voltages were examined with regards to their absolute values and their degree of deviation from the idealised sinusoidal form. Their harmonic spectra were likewise analysed. Finally, areas of disturbed operation and the conditions under which they occur were identified. This study, therefore, will provide the basis for the successive elimination of these areas of disturbed operation.

Acknowledgments

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1 Introduction

The Fundamental Frequency Front End (F3E) is a promising new rectifier topology, which is now being used in conjunction with frequency inverters to control and power electrical drives. The F3E, in many cases, has proven to be more cost-effective than the well-known and widely used Active Front End (AFE). The efforts with regards to semiconductors are, likewise, reduced. The large intermediate capacitor and line inductors can be omitted, as the F3E requires instead a capacitive filter on the input side. Omitting the intermediate capacitor and introducing a capacitive filter renders the F3E susceptible to the influences of other power electronics devices. These influences are significant compared with the other topologies currently used and are expected to increase over time as more F3E devices will be used in the future.

The frequency inverter functions as load to the F3E when connected to the F3E output terminals. Consequently, the line filter will be exposed to the pulsed DC current of the inverter. This condition, in conjunction with the generally unknown impedance of the supply grid, can lead to unwanted interactions or resonant effects. If the AC output terminals of the F3E are used to supply power-electronics devices, interactions with the F3E input filter are possible. Devices employing chopping actions in their operation, such as the AFEs or the Direct Frequency Converters (DFCs) can significantly stress the line filter with higher harmonics.

This study was undertaken to examine the above-mentioned influences of the frequency inverter on the DC side and an AFE operated on the same power line as the F3E on the line filters through the use of computer simulations. The results were evaluated theoretically and with regards to their consequences. Of special importance to the study was the identification of critical operating conditions, which would require corrective measures to ensure a safe operation within the specifications of the devices employed.

2 Review of literature

Significant changes in the realm of electrical drives have taken place since the seventies. The inductive motor has gained wide acceptance mainly because of its robustness and ease of use in conjunction with three-phased inverters. It increases, however, the use of power electronics circuits and the associated non-sinusoidal load currents. It also creates higher harmonics leading to additional losses in the power grid.

Nowadays, a number of energy suppliers demand the implementation of corrective measures such as the use of line filters. Another corrective measure being undertaken is the use of capacitors in conjunction with inductive loads. Both measures lead to the creation of resonant circuits with resonant frequencies, which need to be adjusted to the higher harmonics content created by the power electronics circuits.

Most commonly voltage-source inverters are used in combination with inductive motors resulting in a block-like shape of the motor supply voltage. These non-sinusoidal voltages induce higher harmonics within the motor current leading to additional losses within the motor itself. Insulation problems can also occur due to the higher voltage dynamics. To alleviate these problems, the use of filters on the output side is increased.

Until recently supply side and the output side of the inverter topology could be seen as independent from each other because of the generally large intermediate capacitors used. As such, they do not influence each other. Within the last decade, however, increasing topologies, which aim at eliminating or reducing the expensive intermediate capacitor have been introduced. These topologies are capable of feeding back energy into the power grid. One example is a device called “Fundamental Frequency Front End” or F3E introduced by Göprich et. al., (2003). The disadvantage of this device, is the passing through of the switching patterns from the inverter to the supply side or power grid. The dampening resistors and filter capacitors try to eliminate these feedback effects and in so doing, take over the function of the intermediate capacitor.

To provide a proper understanding of the context, effects, and specifications of the components involved, the relevant classifications and characteristics of modern energy supply networks, including its components, will be introduced and explained. They serve as an entry point for the terminology used in this work.

2.1 Classification of voltage levels

The German power grid, as of 2003, has a total length of 160 mil km, 71% of which are located underground (Buchow, 2006). A classification of networks with different voltage levels ensures the supply for each costumer.

The different levels of voltage as defined by their usage in the power grid are as follows:

- High and ultra-high voltage grid – this is the main element of the power transmission used for long distance power transmission. Sometimes the relatively big industry consumers are connected directly to the high voltage level;
- Medium voltage grid – this is used for the distribution of electrical energy in bigger cities, or sparsely populated rural areas; industrial facilities are oftentimes directly connected to this voltage level; and
- Low voltage grid – this grid is responsible for supplying electrical energy to the end consumers.

High and ultra-high voltage lines are usually limited to a length of 500 km. Longer than this, losses reach an uneconomical level with AC-operation. For distances exceeding 500 km, a high voltage DC current transmission is used.

The low voltage grid is of importance to this study; thus, it will be described more in detail. A low voltage grid is defined as the transmission of voltages below 1kV (Buchow, 2006). There are a number of different configurations being used worldwide. The most common configuration is the one-phased 50Hz grid with a nominal voltage of 230V. In this study the three-phased supply system with a nominal voltage of 400V at 50Hz is of more importance. With this configuration, losses can be reduced and the transmitted power, increased.

2.2 Transformer

The transformer is the connecting piece of equipment between the different voltage levels of the power grid (Buchow, 2006). It can be separated into different categories, depending on its usage. These categories are as follows:

- Generator transformer - typically used at power plants to set the voltage to high and ultra-high levels;
- Interconnection transformer – used in connecting different networks on the high and ultra-high voltage levels;
- Mains transformer – this is the transformer between the high and medium voltage levels; and
- Dispersion transformer – this is the transformer between the medium and low voltage levels.

The dispersion transformer is of direct interest in this study. The alternate circuit diagram used for analysing of transformer power flow and losses is usually a one-phased abstraction of the three-phased transformer (Fig. 2.1). The diagram is further simplified by omitting the inductance L_M and the resistor R_C (Fig. 2.2), which is generally done in the realm of energy supply systems. Under normal operating conditions, they exert little influence on the behaviour of the transformer in the rated power class relevant to this study. The simplified diagram greatly reduces the computational requirements for simulation purposes without unduly sacrificing accuracy.

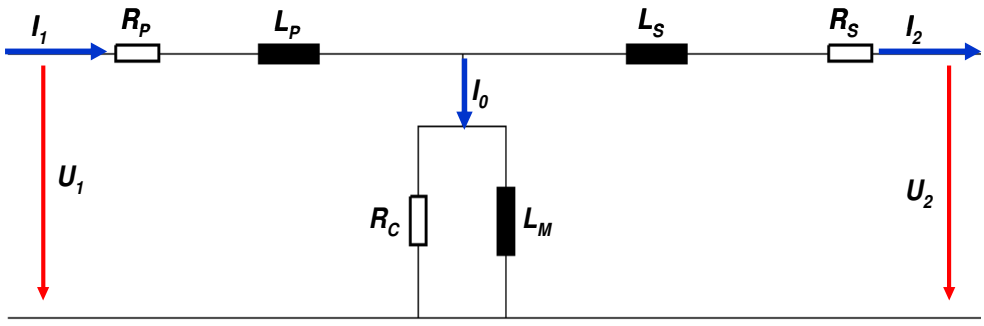

Fig. 2.1: Single-phased alternate circuit diagram of a transformer

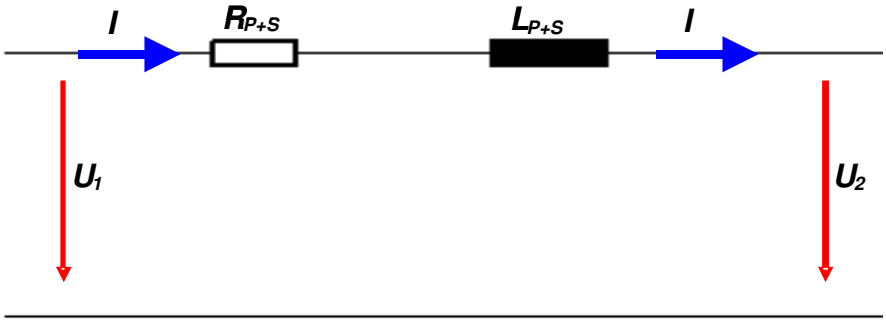

Fig. 2.2: Simplified single-phased alternate circuit diagram

2.3 Power electronics

The power electronics circuits and configurations are based on similar semiconductor components and represent different topologies designed for different purposes. The configurations relevant to this study are:

- Pulse Controlled Inverter (PCI);
- Active Front End (AFE);
- B6-rectifier; and
- Fundamental Frequency Front End (F3E).

2.4 Inverter

Inverters convert a DC voltage or current into an AC voltage or current (Specovius, 2008). The frequency of the AC output value can be set to any value required for the load attached. They are available in two variations, namely: voltage (VSI), and current source inverter (CSI). Figures 2.3 and 2.4 illustrate the resulting basic topologies in combination with a three-phased rectifier. Of relevance to this study is the VSI topology generating a three-phased voltage system.

The internal topology of the VSI (Fig. 2.5) has a significant impact on the analysis of the behaviour of its output values such as voltage and current. Their behaviour, however, is not only determined by the inverter topology, but also by the control strategies used by the inverter. These inverters are usually used to supply AC drives

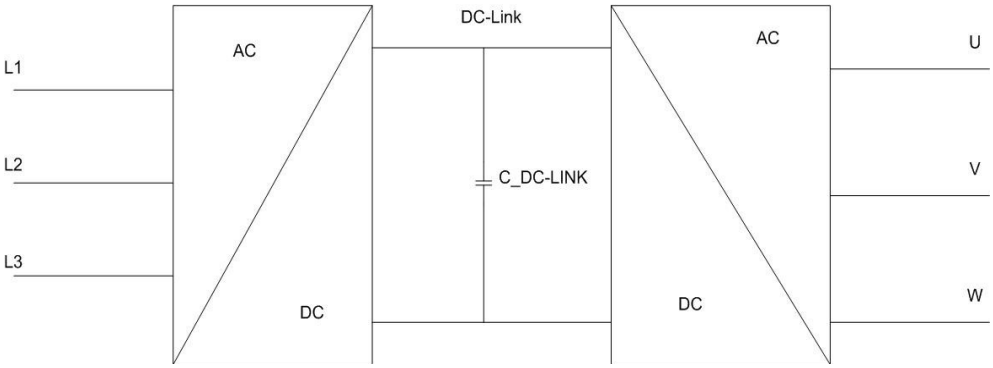

Fig. 2.3 Topology with voltage source inverter

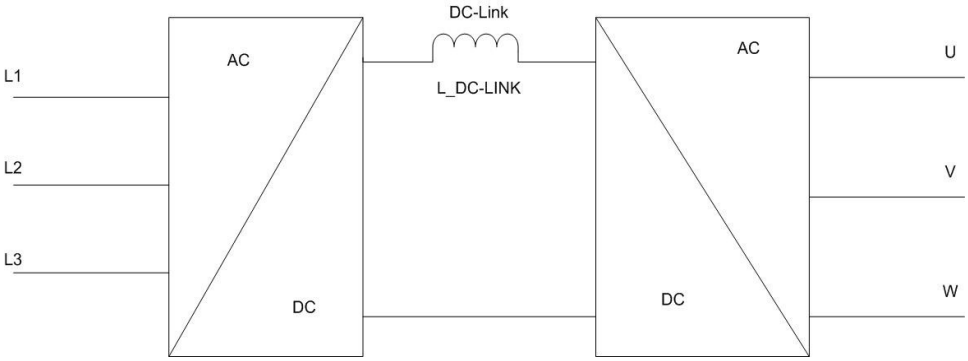

Fig. 2.4 Topology with current source inverter

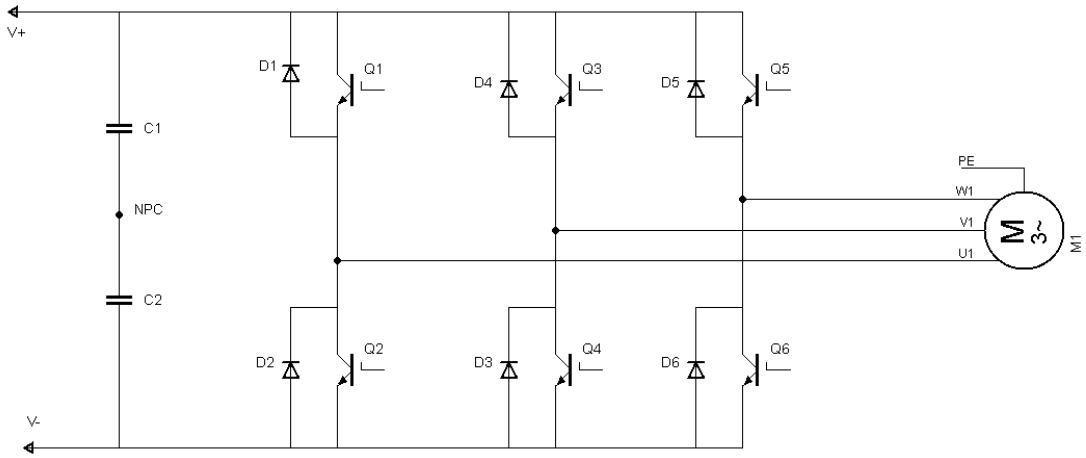

Fig. 2.5: Internal topology of a VSI with an AC drive as load

with the needed voltage and current at a variable frequency. In this regard, the inductive properties of the load are importance.

The semiconductors used (D1 to D6, and Q1 to Q6) in Fig. 2.5 are usually available as integrated modules. For smaller power ratings up to 20kW, all semiconductors are

confined to a single module. Above the rated power of 20kW, multiple modules are used.

For the analysis of the inverter behaviour, the IGBTs Q1 to Q6 are simplified as idealised switches. In standard configurations, the intermediate capacitors C1 and C2 in Fig. 2.5 have sufficient capacity to provide a constant input voltage to the inverter. Thus, the topology of a standard VSI (Fig. 2.3) can be simplified (Fig. 2.6).

Figure 2.6 clearly shows that the basic semiconductor configuration of all three phases of the inverter is identical. For a standard analysis or simulation, the capacitors of the original circuit diagram are replaced by voltage sources. For the control of the insulated gate bi-polar transistors (IGBTs) of any one phase of the inverter, the list in Table 2.1 is valid.

Table 2.1: List of possible semiconductor states

No	T1	T2
1	1	0
2	0	1
3	0	0
4	1	1

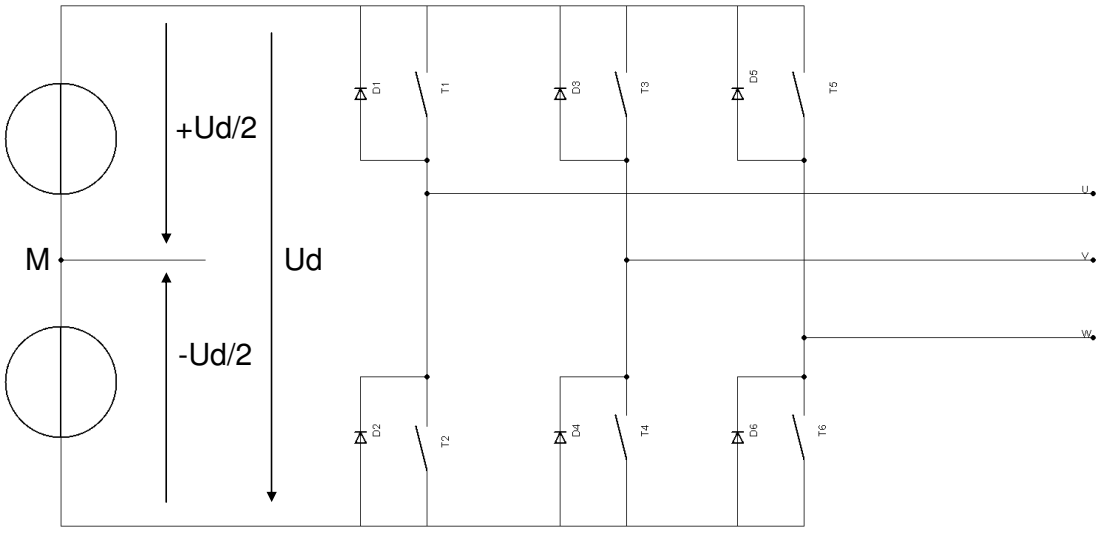

Fig. 2.6: A simplified VSI topology

It is assumed under standard operating conditions that the load in any phase will always include an inductance. Therefore, interrupting the current in any phase will result in high inductive voltages, dangerous to the semiconductors. Short circuiting the intermediate capacitors will also result in high currents, endangering the semiconductors. The allowed states of the semiconductors are presented in Fig. 2.7. Taking into account considerations previously mentioned, and combining an IGBT and its anti-parallel diode into one switch, it can be concluded that only one semiconductor in each phase will be in a conductive state any time. If a semiconductor in the upper half bridge of one phase is in a conductive state, its state will be defined as a logical 1; otherwise, as a logical 0 (Table 2.2).

logical 1 logical 0

Fig. 2.7: Definition of the logical states and the associated flow of current (Peppel, 2006)

Table 2.2: The allowed logical states

No.	Phase U	Phase V	Phase W
1	1	1	1
2	1	1	0
3	1	0	0
4	1	0	1
5	0	1	0
6	0	1	1
7	0	0	1
8	0	0	0

The three possible values for the output voltage of each phase are: $+\frac{U_d}{2}$, $-\frac{U_d}{2}$ and 0. With these three discrete values, a sinusoidal voltage shape can not be synthesised. Even assuming ideal conditions, the shape of the output currents of the inverter will only be an approximation of the idealised sinusoidal waveform. The amount of

deviation will primarily depend on the switching frequency of the inverter and the load characteristics. This is generally true for circuits involving switching semiconductors.

2.4.1 Control algorithms

Among the multiple control algorithms available, the most relevant are:

- Fundamental frequency pulse control;
- Space vector control; and
- Standard Pulse Width Modulation (PWM) with sine under-shoot control.

In this study, the sine under-shoot control algorithm was used to control the semiconductors via pulse width modulation. The other algorithms, although of significant practical import, are not relevant to the study.

A sinusoidal signal compared with a delta-shaped signal of higher amplitude; hence, the name sine under-shoot control (Specovius, 2008). The frequency of the triangular signal is equal to the switching frequency of the semiconductors. When the current value of the triangular signal exceeds that of the sinusoidal signal, an output signal with a value of 0 is generated; otherwise, a value of 1. The output signal is generally referred to as PWM signal (Fig. 2.8).

In the case of three-phased inverters, only one signal for each phase has to be generated. The second control signal is simply the inversion of the first, since both semiconductor switches of one phase always operate in push-pull mode.

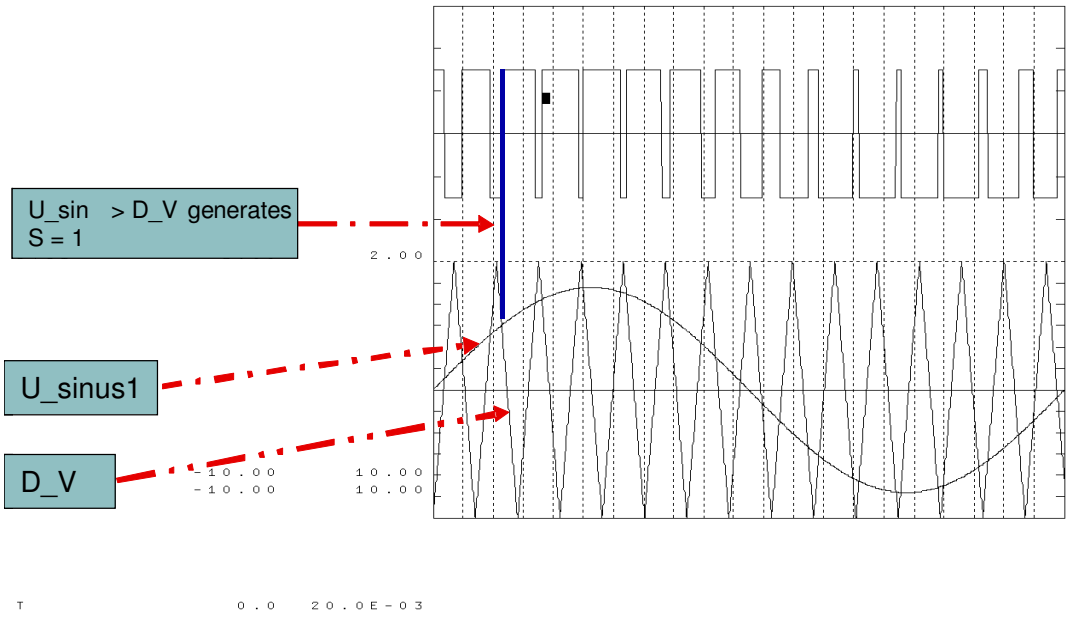

Fig. 2.8: Generation of the PWM signal

2.5 Active Front End

A rectifier capable of inverting the flow of energy, or actively feeding back energy into the power grid, is called an Active Front End (Peppel, 2006). It is capable of both reversing the flow of energy and changing the phase shift between input voltage and current. A further advantage of an AFE is the reduced amount of higher harmonics content of input current in the lower frequency range, especially the 5^{th}, 7^{th}, and 11^{th} harmonics. Figure 2.9 shows the principle circuit diagram of an AFE, including line inductors, which limit the dynamics of the input current.

An AFE is usually controlled using PWM. In order to ensure undisturbed operation of the AFE, the line voltage and current on the input side have to be monitored. The control of an AFE is significantly more complex compared with that of a controlled rectifier (Appendix I). In order to enable feedback operation, the intermediate voltage of the AFE capacitor has to be higher than the amplitude of the phase voltage on the input side for single-phased configurations and higher than the amplitude of the line to line voltage in three-phased configurations.

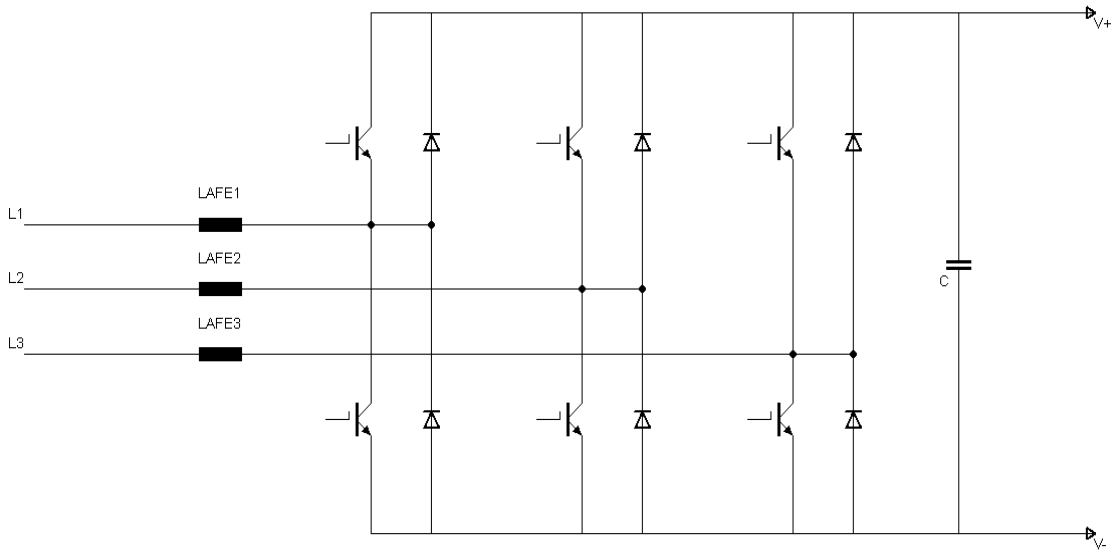

Fig 2.9: The AFE with line inductors and intermediate capacitor C

2.6 Alternative configurations

The common B6 rectifier provides an alternative input configuration serving as power supply. There is no control needed, ensuring significant cost savings (Fig. 2.10). A further advantage is the reduced rated voltage of the intermediate capacitor. In principle, feedback operations are impossible; as such, there is no requirement for exceeding the line voltage, as opposed to the AFE. Its major disadvantage is its lack of feedback capability. Despite this, this configuration is still widely used because it is cheap and easy to manufacture.

2.7 Fundamental Frequency Front End

An F3E is an extension of a three-phased rectifier, which enables the reversal of the energy flow or simply put, to feed back energy from the DC side to the power grid. If the output current of a diode rectifier constitutes a constant and uninterrupted DC-current, each diode of the rectifier will conduct the current for a third of each cycle of the supply network. With F3Es, a thyristor is connected anti-parallel to each diode, forming a bi-directional switch (Fig. 2.11). The DC output current of the F3E can, therefore, turn negative as opposed to diode rectifiers where the current is always positive. This enables the F3E to feed back energy from the DC side. The transistors

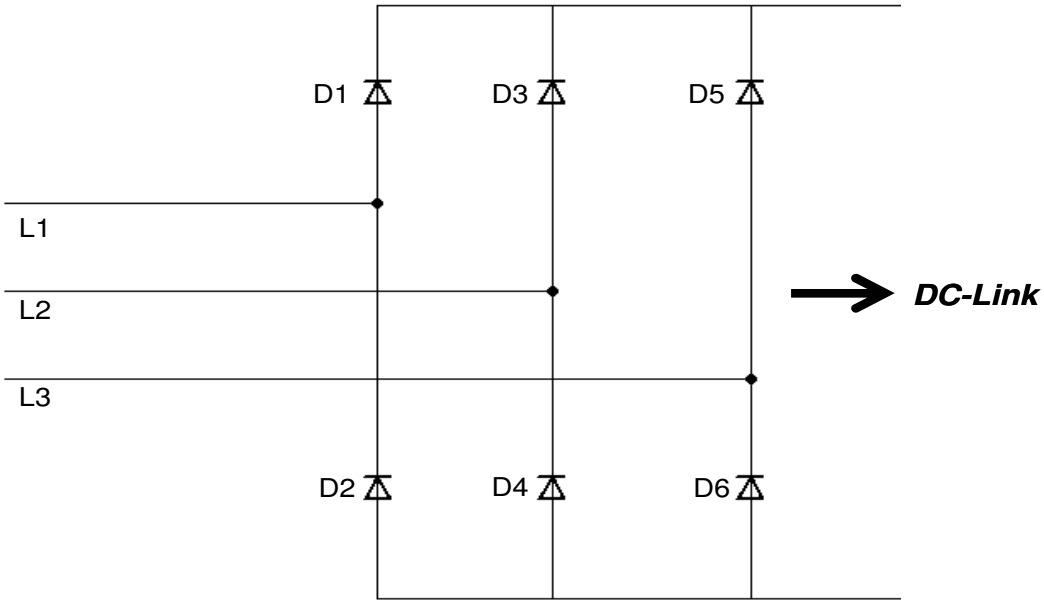

Fig. 2.10: Standard B6 rectifier topology

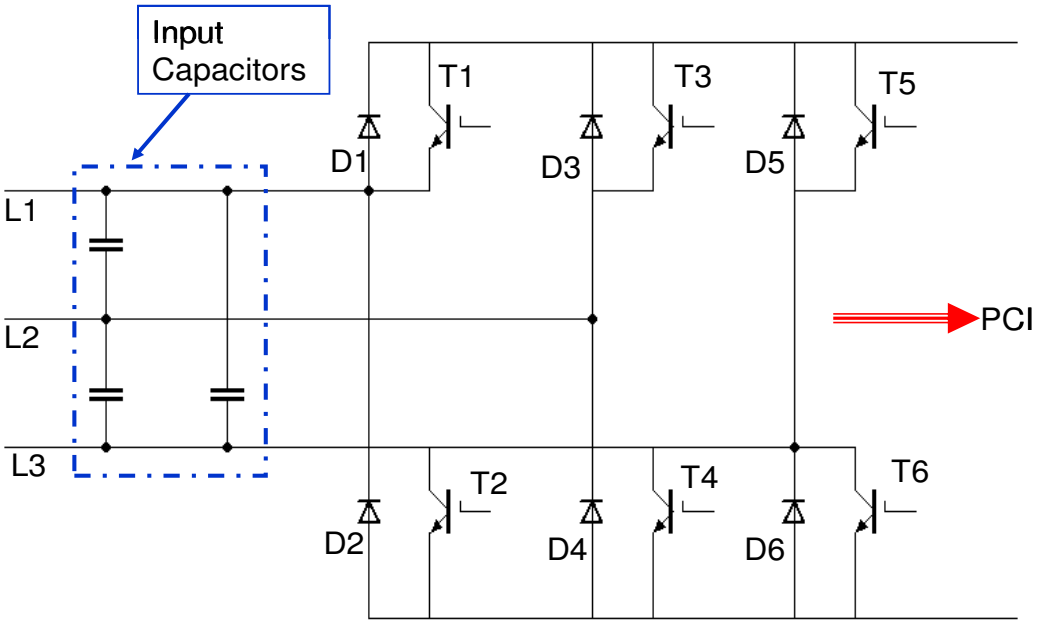

Fig. 2.11: Topology of the F3E

of the F3E are not controlled using PWM, but are switched with the fundamental frequency of the supply side, which is 50Hz in this study. In order to reduce the impact of higher harmonics on the power grid, filter capacitors are used.

2.8 Higher harmonics

Higher harmonics, as defined in the context of this work, are sinusoidal oscillations with a higher frequency than that of the fundamental harmonic. The fundamental harmonic, in the scope of this work, is always at a frequency of 50Hz.

Higher harmonics are produced by many industrial appliances. They generate additional losses, distort the supply voltage, and interfere with the operation of other equipment connected to the power grid. A major concern is the periodic but non-sinusoidal voltages and currents present on the power grid.

Any periodic non-sinusoidal signal relevant to the transmission of electrical power can be transformed into a series of sinusoidal signals with a basically unlimited frequency range. The lowest frequency will always be that of the fundamental harmonic. The Fast Fourier Transformation (FFT) provides an algorithm, which determines the amplitudes of these sinusoidal oscillations (Brigham, 1995).

Only the fundamental harmonic and the higher harmonics are relevant to the study; any constant component is deemed irrelevant. The maximum amount of higher harmonic content on the power grid is stipulated by regulation as follows:

$$U_5, U_7 \leq 0.05 \cdot U_{nN}$$
$$U_{11}, U_{13} \leq 0.03 \cdot U_{nN}$$

The FFT was applied throughout the study to determine the spectra of the electrical currents and assess the effects of current shapes on devices.

2.9 NETASIM

The program NETASIM developed by AEG (later part of the Daimler Benz Aktiengesellschaft) (Daimler Benz AG, 1995), was used as a simulation tool in this study. This program simulates power electronics and their associated applications. NETASIM employs a net list because it lacks a graphical interface to create the circuit of the model. The programming language for NETASIM is ASIM, which is

based on Fortran. It has additional access to a library of ready-to-use program modules. The program can save simulation results and draw the resulting waveforms later without repeating the simulation itself. The saved data can be processed with the help of FFT.

A more detailed description of the program is included in the appendix.

3 Model development

This chapter explains the process involved in the acquisition and verification of the models. In so doing, valuable information on how the models can be used efficiently will be obtained.

3.1 Structure of the F3E model

3.1.1 Structure of the basic model

The first step in the development of the model was the creation of a simple three-phased supply grid and an uncontrolled B6 rectifier bridge. This was done to acquire experiences in handling the simulator program in order to test the functionality and validity of single implemented macros of the simulator routine. Initially, only the existing diode models of the simulator were used for the B6 rectifier. The diode values were taken from sample files supplied with the simulator. As a first load example, a simple R-L-serial connection was used. The line current was equivalent to that of a three-phased load with a rating of approximately 16kW. A 50Hz three wire voltage supply system of 400V/230V, was used as an example. The maximum value of the grid impedance was selected in such a way that the maximum voltage drop would not exceed 3% of the phase-to-earth voltage U_{LN}. This is a requirement for connecting electrical equipment to the power grid in Germany. To determine the two individual values for R and L, a primarily active load with a power factor of 0.95 was assumed. The necessary values were determined using the simplified equations as shown below. Since the voltage drop UZ_N of the grid impedance should not exceed 3%, UZ_N was calculated based on Eq. 3.1.

$$|UZ_N| = \frac{|U_{LN}| \cdot 3}{100} \qquad \text{Eq. 3.1}$$

Another representation of UZ_N using the impedance Z_N and the current I_N is shown in Eq. 3.2.

$$|UZ_N| = |I_N| \cdot |Z_N| \qquad \text{Eq. 3.2}$$

From Eqs. 3.1 and 3.2, the expression to the current I_N was derived.

$$|Z_N| = \frac{|U_{LN}| \cdot 3}{|I_N| \cdot 100} \qquad \text{Eq. 3.3}$$

The I_N was calculated following Eq. 3.4.

$$I_N = \frac{P_N}{\sqrt{3} \cdot |U_{LN}|} \qquad \text{Eq. 3.4}$$

Based on the above-mentioned equations, the value of Z_N was calculated (Eq. 3.5).

$$|Z_N| = \frac{|U_{LN}| \cdot 3}{\left(\frac{P_N}{\sqrt{3} \cdot |U_{LN}|} \cdot 100 \right)} = 0.3\Omega \qquad \text{Eq. 3.5}$$

The computed value of the Z_N represents the maximum permissible value. It was reduced to one-third of the maximum, resulting to a value of $|Z_N| = 0.1\Omega$. For the active resistance R_{NETZ} and inductance L_{NETZ}, the resulting values were:

$$R_{NETZ} = 0.095\Omega \qquad L_{NETZ} = 99.4\mu H$$

The load was computed in a similar way. The resistor R_{LAST} was calculated according to equation 3.6; whereas, the inductance L_{Last} was selected on the assumption that the load current should reach its nominal value as fast as possible. In order to achieve this, a relatively small value of 6.125ms was selected for the time constant τ (Eq. 3.7).

$$R_{LAST} = \frac{U_{di}^2}{P} = \frac{(2.34 \cdot U_{LN})^2}{P_N} = 19.6\Omega \qquad \text{Eq. 3.6}$$

$$L_{LAST} = R_{LAST} \cdot \tau = 120\text{m}H \qquad \text{Eq. 3.7}$$

Figure 3.1 shows the diagram of the programmed B6 circuit. Modelling the circuit was done by inputting its network list consisting of junctions and the elements between them. Indices (numbers or letter sequences) were assigned to the junctions present in the circuit diagram.

The net list for the circuit in Fig. 3.1 is shown in Listing 3.1.

```
Netzwerk
*
        netz = DRNETZ       (r , s , t  / (Us, f, PHIN, RNETZ, LNETZ, IL0N )
        V1   = DI           ( r,  1 / ZV01, VD1, RD1, RSP1, LD1, LSP1, TS1)
        V2   = DI           ( 2,  r / ZV02, VD1, RD1, RSP1, LD1, LSP1, TS1)
        V3   = DI           ( s,  1 / ZV03, VD1, RD1, RSP1, LD1, LSP1, TS1)
        V4   = DI           ( 2,  s / ZV04, VD1, RD1, RSP1, LD1, LSP1, TS1)
        V5   = DI           ( t,  1 / ZV05, VD1, RD1, RSP1, LD1, LSP1, TS1)
        V6   = DI           ( 2,  t / ZV06, VD1, RD1, RSP1, LD1, LSP1, TS1)
        RL   = R            ( 1, 0 / RLAST)
        IL   = L            ( 0, 2 / IL0, LLAST)
*
END
```

Listing 3.1

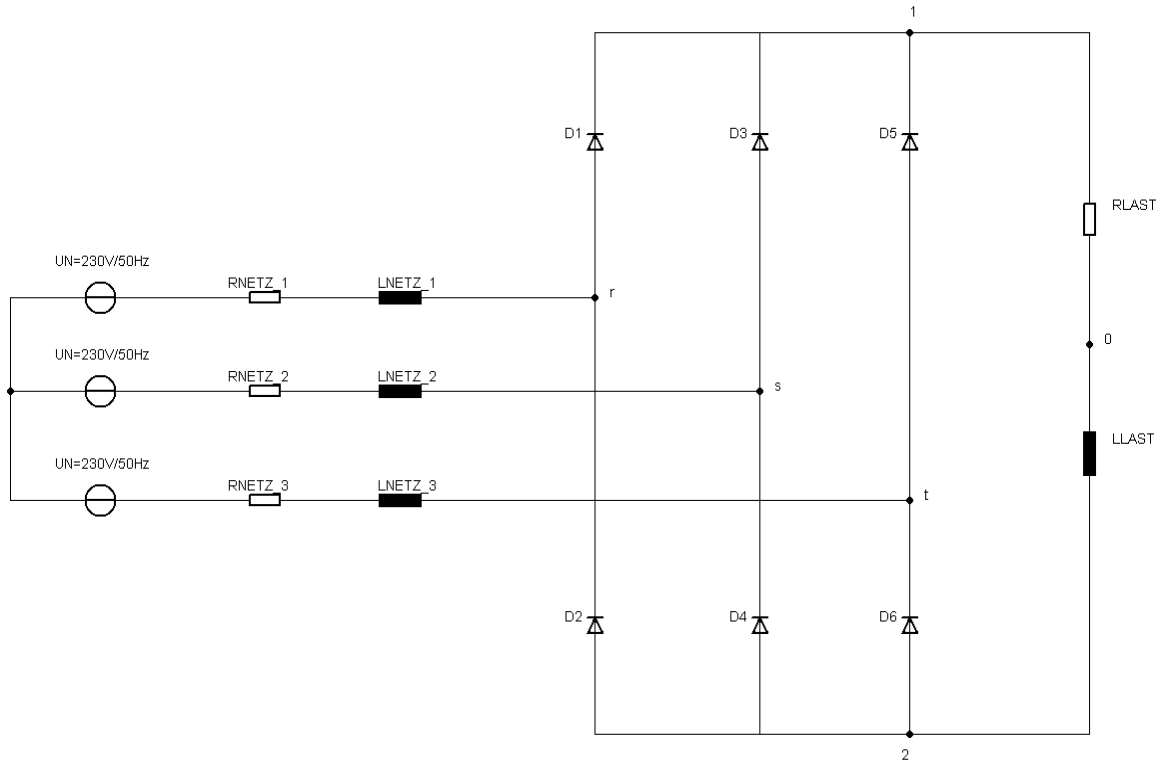

Fig 3.1: Diagram of the programmed B6 bridge

The component DRNETZ symbolises one of the macros in Listing 3.1. It supplies the mains voltage and frequency, and the two elements R_{NETZ} and L_{NETZ}. The elements PHIN and IL0N are defined on the top part of the program as an array with three values. These values symbolise with their position within the array, the phases L1, L2, and L3 (referred to as R, S, and T in the program, an old notation scheme). The value PHIN represents the phase shift of the voltage U_1 with respect to time t=0.

The element IL0N represents the default value of the current. The program requires this default value in conjunction with inductances and capacities. The default value, however, does not have to correspond to the actual value. The right setting of the element IL0N reduces the computation time needed at the beginning of a simulation. In most cases, defaulting to zero is sufficient to achieve this. No further instructions were coded in the model, except for the assigning of exit values such as the states, currents, and voltages of the semiconductor components. After the code was successfully compiled, the plot-function was used to produce a graphical plot of the exit values (Figs. 3.2 and 3.3).

Figure 3.2 shows the plot of the two values I_{NETZ} and U_{NETZ}. Both were assigned to the first phase of the three-phased system. The result also shows that the three-phased

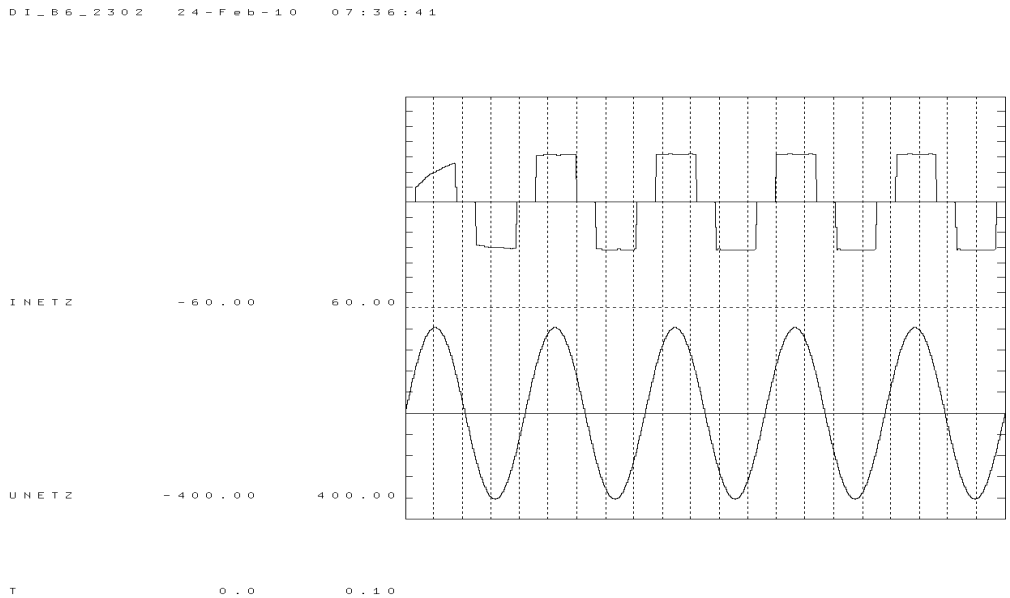

Fig. 3.2: The line current (I_{NETZ}) and mains voltage (U_{NETZ}) of the first circuit

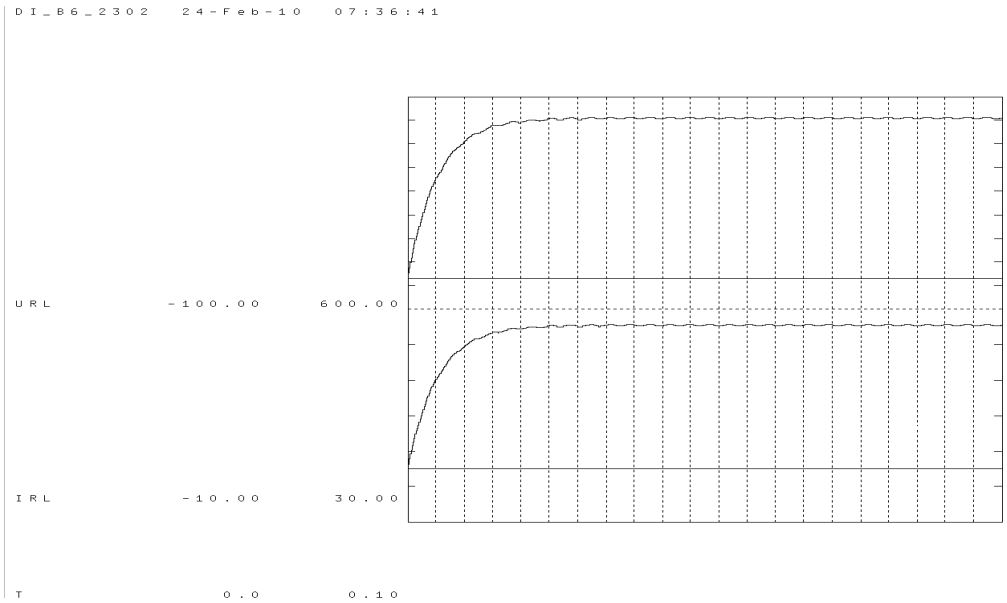

Fig. 3.3: The load voltage (U_{RL}) and the load current (I_{RL})

system did not deviate from the expected 120 degrees phase shift. The current corresponds with the theoretical behaviour of a typical B6 bridge. This current with a block-like shape lasting for 120 degrees, is characteristic for a B6-rectifier and will be detectable in the line current of the F3E later.

There were no deviations with the load values of both voltage and current (Fig. 3.3). This finding validates the assumptions made when the model was developed. There were also no significant problems encountered in the macro used as a model for the three-phased supply grid. Thus, the macro was selected as the basis of the supply network for future models.

An alternative approach requiring three separate phases involved a much higher effort, and was therefore, rejected.

3.1.2 Extension of the model to the F3E

To convert the model of the B6 rectifier into a model of an F3E, appropriate modifications were done. First, the input filter of the F3E was added. This consists of three capacitors in delta configuration in front of the F3E. The single-phased version is shown in Fig. 3.4.

The values of the filter elements of this topology were obtained from Siemens and computed as follows:

$C_{F3E} = 20\mu F$
$R_{CREIHE} = 330m\Omega$
$R_{CPAR} = 20k\Omega$

The extended circuit diagram is shown in Fig. 3.5. The legends of the filter components were omitted to provide a better overview of the diagram. (The legends can be seen in Fig. 3.4.)

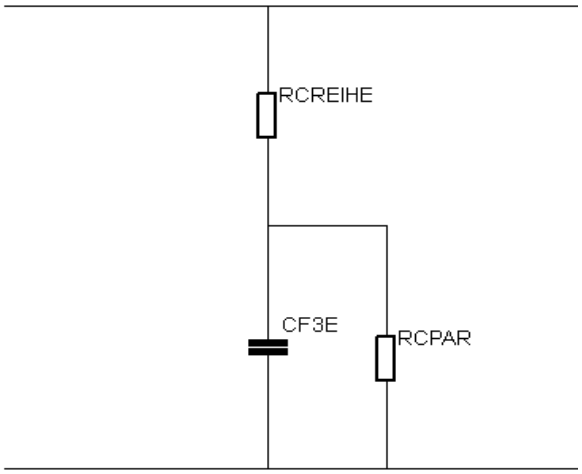

Fig. 3.4: Diagram of a single-phased input filter

Figure 3.6 shows that the shape of the mains voltage (U_{NETZ}) did not change in comparison with the first circuit shown in Fig. 3.2. The form of the line current, however, changed substantially. The former rectangular shape of the current was superimposed by fading oscillations. The resonance frequency of these oscillations were determined by the elements L_{NETZ} and C_{F3E}, and dampened by the resistors. The oscillations were induced with each state change of the respective diodes. Lowering the inductance of the net by one magnitude, resulted in the plot shown in Fig. 3.7.

The oscillations disappeared with a reduced L_{NETZ} (Fig. 3.7). It would also be possible to reduce C_{F3E}, though for the time being, it has to be regarded as a fixed value.

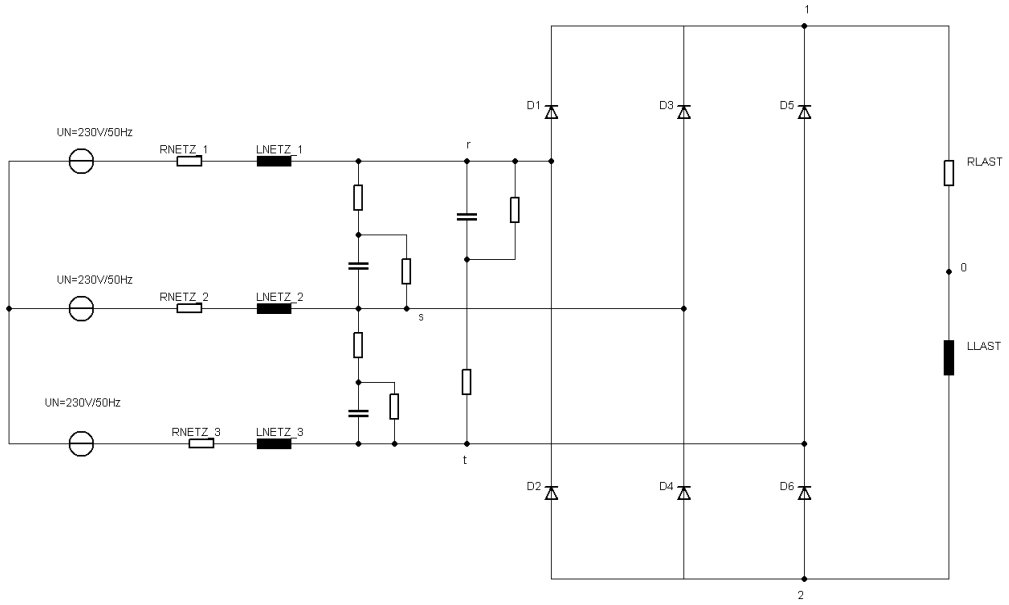

Fig. 3.5: The B6 rectifier with the implemented F3E filter

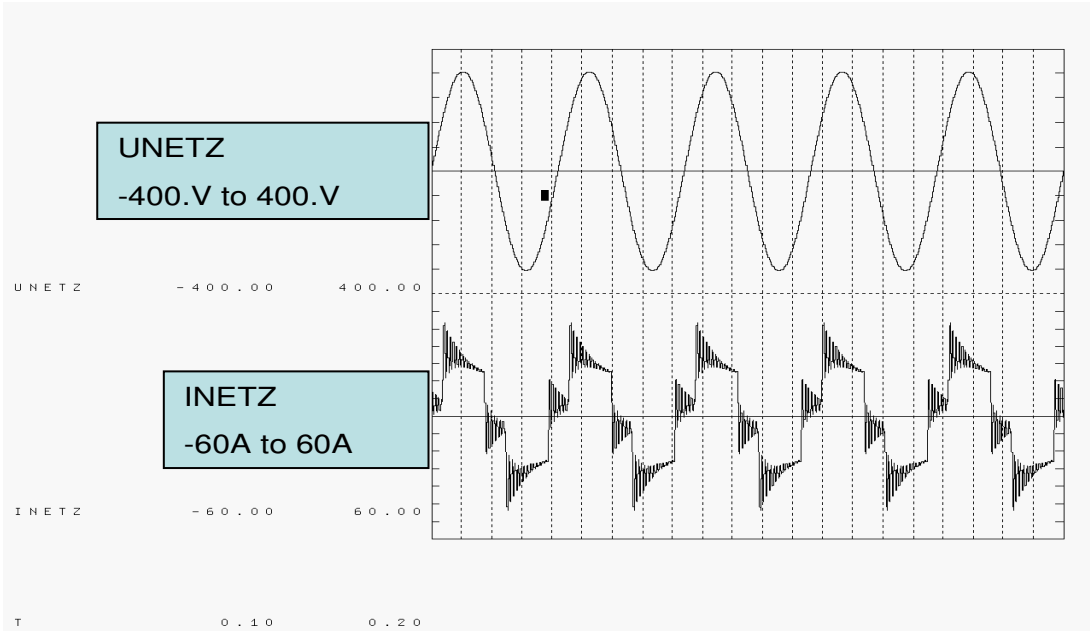

Fig. 3.6: The mains voltage (U_{NETZ}) and line current (I_{NETZ}) of the extended circuit

The next extension of the circuit represents the introduction of the diodes anti-parallel configuration to the semiconductor. The diodes were removed from the net list and replaced by GPV macro contained in the components library (Listing 3.2). This consists of two anti-parallel semiconductors. The use of two individual elements was avoided for programming reasons.

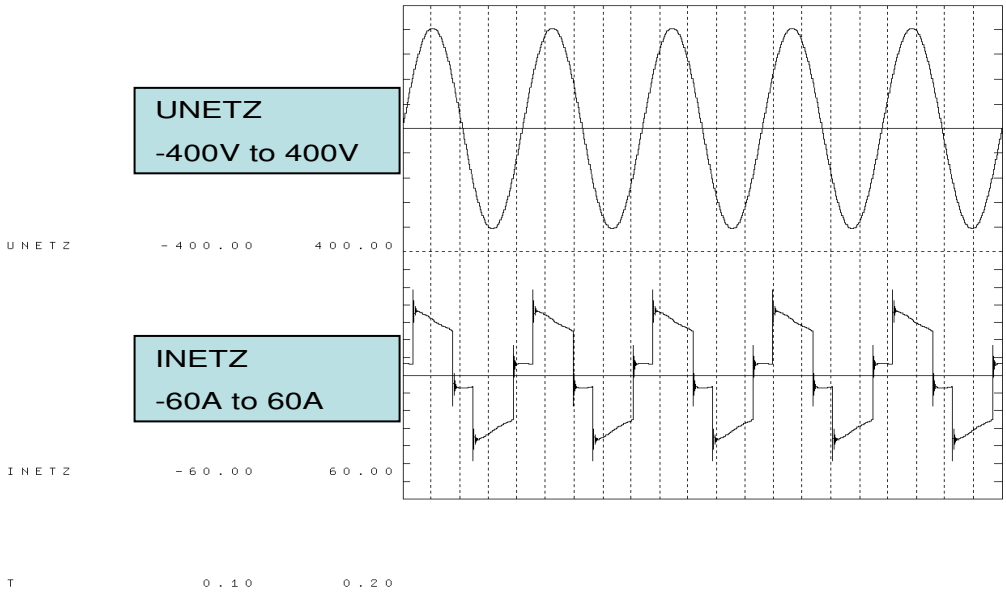

Fig 3.7: The mains voltage (U_{NETZ}) and line current (I_{NETZ}) with a reduced L_{NETZ}

V = GPV	(K1, K2 / ZV0, **VD**, RD, RSP, LD, LSP, TS, **S1, S2**)
V = GPV	(K1, K2 / ZV0, **VV**, RD, RSP, LD, LSP, TS, **SEIN, 1.**)

Listing 3.2

The macro consisted of two anti-parallel thyristors at the start of the programming (Fig. 3.8). These were modified into the desired elements by appropriate entries into the arrays and by subsequent programming. In this case, T2 was assigned the functionality of a diode by replacing the variable S2 with the constant 1. By introducing the variable SEIN, a GTO instruction in the ASIM-part, T1 was turned into a semiconductor, which can be switched off (Listing 3.2). The GTO instruction was then assigned the variable VV (Listing 3.3).

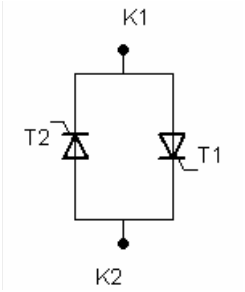

Fig. 3.8: Network lists entry for a GPV macro and alternate circuit diagram

```
VV = GTO (IV, ZV, SEIN, SAB, ANS, VMAX, VD)
```
Listing 3.3

In this programming instruction, the parameters necessary for generating a semiconductor, which can be switched-off, were transferred to the GPV macro. The two variables SEIN and SAB control the switching-on or -off of the semiconductor. As such, the initial focus was on the underlying control method of the semiconductor macro (the complete variable list with short explanation of their meaning can be found in Appendix II). The state value SEIN was then generated. The control principle is quite simple. Whenever the corresponding diode is in the conductive state, SEIN has to provide a power-on signal. It is possible within the simulator to assess the state of a diode through the state variable ZF. It indicates whether the semiconductor is in the conductive state (1) or not (0). It is not possible, however, to determine the switching status since the two semiconductors of the GPV macros share one control variable for the switching status ZF. The ZF can take three values, in this case: 1, 0, and -1. The condition -1 represents the anti-parallel switched semiconductor, the diode. If the switch on signal SEIN would alter from 0 to -1 while ZF is set to -1, the now switched-on thyristor T1 would take over the current, and ZF would then change to 1. The switching-on condition would not be valid and T1 would again be switched-off. This would lead to an increased switching frequency, which does not occur in reality. In order to eliminate incorrect results due to the erroneously switching behaviour of the F3E, a control method based on the actual control algorithm of the equipment was developed.

In order to avoid confusion with models that were developed later, the switching semiconductors T1 to T6 were re-named F1 to F6 (Fig 3.9). As mentioned earlier, T1 (now re-named F1), has to be switched-on, if the diode D1 is in a conductive state. Under normal conditions, this is identical to the B6 circuit. With this circuit, the diode with the highest anode voltage and the lowest cathode voltage of the three phase voltages is always in a conductive state. The modelling of the control algorithm requires that a switching rule be provided first, which later forms the basis of the programmed control algorithm.

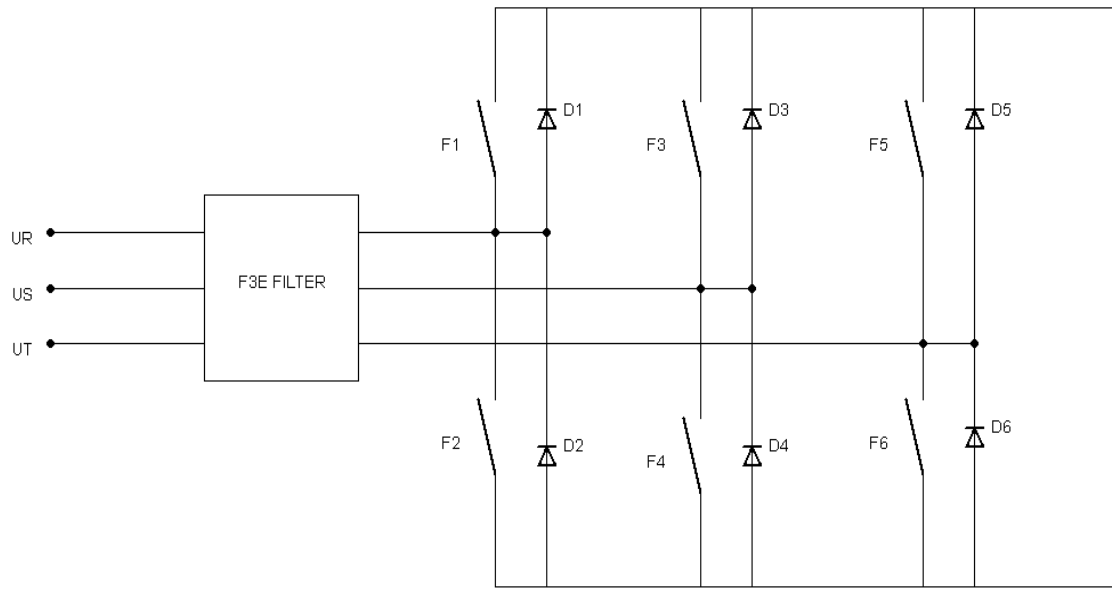

Fig. 3.9: The F3E circuit

In order to determine the switching rule, it is important to know the semiconductor configuration. In Fig. 3.9, some simplifications were incorporated into the F3E circuit diagram. The controllable semiconductors were depicted as ideal switches and the input filter is shown as a block diagram. The switches (F1 to F6) correspond to the designations of the GPV macros used later in the program code. The diodes were designated as D1 to D6 to determine the switching rule. These designations were not needed later in the program code.

The corresponding switch F may only be switched on if the associated diode D is in a conductive state. Since the circuit without the diodes functions like a simple B6 rectifier, only the switching characteristics of the diodes were copied.

The following basic rule applies for switches F1 to F6. Fn may switch (change its state), if its phase voltage is higher than the other two positive phase voltages or lower than the other two negative phase voltages. In this regard, the rules for the individual switches are:

If *UR>US & UR>UT then F1 = 1*
If *US>UR & US>UT then F3 = 1*
If *UT>US & UT>UR then F5 = 1*

If *UR<US & UR<UT then F2 = 1*

If *US<UR & US<UT then F4 = 1*

If UT<US & UT<UR then F6 = 1

The first attempt in implementing the control represented a simple IF instruction. The switching times and the minimum switch-on times of the semiconductors contained within the GPV macro were ignored. A problem was posed by the switch-off signal SAB; it ignored the fact that controllable semiconductors require a falling edge for switching-off. As an initial solution, the semiconductor was subjected to a continuous impulse. The falling edge of the switch-off signal could only occur when re-starting the semiconductor since the switch-off signal SAB of the semiconductor switch F was set to 0. Hence, the IF instruction was rejected. With the switching rules mentioned earlier, a new approach was devised. The switching rules were incorporated as Boolean operations in the program and their exit values were assigned to a variable in each case (Listing 3.4).

```
MSF1 = BOOL((UR0.GT.US0).AND.(UR0.GT.UT0))
MSF3 = BOOL((US0.GT.UR0).AND.(US0.GT.UT0))
MSF5 = BOOL((UT0.GT.US0).AND.(UT0.GT.UR0))
MSF2 = BOOL((UR0.LT.US0).AND.(UR0.LT.UT0))
MSF4 = BOOL((US0.LT.UR0).AND.(US0.LT.UT0))
MSF6 = BOOL((UT0.LT.UR0).AND.(UT0.LT.US0))
```

Listing 3.4

To incorporate a dead time and cancel any algebraic loops, which could develop, the following block was added (Listing 3.5):

```
MSFA1 = LZMIN (0, MSF1)
MSFA3 = LZMIN (0, MSF3)
MSFA5 = LZMIN (0, MSF5)
MSFA2 = LZMIN (0, MSF2)
MSFA4 = LZMIN (0, MSF4)
MSFA6 = LZMIN (0, MSF6)
```

Listing 3.5

The component LZMIN always assigns as its exit value the input value of the previous computation interval. The output values of the components MSFA 1 to 6 were used to generate the switch-on signals for thyristors 1 to 6 and SEIN 1 to 6, respectively. The

switch-on signals were generated with an IF-statement; however, this IF-statement generated only the switch-on signals. The switch-off signals were made available in this version as needle pulses in the following program section (Listing 3.6):

```
SAB1 = NUSIP (0, BOOL(-SEIN1))
SAB2 = NUSIP (0, BOOL(-SEIN2))
SAB3 = NUSIP (0, BOOL(-SEIN3))
SAB4 = NUSIP (0, BOOL(-SEIN4))
SAB5 = NUSIP (0, BOOL(-SEIN5))
SAB6 = NUSIP (0, BOOL(-SEIN6))
```

Listing 3.6

The component NUSIP produced a needle pulse with each positive zero crossover of the input value. The switch-on signals changed during the switching-off from 1 to 0; thus, they are indicated here in a negated state. The needle pulse provided with its falling edge, which occurred in the next calculation step, a safe switching off of the semiconductor.

The first few simulations with the control using an R-L-load provided satisfactory results. Nevertheless, more errors occurred on the next extension of the circuit. This extension consisted of adding a small intermediate circuit capacitor and substituting the R-L-load for a current source capable of inverting the direction of energy flow. Errors occurred mainly due to an insufficiently small delay time. Thus, an additional delay using the VZ1 program module was created to remedy this problem. After its insertion into the program, no further errors occurred in the first few simulations. The PT1 component used, however, had a crucial and very marked disadvantage. Its exit value increased exponentially. In relation to the other transient processes, it reached its stationary value after a long time. Attempts to correct this, such as decreasing the response time and elevating the output value to the desired range by means of a threshold-operated switch failed. Therefore, in order to produce the delay time, a monoflop was inserted into the ASIM part of the program. This was taken from an existing simulation model of a single-phased AFE, which was used in an earlier study by Ganz (1994). The coding of the model was modified for its application in the F3E model (Listing 3.7). The original program was designed for a single-phased system and provided only four semiconductor delay times. Since these were operated in push-pull

mode, only two separate timers were implemented. In the F3E model, each semiconductor was provided with its own timer.

```
PROCEDURAL

*   Set Timer
   IF(MOF3E1.GT.0.)THEN
        FB1 = T
   ENDIF
*   Check of the requirements
   IF(FB1.LE.(TA+HS/2.))THEN
        FMONO1 = 0.
   ELSEIF(T.GT.(FB1+TAU))THEN
        FMONO1 = 0.
   ELSEIF(T.GE.FB1)THEN
        FMONO1 = 1.
   ELSE
        FMONO1 = 0.
   ENDIF

END
```

Listing 3.7

The program section in Listing 3.7 represents the timer for the semiconductor F1 (Fig. 3.10). The variable MOF3E1 was again generated as needle pulse. The input value was provided by the well-known variable MSFA1. Depending on which conditions were fulfilled, the value 0 or 1 was assigned to the newly introduced variable FMONO1. To generate the switch-on signal, the two variables FMONO and MSFA were linked by the Boolean AND operation (Listing 3.8).

```
SEIF1=BOOL((MSFA1)*(-FMONO1))
SEIF2=BOOL((MSFA2)*(-FMONO2))
SEIF3=BOOL((MSFA3)*(-FMONO3))
SEIF4=BOOL((MSFA4)*(-FMONO4))
SEIF5=BOOL((MSFA5)*(-FMONO5))
SEIF6=BOOL((MSFA6)*(-FMONO6))
```

Listing 3.8

The operand * transformed the BOOL instruction within the operation into a logical AND.

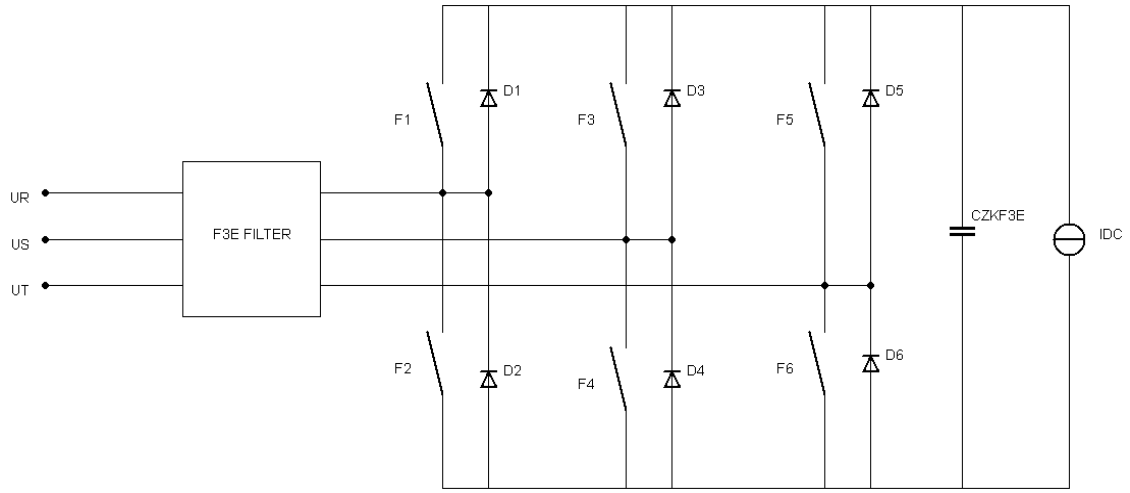

Fig. 3.10: Extended circuit with a DC current source and a small intermediate circuit capacitor

This modified control also enabled the feedback operation of the F3E, as shown in Fig. 3.11. The DC supply, therefore, modified its output current according to a ramp function from +40A to -40A within a pre-determined time.

3.2 The PCI model

The next step in the development of the desired universal model is the design of the PCI model. To do this, it was necessary to find a suitable control algorithm. The possible algorithms that can be used include:

- PWM with sine under-shoot algorithm;
- Space vector modulation; and
- Bang-bang control.

The Bang-bang control is the simplest of the three algorithms; however, it does not produce a defined switching spectrum. Moreover, it switches on the basic momentary values. Thus, it has only limited importance to the PCI control. The second algorithm, the space vector modulation, is often used in conjunction with electrical drives. Its disadvantage is the disproportionately higher implementation effort compared with the other two procedures. Therefore, the PWM with sine under-shoot algorithm was chosen as the most suitable approach. It supplies a firm harmonic spectrum, is relatively simple

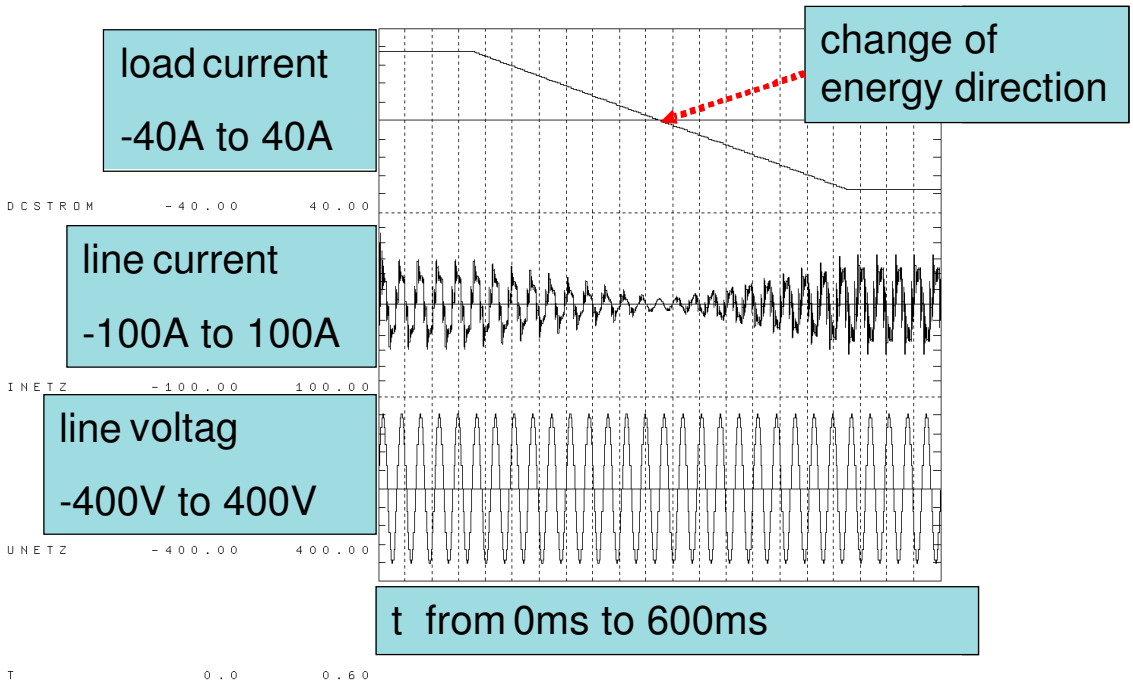

Fig. 3.11: Shape of line current (I_{NETZ}), mains voltage (U_{NETZ}), and the adjusted direct current (DCSTROM)

to handle, and except for the space vector modulation, is the most frequently used control algorithm.

3.2.1 Generation of the PWM signal

This section focuses on the implementation and programming aspects of the PWM. To generate a PWM signal, a delta voltage and a reference value for the output signal, a sinusoidal voltage in this case, are compared with each other. First, the delta carrier was programmed. Its momentary value was calculated according to the linear equation $y = m \cdot x \pm b$. The value x was provided by the current simulation time t. It should be noted that the upward gradient m and the shift constant b must assume different values for the generation of the rising and falling slope triangle function (Fig. 3.12).

With x=0, the upward gradient is m = +2 and b = -10. The gradient turned downwards as the value of y reached a maximum of 10. The values -2 and +10 were assigned to m and b, respectively. This condition remained up to the point x=15. At this point, a permutation of the two values took place again.

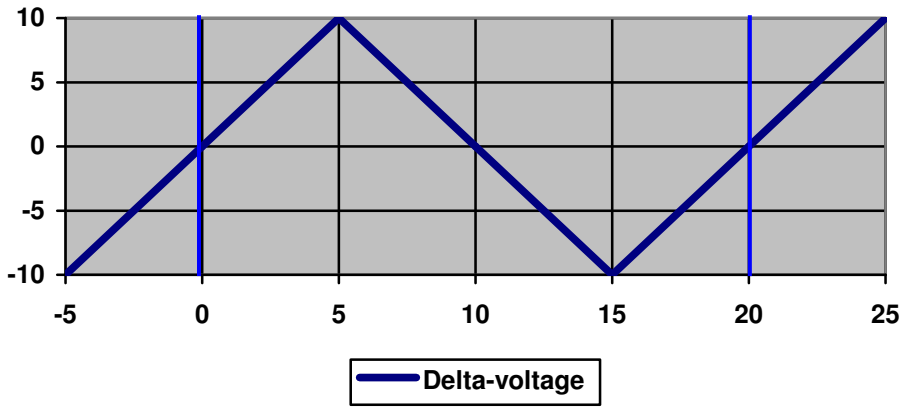

Fig. 3.12: Schematic representation of a triangle signal

The program was implemented according to Listing 3.9. The variable DR represents the upward gradient function.

```
DR = VH*DRSTEIG*(T-TX)+VS*DRDACH
```

Listing 3.9

```
IF (DR .GE. DRDACH) THEN
        TX=T
        VH=-1.
        VS=+1.
ELSEIF (DR .LE. (-DRDACH)) THEN
        TX=T
        VH=+1.
        VS=-1.
ENDIF
```

Listing 3.10

In order to implement the change in slope, an IF-statement was attached to Listing 3.9. The variables VH and VS served only to ensure the sign change of the two parameters m and b. The time of the sign change is always assigned to the variable TX, assuring that the function repeats itself in the same way (Listing 3.10).

The variable DRSTEIG contained in the upward gradient was earlier computed. The constant DRDACH, the amplitude, the variable DRFREQ, and the triangular voltage frequency were used to calculate the variable DRSTEIG (Listing 3.11).

```
DRSTEIG= DRDACH * DRFREQ * 4
```
Listing 3.11

The frequency DRFREQ represents the number of repetitions per second or the reciprocal value of the cycle time. Thus, a factor of 4 is required; otherwise, the function would reach its maximum value only at the end of the cycle. This would correspond to the cycle time increasing by a factor of four.

The sinusoidal threshold voltage UST1 was calculated according to Eq 3.8.

$$U_{ST1}(t) = \hat{U} \cdot \sin(\omega \cdot t + \varphi_B) \qquad \text{Eq. 3.8}$$

The amplitude of the threshold voltage should not be higher than the amplitude of the triangular voltage. This condition can be avoided by multiplying the amplitude of the reference voltage with the relative magnitude (variable AUSST in Listing 3.12).

```
SINDACH = AUSST * DRDACH
UST1 = SINDACH*SIN(OMEGA*T + BPHI0 )
UST2 = SINDACH*SIN(OMEGA*T + BPHI0 - BPHI3 )
UST3 = SINDACH*SIN(OMEGA*T + BPHI0 - 2.*BPHI3 )
```
Listing 3.12

```
DIF1 = UST1 - DR
DIF2 = UST2 - DR
DIF3 = UST3 - DR
```
Listing 3.13

The differences between the delta voltage and the three desired relative magnitudes were calculated (Listing 3.13). These were further processed by the threshold switch component TRI. As a result, the component provided the values 1 (upper exit value) or -1 (lower exit value) for the semiconductor switches operated later through the Bang-bang control. Additionally, the component required an upper and a lower saltus, which

were assigned a value of -0.01 for the lower one, and a value of +0.01 for the upper one. The component needed a start value since it would enter an indefinite state at the beginning of a simulation cycle. An initial value of -1 was assigned to the component (Listing 3.14).

```
STS1 = TRI ( -1., -0.01, +0.01, -1., +1., DIF1 )
STS2 = TRI ( -1., -0.01, +0.01, -1., +1., DIF2 )
STS3 = TRI ( -1., -0.01, +0.01, -1., +1., DIF3 )
```

Listing 3.14

The output variables STS1 to STS3 supplied the PWM signals for the respective phases. The result of this simulation is shown in Fig. 3.13.

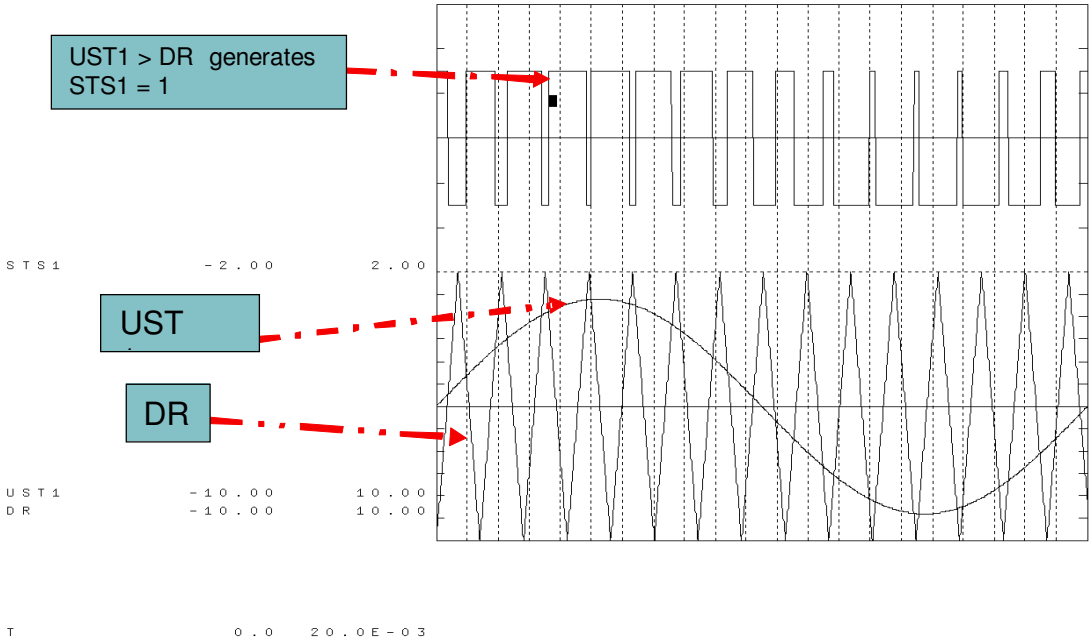

Fig. 3.13: Triangular voltage DR, the reference value UST1, and the resulting values for STS1

Figure 3.13 also shows the correct function of the programmed PWM. Whenever the sinusoidal voltage UST1 exceeded the delta voltage DR, the signal STS1 assumed the logical state of “1”; otherwise it assumed the logical state of “0”.

3.2.2 Model of the PCI circuit

The modelling of the PCI circuit re-applied the GPV macro previously used in the F3E. One of the two thyristors was again converted into a fully controllable semiconductor, and the other was used as a diode. A DC voltage source was used as an energy source, and a series connection of a resistor R and an inductor L, similar to the F3E draft model, was used as load (Fig. 3.14).

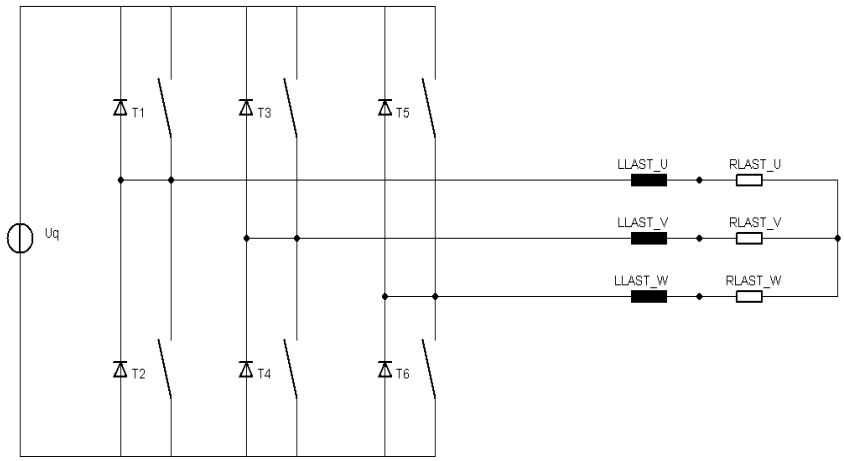

Fig. 3.14: Alternate circuit diagram of the programmed circuit

3.2.3 Modification of the programmed PWM

The previous sections introduced the PWM algorithm necessary to operate the PCI model, and its subsequent incorporation into the model. In addition, the variables STS1 to STS3 were linked with the switch-on variable (SEIP1 to 6) and the switch-off variables (SAP1 to 6). Because of the Bang-bang operation mode of the semiconductors, a dead time was needed. The monoflop used for the control of the F3E was re-used to prevent the short circuiting of the voltage source by the semiconductors. Except for the used variables, the instructions for assigning the switch-on and -off signals were identical to those used with the F3E. The simulation results illustrated the expected current and voltage shapes (Figs 3.15 and 3.16).

The shapes of the voltage and current of the resistor R_{LAST_U} (Fig. 3.15) were dominated

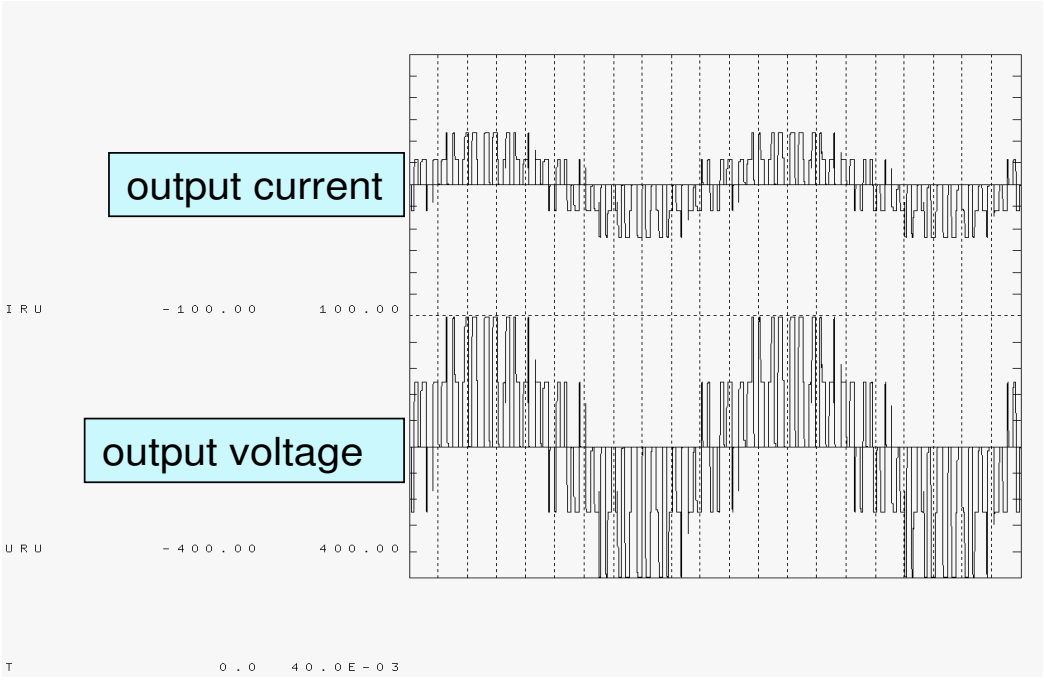

Fig. 3.15: Current and voltage shapes of the PCI model with a small load inductor L_{LAST}

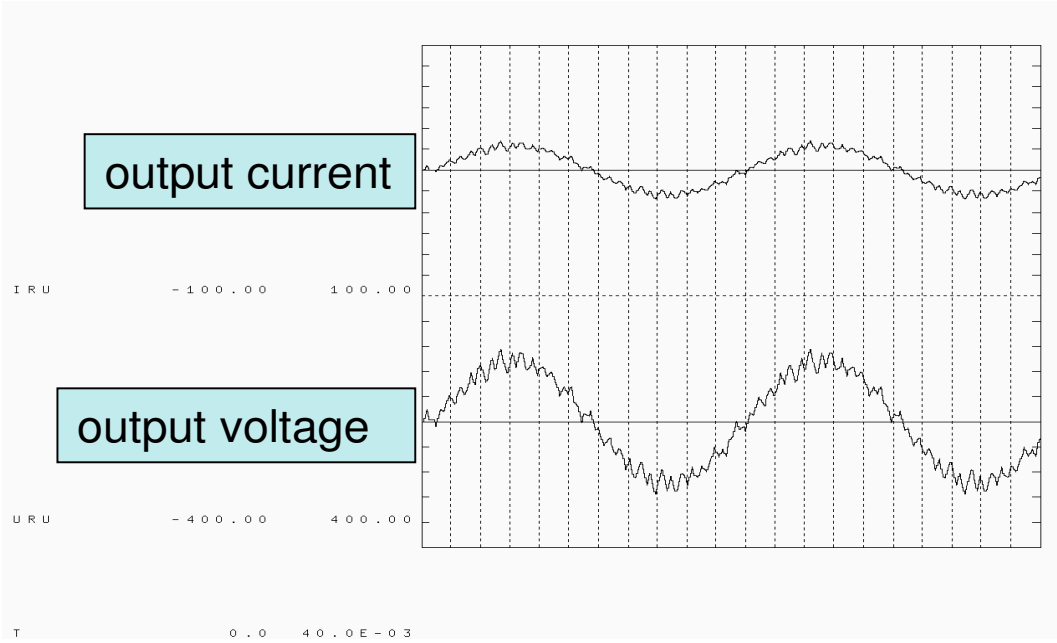

Fig. 3.16: Current and voltage shapes of the PCI model with a large load inductor L_{LAST}

by the pulse patterns of PCI. The influence of the inductor on the load current was negligible since the value of the inductor was small. With a significantly larger inductor, the shape of the load current was almost sinusoidal (Fig. 3.16) and exhibited only a very slight ripple because of the pulsing patterns of the PCI.

3.3 Combination of the F3E and the PCI models

In order to merge the two models into one, the PCI model was inserted into the F3E model (Fig. 3.17). The elements of the PCI model extended the network list of the F3E model. It is important that the current source serving as load to the F3E and the voltage source of the PCI model are removed. Both sources served in the basic models only as substitutes for the other model, and with the combination of the two models, were rendered redundant.

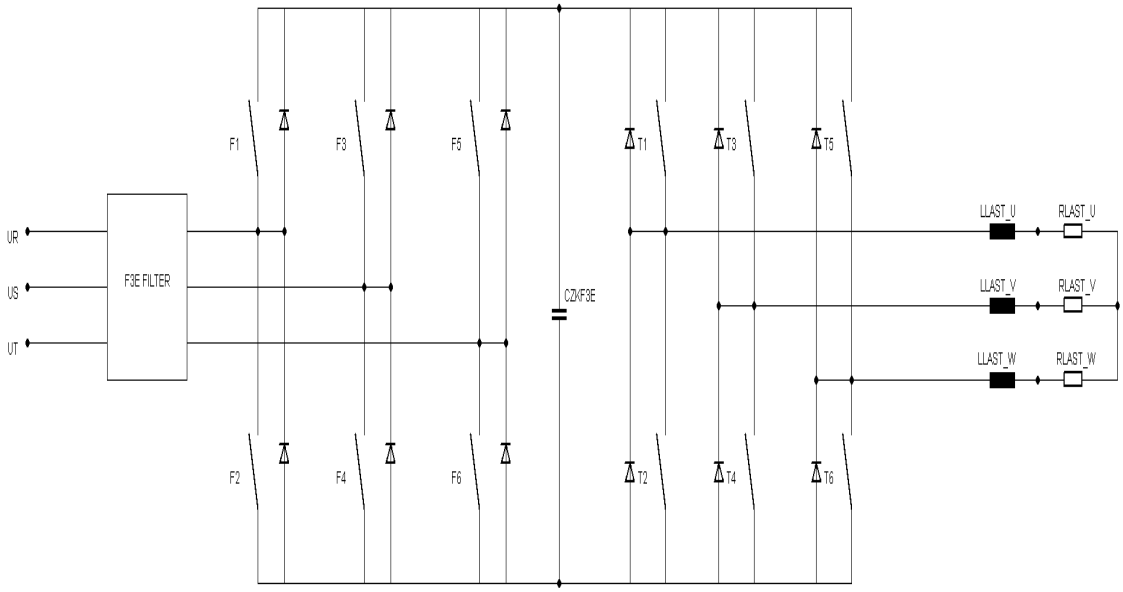

Fig. 3.17: The alternate circuit diagram without supply grid resulting from the new net-list

Subsequently, the controlling circuit of the PCI was inserted into the ASIM part of the unified model, and checked for identical name variables to avoid possible programming errors. During the test runs of the simulation model, errors occurred leading to short-circuits as indicated by the red dashed lines in Fig. 3.18. To trace errors easily, two shunts were introduced at the interface point between the F3E and PCI models (Fig. 3.19). The resistors were inserted to identify errors by depicting the energy flow.

Errors in the unified model occurred mainly due to the idealisation of the load and supply voltage of the two basic models. In the unified model, the two circuits were exposed to currents and voltage shapes, not present in the basic models. Contrary to the

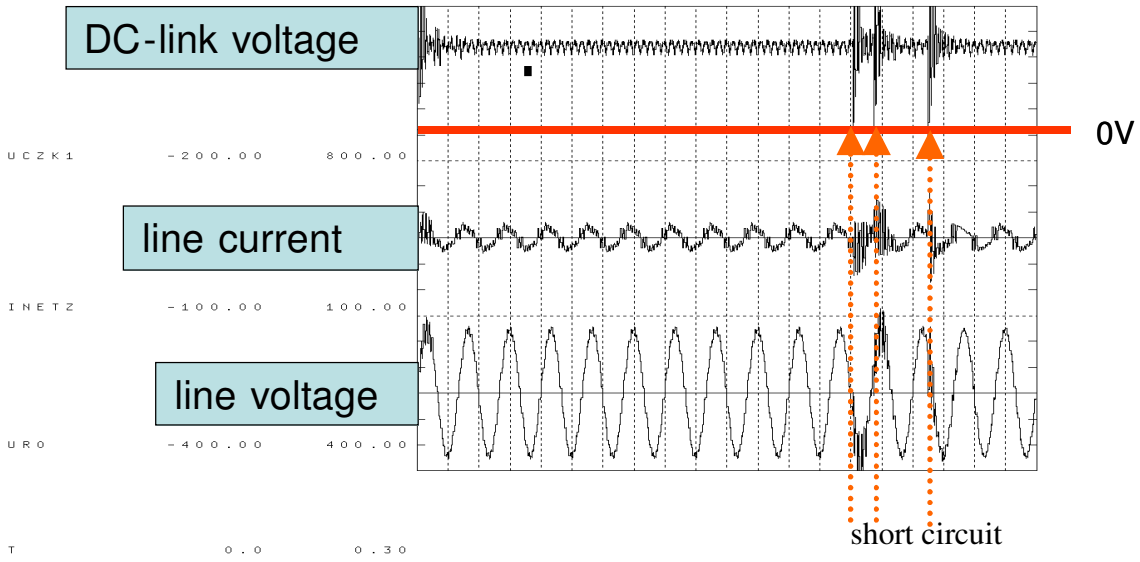

Fig. 3.18: The line current, mains voltage, and intermediate circuit voltage with error

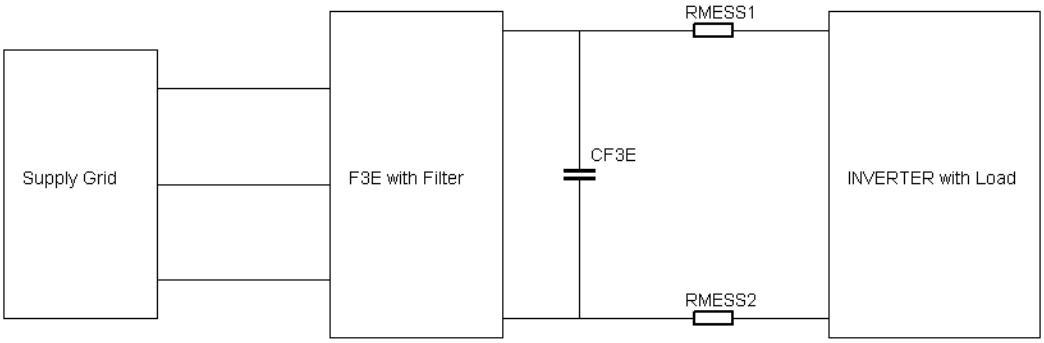

Fig. 3.19: Placement of the shunts in the model

standard circuit topologies, only a small intermediate capacitor was used between the F3E and PCI models. Usually, the intermediate capacitor decouples the input from the output circuits. This, however, was not the case in this configuration. Thus, the pulse pattern of the PWM was visible in the supply current. This led to increased ripples in the input voltage of the model and caused the generation of erroneous switching pulses, especially during periods of commutation. These pulses were slightly longer in duration than the implemented delay times.

Since all semiconductors contained within the NETASIM-library possess a switching time, they remained switched on, even though the switch-on signal is no longer present.

The needle pulse necessary for switching off would not be able to switch-off the semiconductor once it has been generated within the switching time. The element, then, would not be able to recall the impulse as soon as the switching time elapsed. The semiconductor remains switch-on. Thus, short-circuit is inevitable. This constraint was prevented by introducing a minimal switching-on time for semiconductors. This is equal to the quadruple value of the switching time of the semiconductors, and is triggered whenever a semiconductor in the previous calculation step changed from the non-conductive to the conductive state (ZF10 changes from 0 to 1, Listing 3.15).

```
ZF10  = LZMIN(0, ZF1)
F3F1 = NUSIP (0, BOOL(ZF10))
```

Listing 3.15

The procedure used for timers was identical to that of the monoflop (Listing 3.16).

```
PROCEDURAL
        IF(F3F1.GT.0.)THEN
                FEIN1 = T
        ENDIF
        IF(T.LE.(FEIN1+PTAU))THEN
                MINF1 = 1.
        ELSE
                MINF1 = 0.
        ENDIF
END
```

Listing 3.16

The following switch-on instruction in Listing 3.16 incorporated this change by including the variable MINF1.

```
SEIF1=BOOL(((MSFA1)*(-FMONO1))+(MINF1))
```

Listing 3.17

The OR operand ensures that SEIF1 = 1 as long as MINF1 = 1, or the AND operation results in a logical ‘1’ (Listing 3.17). This measure, however, was not reliable under all conditions. Thus, two additional blocking measures were implemented. The first measure involved a direct blocking of the semiconductors of one phase against each

other. The state of the alternate semiconductor in the previous simulation step (ZF10 to 60) was used and incorporated into the AND operator of SEIF (1 to 6) (Listing 3.18).

```
ZF10  = LZMIN(0, ZF1)

SEIF10=BOOL((MSFA1)*(-ZF20)*(-FMONO1))

SEIF1= BOOL((SEIF10)+(MINF1))
```

Listing 3.18

The second measure involved incorporating an additional blocking time to prevent an early switching-on during commutation. The procedure is similar to the one used in implementing a minimum switch-on time, except that it is triggered on the switching status of the alternate diode. In order to dissolve the algebraic loop, the value of the last calculation step was used. The exit of the timer (MINDF1 to 6) was again linked with the instruction for switching-on (Listing 3.19). The instruction for switching-on was divided into two operations to make it clearer.

```
SEIF10=BOOL((MSFA1)*(-ZF20)*(-FMONO1)*(-MINDF2))
SEIF20=BOOL((MSFA2)*(-ZF10)*(-FMONO2)*(-MINDF1))
SEIF30=BOOL((MSFA3)*(-ZF40)*(-FMONO3)*(-MINDF4))
SEIF40=BOOL((MSFA4)*(-ZF30)*(-FMONO4)*(-MINDF3))
SEIF50=BOOL((MSFA5)*(-ZF60)*(-FMONO5)*(-MINDF6))
SEIF60=BOOL((MSFA6)*(-ZF50)*(-FMONO6)*(-MINDF5))


SEIF1= BOOL((SEIF10)+(MINF1))
SEIF2= BOOL((SEIF20)+(MINF2))
SEIF3= BOOL((SEIF30)+(MINF3))
SEIF4= BOOL((SEIF40)+(MINF4))
SEIF5= BOOL((SEIF50)+(MINF5))
SEIF6= BOOL((SEIF60)+(MINF6))
```

Listing 3.19

The programming of the pulse inverter control was also revised. The minimum switch-on time of the F3E control and the state evaluations of the alternate diode to trigger the blocking mechanism were integrated (Listing 3.20). The switchable components were already secured by the signal generation in the Bang-bang operation against simultaneous switching-on.

```
STS10  = LZMIN(0, STS1)
STS20  = LZMIN(0, STS2)
STS30  = LZMIN(0, STS3)
*
*
PVER1 = LZMIN(0, SEIP10)
PVER2 = LZMIN(0, SEIP20)
PVER3 = LZMIN(0, SEIP30)
PVER4 = LZMIN(0, SEIP40)
PVER5 = LZMIN(0, SEIP50)
PVER6 = LZMIN(0, SEIP60)
*
*
SEIP10 = BOOL((-PMONO1)*(STS1)*(STS10)*(-PVER2)*(-MIND2))
SEIP20 = BOOL((-PMONO2)*(-STS1)*(-STS10)*(-PVER1)*(-MIND1))
SEIP30 = BOOL((-PMONO3)*(STS2)*(STS20)*(-PVER4)*(-MIND4))
SEIP40 = BOOL((-PMONO4)*(-STS2)*(-STS20)*(-PVER3)*(-MIND3))
SEIP50 = BOOL((-PMONO5)*(STS3)*(STS30)*(-PVER6)*(-MIND6))
SEIP60 = BOOL((-PMONO6)*(-STS3)*(-STS30)*(-PVER5)*(-MIND5))
*
SEIP1 = BOOL((SEIP10)+(MINT1))
SEIP2 = BOOL((SEIP20)+(MINT2))
SEIP3 = BOOL((SEIP30)+(MINT3))
SEIP4 = BOOL((SEIP40)+(MINT4))
SEIP5 = BOOL((SEIP50)+(MINT5))
SEIP6 = BOOL((SEIP60)+(MINT6))
```

Listing 3.20

With the variables STSx0, an additional delay of the switch-on signal was produced. The variable PVERx generated a blocking with the switch-on signal SEIPx0* from the last calculation step (LZMIN), similar to the one used in generating ZF01 in Listing 3.18. The model test runs succeeded without further errors and the individual signals showed the expected shapes (Fig. 3.20).

3.4 Optimisation of the load behaviour

The three-phased load of the pulse inverter has been treated so far as a simplified series connection of a resistor R and an inductor L. In future studies, it should be possible to simulate power feedback operations. As such, the load model has to be modified; while still minimising the simulation time.

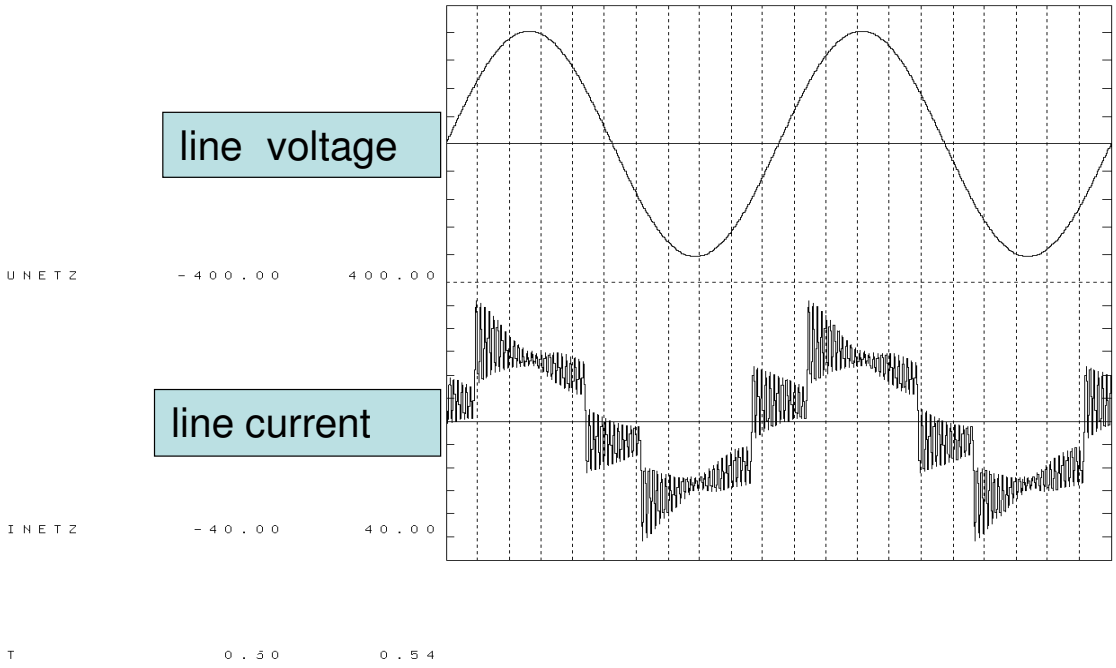

Fig. 3.20: Shapes of line current and voltage after consolidation of the control

The first attempt in expanding the functionality of the model consisted of supplementing the R-L-circuit with a current source. With this approach, the load current can be manipulated directly. This approach, however, was rejected because NETASIM stopped compiling the simulator routine. It also prevented the serial connection of a current source and an inductance, as well as the parallel connection of a voltage source and a capacitor for stability reasons.

An induced electromotive force (EMF) was incorporated into the model to invert the energy flow. To accomplish this, a controlled AC voltage source was utilised. Using voltage vectors, the voltage amplitude was computed as a function of the load current, rotor resistance RA, and inductance LA (Fig 3.21).

Using half of the intermediate circuit voltage and the relative magnitude of the inverter, the output voltage UPWR of the PCI was calculated. By subtracting the voltage URMOT from UPWR, the first vector (UPWID) was formed (Fig. 3.22). The second vector was obtained with the help of the voltage of the reactance (ULMOT). With the

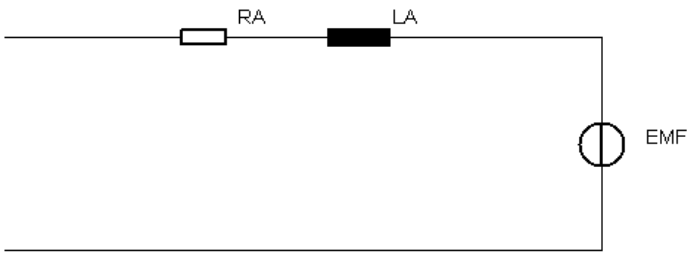

Fig. 3.21: One-phased representation of an alternate circuit diagram of the motor

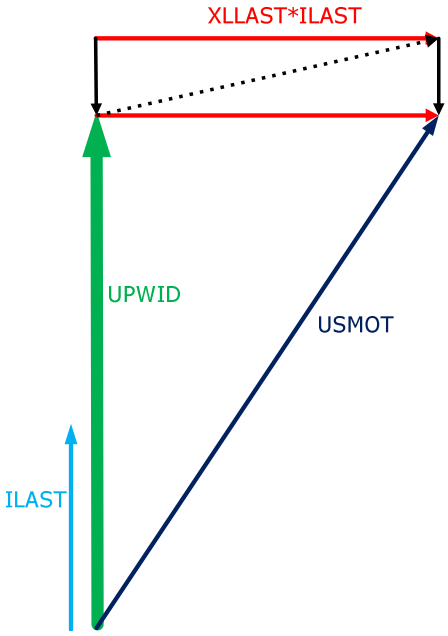

Fig 3.22: Voltage vector diagram based on the calculations in Listing 3.21

two values of ULMOT and UPWID, one of the values of the amplitude (USMOT) and the phase position (PFR) for the counter voltage were calculated (Listing 3.21)

```
UPWR      = AUSST  * (UCZK1/2)
URMOT     = ILAST * RLAST
UPWID     = UPWR   - URMOT
ULMOT     = ILAST * (2*PI*SINFREQ*LLAST)
USMOT     = SQRT((UPWID**2)+(ULMOT**2))
PFR       = ASIN((ULMOT/ USMOT))
```

Listing 3.21

The motor can be modelled as a symmetrical system. As such, it is possible to apply the calculated EMF voltage to the three phases of the motor. With this adjustment, the old entries in the network list for the three-phased load were removed and replaced by the well-known DRNETZ macro, which constitutes a symmetrical load, and reduces programming effort and the needed computing power. Figure 3.23 presents the resulting alternate circuit diagram for the three-phased load of the PCI.

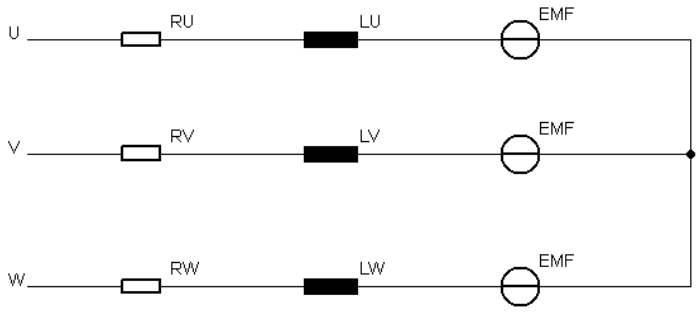

Fig. 3.23: Three-phased alternate circuit diagram of the load model

The model F3E with PCI and the three-phased load is now complete and can be used. Subsequently, the model was examined in stand-alone operation; hence it was named F3E_PWR to differentiate it from the other models.

Figure 3.24 shows the new load model working properly as indicated by the shape of the output voltage. The pulse form of the PWM could be seen between the two conductors U and V. The output current has a sinusoidal waveform.

3.5 The AFE model

The AFE was represented by its own unique model at the start of the study. In so doing, elements already existing were used. For example, the network list of the basic F3E model was re-used almost completely. Only the filter capacitors had to be replaced by line reactors (Fig. 3.25 and Listing 3.22).

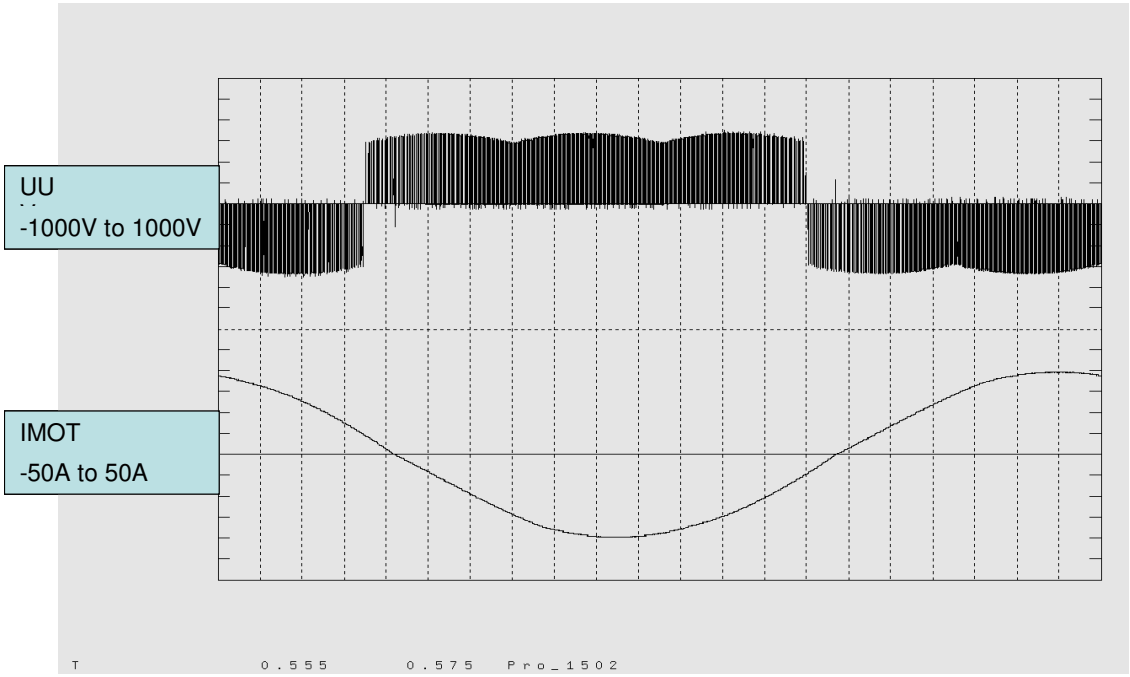

Fig. 3.24: Output waveforms of the PCI with the new load

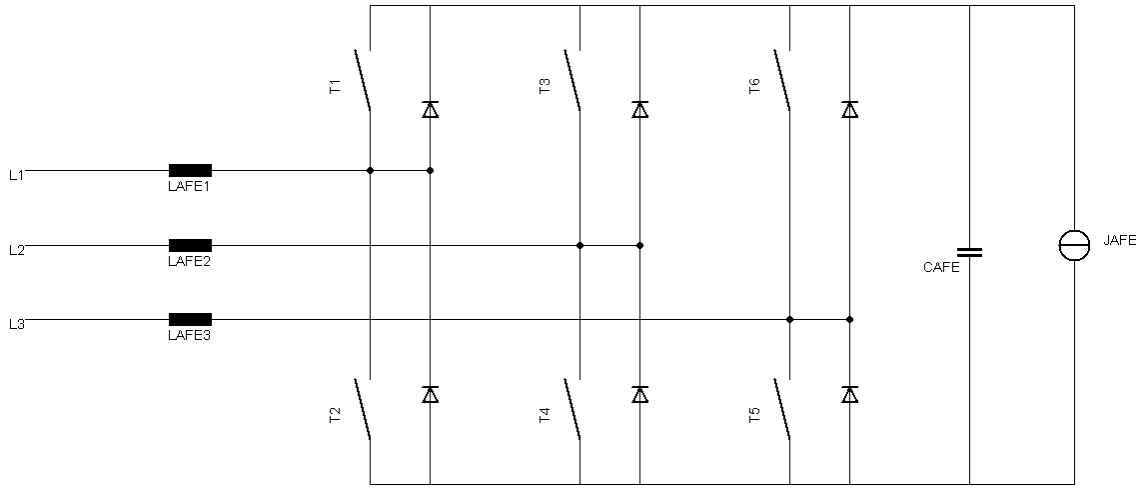

Fig. 3.25: Alternate circuit diagram of the AFE circuit with line reactors LAFE1 to 3

The control of the AFE was essentially derived from an already existing control model programmed by Ganz (1994). It uses the PWM as control method similar to the pulse inverter model.

The program section for the delta carrier was adapted from the PCI model. Only the variable names were modified as a precautionary measure. The computation of the desired value differed, however, from that of the pulse inverter model and is described as follows:

```
netz = DRNETZ       (r, s, t / x )
LAF1   = L          ( r,201  / x)
LAF2   = L          ( s,202  / x)
LAF3   = L          ( t,203  / x)
AF1    = GPV ( 204,201 / x )
AF2    = GPV ( 201,205 / x )
AF3    = GPV ( 204,202 / x )
AF4    = GPV ( 202,205 / x )
AF5    = GPV ( 204,203 / x )
AF6    = GPV ( 203,205 / x )
CAFE   = C          ( 204,205 / x )
JAFE   = J          ( 205,204 / x)
```

```
netz = DRNETZ     (r, s, t / x )
CRS  = C          (9, s /x)
CTR  = C          (11, r / x )
CST  = C          (10, t / x )
RV1  = R          (r, 9 / x )
RV2  = R          (t, 11 / x )
RV3  = R          (s, 10 / x )
RP1  = R          (9, s / x )
RP2  = R          (11, r / x )
RP3  = R          (10, t / x )
F1   = GPV        (7, r / x )
F2   = GPV        (r, 8 / x )
F3   = GPV        (7, s / x )
F4   = GPV        (s, 8 / x )
F5   = GPV        (7, t / x )
F6   = GPV        (t, 8 / x)
CZK  = C          (7, 8 / x )
IDCQ = J          (7, 8 / x)
```

Listing 3.22

```
UEIN = UR0
USOLLA = ABS(UEIN)
```

Listing 3.23

The momentary value of the mains voltage UR0 (supply voltage of the DRNETZ macro) was imported and converted with the component ABS into their absolute value (Listing 3.23).

```
UDACH = 0.5*PI*VZ1(PT1, VERZ, USOLLA)
```

Listing 3.24

This absolute value was then filtered with the delay element PT1 and multiplied with the factor $0.5 \cdot \pi$ to adjust the value according to the maximum value of the voltage delta (Listing 3.24).

```
USOLLB1 = UDACH*SIN(2*PI*f*T+ALPHA)
USOLLB2 = UDACH*SIN(2*PI*f*T+ALPHA-ALPHA3)
USOLLB3 = UDACH*SIN(2*PI*f*T+ALPHA-2*ALPHA3)
```
Listing 3.25

The proper values for phase and frequency were derived from the three line voltages (Listing 3.25). These rated values provided the first vector of the voltage triangle.

```
STROM1 = KP*(USOLL-UCAFE)+KI*INT(0,(USOLL-UCAFE))
```
Listing 3.26

The PI controller calculated the rated value of the current STROM1 using the balance of the rated and the actual value of the intermediate circuit voltage (Listing 3.26) .

```
ISOLLB1 = STROM1*COS(2*PI*f*T+ALPHA)
ISOLLB2 = STROM1*COS(2*PI*f*T+ALPHA-ALPHA3)
ISOLLB3 = STROM1*COS(2*PI*f*T++ALPHA-2*ALPHA3)
```
Listing 3.27

The actual value was then multiplied with a cosine function to achieve the 90 degree phase shift between inductor voltage and current (Listing 3.27). This was necessary because the program cannot perform a complex calculation (multiplication with j) directly. With the values ISOLLB1-3, the rated voltage of the inductor was finally calculated, providing the second vector of the voltage triangle (Listing 3.28).

```
UL1SOLL = 2*PI*f*LAFE*ISOLLB1
UL2SOLL = 2*PI*f*LAFE*ISOLLB2
UL3SOLL = 2*PI*f*LAFE*ISOLLB3
```
Listing 3.28

To compare the rated value of the balance between these two vectors with the triangular carrier, the rated value was multiplied with the factor KPWM (Listing 3.29). This factor is the ratio of the delta voltage amplitude and the actual value of the intermediate circuit voltage.

```
KPWM = (2*SPITZE)/UCAFE
UPWM1 = KPWM*(USOLLB1- UL1SOLL)
UPWM2 = KPWM*(USOLLB2- UL2SOLL)
UPWM3 = KPWM*(USOLLB3- UL3SOLL)
```

Listing 3.29

The PWM of the AFE works properly as illustrated in Fig. 3.26. The sinusoidal voltage UPWM1 together with the delta voltage AFDR generate the PWM signal AREG1. The rest of the control algorithm is identical to that of the pulse inverter. Only new variables names were assigned to prevent an erroneous double use of values.

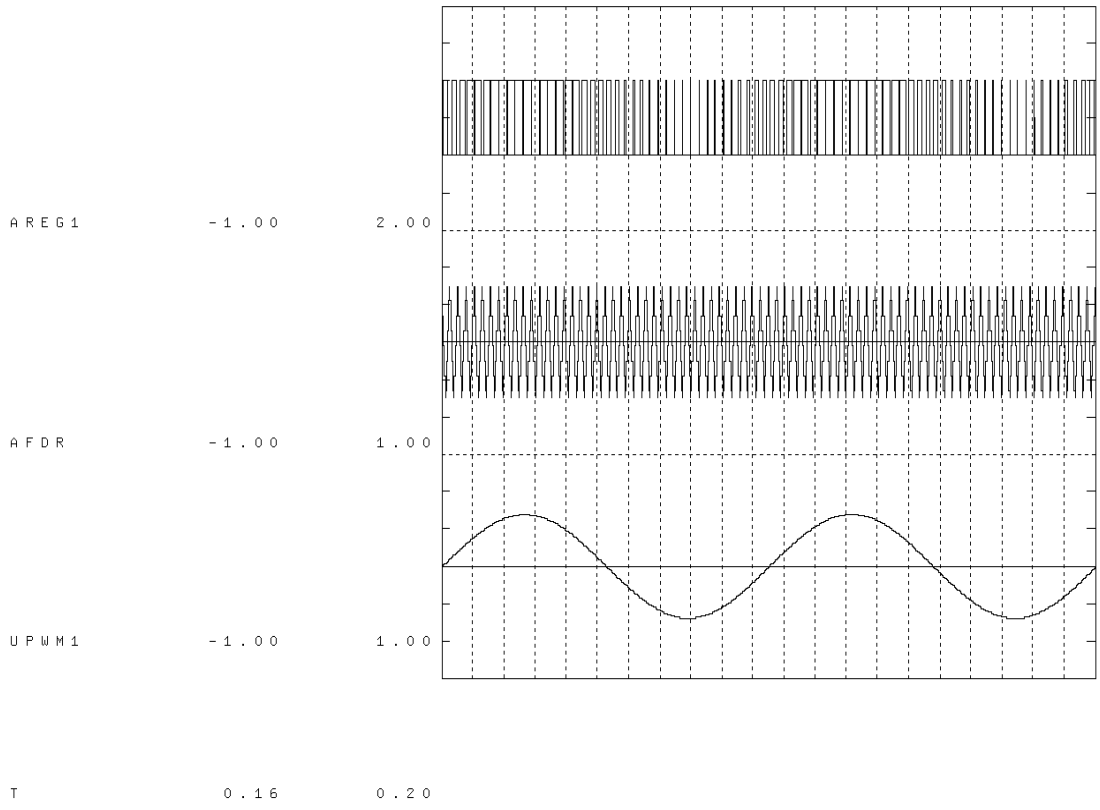

Fig. 3.26: Shapes of the UPWM1, the AFDR, and the PWM signal AREG1

3.5.1 Testing the model functionalities

To determine the functionality of the model, all controller parameters were initially taken from the single-phased model. They were tested by trial and error to ensure that the AFE model will not require an excessive amount of time reaching the stationary or post transient state.

A control unit producing oscillating values significantly influenced the mains current of the AFE and the complete model, including the F3E. During the test-phase, the following values for the parameters K_p and K_I were found to be reliable and used for the simulations:

$$K_p = 0.5$$
$$K_I = 200$$

With this set-up, it is possible for the controller to maintain the reference value of the intermediate circuit voltage (Fig. 3.27).

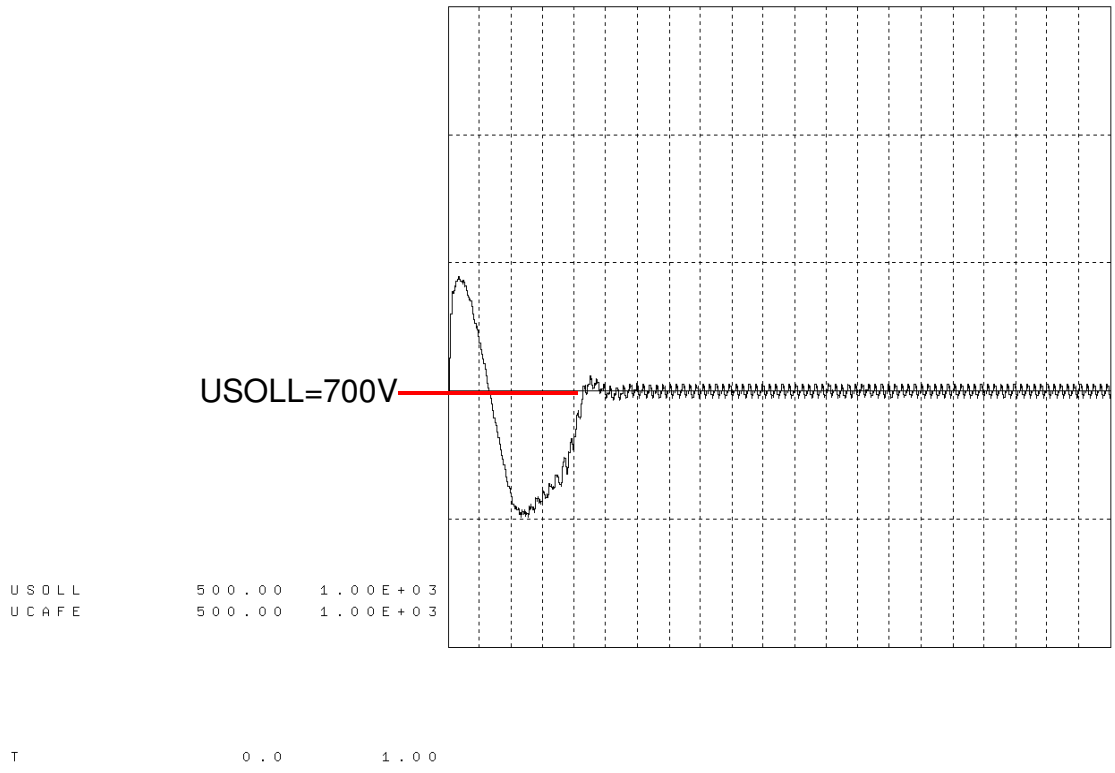

Fig. 3.27: Shape of the intermediate voltage using the parameter values of K_p and K_I

This model is also capable of reversing the energy flow, if needed, and operate as a generator. This reverse operation is shown in Fig. 3.28. During the generator-operation, the direction of the current reversed and the intermediate voltage slightly increased.

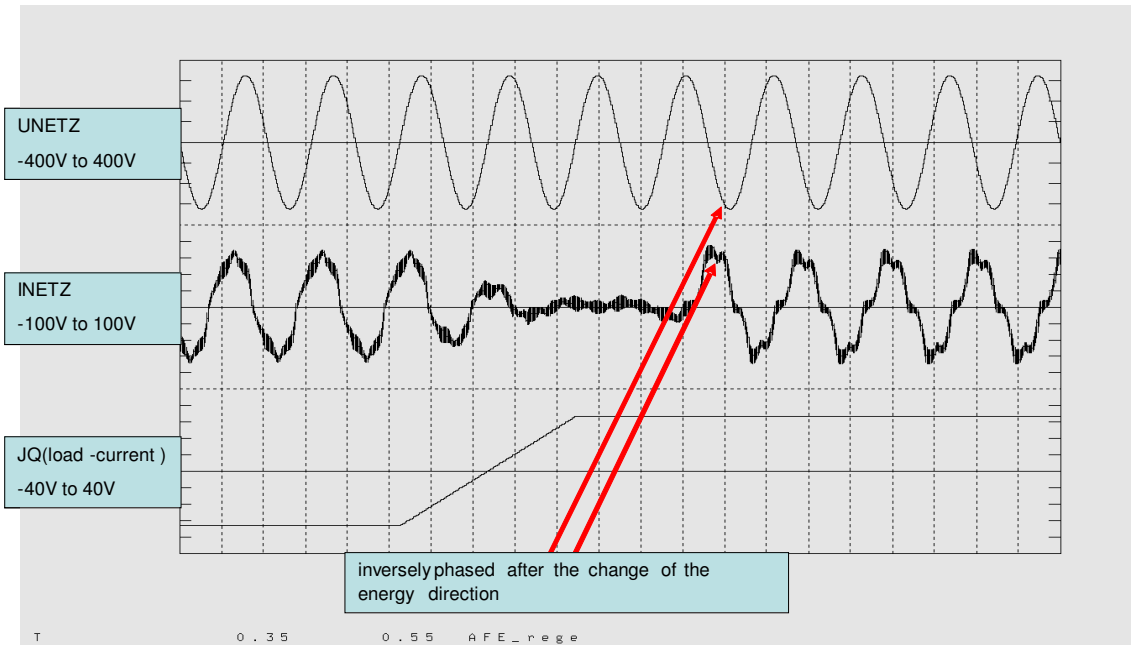

Fig. 3.28: Change from motor operation to generator operation of the AFE

The AFE model is operational, and produces current and voltage shapes close to reality.

3.6 Mains model used

In all the models developed, the power supply system has always been modelled using the simulator build-in macro DRNETZ. It provides the mains voltages not only with a phase shift of 120 degrees but also a line impedance consisting of a resistor R and an inductor L. The macro, therefore, provides a solid base for simulating the single sub-models of the input topologies. Additionally, these examinations were limited to the low voltage 230/400V 50Hz power grid. This limitation of the examined area makes it feasible to omit the line capacitors ordinarily present in the alternate circuit diagram of the power grid. They are very small and therefore, exert very little influence on the behaviour of the grid. Due to this simplification, it was not necessary to include line capacitors in the mains model provided by the DRNETZ macro. A simplified model of the mains grid based on these assumptions is shown in Fig. 3.29.

This grid representation is sufficient to examine the F3E. It is possible though, to encounter problems while examining the F3E and AFE connected to the same grid. The rated power of the AFE exceeds that of the F3E by one magnitude. It can, therefore, be

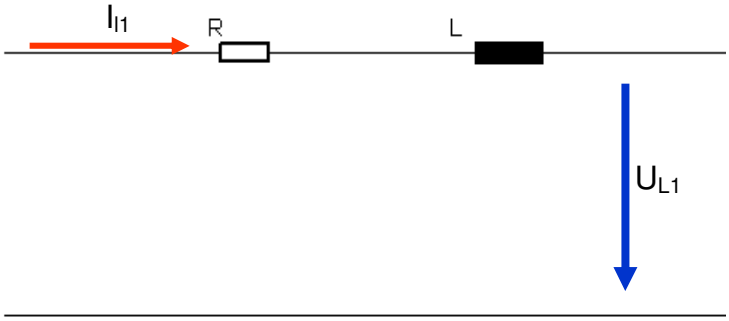

Fig. 3.29: Simplified alternate circuit diagram of a power supply line

concluded that the impedance of the power line should not be too large; otherwise, the current of the AFE would produce a large voltage drop over the impedances. A power grid rated for the AFE looks like a very robust net to the F3E. Hence, the configuration shown in Fig. 3.30 cannot be used in the examinations undertaken in this study.

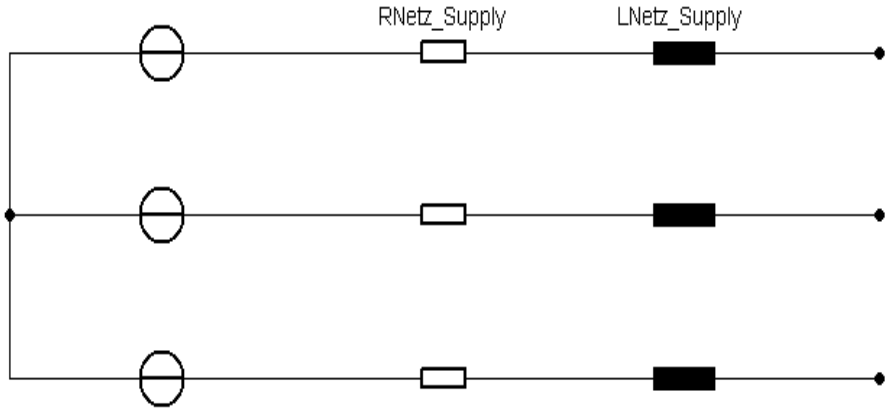

Fig. 3.30: Simple mains model

To avoid this limitation, an additional impedance consisting of a resistor and an inductor was introduced to the right of the access point of the AFE. The resulting mains model is shown in Fig. 3.31. With this configuration, it is possible to operate the F3E connected to a power grid designed for its rated power without limiting the rated power of the AFE.

A further advantage of this configuration is the possibility of configuring each of the two mains parts differently. For example, it would be possible to provide the AFE with

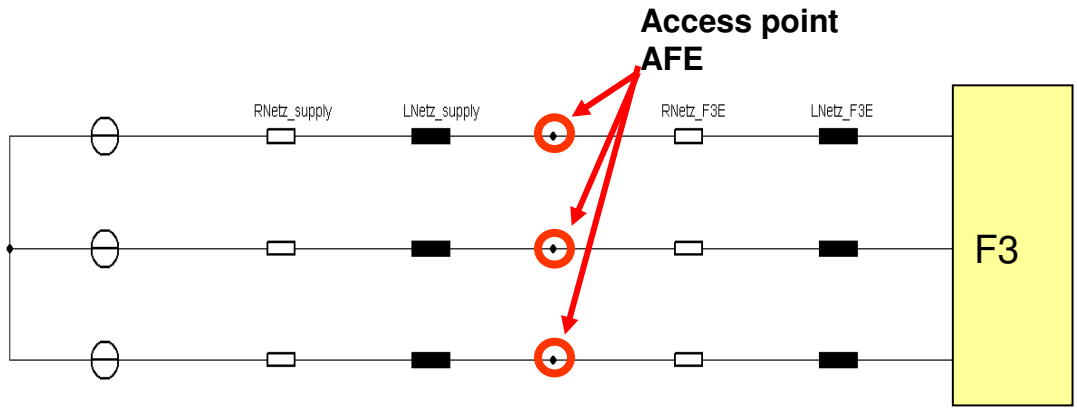

Fig. 3.31: Expanded mains configuration

a very rigid power grid; while still exposing the F3E to a grid with relatively high impedances.

4 Research implementation

4.1 Aspects of the research

The research is divided into two independent aspects. The first part contains the investigations of the model and the circuit; whereas, the second part examines the grid feedbacks of the model developed and evaluates the factors influencing the model in conjunction with AFE.

4.1.1 Investigation of the F3E_PWR model

The F3E_PWR model is used to examine the feedbacks of the frequency-inverter to the supply network. It was mentioned in Chapter 2.4 that power electronic circuits often result to non-sinusoidal currents on the supply side.

During the development of the F3E model, it was observed that the current ripple in most cases strongly depends on the properties of the network. This model did not include the pulse controlled inverter (PCI), which was added afterwards. The PCI, however, created additional feedbacks passed on to the supply network because of its small intermediate capacitor. These feedbacks originated from the switching actions performed by the inverter.

Despite the input filter preventing the majority of the harmonics caused by the PWM to enter the grid, a small part still affected the line current. This effect was illustrated in the simulation study conducted under laboratory conditions. Figure 4.1 shows the three line-currents of the power-supply line I_{NETZ} of the F3E filter I_{CRS}, as well as the unfiltered F3E current. It should be noted that the filter was designed in a delta configuration. The current I_{CRS} flows in a branch of the filter between phases L1 and L2. The F3E current consists of the sections of the intermediate circuit current of the PCI. The intermediate circuit current is a series of approximately rectangular blocks. The width of the blocks is determined by the switching frequency of the PCI and demonstrated in the temporal resolution in Fig. 4.1.

The simulation results were submitted to an FFT analysis. In order to provide a better

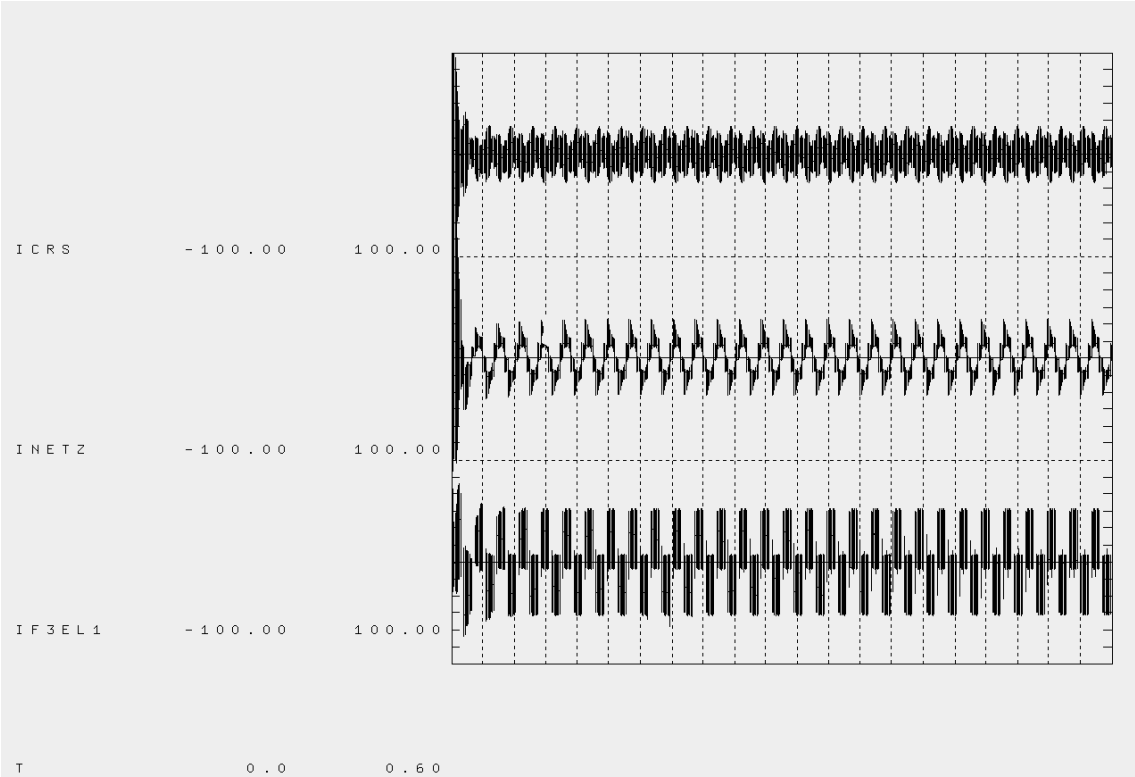

Fig. 4.1: Three line-currents of the power-supply line I_{NETZ} of the F3E filter, I_{CRS}, and I_{F3EL1}

overview, only the components with considerable amplitude, and not the whole spectrum, were represented.

Figure 4.2 shows that hardly any higher harmonics content was present in the lower frequency range in the filter circuit, except for the 50Hz fundamental frequency current with an amplitude of about 15A. The harmonics contained in this range enter the supply network unfiltered. Figure 4.3 presents a cut-out range from about 15 to 17kHz. This range contains the switching frequency of the attached pulse inverter. The harmonics of the F3E current were large and originated from the intermediate circuit current of the PCI, which were handed through towards the supply side by the F3E nearly unmodified. A majority of these harmonics was filtered, representing a significantly smaller filter impedance in this frequency range as compared with that of the supply network.

Nevertheless, it is necessary to determine the consequences of the switching frequency of the pulse inverter being in the same range as the resulting resonant frequency of the supply network and filter components. First, the resonance frequency of the F3E_PWR

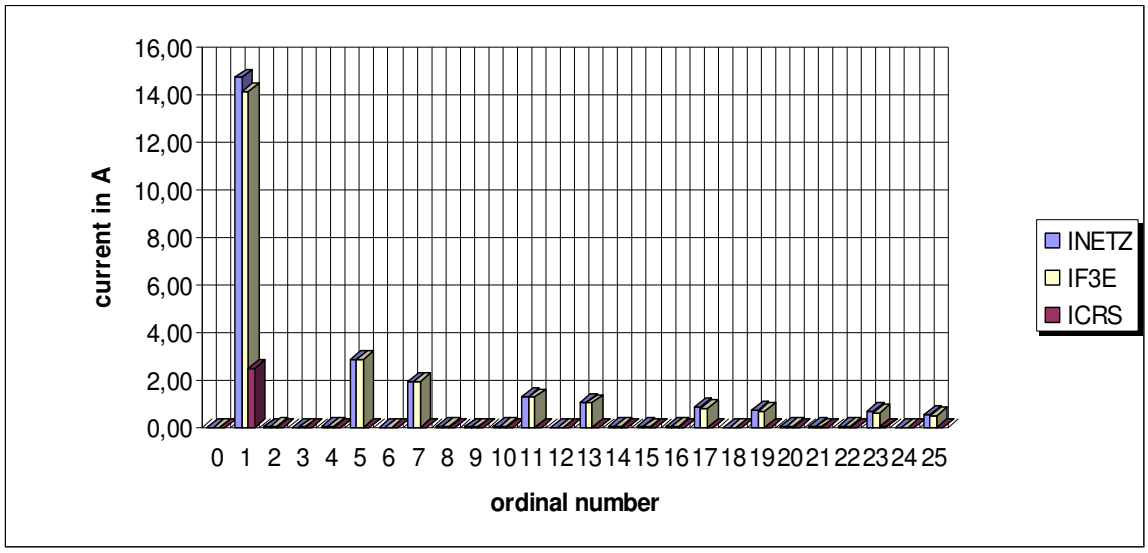

Fig. 4.2: Harmonic spectra from 0Hz to 1250Hz

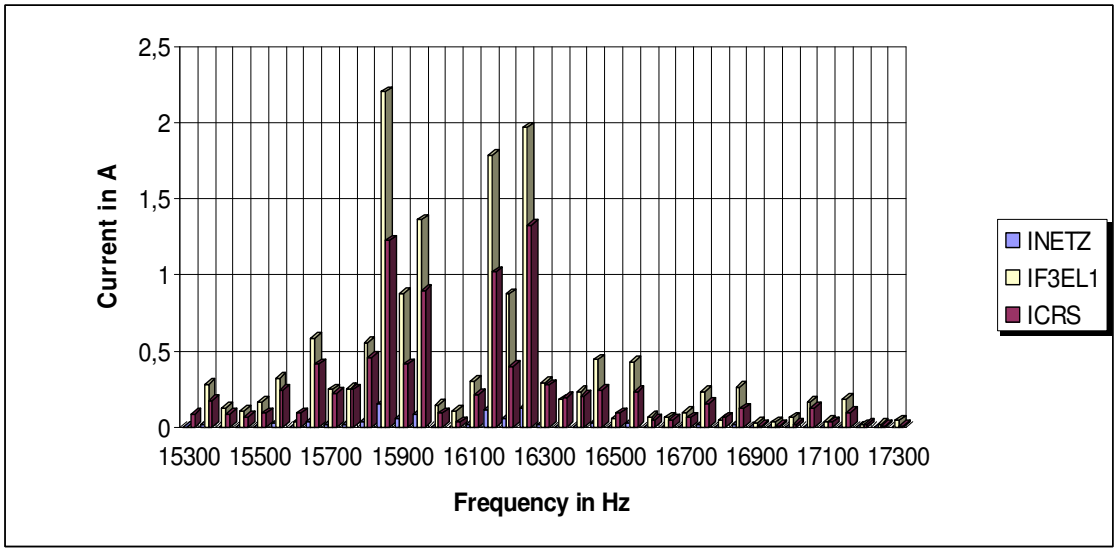

Fig. 4.3: Harmonic spectra from 15.3kHz to 17.3kHz

model was investigated (Fig. 4.4); then, an alternate circuit diagram for one phase was developed.

The alternate circuit diagram consisted of the net-resistance R_{NETZ}, the net-inductance L_{NETZ}, the filter capacitor C_{F3E}, and the current power source I_{F3E} (Fig. 4.5). In this circuit diagram, the two energy storing components L_{NETZ} and C_{F3E} resulted in a parallel resonant circuit, which can be stimulated by the power source I_{F3E}. The parallel resonant

circuit in conjunction with a primarily inductive mains impedance had very little dampening properties. To increase the dampening properties of the resonant circuit, Siemens used resistors in series-connection with the filter capacitors (Fig. 4.6).

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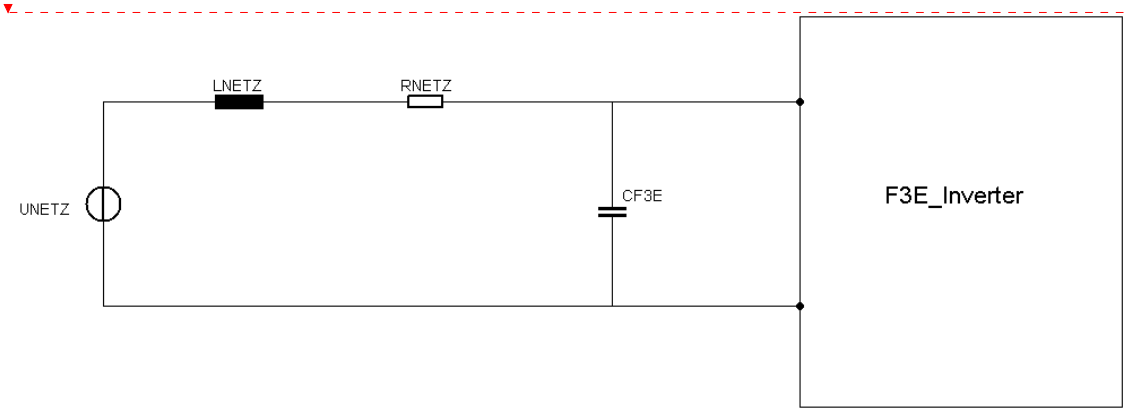


Fig. 4.4: Schematic diagram of a one-phased circuit

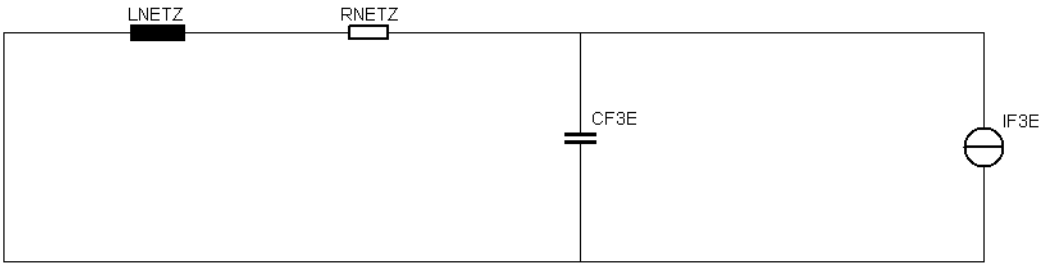


Fig. 4.5: One-phased alternate circuit diagram for determining the resonant frequency

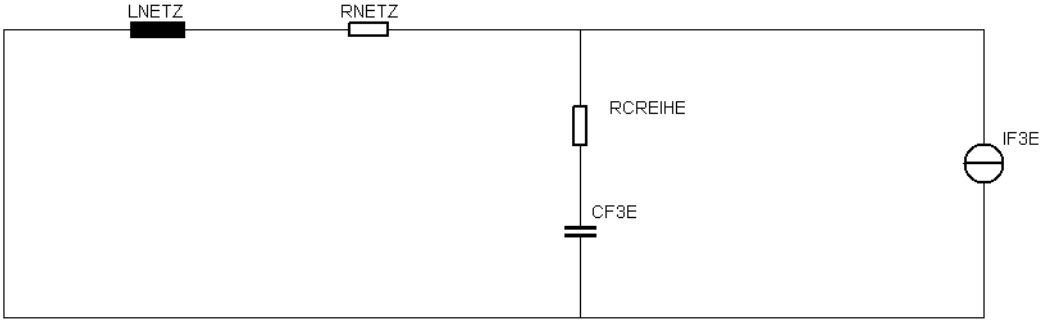


Fig. 4.6: Alternate circuit diagram including the series resistor R_{CREIHE}

The additional resistors allowed a stable and reliable operation of the F3E. The resistors produced additional losses and reduced slightly the effectiveness of the filter circuit. Results from the study conducted by Göpfrich (2006) show that according to established norms and standards, no excessive amount of higher harmonics is produced from the mains point of view. This study, therefore, concentrated on mains configurations in which the parallel resonant circuit is sufficiently dampened by the line resistors without resistors in series to the capacitors. If the line resistors achieve a substantial dampening, the series resistors can be reduced or even be omitted.

4.1.2 Investigation of the anti-resonant circuit

This section originally intended to evaluate the model under environmental conditions; hence, a Bode diagram with the amplitude and frequency response of the resulting impedance from the F3E point of view was generated. The resulting impedance is the parallel circuit consisting of the filter capacitor and network impedance. The frequency response analysis was based on the alternate circuit shown in Fig. 4.6.

A resonance frequency of about 4kHz with a significantly increased parallel impedance can be seen clearly in Fig. 4.7. It represents the expected parallel resonance.

The computation algorithm transformed the elements L_{NETZ} and R_{NETZ} into an equivalent parallel circuit for each calculation step, resulting in a parallel resonant circuit (Fig. 4.8).

$$G_p = \frac{R_{NETZ}}{(R_{NETZ})^2 + (\omega \cdot L_{NETZ})^2} \qquad \text{Eq.4.1}$$

$$BL_p = \frac{-(\omega \cdot L_{NETZ})}{(R_{NETZ})^2 + (\omega \cdot L_{NETZ})^2} \qquad \text{Eq.4.2}$$

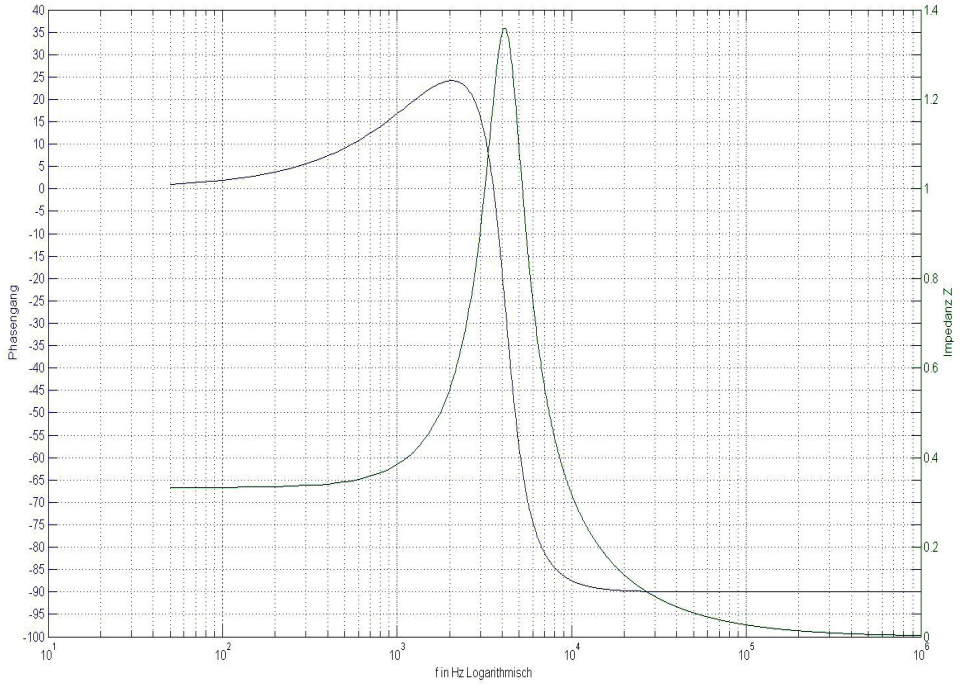


Fig. 4.7: Bode diagram of the frequency response of the impedance

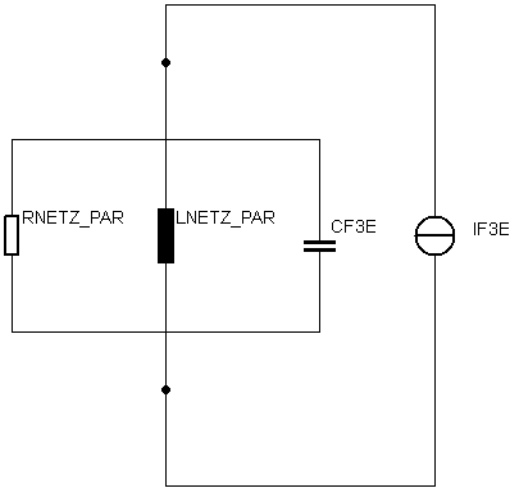


Fig. 4.8: Alternate circuit with the transformed components R_{NETZ_PAR} and L_{NETZ_PAR}

The conductance of the two elements, which is frequency dependent, was computed using Eqs. 4.1 and 4.2. They had to be calculated individually for each frequency because of their frequency dependence. Subsequently, the complex impedance Z, the absolute value, and the angle of Z were obtained (Eq. 4.3).

$$\underline{Z} = \frac{1}{G_p + (jB_{L_P} + jB_{CF3E})} \qquad \text{Eq.4.3}$$

This approach, however, has a disadvantage. The parameters have to be calculated and inputted manually, which make them suitable for individual case reviews only. Therefore, another program was written, which computed first the net parameters with the defaults values:

- Relationship of short-circuit power to the rated output load
- Relationship between inductive and active resistance of the grid at 50Hz

The relationship of the supply network's short-circuit power and the rated output of the load attached to it is generally referred to as R_{sce} (IEC norm 61000-3-12). It must be considered to which load it refers to, as it is quite possible that it refers to a single phase only, and/or to two phases. As it is always used in conjunction with a complete three-phase system in this study, it was not calculated anymore later on. On the basis of the R_{sce} value, the behaviour of the supply network (whether it is a very rigid net or a rather weak one) can already be drawn. In this study, R_{sce} was supplemented by the power factor $\cos(\varphi)$, which is the active portion of the net in relation to the impedance at 50Hz (Eqs. 4.4 and 4.5).

$$R_{NETZ} = Z \cdot \cos(\varphi) \qquad \text{Eq. 4.4}$$

$$X_{NETZ} = Z \cdot \sin(\varphi) \qquad \text{Eq. 4.5}$$

The net parameters were not only determined on the basis of one reference parameter but also on different set-up variants for the same short-circuit power. They varied from an almost active behaviour to a semi-purely inductive behaviour of the net.

The R_{sce_min} was taken from IEC norm 61000-3-12 with a value R_{sce}=33. This value sets the lower limit for power related EMV investigations (harmonic analysis) and was calculated according to Eq. 4.6.

$$R_{sce} = \frac{S_k}{S_{lr}} \qquad \text{Eq. 4.6}$$

The S_k is the short circuit power of the supply network and S_{lr} is the rated power of the load. For the calculation, Eq. 4.6 is transposed to S_k (Eq. 4.7).

$$S_k = R_{sce} \cdot S_{lr} \qquad \text{Eq. 4.7}$$

The rated output of the load is known and the valid range of R_{sce} limited by a minimum value of 33 taken from the standard, and a maximum pre-defined value of 750. As such, the short circuit power can be calculated according to Eq. 4.7. At a rated power of 16kW, this results in a short-circuit power range from 528kVA to 12MVA under the conditions assumed in the model. The examined values of the power factor were within the range of 0.99 to 0.01. In order to keep the quantity of cases examined manageable, the number of values for the power factor was limited to:

[0.99 ; 0.9 ; 0.8 ; 0.6 ; 0.4 ; 0.2 ; 0.1 ; 0.01]

The range of values covers mains configurations ranging from the almost purely inductive to active properties at 50Hz frequency.

In each case, the calculation increments were reduced at the beginning and the end of the range, since the probability of interference is at its largest within these areas. Even with these very few values chosen for the power factor, the program still supplied nearly 800 values per output variable. In total, five nominal output values were produced by the program. These were:

- the active resistance of the grid R_{NETZ};
- grid inductance L_{NETZ};

- the resonant frequency of the respective configuration;
- the quality of the resonant circuit; and
- total impedance Z.

The active resistance of the grid R_{NETZ}, and L_{NETZ} later served as grid parameters in the model, which led to the possibility of looking for areas of malfunction more thoroughly. Additionally, since the resonant frequency was also known, the switching frequency of the pulse inverter could be adjusted to excite the resonant circuit. With the aid of the quality Q of the resonant circuit, a further pre-selection of parameters was done. The quality Q was calculated according to Eq. 4.8.

$$Q = \frac{\sqrt{\frac{CF}{L_p}}}{G_p} \qquad \text{Eq. 4.8}$$

The quality of the resonant circuit Q is valid only in the case of resonance. It should be noted that the elements L_{NETZ} and R_{NETZ} were converted in each step into the equivalent values of a parallel circuit. Therefore, the values of L_{NETZ} and R_{NETZ} could not be used for the computation of the quality Q. The values of the equivalent alternate circuit had to be used. They were computed based on Eqs. 4.1 and 4.2 with the proper frequencies. The quality Q in the cases selected was determined according to Eq. 4.9.

$$Q = \frac{\sqrt{\frac{C_F}{\left(\frac{\left(R_{NETZ^2} + (\omega_0 \cdot L_{NETZ})^2\right)}{\frac{\omega_0 \cdot L_{NETZ}}{\omega_0}}\right)}}}{\frac{R_{NETZ}}{(R_{NETZ^2} + (\omega_0 \cdot L_{NETZ})^2)}} \qquad \text{Eq. 4.9}$$

C_F represents the filter capacitor and ω_0, the resonant angular frequency of the circuit. Figure 4.9 shows the quality Q as a function of the power factor (PF) of the grid and of R_{sce}. The quality Q of the resonant circuit obtained high values at a lower range of R_{sce}. R_{sce} achieved its maximum value at a PF<=0.1. Moreover, even with the smallest value

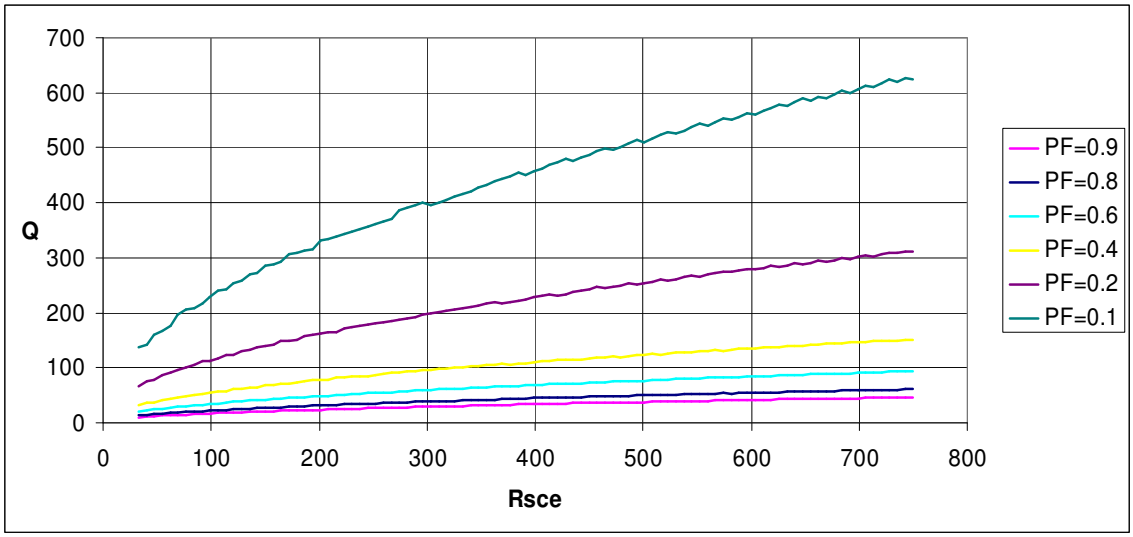


Fig. 4.9: The quality Q as a function of the grid PF and of R_{sce}

for R_{sce}, and a nearly active grid impedance $(PF \geq 0.8)$, the quality Q still exceeded the value of 1 (Fig. 4.10).

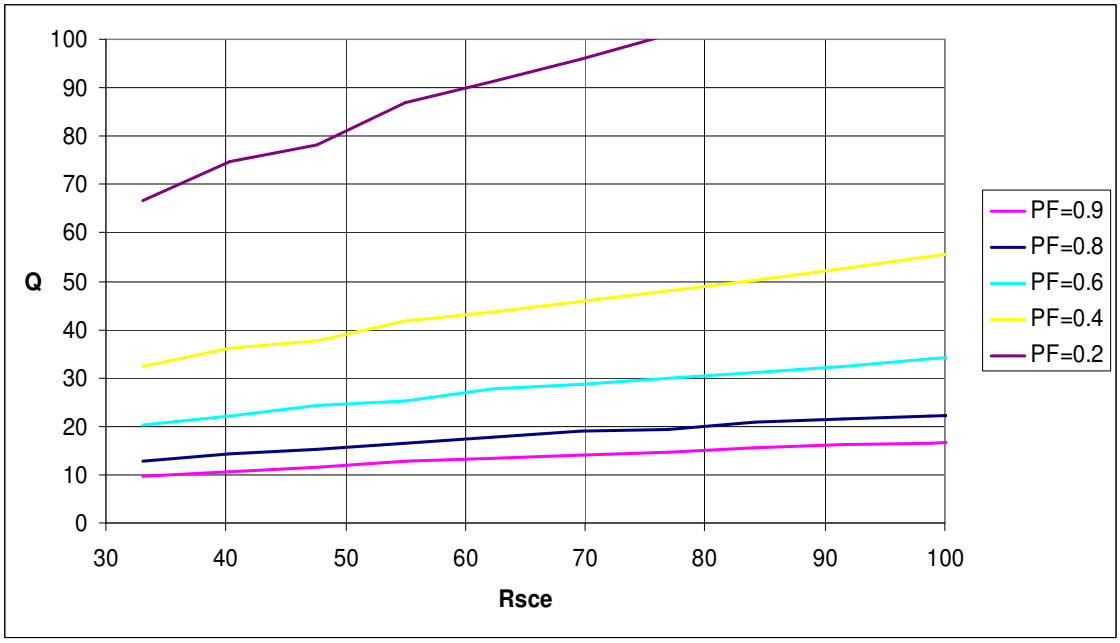


Fig. 4.10: Enlargement of the lower range of R_{sce} from Fig. 4.9

In the model, the quality Q is the direct quotient of the capacitor current in relation to the harmonic content fed by the F3E at resonance frequency. It can then be concluded that high filter currents will result from the excitation with resonant frequency due to higher harmonics.

The resonant frequencies of these configurations were distributed over a very large range (Fig. 4.11). A high PF value, i.e., a net with a large active resistance in relation to the inductive resistance, results in an even higher resonant frequencies. The grid inductance in this case was small; therefore, the resonant frequency was high.

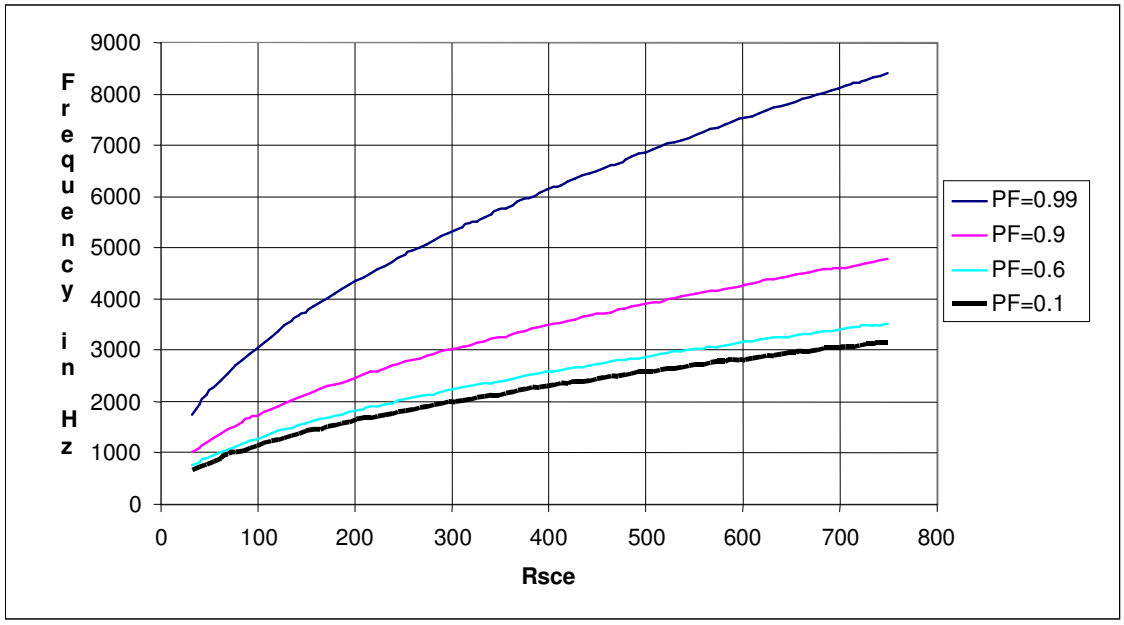


Fig. 4.11: Resonant frequency over R_{sce} with different PF values

With a PF=0.01, the net is almost completely inductive with only a very small active portion. The quality Q in this configuration varied between Q=1277 and Q=6292 (Fig. 4.12) because of the small active portion of the grid impedance. The resonant circuit exhibited almost no dampening.

The capacitor current at resonant frequency clearly increased in relation to the current fed by the F3E. In a worst case scenario, a quality of Q=6292, and an F3E current of 1A would result in a capacitor current of 6292A. Such high qualities must not occur. A resistor R_{CREIHE} in series connection with the filter capacitor was incorporated to reduce

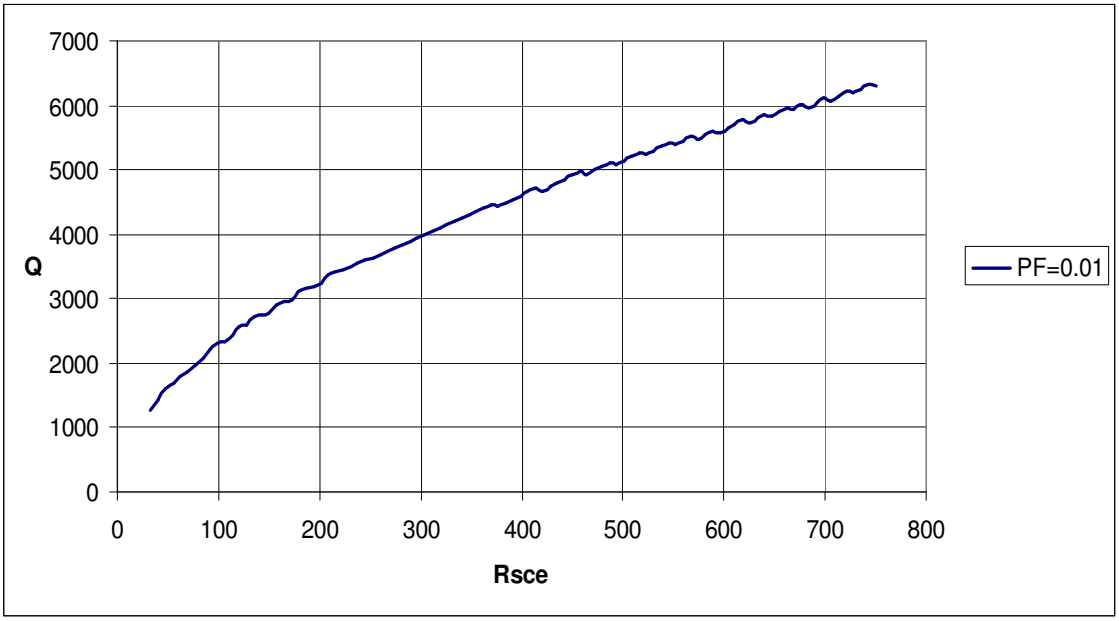


Fig. 4.12: The quality Q over R_{sce} with PF=0.01

the quality to manageable values. Cases with high quality (Q>200), however, exhibited a narrow bandwidth B limited to 10Hz.

A study with $PF \leq 0.1$ range was conducted by Göpfrich (2006). He examined a highly inductive grid in connection with a series resistor and the capacitor, focusing on possible voltage increases. Findings revealed that problems can occur with low R_{sce} values (R_{sce}<100). Increased harmonic voltage levels, higher than the permitted values, can actually occur (International Electronic Commission, 2010). Göpfrich (2006) then proposed as a solution, the use of a second input filter in order to shift the resonant frequencies into an innocuous range. In this study, only a single filter was employed, since it represents the standard configuration and only the response within a range of 100Hz to 2.5kHz with its feedback effects to grid voltage was examined.

The limited range of R_{sce}<100 examined earlier by Göpfrich (2006) produced resonant frequencies in the 650Hz to 1.15kHz range in the preliminary findings. These frequencies correspond to the ordinal numbers of the harmonics from 13 to 23. The F3E line-current displayed a harmonic spectrum comparable with conventional diode rectifiers. Within the range of small ordinal numbers (2 to 16), the F3E performed better; though, worse for higher numbers (>16). This means that within this range, the

F3E can excite the resonant circuit situated at its input terminals. For an R_{sce}>100, the danger of exciting the resonant frequency diminishes because of the small bandwidth and the rising ordinal number. The resonant frequency, however, for a PF lower than 0.1 does exceed 3.15kHz within the range of R_{sce}=33 to R_{sce}=750. Changing the characteristics of the grid from purely inductive to one of predominantly active behaviour increases the resonant frequencies to a value of 8.4kHz. Based on the harmonic spectra shown at the beginning, no further problems should be expected on exciting resonant frequencies for switching frequency of 16kHz, except within the range pointed out by Göpfrich (2006). This is not true, however, with regards to the semiconductors. In reality, the PCI attached to the F3E can also operate with this switching frequency (16kHz). Due to the associated high losses in the semiconductors, a thermal overloading of the semiconductors will result, though not at rated output. At rated output, the switching frequency used by the PCI is approximately 4kHz. The F3E passes through the switching pattern of the PWM to the input filter. Thus, the switching frequency of the PCI could excite the parallel resonant circuit formed by the filter capacitor and the grid inductance.

4.2 Simulations and data evaluation

This section describes the simulation runs and presents the output data. The simulations utilised the model F3E_PWR with limited grid parameters according to the rules stated in Chapter 4.1.2. Subsequently, the current shapes and their harmonic spectra were evaluated.

4.2.1 Range of grid parameters examined

Grid parameters have a limited range as shown in Chapter 4.1. Hence, the following investigations were conducted to determine the stimulation potential of the switching frequencies of the pulse controlled inverter with regards to parallel resonant circuit. Initially, only grid parameters which would result in a resonant frequency close to the switching frequency of the inverter were considered. In conjunction with the net filter, the resonant frequency was approximately 4kHz. The bandwidth of the examined parameter range was limited to 200Hz, which was four times the mains frequency. This frequency range is based on the assumption that the switching frequency of the inverter

at rated power output is 4kHz. It has already been established that an increased amount of harmonics can be observed within the frequency range from 3.9kHz to 4.1kHz. As a result, 25 different parameter configurations were examined within that frequency range. To present the results of all technically relevant combinations would exceed the scope of this work; hence, only one parameter configuration as a typical example is described and analysed.

4.2.2 Model simulation at a selected critical parameter configuration

This section aims to determine whether the assumptions made earlier (Chapter 4.1.2) were correct, and a distinct increase of the filter current would be observed. The quality Q for the assumed parameters in this case was 60.

The following configuration parameters were used for simulating the model F3E_PWR.

PF 0.8				
R_{sce}	S_k/VA	R_{NETZ}/Ω	L_{NETZ}/H	f_{r0}/Hz
721	3.689	0.011	2.65E-05	4k

In the configuration, the R_{sce} and S_k indicate a relatively stiff grid. The voltage drop along the supply was low. The resonant frequency was very close to the switching frequency of 4kHz of the inverter.

Figure 4.13 presents the voltage and current shapes of the simulation of the model with the given parameter set. The voltage U_{NETZ} represents the ideal voltage source incorporated into the macro of the three-phased power system. It is used as a reference for periodic time and angular phase shift. As mentioned earlier, the rated output of the inverter should be approximately 16kW. At this rated output, a rough estimation of the current can be calculated using Eq. 4.10.

$$I = \frac{P}{\sqrt{3} \cdot U} = \frac{16000kW}{\sqrt{3} \cdot 400V} = 23A \qquad \text{Eq. 4.10}$$

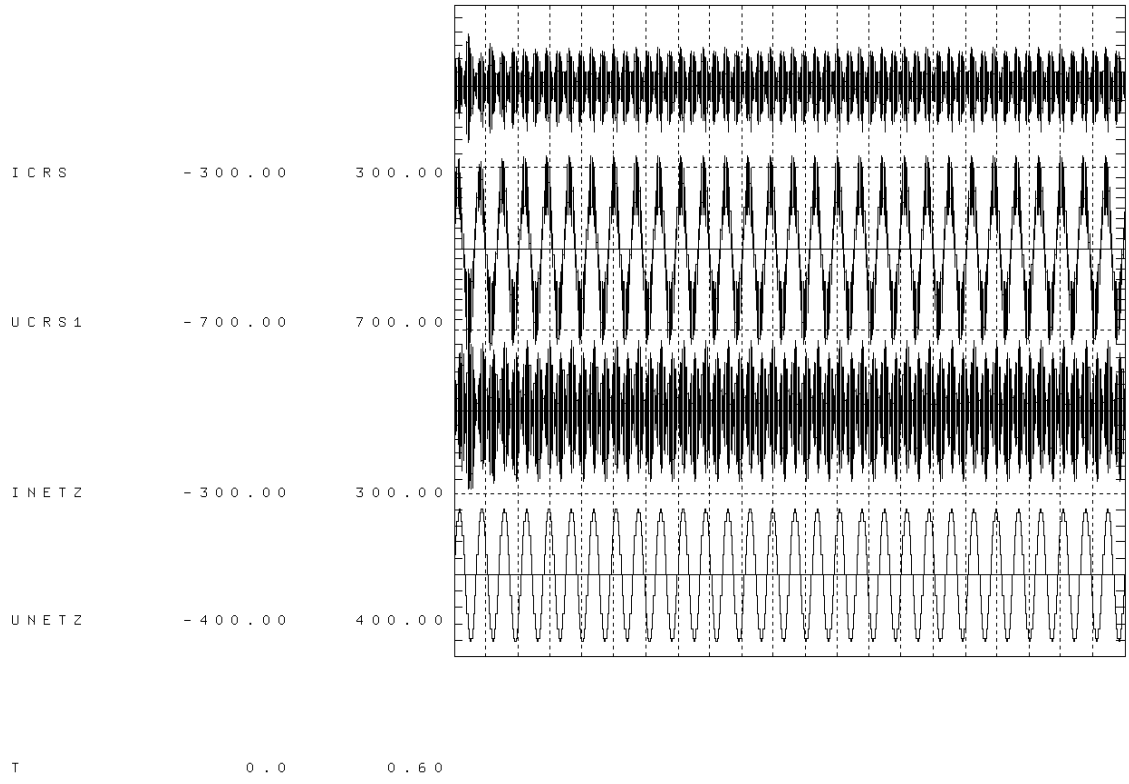


Fig. 4.13: Shapes of the net and filter voltages, and currents

It is interesting to note that on close observation, the filter and mains current were in the –300A to +300A range. This range exceeded the rated current by a factor of 13. The characteristic input current shape of the circuit could not be recognised despite enlarging some segments of the currents (Fig. 4.14).

The shapes of the two currents were completely distorted and deviated greatly from the currents shapes of normal operational conditions as shown in Fig. 4.15.

Disturbed operation is defined as the operation of the model under excitement with the resonant frequency. Figure 4.15 shows the currents I_{CRS} and I_{NETZ} under normal or non resonant conditions. This is simply defined as normal operation for future reference.

The amplitudes of the currents in Fig. 4.14 increased greatly to about 250A. In contrast, normal amplitude values were in the range of about 96A. Therefore, the amplitudes of the distorted currents increased by a factor of 2 to 3 as compared with the normal operational conditions.

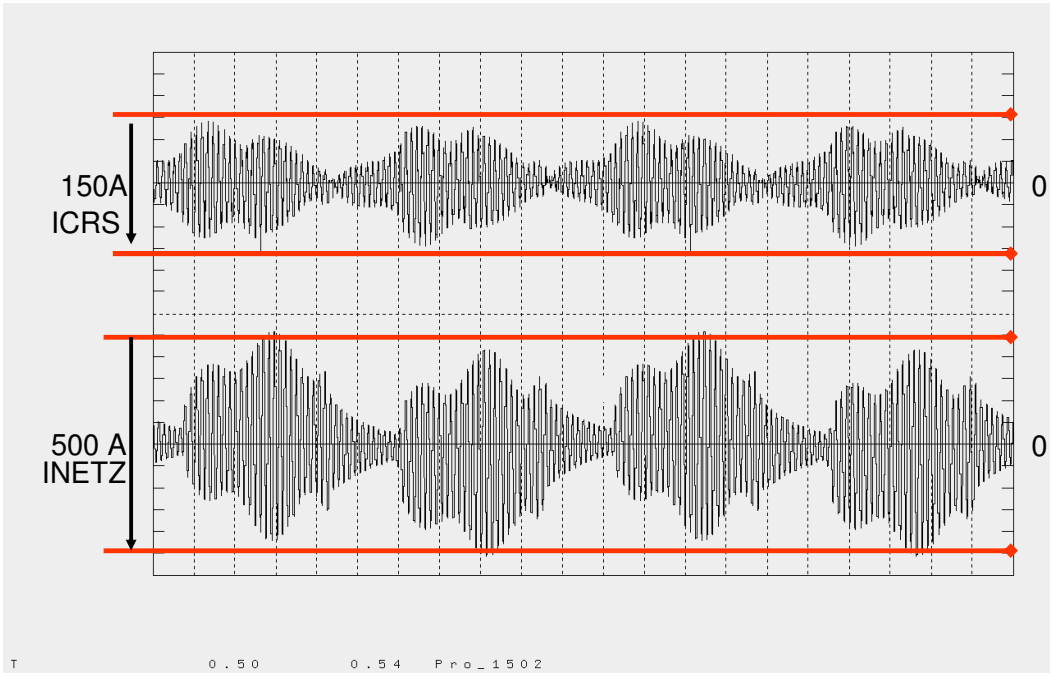


Fig. 4.14: Shapes of I_{CRS} and I_{NETZ} for a duration of 40ms of resonant operation (R_{sce}=721, PF=0.8, f_0=4kHz)

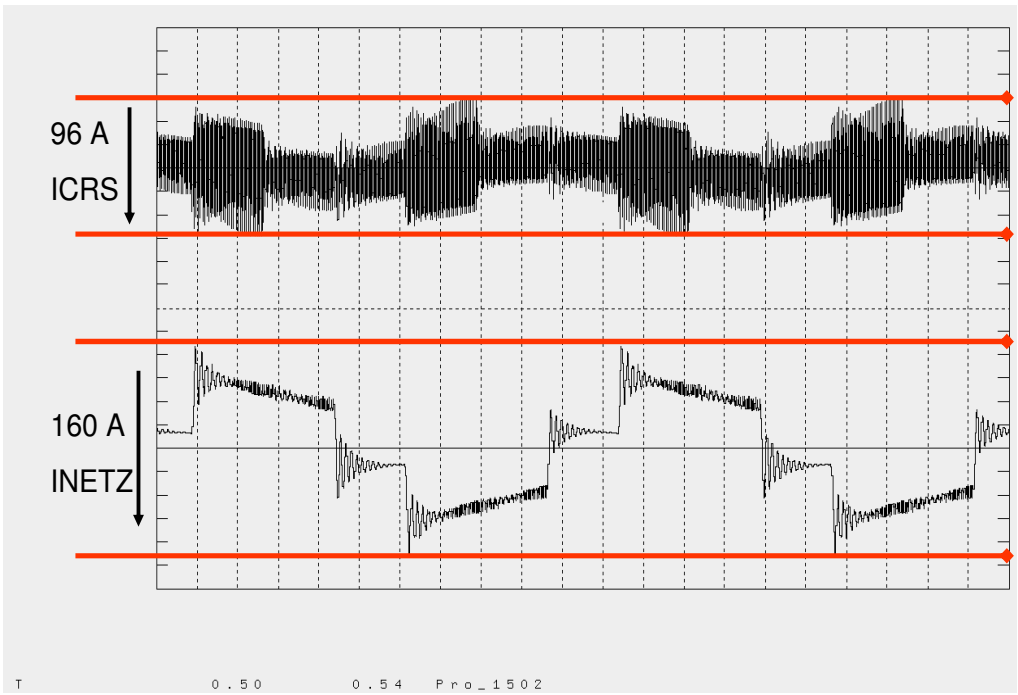


Fig. 4.15: I_{NETZ} and I_{CRS} under normal operation for a duration of 40ms (R_{sce}=750, PF=0.2, f_0=3.175kHz)

It can be observed, though, that the general shape of the distorted currents showed fewer distortions in the higher harmonics range (Figs. 4.16 and 4.17).

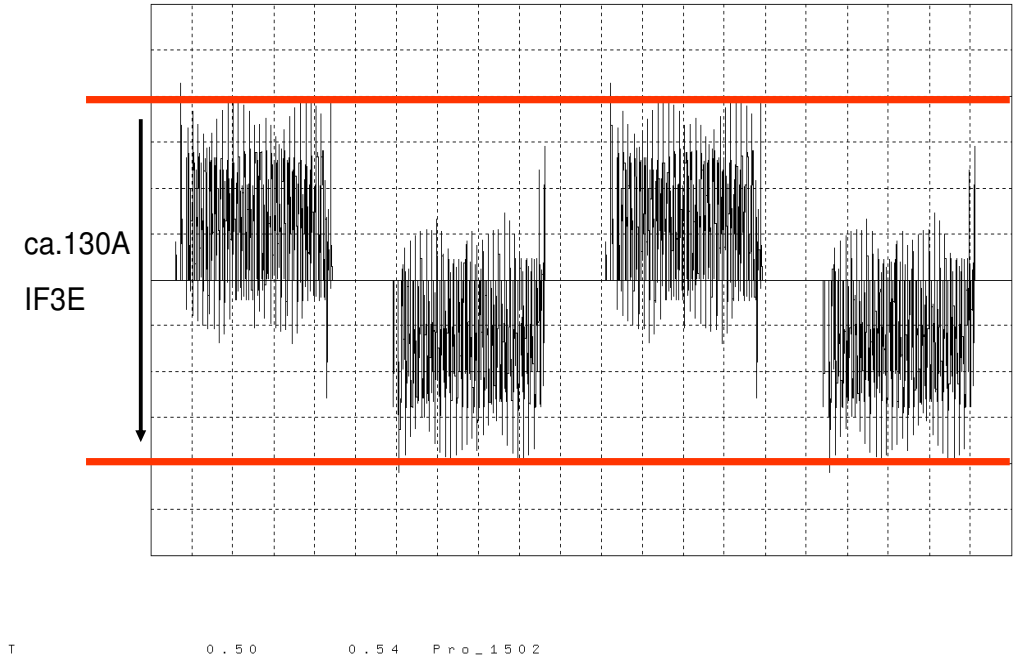


Fig. 4.16: Current shape of the F3E under distorted operational conditions for a duration of 40ms

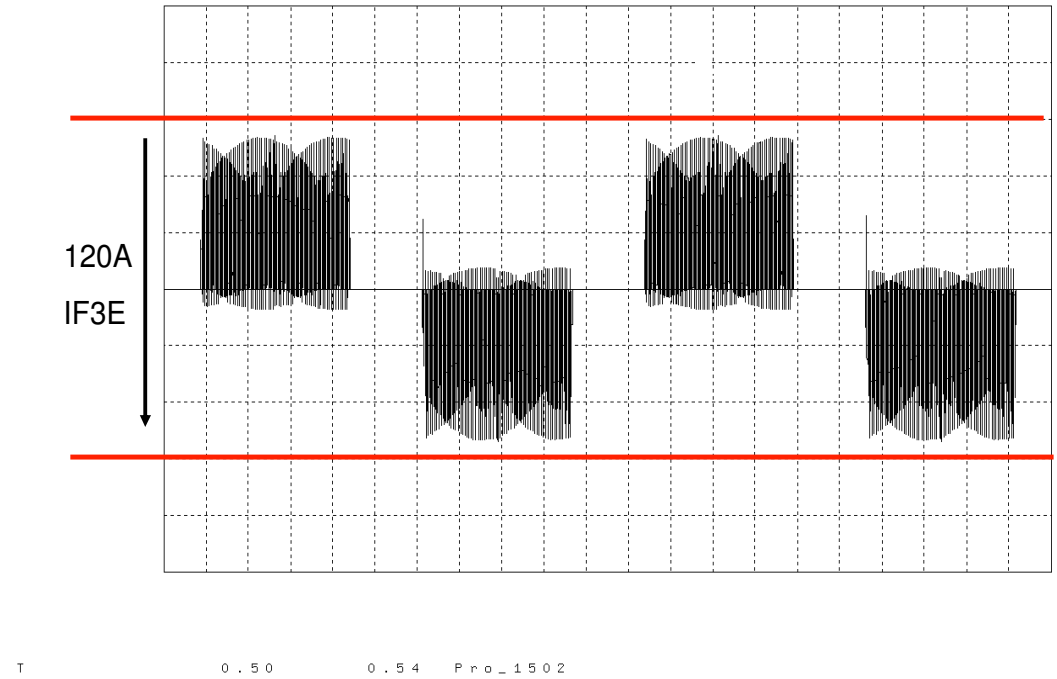


Fig. 4.17: Current shape of the F3E under normal operational conditions for a duration of 40ms

The amplitude of the F3E current confirms the results of the preliminary investigation with regards to the effects of the switching frequency of the inverter. It can be clearly seen that the inverter with its switching frequency of 4kHz stimulated the resonant circuit. As a result, the input current increased by a factor of almost three as compared with the normal operation. Therefore, it is theoretically possible to have an operation without the series resistor R_{CREIHE}, but a stimulation with resonant frequency must be prevented, since it would most likely damage the circuitry. This, however, can not be guaranteed for a large number of industrial applications. In most cases, the grid impedances are unknown and tend to change over time.

The harmonic spectra of the currents I_{NETZ}, I_{CRS}, and I_{F3E} were analysed. This was done in two steps. First, the lower frequency range from 0Hz to 1850Hz was evaluated. The harmonic spectra of the three currents in this frequency range shown in Fig. 4.18 exhibited no peculiarities. The distribution of the higher harmonics was similar to the distribution under normal operating conditions. The current amplitude of the 5th harmonic was about 20 percent of the fundamental mode, and the amplitude of the 7th

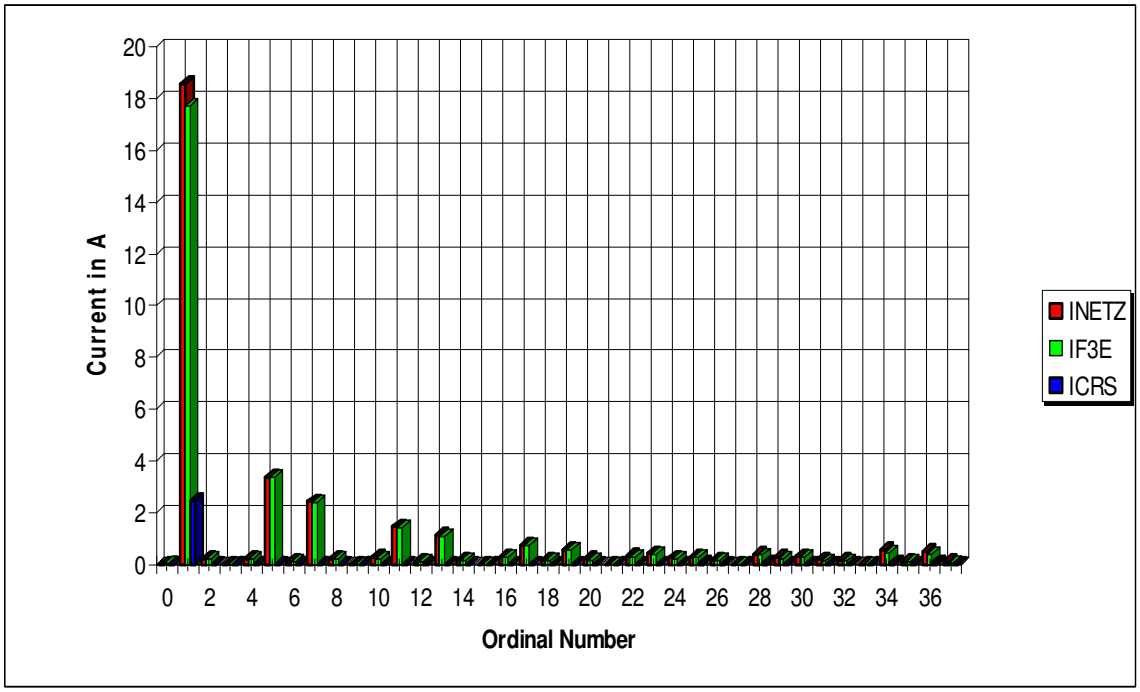


Fig. 4.18: Spectra of the three currents in the frequency range 0Hz to 1.85kHz

harmonic, almost one-seventh. The amplitude of the fundamental mode was between 18A and 19A. This suggests that the load connected to the inverter did not represent the rated value of 16kW. This, however, has no negative repercussions on the situation examined since the output power was still significantly above 10kW.

It can also be seen that, except for a filter current of 2.5A at 50Hz (in blue in Fig. 4.18), no further filter currents were present in the lower frequency range. Therefore, the spectra of normal operation and disturbed operation mode were similar in the lower frequency range of up to 1850Hz. As such, the current components present under disturbed operation conditions must occur at a higher frequency range in the harmonic spectra.

The second step involves the examination of the frequency range from 3.5kHz up to 4.5kHz using a Fast Fourier Transformation (FFT). The result is shown in Fig. 4.19.

The highest values were reached at the 76^{th} and 78^{th} harmonics, representing frequencies of 3.8kHz and 3.9kHz, respectively. Figure 4.19 clearly shows a significant increase in the mains and filter currents as compared with the input current (shown in green) of the F3E. As previously described, the quality Q of the resonant circuit reached a value of 60. If the assumptions made earlier were correct, the filter current should exceed the input current of the F3E by the same value (Eq. 4.11).

$$Q = \frac{I_C}{I_0} = \frac{I_{CRS}}{I_{F3E}} \qquad \text{Eq. 4.11}$$

Transposing Eq 4.11 to I_{CRS} results to Eq 4.12.

$$I_{CRS} = Q \cdot_{IF3E} 60 \cdot 4.67 = 280.2\text{A} \qquad \text{Eq. 4.12}$$

The theoretical result deviated, however, from the simulation result. Instead of the expected 280A, the resulting filter current was only 42.7A. One reason for this reduction was the delta configuration of the filter capacitors. The filter current of one capacitor had to be multiplied by a factor of $\sqrt{3}$ in order to calculate the real filter

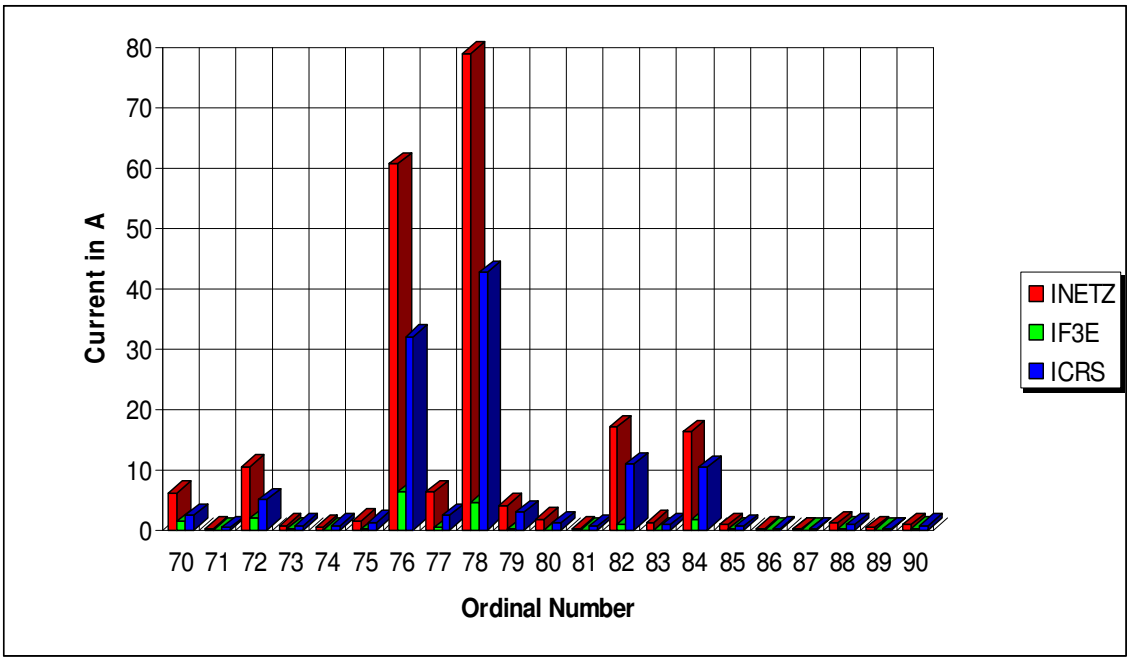


Fig. 4.19: Harmonic analysis of the three currents I_{NETZ}, I_{CRS}, and I_{F3E}

current, resulting to a value of only 73.9A. This was only about one fourth of the expected 280A.

The greatly reduced current can be explained by looking at the value of 30mΩ of the serial resistor R_{CREIHE}. If this resistor would not have been omitted to calculate the quality Q of the resonant circuit, Eqs. 4.13 to 4.16 would have been valid.

The value for G_P can be calculated according to Eq. 4.15.

$$L_p = \frac{1}{B_{Lp} \cdot \omega} = \left(\frac{(\omega \cdot L_{NETZ})}{(R_{NETZ})^2 + (\omega \cdot L_{NETZ})^2} \right) \cdot \frac{1}{\omega} \qquad \text{Eq. 4.13}$$

The capacitor C_p can be computed according to Eq. 4.14.

$$C_p = \frac{B_{Cp}}{\omega} = \left(\frac{\left(\frac{1}{\omega \cdot C_{F3E}}\right)}{(R_{CREIHE})^2 + \left(\frac{1}{\omega \cdot C_{F3E}}\right)^2} \right) \cdot \frac{1}{\omega} \qquad \text{Eq. 4.14}$$

The conductance G_p can be calculated according to Eqs. 4.15 and 4.16.

$$G_p = \frac{1}{R_{NETZ}} + \frac{1}{R_{CREIHE}} \qquad \text{Eq. 4.15}$$

$$G_p = \left(\frac{R_{NETZ}}{(R_{NETZ})^2 + (\omega \cdot L_{NETZ})^2} \right) + \left(\frac{R_{CREIHE}}{(R_{CREIHE})^2 + \left(\frac{1}{\omega \cdot C_{F3E}}\right)^2} \right) \qquad \text{Eq. 4.16}$$

$$Q = \frac{\sqrt{\frac{C_p}{L_p}}}{G_p} = 30 \qquad \text{Eq. 4.17}$$

The value of the quality Q calculated using Eq 4.17 was 30. As such, the result using Eq 4.12 was changed, and is now expressed using Eq. 4.18.

$$I_{CRS} = I_{F3E} \cdot Q = 4.67 \cdot 30 = 140A \qquad \text{Eq. 4.18}$$

Nevertheless, the quality obtained using these more accurate assumptions regarding the topology of the resonant circuit still resulted into a value which deviated roughly by a factor of two from the simulation results. This deviation can be explained by taking a closer look at the semiconductor models used. The values of the dampening resistor and the active component of the mains impedance were similar to the forward resistance of the diodes cannot be neglected. It forms an active part of the resonant circuit, increasing its dampening properties. During the simulation runs, this forward resistance of the diodes reduced the quality Q of the resonant circuit to a value of 16.

The variation of the dampening resistor should help in detecting problem areas or highlight their occurrence. Thus, a further simulation run with an increased value of one magnitude for the resistor R_{CREIHE} was done. This changed the quality of the resonant circuit significantly. The new quality, calculated using Eqs 4.14 to 4.17, resulted to a value of 5.5. This increased the filter current, but on a much reduced scale. The comparison with the new simulation results highlighted the influence of the dampening resistors on the current behaviour.

The current and voltage shapes of grid and filter components as illustrated in Fig. 4.20 show a significant improvement in comparison with the distorted operation mode shown in Fig 4.13. The mains current I_{NETZ} was, however, still greatly distorted. As expected, the higher dampening resulted in a reduced current (Fig. 4.21).

Figure 4.21 shows the shape of the currents I_{NETZ} and I_{CRS} within a time range of 40ms. The shape of the mains current was closer to the shape shown under normal operation

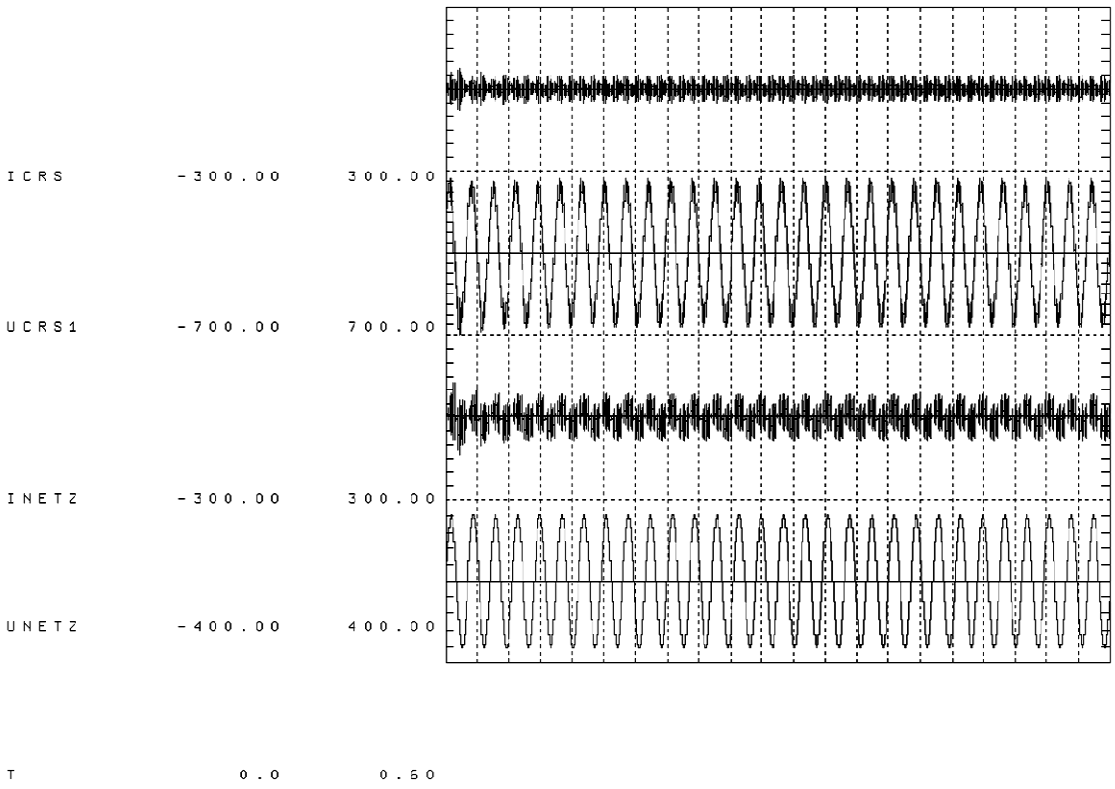


Fig. 4.20: Current and voltage shapes of grid and filter components

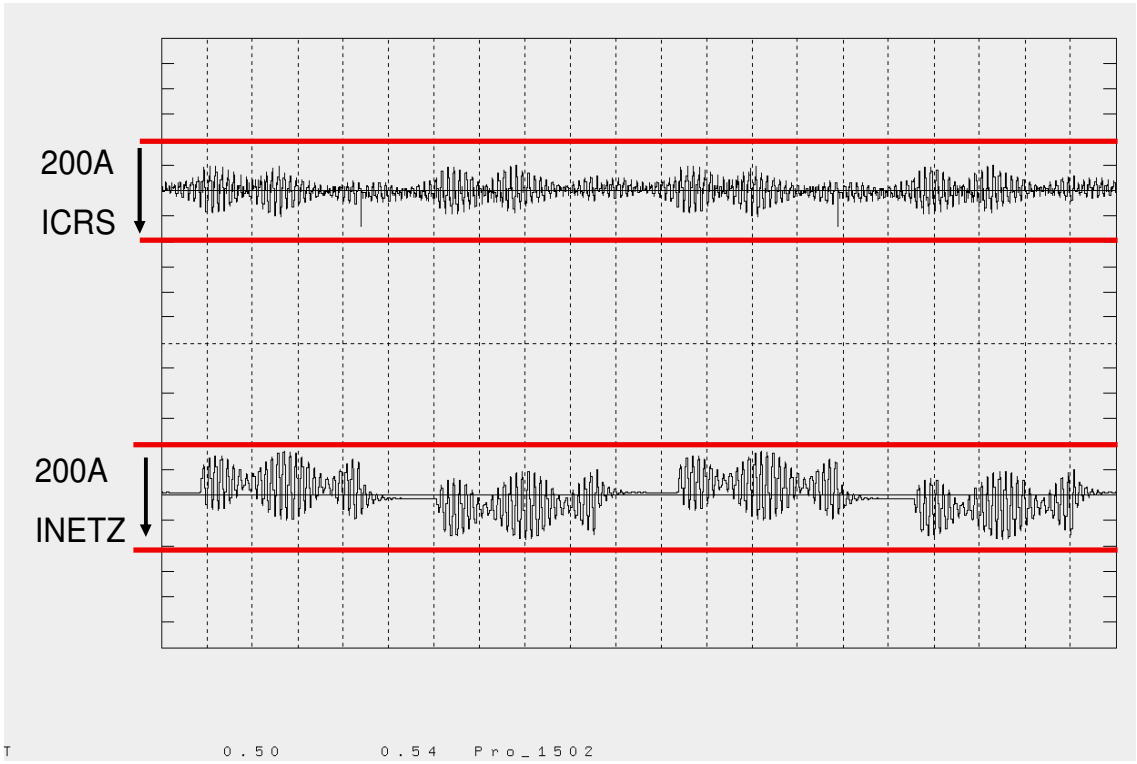


Fig. 4.21: Shapes of I_{NETZ} and I_{CRS} for a duration of 40ms

conditions. It can then be assumed, even before performing an FFT, that the spectral distortions in the 4kHz range would be reduced.

Within the mains current, the 120 degree block produced by the F3E can be recognized. The shape of the I_{F3E} current (Fig. 4.22) was very similar to that of the normal operation mode with a small series resistor, and was not described here any further.

The analysis of the lower frequency range was omitted, as this would produce no new results.

Figure 4.23 shows the analysis of the higher frequency range. Observing the ordinate scale reveals a significant reduction of the current values.

The quotient of the currents I_{CRS} and I_{F3E} produced an approximate value of 5.5, which is within the expected range. With the increased dampening resistor, forward resistance of the diodes exerted no further significant effect on the dampening properties of the resonant circuit.

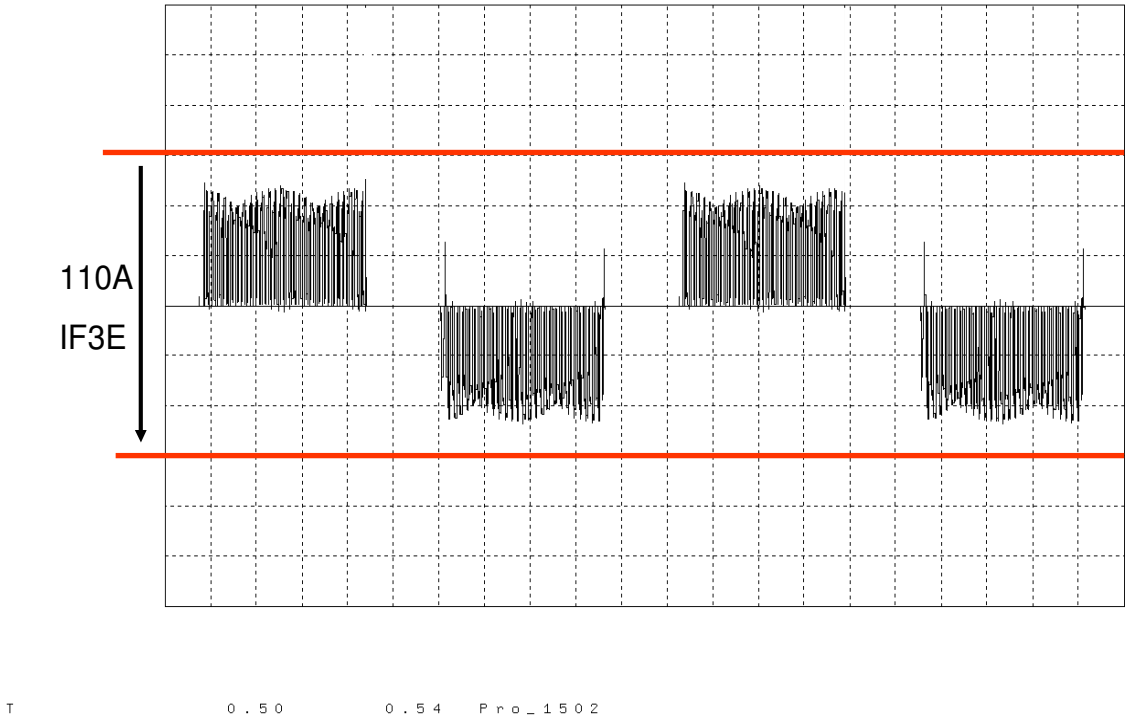


Fig. 4.22: Current shape of the I_{F3E} for a duration of 40ms

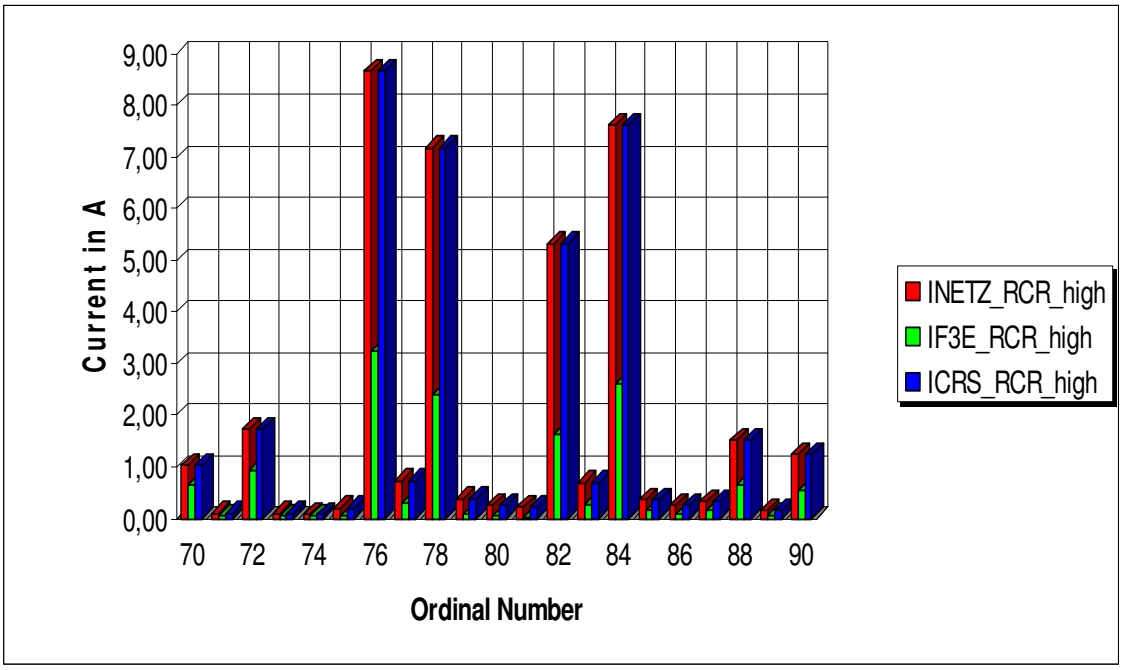


Fig. 4.23: The harmonic spectra within the range 3500Hz and 4500Hz

The increase in the value of the dampening resistor produced the expected results by reducing the currents I_{CRS} and I_{NETZ} by one magnitude. This one magnitude decrease, however, incurred an increase in associated losses as computed using Eq 4.19.

$$P_V = I^2 \cdot R = I_{CRSrms}^2 \cdot R_{CREIHE} \qquad \text{Eq. 4.19}$$

In this configuration, they amounted to 94W (Eq. 4.20).

$$P_v = (56.64A)^2 \cdot 0.033\Omega = 94.08W \qquad \text{Eq 4.20}$$

These were the losses only from one phase of the filter circuit. To calculate the total losses of the filter, the filter was multiplied by a factor of three, resulting to a value of 282W. This would significantly raise the temperature within the filter itself.

In the second example, the currents were reduced; however, the value of the resistor R_{CREIHE} increased, resulting in associated losses amounting to 83.7W (Eg. 4.21).

$$P_v = (16.7\text{A})^2 \cdot 0.33\Omega = 83.7W \qquad \text{Eq. 4.21}$$

Although the current in this example was reduced by 40A, the resistor increased by one magnitude, resulting in losses approximately 10W lower than the first example. The total losses amounted to 251W, which does not constitute a significant improvement; although, the grid elements would be less stressed.

Thus, it can be concluded that with a higher dampening resistance, the harmonic spectra of the line current in the case of resonance improve substantially. The losses incurred, however, are only marginally reduced. Reducing the series resistor by one magnitude does not reduce the total active power losses either. In this regard, saving losses by omitting the series resistors does not seem to be promising.

5 Configuration of the AFE and F3E connected to the same mains

5.1 Examination of the model including F3E and AFE

This chapter starts with a theoretical examination of the system. As a first step, an alternate circuit diagram will be introduced and examined with regards to the resonant circuits contained within it. The hypothesis is that circuit topologies will work flawlessly outside the areas of resonance. The results thus obtained will be compared with the examinations done in chapter 4. Areas of suspected disturbed operation will then be examined, always starting with the simulation first and a discussion of the spectra of currents and voltages after that.

The second part of the study extends the F3E_PWR model by including the AFE model and the adapted mains network structure (Fig. 5.1). This new model is referred to as AFE_F3E. It is used to examine the feedback effects on the mains network and the mutual interferences of the two drive systems.

Taking into account the results presented in Chapter 4, this chapter focuses on the resonant circuits contained within the model and the resulting resonant frequencies. As a first step, a single-phased alternate circuit diagram of the model was again developed (Fig. 5.2).

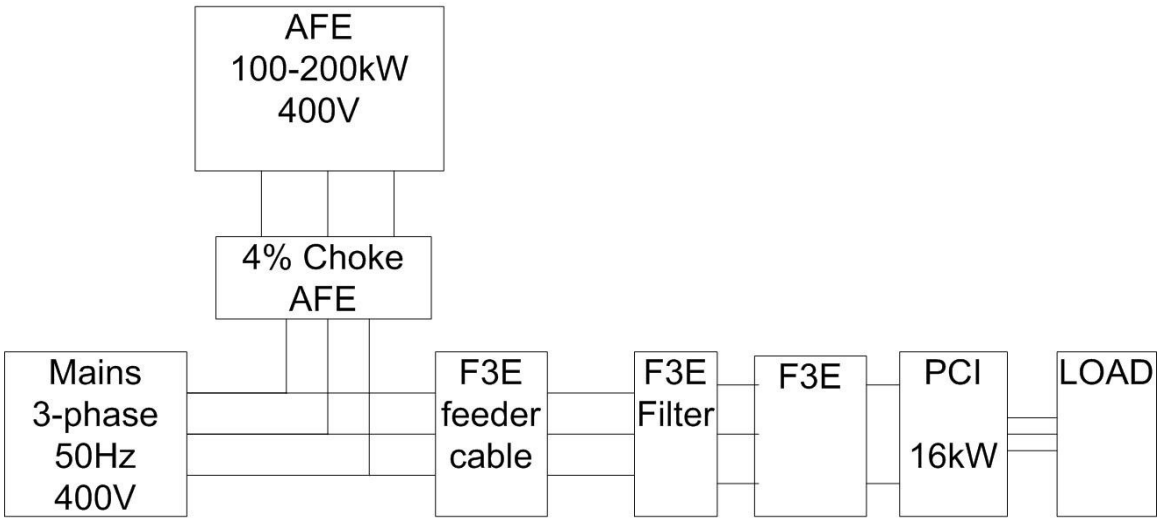


Fig. 5.1: Schematic diagram of the complete model AFE_F3E

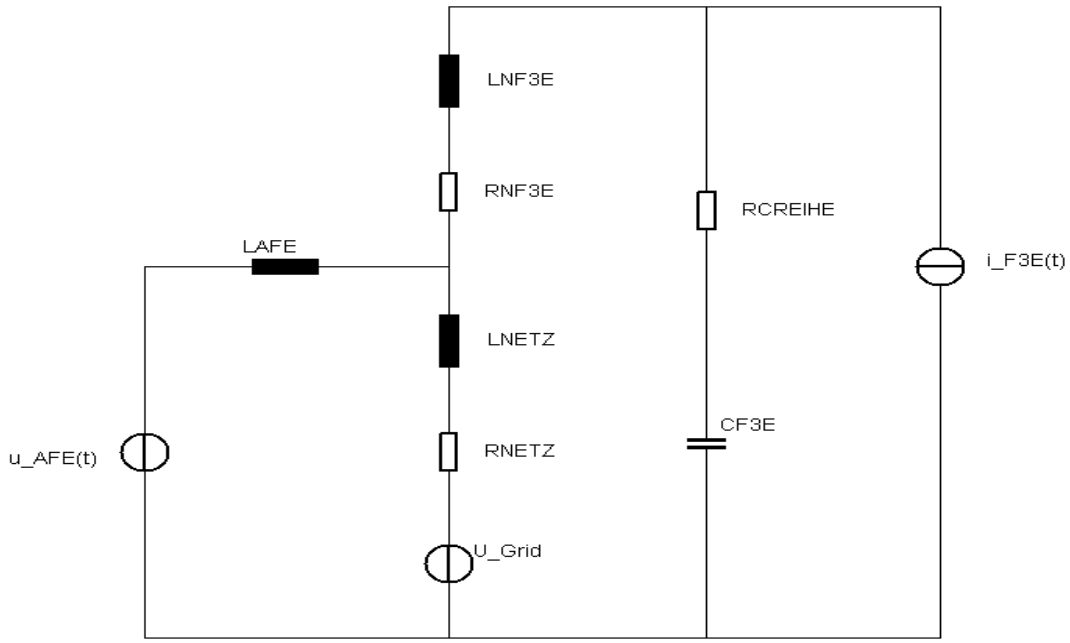


Fig. 5.2: Single-phased alternate circuit diagram of the AFE_F3E model

Figure 5.2 contains the mains voltage as represented by the voltage source U_Grid, the currents source i_F3E(t) substituting the F3E, and the voltage source u_AFE(t) substituting the AFE. The voltage source U_Grid can be disregarded because of its low frequency (50Hz). Therefore, the alternate circuit diagram was simplified to contain only the relevant energy sources u_AFE(t) and i_F3E(t).
The AFE was substituted by a voltage source instead of a current source like F3E because of the design of the respective intermediate circuits. The intermediate circuit of the AFE was equipped with a relatively large capacitor of 5mF. This capacitor was 2500 times larger than the intermediate capacitor of the F3E. Therefore, the AFE unlike the F3E, transfers rectangular shaped voltages to its terminals. These voltages are generated through the chopping of the nearly constant DC-line voltage by means of PWM.

5.1.1 Influence of the F3E on the AFE_F3E model

To determine the influence of the energy sources, i_F3E(t) and u_AFE(t), on the alternate circuit diagram, the superposition principle was applied. Two modified circuit diagrams with only one energy source each were analysed. As a rule, unused current sources are simply omitted and unused voltage sources are short circuited. The effects

of the current source i_F3E(t) were first examined (Fig. 5.3). The voltage source u_AFE(t) was short-circuited, resulting to a parallel configuration of the filter inductor L_{AFE} with the mains impedance consisting of L_{NETZ} and R_{NETZ}.

Connecting inductors in parallel configuration results in an alternate inductor, which is always smaller than the smallest inductor present in the configuration. Since the inductor L_{AFE} was large in comparison with the mains inductor L_{NETZ}, the former was omitted to simplify the network, resulting in the serial configuration of the mains components (Fig. 5.4). This is identical to the alternate circuit diagram used in Chapter 4.1. The topology of the mains network, however, is unchanged from the F3E point of view. It is still basically a parallel resonant or trap circuit.

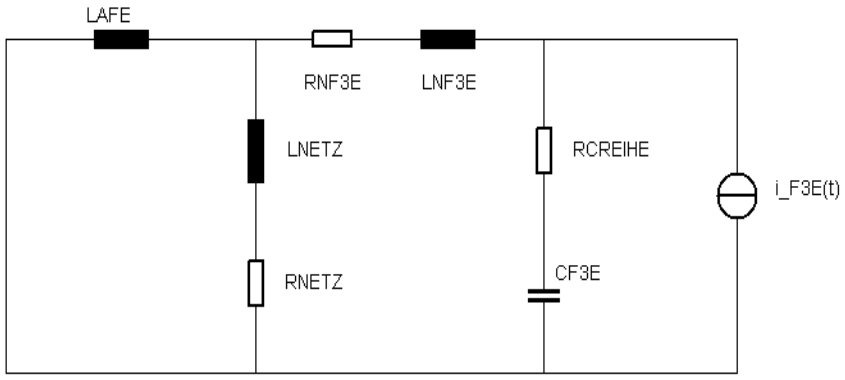


Fig. 5.3: Alternate circuit for analysing the current source effects

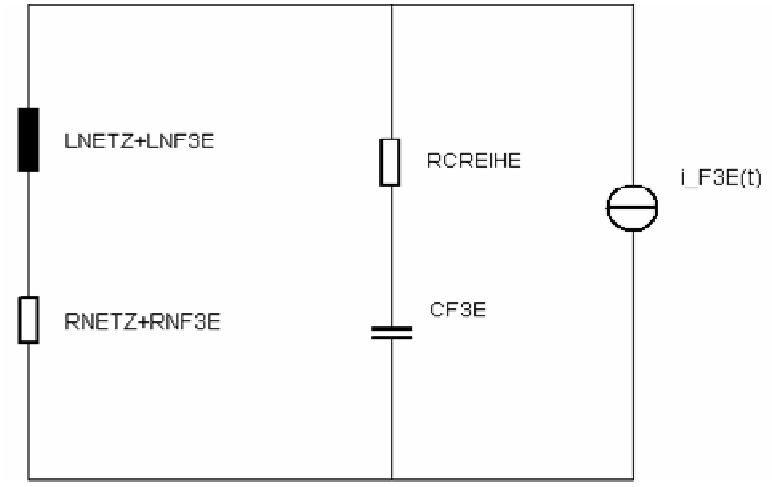


Fig. 5.4: The resulting alternate circuit with mains components in serial configuration and trap circuit

It can be concluded that the influences on external components produced by the F3E under operating conditions are similar to those pointed out in Chapter 4.

5.1.2 Influence of the AFE on the AFE_F3E model

Examining the alternate circuit diagram (Fig. 5.2) from the AFE point of view, or to be more precisely, from the point of view of the voltage source u_AFE(t) substituting for the AFE, the current source i_F3E(t) was simply removed, and the voltage source U_grid, short circuited (Fig. 5.5).

In this alternate circuit diagram (Fig. 5.5), two major resonant circuits can be identified. These were examined starting with the series resonant circuit consisting of R_{NF3E}, L_{NF3E}, R_{CREIHE}, and C_{F3E}.

In case of the resonance, only the active resistance was relevant (Eq. 5.1).

$$Z_0 = R_{NF3E} + R_{RCREIHE} \qquad \text{Eq. 5.1}$$

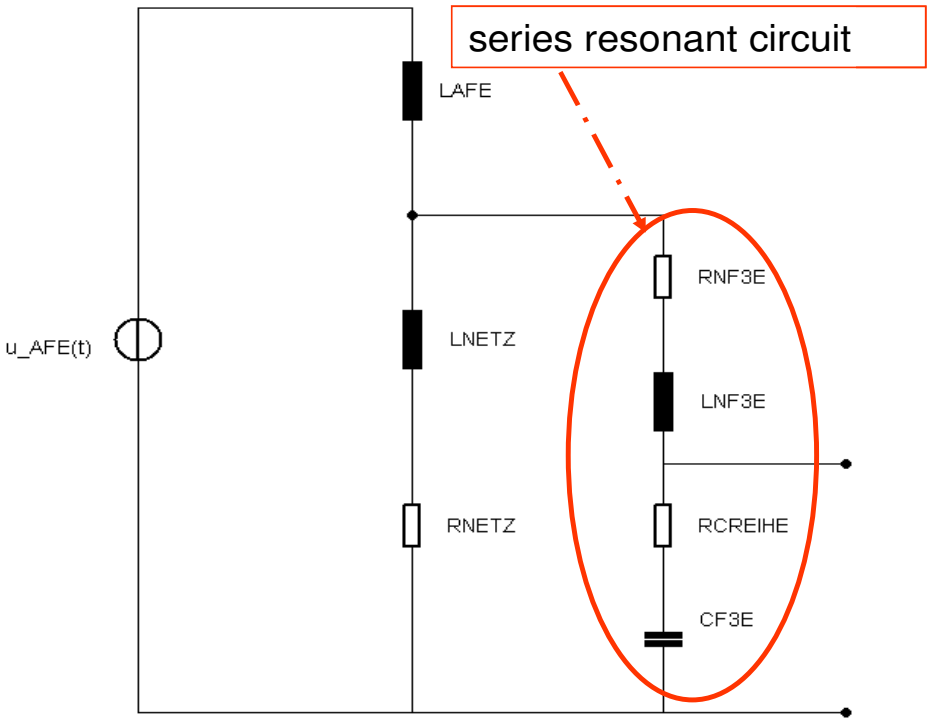


Fig. 5.5: Alternate circuit with resonant circuit

The topology shown in Fig. 5.5 suggests that the resonant circuit can result in an effective resistance smaller than that of the components of mains circuit L_{NETZ} and R_{NETZ}. This is true in case of moderate short circuit power in comparison with the active power of the load connected to the mains (R_{sce}<200). At 50Hz, the line impedance, consisting of L_{NETZ} and R_{NETZ}, was significantly smaller than the impedance of the series-resonant circuit. At higher frequencies, the inductive component of the line impedance increased (Eq. 5.2) and exceeded the value of Z_0.

$$X_{LNETZ} = 2 \cdot \pi \cdot f \cdot L_{NETZ} \qquad \text{Eq. 5.2}$$

As a result, the higher harmonics close to the resonant frequency were not conducted by the mains components L_{NETZ} and R_{NETZ}, but by the resonant circuit. Since the AFE in this configuration had a rated power 10 to 15 times that of the F3E, the current through the F3E filter components could exceed the rated current of these components despite the inductor L_{AFE}. A further risk to the components is the resulting voltage increase within the resonant circuit. The capacitor voltage U_{CF3E} and the inductor voltage U_{LNF3E} cancel each other out; although, within the resonant circuit, these two voltages might still exceed voltage applied to the resonant circuit, depending on its quality Q (Fig. 5.6). This might also pose a risk to the filter. The veracity of this assumption was examined subsequently.

The second resonant circuit is formed by the mains components R_{NETZ} and L_{NETZ}, and

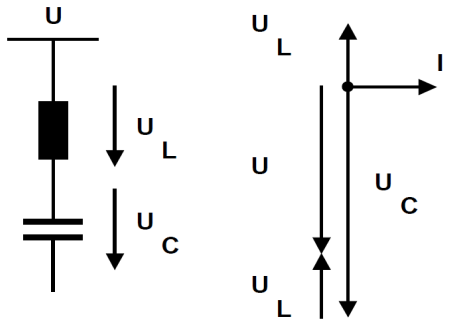


Fig. 5.6: Voltage vector diagram of a resonant circuit in case of resonance (Dib, 2009)

the capacitor of the series resonant circuit. For frequencies below the resonant frequency f_{r0} of the series resonant circuit, the series resonant circuit behaved like a capacitor to any connected circuitry (Fig. 5.7).

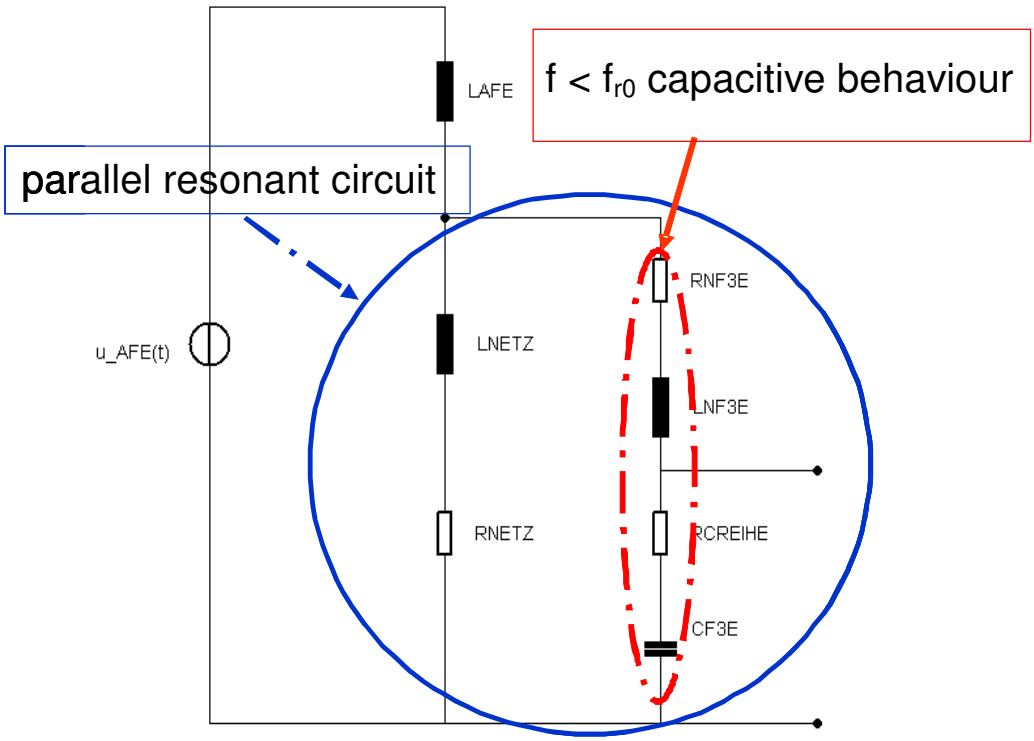


Fig 5.7: Alternate circuit diagram with parallel resonant circuit

This could result in increased currents within the parallel resonant circuit. In comparison with the active component R_{NETZ}, the large dampening resistor of the F3E filter reduced the quality Q significantly. It also limited the currents in case of resonance. It is still possible, however, that due to a large difference in rated power between the AFE and the F3E, currents which exceed the rated values of single components of the circuitry might occur. Therefore, the possible occurrence of disturbances was examined.

To further assess the complete model, the possible areas of disturbance due to resonant circuits were investigated. The model was also examined for operation outside these areas of disturbance. These two situations were compared with each other in order to determine the effects of the areas of disturbance on the system described by the model.

5.2 Simulation of the model outside the areas of disturbance

5.2.1 Model parameters for the simulation

The model was first simulated under secure operating conditions. This was done in order to be able to compare the results of investigation under the influence of disturbances with the ones obtained under secure operating conditions. Secure conditions in this context are defined as a non-occurrence of resonance frequencies. This can be done by selecting mains parameters, which do not form resonant circuits with resonant frequencies, close or identical to the switching frequencies of the equipment connected to the power grid. To achieve this, the switching frequency of PWR was set to 16kHz. This switching frequency was also used in examining the two areas of disturbance. The main emphasis was on the examination of the effects of AFE addition. The AFE switching frequency was set to 4kHz, and the AFE inductance was set to a value equal to four percent of the load impedance. The AFE current was calculated according to Eq. 5.3 with the assumption that the apparent power of the AFE is equal to the rated active power.

$$I = \frac{P}{\sqrt{3} \cdot U} = \frac{200kW}{\sqrt{3} \cdot 400V} = 288A \qquad \text{Eq. 5.3}$$

The current calculated according to Eq. 5.3 is equal to the inductor current. In order to calculate the value of the inductor, a voltage of 230V was used since only the line inductance had to be calculated and not the total inductance (Eq. 5.4).

$$L = \frac{\frac{U}{I} \cdot 4}{2 \cdot \pi \cdot 50Hz} = \frac{\frac{230V}{288A} \cdot 0.04}{2 \cdot \pi \cdot 50Hz} = 0.102\mu H \qquad \text{Eq. 5.4}$$

The impedance of the complete mains grid was calculated based on an R_{sce} of 750 (Eq. 5.5) and the impedance of F3E sub-section based on a R_{sce} of 500. By definition, this impedance qualifies as a rigid system.

$$Z_k = \frac{U^2}{S_k} = \frac{U^2}{R_{sce} \cdot P_{total}} = \frac{400V^2}{750 \cdot 216kVA} = 0.987m\Omega \quad \text{Eq. 5.5}$$

Furthermore, the quotient between the active resistance and the inductive resistance was set to a small value. In other words, the grid appears mainly as an inductive system.

The mains parameters R_{NETZ} and L_{NETZ} were calculated using Eqs. 5.6 to 5.8, resulting to a quotient of 0.1.

$$R_{NETZ} = Z_k \cdot 0.1 = 0.0987m\Omega \quad \text{Eq. 5.6}$$

$$X_{LNETZ} = \sqrt{Z_k^2 - R_{NETZ}^2} = 0.982m\Omega \quad \text{Eq. 5.7}$$

$$L_{NETZ} = \frac{X_{LNETZ}}{2 \cdot \pi \cdot 50Hz} = 3.145\mu H \quad \text{Eq. 5.8}$$

In the F3E sub-section, the quotient between active and inductive resistance was set to a value of 0.15. This sub-section was not supposed to be inductive, hence the slight increased in the quotient. Values for R_{NF3E} and L_{NF3E} were computed using Eqs 5.9 to 5.12.

$$Z_{kF3E} = \frac{U^2}{S_k} = \frac{U^2}{R_{sce} \cdot P_{F3E}} = \frac{400V^2}{500 \cdot 16kVA} = 20m\Omega \quad \text{Eq. 5.9}$$

$$R_{NF3E} = Z_{kF3E} \cdot 0.15 = 3\text{m}\Omega \quad \text{Eq. 5.10}$$

$$X_{LNETZ} = \sqrt{Z_{kF3E}^2 - R_{NF3E}^2} = 19.77m\Omega \quad \text{Eq. 5.11}$$

$$L_{NF3E} = \frac{X_{LNF3E}}{2 \cdot \pi \cdot 50Hz} = 62.9\mu\text{H} \quad \text{Eq. 5.12}$$

Additionally, the dampening resistor of the F3E-filter was set to a value of 330mΩ.

5.2.2 Analysis of simulation results

As expected, the simulation with these parameters resulted in undisturbed shapes for the currents and voltages of the whole system.

Figure 5.8 shows that only the mains current deviated from the idealised sinusoidal shape. Figure 5.9 shows the AFE current I_{LAF} through the inductor L_{AFE} and the AFE input voltage. The influence of the AFE current on the mains current can be seen by

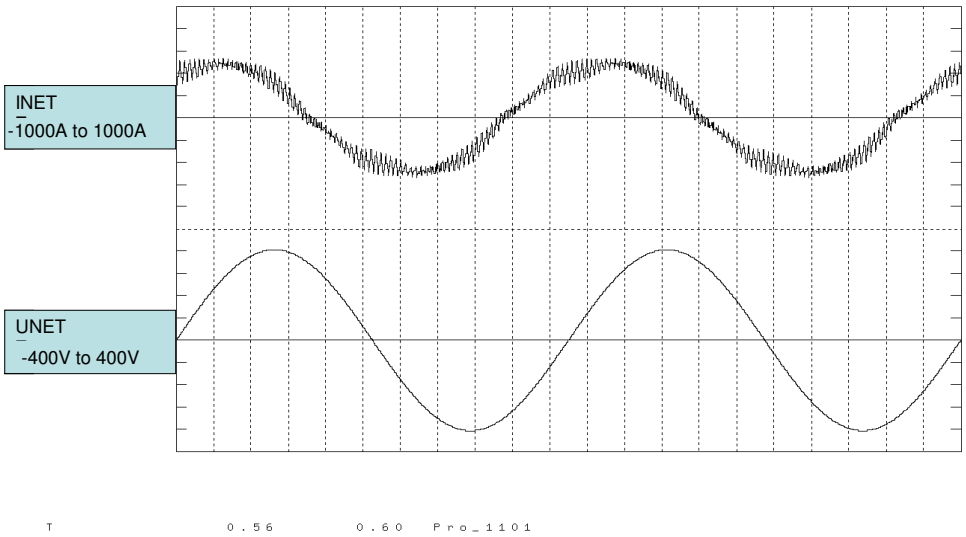


Fig. 5.8: Shapes of mains current and voltage

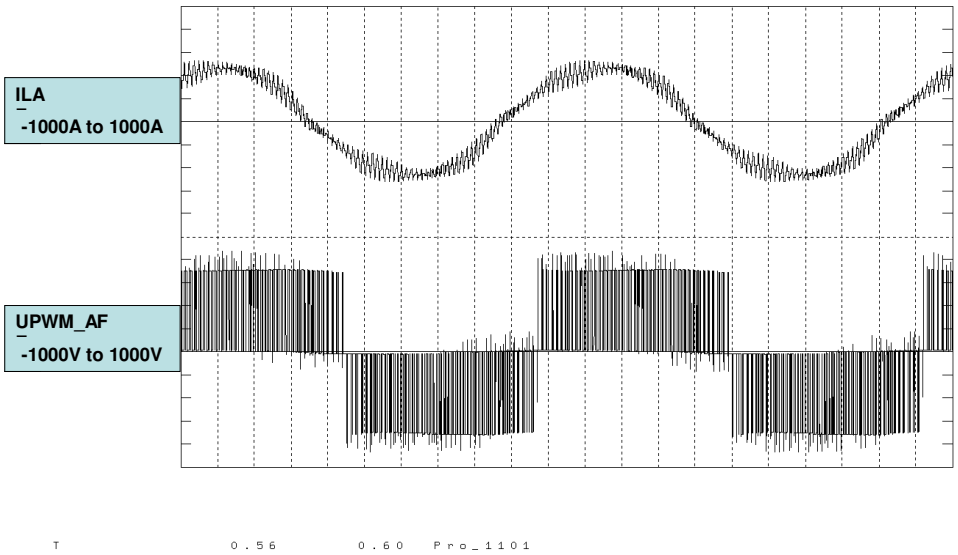


Fig. 5.9: Shapes of the inductor current I_{LAF} of the AFE and input voltage U_{PWM_AFE}

comparing current shapes.

Within the shape of the input voltage of the AFE, the pulse patterns typical for PWM operation can be identified. The inductor current, similar to the input current, shows a superimposed ripple. In contrast, the currents and voltages of the F3E had only very limited influence on the voltage and current shapes of the whole model.

The voltage and currents shown in Fig. 5.10 display only the ordinary shapes found with an F3E operating under normal conditions. They define what is later referred to as normal operation.

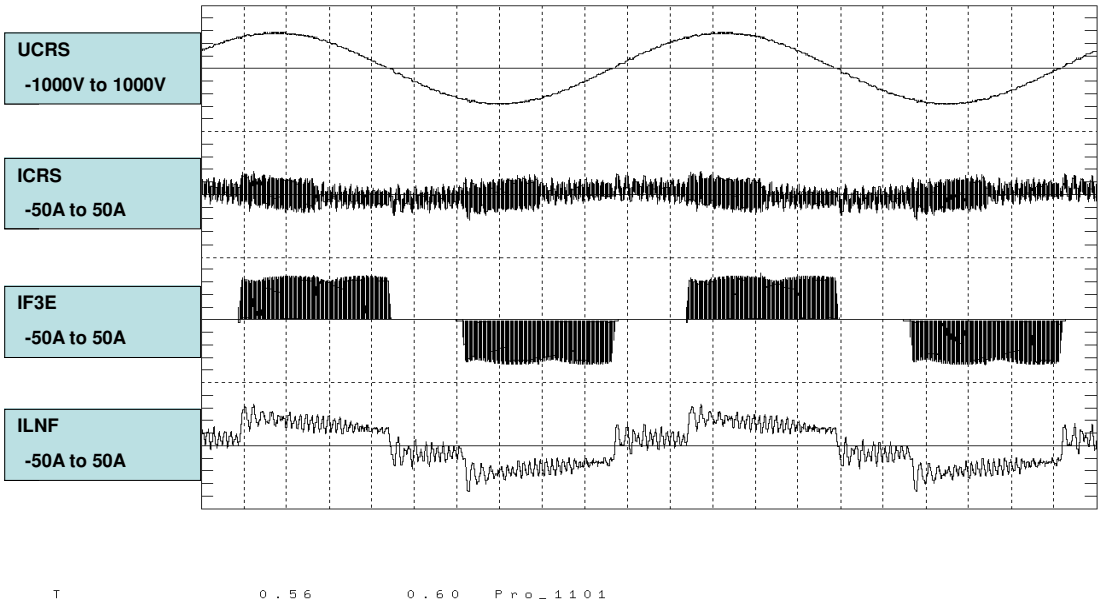


Fig. 5.10: Shapes of the F3E input voltage and currents (filter voltage U_{CRS}, filter current I_{CRS}, F3E current without filter I_{F3E}, and F3E line current I_{LNF})

The frequency spectra of the following currents and voltages were examined:

- Line current and voltage (I_{NETZ} & U_{NETZ});
- Inductor current of the AFE (I_{LAF});
- F3E filter current and voltage (U_{CRS} & I_{CRS});
- F3E line current (I_{LNF}); and
- F3E input current (I_{F3E}).

The spectra of the line current I_{NETZ} and the inductor current I_{LAF} were analysed. The value range of these currents indicates that the line current is almost exclusively dominated by the AFE current. As such, the line current of the F3E was considered irrelevant and therefore, omitted.

Neither the inductor current nor the line current contained significant higher harmonics in the frequency range of up to 1.5kHz (Fig. 5.11). Therefore, the omission of the F3E current was apt, and did not distort the results in any discernible way. It can likewise be

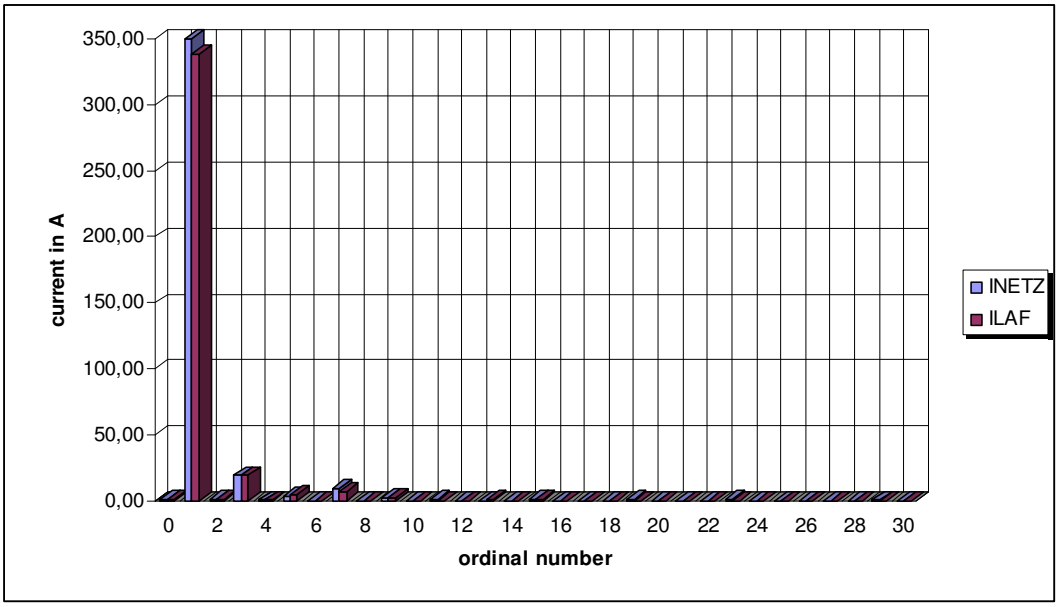


Fig. 5.11: Spectra of the lower range of higher harmonics of currents I_{LAF} and I_{NETZ}

concluded, that the AFE fulfilled its designed purpose and produced almost no higher harmonics in the range shown in Fig. 5.11.

Since the switching frequency of the AFE was set to 4kHz, a slight increase of higher harmonics in this range could be expected.

Figure 5.12 shows the higher harmonics spectra of the line current and inductor current of the AFE. A visible increase in higher harmonics can be noted starting from the 3.75kHz until the 4.25kHz range. The inductor current was also higher than the line current in this range. From these results, it can be assumed that the higher harmonics currents do not enter the sub-section of the power grid of the F3E. To verify this

assumption, the frequency range from 3.75kHz to 4.25kHz of the currents I_{F3E}, I_{LNF}, and I_{CRS} was analysed (Fig. 5.13).

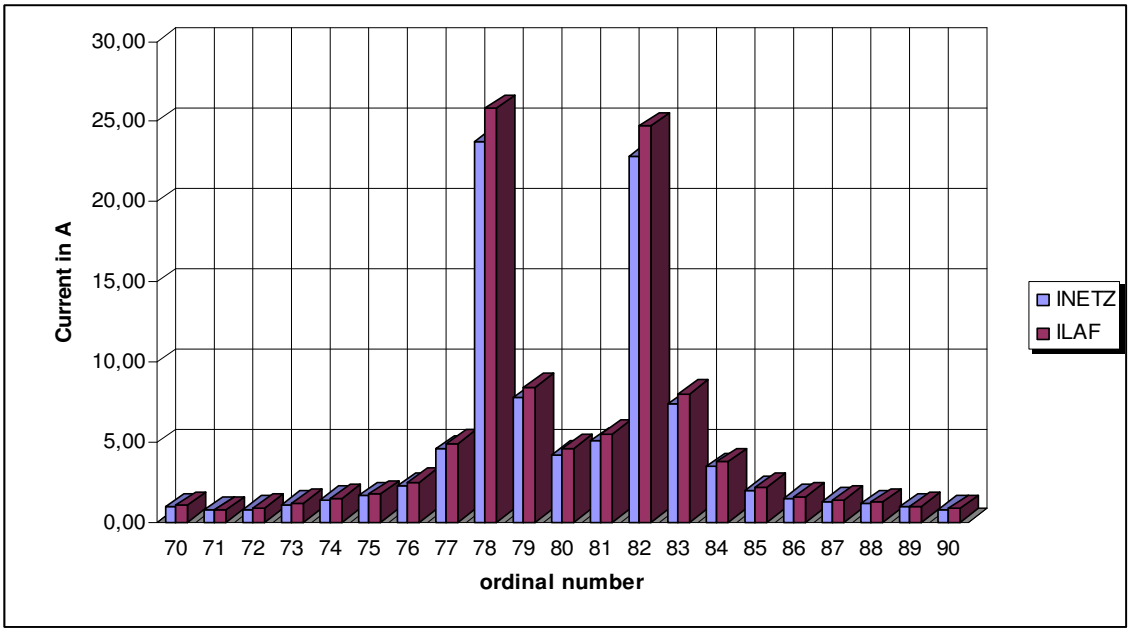


Fig. 5.12: Higher harmonics of I_{NETZ} and I_{LAF} in the frequency range 3.5kHz to 4.5kHz

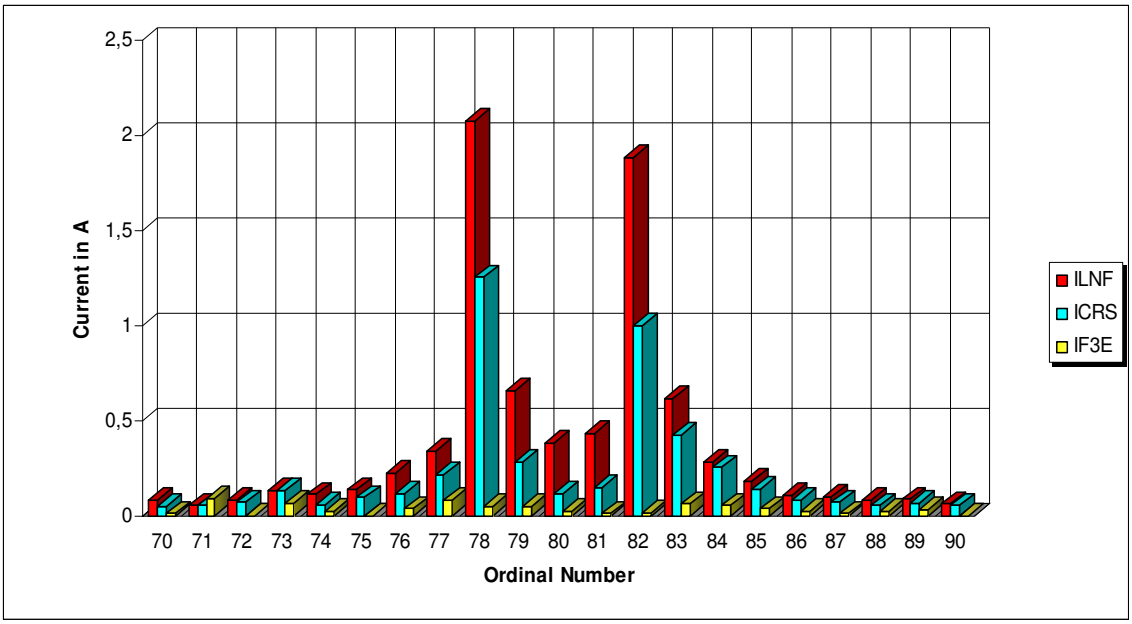


Fig. 5.13: Higher harmonics of the currents I_{LNF}, I_{CRS}, und I_{F3E}

The currents I_{LNF} and I_{CRS} show distinct enlarged values within this frequency range. In contrast, the value of the F3E current was small. This indicates that only a part of higher harmonics of the AFE current propagated through the sub-section of the power grid of the F3E, thereby, entering its input filter. This is further confirmed by comparing the higher harmonics of the current model with the model F3E_PWR, which is basically the same model, but without the AFE (Fig 5.14).

Figure 5.14 clearly shows that the enlarged currents observed in Fig. 5.13 were not generated by the F3E, but were actually part of the higher harmonics produced by the AFE. The F3E itself generates only a few milli-amperes of higher harmonics content. Therefore, the F3E filter will experience additional stress due to higher harmonics present in the power grid.

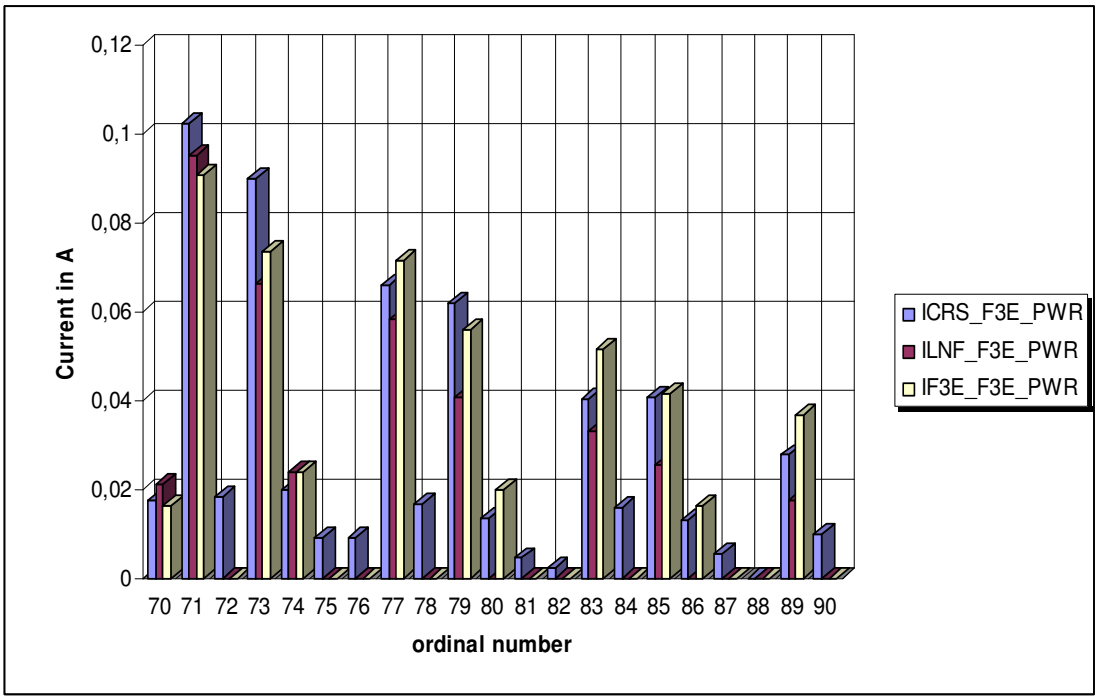


Fig. 5.14: Higher harmonics of the currents I_{CRS}, I_{LNF}, and I_{F3E} of the model without AFE

In these two cases, the comparison of the effective values of the two F3E filter currents I_{CRS} shows only a difference of less than 230mA.

ICRS AFE_F3E	ICRS F3E_PWR
7.099A	6.864A

The difference in the spectra of the higher harmonics was noticeable, but can be neglected.

5.3 Model simulation in areas of expected disturbance

Similar to that of normal operating conditions, the areas of expected disturbance were examined. The first area of expected disturbed operation was defined by the resonant frequency of the series resonant circuit (Fig. 5.5), and the second, by that of the parallel resonant circuit (Fig. 5.7).

5.3.1 Operation with the resonant frequency of series resonant circuit

The model behaviour under stimulation with the series resonant frequency mentioned in Chapter 5.1.2 was analysed. The switching frequencies remained unchanged. As such, the spectra of the AFE and F3E in case of resonance could be compared with the spectra analysed for normal operating conditions. The value for the AFE inductor L_{AFE} likewise, did not change. The parameter of the F3E mains sub-net, however, was modified to generate a resonant frequency of 4kHz in conjunction with the F3E filter components. The inductive component of the F3E sub-net was calculated according to Eq. 5.13.

$$f_0 = \frac{1}{2\pi \cdot \sqrt{L_{NF3E} \cdot C_{F3E}}} \qquad \text{Eq. 5.13}$$

Since the capacitor C_{F3E} and the resonant frequency f_0 were known, the equation could be transformed into Eq. 5.14.

$$L_{NF3E} = \frac{1}{(2 \cdot \pi \cdot f_0)^2 \cdot C_{F3E}} = 26.4\mu H \qquad \text{Eq. 5.14}$$

The active component R_{NF3E} of the F3E sub-net was set to 3mΩ to ensure that the sub-net will not behave too rigidly. These parameters (capacitor and resistor) remain unchanged throughout this part of the study.

The parameters for the mains grid, L_{NETZ} and R_{NETZ}, were varied via the quotient R_{sce} of the total short circuit power in relation to the total rated power. The value of R_{sce} ranged from 33 to 750. The results for the lower and upper boundary were analysed in detail.

5.3.2 Analysis of the resulting current shapes

The lower boundary with R_{sce}=33 was examined first. A significant change in the shape of line current I_{LNF} in the F3E sub-net is visible (Fig. 5.15) as compared with the shape illustrated in Fig. 5.10 (Chapter 5.2). Not only was the line current distorted, but its

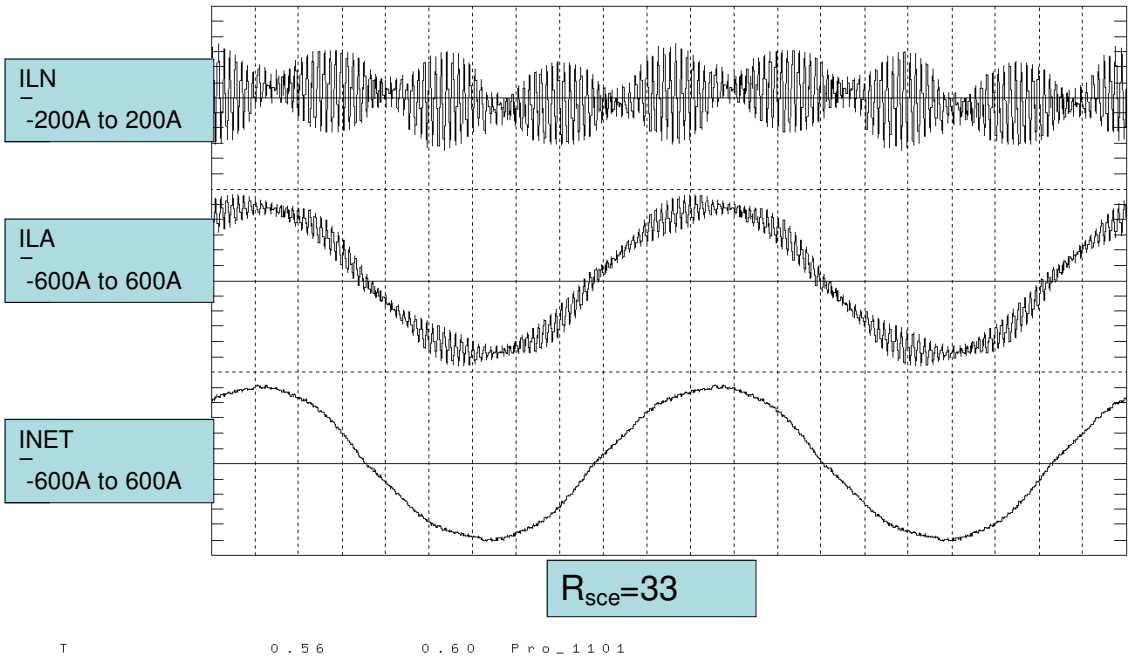


Fig. 5.15: Shapes of grid currents I_{LNF}, I_{LAF}, and I_{NETZ}

range also increased four times from $\pm 50A$ to $\pm 200A$. Whereas the grid current I_{NETZ} showed very little harmonic distortion, nearly the whole harmonic current of the AFE was taken up by the F3E filter. The quotient R_{sce} refers to the total rated power of the whole system. Thus, in comparison with the AFE, the mains grid appeared to be very rigid from the F3E point of view. Since the difference in rated power between the two components was about 10, the resulting R_{sce} from the F3E point of view equalled 300. This figure is in excess of the recommended value of 100 (Göpfrich, 2006).

The shapes of the F3E current I_{F3E}, the filter current I_{CRS}, and the line current I_{LNF} are shown in Fig. 5.16. A significant share of the current increase was taken up by the filter. This is indicated by the four-fold increase of the range of the filter and line current,

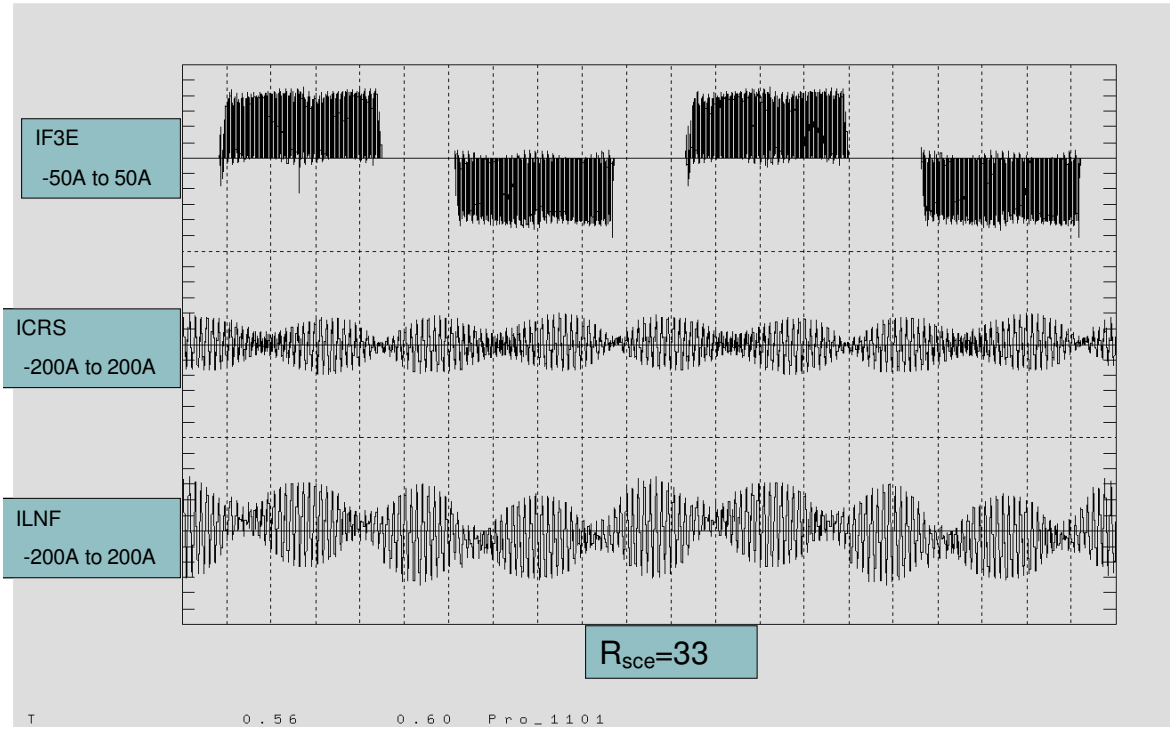


Fig. 5.16: Shapes of the F3E input currents I_{F3E}, I_{CRS}, and I_{LNF}

respectively, in comparison with the shapes shown in Fig. 5.10. Compared with that figure, the F3E current I_{F3E} was within the normal range of this power class. The range of values ($\pm 50A$) was similar to that in Fig. 5.10.

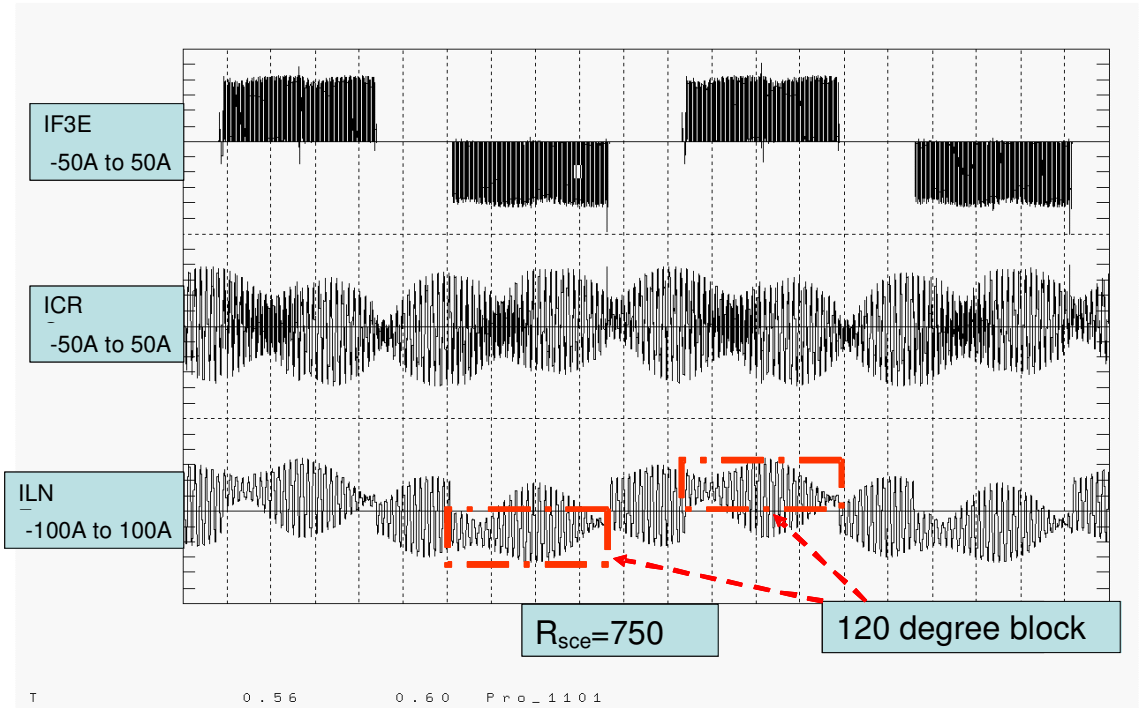


Fig. 5.17: Shape of the F3E input currents I_{F3E}, I_{CRS}, and I_{LNF} with an R_{sce}=750

A decrease of the values for L_{NETZ} and R_{NETZ}, constituting the mains impedance, or an increase of the R_{sce} value showed an improvement in the current shapes of I_{LNF} and I_{CRS}. The range of their values, though, might still be considered excessive (Fig. 5.17).
The filter current was within the same value range as the F3E current I_{F3E}. It was, however, still twice as large as that under normal operating conditions shown in Fig. 5.10. In comparison with Fig 5.15, the F3E line current showed the 120 degree blocks at an R_{sce}=750 even more clearly. The higher harmonics spectra were analysed to achieve a more detailed analysis of the operation of the model under resonant conditions.

5.3.3 Analysis of the resulting higher harmonics

From the previous analysis (Chapter 5.3.2), it can be assumed that the sub-net components R_{NF3E}, L_{NF3E}, and the filter components of the F3E will experience a higher level of stress due to higher currents and the resulting losses. To corroborate this assumption, the higher harmonics range of the currents I_{LNF} and I_{CRS} were compared with that of the F3E current I_{F3E}. Analogous to the preceding chapter, the case studies with R_{sce}=33 and R_{sce}=750 were analysed. Both currents I_{LNF} and I_{CRS} showed increased values as compared with the case examined in Chapter 5.2 (Fig. 5.10). The higher

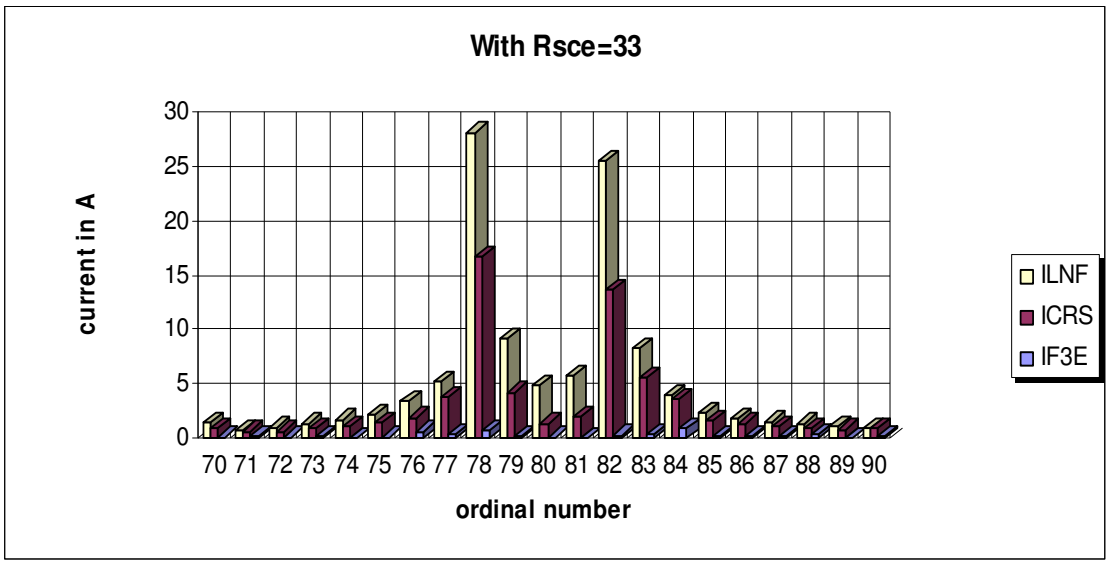


Fig. 5.18: Higher harmonics range of the F3E input currents from 3.5kHz to 4.5kHz for an R_{sce}=33

harmonics currents from 3.9kHz to 4.1kHz (Fig. 5.18) exceeded the values of the higher harmonics in Chapter 5.2 by one magnitude. This led to an increase in the actual values for both currents. The actual values for both currents were:

$$I_{LNFrms} = 46.0\text{A}$$

$$I_{CRSrms} = 25.6\text{A}$$

An increase of R_{sce} to 750 led to a decrease in the values of the higher harmonics (Fig 5.19). The higher harmonics currents from 3.9kHz to 4.1kHz significantly decreased by a factor of almost 0.5. This reduction results from the fact that with an increasing R_{sce}, the line impedance decreases. This also leads to a decrease of the line inductor L_{NETZ}, which is dominating the line impedance, giving it a primarily inductive behaviour. The reactance of the inductor also increases with frequency. The increase, however, is also reduced by lowering the value of the inductor itself. This, in turn, results into a shift of the higher harmonics currents around the resonant frequency into the mains grid as seen by comparing Figs 5.20 and 5.21. Both diagrams show the line current I_{NETZ}, the inductor current I_{LAF}, and the F3E input current at a frequency range from 3.5kHz to 4.5kHz.

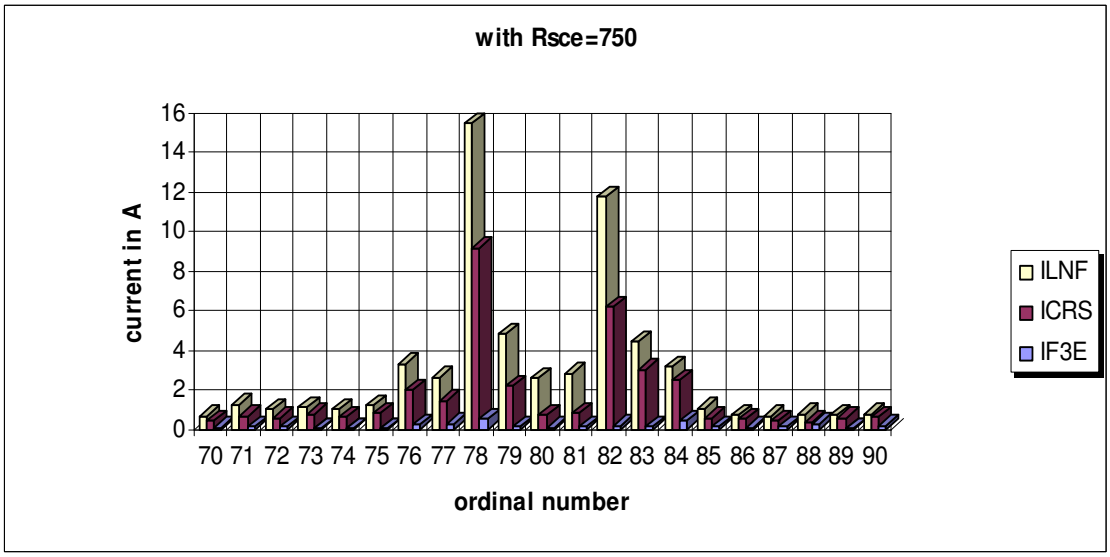


Fig. 5.19: Higher harmonics range of the F3E input currents from 3.5kHz to 4.5kHz for an R_{sce}=750

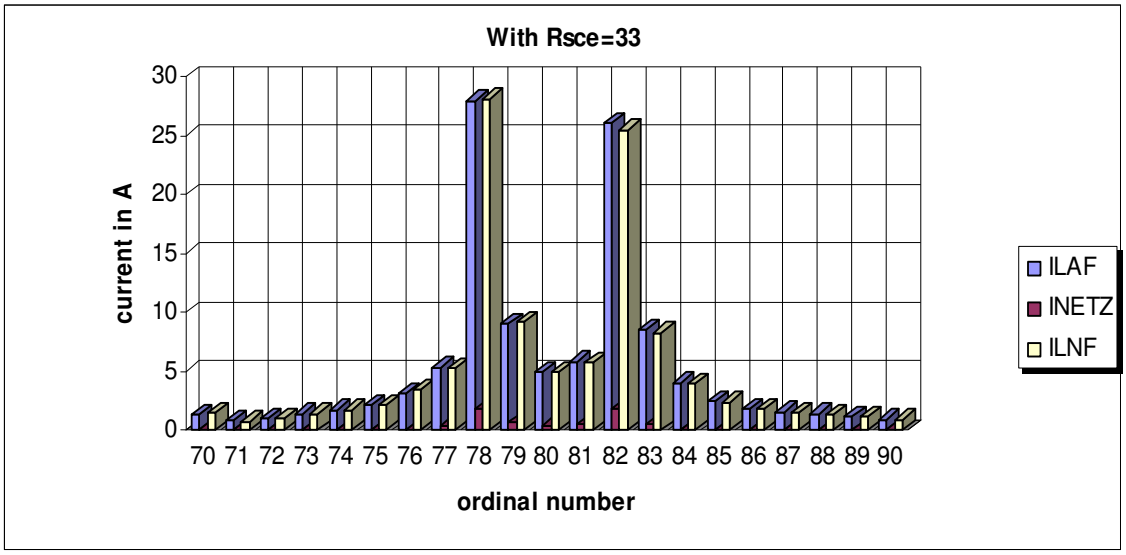


Fig. 5.20: Higher harmonics range of the currents I_{NETZ}, I_{LAF}, and I_{LNF} from 3.5kHz to 4.5kHz for an R_{sce}=33

In Fig. 5.20, the line current I_{NETZ} was only one-tenth of the value of the other two currents I_{LAF} and I_{LNF}. With an increase in $R_{sce,}$ the current I_{NETZ} also increased. Figure

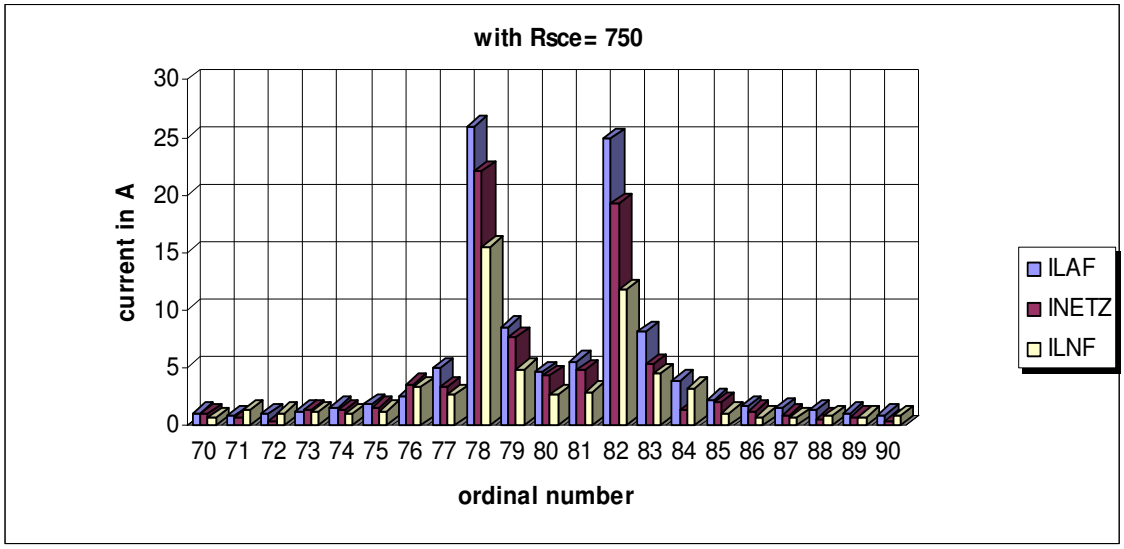


Fig. 5.21: Higher harmonics range of the currents I_{NETZ}, I_{LAF}, and I_{LNF} from 3.5kHz to 4.5kHz for an R_{sce}=750

5.21 shows the same currents as Fig. 5.20 at an R_{sce}=750. In that case, I_{NETZ} was even larger than I_{LNF}.

Figure 5.22 presents the 38th harmonic of the currents I_{LAF}, I_{NETZ}, and I_{LNF} as a function

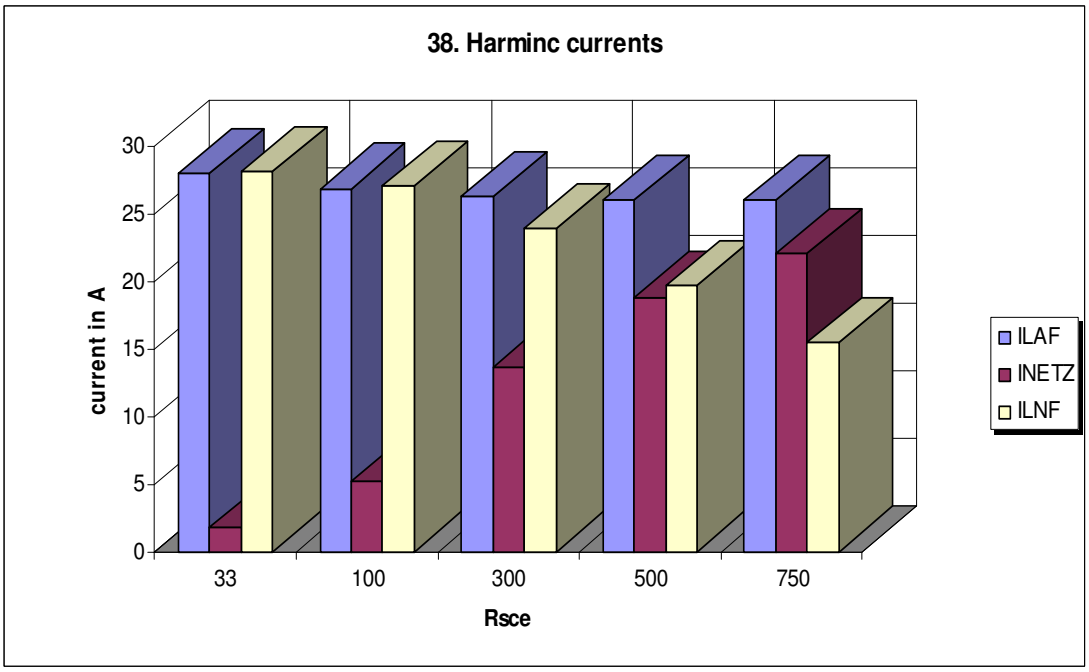


Fig. 5.22: The I_{LAF}, I_{NETZ}, and I_{LNF} of the 38th harmonic as a function of R_{sce}

of R_{sce}. The AFE current I_{LAF} hardly changed; whereas, I_{LNF} decreased starting at an R_{sce} of 300. From this point on, the line impedance at 4kHz was smaller than the impedance of series resonant circuit. The behaviour of the line current I_{NETZ} was inverse to that of I_{LNF} for the same reason, and showed a steady increase.

These changes in the higher harmonics range affected the actual values of the three currents. The effect on the line current I_{NETZ}, however, can be disregarded since its fundamental component is dominating the current shape and value. In contrast, the fundamental components of the current I_{F3E} in the F3E sub-net and the F3E filter current I_{F3E} are relatively small, thus the occurring resonant frequency has no influence on the intermediate circuit. Thus, changes in the higher harmonics of these currents have a significant impact on their actual values.

The decrease of the actual value of the filter current I_{CRS} is shown in Fig. 5.23. The last value showed the filter current under the normal operating conditions stated in Chapter 5.2. At an R_{sce}=750, however, the filter current value was still twice the value of operations without any resonant effects, or normal operation.

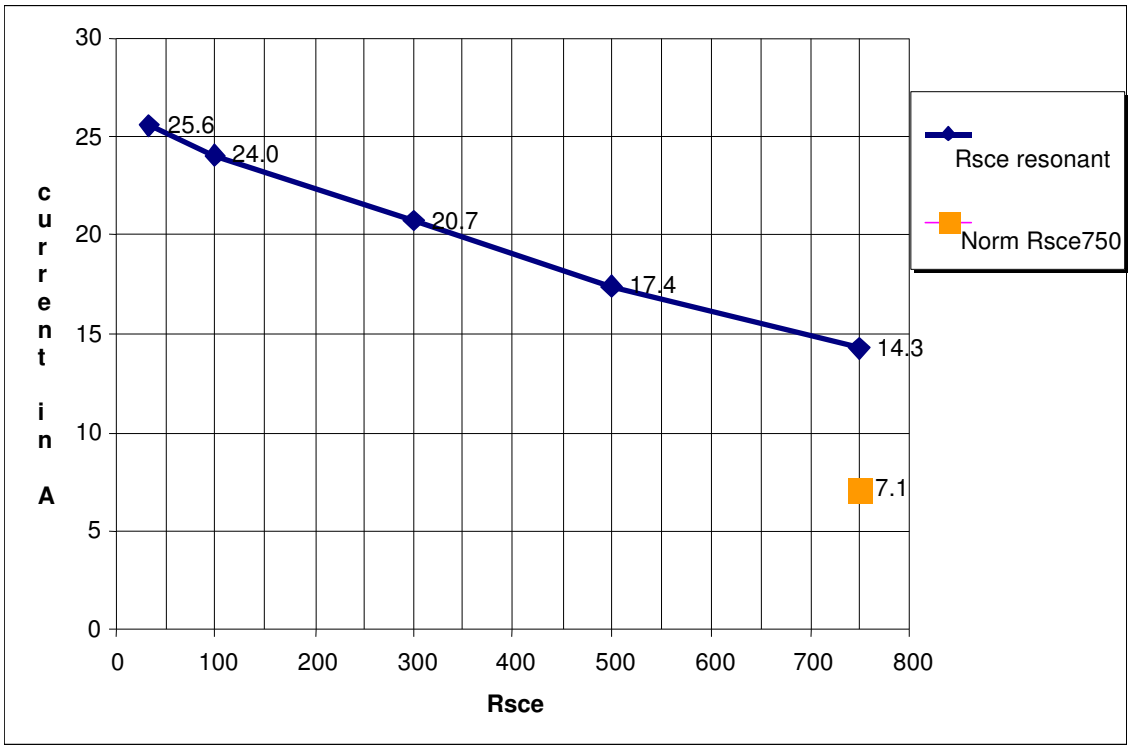


Fig. 5.23: Actual value of the filter current I_{CRS}

Figure 5.24 illustrates an extension of Fig. 5.23 with the inclusion of the currents I_{LNF} and I_{F3E}. It can be seen that the F3E input current I_{F3E} was almost constant (red line), corroborating the behaviour shown in Figs 5.16 and 5.17. The filter current I_{CRS} decreased below the value of I_{F3E} at a R_{sce}=500 and above.

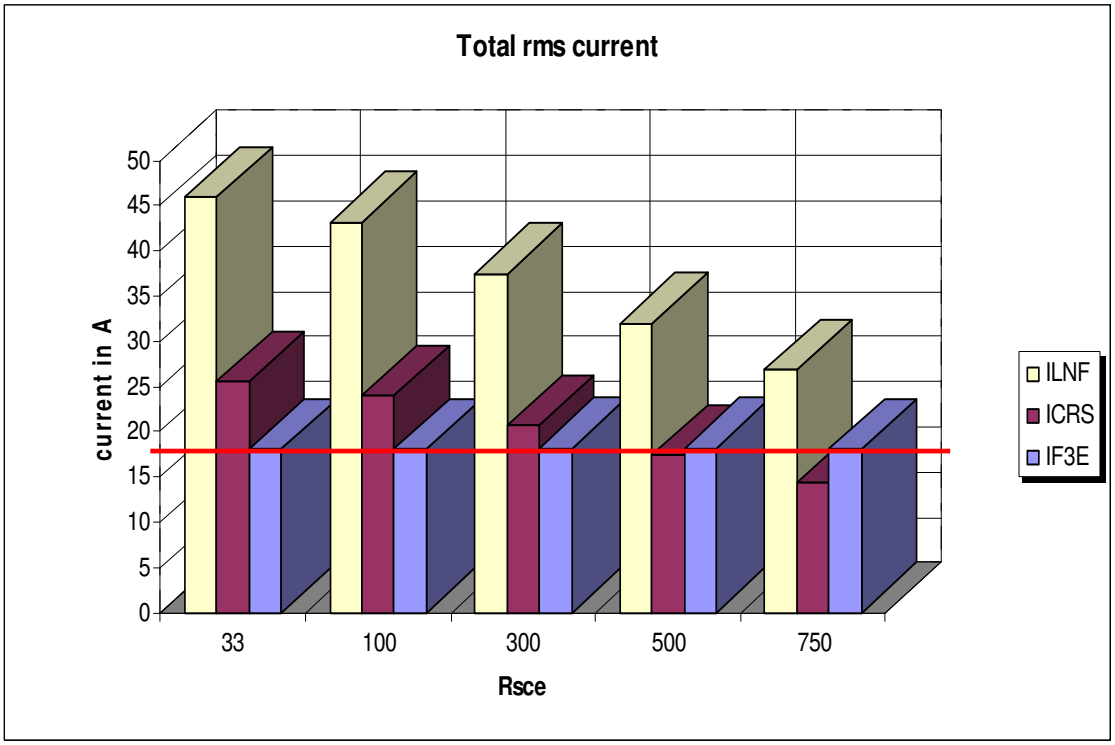


Fig. 5.24: Actual value of the currents I_{LNF}, I_{CRS}, and I_{F3E} at an R_{sce} from 33 to 750

The possibility of voltage increases within the series resonant circuit was brought up in Chapter 5.1. A closer analysis of the results reveals, however, that the voltage increase in case of resonance does not pose a serious problem (Fig 5.25). The voltage U_{CRS} increased to about 410V at an R_{sce} of 33. This voltage value is within the stipulated allowed voltage fluctuations of low voltage mains networks. It, therefore, poses no risk to the filter components of the F3E.

5.3.4 Operation at parallel resonant frequency

The behaviour of the model under operation with resonant frequency was examined. The parallel resonant frequency for the alternate circuit shown in Fig. 5.7 should be

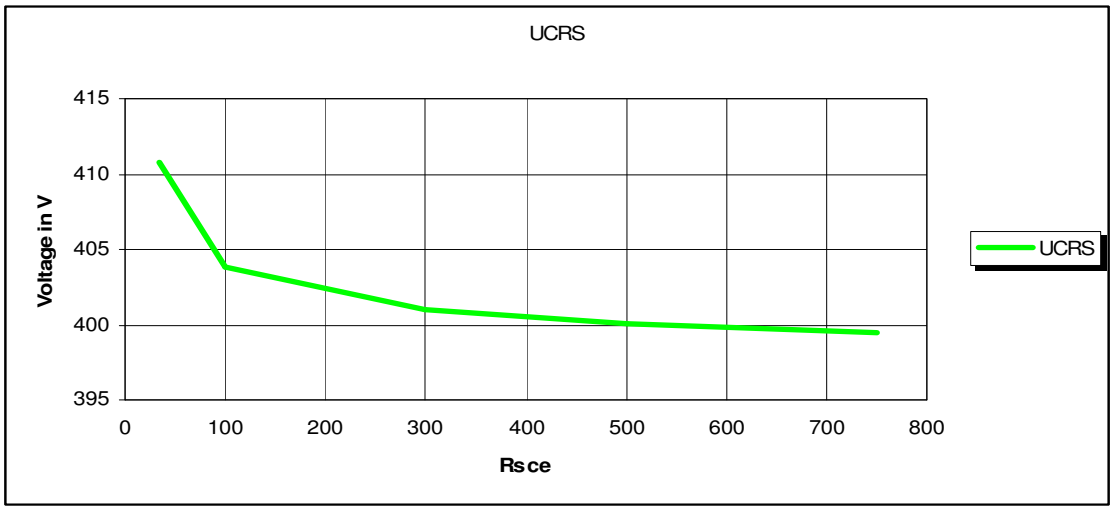


Fig. 5.25: Actual value of capacitor voltage U_{CRS} as a function of R_{sce}

lower than the series resonant frequency described in Chapter 5.1.2. This is because the series resonant circuit shows inductive properties for frequencies above its resonant frequency. Therefore, further points of resonance are not possible above its resonant frequency.

This fact was considered in the selection of the proper simulation parameters. In the succeeding case studies, the filter components were left unchanged as before. The line inductor of the F3E sub-net, however, was changed to create a parallel resonance at 4kHz in conjunction with the mains inductor used in Fig. 5.7. In this configuration, the electrical susceptance of the inductive and capacitive components of the circuit were calculated according to Eqs. 5.15.to 5.18.

$$B_{Par} = B_1 + B_2 = 0 \qquad \text{Eq. 5.15}$$

Equation 5.15 shows another way the same fact can be stated.

$$B_1 = -B_2 \qquad \text{Eq. 5.16}$$

Equations 5.16 and 5.17 are valid for the susceptances used in Fig. 5.6.

$$B_1 = \frac{1}{2 \cdot \pi \cdot f \cdot L_{NETZ}} \qquad \text{Eq. 5.17}$$

$$B_2 = \frac{1}{2 \cdot \pi \cdot f \cdot L_{NF3E} - \frac{1}{2 \cdot \pi \cdot f \cdot C_{F3E}}} \qquad \text{Eq. 5.18}$$

Based on Equation 5.16, the last two equations can, therefore, be expressed as:

$$\frac{1}{2 \cdot \pi \cdot f \cdot L_{NETZ}} = \frac{1}{-2 \cdot \pi \cdot f \cdot L_{NF3E} + \frac{1}{2 \cdot \pi \cdot f \cdot C_{F3E}}} \qquad \text{Eq. 5.19}$$

The transposition of Eq. 5.19 to the inductance L_{NETZ} results to Eq. 5.20.

$$L_{NETZ} = \left(\frac{1}{2 \cdot \pi \cdot f \cdot C_{F3E}} - 2 \cdot \pi \cdot f \cdot L_{NF3E} \right) \cdot \frac{1}{2 \cdot \pi \cdot f} \qquad \text{Eq. 5.20}$$

In order to calculate the components parameters, the value of f was set to the resonant

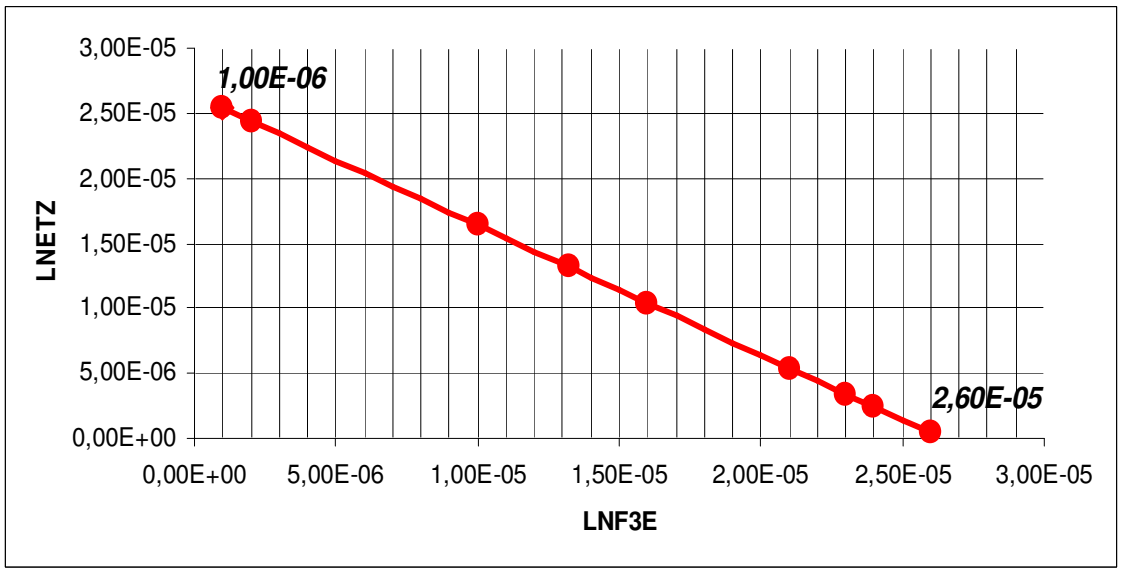


Fig. 5.26: The selected value combinations for L_{NF3E} and L_{NETZ}

frequency of 4kHz. The range of values for the F3E sub-net inductance was set to a minimum value of 1µH and to a maximum value of 26µH. The relationship between the inductors L_{NF3E} and L_{NETZ} is shown in Fig. 5.26. This diagram was used to select different combinations of values for L_{NF3E} and L_{NETZ} (marked with red dots in the graph).

The active component of both sub-nets was kept constant to further restrict the range of possible mains configurations. Due to the change in L_{NETZ}, the value of R_{sce} also changed as can be seen in Fig. 5.27.

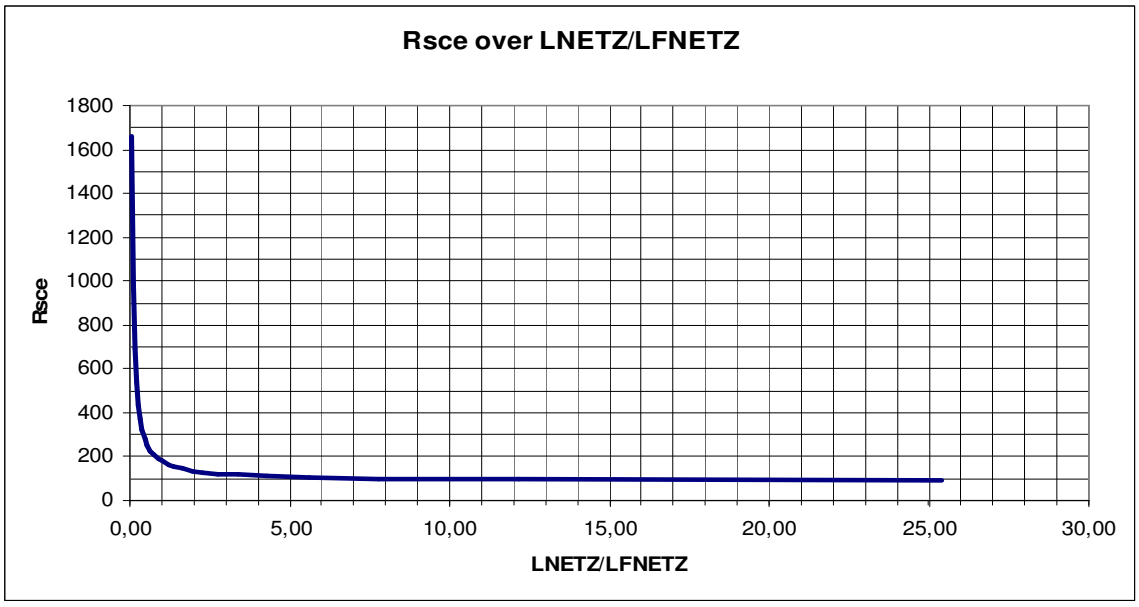


Fig. 5.27: The R_{sce} as a function of the quotient of L_{NETZ} over L_{NF3E}

Figure 5.27 shows that the minimum value of R_{sce} for the selected values of L_{NF3E} was slightly below 100. The only way to further reduce the value of R_{sce} is to increase the active component R_{NETZ} of the mains impedance. The minimum value of Rsce was 92. In the succeeding discussion, the selected value pairings of L_{NETZ} and L_{NF3E} will be explained in detail. The resulting values for R_{sce} ranged from 96 to 1164 (Table 5.1).

Table 5.1: Value pairings

R_{sce}	L_{NETZ}/H	L_{NF3E}/H
96	$2.44 \cdot 10^{-5}$	$2. \cdot 10^{-6}$
1164	$2.0 \cdot 10^{-6}$	$2.44 \cdot 10^{-5}$

5.3.5 Analysis of the current shapes for R_{sce}=96 and R_{sce}=1164

The shape of the current I_{LNF} in Fig. 5.28 shows distinct deviations from its known behaviour shown in Fig. 5.10. Its range of values was eight times higher than normal. Furthermore, the shape of the AFE-current I_{LAF} was different from the shape in Fig. 5.9. The current has an almost sinusoidal shape, but its range in values was significantly increased. In contrast, the shape of the line current I_{NETZ} was very similar to that in Fig 5.8; although, I_{NETZ} showed a much higher ripple than that in Fig 5.8 and that of the AFE current in Fig. 5.28. This is caused by the 4kHz oscillation of the parallel resonant circuit. However, the range of values increased, mainly due to the large difference in

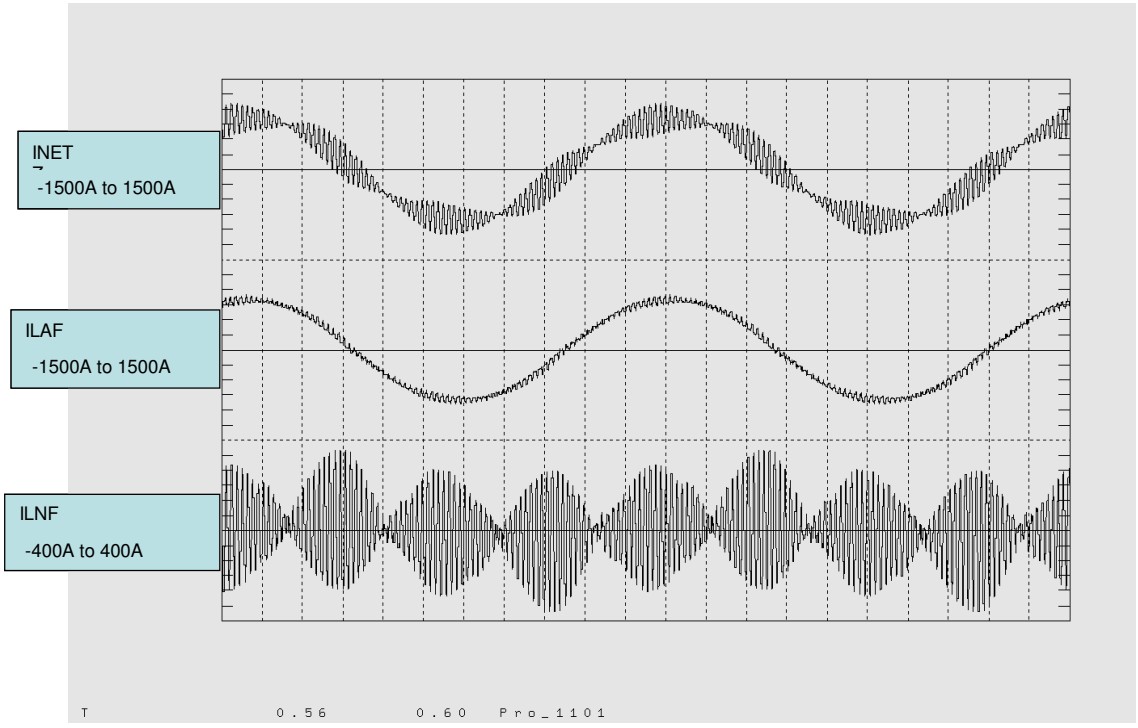


Fig. 5.28: Shape of the line currents at an R_{sce}=96

rated power between the AFE and the F3E. The influence on the input current I_{LNF} of the F3E was more significant than that of the AFE. This is again similar to the relationships between the currents explained in Chapter 5.3.2. Figure 5.29 shows the currents I_{LNF}, I_{CRS} and I_{F3E}. A large share of the current increase was taken up by the

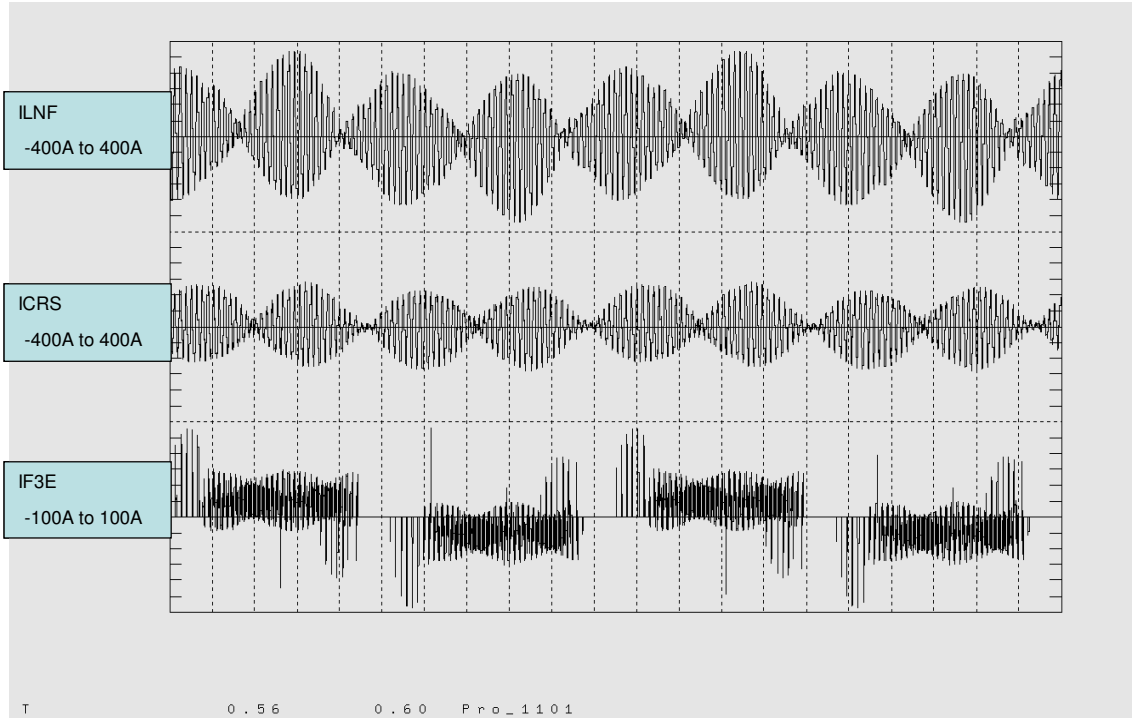


Fig. 5.29: Shape of the F3E currents at an R_{sce}=96

filter and the F3E current I_{F3E} was affected.

The typical 120 degree blocks can be discerned, but they showed a significant deviation when compared with their shape in Fig. 5.10. This deviation is caused by the filter voltage U_{CRS} shown in Fig. 5.30. The shape of the filter voltage U_{CRS} consisted of the sinusoidal shape of the mains voltage with a frequency of 50Hz superimposed by the voltage drop caused by the current I_{CRS}.

This voltage drop has repercussions on the intermediate voltage U_{CZK} (Fig. 5.31). The voltage shape still expressed the typical pulse pattern at a frequency of 300Hz caused by the rectifier topology and the mains frequency. The distorted filter voltage, however, caused large fluctuations in the intermediate voltage.

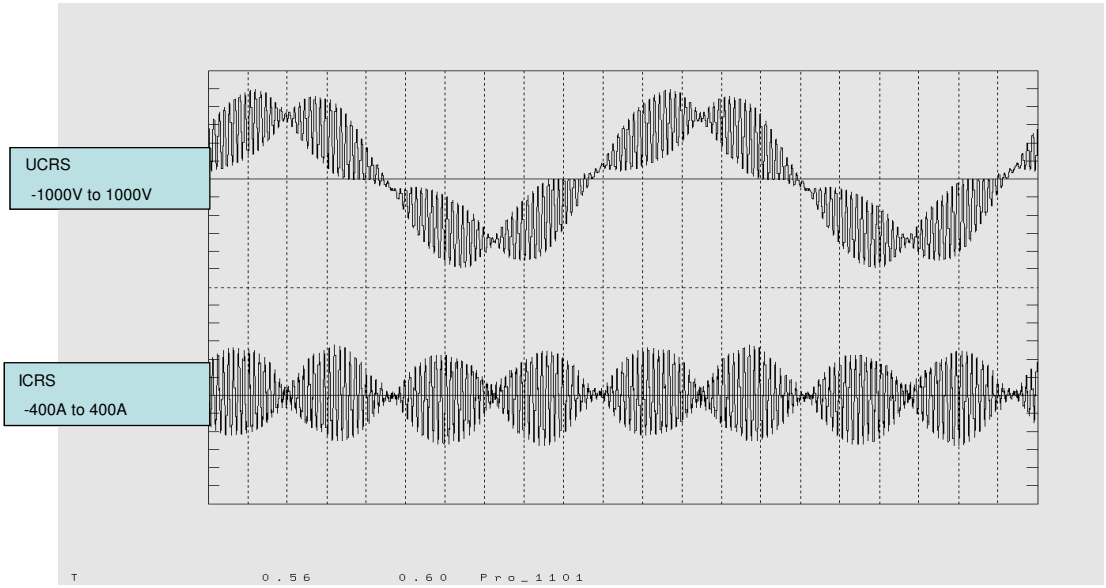


Fig. 5.30: Filter current I_{CRS} and filter voltage U_{CRS} at an R_{sce}=96

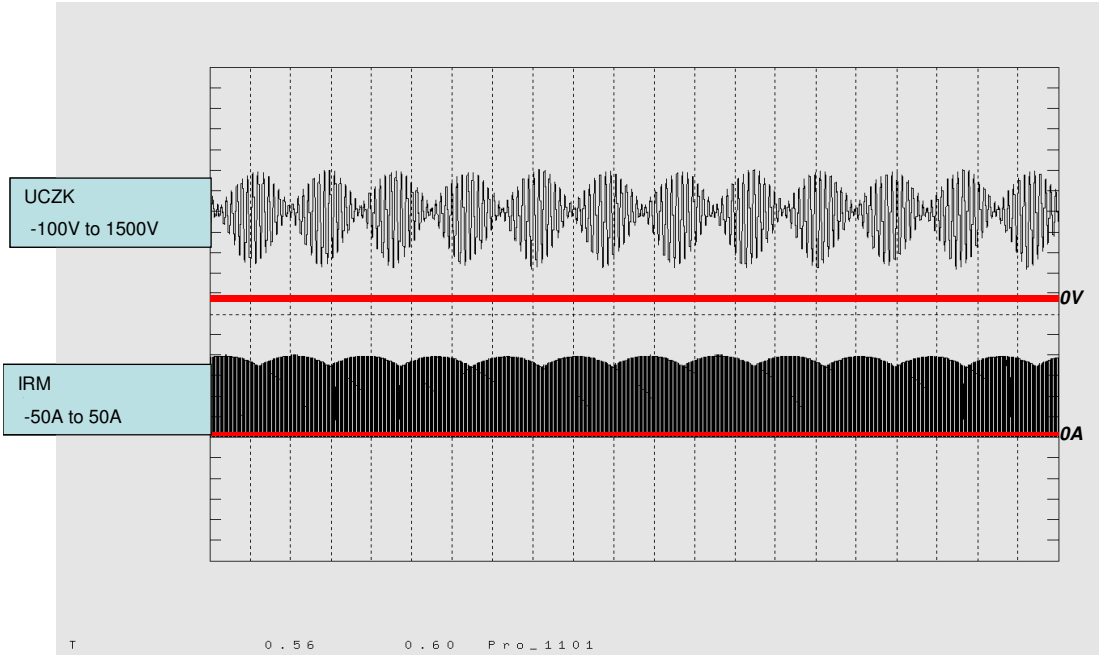


Fig. 5.31: Intermediate current I_{RM1} feeding the PWR and intermediate voltage at an R_{sce}=96

These fluctuations influenced the output line-voltage U_{UV} of the inverter, but not the output current I_{MOT} (Fig. 5.32).

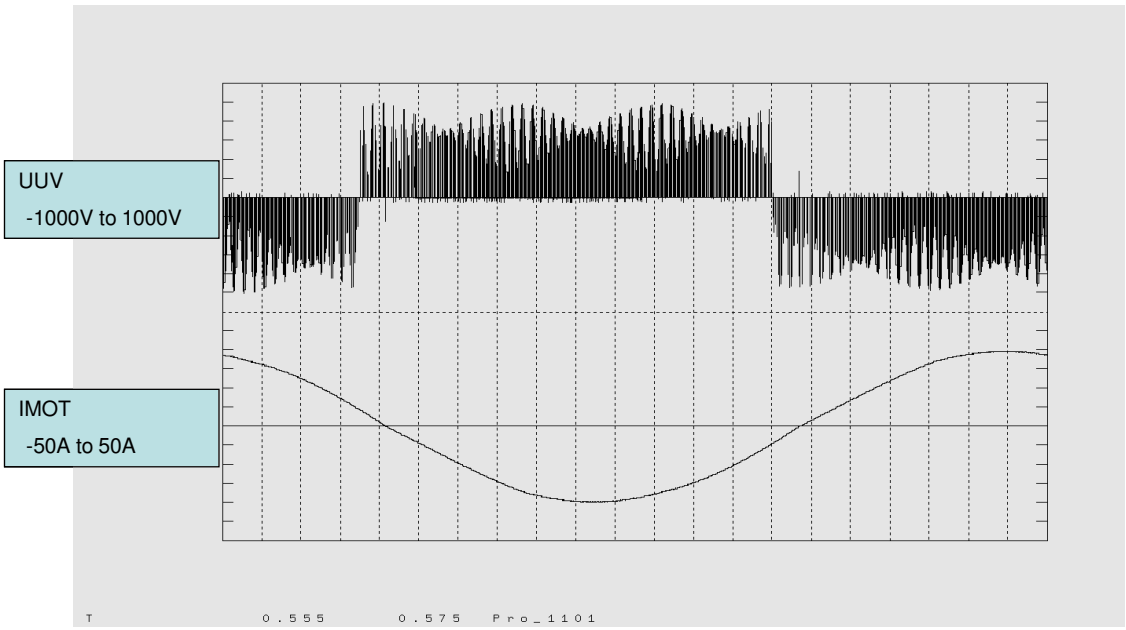


Fig. 5.32: Output current I_{MOT} and output voltage U_{UV} at an R_{sce}=96

There was a significant improvement when the inductors were assigned the values $L_{NETZ} = 2.0\mu\text{H}$ and $L_{NF3E} = 24.4\mu\text{H}$. An R_{sce}=1164 resulted. The F3E currents showed a significant improvement in shape and in the range of their values. The range of values was similar to the operating conditions outside resonant frequencies (Fig. 5.33).

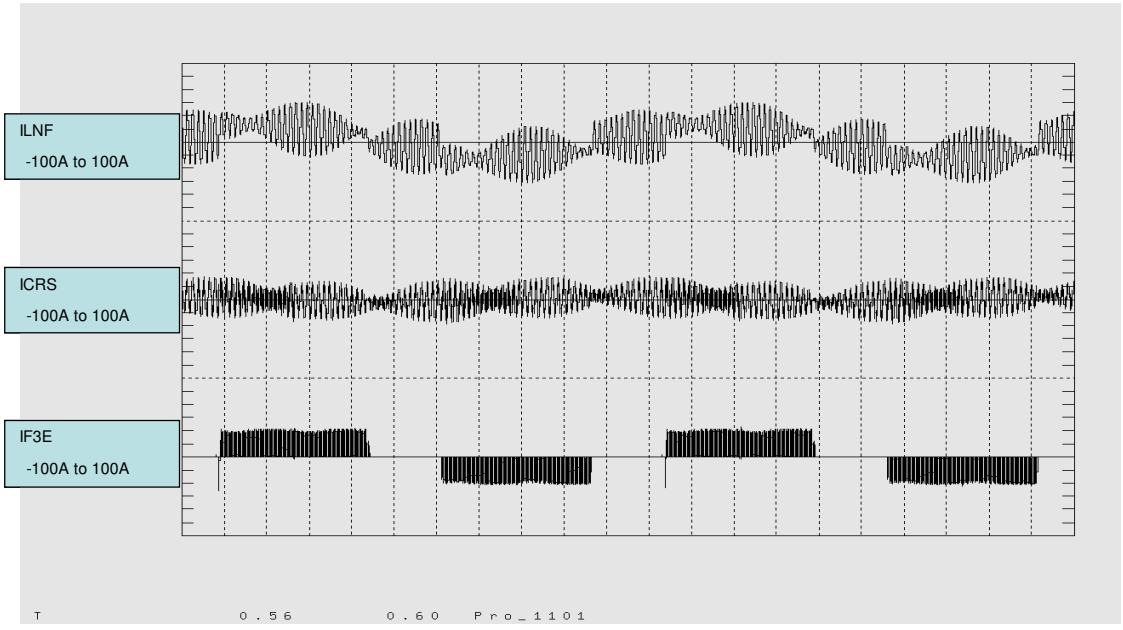


Fig. 5.33: The F3E currents at an R_{sce}=1164

The F3E current I_{F3E} again showed a typical 120 degree block-like shape without any perceptible distortions. The changes in shape of the currents I_{LNF} and I_{CRS} also affected the filter voltage U_{CRS}. The voltage was still slightly distorted by higher harmonics (Fig 5.34).

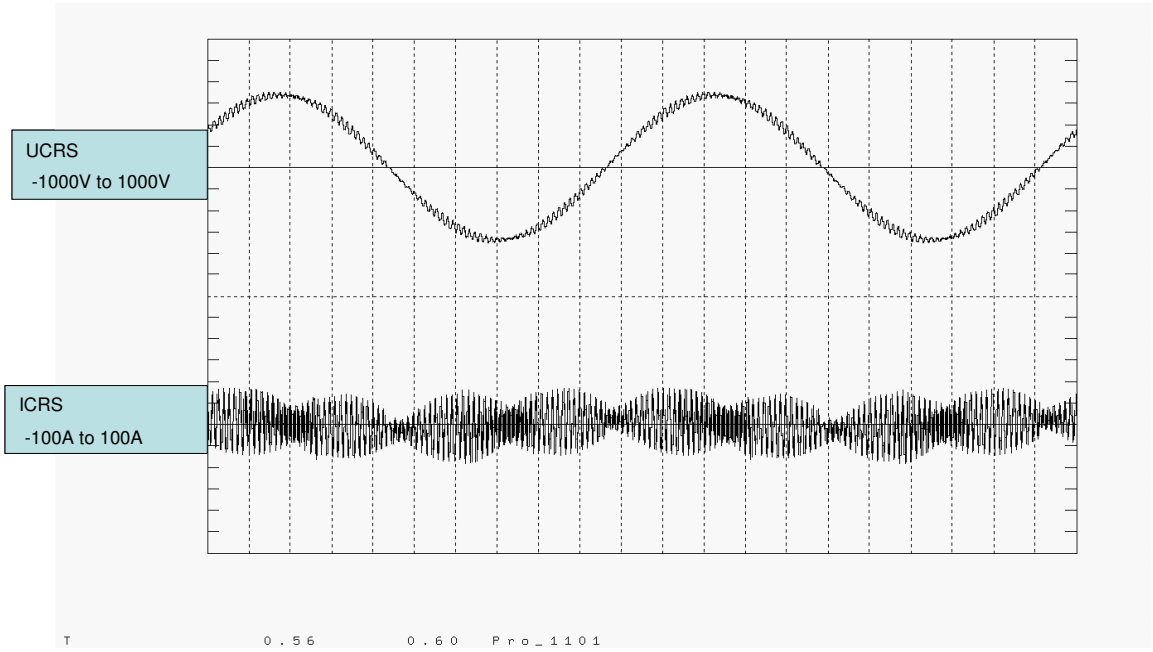


Fig. 5.34: Shape of filter voltage U_{CRS} and current I_{CRS} at an R_{sce}=1164

This distortion by higher harmonics was also discernible in the shape of the intermediate voltage U_{CZK} (Fig. 5.35). These superimposed higher harmonics, however, did not influence the output voltage and current of the inverter (Fig. 5.36).

The shapes of the currents I_{LAF} and I_{NETZ} were similar to the ones under non-resonant conditions and are not shown here.

5.3.6 Analysis of the higher harmonics spectra

An analysis of the higher harmonics spectra in the 0Hz to 1.5kHz range was performed. Figure 5.37 shows the F3E currents I_{LNF}, I_{F3E},and I_{CRS} at an R_{sce}=96.

Contrary to the distribution of the higher harmonics previously examined, a significant deviation from the distribution typical for B6 rectifier circuits exhibited by the F3E

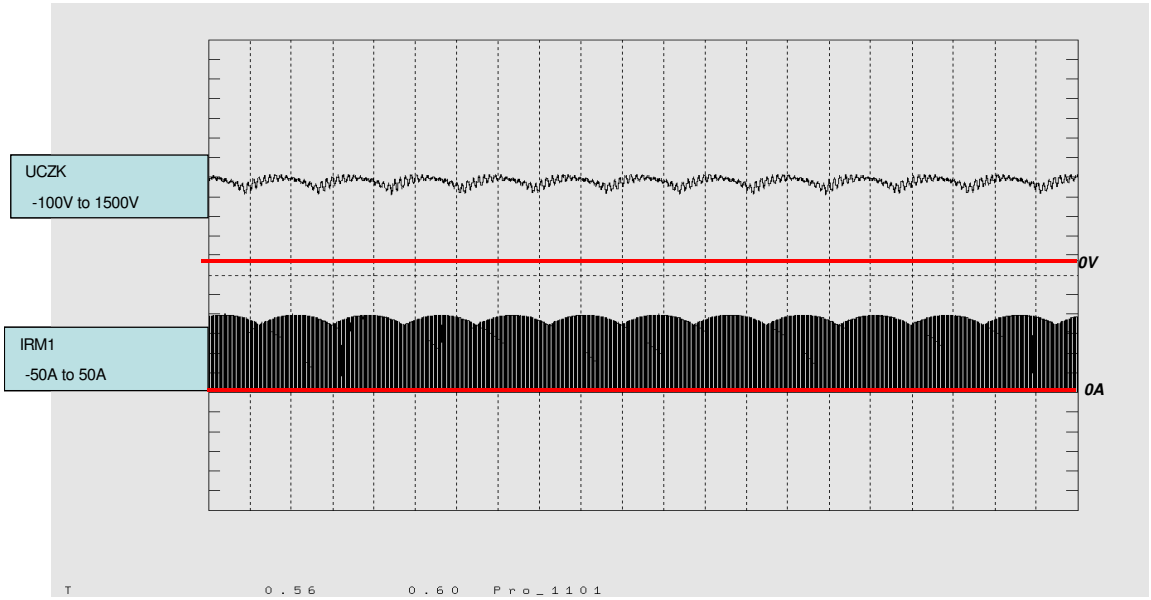


Fig. 5.35: Intermediate PWR current I_{RM1} and intermediate voltage U_{CZK} at an R_{sce}=1164

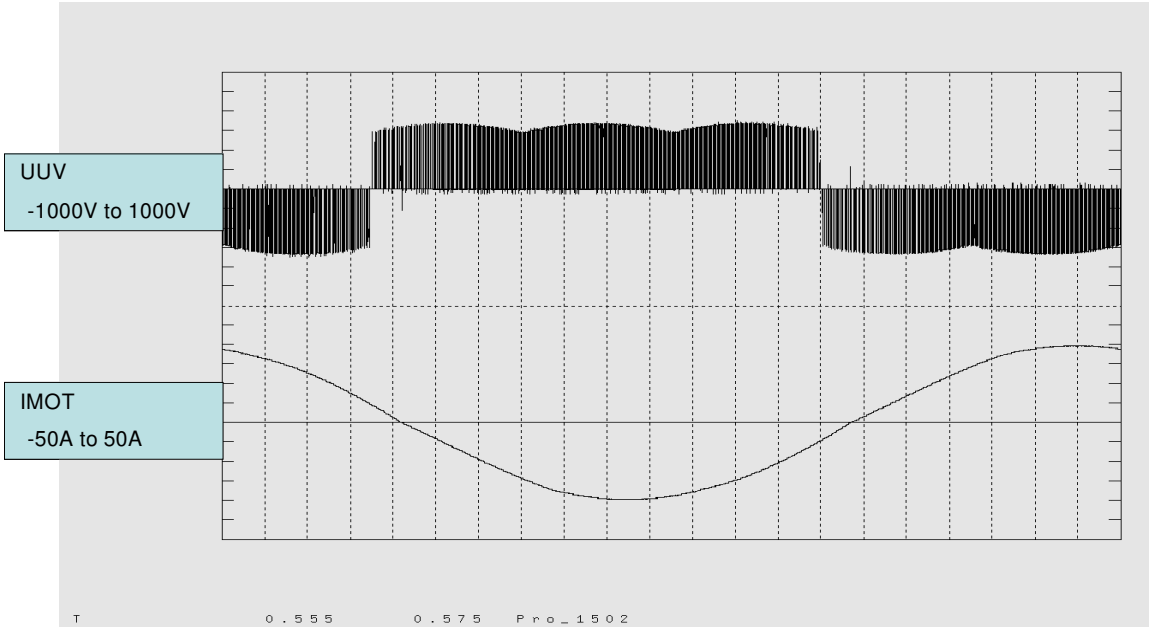


Fig. 5.36: Output current I_{MOT} and voltage U_{UV} at an R_{sce}=96

occurred. The currents I_{LNF} and I_{F3E} showed amplitudes of the 5th and 7th harmonics, which were significantly smaller than that observed in the earlier case studies. The 120 degree block of the F3E current has now a very limited influence on the input current. The spectra at an R_{sce}=1164 look more typical of the distribution expected from the F3E. The amplitudes of the 5th and 7th harmonics again reached values around 20% and 13%, respectively of the fundamental oscillation (Fig. 5.38).

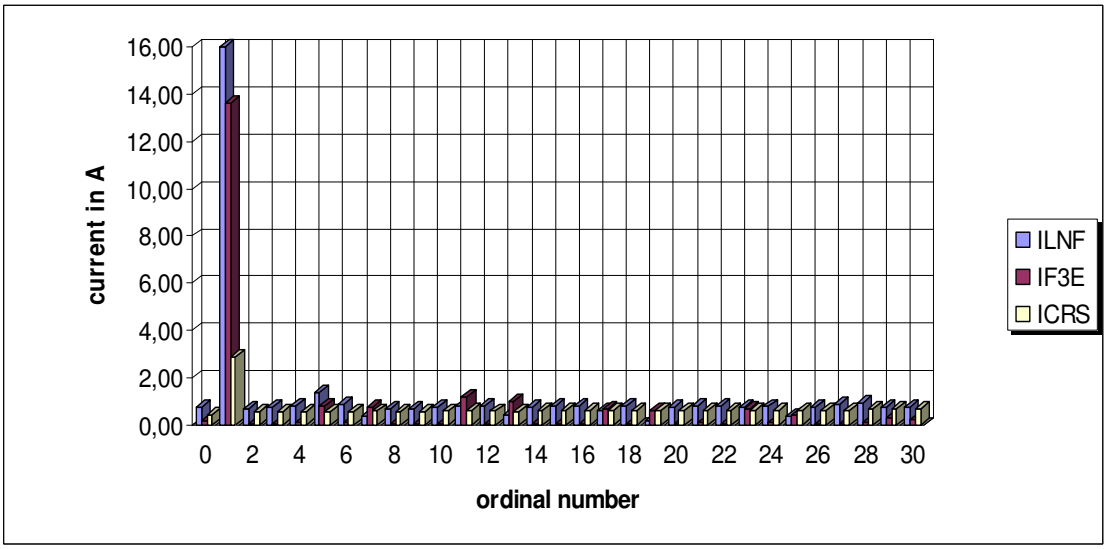


Fig. 5.37: Higher harmonics spectra of I_{LNF}, I_{F3E}, and I_{CRS} at an R_{sce}=96

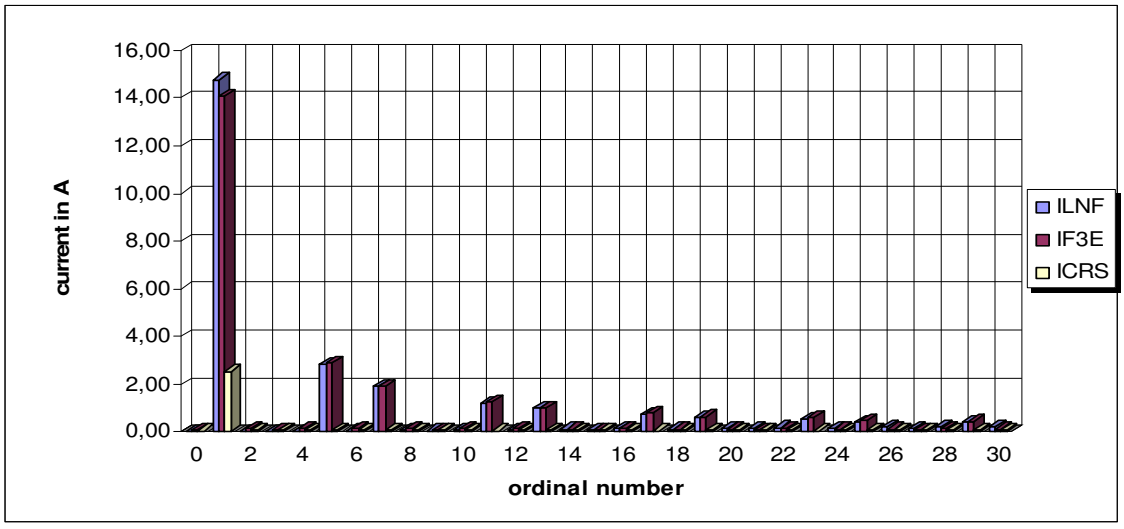


Fig. 5.38: Higher harmonics spectra of the three F3E currents I_{LNF}, I_{F3E}, and I_{CRS} at an R_{sce}=1164

In Fig. 5.38, the filter current I_{CRS} showed only its fundamental component as opposed to Fig. 5.37, which represents conditions with an R_{sce}=96 and where all higher harmonics up to 3rd order were present.

Even more pronounced are the differences of the spectra in the frequency range from 3.5kHz to 4.5kHz. Figure 5.39 shows the spectra of the currents I_{LNF}, I_{F3E}, and I_{CRS} at an R_{sce}=96. The range of amplitudes in Fig. 5.39 was almost one magnitude higher than the range shown in Fig. 5.40, which depicts the analysis for an R_{sce}=1164.

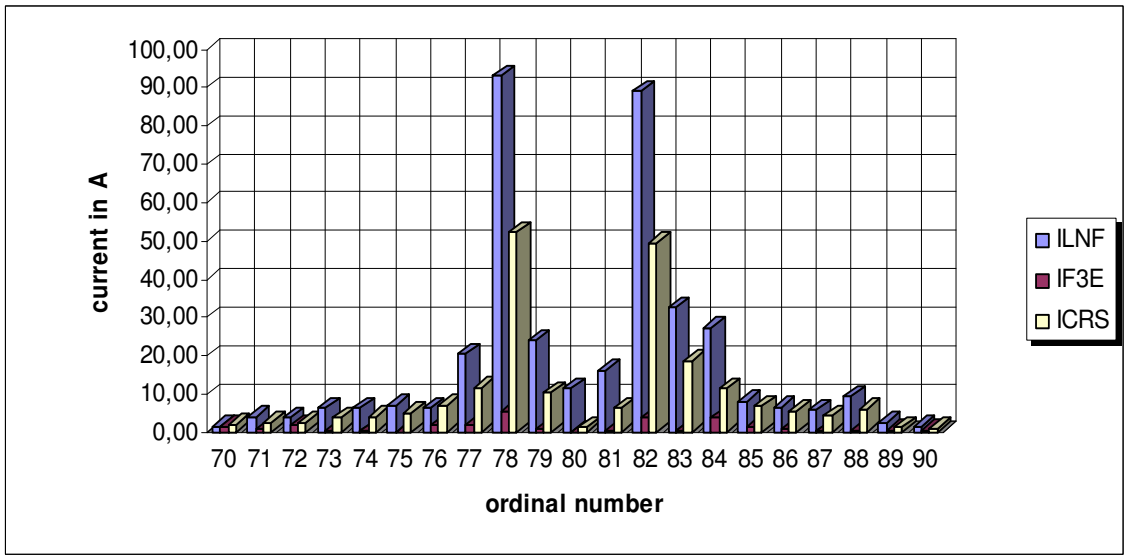


Fig. 5.39: Higher harmonics spectra of the F3E currents I_{LNF}, I_{F3E}, and I_{CRS} at an R_{sce}=96

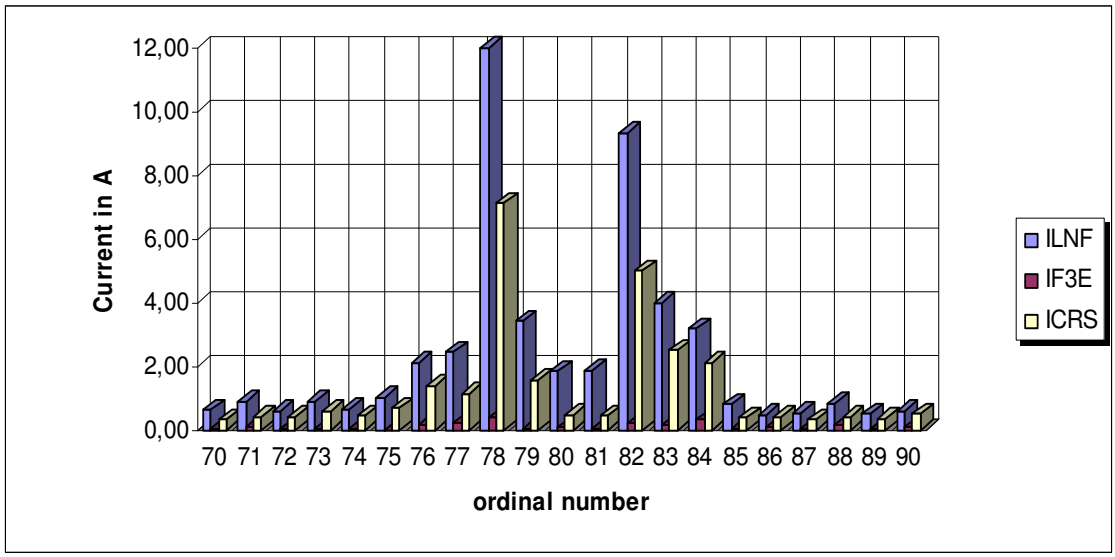


Fig. 5.40: Higher harmonics spectra of the F3E currents I_{LNF}, I_{F3E}, and I_{CRS} at an R_{sce}=1164

The difference can be seen even better through the direct comparison of the higher harmonics spectra of the current ILNF at an R_{sce} of 96 and 1164, respectively (Fig. 5.41).

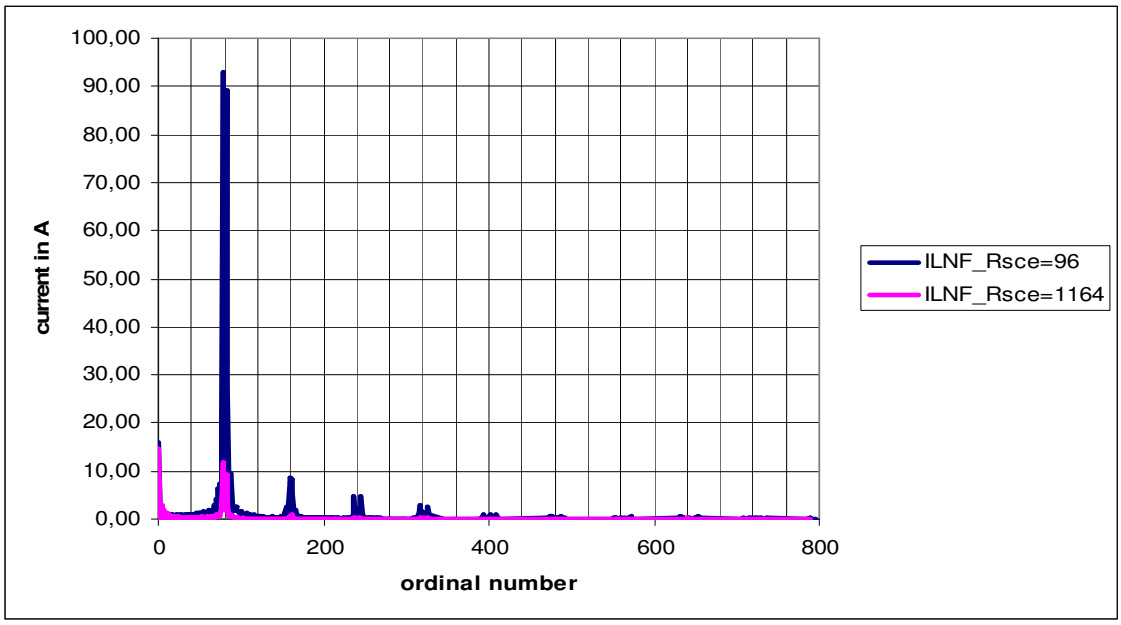


Fig. 5.41: Higher harmonics spectra of I_{LNF} at R_{sce}=96 and R_{sce}=1164

The fundamental component in both cases shows almost the same amplitude of about 16A. At an R_{sce}=96, however, higher harmonics at 4kHz and multiples of that frequency were significantly increased by a factor of almost eight as compared with that of an R_{sce}=1164. It is also about six times higher than the fundamental component of the F3E input current. Thus, the oscillating current of the resonant circuit dominates I_{LNF} and overloads the F3E filter.

This finding reveals that increasing the R_{sce} improves the shape and behaviour of the currents. This is in accordance with the results presented so far, and is supported by Fig. 5.42 showing the effective value of the filter current I_{CRS} as a function of R_{sce}. At an R_{sce}=750, the effective value of I_{CRS} was still higher than 15A.

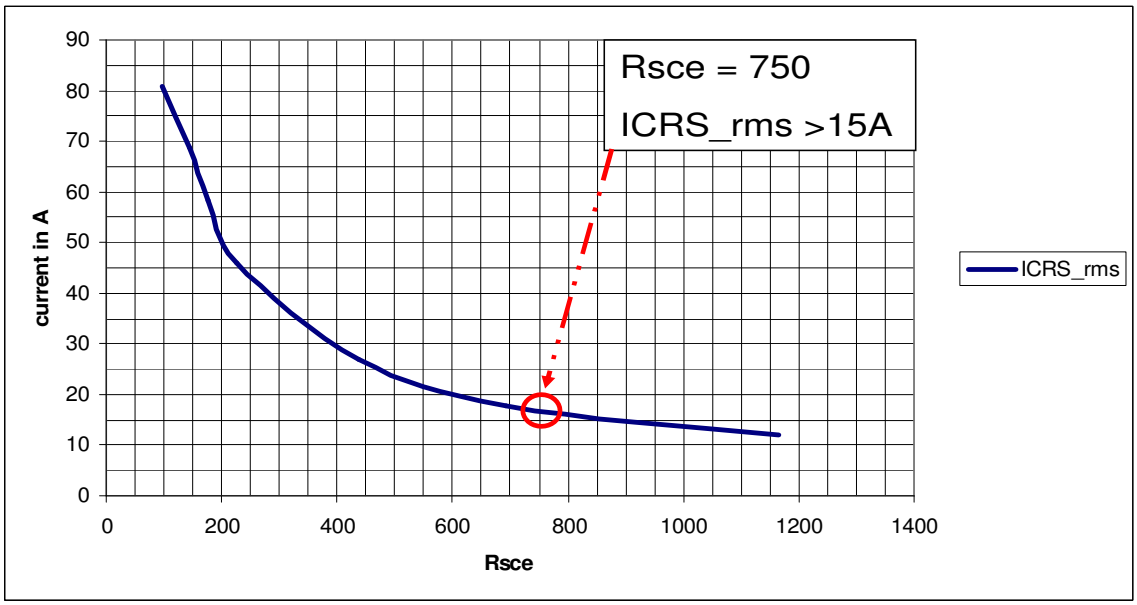


Fig. 5.42: Effective value of the filter current I_{CRS} as a function of R_{sce}

Since the filter current I_{CRS} influences the filter voltage U_{CRS} (Chapter 5.3.3), the effective value of this voltage as a function of R_{sce} was analysed. The result is shown in Fig. 5.43. The voltage decreased with an increase of R_{sce}, but the overall value of the voltage was higher as compared with that in Fig 5.42.

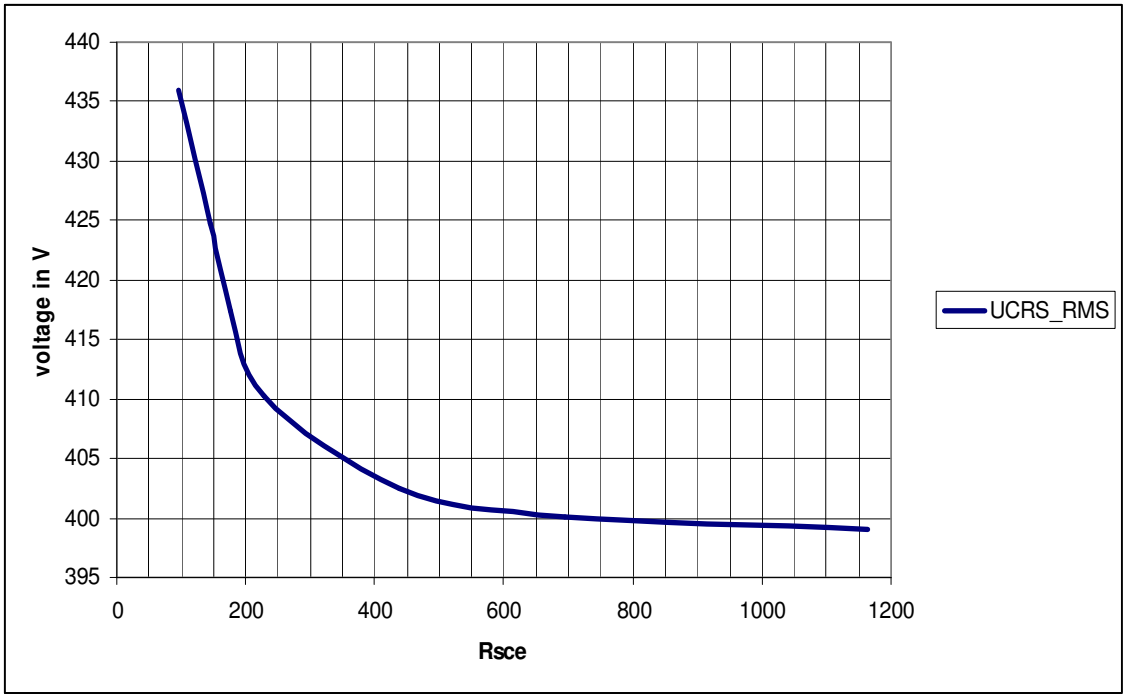


Fig. 5.43: Filter voltage U_{CRS} as a function of R_{sce}

In the case of R_{sce}=96, the filter voltage reached a value of 436V, which is slightly below the tolerances allowed at a mains voltage of 400V. This, however, is insignificant compared with the high currents in that case, which already prohibited this mode of operation.

6 Conclusions

The study was conducted to simulate a functioning and realistic model consisting of AFE, F3E, the associated filter components and the connecting power grid segments.

The F3E_PWR Model

The examination of the F3E_PWR model focused on the influence of the dampening resistor R_{CREIHE} of the filter on the model behaviour. The main purpose was to determine whether this resistor can be omitted completely or only under specific circumstances. On the basis of the preliminary analysis of the alternate circuit diagrams, it can be concluded that the reduction of the dampening resistor or its omission would create additional stress for the filter components. This is attributed to the higher harmonics caused by the F3E. The simulations also revealed that operation without a dampening resistor is theoretically possible, but not advisable. An excitation of the parallel resonant circuit by the switching frequency of the PCI has to be avoided under any circumstances. In case of excitation, the filter elements and the section of the power grid between the filter and the F3E incur additional stress due to the increased currents in case of resonance. This will not damage the F3E itself, but might result in a general system failure.

The AFE_F3E Model

Based on the results of the first simulations, it can be concluded that a small influence of the AFE on the F3E filter currents, even without exciting any points of resonance, occurs. Because of the capacitive properties of the F3E filter, it constitutes only a small resistance to the currents in the frequency range examined.

Series resonant circuit of the AFE_F3E model

The switching frequencies can excite the series resonant circuit, consisting of the filter components and the F3E mains components. As a consequence, the majority of the higher harmonics content close to the switching frequency is conducted by the F3E filter and its associated grid section.

The line current I_{LNF} of the F3E and the filter current increase; while, the input current of the F3E remains almost unchanged. It can be concluded that the filter and grid elements are stressed by the currents in this case. The F3E itself is not affected but due to the high currents, safety measures like fuses might be triggered, leading to a system shutdown.

Parallel resonant circuit of the AFE_F3E Model

The filter current in case of an R_{SCE} of 96 showed a significant ripple, distorting the filter voltage. Due to the small intermediate capacitor, this distortion has repercussions on the intermediate voltage of the PCI connected to the F3E. The output voltage of the PCI also showed distortions.

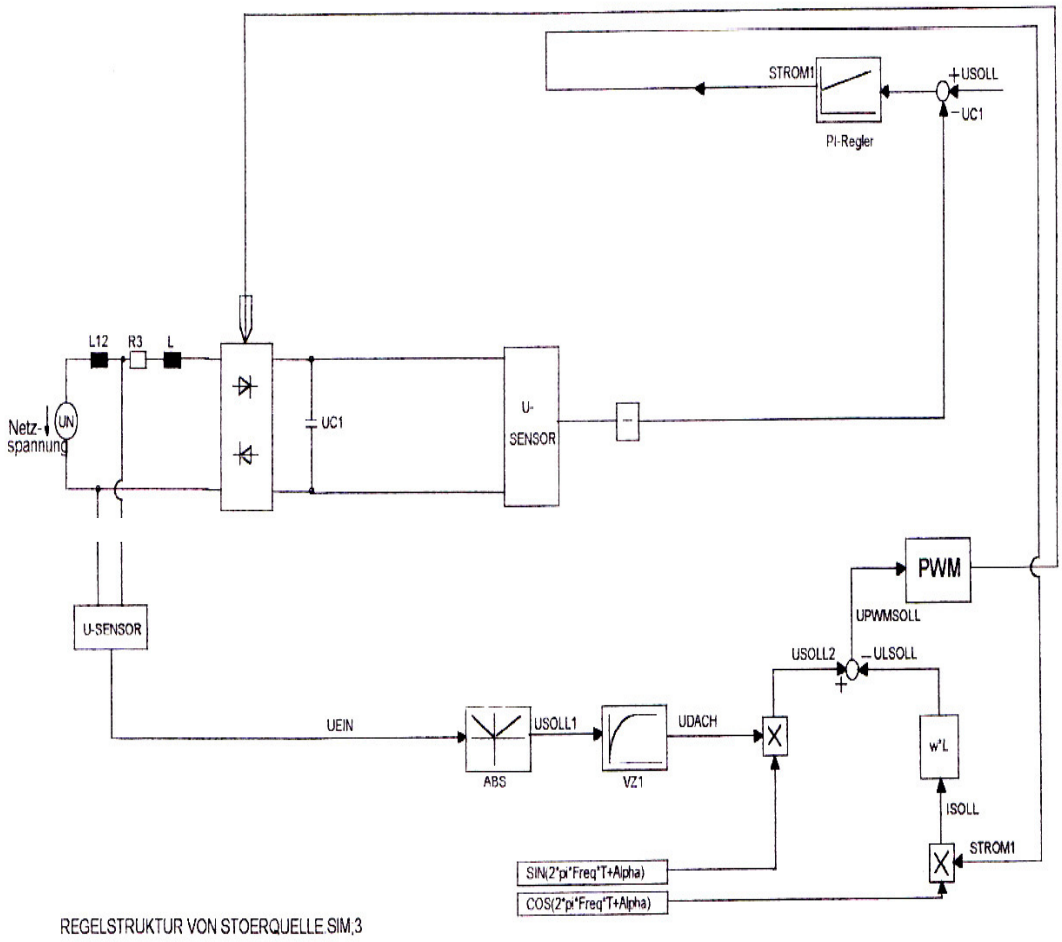
This influence of the filter current is noticeable in the effective values of the filter voltage. The voltage was below the limit stipulated by regulation, which sets a tolerance of +10% of the nominal supply voltage of 400V. In reality, fluctuations can occur, increasing ultimately the calculated value of the filter voltage. This in turn, can lead to a voltage increase affecting the semiconductors of the F3E, leading to their destruction and the disabling of the F3E.

The quality of the parallel resonant circuit was higher than one in case of moderate values of R_{sce}. In case of R_{sce} values higher than 750, the current of the filter capacitors was equal to or higher than the fundamental current of the F3E. This is due to the oscillating current of the parallel resonant circuit. At lower values of R_{sce} (<100), the oscillating current was about six times higher than the fundamental component of the F3E input current.

The F3E filter may be overloaded by ripple currents of an AFE operated on the same power grid. The effect of parallel resonance may further increase the filter currents significantly.

Appendix I

Control structure of an AFE



REGELSTRUKTUR VON STOERQUELLE SIM.3

Apendix II

List if model variables and signals

AFDRz	Delta Carrier for the AFE
ALPHA	Zero phase angle of the first phase of the reference sinusoidal voltage for the AFE
ALPHA3	120° phase angle for the reference sinusoidal voltage for the AFE
AREG1-AREG3	Boolean Output of the AFE PWM comparator
AREG10-AREG 30	Boolean Output of the AFE PWM comparator of the last calculation step
AUSST	Duty cycle
BPHI0	Zero phase angle of the first phase of the reference sinusoidal voltage for the PCI
BPHI3	120° phase angle for the reference sinusoidal voltage for the PCI
DEIN1-DEIN6	Timer Variable for the interlock MIND1-MIND6
DFEIN1- DFEIN6	Timer Variable for the interlock MINDF1-MINDF6
DIF1-DIF3	Analog Output of the PCI PWM comparator
DR	Delta carrier for the PCI PWM
DRDACH	Amplitude of the delta carrier for the PCI PWM
DRFREQ	Frequency of the delta carrier for the PCI PWM
DRSTEIG	upward gradient of the delta carrier for the PCI PWM
F3F1-F3F6	Start signal for the MINF1-MINF6 timer
FB1-FB6	Starting time of the timer FMONO1-FMONO6
FEIN1-FEIN6	Starting time of the timer MINF1-MINF6
FMONO1-FMONO2	Timer output of the switch on delay timer
ISOLLB1-ISOLLB3	90° phase shifted current in the AFE control for the three phases
KI	Amplification of the I-controller of the AFE control
KP	Amplification of the P-controller of the AFE control
KPWM	Conversion factor for the AFE PWM-voltage
MIND1-MIND6	Interlock signal for the switch on signal SEIP1-6

MINDF1-MINDF6	Interlock signal for the switch on signal SEIF1-6
MINF1-MINF6	Interlock signal for the suppressing a to short switch on signals(F3E)
MINT1-MINT6	Interlock signal for the suppressing a to short switch on signals(PCI)
MOF3E1-MOF3E6	Start signal for the FMONO1-FMONO6 timer
MOWR1-MOWR6	Start signal for the PMONO1-PMONO6 timer
MSF1-MSF6	Result of the Boolean operation about the F3E switching rule
MSFA1-MSFA6	Result of the Boolean operation about the F3E switching rule of the last calculation step
OMEGA	Angular frequency for the reference voltages
PFR	Phase shift angle for the EMF
PHIL (3)	Phase shift angle for the PCI output current
PHIN (3)	0°,-120° and 120° phase shift for the PCI three phase output current
PMONO1-PMONO6	Timer output of the switch on delay timer
PTAU	Delay time for the MINT1-MINT6 timer
PVER1-PVER6	Interlock signal for the switch on signal SEIP1-6
SAF1-SAF6	Switch-of signal F3E semiconductors
SAF10-SAF60	Switch-of signal F3E semiconductors of the last calculation step
SAP1-SAP6	Switch-of signal PCI semiconductors
SAP10-SAP60	Switch-of signal PCI semiconductors of the last calculation step
SEIF1-SEIF6	Switch-on signal F3E semiconductors
SEIF10-SEIF60	Switch-on signal F3E semiconductors of the last calculation step
SEIP1-SEIP6	Switch-on signal PCI semiconductors
SEIP10-SEIP60	Switch-on signal PCI semiconductors of the last calculation step
SEIN	Switch-on signal used in the example
SAB	Switch-off signal used in the example

SINDACH	Amplitude of the sinusoidal reference voltage of the PCI
SINFREQ	Frequency of the sinusoidal reference voltage of the PCI
STROM1	Current reference value
STS10-STS30	PWM signal for the PCI from the last calculation step
STS1-STS3	PWM signal for the PCI
TAU	delay time for the switch on timer
TEIN1-TEIN6	Starting time of the timer MINT1-MINT6
TS1	Minimum switch on time
TX	Time of the algebraic sign change for the PWM delta voltage upward
UDACH	Adjusted value for the voltage triangle of the AFE control
UEIN	momentary Voltage value of the first phase
UL1SOLL	Voltage of the AFE inductor in the first phase for the voltage triangle (AFE)
UL2SOLL	Voltage of the AFE inductor in the second phase for the voltage triangle (AFE)
UL3SOLL	Voltage of the AFE inductor in the third phase for the voltage triangle (AFE)
ULMOT	Voltage of the PCI Load inductor (motor load)
UPWID	Output voltage of the PCI for the motor voltage triangle
UPWM1	Reference voltage for the AFE PWM first phase
UPWM2	Reference voltage for the AFE PWM second phase
UPWM3	Reference voltage for the AFE PWM third phase
UPWR	Output voltage of the PCI including the voltage over the load resistor
URMOT	Voltage over the load resistor
USMOT	Amplitude of the PCI load EMF
USOLL	Reference voltage of the AFE intermediate voltage
USOLLA	Rectified value of momentary Voltage value of the first phase for the AFE control
USOLLB1- USOLLB3	Vector of the AFE voltage triangle representing
UST1-UST3	Reference voltage of the PCI PWM
VH & VS	Variable for the algebraic sign change in the delta voltage

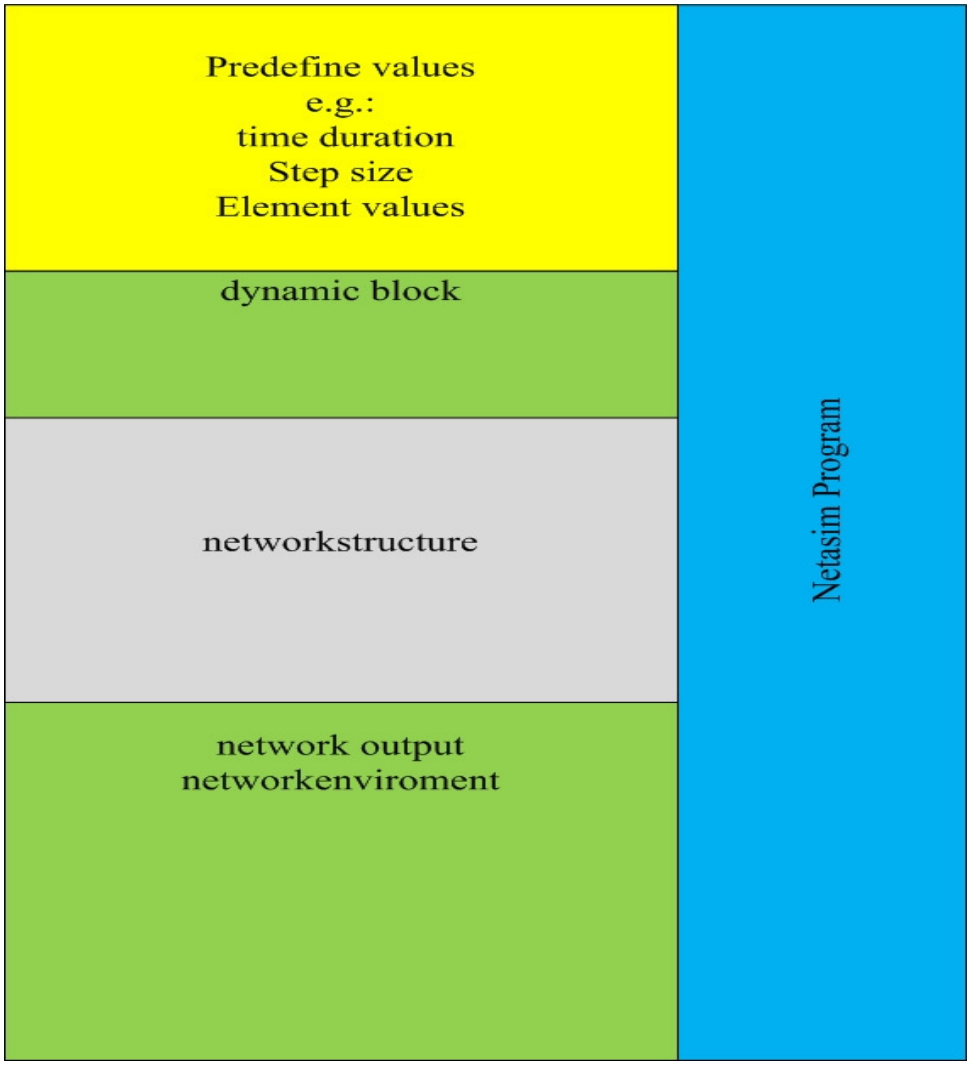
	algorithm
Z0F1-Z0F6	switching status of the F3E Semiconductors
Z0T1-Z0T6	switching status of the PCI Semiconductors
ZF10-ZF60	switching status of the F3E Semiconductors in the last calculation step
ZT10-ZT60	switching status of the PCI Semiconductors in the last calculation step

Apendix III

Netasim

Netasim is a simulation tool specially designed to simulate power electronics applications. It is also possible to model systems components not representing electrical circuits, but mechanical or thermal components.

Netasim uses a pre-processor which translates a circuit into a structural description for effect propagation and describe which part of a system affects another part quantitatively and qualitatively. The pre-processor is called ASIM3 and is based on the programming language Fortran. This programming language is also used to describe models of systems and circuits. Since Netasim is not equipped with a graphical user interface, every system to be modelled has to be described using the ASIM3 syntax.
Netasim provides a dynamically operating block, designed to simulate electrical circuits. This dynamically operating block can be incorporated into the structural description of the system to be modelled. This description method is well-suited for the technical systems examined in this thesis.



Structure of a Netasim Program

Figure above shows the structure of Netasim. The top-most part of the figure shows the section for defining global simulation parameters and variables. Initial values required for the mathematical algorithms implemented are also calculated there. Netasim provides the following algorithms for evaluating differential equations:

- Runge-Kutta-Algorithm 2.order (RK2)
- Runge-Kutta-Algorithm 4.order (RK4)
- Second order algorithm with dynamical increment adjustment (DI2)

In cases where no algorithm is selected, Netasim defaults to RK2. In this thesis, however, the DI2 algorithm was used. This algorithm requires the evaluation of calculation errors due to a possible increase in the value of the calculation steps.
Netasim provides for the output of results in files and as graphical data. However, it has to be decided which values which should be outputted at the beginning of each simulation run. Netasim also includes a pos-processor for Fast Fourier Transformation.

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